OPTi Inc.
888 Tasman Drive
Milpitas, CA 95035
(408) 486-8000
Fax: (408) 486-8001

Application Note (OPTi Confidential)

Product Name: Viper Xpress+ Chipset

Title: PCB Layout Reference Guide

Date: January 16, 1997

Scope

This document provides the PCB (printed circuit board) designer with an overview of layout methodologies, issues, and guidelines when using the Viper Xpress+ Chipset (82C576, 82C578, and 82C579).

Discussion

Viper Xpress+ is an advanced Pentium® processor class chipset capable of extracting the best memory and PCI performance on a personal computing system. To minimize signal integrity issues and routing complexity, much effort has been put into logically assigning each pin of each device in the Viper Xpress+ Chipset. In the OPTi recommended placement of a PCB (refer to Figure 1), the various subsystem buses flow in a straightforward fashion between CPU, cache, chipset components, IDE, and PCI.

Placement of System Components

Key components of the Viper Xpress+ system should be placed as per the following guidelines. This placement consists of:

- Baby AT form factor.
- 4-layer design with one VCC, one GND, and two signal routing layers.
- Pentium Socket-7™, power planes and cooling as per Pentium Processor Flexible Motherboard and Socket-7 specifications.
- 82C579 and DRAM SIMMs placement in such a way that memory interface routing is minimized.
- IDE interface to have termination placed before the connector.
- IDE data buffers to IDE connectors within 1 inch distance.

Routing Priority

Best placement coupled with tight routing (minimum trace length) of nets will give extremely reliable production quality boards. The following order of priority should be applied while trading off the signal priorities during routing:

- CPU clock, chipset clocks, SDRAM clocks (all at 66MHz), and PCI clocks (33MHz).
- Processor interface signals: ADS#, R/W#, and BRDY#.
- Cache RAM connections: ADSC#, ADV#, GWE#, BWE#, and TAGWE#.
- DRAM signals: MA lines, RAS#, CAS#, SDRAS#, SDCAS#, and DWE#.
- Viper Xpress+ 82C576 (DBC) to 82C578 (IPC), and 82C569 (SYSC) control signals: All control signals must have a 10Ω series resistor at the driving agent side.
- PCI bus signals.
- IDE bus control signals and IDE data bus.

Layout Guidelines

1. VCC/GND traces at 25mils minimum and ±5V/12V traces at 50mils.
2. VCC pin of ICs should be connected first to the VCC of its DECAP and then to the VCC plane. Direct connections to the plane are not permitted.
3. DECAPs should be placed as close to ICs as possible.
4. Battery power pins should be at least 25mils.
5. All clock lines shall have minimum 16mil clearance on each side.
6. All clock lines of similar groups (CPU, PCI CLK) will have equal trace length (±0.25 inches). ±1.0 inch difference in trace length will result in +160ps skew of the clocks.
7. Avoid daisy chaining series terminated signals.

8. The following are critical signals in a Viper Xpress+ design. Keep them as short as possible:
   - All clock signals.
   - All CPU bus control signals.
   - Connections to the clock generator and clock buffers.
   - All cache control signals from 82C579.
   - Tag lines.
   - Memory control signals.
   - 82C579-to-82C576 control signals.
   - PCI control signals.
   - IDE primary and secondary DATA and control signals.

8. No signal routing allowed on power and ground planes.

9. No reset signal should be routed within 1 inch of the edge of the board.

10. SENSE input to the VRM module should be picked from the middle of the VCORE plane. The resistor should be also in the middle of VCORE plane.

11. The Viper Xpress+ boards shall meet the Socket-7, VRM and Intel® Flexible Motherboard electrical and mechanical specifications.

Layout Precautions

1. All series termination resistors should be within 1 inch of the driving agent.

2. Test connectors should be placed in such a way that they do not add length on critical control signals.

3. Jumpers on critical signals should be placed next to the ICs.

Trace Length Guidelines

- Pentium CPU to HA latch: under 3.5 inches
  - CPU to 82C579 HA lines: under 5 inches
  - Total HA trace length: 3.5 + 5 = 8.5 inches
  - All memory control signals: under 6 inches
  - HD from CPU to L2: under 5 inches
  - HD from L2 to 82C576: under 2 inches
  - L2 control signals from 82C579: under 6 inches
  - MD bus on board: 8 inches
  - CPU clocks: all 66MHz clocks should have equal trace lengths ±0.25" allowed: Maximum trace length 2.5 inches.
  - PCI clocks: all 33MHz PCI clocks should have equal trace lengths ±1.0" allowed. Maximum trace length on board 3.0 inches.
- Voltage Planes
  - Four power planes: 3.3V, VCORE, 5.0V and 3.3V/5.0V. DRAM power plane: Follow Socket-7 specification and routing guidelines.
- VCC and GND Planes
  - No signals to be routed on the power planes.
  - Power plane splits to avoid small power islands.
  - Adequate shorting jumpers for power plane shorting (e.g. VCORE to VCC3 or VIO externally).
- Trace width and clearance
  - On 4-layer board use 6x6mil routing for signal routes.

Performance Considerations

The Viper Xpress+ Chipset is designed to provide the best memory, cache and PCI master timings. In order to achieve this timing, the layout and signal buffering must be optimum on a system board.

To achieve 5-2-2-2 memory timing, the MA and RAS lines for Bank 0 SIMM pair must be driven directly by the 82C579 memory controller where as Bank 1 and Bank 2 SIMM pairs can be driven through a 74F244 address buffer which will result in a 6-2-2-2 timing in those banks.

Figure 1 Recommend Viper Xpress+ Sample PCB Layout