82C495XLC

82C495XLC/82C206 PC/AT Chip Set

Data Book

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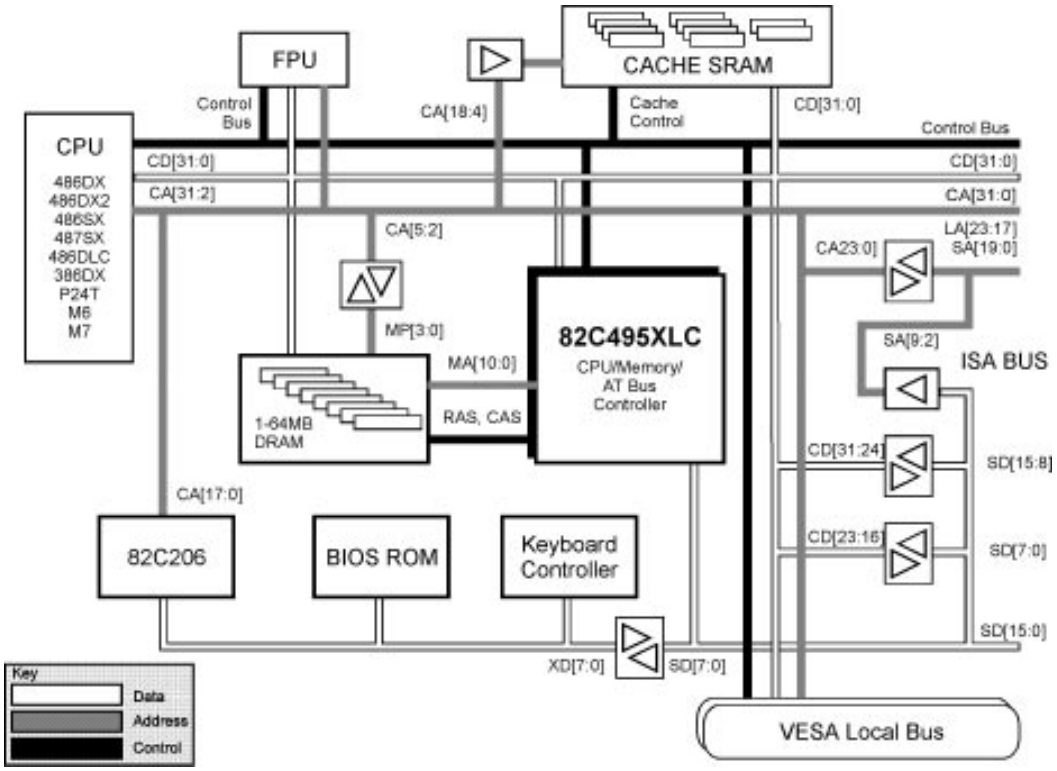
82C495XLC/82C206 PC/AT Chip Set

1.0 Features

- Low cost, low power, CMOS Technology
- Supports 386DX, 486 DX/DX2/SX CPUs as well as Intel P24T and Cyrix Cx486S/S2 and Cx486DX/DX2 CPUs
- One 160-pin CMOS Plastic Flat Package (PFP), one 84 pin PLCC (or one 100-pin PFP)
- Internal buffers and termination to reduce external parts count
- Copy-Back Direct-Mapped Cache: 32/64/128/256KB for 386, and
  64/128/256/512KB for 486
- Up to 10% performance enhancement from write-through cache scheme
- Supports 2-1-1-1 or 3-2-2-2 cache cycles
- On-chip comparator determines cache hit/miss
- Up to 64MB of local high-speed, page mode DRAM memory space
- Burst line fill during cache read-miss
- Control of one non-cacheable region
- Shadow RAM support for system, video and adapter card BIOS
- Optional caching of shadowed video BIOS
- Hidden refresh support to enhance system performance
- Turbo/slow speed selection (386 mode only)
- AT bus clock selectable from CLKI (/6, /5 /4, /3)
- CAS-before-RAS refresh reduces power consumption
- Optional 0 or one wait state for cache write-hit
- 387 coprocessor support for 386 mode
- Internal CD and CA bus pull-up resistors to save components and board real-estate
- Comprehensive VL bus and OPTi high-performance local bus support
- On-chip hardware provides direct support for up to two VL bus master devices

Figure 1-1 System block Diagram



2.0 Overview

The OPTi 82C495XLC is a low-cost two-chip solution offering optimal performance for low to mid range 386/486-based AT systems. The OPTi 82C495XLC is designed for 486 systems running at 20, 25, 33, 40 and 50MHz or 386 systems running at 20, 25, 33 and 40MHz. Please refer to the data book supplied by your third-party source for information on the 82C206.

3.0 Signal Descriptions

Figure 3-1 Pin Diagram

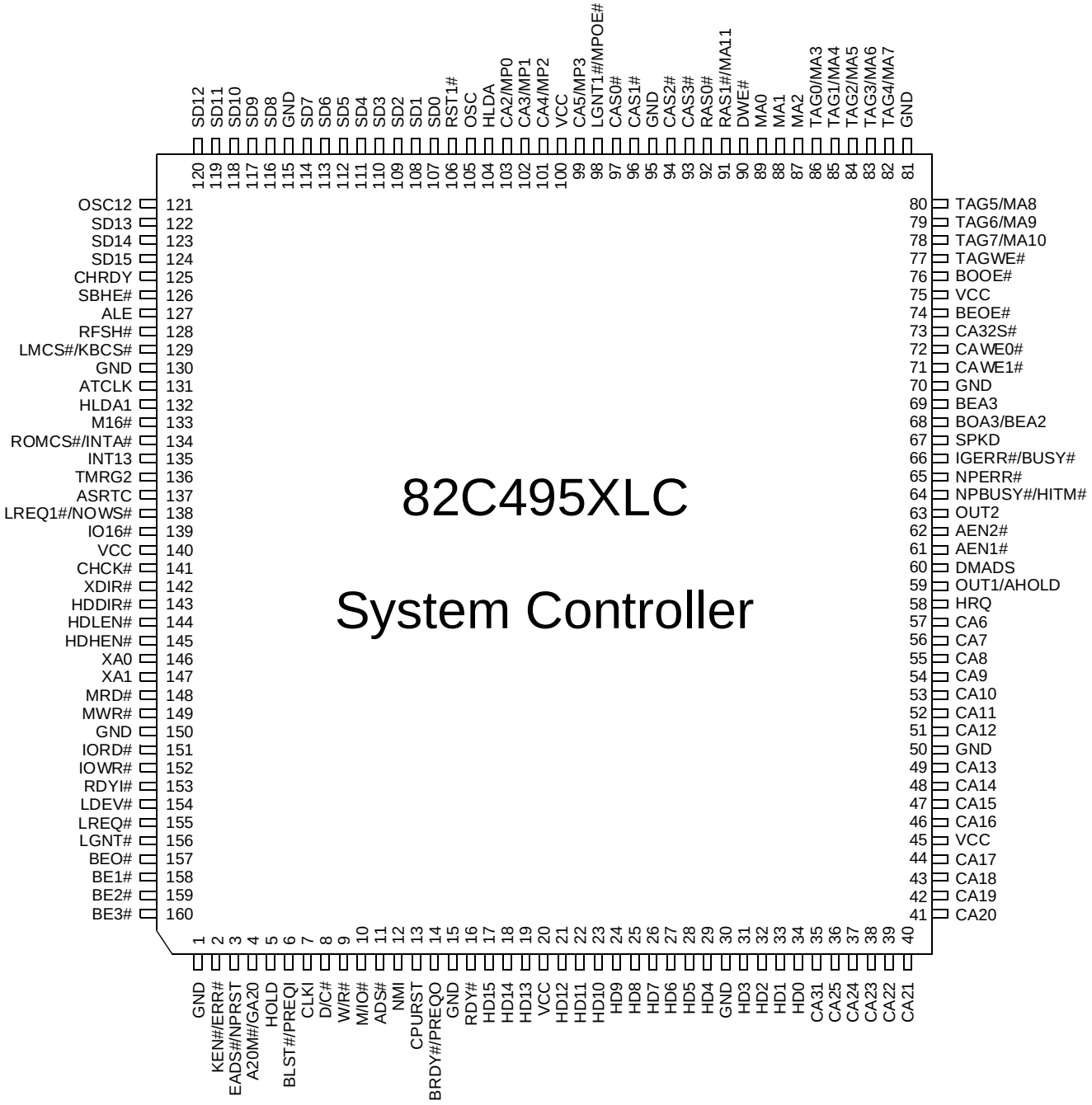


Table 3-1 Alphabetical Cross Reference List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
4	A20M#/GA20	56	CA7	26	HD7	128	RFSH#
11	ADS#	55	CA8	25	HD8	134	ROMCS#/INTA#
61	AEN1#	54	CA9	24	HD9	106	RST1#
62	AEN2#	97	CAS0#	143	HDDIR#	126	SBHE#
127	ALE	96	CAS1#	145	HDHEN#	107	SD0
137	ASRTC	94	CAS2#	144	HDLEN#	108	SD1
131	ATCLK	93	CAS3#	104	HLDA	118	SD10
157	BE0#	72	CAWE0#	132	HLDA1	119	SD11
158	BE1#	71	CAWE1#	5	HOLD	120	SD12
159	BE2#	141	CHCK#	58	HRQ	122	SD13
160	BE3#	125	CHRDY	66	IGERR#/BUSY#	123	SD14
69	BEA3	7	CLKI	139	IO16#	124	SD15
74	BEOE#	13	CPURST	151	IORD#	109	SD2
6	BLST#/PREQI	8	D/C#	152	IOWR#	110	SD3
68	BOA3/BEA2	60	DMADS	135	INT13	111	SD4
76	BOOE#	90	DWE#	2	KEN#/ERR#	112	SD5
14	BRDY#/PREQO	3	EADS#/NPRST	154	LDEV#	113	SD6
53	CA10	1	GND	156	LGNT#	114	SD7
52	CA11	15	GND	98	LGNT1#/MPOE#	116	SD8
51	CA12	30	GND	129	LMCS#/KBCS#	117	SD9
49	CA13	50	GND	155	LREQ#	67	SPKD
48	CA14	70	GND	138	LREQ1#/ NOWS#	86	TAG0/MA3
47	CA15	81	GND	133	M16#	85	TAG1/MA4
46	CA16	95	GND	89	MA0	84	TAG2/MA5
44	CA17	115	GND	88	MA1	83	TAG3/MA6
43	CA18	130	GND	87	MA2	82	TAG4/MA7
42	CA19	150	GND	10	M/IO#	80	TAG5/MA8
103	CA2/MP0	34	HD0	148	MRD#	79	TAG6/MA9
41	CA20	33	HD1	149	MWR#	78	TAG7/MA10
40	CA21	23	HD10	12	NMI	77	TAGWE#
39	CA22	22	HD11	64	NPBUSY#/ HITM#	136	TMRG2
38	CA23	21	HD12	65	NPERR#	20	VCC
37	CA24	19	HD13	105	OSC	45	VCC
36	CA25	18	HD14	121	OSC12	75	VCC
102	CA3/MP1	17	HD15	59	OUT1/AHOLD	100	VCC
35	CA31	32	HD2	63	OUT2	140	VCC
73	CA32S#	31	HD3	92	RAS0#	9	W/R#
101	CA4/MP2	29	HD4	91	RAS1#/MA11	146	XA0
99	CA5/MP3	28	HD5	16	RDY#	147	XA1
57	CA6	27	HD6	153	RDYI#	142	XDIR#

Table 3-2 Numerical Pin Cross Reference List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	41	CA20	81	GND	121	OSC12
2	KEN#/ERR#	42	CA19	82	TAG4/MA7	122	SD13
3	EADS#/NPRST	43	CA18	83	TAG3/MA6	123	SD14
4	A20M#/GA20	44	CA17	84	TAG2/MA5	124	SD15
5	HOLD	45	VCC	85	TAG1/MA4	125	CHRDY
6	BLST#/PREQI	46	CA16	86	TAG0/MA3	126	SBHE#
7	CLKI	47	CA15	87	MA2	127	ALE
8	D/C#	48	CA14	88	MA1	128	RFSH#
9	W/R#	49	CA13	89	MA0	129	LMCS#/KBCS#
10	M/IO#	50	GND	90	DWE#	130	GND
11	ADS#	51	CA12	91	RAS1#/MA11	131	ATCLK
12	NMI	52	CA11	92	RAS0#	132	HLDA1
13	CPURST	53	CA10	93	CAS3#	133	M16#
14	BRDY#/PREQO	54	CA9	94	CAS2#	134	ROMCS#/INTA#
15	GND	55	CA8	95	GND	135	INT13
16	RDY#	56	CA7	96	CAS1#	136	TMRG2
17	HD15	57	CA6	97	CAS0#	137	ASRTC
18	HD14	58	HRQ	98	LGNT1#/MPOE#	138	LREQ1#/ NOWS#
19	HD13	59	OUT1/AHOLD	99	CA5/MP3	139	IO16#
20	VCC	60	DMADS	100	VCC	140	VCC
21	HD12	61	AEN1#	101	CA4/MP2	141	CHCK#
22	HD11	62	AEN2#	102	CA3/MP1	142	XDIR#
23	HD10	63	OUT2	103	CA2/MP0	143	HDDIR#
24	HD9	64	NPBUSY#/ HITM#	104	HLDA	144	HDLEN#
25	HD8	65	NPERR#	105	OSC	145	HDHEN#
26	HD7	66	IGERR#/BUSY#	106	RST1#	146	XA0
27	HD6	67	SPKD	107	SD0	147	XA1
28	HD5	68	BOA3/BEA2	108	SD1	148	MRD#
29	HD4	69	BEA3	109	SD2	149	MWR#
30	GND	70	GND	110	SD3	150	GND
31	HD3	71	CAWE1#	111	SD4	151	IORD#
32	HD2	72	CAWE0#	112	SD5	152	IOWR#
33	HD1	73	CA32S#	113	SD6	153	RDYI#
34	HD0	74	BEOE#	114	SD7	154	LDEV#
35	CA31	75	VCC	115	GND	155	LREQ#
36	CA25	76	BOOE#	116	SD8	156	LGNT#
37	CA24	77	TAGWE#	117	SD9	157	BE0#
38	CA23	78	TAG7/MA10	118	SD10	158	BE1#
39	CA22	79	TAG6/MA9	119	SD11	159	BE2#
40	CA21	80	TAG5/MA8	120	SD12	160	BE3#

3.1 Signal Descriptions

3.1.1 AT Bus Interface Signals

Name	Type	Pin No	Description
A20M#/GA20	I/O	4	*Cyrix A20M/GATEA20.* In Cyrix mode, this pin is A20M# to the Cyrix 486DLC CPU. Emulation of GATEA20 ORed with internal fast GATEA20 output to 486 CPU. This signal must remain high during the power-up CPU reset period. In 386 mode (not Cyrix), this is the GA20 signal indirectly buffered to the AT bus line LA20.
ALE	O	127	*Address Latch Enable.* This signal is used to indicate that the AT cycle has started. It is brought high during non-CPU cycles.
CHRDY	I/O	125	*Channel Ready Input from AT bus.* This pin is a Schmitt-trigger input.
IO16#	I	139	*16-bit I/O Slave Cycle Status.* This is a Schmitt-trigger input pin.
IORD#	I/O	151	*I/O Read Command.* This is an input pin during DMA or master cycles, and an output pin during CPU cycles.
IOWR#	I/O	152	*I/O Write Command.* This is an input pin during DMA or master cycles, and an output pin during CPU cycles.
LMCS#/ KBCS#	O	129	*Low Memory Chip Select/Keyboard Chip Select.* This pin is used to indicate that the current CPU cycle is a memory cycle and the address is below 1MB. This signal is also used as the keyboard chip select. It must be qualified with M/IO# from the CPU before being applied to the keyboard controller chip.
M16#	I/O	133	*16-bit AT Memory Slave Cycle Status.* Schmitt-trigger input pin normally; driven low during a master cycle.
MRD#	I/O	148	*Memory Read Command.* This is an input pin during DMA or master cycles.
MWR#	I/O	149	*Memory Write Command.* This is an input pin during DMA or master cycles.
LREQ1#/ NOWS#	I	138	*VL Bus Request 1/Zero Wait State Input from AT bus.* This is a Schmitt-trigger input pin. Note that the system BIOS ROM is accessed as a one wait state AT cycle. This signal is also used as the VL bus master request signal to gain control of the VL bus when TAG1 is sampled low during reset (pull-down).
ROMCS#/ INTA#	O	134	*ROM Chip Select/Interrupt A.* System BIOS ROM accesses could be either 8- or 16-bit. This signal will be asserted from the end of the first T2 to the end of the last T2.
SBHE#	I/O	126	*System Bus High Byte Enable.* This is an input pin during master cycles.
XA0	I/O	146	*System Address Line 0.* This pin is an input during master cycle; an output pin during CPU, DMA, or refresh cycles.
XA1	I/O	147	*System Address Line 1.* This pin is an input during master cycle; an output pin during CPU, DMA, or refresh cycles.

3.1.2 Bus Arbitration Interface Signals

Name	Type	Pin No	Description
AEN1#	I	61	*Address Enable Bit 1.* When active, indicates an 8-bit DMA cycle.
AEN2#	I	62	*Address Enable Bit 2.* When active, indicates a 16-bit DMA cycle.

Name	Type	Pin No	Description
DMADS	I	60	*DMA Address Strobe.* The 82C495XLC latches XD[7:0] with this signal to translate an 8-bit DMA cycle to CA[16:9] or a 16-bit DMA cycle to CA[15:8].
EADS#/ NPRST	O	3	*Early Address Strobe/Numeric Coprocessor Reset.* This signal is asserted for two T states during DMA or master cycles. In 386 mode, a reset of the numeric coprocessor can be generated by an I/O write to port F1h, which will trigger NPRST.
HD[15:0]	I/O	17-19, 21-29, 31-34	*Host Data.* CPU Data Bus lines [15:0]
HDDIR#	O	143	*Host Data Bus Buffer Direction Control* between HD[31:16] and SD[15:0]. If HDDIR# is asserted low, SD[15:0] is directed to HD[31:16]. If HDDIR# is asserted high, the HD bus is directed to the SD bus.
HDHEN#	O	145	*Host Data Bus High Byte Enable.* This buffer control signal enables the buffer between HD[31:24] and SD[15:8].
HDLEN#	O	144	*Host Data Bus Low Byte Enable.* This buffer control signal enables the buffer between HD[23:16] and SD[7:0].
HLDA	I	104	*Hold Acknowledge from CPU.*
HLDA1	O	132	*Hold Acknowledge 1.* DMA or Master Cycle Granted Notice.
HOLD	O	5	*Hold Request to CPU.* Hidden refresh will not hold the CPU.
HRQ	I	58	*Hold Request.* DMA or Master Cycle Request from 82C206.
LGNT#	O	156	*VL Bus Master Grant.* The VL bus master can initiate its own cycle.
LREQ#/ TURBO	I/O	155	*VL Bus Master Request/Turbo Input.* This signal is used to gain control of the VL bus. In 386 mode, this pin is the hard-wired TURBO input.
LGNT1#/ MPOE#	O	98	*VL Bus Grant 1/Memory Parity Bit Output Enable.* If memory parity check is enabled, MPOE# will be asserted low during DRAM read and write cycles. This signal is also used as the VL Bus Master grant when TAG1 is sampled low during reset (pull-down).
OUT1/AHOLD	I	59	*Refresh Request from Timer1 Output/Address Hold.* This signal is also used as the CPU address hold signal when TAG0 is sampled low during reset (pulled down). Address Hold is used to tri-state the CPU address bus for internal cache snooping.
RFSH#	I/O	128	*Refresh Cycle Indication.* This is an input pin during the DMA or master cycle. Note that 82C495XLC will not HOLD the CPU during AT refresh cycles. The 82C495XLC puts the CPU on “waiting” if an AT refresh cycle is underway.
SD[15:0]	I/O	124-122, 120-116, 114-107	*System Data Bus Lines [15:0].*
XDIR#	I/O	142	*XD Bus Direction Control* for the buffer between XD[7:0] to SD[7:0]. If XDIR# is asserted low, XD[7:0] is driven to SD[7:0]. If XDIR# is asserted high, SD[7:0] is driven to XD[7:0].

3.1.3 Clock and Reset Interface Signals

Name	Type	Pin No	Description
ATCLK	O	131	*ATCLK to AT bus.* This is a free running clock output. It could be CLKI/3, CLKI/4, CLKI/5 or CLKI/6.
CLKI	I	7	*Single Phase Clock Input* for the 82C495XLC internal state machine. The 82C495XLC uses single phase clock input only.
CPURST	O	13	*CPU Reset* for the 386 or 486 microprocessor.
OSC	I	105	*14.3 MHz Oscillator input.*
OSC12	O	121	*1.19 MHz clock output to the 82C206.*
RST1#	I	106	*Cold Reset Input* from either the Powergood signal from the power supply, or from the reset switch.

3.1.4 CPU Interface Signals

Name	Type	Pin No	Description
ADS#	I/O	11	*Address Status input from CPU.* This active low signal indicates the CPU is starting a new cycle. ADS# becomes an output pin during DMA and master cycles for local device accesses.
BE[3:0]#	I/O	160-157	*Byte Enables [3:0].* These signals are inputs during CPU cycles and are outputs during DMA and master cycles, derived from SA[1:0] and SBHE# from the AT Bus.
BLST#/PREQI	I	6	*Burst Last Cycle Indication/Processor Request Input.* In 486 mode, 82C495XLC terminates the burst cycle as long as the BLST# is sampled low at the end of each T2 when BRDY# is active. During 386 mode, this is the PREQI signal from the 387.
BRDY#/ PREQO	I/O	14	*Burst Ready Output/Processor Request Output.* Burst ready output for CPU to sample the read data during burst cycles. This pin becomes PREQO for the 386 mode of operation.
CA[5:2]/ MP[3:0]	I/O	99, 101-103	*CPU Address/Memory Parity.* CPU address lines [5:2] and DRAM parity bits [3:0]. A buffer is required for CA[5:2] if parity checking is used. The 82C495XLC will latch CA[5:2] and then disable the input buffer to enable MP[3:0] for the rest of the cycle.
CA[7:6]	I	56,57	*CPU Address.* CPU address lines 7 and 6. These lines are input only.
CA[16:8]	I/O	46-49, 51-55	*CPU Address.* CPU address lines [16:8]. These are input pins during CPU and master cycles. CA[16:9] are output pins for DMA address A[16:9] by latching XD[7:0] during 16-bit DMA cycles and CA[15:8] are output pins during 8-bit DMA address A[15:8].
CA31, CA[25:17]	I	35-44	*CPU Address.* CPU address lines 31 and 25 through 17. These lines are input only.
D/C#	I	8	*Data and Code Cycle Status.* This signal indicates data transfer operations when high, or control operations (code fetch, halt, etc.) when low.
KEN#/ERR#	O	2	*Cacheable or Non-Cacheable Status/Error.* Cacheable or non-cacheable for 486 internal cache. This signal is low normally, and is brought high at the end of T1. The 82C495XLC asserts KEN# again if it is a cacheable cycle. During 386 mode, this pin is ERR# to the 386.
LDEV#	I	154	*Local Bus Device Cycle Indication;* (for local devices on the CPU bus). This signal is sampled at the end of the first T2.

Name	Type	Pin No	Description
M/IO#	I/O	10	*Memory and I/O Cycle Status.* It indicates a memory cycle if high, and I/O cycle if low. It becomes an output pin during DMA and master cycles for local device accesses.
RDY#	I/O	16	*Ready Output.* Ready output for CPU to terminate the current cycle. This pin becomes an input pin during local device cycle if a tri-stated local bus device's Ready was connected.
RDYI#	I	153	*Ready Input.* This signal is synchronized by the 82C495XLC before sending to CPU.
W/R#	I/O	9	*Write and Read Cycle Status.* This signal is used to indicate a write cycle if high and read cycle if low. It becomes an output pin during DMA and master cycles for local device accesses.

3.1.5 External Cache Control Interface Signals

Name	Type	Pin No	Description
BEA3	O	69	*Even Bank Address 3.* This signal is tri-stated during the T1 cycle and during the first half of the T2 cycle, after which it reflects the status of CA3 and will toggle during dirty write-back, cache line fill, and CPU burst read cycles.
BEOE#	O	74	*Even Bank Output Enable.* This signal is activated when CA2 is low during cache read cycles. BEOE# also will toggle during dirty write-back and CPU burst read cycles.
BOA3/BEA2	O	68	*Odd Bank Address 3/Even Bank Address 2.* This signal is tri-stated during the T1 cycle and during the first half of the T2 cycle, after which it reflects the status of CA3 and will toggle during dirty write-back, cache line fill, and CPU burst read cycles. This line is used as BEA2 when only one cache bank is used.
BOOE#	O	76	*Odd Bank Output Enable.* This signal is activated when CA2 is high during cache read cycles. BOOE# becomes the compliment of BEOE# during dirty write-back and CPU burst read cycles.
CA3S#	O	73	*External Cache Address Bit 3 Select.* This signal is used to choose between CA3 and BEA3 for the even cache bank address 3, or BOA3 for the odd bank address 3. CA3S# is active for the first T1 and T2 cycles. This pin is also used to latch the MA address lines to allow quick switching of Tag RAM data bits.
CAWE[1:0]#	O	71,72	*External Cache Write Enables.* CAWE1# is used to select the even cache bank for writes and CAWE0# is used to select the odd cache bank for writes.
TAG[7:0]/ MA[10:3]	I/O	78-80, 82-86	*Tag RAM/Memory Address.* Tag RAM I/O lines [7:0] and DRAM row/column address lines [10:3].
TAGWE#	O	77	*Tag RAM Write Enable.* This signal is used to update the Tag RAM.

3.1.6 Local DRAM Interface Signals

Name	Type	Pin No	Description
CAS[3:0]#	O	93, 94, 96, 97	*Column Address Strobes [3:0].*
DWE#	O	90	*DRAM Write Enable Output Signal.*
MA[2:0]	O	87-89	*Memory Address Lines [2:0].*

Name	Type	Pin No	Description
RAS0#	O	92	*Row Address Strobe 0.*
RAS1#/MA11	O	91	*Row Address Strobe/Memory Address.* Row address strobe 1 and row/column address bit 11.

3.1.7 Miscellaneous Signals

Name	Type	Pin No	Description
ASRTC	O	137	*Real Time Clock (RTC) Address Strobe.*
CHCK#	I	141	*Channel Check Input* from AT bus to indicate there is a parity error generated by the AT memory card. (NMI interrupt request).
NMI	O	12	*Non-Maskable Interrupt to CPU.* Caused by system parity error or AT bus channel check.
OUT2	I	63	*Timer 2 Output.*
SPKD	O	67	*Speaker Data Output.* Generated by OUT2 and port 61h bit 1.
TMRG2	O	136	*Timer Gate 2 to 82C206*

3.1.8 Numeric Processor Interface

Name	Type	Pin No	Description
IGERR#/ BUSY#	O	66	*Ignore Numeric Error/Coprocessor Busy.* This normally high signal will go low as soon as NPERR# is asserted and then will immediately return high, which will cause the coprocessor to freeze on the next non-control FPU instruction if a previous FPU instruction caused an error. IGERR# is normally connected to the CPU input IGNNE#. During 386 mode, this pin is the BUSY# signal to the 386 from the coprocessor.
INT13	O	135	*Interrupt 13.* This active high output is the error interrupt request from the math coprocessor, which is connected to the interrupt controller.
NPBUSY#/ HITM#	I	64	*Numeric Processor Busy/Cache Hit.* 387 numeric coprocessor busy signal. This pin is also used to determine 386 or 486 mode. A high indicates a 386, a low indicates a 486DX. This signal is also used as HITM# for the internal cache when TAG0 is pulled down. HITM# indicates that the CPU has had a hit in its internal cache during an inquire cycle.
NPERR#	I	65	*Numeric Processor Error.* Used to generate IGERR# for the 486 CPU. This signal also generates NPINT for PC/AT compatibility and will generate BUSY# for the 386.

3.1.9 Power

Name	Type	Pin No	Description
GND	GND	1,15,30,50,70,81,95,115,130,150	Ground or VSS
VCC	PWR	20,45,75,100,140	+5v or VDD

4.0 Functional Description

4.1 Reset Logic

The RST1# input to the 82C495XLC is used to generate the CPU reset (CPURST), the numeric coprocessor reset (NPRST). RST1# is a “cold reset” which is generated when either POWERGOOD goes low (from the power supply, indicating a low power condition) or the system reset button is activated. This reset signal is used to force the system to begin execution at a known state. When RST1# is sensed active, the 82C495XLC will assert CPURST and NPRST. CPURST is also generated when a shutdown condition is decoded from the CPU bus definition signals. CPURST and NPRST are asserted for 128 CLK2 cycles.

The 82C495XLC emulates the keyboard reset function. The keyboard reset is intercepted by monitoring the I/O write cycle “FE” command to port 64h. This fast CPU reset from the chipset will be generated directly after the I/O write is decoded unless bit 1 of index register 20h is disabled, in which case the reset will not start until a “HALT” instruction is executed.

When configured to interface with a math coprocessor, the 82C495XLC will generate the NPRST signal when the CPURST is activated, or if an I/O write to port F1h is issued.

4.2 System Clock Generation

CLK is a master single phase clock which is used to drive all host CPU synchronous signals and the 82C495XLC's internal state machines.

The 82C495XLC generates the AT bus clock (ATCLK) from an internal division of CLK. The ATCLK frequency is programmable and can be set to any of four clock division options by programming bits [1:0] of index register 25h. This allows the system designer to tailor the AT bus clock frequency to support a wide range of system designs and performance platforms.

4.3 CPU Burst-Mode Control

The 82C495XLC chipset fully supports 486 burst cycles. The 82C495XLC cache and DRAM controllers insure that data is burst into the CPU whenever the 486 requests a burst line fill. The secondary cache provides data on read-hits and the DRAM supplies the data during cache read-misses.

For a cache read-hit cycle, BRDY# (Burst Ready) is asserted at the middle of the first T2 state when a 2-1-1-1 (zero wait state) cache burst cycle is chosen, otherwise it is asserted at the middle of the second T2 state when one wait state is required. If a read-miss occurs, the DRAM data is first written into cache memory, then it is burst from the cache to the 486 CPU. BRDY# is asserted after cache memory is updated for cache read-misses. Once asserted, BRDY# stays active until BLST# (Burst Last) is detected during a zero wait state burst cycle. BRDY# is never active during DMA or MASTER cycles.

The 82C495XLC contains separate burst counters to support DRAM and external cache burst cycles. The DRAM burst counter performs the cache read-miss line fill (DRAM to external cache) and the cache burst counter supports the 486 burst line fill (external cache to the 486 CPU). The burst order of the cache burst counter exactly matches the double-word address sequencing expected by the 486 CPU. The DRAM burst counter is used for cache read-miss cycles and dirty-line fill write operations.

4.4 Cache Subsystem

The integrated cache controller, which uses a direct-mapped, bank-interleaved scheme dramatically boosts the overall performance of the local memory subsystem by caching writes as well as reads (write-back mode). Cache memory can be configured as one or two banks and sizes of 32/64/128/256KB for 386 mode and 64/128/256/512KB for 486 mode. Provisions for two programmable non-cacheable regions are provided. The cache controller operates in non-pipeline mode, with a fixed 16-byte line size (optimized to match a 486 burst line fill) in order to simplify the motherboard design without increasing cost or degrading system performance. For 486 systems, the secondary cache operates independently and in addition to the CPU's internal cache.

The cache controller works as the front-end for both the DRAM and AT bus controllers. ADS# from the CPU must pass through the cache logic first. When the cache is disabled, ADS# just falls through the cache controller and delivers internal MADS# to the DRAM and AT bus controllers. When the cache is enabled, ADS# is blocked when a cache cycle is detected. If this cycle is determined to be a non-cacheable address or a cache miss cycle, ADS# is delayed one CLK before outputting internal MADS# (due to the time needed for non-cacheable address and cache hit/miss detection.

4.4.1 Cache Bank Interleave

In order to support cache burst cycles at elevated frequencies and still utilize conventional speed SRAMs, a bank interleave cache access method is employed. The addresses are applied to the cache memory one cycle earlier, while cache-output-enable signals control even/odd bank selection and enable cache RAM data to the CPU data bus. Since the output enable time is about one-half of the address access time, the 82C495XLC can achieve a high performance cache burst mode without using the more expensive high speed SRAMs.

The 82C495XLC supports one or two cache banks. Two cache banks are required to interleave and realize the performance advantages of this cache scheme. Cache sizes of

128KB and 512KB are single bank caches, while 64KB and 256KB cache sizes are double bank. When using a double bank configuration, the even and odd banks receive the same address lines. Signals A2/A3, CAWE1#/CAWE0#, and BEOE#/BOOE# are used to dictate the even or odd bank access.

4.4.2 Write-Back Cache

The write-back cache scheme derives its superior performance by optimizing write cycles. There is no performance penalty in the cache write cycle, since the cache controller does not need to wait for the much slower DRAM controller to finish its cycle before proceeding to the next cycle.

4.4.3 Tag RAM

A built-in tag comparator improves system performance while reducing component count on the system board. The comparator internally detects the cache hit/miss status by comparing the high-order address bits (for the memory cycle in progress) with the stored tag bits from previous cache entries. When a match is detected, and the location is cacheable, a cache hit cycle takes place. If the comparator does not match, or a non-cacheable location is accessed (based on the internal non-cacheable region registers), the current cycle is a cache miss. The tag is invalidated automatically during memory reads when the cache is disabled; each memory read will write into the corresponding tag location a non-cacheable address (such as A0000h or B0000h of the video memory area). To flush the cache, simply disable the cache in configuration register 21h and read a block of memory equal to the size of the cache. The advantage of this invalidation scheme is that no valid bit is necessary and expensive SRAM can be conserved.

The following tables detail which CPU address bits are stored as tags for the various cache sizes supported in the 82C495XLC.

Table 4-1 describes how the Tag RAM bits are addressed for different cache sizes.

Table 4-1 Correspondence Between Tag Bits and CPU Address Lines

ADDRESS to Tag Bit Mapping					
Tag Bit	**32KB (386 only)**	**64KB**	**128KB**	**256KB**	**512KB (486 only)**
7	A22	A22	A22	A22	A22
6	A21	A21	A21	A21	A21
5	A20	A20	A20	A20	A20
4	A19	A19	A19	A19	A19
3	A18	A18	A18	A18	x
2	A17	A17	A17	A25	A25
1	A16	A16	A24	A24	A24
0	A15	A23	A23	A23	A23

Table 4-2 shows the cache sizes supported by the 82C495XLC, with the corresponding Tag RAM address bits, Tag RAM size, cache RAM address bits, cache RAM size, and cacheable main memory size.

Table 4-2 Cache SRAM Requirements

Cache Size	Tag Field Address/ Tag RAM Size	Cache SRAM Address Qty/ Cache RAM Size	Cacheable Main Memory
32KB	A22-A15 8Kx8	A14-A2 4ea 8Kx8	8MB
64KB	A23-A16 8Kx8	A15-A2 8ea 8Kx8	16MB
128KB	A24-A17 8Kx8	A16-A2 4ea, 32Kx8	32MB
256KB	A25-A18 32Kx8	A17-A2 8ea, 32Kx8	64MB
512KB	A25-A19 32Kx8	A18-A2 4ea, 128Kx8	64MB

Table 4-3 shows what speed SRAM and Tag SRAM to use for a particular CPU clock rate.

Table 4-3 SRAM Speed Requirements

CPU Speed	Cache SRAM	Tag SRAM	DRAM speed	Note
20MHz	25ns	25ns	80ns	Cache Burst 3-2-2-2 Cache Write 1ws DRAM R&W = 0ws
25MHz	25ns	25ns	80ns	Cache Burst 3-2-2-2 Cache Write 1ws DRAM R&W = 0ws
33MHz	20ns	15ns	80ns	386 only: Cache Read 1ws Cache Write 1ws DRAM R&W = 0ws
33MHz	20ns	15ns	80ns	486 only: Cache Burst 3-2-2-2 Cache Write 1ws DRAM R&W = 0ws
40MHz	20ns	15ns	80ns	386 only: Cache Read 1ws, Cache Write 1ws DRAM R&W = 1ws

CPU Speed	Cache SRAM	Tag SRAM	DRAM speed	Note
40MHz	20ns	15ns	80ns	486 only: Cache Burst 3-2-2-2 Cache Write 1ws DRAM R&W = 1ws
50MHz	20ns	15ns	80ns	Cache Burst 3-2-2-2 Cache Write 1ws DRAM R&W = 1ws

NOTE DRAM and cache cycles are at their minimum wait states.

4.4.4 P24T (L1 Write-Back) Mode

The 82C495XLC supports write-back CPU cycles when TAG0 is sampled low at reset. During a DMA or bus master transfer to the memory, EADS# will be asserted for one CPU clock delay after ADS#. The HITM# signal will be sampled two CPU clocks after EADS# is generated. If HITM# is active (low), the 82C495XLC will suspend the current cycle by de-asserting HOLD and then start the CPU L1 write-back cycle to update the modified line from the CPU internal write-back cache. IOCHRDY will be de-asserted for DMA and ISA bus masters until the L1 write-back cycle is completed. After completing the L1 write-back cycle, the DMA or bus master will continue the previous suspended cycle.

4.5 Local DRAM Control Subsystem

The 82C495XLC supports up to two banks of page-mode local DRAM memory for configurations of up to 64MB. 256KB, 1MB, 4MB or 16MB page-mode DRAM devices may be used. The DRAM configuration is programmable through configuration register 24h. DRAM performance features are programmable through configuration register 25h.

Table 4-4 illustrates the DRAM configurations supported via register index 24h.

Table 4-4 DRAM Configurations

Bank0 DRAM	Bank1 DRAM	Total Mem.	Register Bits 7 6 5 4
256KB	x	1MB	0 0 0 0
256KB	256KB	2MB	0 0 0 1
1MB	x	4MB	1 0 0 0
256KB	1MB	5MB	0 0 1 0
1MB	1MB	8MB	1 0 0 1
4MB	x	16MB	1 1 0 0
1MB	4MB	20MB	1 0 1 0
4MB	1MB	20MB	1 0 1 1
4MB	4MB	32MB	1 1 0 1
16MB	x	64MB	1 1 1 0

Table 4-5 describes how the DRAM address lines are multiplexed when different memory device types are used.

Table 4-5 CPU Address to MA Bus Mapping

Address to MA bus Mapping								
Memory Address	256KB		1MB		4MB		16MB	
	Col	Row	Col	Row	Col	Row	Col	Row
MA0	A2	A12	A2	A12	A2	A23	A2	A23
MA1	A3	A13	A3	A13	A3	A13	A3	A13
MA2	A4	A14	A4	A14	A4	A14	A4	A14
MA3	A5	A15	A5	A15	A5	A15	A5	A15
MA4	A6	A16	A6	A16	A6	A16	A6	A16
MA5	A7	A17	A7	A17	A7	A17	A7	A17
MA6	A8	A18	A8	A18	A8	A18	A8	A18
MA7	A9	A19	A9	A19	A9	A19	A9	A19
MA8	A10	A11	A10	A20	A10	A20	A10	A20
MA9	x	x	A11	A21	A11	A21	A11	A21
MA10	x	x	x	x	A12	A22	A12	A22
MA11	x	x	x	x	x	x	A24	A25

4.6 Parity Generation/Detection Logic

During local DRAM write cycles, the 82C495XLC generates a parity bit for each byte of write data from the processor. Parity bits are stored into local DRAM along with each data byte. During a DRAM read, the parity bit is checked for each data byte. If the logic detects incorrect parity, the 82C495XLC will generate a parity error to the CPU. The parity error will invoke the NMI interrupt, providing the parity check is enabled in configuration register 21, bit 5. Parity check must also be enabled in port B register 61h, bits [2:3].

4.7 Refresh Logic

The 82C495XLC supports both normal and hidden refresh. Normal refresh refers to the classic refresh implementation which places the CPU on “hold” while a refresh cycle takes place to both the local DRAM and any AT bus memory. This is the default condition at power-up. However, hidden refresh is performed independent of the CPU and does not suffer from the performance restriction of losing processor bandwidth by forcing the CPU into its hold state. Hidden refresh delivers higher system performance and is recommended over normal refresh. As long as the CPU does not try to access local memory or the AT bus during a hidden refresh cycle, refresh will be transparent to the CPU. The CPU can continue to execute from its internal and secondary caches as well as execute internal instructions during hidden refresh without any loss in performance due to refresh arbitration. If a local memory or AT bus access is required during hidden refresh, wait states will be added to the CPU cycle until the resource becomes available. Hidden refresh also separates refreshing of the AT bus and local DRAM. The DRAM controller arbitrates between CPU DRAM accesses and DRAM refresh cycles, while the AT bus controller arbitrates between CPU accesses to the AT bus, DMA, and AT refresh. The AT bus controller asserts the RFSH# and MEMR# commands and outputs the refresh address during AT bus refresh cycles.

The 82C495XLC implements refresh cycles to the local DRAM using CAS-before-RAS timing. CAS-before-RAS refresh has lower power consumption than RAS-only refresh—which is important when dealing with large memory arrays. CAS-before-RAS refresh is used for both normal and hidden refresh to local memory.

The output of internal counter1/timer1 (OUT1) inside the 82C495XLC is programmed as a rate generator to produce the periodic refresh request signal which occurs every 15µs. Requests for refresh cycles are generated by two sources: counter1/timer1 or 16-bit ISA masters that activate refresh when they have bus ownership. These ISA masters supply refresh cycles because the refresh controller cannot preempt the bus master to perform the necessary refresh cycles. 16-bit ISA masters that hold the bus longer than 15µs must supply refresh cycles.

4.8 Shadow RAM

Since accesses to local DRAM are much faster than those to EPROM, the 82C495XLC provides shadow RAM capability. With this feature, code from slow devices like ROM and EPROM memories can be copied to local DRAM to speed up memory accesses. Accesses to the specified EPROM space are redirected to the corresponding DRAM location. Shadow RAM addresses range from C0000h-FFFFFh. 16KB granularity is provided for the address range C0000h to EFFFFh, while the 64KB range from F0000h-FFFFFh (the location of system BIOS) can be shadowed as an entire segment.

The shadow RAM control is setup in the configuration registers. First, the ROM contents must be copied into the shadow RAM area. Then, the shadow RAM enable bit is set in the configuration register. For the system BIOS area, once the bit is set, the RAM area becomes read-only. For the video and adapter BIOS area, the user can select read only or read/write by setting the write protect bit in index register 26h accordingly. Video BIOS at the C0000h-C8000h area can be shadowed and cached if bit 4 of register 27h is set to 1.

4.9 System ROM BIOS Cycles

The 82C495XLC supports both 8- and 16-bit EPROM cycles. If the system BIOS is 16 bits wide, ROMCS# should be connected to M16# through an open collector gate indicating to the 82C495XLC that a 16-bit EPROM is responding. The system BIOS resides on the XD bus.

ROMCS# is generated for the both the E0000h-EFFFFh and F0000h-FFFFFh segments. If a combined video/system ROM BIOS is desired, these two segments should be used.

4.10 AT Bus State Machine

The AT bus state machine gains control when the 82C495XLC's decoding logic detects a non-local memory cycle. It monitors status signals M16#, IO16#, CHRDY and NOWS# and performs the necessary synchronization of control and status signals between the AT bus and the microprocessor. The 82C495XLC supports 8- and 16-bit memory and I/O devices located on the AT bus.

An AT bus cycle is initiated by asserting ALE in AT-TS1 state. On the trailing edge of ALE, M16# is sampled for a memory cycle to determine the bus size. It then enters the AT-TC state and provides the command signal. For an I/O cycle, IO16# is sampled after the trailing edge of ALE until the end of the command. Typically, the wait states for an AT transaction are five for 8-bit and one for 16-bit. The command cycle is extended when CHRDY is detected inactive, or the cycle is terminated when zero wait state request signal (NOWS#) from the AT bus is active. Upon expiration of the wait states, the AT state machine terminates itself and passes an internal READY to the CPU state machine to generate a synchronous RDY# to the CPU. The AT bus state machine also routes

data and address when an AT bus master or DMA controller accesses memory.

4.11 Bus Arbitration Logic

The 82C495XLC provides arbitration between the CPU, DMA controller, AT bus masters, and the refresh logic. During DMA, AT bus master, and conventional refresh cycles, the 82C495XLC asserts HOLD to the CPU. The CPU will respond to an active HOLD signal by generating HLDA (after completing its current bus cycle) and placing most of its output and I/O pins in a high impedance state. After the CPU relinquishes the bus, the 82C495XLC responds by issuing RFSH# (refresh cycle) or HLDA1 (AT bus master or DMA cycle), depending on the requesting device. During hidden refresh, HOLD remains negated and the CPU continues its current program execution as long as it services internal requests or achieves cache hits (please refer to the refresh section for additional information).

The AT bus controller in the 82C495XLC arbitrates between hold and refresh requests, deciding which will own the bus once the CPU relinquishes control with the HLDA signal. The arbitration between refresh and DMA/Master is based on a FIFO (first in-first out) priority. However, a refresh request (RFSH#) will be internally latched and serviced immediately after DMA/Master finishes its request if queued behind HRQ. HRQ must remain active to be serviced if a refresh request comes first. DMA and bus masters share the same request pin, HRQ. To distinguish between DMA and bus master requests during an active HLDA1 period, the two signals AEN8# and AEN16# need to be monitored. If either AEN8# or AEN16# is active, then the cycle is an 8/16-bit DMA respectively. When these signals are inactive, then an external bus master controls the system bus. The “master” signal from the AT bus indicates an AT bus master cycle and may be sampled by external logic.

4.12 Numeric Coprocessor Cycles

The 82C495XLC monitors NPERR# and NPBUSY# to provide support for the 80387 numeric coprocessor (NPU). The NPU asserts NPERR# during a power-on reset to indicate its presence. The NPU asserts NPBUSY# while executing a floating-point calculation and asserts RDYI# to the chipset when it is finished. If NPBUSY# is active and an NPU error occurs, (NPU asserts NPERR#) the 82C495XLC latches NPBUSY# and generates INT13. Latched BUSY# and INT13 can be cleared by an I/O port F0h write command. If the NPU is not installed, the 82C495XLC treats any access to the NPU address space as an AT cycle. With the NPU in place, CPU accesses to the NPU address space are direct, except for the re-synchronizing of the NPU ready signal (RDYI#) before sending RDY# back to the CPU.

4.13 Local Bus Interface

The 82C495XLC allows peripheral devices to share the “local bus” with the CPU and numeric coprocessor. The performance of these devices (which may include the video subsystem, hard disk adapters, LAN and other PC/AT controllers) will dramatically increase when allowed to operate in this high-speed environment. These devices are responsible for their own address and bus cycle decode and must be able to operate compatibly at the elevated frequencies required for operation on the local CPU bus.

The LDEV# input signal to the 82C495XLC indicates that a local device is intercepting the current cycle. If this signal is sampled at the end of the first T2 clock cycle (end of the second T2 at 50MHz), then the 82C495XLC will allow the responding local device to assume responsibility for the current local cycle. When the device has completed its operation, it must terminate the cycle by asserting the RDYI# pin of the 82C495XLC. The RDYI# signal is synchronized by the 82C495XLC before being sent to the CPU via the RDY# line. Alternatively, the local bus device may drive RDY# directly to the CPU. The 82C495XLC supports two VL bus masters when TAG1 is sampled low at reset.

4.14 Data Bus Conversion/Data Path Control Logic

The 82C495XLC performs data bus conversion when the CPU accesses 16- or 8-bit devices through 16- or 32-bit instructions. It also handles DMA and AT master cycles that transfer data between local DRAM or cache memory and locations on the AT bus. The 82C495XLC provides all of the signals to control external bi-directional data buffers.

4.15 Turbo/Slow Mode Operations

Turbo mode is controlled through configuration register 20h, bit 4 for 386 mode only. Slow mode operation is implemented by applying a periodic clock to the HOLD input of the CPU. OSC12 is the clock source used for this operation. OSC12 is internally derived from the 14.31818MHz OSC clock input to the 82C495XLC. The HOLD is maintained for approximately 2/3 of the time, while the CPU is allowed to perform normal external operations during the remaining 1/3 interval. For system design, the TURBO pin should be pulled high through a 10KΩ resistor. In 386 mode, the LREQ# pin becomes the hard-wired TURBO input. To implement the hard-wired TURBO capability, index register 20h, bit 4 must be set to 0 (default is 1).

4.16 Fast GATEA20 and RESET Emulation

The 82C495XLC will intercept commands to ports 60h and 64h so that it can emulate the keyboard controller, allowing the generation of the fast GATEA20 and fast CPURST signals. The decode sequence is software transparent and requires no BIOS modifications to function. The fast

GATEA20 generation sequence involves writing “D1h” to port 64h, then writing data “02h” to port 60h. The fast CPU “warm reset” function is generated when a port 64h write cycle with data “FEh” is decoded. A write to port 64h with data “D0h” will enable the status of GATEA20 (bit 1 of port 60h) and the warm reset (bit 0 of port 60h) to be readable.

4.17 Special Cycles

The 486 microprocessor provides special bus cycles to indicate that certain instructions have been executed, or certain conditions have occurred internally. Special cycles such as Shutdown and Halt cycles are covered by dedicated handling logic in the 82C495XLC. Based on the operating microprocessor mode, this logic decodes the CPU bus status signals M/IO#, D/C#, and W/R# and takes the appropriate action.

5.0 Register Descriptions

There are 12 configuration registers inside the 82C495XLC. An indexing scheme is used to access all of the registers. Port 22h contains the index register and port 24h is the data register. A register is accessed by first writing the desired address to port 22h, and then reading or writing port 24h. The index resets after every access so every read or write access to port 24h requires a write first to port 22h to set the desired address, even if the same address is being accessed. Unless mentioned otherwise, all reserved bits are set to zero by default and must be set to zero for future compatibility purposes.

5.1 Control Register 1 - Index: 20h

Bit	Description	Default
7-6	Version number of 82C495XLC (read-only).	00
5	Burst Wait State Control 0 = secondary cache read-hit cycle is 3-1-1-1 or 2-1-1-1. 1 = secondary cache read-hit cycle is 3-2-2-2 or 2-2-2-2. Note: This bit is ignored in 386 mode. Refer to register 21h bit 0.	0
4	Turbo Mode Control (386 mode only, ignored in 486 mode). 0 = disable, 1 = enable When Turbo Mode Control is enabled (and in 386 mode), the state of LREQ# (pin 155) determines whether the CPU is in Turbo or non-Turbo mode. If LREQ# is low, TURBO mode is disabled and the CPU will be held for 2/3 of its operation time.	0
3	Single ALE Enable - 82C495XLC will activate single ALE instead of multiple ALEs during bus conversion cycle if this bit is enabled. 0 = disable, 1 = enable	0
2	Reserved	0
1	Emulation Keyboard Reset Control - turn on this bit requires a Halt instruction to be executed before the 82C495XLC generates CPURST. 0 = disable, 1 = enable This bit also affects soft resets via writes to ports 64h and 92h. Note: This bit must be set to 1 in BIOS default value.	1
0	Reserved	0

5.2 Control Register 2 - Index: 21h

Bit	Description	Default
7	Single Bank Cache Enable 0 = disable, 1 = enable	0
6	Cache Write Two Wait States Control 1 = two wait states, bit 1 of index register 21h will be ignored 0 = either zero or one wait state, refer to bit 1 of index register 21h	0
5	Parity Check 0 = enable, 1 = disable	1

Bit	Description	Default
4	Cache Enable 0 = cache is disabled and DRAM burst mode is enabled 1 = cache enable and DRAM burst mode is disabled	0
3-2	Cache Size 3 2 Cache Size 0 0 64KB 0 1 128KB 1 0 256KB 1 1 512KB for 486 mode, 32KB for 386 mode	00
1	Cache Write 0/1 Wait State Control - with bit 6 of index register 21h = 0 0 = 1 wait state, 1 = 0 wait state	0
0	Cache Read Wait State Control 486 Mode: 0 = 3-1-1-1 cycle, 1 = 2-1-1-1 cycle (refer also to register 20h bit 5) 386 Mode: 0 = 1ws, 1 = 0ws	0

5.3 Shadow RAM Control Register 1 - Index: 22h

Bit	Description	Default
7	ROM (F0000-FFFFFh) Enable 1 = read from ROM, write to DRAM. ROMCS# is generated during read access only 0 = read/write on DRAM and DRAM is write-protected	1
6	Shadow RAM at D0000h-DFFFFh Area 0 = disable, 1 = enable	1
5	Shadow RAM at E0000h-EFFFFh Area 0 = disable shadow RAM, enable ROMCS#. The E0000-EFFFFh ROM is defaulted to reside on XD bus. 1 = enable shadow RAM and disable ROMCS# generation	1
4	Shadow RAM at D0000h-DFFFFh Area Write Protect Enable 0 = disable, 1 = enable	0
3	Shadow RAM at E0000h-EFFFFh Area Write Protect Enable 0 = disable, 1 = enable	0
2	Hidden refresh enable (without holding CPU) 1 = disable, 0 = enable	1
1	Reserved	0
0	Reserved	0

5.4 Shadow RAM Control Register 2 - Index: 23h

Bit	Description	Default
7	Shadow RAM at EC000h-EFFFFh area 0 = disable, 1 = enable	0
6	Shadow RAM at E8000h-EBFFFh area 0 = disable, 1 = enable	0
5	Shadow RAM at E4000h-E7FFFh area 0 = disable, 1 = enable	0
4	Shadow RAM at E0000h-E3FFFh area 0 = disable, 1 = enable	0
3	Shadow RAM at DC000h-DFFFFh area 0 = disable, 1 = enable	0
2	Shadow RAM at D8000h-DBFFFh area 0 = disable, 1 = enable	0
1	Shadow RAM at D4000h-D7FFFh area 0 = disable, 1 = enable	0
0	Shadow RAM at D0000h-D3FFFh area 0 = disable, 1 = enable	0

5.5 DRAM Control Register 1 - Index: 24h

Bit	Description					Default
7-4	DRAM types used for Bank 0 and Bank 1.					0000
	7	6	5	4	Bank 0 Bank 1	
	0	0	0	0	256Kx	
	0	0	0	1	256K256K	
	0	0	1	0	256K1M	
	0	0	1	1	256K4M	
	0	1	x	x or 1 1 1 1	xx	
	1	0	0	0	1Mx	
	1	0	0	1	1M1M	
	1	0	1	0	1M4M	
	1	0	1	1	4M1M	
	1	1	0	0	4Mx	
	1	1	0	1	4M4M	
	1	1	1	0	16Mx	
3-0	Reserved					0000

5.6 DRAM Control Register 2 - Index: 25h

Bit	Description	Default
7-6	Read cycle wait state 7 6 Additional wait States 0 0 Not used 0 1 0 1 0 1 1 1 2 **NOTE** Base wait states is 3.	11
5-4	Write cycle wait state 5 4 Additional wait states 0 0 0 0 1 1 1 0 2 1 1 3 **NOTE** Base wait states is 2.	11
3	Fast decode enable. This function may be enabled in 20/25 MHz operation to speed up the DRAM access. 0 = disable fast decode, DRAM base wait states is not changed 1 = enable fast decode, DRAM base wait states is decreased by 1 This bit is automatically disabled even when it is set to 1 when bit 4 of index register 21h (cache enable bit) is enabled.	0
2	Reserved	0
1-0	ATCLK selection. 1 0 ATCLK selection 0 0 ATCLK = CLKI/6 (Default) 0 1 ATCLK = CLKI/4 1 0 ATCLK = CLKI/3 1 1 ATCLK = CLKI/5	00

5.7 Shadow RAM Control Register 3 - Index: 26h

Bit	Description	Default
7	Enable Fast AT cycle 1 = enable, 0 = disable	1
6	Shadow RAM copy enable for address area C0000h-EFFFFh 0 = Read/write at AT bus 1 = Read from AT bus and write into shadow RAM	0
5	Shadow write protect at address area C0000h-CFFFFh 0 = Write protect disable 1 = Write protect enable	0

Bit	Description	Default
4	Shadow RAM enable at C0000h-CFFFFh area 0 = disable, 1 = enable	0
3	Enable shadow RAM at CC000h-CFFFF area 0 = disable, 1 = enable	0
2	Enable shadow RAM at C8000h-CBFFF area 0 = disable, 1 = enable	0
1	Enable shadow RAM at C4000h-C7FFFh area 0 = disable, 1 = enable	0
0	Enable shadow RAM at C0000h-C3FFFh area 0 = disable, 1 = enable	0

5.8 Control Register 3 - Index: 27h

Bit	Description	Default
7	Enable NCA# pin to low state, 0 = disable, 1 = enable	1
6	Reserved	0
5	Back to Back I/O Delay Control 0 = enable delay, 1 = disable delay	1
4	Video BIOS at C0000h-C7FFFh area non-cacheable 0 = Cacheable 1 = Non-Cacheable	1
3-0	Cacheable address range for local memory Bits 3 2 1 0 Cacheable Address range — 3 2 1 0 Cacheable Address Range 0 0 0 0 0-64MB — 1 0 0 0 0-32MB 0 0 0 1 0-4MB — 1 0 0 1 0-36MB 0 0 1 0 0-8MB — 1 0 1 0 0-40MB 0 0 1 1 0-12MB — 1 0 1 1 0-44MB 0 1 0 0 0-16MB — 1 1 0 0 0-48MB 0 1 0 1 0-20MB — 1 1 0 1 0-52MB 0 1 1 0 0-24MB — 1 1 1 0 0-56MB 0 1 1 1 0-28MB — 1 1 1 1 0-60MB **NOTE** If total memory is 1MB or 2MB, the cacheable range is 0-1 or 0-2MB respectively and independent of the value of bits 3:0 of index register 27h.	0001

NOTE Memory area at 640K-1MB is defaulted to be non-cacheable.

5.9 Non-Cacheable Block 1 Register 1 - Index: 28h

This register is used in conjunction with index register 29h register to define a non-cacheable block. The starting address for the Non-Cacheable Block must have the same granularity as the block size. For example, if a 512KB non-cacheable block is selected, its starting address is a multiple of 512KB; consequently, only address bits of A19-A23 are significant and A16-A18 are “don't care”.

Bit	Description		Default
7-5	Size of non-cacheable memory block 1		100
	7 6 5	Block Size	
	0 0 0	64K	
	0 0 1	128K	
	0 1 0	256K	
	0 1 1	512K	
	1 x x	Disabled	
4-2	Unused		000
1-0	Address bits of A25 and A24 of non-cacheable memory block 1		00

5.10 Non-Cacheable Block 1 Register 2 - Index: 29h

Bit	Description								Default
7-0	Address bits A23-A16 of non-cacheable memory block 1								0001 xxxx
		Valid Starting Address Bits							
	Block Size	A23	A22	A21	A20	A19	A18	A17	A16
	64KB	V	V	V	V	V	V	V	V
	128KB	V	V	V	V	V	V	V	x
	256KB	V	V	V	V	V	V	x	x
	512KB	V	V	V	V	V	x	x	x

x = Don't Care
V = Valid Bit

6.0 Electrical Specification

6.1 Absolute Maximum Ratings

Sym	Description	Min	Max	Units
Vcc	Supply Voltage		6.5	V
Vi	Input Voltage	-0.5	VCC + 5.5	V
Vo	Output Voltage	-0.5	VCC + 5.5	V
Top	Operating Temperature	0	70	°C
Tstg	Storage Temperature	-40	125	°C

NOTE Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

6.2 DC Characteristics

Sym	Description	Min	Max	Units
VIL	Input Low Voltage	-0.5	0.8	V
VIH	Input High Voltage	2.0	VCC + 5.5	V
VOL	Output Low Voltage (LOL = 4.0mA)		0.4	V
VOH	Output High Voltage (IOH = -1.6mA)	2.4		V
IIL	Input Leakage Current (VIN = VCC)		10	uA
IOZ	Tri-State Leakage Current		10	uA
CIN	Input Capacitance		10	pF
COUT	Output Capacitance		10	pF
ICC	Power Supply Current		80	mA

6.3 AC Characteristics - 33MHz *Preliminary*

Temperature: 0°C to 70°C, Vcc: 5V ± 5%

Sym	Description[1]	Min	Typical	Max	Units
t103	CPURST active delay from CLKI↓[2]	6		11	ns
t104	CPURST inactive delay from CLKI↓	6		11	ns
t201	CAS# active to RAS0# active delay	30			ns
t203	RAS0# active to RAS1# active delay	30			ns
t205	RAS# pulse width	80			ns
t210	LDEV# setup time to CLKI↑[3]	8			ns
t211	LDEV# hold time to CLKI↑	5			ns
t213	KEN# active delay from CLKI↑			15	ns
t214	KEN# inactive delay from CA[31:2]			20	ns
t215	RDYI# setup time to CLKI↑	8			ns
t216	RDYI# hold time to CLKI↑	5			ns
t402	CPU address and status valid to BEOE# active delay			21	ns
t403	CLKI↑ to BEOE#/BOOE# inactive delay			13	ns
t404	CLKI↑ to BEOE#/BOOE# active delay			14	ns
t405	CLKI↓ to CA32S# inactive delay			14	ns
t406	CLKI↓ to CA32S# active delay			14	ns
t407	CLKI↑ to BRDY# active delay	8		20	ns
t408	CLKI↑ to BRDY# inactive delay	8		20	ns
t411	CLKI↑ to CAWE1#/CAWE0# active delay			14	ns
t412	CLKI↓ to CAWE1#/CAWE0# inactive delay			14	ns
t419	CLKI↑ to RDY# active delay	8		20	ns
t420	CLKI↑ to RDY# inactive delay	8		20	ns
t423	CLKI↓ to TAGWE# active delay	10		18	ns
t424	CLKI↓ to TAGWE# inactive delay	10		18	ns
t425	CPU address and status valid to BEA3 and BOA3/BEA2 active delay			18	ns
t426	CLKI↑ to BEA3 and BOA3/BEA2 inactive delay			18	ns
t428	TAG(7:0) invalid delay from CLKI↑	1			ns
t429	CLKI↑ to CAS# active delay	10		14	ns
t430	CLKI↑ to CAS# inactive delay	10		14	ns
t433	CLKI↑ to RAS# inactive delay	10		14	ns
t434	CLKI↑ to RAS# active delay	10		14	ns
t435	CLKI↑ to column address valid delay	10		14	ns
t436	CLKI↑ to row address hold time	20		24	ns

6.3 AC Characteristics - 33MHz *Preliminary* (cont.)

Temperature: 0°C to 70°C, Vcc: 5V ± 5%

Sym	Description[1]	Min	Typical	Max	Units
t437	CLKI↑ to DWE# active delay	10		14	ns
t438	CLKI↑ to DWE# inactive delay	10		14	ns
t439	CLKI↑ to new row address delay	10		14	ns
t440	RAS# precharge time		4 CLKI		
t441	CAS# precharge time		1 CLKI		
t443	CLKI↑ to row address valid time	10		14	ns
t454	MRD# active to BEOE#/BOOE# active delay	10		20	ns
t455	MRD# inactive to BEOE#/BOOE# inactive delay	10		20	ns
t458	MRD#/MWR# active to RAS# active delay	10		20	ns
t459	MRD#/MWR# inactive to RAS# inactive delay	10		20	ns
t460	CLKI↓ to CAS# active delay	10		20	ns
t461	CLKI↓ to CAS# inactive delay	10		20	ns
t462	CLKI↓ to column address active delay	10		15	ns
t463	CLKI↓ to row address hold time	10		15	ns
t464	MWR# active to CAWE1#/CAWE0# active delay		1 CLK		ns
t465	MWR# active to DWE# active delay	10		20	ns
t466	MWR# inactive to DWE# inactive delay	10		20	ns
t501	ATCLK↓ to ALE active delay	10		30	ns
t502	ATCLK↑ to ALE inactive delay	10		30	ns
t503	ATCLK↓ to CMD[4] active delay	10		30	ns
t504	ATCLK↑ to CMD inactive delay	10		30	ns
t505	ATCLK↑ to CMD active delay	10		30	ns
t506	M16# to ATCLK↑ setup time	10			ns
t507	M16# to ATCLK↑ hold time	10			ns
t508	IO16# to ATCLK↑ setup time	10			ns
t509	IO16# to ATCLK↑ hold time	10			ns
t510	NOWS# to ATCLK↓ setup time	10			ns
t511	NOWS# to ATCLK↓ hold time	20			ns
t512	CHRDY to ATCLK↑ setup time	10			ns
t513	CHRDY to ATCLK↑ hold time	20			ns
t515	ATCLK↓ to HOLD active delay	5		16	ns
t516	ATCLK↑ to HOLD inactive delay	5		16	ns
t517	ATCLK↑ to RFSH# active delay	8		30	ns
t518	ATCLK↑ to RFSH# inactive delay	8		30	ns

6.3 AC Characteristics - 33MHz *Preliminary* (cont.)

Temperature: 0°C to 70°C, Vcc: 5V ± 5%

Sym	Description[1]	Min	Typical	Max	Units
t519	ATCLK↑ to MRD# active delay	5		25	ns
t520	ATCLK↑ to MRD# inactive delay	5		25	ns
t601	CLKI↑ to EADS# active delay	8		20	ns
t602	CLKI↑ to EADS# inactive delay	8		20	ns
t603	HITM# to CLKI↑ setup time	8			ns
t604	AHOLD to CLKI↑ active delay	8		20	ns

1.The capacitance loading is 50 pF

2.↓ means falling edge

3.↑ means rising edge

4.CMD equals memory read/write or I/O read/write.

6.4 AC Characteristics - 50MHz *Preliminary*

Temperature: 0°C to 70°C, Vcc: 5V ± 5%

Sym	Description[1]	Min	Typical	Max	Units
t103	CPURST active delay from CLKI↓[2]	6		11	ns
t104	CPURST inactive delay from CLKI↓	6		11	ns
201	CAS# active to RAS0# active delay	20			ns
t203	RAS0#, active to RAS1# active delay	20			ns
t205	RAS# pulse width			80	ns
t210	LDEV# setup time to CLKI↑[3]	8			ns
t211	LDEV# hold time to CLKI↑	5			ns
t213	KEN# active delay from CLKI↑			15	ns
t214	KEN# inactive delay from CA[31:2]			20	ns
t215	RDYI# setup time to CLKI↑	8			ns
t216	RDYI# hold time to CLKI↑	5			ns
t402	CPU address and status valid to BEOE#/BOOE# active delay			21	ns
t403	CLKI↑ to BEOE#/BOOE# inactive delay			13	ns
t404	CLKI↑ to BEOE#/BOOE# active delay			14	ns
t405	CLKI↓ to CA32S# inactive delay			14	ns
t406	CLKI↓ to CA32S# active delay			14	ns
t407	CLKI↑ to BRDY# active delay	8		20	
t408	CLKI↑ to BRDY# inactive delay	8		20	
t407	CLKI↑ to BRDY# active delay	8		20	ns

6.4 AC Characteristics - 50MHz *Preliminary* (cont.)

Temperature: 0°C to 70°C, Vcc: 5V ± 5%

Sym	Description[1]	Min	Typical	Max	Units
t408	CLKI↑ to BRDY# inactive delay	8		20	ns
t411	CLKI↑ to CAWE1#/CAWE0# active delay			12	ns
t412	CLKI↓ to CAWE1#/CAWE0# inactive delay			12	ns
t419	CLKI↑ to RDY# active delay	8		20	ns
t420	CLKI↑ to RDY# inactive delay	8		20	ns
t423	CLKI↓ to TAGWE# active delay	10		18	ns
t424	CLKI↓ to TAGWE# inactive delay	10		18	ns
t425	CPU address and status valid to BEA3 and BOA3/BEA2 active delay			18	ns
t426	CLKI↑ to BEA3 and BOA3/BEA2 active delay			18	ns
t428	TAG(7:0) invalid delay from CLKI↑	1			ns
t429	CLKI↑ to CAS# active delay	10		14	ns
t430	CLKI↑ to CAS# inactive delay	10		14	ns
t433	CLKI↑ to RAS# inactive delay	10		14	ns
t434	CLKI↑ to RAS# active delay	10		14	ns
t435	CLKI↑ to column address valid delay	10		14	ns
t436	CLKI↑ to row address hold time	20		24	ns
t437	CLKI↑ to DWE# active delay	10		14	ns
t438	CLKI↑ to DWE# inactive delay	10		14	ns
t439	CLKI↑ to new row address delay	10		14	ns
t440	RAS# precharge time		4 CLKI		
t441	CAS# precharge time		1 CLKI		
t443	CLKI↑ to row address valid time	10		14	ns
t454	MRD# active to BEOE#/BOOE# active delay	10		20	ns
t455	MRD# inactive to BEOE#/BOOE# inactive delay	10		20	ns
t458	MRD#/MWR# active to RAS# active delay	10		20	ns
t459	MRD#/MWR# inactive to RAS# inactive delay	10		20	ns
t460	CLKI↓ to CAS# active delay	10		20	ns
t461	CLKI↓ to CAS# inactive delay	10		20	ns
t462	CLKI↓ to column address active delay	10		15	ns
t463	CLKI↓ to row address hold time	10		15	ns
t464	MWR# active to CAWE1#/CAWE0# active delay		1 ATCLK		
t465	MWR# active to DWE# active delay	10		20	ns
t466	MWR# inactive to DWE# inactive delay	10		20	ns
t501	ATCLK↓ to ALE active delay	10		30	ns

6.4 AC Characteristics - 50MHz *Preliminary* (cont.)

Temperature: 0°C to 70°C, Vcc: 5V ± 5%

Sym	Description[1]	Min	Typical	Max	Units
t502	ATCLK↑ to ALE inactive delay	10		30	ns
t503	ATCLK↓ to CMD[4] active delay	10		30	ns
t504	ATCLK↑ to CMD inactive delay	10		30	ns
t505	ATCLK↑ to CMD active delay	10		30	ns
t506	M16# to ATCLK↑ setup time	10			ns
t507	M16# to ATCLK↑ hold time	10			ns
t508	IO16# to ATCLK↑ setup time	10			ns
t509	IO16# to ATCLK↑ hold time	10			ns
t510	NOWS# to ATCLK↓ setup time	10			ns
t511	NOWS# to ATCLK↓ hold time	20			ns
t512	CHRDY to ATCLK↑ setup time	10			ns
t513	CHRDY to ATCLK↑ hold time	20			ns
t515	ATCLK↓ to HOLD active delay	5		16	ns
t516	ATCLK↑ to HOLD inactive delay	5		16	ns
t517	ATCLK↑ to RFSH# active delay	8		30	ns
t518	ATCLK↑ to RFSH# inactive delay	8		30	ns
t519	ATCLK↑ to MRD# active delay	5		25	ns
t520	ATCLK↑ to MRD# inactive delay	5		25	ns
t601	CLKI↑ to EADS# active delay	8		20	ns
t602	CLKI↑ to EADS# inactive delay	8		20	ns
t603	HITM# to CLKI↑ setup time	6			ns
t604	AHOLD to CLKI↑ active delay	8		16	ns

1.The capacitance loading is 50 pF

2.↓ means falling edge

3.↑ means rising edge

4.CMD equals memory read/write or I/O read/write.

6.5 Timing Characteristics

Figure 6-1 Read-Miss Cycle, (64KB/256KB Cache) (1 of 3)

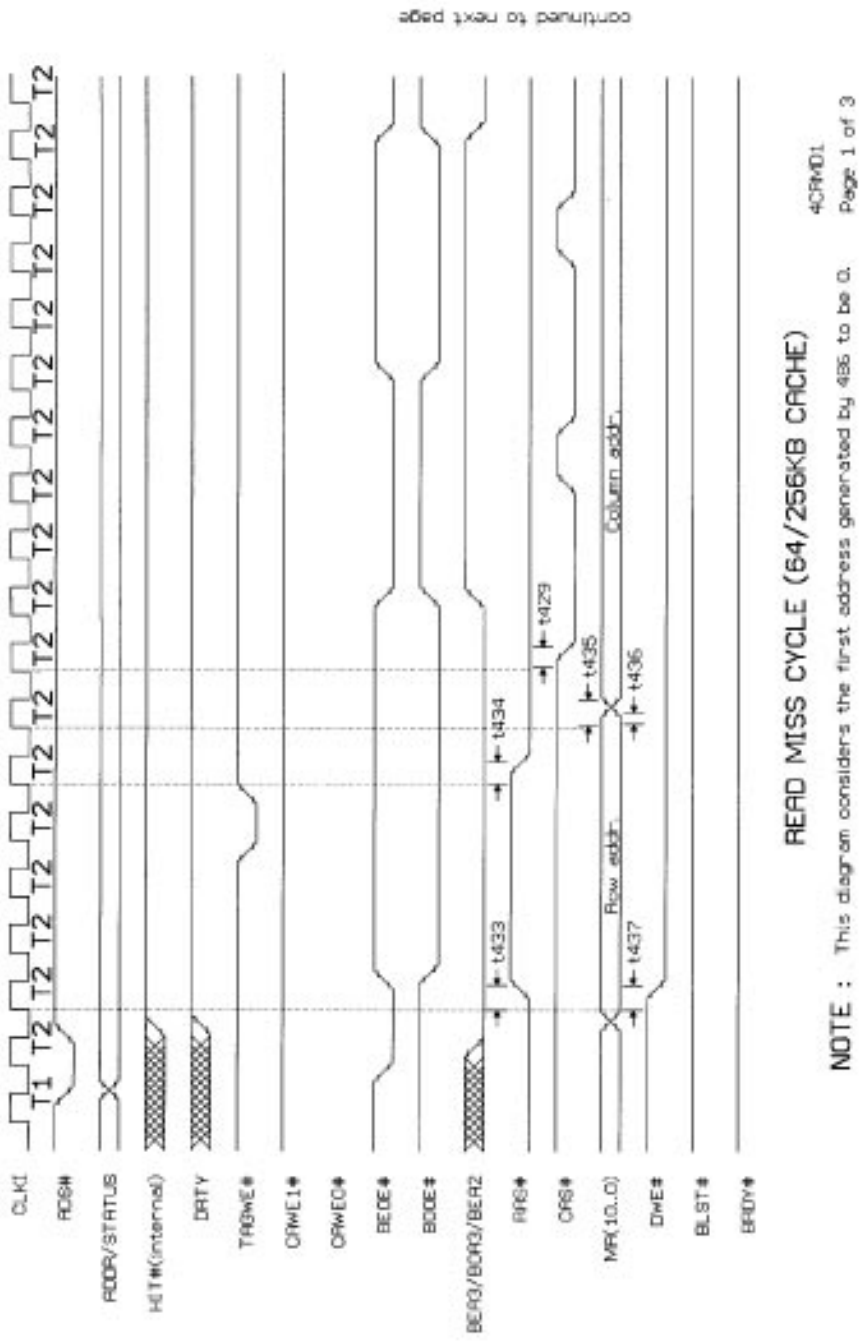


Figure 6-2 Read-Miss Cycle, (64KB/256KB Cache) (2 of 3)

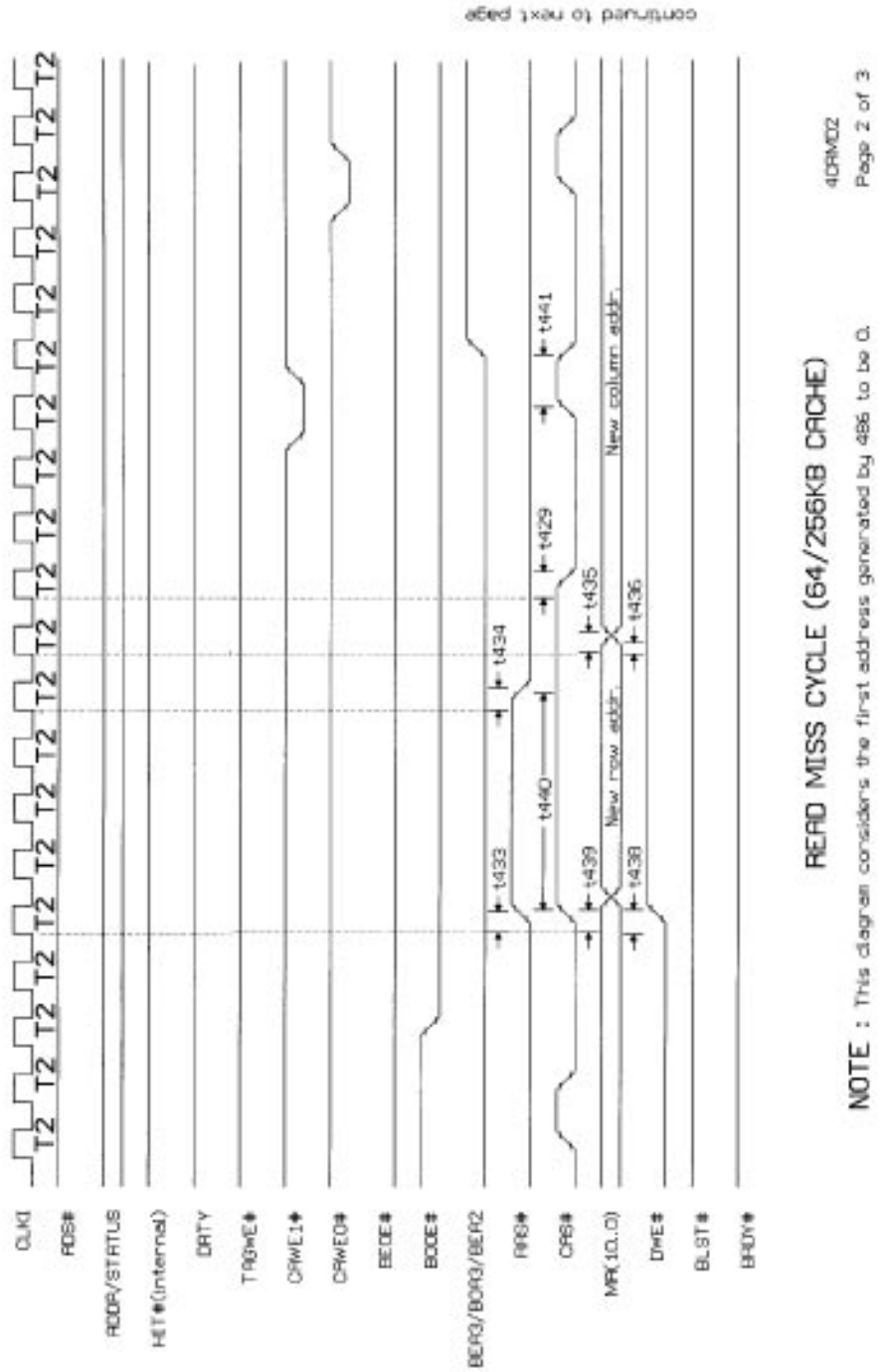


Figure 6-3 Read-Miss Cycle, (64KB/256KB Cache) (3 of 3)

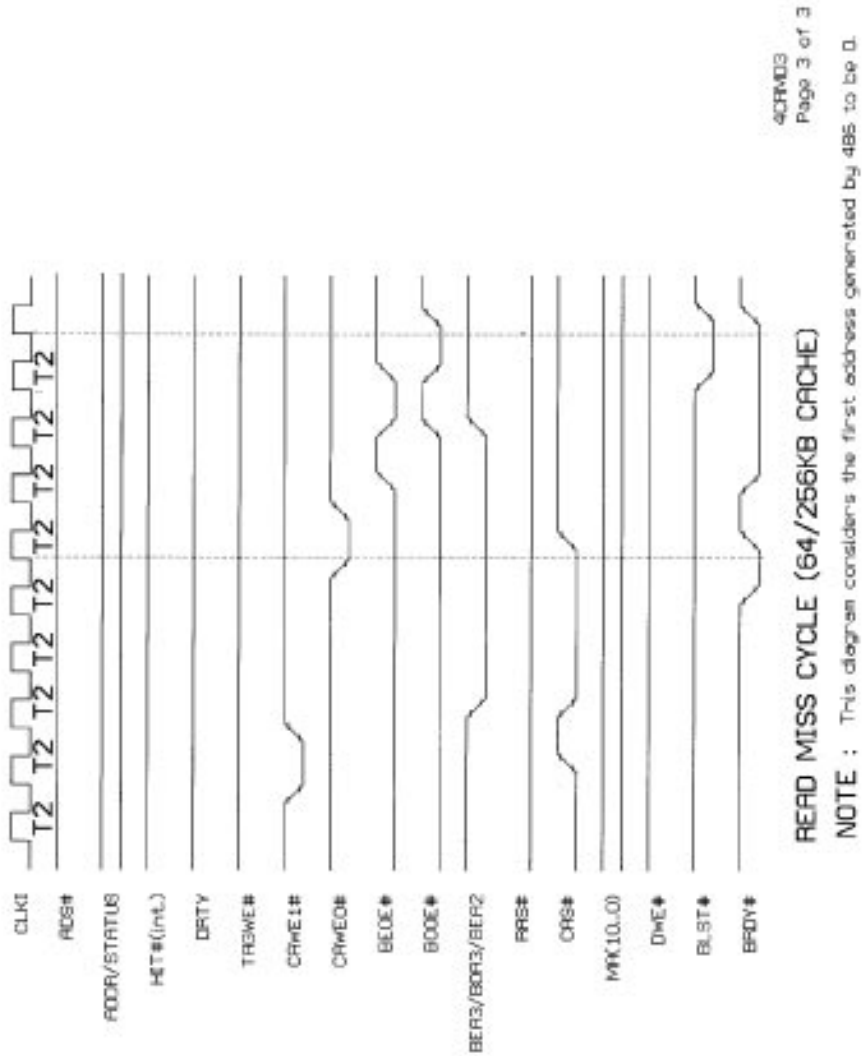


Figure 6-4 486 Secondary Cache Read Hit Cycle, Bank Interleave (64KB/256KB)

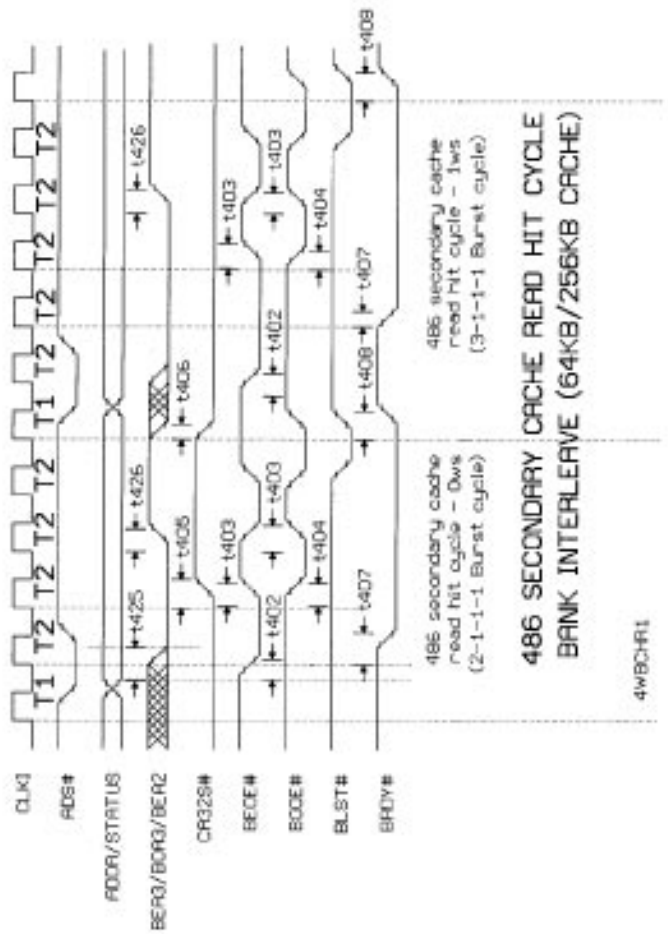


Figure 6-5 486 Secondary Cache Read Hit Cycle, Single Bank (128KB/512KB)

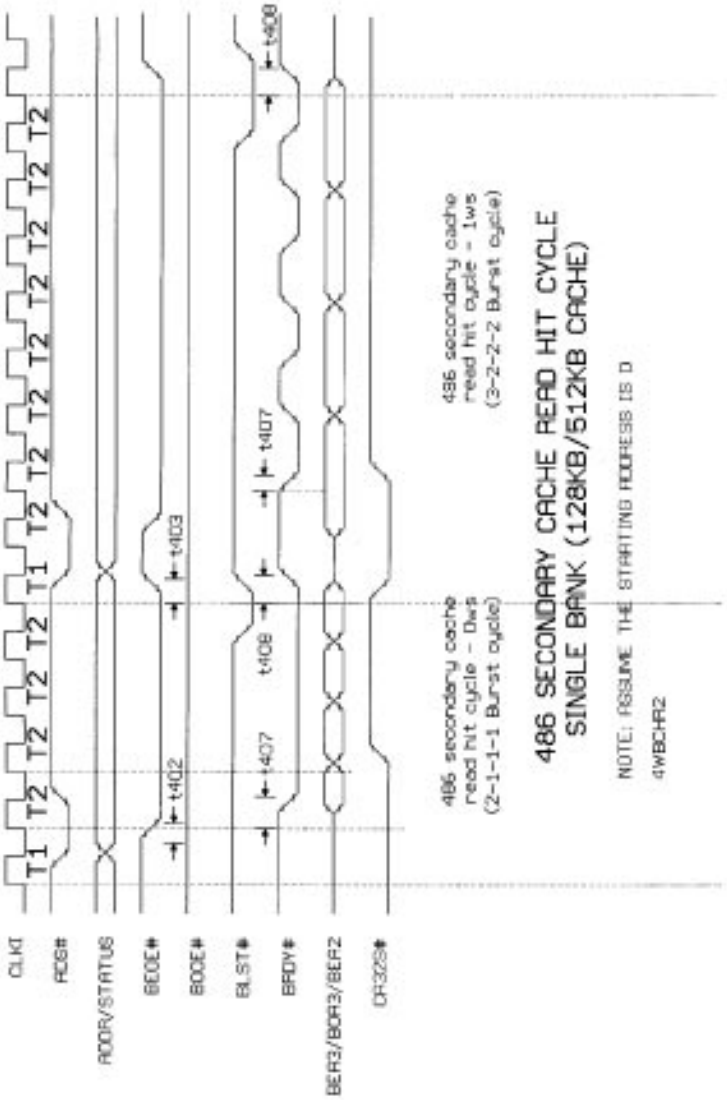


Figure 6-6 486 Secondary Cache Write Hit Cycle

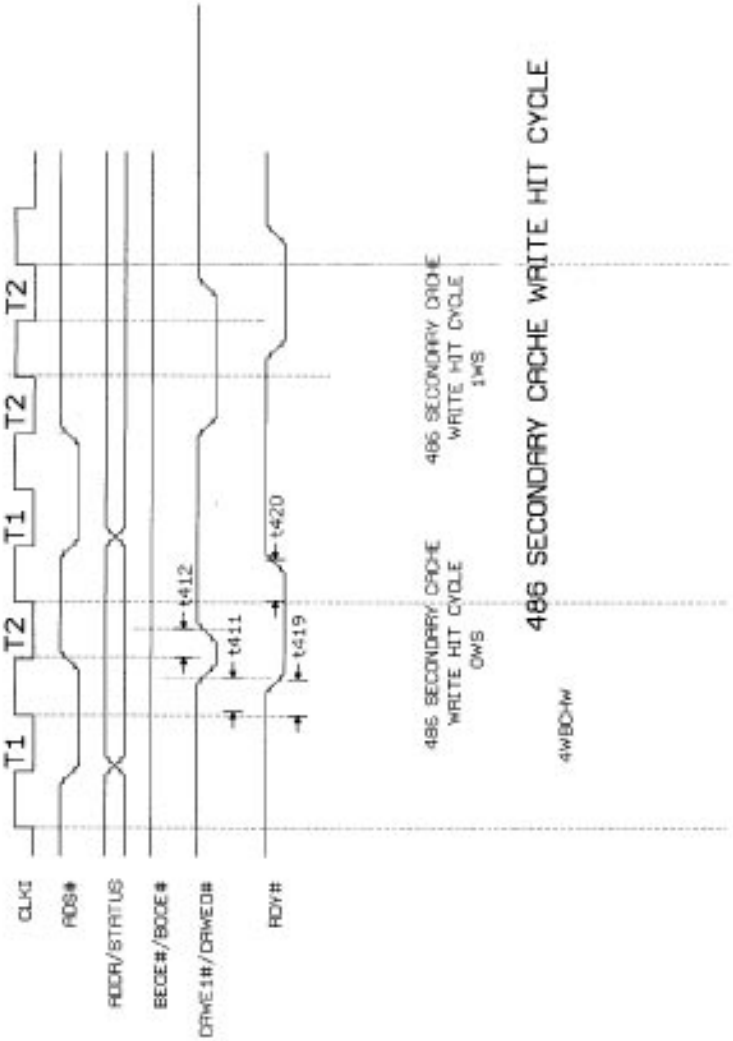


Figure 6-7 Read-Miss Cycle, (128KB/512KB Cache) (1 of 3)

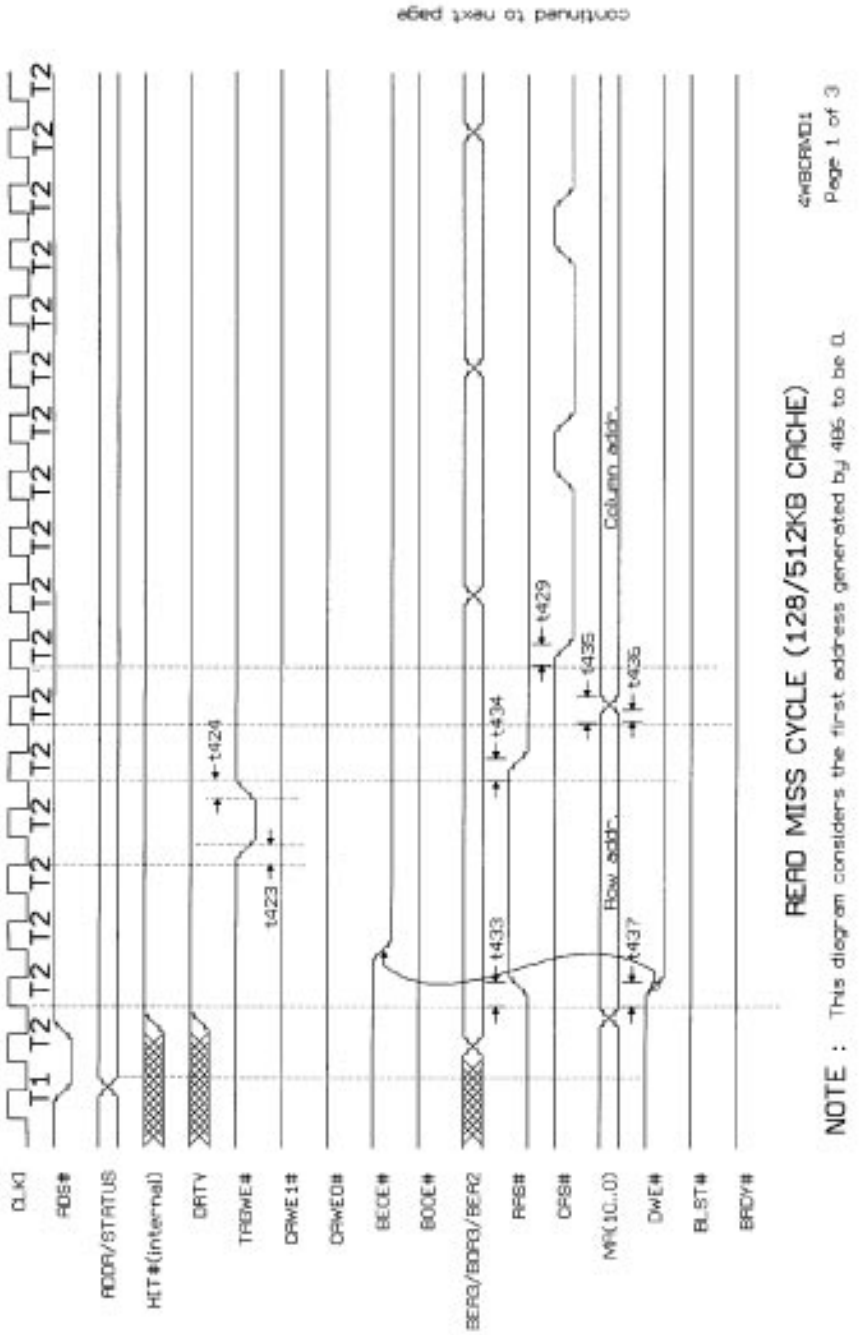


Figure 6-8 Read-Miss Cycle, (128KB/512KB Cache) (2 of 3)

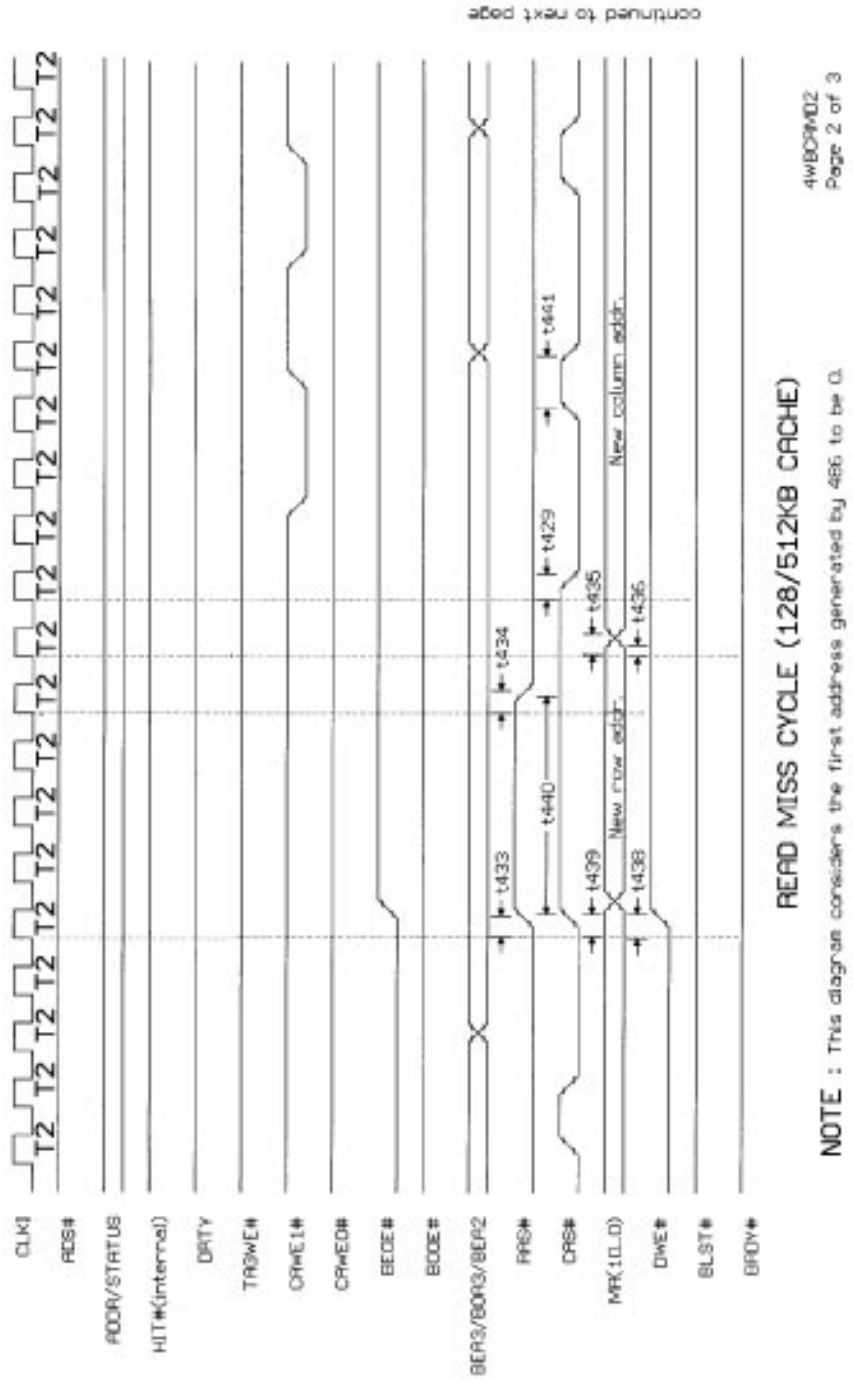


Figure 6-9 Read-Miss Cycle, (128KB/512KB Cache) (3 of 3)

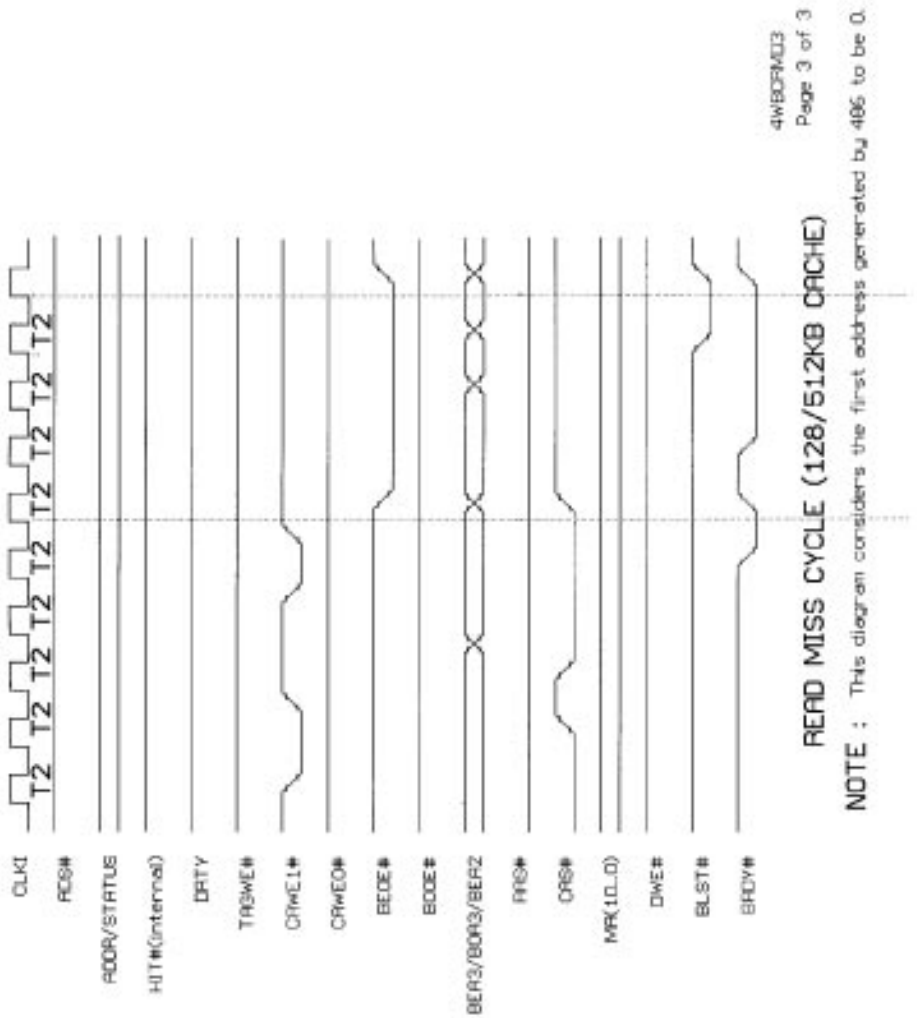


Figure 6-10 486 Secondary Cache Write Miss Cycle

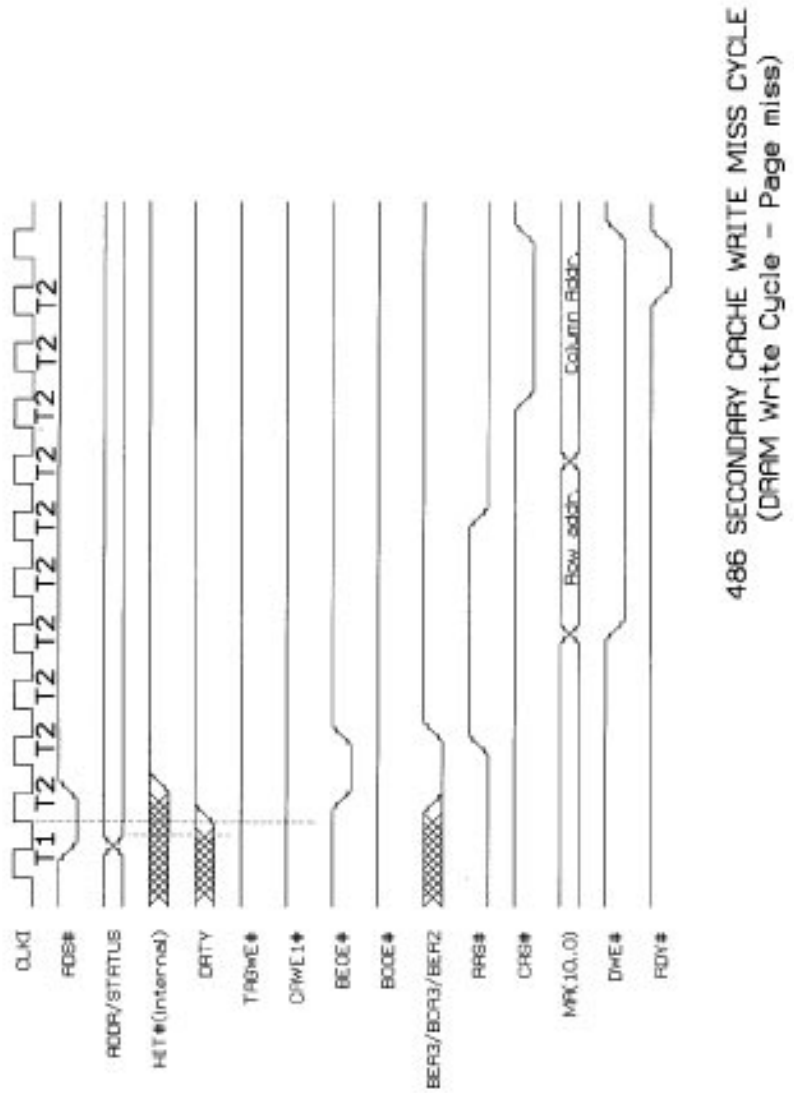


Figure 6-11 DMA Read Cycle - Secondary Cache Hit

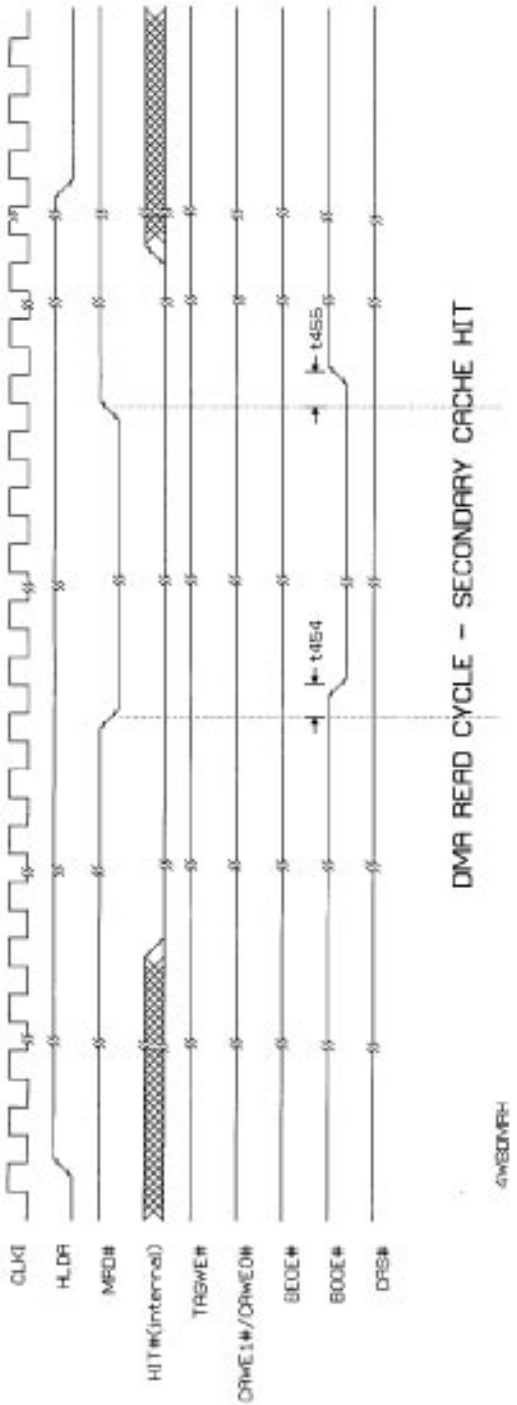


Figure 6-12 DMA Read Cycle - Secondary Cache Miss

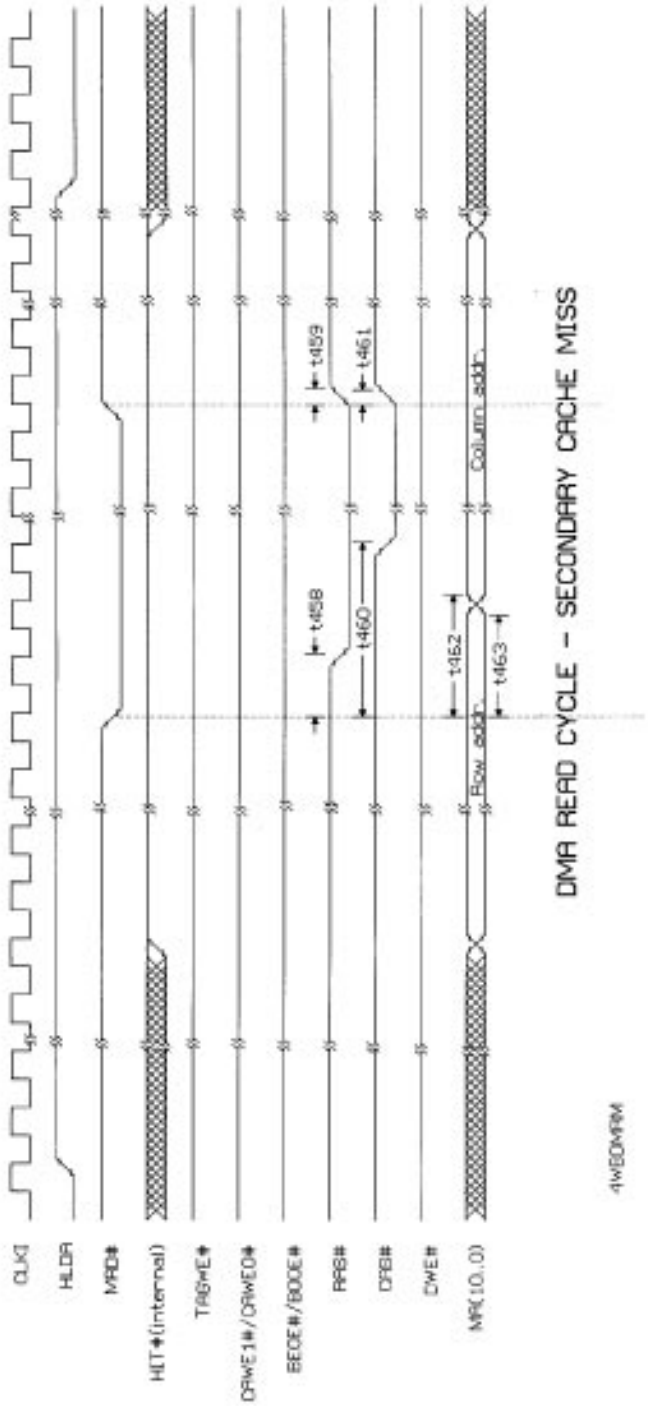


Figure 6-13 DMA Write Cycle - Secondary Cache Hit

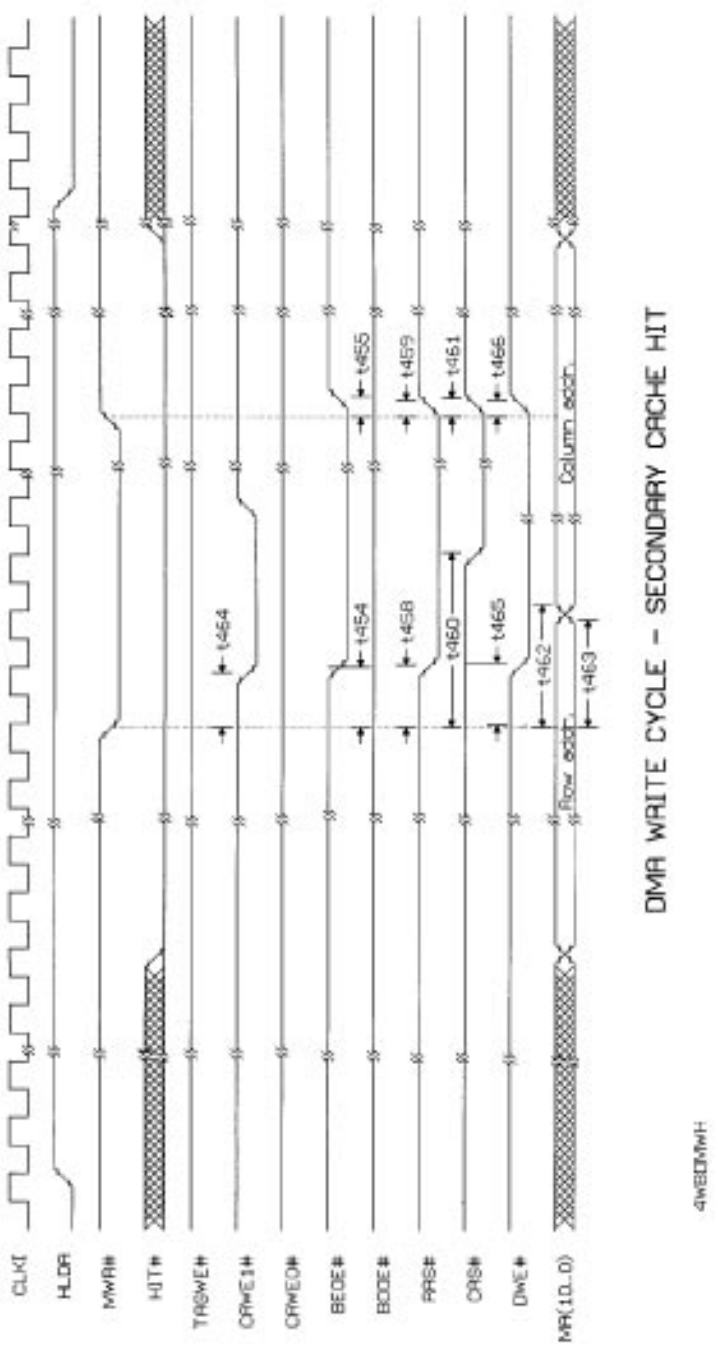


Figure 6-14 DMA Write Cycle - Secondary Cache Miss

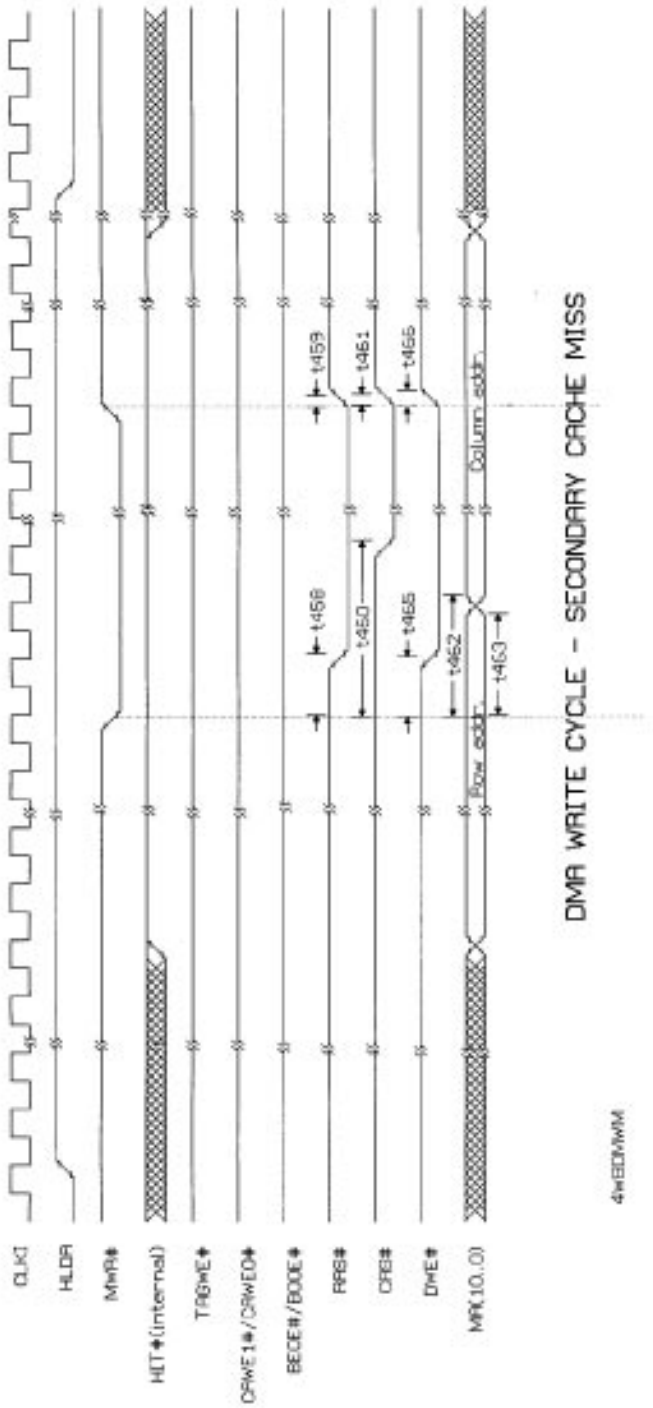


Figure 6-15 DRAM Read Cycle

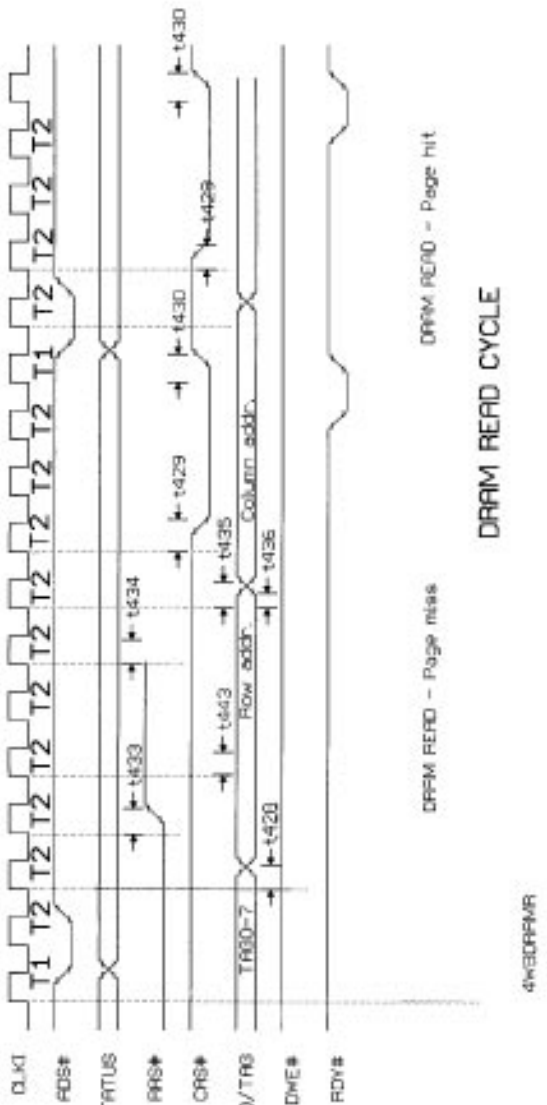


Figure 6-16 DRAM Write Cycle

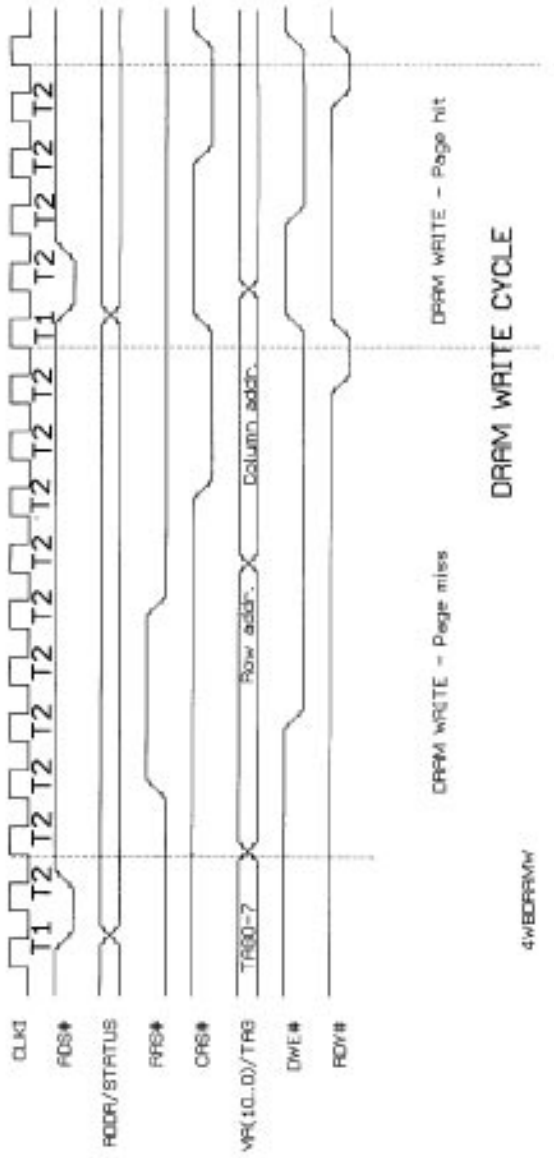


Figure 6-17 AT BUS Hold Timing

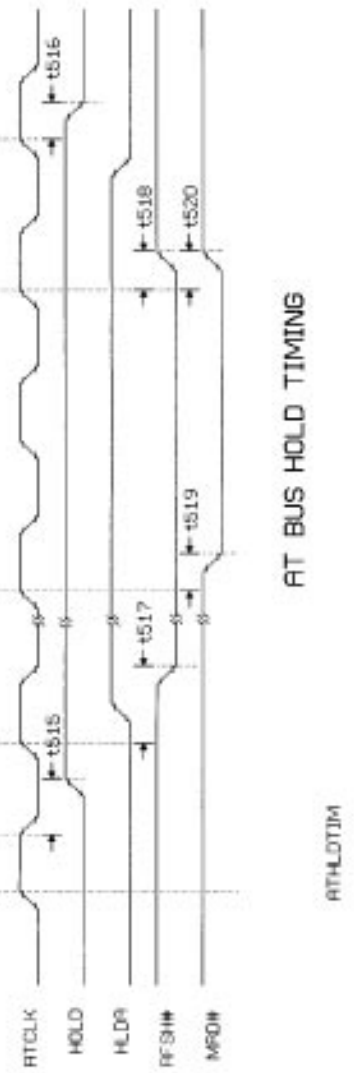


Figure 6-18 AT BUS Timing

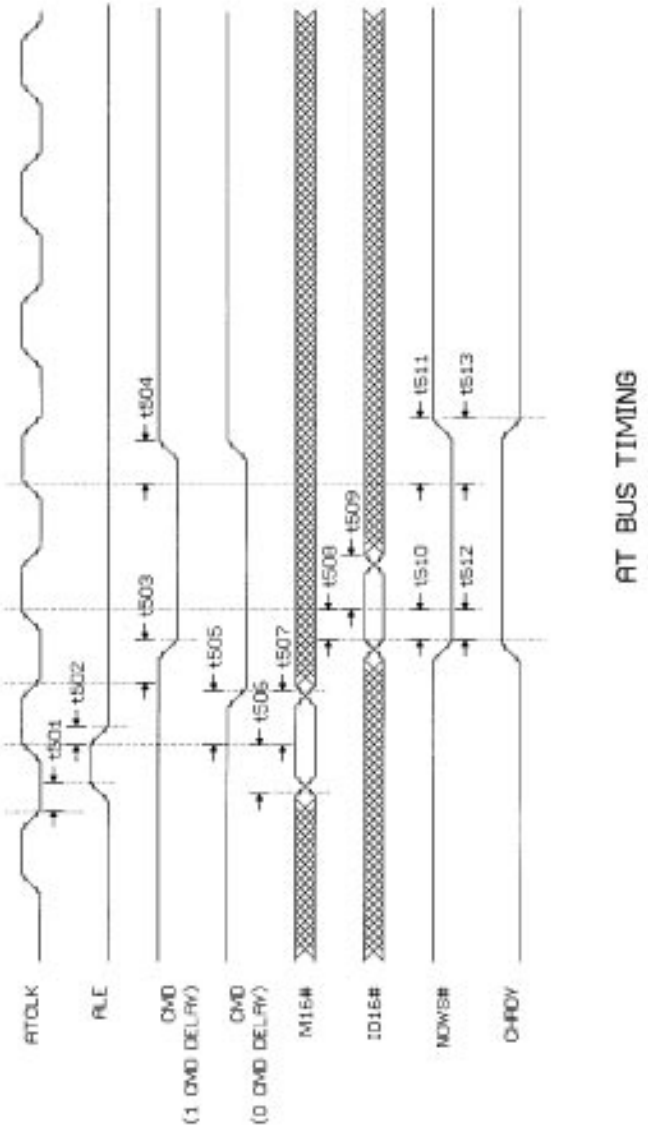


Figure 6-19 Local Device Cycle

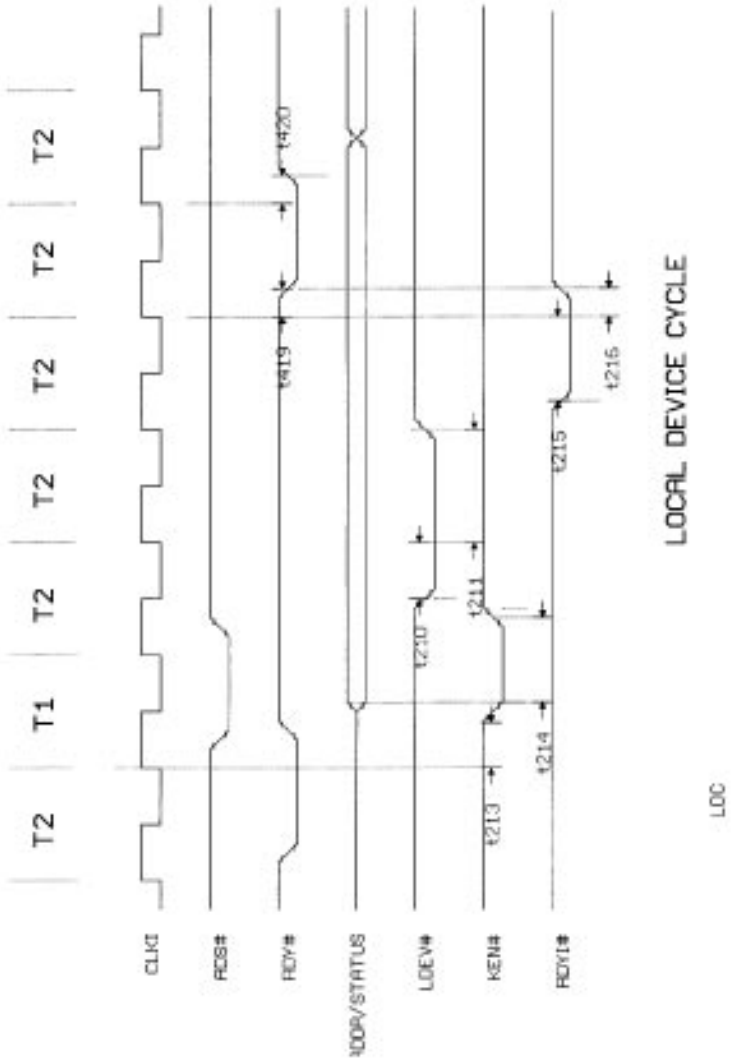


Figure 6-20 Reset Timing and Refresh Cycle

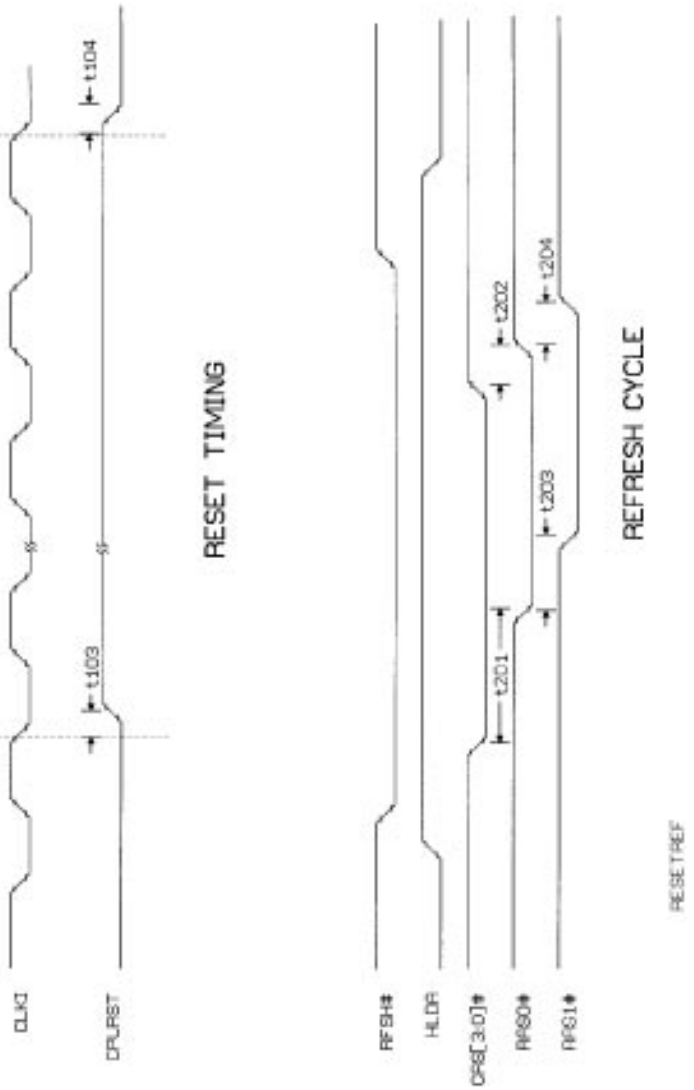


Figure 6-21 L1 Write Back Cycle - (HITM# Active) Local Bus Master (page 1 of 2)

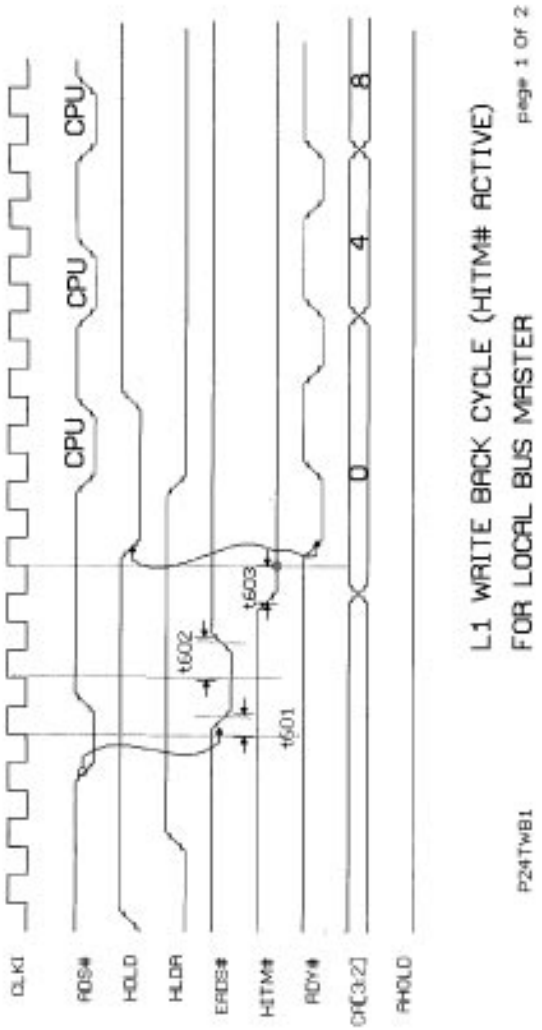


Figure 6-22 L1 Write Back Cycle - (HITM# Active) Local Bus Master (page 2 of 2)

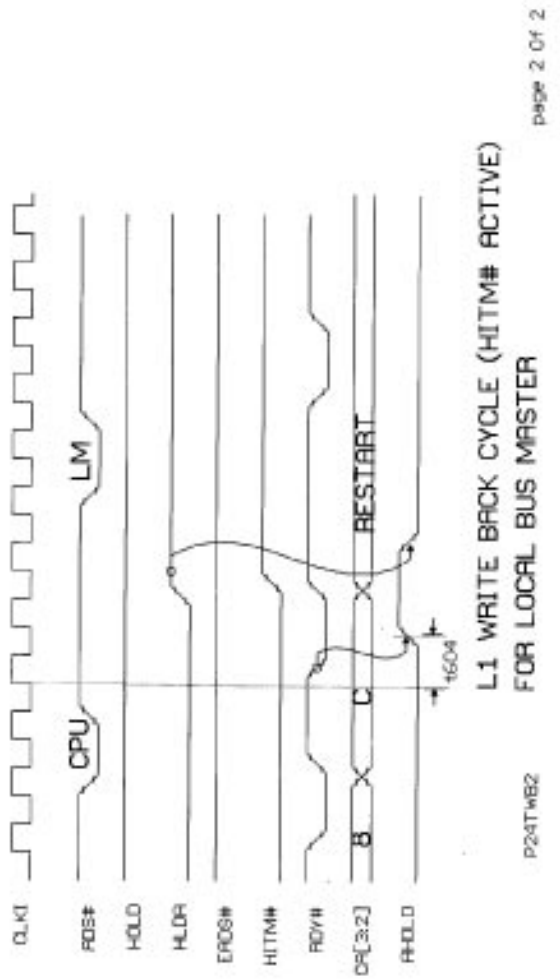


Figure 6-23 L1 Write Back Cycle - (HITM# Active) DMA/ISA Bus Master (page 1 of 2)

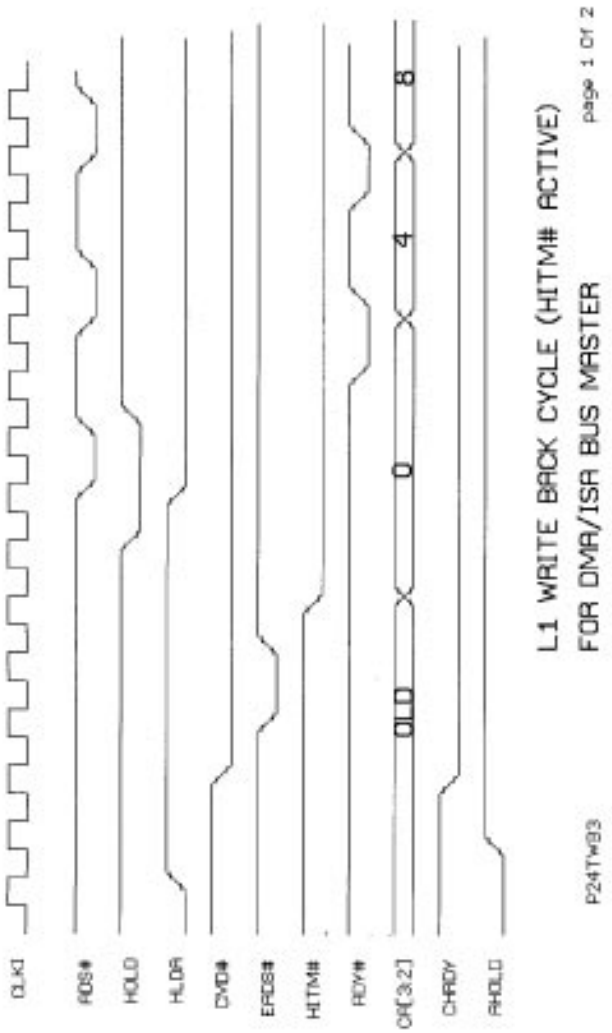
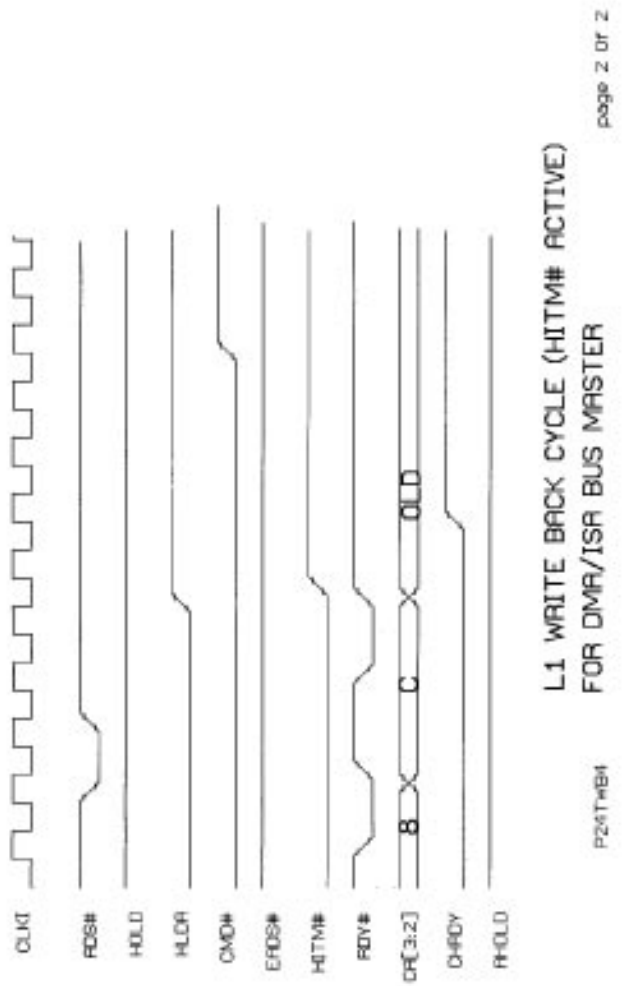
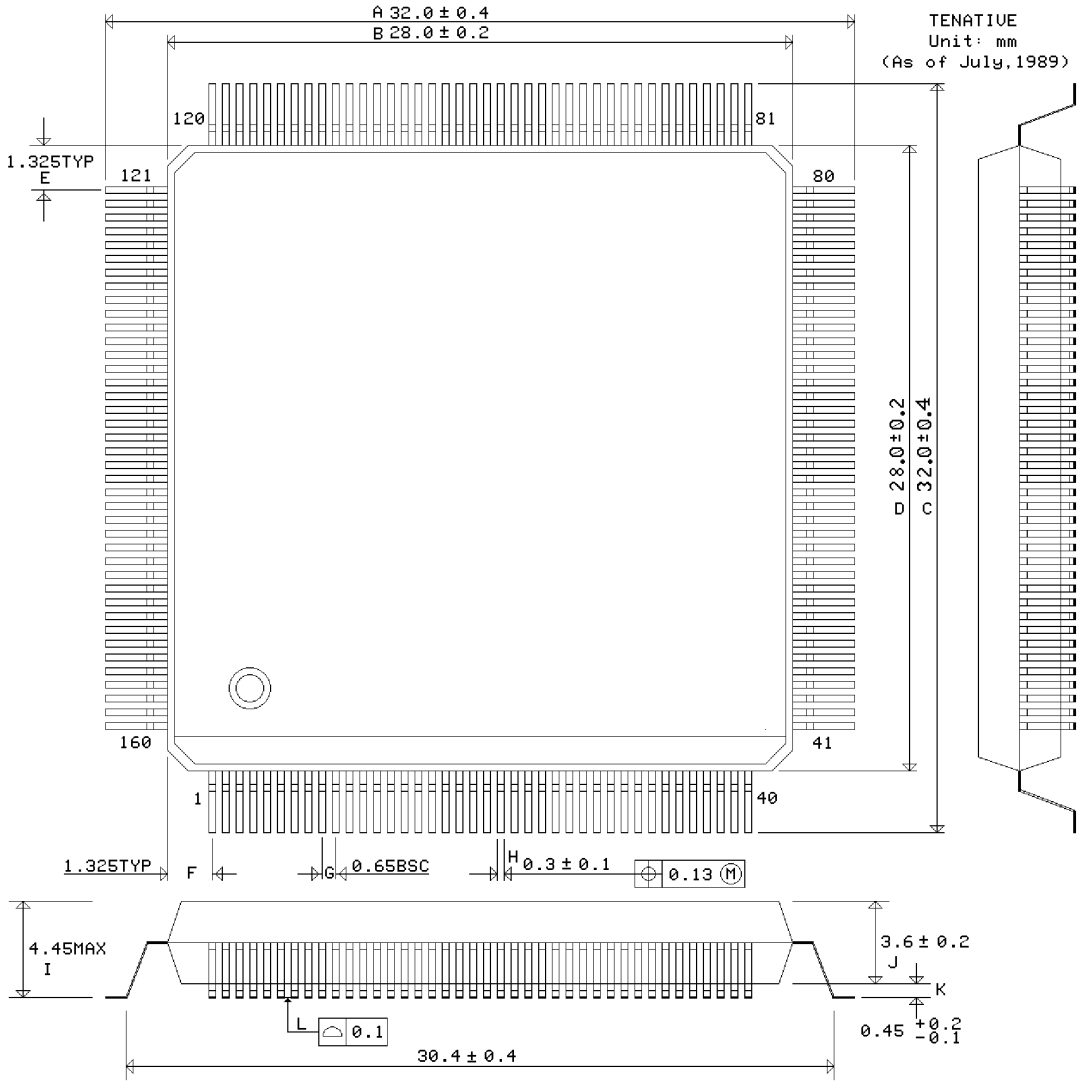


Figure 6-24 L1 Write Back Cycle - (HITM# Active) DMA/ISA Bus Master (page 2 of 2)



7.0 Mechanical Package



DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	31.6	32.4	1.244"	1.276"	Maximum Width LEAD TO LEAD
B	27.8	28.2	1.094"	1.110"	Maximum Width PACKAGE ENVELOPE
C	31.6	32.4	1.244"	1.276"	Maximum Height LEAD TO LEAD
D	27.8	28.2	1.094"	1.110"	Maximum Height PACKAGE ENVELOPE
E	1.325 TYP		.0522" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	1.325 TYP		.0522" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.65 BSC		.0256" BSC		LEAD TO LEAD CENTER SPACING
H	0.2	0.4	.008"	.016"	LEAD WIDTH
I	——	4.45	——	.175"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	3.4	3.8	.134"	.150"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.35	0.65	.0138"	.0256"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.1	——	.004"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.01"	LEAD THICKNESS
N	0.6	1.0	.024"	.039"	LEAD FOOTPRINT