HiD/386 AT CHIPSET
HIGH INTEGRATION DIRECT MAPPED CACHE AT
82C381/82C382D-25/33

100% IBM PC/AT Compatible 386/AT Chipset for 25 and 33 MHz systems

Designed to provide the most cost-effective, high performance Cache based 386/AT with high integration

Advanced Memory Controller design
- o **Direct support for 64KB, 128KB and larger-Cache Subsystems**
- o **Implements sophisticated DRAM Controller with Paging in odd banks and 2/4 way Page Interleaving with even banks**
- o **BIOS Shadow Ram**
- o **256K Relocation to top of Memory**
- o **Non-Cacheable programmable memory regions, and GateA20 support**

Software configurable Command Delays, Wait States and Memory Organization

Synchronous AT Bus Clock with programmable CPU Clock divide options: by 2, by 3 and by 4

Complete AT/386 system board requires only 20 components plus memory

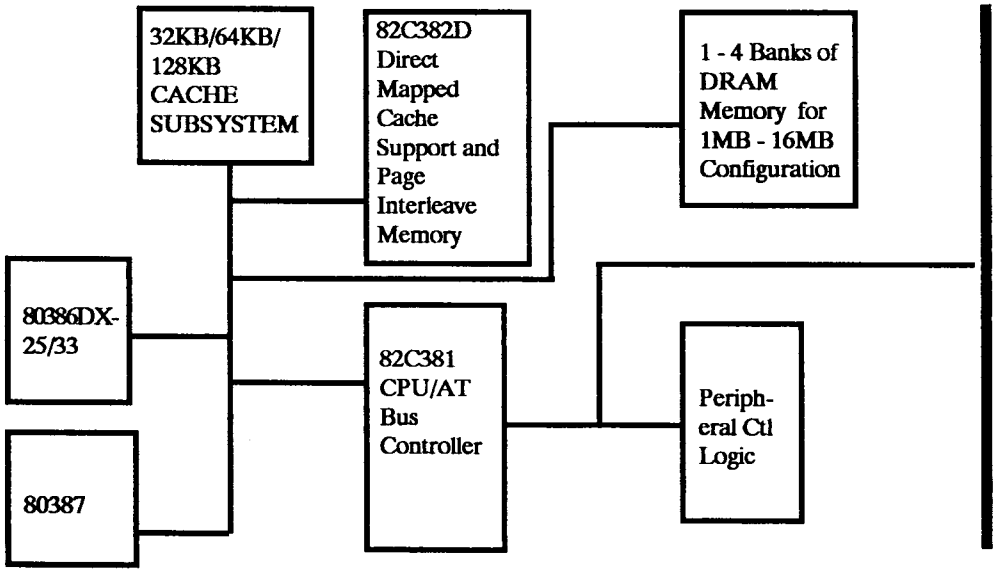
Single EPROM configuration

Targeted at very high performance 32-bit power PCs and file-server designs

Low power, high speed 1.2u CMOS Technology

The HiD/386 Chipset, 82C381 and 82C382D, support high integration implementations of Direct Mapped Cache with 32KB/64KB/128KB Cache for 25 and 33 MHz 386/AT Personal Computers. Combined with the 82C206 Integrated Peripherals Controller, it integrates the 386/AT motherboard to under 20 devices, plus memory. It is designed to cost reduce discrete and CHIPS' CS8230 based 82385 Cache 386/AT designs, as well as boost the performance of these designs to 33 MHz, with >64KB Cache.

The 82C381 provides system control logic and data bus conversion logic. The control logic consists of 386 CPU control logic, AT Bus cycle control, 387 Numeric Processor control logic, synchronous clock divide logic and control of the local peripheral bus. The data bus conversion logic consists of various 8, 16, 32 bit conversions for ROM cycles, AT bus cycles and memory cycles.



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The 82C382D performs the Memory Management functions for the HiD/AT chipset. It is designed to optimize cost of high performance 386/AT systems with 64KB, 128KB or larger Direct Mapped Cache Memory. It also implements logic to maintain compatibility in the AT environment . It provides a Page Interleave backend for main DRAM memory, in order to improve performance during miss cycles. It also has features for reducing system cost.

It minimizes Cache Memory cost by allowing the use of slow SRAM; by supporting single EPROM BIOS configurations; putting DRAM on the local bus and consequently reducing DRAM speeds by 15ns typically; and by remapping 256K of DRAM between 640K and 1024K to top of main memory.

It provides a very flexible implementation of paging for the main DRAM memory. For even bank configurations, it provides 2-way or 4-way interleaving; for odd banks it provides paging. This provides a flexible approach to increasing the size of the local memory as software demands increase, without imposing a penalty on performance.

Finally, memory performance is optimised by shadow RAM techniques for BIOS ROMs; concatenated pages for multiple bank configurations; paging for odd banks; and variable page size for larger DRAMs.

System Architecture

The HiD/AT chipset is compatible with the 82C206 Integrated Peripherals Controller. Consequently, with the 82C206, a very high integration and very high performance 386/AT can be implemented. A typical motherboard can be designed with less than 20 devices plus memory.

For larger AT designs, targeted at file-servers and departmental computers, designs with 8 or more slots can be supported with external AT bus drivers.

Ordering Information

82C381-25 or 82C381-33= 386/AT Advanced CPU Controller for 25 MHz and 33 MHz respectively
82C382D-25 or 82C382D-33 = 386/AT Direct Mapped/ Page Interleave Memory Controller for 25 MHz and 33 MHz respectively
HiD/386-25 = 25 MHz Direct Mapped 82C381-25 and 82C382D -25 chipset
HiD/386-33 = 33 MHz Direct Mapped 82C381-33 and 82C382D-33 chipset
DK/HiD-386 = 25 MHz Development Kit with 1MB DRAM and 386-25

(See Development Kit Price list for complete details)

Order Number	Speed	Package Type
F82C381D	-25, -33	PFP-160 pins
F82C382D	-25,-33	PFP-136 pins
DK/HiD-386	-25	Baby AT

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OPTi

82C381_B AT/386 High Integration CPU Controller

V1.1, December 12, 1989

1.0 The HiD/386 Chipset consists of the 82C381_B and 82C382_B. Together, they are designed to implement high performance, highly integrated, 386/AT Personal Computers operating at 20, 25 and 33 MHz. The 82C381_B provides CPU control and Bus Conversion functions, while the 82C382_B provides Direct Mapped Cache Control (of any size) and 1-16MB of Page Interleave Memory Control. With an Integrated Peripherals Controller like the 82C206 (available from Texas Instruments, Siemens, Chips and Technologies, UMC, Winbond, etc) or VL82C100 (from VLSI Technology), a highly integrated, compact 386/AT can be implemented.

2. Overview

The 82C381_B performs the CPU interface, AT system bus interface and data path control. It provides the following features to 386/AT systems:

* Software programmable AT bus clock & CPU clock.
* CPU interface & bus control.
* OS/2 Alternate Hot RESET support.
* Optimized programmable stretched AT Bus clock.
* Port B register.
* Built-in direct-mapped, flexible cache size cache controller.

2.0 Functional Description

The 82C381_B CPU Controller consists of the following functional sub-modules:

* Reset and Shut Down Logic.
* Clock Generation and Selection Logic.
* CPU State Machine and AT Bus State Machine.
* Bus Arbitration Logic, DMA/Master and Refresh Logic.
* Port B Register and NMI Logic.
* Configuration Registers.
* Data Bus Conversion and Data Path Control Logic.
* Data Buffers and Latches.
* Parity Generation/detection Logic.
* Cache Controller Logic.

2.1 Reset and Shut Down Logic

Two reset inputs RST1# and RST2# are provided on the 82C381_B chip. RST1# is the Power Good signal from the power supply. When RST1# is low, the 82C381_B asserts CPURST for

CPU reset and SYSRST for system reset. RST2# is generated from the 8042 keyboard controller when a CPU warm reset is required. CPURST is also activated by the 82C381_B when a shut down condition is detected from CPU status. Additionally, a low to high transition in REG00<5> causes CPURST to be active after the current I/O command goes inactive and a HALT instruction has been executed. Both CPURST and SYSRST are asserted for at least 128 CLK2 cycles and is synchronized with respect to CLK2 to meet the setup and hold time requirements of the 80386 CPU.

2.2 Clock Generation

The 82C381_B provides two set of synchronous clocks: CLK and ATCLK, and OSC and OSC/12. It has two input clocks, CLK2IN and OSX1. CLK2IN is driven from a TTL crystal oscillator, running at a maximum of 3X the processor clock frequency. OSX1 is the input of a 14.31818 MHz crystal to generate the OSC and OSC/12 clock.

The 82C381_B generates the processor clock, CLK, for driving the 82C382_B memory controller, 80386 CPU, 80387 Coprocessor and 80385 Cache controller. CLK can be derived from CLK2IN or from ICLK which is CLK2IN/2, CLK2IN/3 or CLK2IN/4, and is used internally as the clock of AT Bus State Machine. ATCLK is always half frequency of ICLK. Note that when CLK is derived from CLK2IN, ICLK can be derived from any of the CLK2IN/2, CLK2IN/3 and CLK2IN/4.

2.3 CPU and AT Bus State Machine

In order to achieve maximum performance of the 80386 CPU and maintain 100% IBM PC/AT compatibility, it is desirable to run the local memory at the rated maximum CPU frequency and the AT bus at a slower clock frequency. The two state machines maintain a synchronous protocol, at all times.

2.3.1 CPU State Machine

The interface to the 80386 requires interpretation of the status lines D/C#, W/R# and M/IO# from CPU during phase 1 of T2/T1P and generation of READY# during phase 2 of T2/T2P to the CPU upon completion of the cycle. 82C382_B acts as the arbitrator by sending AF32# to 82C381_B as a flag to trigger the AT Bus State Machine. A low AF32# indicates a 82C382_B local memory cycle, the AT Bus State Machine stays idle, and the CPU State Machine terminates itself by monitoring the active READY# signal from outside. A high AF32# triggers the AT Bus State Machine, and upon completion of the instruction, a synchronized READY# terminates the CPU State Machine as well as all external devices including CPU and 82C382_B.

2.3.2 AT Bus State Machine

The AT Bus State Machine gains control when the 82C382_B's Decoding Logic decodes a non-local memory cycle. It uses BCLK which is twice the frequency of AT system clock ATCLK. It also performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C381_B supports 8 and 16 bit memory or I/O devices located on the AT bus.

An AT bus cycle is initiated by asserting ALE in AT-TS1 state. On the trailing edge of ALE, M16# is sampled for a memory cycle to determine the bus size. It then enters AT-TC state and provides the command signal. For an I/O cycle, IO16# is sampled after the trailing edge of ALE till the end of the command. Typically, the wait state for an AT 8/16 bit transaction is 5/1 respectively. The command cycle is extended when CHRDY is detected inactive, or is terminated when zero wait state request signal NOWS# from the AT bus is active. Upon expiration of the wait states, the AT State Machine terminates itself and passes internal READY to CPU State Machine for outputting synchronous READY# to the 80386.

A one in REG00<4> enables stretched ATCLK. From the beginning of a bus cycle, ATCLK stays high until it receives AF32# from 82C382_B. An AT bus cycle then starts immediately without waiting for the synchronization of ATCLK in order to maximise performance. A local memory cycle drops ATCLK to zero.

2.4 Bus Arbitration Logic, DMA/Master and Refresh Logic

The 82C381_B provides arbitration between the CPU, DRAM refresh logic and DMA/Master devices. It handles HRQ and RFSHRQ by generating HOLD request to the CPU. The CPU will respond to an active HOLD signal by asserting HLDA and placing most of its output and I/O pins in a high impedance state after completing its current bus cycle. After the CPU relinquishes the bus, the 82C381_B responds by issuing RFSH# or HLDAO depending on the requesting device.

The arbitration between Refresh and DMA/Master is based on FIFO (first in first out) priority. However, RFSHRQ will be internally latched and serviced immediately after DMA/Master finishes its request if RFSHRQ is queued behind HRQ. HRQ has to remain active to be serviced if RFSHRQ comes first.

During a refresh cycle, the refresh address is put out on the XA0-XA9 address lines, and XMR# is active 2 SYSCLK after RFSH# is active.

DMA and Bus Master share the same request pin HRQ. After the 82C381_B receives HRQ it asserts HOLD request to the CPU.

Upon finishing the current cycle, the CPU relinquishes the bus by asserting HLDA. The 82C381_B issues HLDAO to the requesting device to start gaining control of the bus. During an active HLDAO period the only way to distinguish between DMA and Bus Master request is to monitor the DMA8# and DMA16# signals. DMA8#/DMA16# active indicates an 8-bit/16-bit DMA transfer, while if both are inactive, it means it is a Master cycle.

2.5 Numeric Processor Interface

Incorporated in the 82C381_B is the circuitry to interface a 80387 Numeric Coprocessor to 80386. The circuitry handles the decoding required for selecting and resetting the Numeric Coprocessor, handling CPBUSY# and CPERR# signals from Coprocessor to the CPU, and generating interrupt signals for error handling.

82C381_B samples ERROR# pin from Coprocessor during power on reset. A low indicates an 80387 is present, and any further Coprocessor cycles will be terminated by an active READY# from the 80387. Otherwise, the 82C381_B is responsible for the READY# return for all the Coprocessor cycles.

While executing a task, the Coprocessor issues a CPBUSY# signal to the 82C381_B and it is passed on to the CPU as BUSY#. If during this busy period, a numeric coprocessor error CPERR# occurs, it results in an internal latching of the BUSY# output and assertion of IRQ13 for a NP exception request. The latched BUSY# stays active until cleared by an I/O write cycle to address 0F0H or 0F1H. IRQ13 is cleared only when CPERR# from Coprocessor is inactive, which can be achieved by executing a coprocessor instruction FNINIT to clear the ERROR status. The Coprocessor is reset through the CPRST output, which can be activated by a system reset or by performing a write operation to I/O port 0F1H. This reset signal is synchronized with CLK and lasts for 128 cycles.

2.6 Port B and NMI Logic

The 82C381_B provides access to Port B, IO port address 61H, defined for the PC/AT as shown in Table 1.1.

Bits	READ/WRITE	FUNCTION
7	R	PCK - System parity check
6	R	IOCHCK - IO channel check
5	R	OUT2 - Timer 2 out
4	R	REFDET - Refresh detect
3	R/W	ENAIOCK - Enable I/O channel check
2	R/W	ENBRAMPCK - Enable RAM parity check
1	R/W	SPKRDATA - Speaker data
0	R/W	TIM2GATESPK - Timer 2 gate (speaker)

Table 1.1

At power-on time, the NMI is disabled. However, it can be enabled or disabled by writing to IO port 70H with data bit 7 equal to zero or one respectively. An NMI occurs when NMI is enabled, ENAIOCK/ENBRAMPCK is enabled and an IOCHCK or PCK occurs.

2.7 Configuration Registers

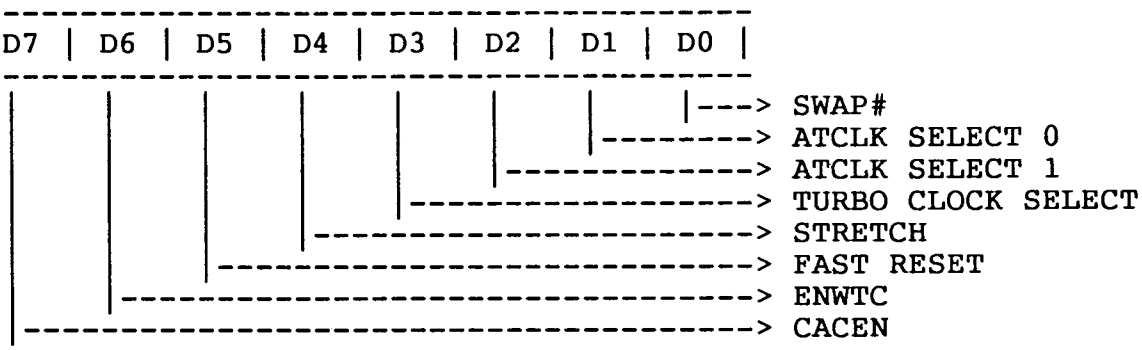
There are two bytes of configuration registers in the 82C381_B: REG00 and REG01. An indexing scheme is used to reduced the I/O ports required to access all the registers required for 82C381_B & 82C382_B and also avoids possible mistakes by incorrect programming. Writing to or reading from these registers involves two steps:

1. OUT to port 22H with the index addressing value that a particular register is to be written to or read from.

2. OUT or IN from port 24H for the write to or read from operation.

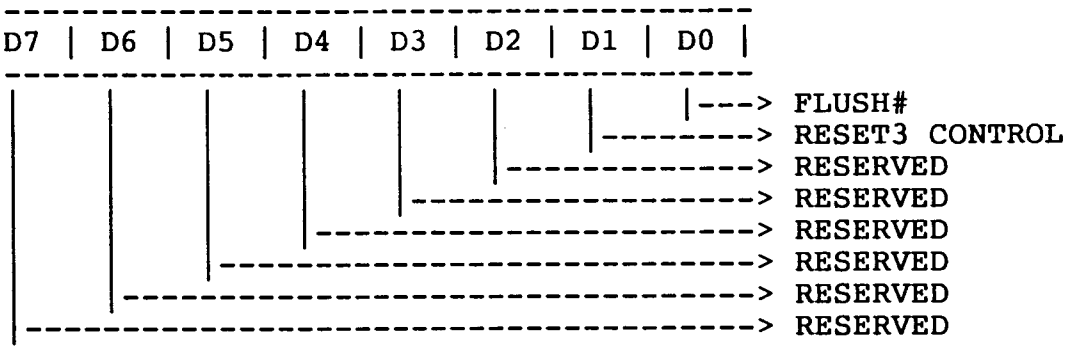
2.7.1 Register Description

REG00



Bits	Function
7 6	Cache Controller Enable and Multiplex pins Control. Default is 00. 00 Cache Controller disabled; PPCS#=1,SPCS#=1,NPCS#=1 NPCLK active (Default) 01 Cache Controller disabled; PPCS#,SPCS#,NPCS# active if selected, NPCLK active 10 External cache controller installed; PPCS#, SPCS# NPCS# active if selected, NPCLK active 11 On-chip cache controller installed; PPCS#=CAOE# SPCS#=CAWE#,NPCS#=TAGW#,NPCLK=CSL#
5	Alternate hot CPU reset. A low to high transition in this bit activates a CPU reset. Once active, it remains active until cleared by another write. Default is 0.
4	ATCLK stretch enable.Default is 0.
3	TURBO Clock Select. A zero selects CLKIN as the CPU clock, and a one enables the HIGH pin to select the CPU clock. If HIGH pin has been enabled, then a low on this pin selects CLKIN as CPU clock (high speed mode), and a high on this pin selects ICLK as the CPU clock(low speed mode). Default is 0.
2, 1	ICLK clock select. Default is 00. 00 ICLK = CLKIN/4. 01 ICLK = CLKIN/3. 10 ICLK = CLKIN/2. 11 Reserved
0	Master byte swap enable.Default is 0.

REG01



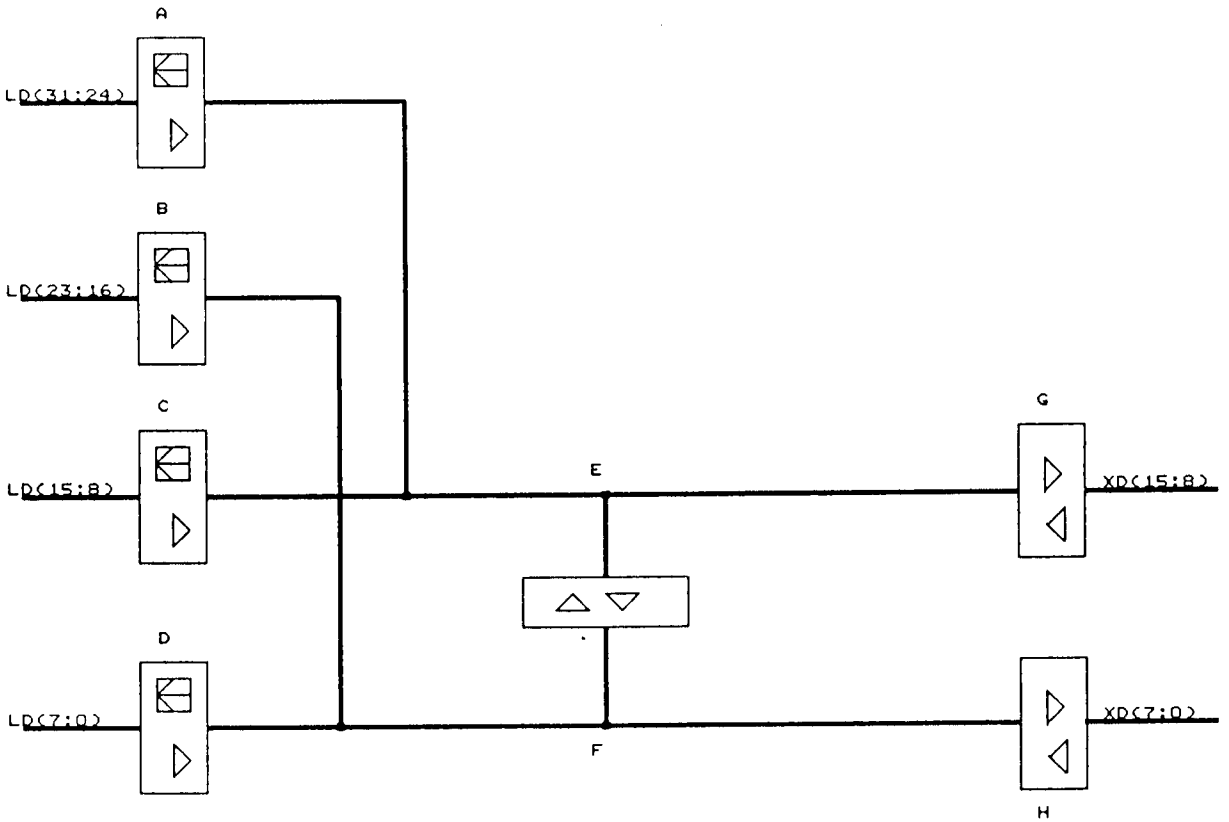
Bits	Function
0	Cache controller Flush#. A one activates FLUSH# pin output to the Cache Controller, and zero deactivates FLUSH#. Default is 1.
1	RESET3 Control. A one generates RESET3 on receiving a RESET2 only after a HALT instruction is detected by the 82C381_B. A zero generates a RESET3 immediately after receiving a RESET2. Default is zero.

2.8 Data Bus Conversion and Data Path Control Logic

The 82C381 performs data conversion when CPU's 32/16 bit instruction accesses 16/8 bit devices on AT Bus, or when DMA/MASTER accesses local DRAM or devices on AT Bus. It also provides all the control signals necessary to set the data flow path for external buffers.

The following table shows the data paths for various system cycles:

CPU Cycle	Data Path
Low word AT bus 16-bit access	C/D -- E/F -- G/H
High word AT bus 16-bit access	A/B -- E/F -- G/H
1st byte AT bus 8-bit access	D -- F -- H
2nd byte AT bus 8-bit access	C -- F -- H
3rd byte AT bus 8-bit access	B -- F -- H
4th byte AT bus 8-bit access	A -- F -- H
Local DRAM or 387 access	A,B,C,D tri-stated
8-bit DMA Cycle	**Data Path**
Local DRAM 1st byte access	D -- F -- H
Local DRAM 2nd byte access	C -- F -- H
Local DRAM 3rd byte access	B -- F -- H
Local DRAM 4th byte access	A -- F -- H
AT bus 8-bit memory access	H tri-stated
AT bus 16-bit memory 1st byte access	H tri-stated
AT bus 16-bit memory 2nd byte access	H - F - E - G
16-bit DMA Cycle	**Data Path**
Local DRAM low word access	C/D -- E/F -- G/H
Local DRAM high word access	A/B -- E/F -- G/H
AT bus 16-bit memory access	G,H tr-stated
Master Cycle	**Data Path**
Local DRAM low word access	C/D -- E/F -- G/H
Local DRAM high word access	A/B -- E/F -- G/H
AT bus 16-bit access	G,H tri-stated
AT bus 1st byte 8-bit access	G,H tristated
AT bus 2nd byte 8-bit access	G - E - F - H (default) G,H tristated(optional)



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Size A	Document Number DATA BUFFER PATH FLOW	REV 1
Date: October 23, 1989	Sheet 1 of 1	

2.9 Data Latches

The 82C381 provides data latches for all AT read cycles, not only for bus conversion, but also for the AT cycle read command which may be terminated before CPU samples the data.

2.10 Parity Generation/Detection Logic

For local DRAM write cycle, the 82C381_B generates even parity for each of the four bytes of the CPU 32 bit data. These valid parity bits are stored in the local DRAMs. During a local memory read access, the 82C381 checks for parity validation for each byte read. If the parity is detected as being odd, and if bit2 of Port B is 0, bit7 of Port B is set and NMI will be issued, if it is not masked.

If the cache enable bits, bit 6 & 7 in the REG00, are enabled, the parity checking circuitry will check the parity validation on a four bytes basis for every local DRAM read cycle, since the memory controller reads four bytes at a time to update cache.

2.11 Cache Controller Logic

The 82C381_B supports direct map/write-through cache memory control logic. This cache implementation provides a very flexible and low cost alternative for a simple, high performance cache system.

There are three factors that the system designer must take into consideration when he implements a cache system with this chip set. They are:

TAG-RAM
Line size
Cache memory

1) TAG-RAM

The TAG-RAM is implemented outside of the chip which increases the flexibility in the system design. Standard fast SRAM coupled with a comparator generates the tag HIT or MISS status. Depending on the total cache memory required and the line size selected, the designer can select the TAG-RAM from 4Kx4, 8Kx8 or 16Kx4 SRAMs. For example, in a 64k cache memory design, to cache upto 8M bytes local memory, you select 16-bytes as line size and two 4kx4 SRAMs for TAG; or in a 64k cache memory design, to cache upto 16M bytes local memory, you select 16-bytes as line size and two 16kx4 SRAMs to serve as TAG; or in a 128k cache memory design which caches upto 16M bytes local memory, you use line size is 16-bytes, and one 8kx8 or two 16kx4 SRAM for TAG. The selection is very flexible.

Another factor in selecting the TAG-RAM is the SRAM speed. 15-ns TAG RAM is required for the 33MHZ 386 cache system; while a 25-ns TAG RAM is reuired for the 25MHZ 386 cache system. Compared with the cost of current cache controllers, the cost of the TAG RAM used with the 381 is very low.

2) Line size

A programmable register inside the 382 allows the user to select the cache memory line size between 8-bytes and 16-bytes. Normally, a larger line size increase the hit rate, but also requires more time to update the cache memory during read miss cycles. The burst read implementation for the miss cycle reduces the overhead, thereby increasing the system performance.

3) Cache memory

The chip set allows the system designer to utilize any size cache SRAMS. The development kit schematics show 8Kx8s, however, most other SRAMs should be usable.

In addition, the SRAM access times are quite relaxed. To implement a 25-MHZ 386 cache system, 35ns cache memory is required; and, 25 ns cahe memory is reuired for the 33-MHZ 386 cache system.

2.11.1 TAG RAM invalidation

The Index register 01 bit 0 controls the TAG RAM's invalidation. After power-up, the bit is set logic high which forces the FLUSH# pin low. The cache control logic monitors this signal internally and generates TAGWE# during local DRAM read cycles which will force the TAG RAM invalid while the POST performs memory read/write checking automatically.

A driver is required to enable the cache function. This should first disable FLUSH#, next enable the cache control function inside the 381 and 382, then select the line size and finally, disable the NCA# signal.

In normal applications, to invalidate the TAG RAM, a driver is required to enable FLUSH# and then perform a number of read operations of local DRAM, equal to the TAG RAM size; e.g. 16K times if 16Kx4 SRAMs are used as TAG RAM.

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82C381_B Pin Description

Type	Pin NO.	Symbol	Description
Clocks			
I	139	CLKIN	Oscillator clock input from a TTL crystal oscillator having a frequency equal to twice the rated CPU clock
B	43	PCLK2	PROCESSOR CLOCK output from the 82C381_B.
I	77	OSCX1	Input from 14.3 MHz Crystal
O	78	OSCX2	Output to 14.3 MHz Crystal
O	125	OSC	14.3 MHz Oscillator output must be buffered by a 244 driver to provide 24 ma drive.
O	126	OSC/12	1/12 of 14.3 MHZ oscillator frequency.
O	82	ATCLK	AT System Clock output drives the SYSCLK line on the AT bus I/O Channel.
I	61	CCLK2	This Input Pin is the buffered PCLK2. It is derived from the same buffer as the CPU CLK2.
Control Signals			
I	46	ADS*	Status input from CPU. This active low signal indicates the CPU is starting a cycle.
I	51	D/C*	Data/Code status from CPU. Indicates data transfer operations when high, or control operations (code fetch, halt, etc.) when low
I	52	W/R*	Write/Read status from CPU. It indicates a write cycle if high and read cycle if low.
I	53	MIO*	Memory/IO status from CPU. If high it indicates a memory cycle. If low, it indicates an I/O cycle.
B	50-47	BE<3:0>	Byte Enable from CPU; during non-cpu cycles, they reflect the XA0, XA1

status.

B 45	READY*	Ready as an output is driven low to terminate the current CPU cycle. During all other cycles, it is an input from the 82C382_B or 387. It is an open collector output requiring an external pull-up resistor. It is connected to 80386 READY* pin indirectly and with the 387's RDYO*.
I 124	RST1*	Reset1 is an active low input generated by the power good signal of the power supply. When low, it activates Reset3 and Reset4. RST1* is latched internally
I 76	RST2*	Active low input generated from the 8042 Keyboard Controller for a "warm reset" not requiring the system power to be shut down. It forces a CPU reset by activating RESET3.
O 64	RESET3	Power on Reset or active high output to the 80386 when RESET2 is active. It is also activated when a shutdown condition in the CPU is detected.
O 149	RESET4	System reset output used to reset the AT Bus, 82C206, 8042 Keyboard Controller, 82C382_B Memory Controller. It is synchronized with the CPU clock.
I 63	HLDA	HOLD ACKNOWLEDGE from CPU in response to a hold request. It indicates to the requesting master that the CPU has relinquished the bus. When active, it forces commands (IOR*, IOW*, MEMR*, MEMW*) to be tristated.
O 83	HOLD	CPU HOLD request is an active high output to the CPU. It is activated during DMA, Master and refresh cycles.
O 84	HLDA1	Hold Acknowledge 1 is an active high output when the bus is granted in response to Hold Request.
I 88	HRQ	Hold Request is an active high input when DMA/Master requests a bus cycle.
I 86	AEN8*	Address Enable 8 bit DMA transfer is active low input from one of the two 8237s to enable the address latches.

I 85	AEN16*	Address Enable 16 bit DMA transfer is active low input from one of the two DMA controllers to enable the address latches.
O 143	NMI	Non Maskable Interrupt is an active high output to the NMI pin of the CPU.
T 135	ALE	Address latch enable for AT Bus. It controls the address latches driving the AT bus. It is tri-stated during master cycles.
O 150	EALE*	Early address latch enable is an active low output used to latch the CPU A23-A2 lines to the XA23-XA2 AT bus lines.
O 71	INTA*	Interrupt Acknowledge is an active low output to the 82C206 interrupt controller.
B 102	XBHE*	Byte High Enable is an active low signal which indicates transfer of data on the upper byte of the data bus. It is an output when the CPU is in control of the bus, and is an input when the DMA controller is in control of the bus.
I 152	AF32*	AF32 is an active low signal that indicates that a bus cycle is a local bus access.
I 55	RDYI*	CPU ready input.

System Buses

B 119-112	XD0-XD7	X Data Bus bits <0:7>
B 110-103	XD8-XD15	X Data Bus bits <8:15>
B 98-89	XA0-XA9	X Address Bus bits <0:9>; they are output pins for refresh cycles.
I 2-9	D0-D7	CPU Data Bus bits <0:7>
I 11-18	D8-D15	CPU Data Bus bits <8:15>
I 22-29	D16-D23	CPU Data Bus bits <16:23>
I 31-38	D24-D31	CPU Data Bus bits <24:31>

I 57	A31	CPU Address Data bus bit <31>
B 155-158	MP0-MP3	Memory Parity Bits for the 4 bytes of System Memory. These are inputs during memory read operations and output during memory write operations

Numeric Processor Interface

O 60	NPINT	Numeric Coprocessor Interrupt is an active high output. It is an interrupt request from the numeric processor and is connected to IRQ13 of the 82C206.
O 62	NPEST	387 installed signal.
I 65	NPBUSY*	Numeric Coprocessor Busy is an active low input indicating that a 387 command currently being executed. It is used to generate the BUSY signal to the CPU.
O 70	BUSY*	Active low BUSY to the CPU, initiated by the Numeric Coprocessor indicating that it is busy.
I 66	NPERR*	Numeric Coprocessor Error is an active low input indicating that an unmasked error condition exists.
O 123	NPRST	Numeric Coprocessor reset is an active high reset. It is active when RESET4 is active or when a write operation is made to Port 0F1H. In the later case, it is active for the half period of the command.
O 58	ERR*	386 error signal. It reflects the NPERR* signal during the period from RESET4* active to first ADS*. After the first ADS*, it stays high.

Cache Interface

O 44	FLUSH*	Tag Ram Invalidation control signal. It is programmable through INDEX Register 01 bit 0.
I 54	CALTH	CPU Status signals latch enable. It is from the 385 and is used to synchronize status signals with the 385

		signals. For Direct Map Cache implementations, this signal should be tied low.
T 56	CRDY0*	Ready output in Direct Map Cache systems. It is an open drain output and becomes active at the end of the last T-state of a read hit cycle.
O 136	TAGWE*	Tag Ram Write Enable. It is used to update the tag ram's validation. Note, that when FLUSH* is active, a local DRAM read will force this signal active
O 137	CAWE*	Cache Memory Write Enable. A write hit and cachable cycle, this signal will be activated which updates the contents inside the cache memory.
O 141	CSL*	Cache Memory Chip Selects control. A read miss and cachable cycle will activate this signal which forces all the chip selects of cache memory to low.
O 142	CAOE*	Cache Memory Output enable. A memory read hit and cachable cycle activates this signal.
I 147	NCA*	Non Cachable signal from the 82C382_B. This signal is used to indicate that the cache function is not enabled.
I 148	HIT*	Hit or miss signal from Tag Ram. This is used to determine whether the current memory cycle is from cache memory or not.
I 39	AMUX*	Indicates whether the 385 is installed (active low) or not.

AT Bus Signals

I 146	CHRDY	I/O Channel Ready is an active high input from the AT Bus. When low it indicates a not ready condition and inserts wait states in AT-I/O or AT-memory cycles. When high, it allows termination of the current AT-bus cycle
I 145	M16*	Memory Chip Select 16 is an active low input from the AT Bus indicating a 16-bit transfer. If high, it implies an 8-bit transfer.

I 144	IO16*	I/O Channel Select 16 is an active low input from the AT Bus indicating a 16-bit I/O transfer. If high it implies an 8-bit transfer.
I 74	NOWS*	No Wait States is an active low input from the AT bus, causing immediate termination of the current AT Bus cycle Memories capable of zero wait states, use this line to speed up memory cycles
I 73	CHCK	I/O Channel Check is an active low input from the AT bus causing an NMI to be generated if enabled. It is used to signal an I/O error condition from a device residing on the AT bus.
B 133	MEMRD*	AT Bus memory read.
B 134	MEMWR*	AT Bus memory write.
B 132	IOWR*	AT Bus I/O write.
B 131	IORD*	AT Bus I/O read.

Miscellaneous

I 59	TURBO	The TURBO Input Pin enables an external switch to control the speed of the CPU. A low select high speed operation and a high select low speed operation. Note, Bit 3 in Configuration Register 0 needs to enable the HIGH pin function. The default state of Bit 3 is to disable the HIGH pin function.
I 154	DRD*	Data Read is an active low output used to transfer data from the memory bus to the local CPU bus. If high it sets the data path from the local CPU bus to the memory bus.
I 153	DLE	Data Latch Enable is an active high output to enable the local memory data buffer.
I 138	HIGH	Tie to high for proper operation.
I 151	LMEN*	Local Memory Enable signal. It is used to control the local data buffers.
O 129	SPKDATA	Speaker Data is an active high output

		used to gate the 8254 compatible tone signal of the 82C206 to the speaker.
O 130	KBDCS*	8042 Keyboard Controller chip select is an active low.
O 128	ASRTC	Address Strobe to Real Time Clock is an active high signal used on the 82C206.
O 127	GATE2	Timer Gate 2 is an active high output that enables the 8254 counter timer in the 82C206 to enable the tone signal for the speaker.
I 87	OUT1	Refresh Request generated by the 82C206. It is activated normally every 15.6us to refresh the DRAMs.
T 75	RFSH*	System refresh control.It is an active low open collector output from 82C381_B.
I 72	OUT2	Active high output from 8254 timer. It can be read from Port B.
O 69	SDIR2*	System Data Bus direction for the high byte. A low sets the data path from the SD bus to the XD bus. A high sets the data path from the XD bus to the SD bus.
O 68	SDIR1*	System Data Bus direction for the low byte. A low sets the data path from the SD bus to the XD bus. A high sets the data path from the XD bus to the SD bus.
O 67	SDEN	System Data Bus (AT bus) buffer enable control. It is active high.

Power and Ground

I	120,100 81,40,20 1	Vcc	+5V
I	10,19, 21,30, 41,42, 79,80, 99,101, 111,121 122,159 160,140	Vss	Ground

OPTi

82C382_B 386/AT High Integration Direct Mapped/Page Interleave Controller

v1.1, December 12, 1989

1.0 The HiD/386 Chipset consists of the 82C381_B and 82C382_B. Together, they are designed to implement high performance, highly integrated, 386/AT Personal Computers running at 25 MHz and 33 MHz. The 82C381_B provides CPU control and Bus Conversion funtions, while the 82C382_B provides Direct Mapped Cache Control of any size (note, 64KB design on Development Kit board available) and 1-16MB of Page Interleave Memory Control.

2.0 Overview

The 82C382_B performs the memory control functions in 386 based AT-compatible systems. The 82C382_B is designed and optimized for the 25/33 MHZ 386 bus architecture. It supports two types of Memory Subsystem implementations - with and without cache. In either case, the DRAM Memory Controller is a page mode, interleaved memory design, which allows 0 wait state performance on most memory accesses. The benefit for cost-sensitive 386/AT designs is that there is minimum performance penalty for not using Cache; while in a Cache based system, performance is enhanced due to fewer wait states during cache miss cycles.

The 82C382_B supports a large range of DRAM memory configurations in order to provide flexibility to the OEM in spec'ing his products. It provides shadow RAM support for BIOS ROMs in order to increase system performance; and finally, it includes system cost saving features such as putting DRAM on the local bus, consequently reducing DRAM speed requirements, a single EPROM for BIOS, and address remapping of the unused 256K between 640K to 1M to the top of the system memory.

2.0.1 Page/Interleaved Operation

During DRAM read or write cycles, a row address and a column address is required. In most DRAMs, the row address access time is longer the column address access time. Therefore bus performance can be improved by using page-mode DRAM operation. Memory locations sharing the same row address are in the same memory page, therefore only a new column address is required. In page-mode operation, the row address strobe, RAS*, can be kept active, and only a new CAS* needs to be generated, thus reducing memory cycle time. In a four bank configuration, a maximum of four pages of memory can be kept active at a time, since each bank has an independent RAS*.

The effectiveness of page-mode operation depends heavily on the page-size. A larger page size increases the chance of page hit. Therefore, if the pages for the four banks are concatenated, the effective hit space is quadrupled. Consequently, system performance is further improved. The 82C382_B interleaves the pages of each bank in order to increase the effective hit space.

The 82C382_B supports both two and four way page/interleaved mode. If four way interleaved mode is used, the DRAMs used in each of the four banks must be identical.

FUNCTIONAL DESCRIPTION

2.1 Introduction

The 82C382_B is a highly integrated VLSI chip for the INTEL 386 32-bit microprocessor. It interfaces to the 82C381_B and provides the most cost-effective and highest performance system design for AT-compatible 386 based systems.

The 82C382_B consists of five functional blocks:

1) Memory Interface Logic
2) Cache Interface Logic
3) System Interface Logic
4) Configuration Registers
5) Address Latches

Each functional block is described in the following sections.

2.2 Memory Interface Logic

The local DRAM system can be configured from one upto four banks of 256K X 36-Bits OR 1M X 36-Bits each. Each bank of memory is further divided into four 8-bit banks with one additional bit for parity.

2.2.1 DRAM Bank Configuration

The 82C382_B provides tremendous flexibility in configurations for on-board memory. Table 2.1 lists the possible memory configuration.

	DRAM TYPE				
CFG	Bank0	Bank1	Bank2	Bank3	Total Memory
1	0	0	0	0	0
2	256K	0	0	0	1M
3	256K	256K	0	0	2M
4	256K	256K	256K	0	3M
5	256K	256K	256K	256K	4M
6	1M	0	0	0	4M
7	256K	1M	0	0	5M
8	1M	256K	0	0	5M
9	256K	256K	1M	0	6M
10	256K	1M	256K	0	6M
11	1M	256K	256K	0	6M
12	256K	256K	1M	256K	7M
13	256K	1M	256K	256K	7M
14	1M	256K	256K	256K	7M
15	1M	1M	0	0	8M
16	256K	1M	1M	0	9M
17	1M	1M	256K	0	9M
18	1M	256K	1M	0	9M
19	256K	256K	1M	1M	10M
20	256K	1M	1M	256K	10M
21	1M	1M	256K	256K	10M
22	1M	256K	1M	256K	10M
23	1M	1M	1M	0	12M
24	256K	1M	1M	1M	13M
25	1M	1M	1M	256K	13M
26	1M	256K	1M	1M	13M
27	1M	1M	1M	1M	16M

Page/interleaving is possible only for those combinations with similar pairs or quartet of DRAMs. otherwise, page mode is used. For example, in Cfg4, bank0 and bank1 are 2-way page-interleaved and bank2 is page mode only; while in Cfg 5 bank0-3 are 4-way page-interleaved.

2.2.2 DRAM and EPROM Control Logic

DRAM and EPROM control logic in the 82C382_B is responsible for the generation of RAS*, CAS*, MWE*, the memory address for DRAM accesses and the generation of ROMCS* for EPROM accesses. The DRAM read cycle can be completed in 0 to 3 wait states and the write cycle in 0 or 1 wait states as programmed by software in the configuration register. The EPROM can be accessed in either an 8-bit or 16-bit cycle.

2.2.3 Shadow RAM and Memory Remapping

Since access to local RAM is much faster than EPROM, the 82C382_B provides shadow RAM capability. With this feature data from slow devices like ROM and EPROM memories are copied into RAM to speed up memory accesses. The 82C382_B has built in support for shadowing different areas of memory - system BIOS , video BIOS, and adapter BIOS.

The shadow RAM feature is setup by bits in configuration registers. First, the ROM contents must be copied to the shadow RAM area. Next the shadow RAM enable bit is set in the configuration register. For system BIOS and video BIOS, once the bit is set, the RAM areas become read only. For the adapter BIOS area, the user can select the area to be read only or read/write by setting the write protect bit in the configuration register.

If the adapter BIOS area is not shadowed, the 82C382_B can remap 256KB of memory (A0000H - BFFFFH and D0000H to EFFFFH) to the top of system memory.

2.2.3.1 Algorithm for turning on Shadow RAM with Rev B.

The Procedure to copy the ROM to Shadow RAM and enable the Shadow RAM is the following:

F0000H-FFFFFH

1. Read from System BIOS ROM and Write to the Local DRAM since the default state of Bit 7 CFG REG 11H enable this.

2. After finishing the copy to local DRAM, in order to write protect the Shadow RAM and enable the future accesses to the Shadow RAM (instead of ROM), reset Bit 7 CFG REG 11H to 0.

E0000H-EFFFFH

Case 1. This region is System Board BIOS

1. Enable System Board BIOS reads by resetting Bit 5 of CFG REG 11H to 0; enable write to Local DRAM by setting Bit 6 of CFG REG 15H to 1.

2. Read from the System Board BIOS and write to Local DRAM.

3. Set the appropriate bits <4:7> in CFG REG 12H in order to enable shadow RAM for the selected blocks.

4. Set Bit 5 in CFG REG 11H to enable shadow RAM. Write Protect the Shadow RAM by setting Bit 3 in CFG REG 11H to 1.

5. Reset Bit 6 in CFG REG 15H to write protect the local DRAM in the C0000H-EFFFFH region.

Case 2. This region is on the AT Channel.

1. Enable AT Channel reads by setting Bit 5 of CFG REG 11H to 1 (default state); enable write to Local DRAM by setting Bit 6 of CFG REG 15H to 1.

2. Read from the AT Channel and write to Local DRAM.

3. Set the appropriate bits <4:7> in CFG REG 12H in order to enable shadow RAM for the selected blocks. Write Protect the Shadow RAM by setting Bit 3 in CFG REG 11H to 1.

4. Reset Bit 6 in CFG REG 15H to write protect the local DRAM in the C0000H-EFFFFH region.

C0000H-DFFFFH

1. Enable write to Local DRAM by setting Bit 6 of CFG REG 15H to 1.

2. Read from the AT channel and write to the local DRAM.

3. Set the appropriate bits <0:3> in CFG REG 12H for D0000H-DFFFFH and <0:3> in CFG REG 15H for C0000H-CFFFFH in order to enable shadow RAM for the selected blocks. Write Protect the Shadow RAM by setting Bit 4 in CFG REG 11H to 1 for D0000H-DFFFFH and by setting Bit 5 in CFG REG 15H to 1 for C0000H-CFFFFH.

4. Reset Bit 6 in CFG REG 15H to write protect the local DRAM in the C0000H-EFFFFH region.

2.3 Cache Interface Logic

In order to achieve the highest possible performance, the 82C382_B supports a Cache interface. This cache is a direct mapped write-through architecture and can be of any size. The user can set two blocks of non-cacheable areas through software programmable registers.

2.4 System Interface Logic

The 82C382_B generates DDIR*, DLTACH, LOCAL*, ENXD* for system control. DDIR* controls the direction of data flow in and out of the data buffer inside of the 82C381_B. DLTACH latches the DRAM data for parity check purpose. LOCAL* is issued for local memory accesses. XDEN* is activated for I/O accesses to the internal registers of 82C382_B.

2.4.1 Memory Subsystem Design Specifications

The following tables describe the access timings for the Memory subsystem. Note, PWS stands for the Programmed Wait States in the Configuration Register.

a. Page Interleave Mode, Cache not installed, CPU running in Pipeline Mode

Cycle	Page Active	Page Inactive	Page Miss
Read	0+PWS	1+PWS	3+PWS
Write	0+PWS	0+PWS	2+PWS

b. Page Interleave Mode, Cache not installed, CPU running in non-Pipeline Mode

Cycle	Page Active	Page Inactive	Page Miss
Read	1+PWS	2+PWS	4+PWS
Write	1+PWS	1+PWS	3+PWS

c. Direct Mapped Cache installed, CPU always running in non-Pipeline mode

Cycle	Cache Hit	Cache Miss
Read	0	Same as DRAM
Write	Same as DRAM	Same as DRAM

d. SRAM Timing for Direct Mapped Cache

Clock (MHz)	TAG RAM Speed	Cache RAM	Comparator
20	35ns	45ns	15ns
25	25ns	35ns	11ns
33	15ns	25ns	5.5ns

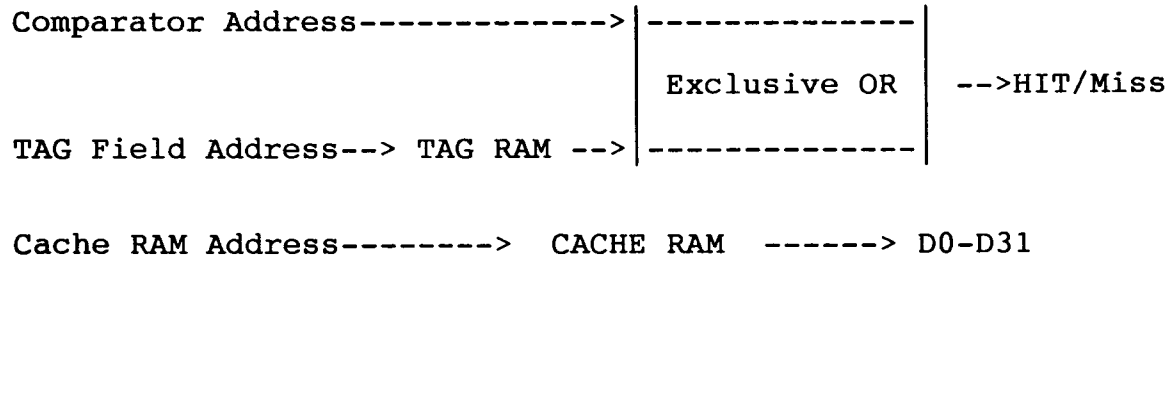
e. DRAM Timing

Clock (MHz)	1 Wait State	0 Wait State
20	120ns	100ns(CAS* access time<=48ns)
25	100ns	80ns(CAS* access time<=30ns)
33	80ns	60ns(CAS* access time<=21ns)

2.4.2. Direct Mapped Cache Design Options

Cache Size	Line Size Bytes	TAG Field Address	Cache RAM Address	Comparator Address
32K	8	A3-A14	A2-A14	A15-A23 + Valid Bit
	16	A4-A14	A2-A14	A15-A23 + Valid Bit
64K	8	A3-A15	A2-A15	A16-A23 + Valid Bit
	16	A4-A15	A2-A15	A16-A23 + Valid Bit
128K	8	A3-A16	A2-A16	A17-A23 + Valid Bit
	16	A4-A16	A2-A16	A17-A23 + Valid Bit
256K	8	A3-A17	A2-A17	A18-A23 + Valid Bit
	16	A4-A17	A2-A17	A18-A23 + Valid Bit
512K	8	A3-A18	A2-A18	A19-A23 + Valid Bit
	16	A4-A18	A2-A18	A19-A23 + Valid Bit

Note: If you only want to have 0-8MB Cacheable, then the Comparator Address most significant bit A23 can be dropped to A22.



2.4.3 Memory Address Line Contents for different Memory Configurations

Depending on the Memory Configuration programmed in Configuration register 13H, the 82C382_B puts out different physical address bits out on the MA0-MA9 lines, as shown in the table below. This information may be used to put in dynamic memory configuration into the BIOS.

	Memory Address Lines - MA									
	9	8	7	6	5	4	3	2	1	0
256K DRAM, PAGE MODE										
RAS	-	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS	-	A10	A9	A8	A7	A6	A5	A4	A3	A2
1M DRAM, PAGE MODE										
RAS	A21	A19	A18	A17	A16	A15	A14	A13	A12	A20
CAS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2
256K DRAM, 2-WAY PAGE INTERLEAVE MODE										
RAS	-	A19	A18	A17	A16	A15	A14	A13	A12	A20
CAS	-	A10	A9	A8	A7	A6	A5	A4	A3	A2
1M DRAM, 2-WAY PAGE INTERLEAVE MODE										
RAS	A22	A19	A18	A17	A16	A15	A14	A13	A12	A20
CAS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2
256K DRAM, 4-WAY PAGE INTERLEAVE MODE										
RAS	-	A19	A18	A17	A16	A15	A14	A13	A21	A20
CAS	-	A10	A9	A8	A7	A6	A5	A4	A3	A2
1M DRAM, 4-WAY PAGE INTERLEAVE MODE										
RAS	A22	A19	A18	A17	A16	A15	A14	A23	A21	A20
CAS	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2

2.4.4 Configuring Memory Configuration using DIP Switches

With Rev B, the OEM can set the value of Configuration Reg 13H and the Read and Write Wait states under hardware control. The values are read into the 82C382_B-B during RESET4# on MA0-MA7. The 386DM Rev 2 schematic shows the logic required.

This feature is necessary only in the following two cases:

-if the OEM does not want to use Dynamic Memory Configuration, which is normally available in most OPTi

configured BIOS like AMI, AWARD or Phoenix's. It is generally recommended to use Dynamic Memory Configuration rather than the Hardware configuration approach because of End-User conveniences.

-if the OEM does not want to use the 82C206 with its built in additional 64 bytes of CMOS RAM for storing configuration data; then the OEM can use a DALLAS Semiconductor style RTC, with some other peripheral chip, since now there is no requirement to store configuration data in battery backed up CMOS RAM.

OEMs who use Generic BIOSes, can use the hardware configuration approach with a software driver, which can be put in the Autoexec.bat file in order to configure the chipset into the proper state.

The Bit and Pin assignments are:

MA0 = Pin #5 = CFG REG 13H Bit 0
MA1 = Pin #6 = CFG REG 13H Bit 1
MA2 = Pin #7 = CFG REG 13H Bit 2
MA3 = Pin #8 = CFG REG 14H Bit 5
MA4 = Pin #9 = CFG REG 13H Bit 4
MA5 = Pin #10 = CFG REG 13H Bit 5
MA6 = Pin #11 = CFG REG 13H Bit 6
MA7 = Pin #12 = CFG REG 14H Bit 6

In systems that do not use a Configuration Switch, the MA0-MA7 lines should be pulled up during RESET4#. This can be done with pull-up resistors on the MA0-MA7 lines.

2.5 Configuration Registers

There are thirteen configuration registers in the 82C382_B - REG0-REG12. The registers are accessed through IO ports 22H and 24H. Location 22H is the "Index Address". This address corresponds to the specific register which points to the required data value accessed through port 24H. Thus, reading or writing to a specific register is a two step operation :

1) write to I/O port 22H with the register index.

2) write or read the data to or from I/O port 24H.

Every access to port 24H must be preceded by a write of the index value to port 22H even if the same data register is being accessed. After power up, the configuration registers assume default values. *All bits marked as Reserved must be programmed zero.* Table 2.0 lists these registers and the purpose of each bit is described below.

Reg #	Reg Name	Index
0	Remapping Address	10H
1	Shadow Ram	11H
2	Memory Enable	12H
3	Bank Configuration	13H
4	DRAM Configuration	14H
5	Video Adapter Shadow	15H
6	Fast GateA20	16H
7	Cache Configuration	17H
8	Non-cacheable Block 1 size	18H
9	Non-cacheable Block 1	19H
10	Non-cacheable Block 2 size	1AH
11	Non-cacheable Block 2	1BH
12	Cacheable area	1CH

2.5.1 Register Description

Remapping Address Register
Index : 10H

Note, the remap address is always on a 1MB boundary.

BIT POSITION	FUNCTION	DEFAULT
0-3	Address range to be remapped(A20-A23)	0001H

A23	A22	A21	A20	Remap Address
0	0	0	0	no mapping
0	0	0	1	1MB
0	0	1	0	2MB
0	0	1	1	3MB
0	1	0	0	4MB
0	1	0	1	5MB
0	1	1	0	6MB
0	1	1	1	7MB
1	0	0	0	8MB
1	0	0	1	9MB
1	0	1	0	10MB
1	0	1	1	11MB
1	1	0	0	12MB
1	1	0	1	13MB
1	1	1	0	14MB
1	1	1	1	15MB

4	Remap enable bit 0 = disable, 1 = enable	0
5-7	Reserved	0

Shadow Ram Register
Index : 11H

BIT POSITION	FUNCTION	DEFAULT
0-1	Reserved	0
2	Disable RAS* timeout precharge counter. 0 = enable counter, 1 = disable counter.	0
3	Shadow RAM at E0000H-EFFFFH read/write status. 0 = read/write, 1 = read only. (while shadow RAM is being loaded, this must be set to 0; after it is loaded shadow RAM is write-protected by setting this bit to 1)	0
4	Shadow RAM at D0000H-DFFFFH read/write status. 0 = read/write, 1 = read only. (while shadow RAM is being loaded, this must be set to 0; after it is loaded shadow RAM is write-protected by setting this bit to 1)	0
5	Adaptor ROM located at E0000H-EFFFFH 0 = *All* accesses are to System Board ROM, shadow RAM is disabled 1 = Shadow RAM is selectively enables in 16KB blocks by CFG Reg 12h; other accesses are *AT channel cycles*.	1
6	ROM located at D0000H-DFFFFH 0 = *All* accesses are on the AT channel and shadow RAM is disabled. 1 = Shadow RAM is selectively enabled in 16KB blocks by CFG Reg 12h; other accesses are AT channel cycles	1
7	Shadow RAM enable for system BIOS ROM at F0000H-FFFFFH. 1 = Reads go to ROM and writes go to shadow RAM 0 = *Read Only* from Shadow RAM	1

Memory Enable Register
Index : 12H

This register selectively enables shadow RAM in 16KB blocks from D0000H to EFFFFH. These controls in conjunction with the Shadow RAM Register (CFG Reg 11H), are used to implement selective shadowing for the full range of systems implementations.

BIT POSITION	FUNCTION	DEFAULT
0	Shadow RAM enable in D0000H-D3FFFH area. 0 = Disable, 1 = Enable.	0
	1 Shadow RAM enable in D4000H-D7FFFH area.	0
2	Shadow RAM enable in D8000H-DBFFFH area.	0
3	Shadow RAM enable in DC000H-DFFFFH area.	0
4	Shadow RAM enable in E0000H-E3FFFH area.	0
5	Shadow RAM enable in E4000H-E7FFFH area.	0
6	Shadow RAM enable in E8000H-EBFFFH area.	0
7	Shadow RAM enable in EC000H-EFFFFH area.	0

Bank Configuration Register
Index : 13H

BIT POSITION	FUNCTION	DEFAULT
0-2	These bits contain the information for the DRAM types used for BANK2 and BANK3.	111
3	Reserved -	0
4-6	These bits contains the information for the DRAM types used for BANK0 and BANK1.	111
7	Reserved	0

2 1 0	BANK2	BANK3
0 0 0	256K	none
0 0 1	256K	256K
0 1 0	none	none
0 1 1	1M	256K
1 0 0	1M	none
1 0 1	1M	1M
1 1 X	none	none

6 5 4	BANK0	BANK1
0 0 0	256K	none
0 0 1	256K	256K
0 1 0	256K	1M
0 1 1	1M	256K
1 0 0	1M	none
1 0 1	1M	1M
1 1 0	none	none
1 1 1	256K	none

DRAM Configuration Register
Index : 14H

BIT POSITION	FUNCTION	DEFAULT
0-4	Reserved	0
5	DRAM write cycle wait state 0 = 0 wait state 1 = 1 wait state.	1
7,6	DRAM read cycle wait state	01

7 6	# of wait state
0 0	0
0 1	1
1 0	2
1 1	3

Adapter Region Shadow Register
Index : 15H

BIT POSITION	FUNCTION	DEFAULT
0	Shadow Ram Enable in C0000h-C3FFFH	0
1	Shadow Ram Enable in C4000h-C7FFFH	0
2	Shadow Ram Enable in C8000h-CBFFFH	0
3	Shadow Ram Enable in CC000h-CFFFFH	0
4	ROM located at C0000H-CFFFFH 0 = All accesses are to AT Channel, Shadow RAM disabled 1 = Shadow RAM is selectively enabled in 16KB Blocks by Bits<0:3>.	1
5	Shadow RAM at C0000H-CFFFFH R/W Control 0 = Read/Write. 1 = Read only	0
6	Shadow RAM Copy Enable Control for C0000H-EFFFFH 0 = Write to the AT Channel 1 = Write to the Local DRAM	0
7	Reserved	

Fast GateA20 Register
Index : 16H

BIT POSITION	FUNCTION	DEFAULT
0-2	Reserved	0
3	Fast GateA20 Control 0 = GA20 signal is controlled by GATEA20 signal from Keyboard Cntrlr 1 = CPUA20 is enabled onto GA20	0
4-7	Reserved	0

Cache Configuration Register
Index : 17H

BIT POSITION	FUNCTION	DEFAULT
0-2	Reserved	0
3,4	Line Size Selection	00
	4 3 Line Size 0 0 4 bytes 0 1 8 bytes 1 0 16 bytes 1 1 Reserved	
5	Write-thru Cache - This bit must be set to 1	1
6	1= Cache enabled 0= Cache disabled	0
7	Force NCA* output pin to be low if this bit is a one, otherwise this bit has no effect on NCA* output pin.	1

Non-Cacheable Block 1 Size Register
Index : 18H

BIT POSITION	FUNCTION	DEFAULT
0-4	Reserved	0
5-7	Size of non-cacheable memory block 1.	111

7 6 5	Block size
0 0 0	64K
0 0 1	128K
0 1 0	256K
0 1 1	512K
1 0 0	1M
1 0 1	4M
1 1 0	8M
1 1 1	Disable

Non-cacheable Block Address 1 Register
Index : 19H

This register is used in conjunction with Index 18H register to define a non-cacheable block. The starting address for the Non-Cacheable Block *must* have the same granularity as the Block size. For example, if a 1MB non-cacheable block is selected, its starting address is a multiple of 1MB; consequently, only address bits are A20-A23 are significant, A16-A19 are don't care..

BIT POSITION	FUNCTION	DEFAULT
0-7	Valid starting address bits A16-A23 of non-cacheable memory block 1.	

Block Size	Valid Starting Address Bits A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	X
256K	V	V	V	V	V	V	X	X
512K	V	V	V	V	V	X	X	X
1M	V	V	V	V	X	X	X	X
4M	V	V	X	X	X	X	X	X
8M	V	X	X	X	X	X	X	X

X = Don't Care
V = Valid Bit

Non-Cacheable Block 2 Size Register
Index : 1AH

BIT POSITION	FUNCTION	DEFAULT
0-4	Reserved	0
5-7	Size of non-cacheable memory block 2.	111

7 6 5	Block size
0 0 0	64K
0 0 1	128K
0 1 0	256K
0 1 1	512K
1 0 0	1M
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Disable

Non-cacheable Block Address 2 Register
Index : 1BH

This register is used in conjunction with Index 18H register to define a non-cacheable block. The starting address for the Non-Cacheable Block *must* have the same granularity as the Block size. For example, if a 1MB non-cacheable block is selected, its starting address is a multiple of 1MB; consequently, only address bits are A20-A23 are significant, A16-A19 are don't care.

BIT POSITION	FUNCTION	DEFAULT
0-7	Address bit A16-A23 of non-cacheable memory block 2.	

Block Size	Valid Starting Address Bits A23	A22	A21	A20	A19	A18	A17	A16
64K	V	V	V	V	V	V	V	V
128K	V	V	V	V	V	V	V	X
256K	V	V	V	V	V	V	X	X
512K	V	V	V	V	V	X	X	X
1M	V	V	V	V	X	X	X	X

X = Don't Care
V = Valid Bit

Cacheable Area Register
Index : 1CH

BIT POSITION	FUNCTION	DEFAULT
0-2	Reserved	0
3	256KB Remaped area cacheable. 1 = Cacheable, 0 = Non-cacheable 1	1
4-7	Cacheable address range for local memory.	0000

7 6 5 4	Address Range
0 0 0 1	1 MByte
0 0 1 0	2 MByte
0 0 1 1	3 MByte
0 1 0 0	4 MByte
0 1 0 1	5 MByte
0 1 1 0	6 MByte
0 1 1 1	7 MByte
1 0 0 0	8 MByte
1 0 0 1	9 MByte
1 0 1 0	10 MByte
1 0 1 1	11 MByte
1 1 0 0	12 MByte
1 1 0 1	13 MByte
1 1 1 0	14 MByte
1 1 1 1	15 MByte
0 0 0 0	16 MByte

2.5 Address Latches

The 82C382_B provides the buffering between the CPU address and the XA address. The CPU address lines are latched by ALE and EALE to generate the XA address lines during CPU cycles. The XA address lines become inputs for DMA, MASTER and REFRESH cycles. For DMA and MASTER write cycles, the XA address lines are connected to the 386 address lines for cache snooping purposes.

82C382_B PIN DESCRIPTION

Type	Pin NO.	Symbol	Description
		Clocks	
I	66	CLK2	PROCESSOR CLOCK input from the 82C381_B.
I	127	OSC/12	1/12 of 14.3 MHZ oscillator frequency.
		Control Signals	
I	62	ADS*	Status input from CPU. This active low signal indicates that the CPU is starting a cycle.
I	57	D/C*	Data/Code status from CPU. Indicates data transfer operations when high, or control operations (code fetch, halt, etc.) when low
I	56	W/R*	Write/Read status from CPU.It indicates a write cycle if high and read cycle if low.
I	55	MIO*	Memory/IO status from CPU. If high it indicates a memory cycle. If low, it indicates an I/O cycle.
B	54-37	A<31:14>	Address inputs from CPU.These are input signals during the CPU cycle and become outputs during DMA or MASTER cycle.
B	33-22	A<13:2>	Address from CPU. These are input signals during the CPU cycle and become outputs during DMA or MASTER cycle.
I	58-61	BE<3:0>	Byte Enable from CPU.
I	122	RESET4	System reset from 82C381_B.
I	65	HLDA	HOLD ACKNOWLEDGE from CPU in response to a hold request.
I	112	RFSH*	System refresh control.It is an active low input from 82C381_B. Note, during Reset4, this signal must be pulled high

OPTi

I 124	ALE	Address latch enable for AT Bus. It controls the address latches driving the AT bus.
I 123	EALE*	Early address latch enable is an active low input used to latch the LA17-LA23 address lines.
I 125	XMEMR*	AT Bus memory read.
I 126	XMEMW*	AT Bus memory write.
I 128	GATEA20	Gate address 20 control from keyboard controller. When high, GA20 = CPU A20. When low, GA20 = 0.
I 111	AMUX*	Indicates 82385 cache controller is installed when this signal is low.
I 75	BACP	Latch enable signal from 82C385
I 113	HIT*	Cache hit signal
I 74	LOCK*	LOCK signal from CPU

DRAM Interface

O 20,19 16,15	RAS<3:2> RAS<1:0>	Row address strobes are active low outputs used to drive the DRAM RAS* pins.
O 4-2 134-130 110-105 101,100	CAS<15:13> CAS<12:8> CAS<7:2> CAS<1:0>	Column address strobes are active low outputs used to drive the DRAM CAS* pins. These signals may be used to drive the RAM chips without buffering
O 129	MWE*	Memory write enable is an active low output for DRAM write enable.
O 14,13	MA<9:8>	Multiplexed DRAM address lines MA9,MA8.
B 12-5	MA<7:0>	Multiplexed DRAM address lines MA7 to MA0. These also provide an 8 bit bi-directional data path forI/O operations to the internal registers of the 82C382_B.
O 121	DLE	Data latch enable is an active high output used to enable the local memory data buffer latch for 82C381_B.
O 120	DRD*	Data read is an active low output used to enable the data to the local CPU

bus.

O 118	LMEN*	Local bus enable is an active low output which indicates system board memory cycle.
O 21	XDEN*	X data buffer enable is an active low output used to control the external MA-XD bus buffer.

Cache Interface

O 70	CWEN	Cache memory write enable is an active high output during the cache read miss prefetch cycles.
O 73	SSTB*	Snooping address strobe to cache controller; This signal is enabled during DMA or MASTER memory write cycles.
O 72,71	CACNT<3:2>	Cache address counter outputs which control the correct value to the cache address line 1-0 during the cache miss prefetch.
O 114	NCA*	Non-cachable memory status to cache controller which is used to tell cache controller that the current CPU cycle is non-cachable.

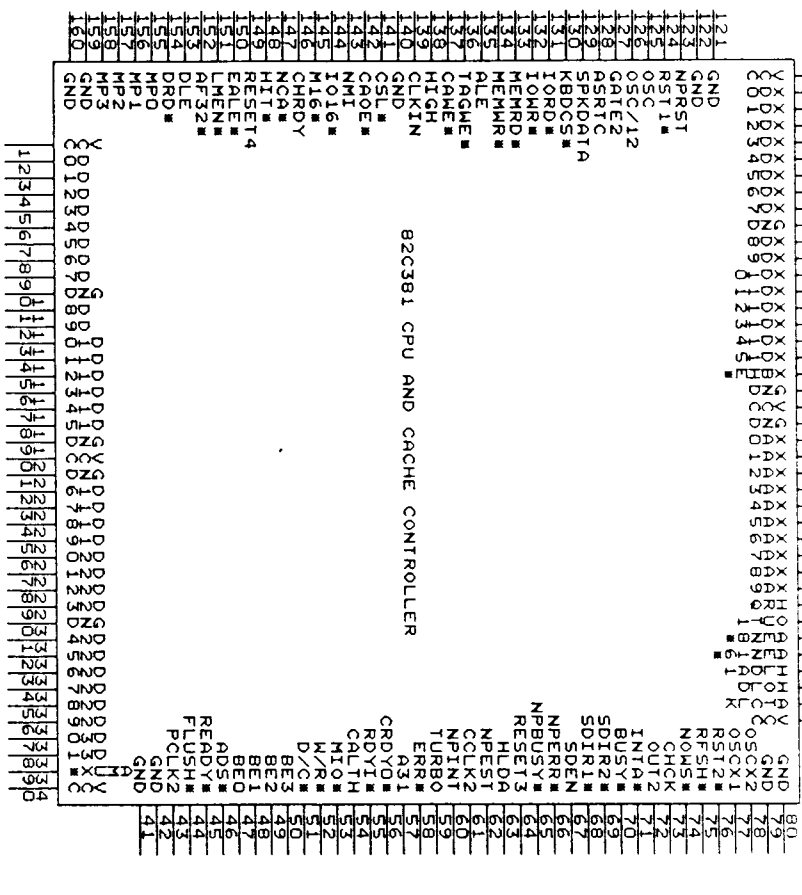
Miscellaneous

O 115	ROMCS*	Rom chip select is an active low output to the BIOS EPROM. It can be connected to the output enable pin of the EPROM.
O 116	LMGCS*	Lower 1 Meg chip select is an address decode when address A20 - A23 are low.
T 119	AF32*	AF32* is an active low output for local DRAM cycle.
O 117	GT20	A20 control signal which is controlled by GATEA20 or FAST GATEA20 control bit from internal register of 82C382_B.This signal is used to control the A20 into cache controller.
B 79	GA20	Address line 20 is the gated A20 bit which is controlled by GATEA20 or FAST GATEA20 control bit from 82C382_B

			internal register. It becomes an input during DMA and MASTER cycles.
T	64	READY*	READY is the system ready signal to the CPU.
I	63	RDYI*	RDYI is an input which indicates the current CPU cycle is completed.
B	76-78 80-82	XLA<23:21> XLA<19:17>	AT bus unlatched address 23-17; these are outputs for CPU cycles and become inputs during DMA, REFRESH or MASTER cycles.
B	83,84 87-99	XA<16:15> XA<14:2>	AT bus latched address line 16-2. these are outputs for CPU cycles and become inputs for DMA, REFRESH or MASTER cycles.

Power and Ground

I	1,34,69 102	Vcc	+5V
I	17,18 35,36,67 68,85,86 103,104, 135,136	Vss	Ground

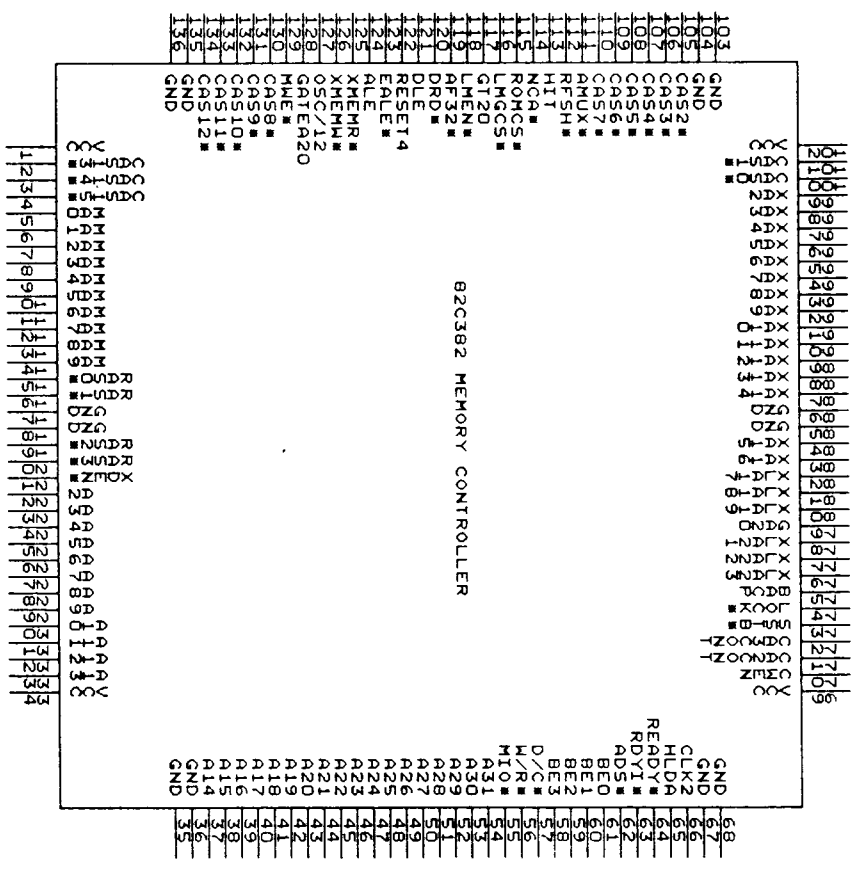


OPTi, Inc
2700 Augustine Drive, #165
Santa Clara, California 95054

Title: 82C381 PIN OUT

Size: A | Document Number | REV: B

Date: November 7, 1989 | Sheet | of



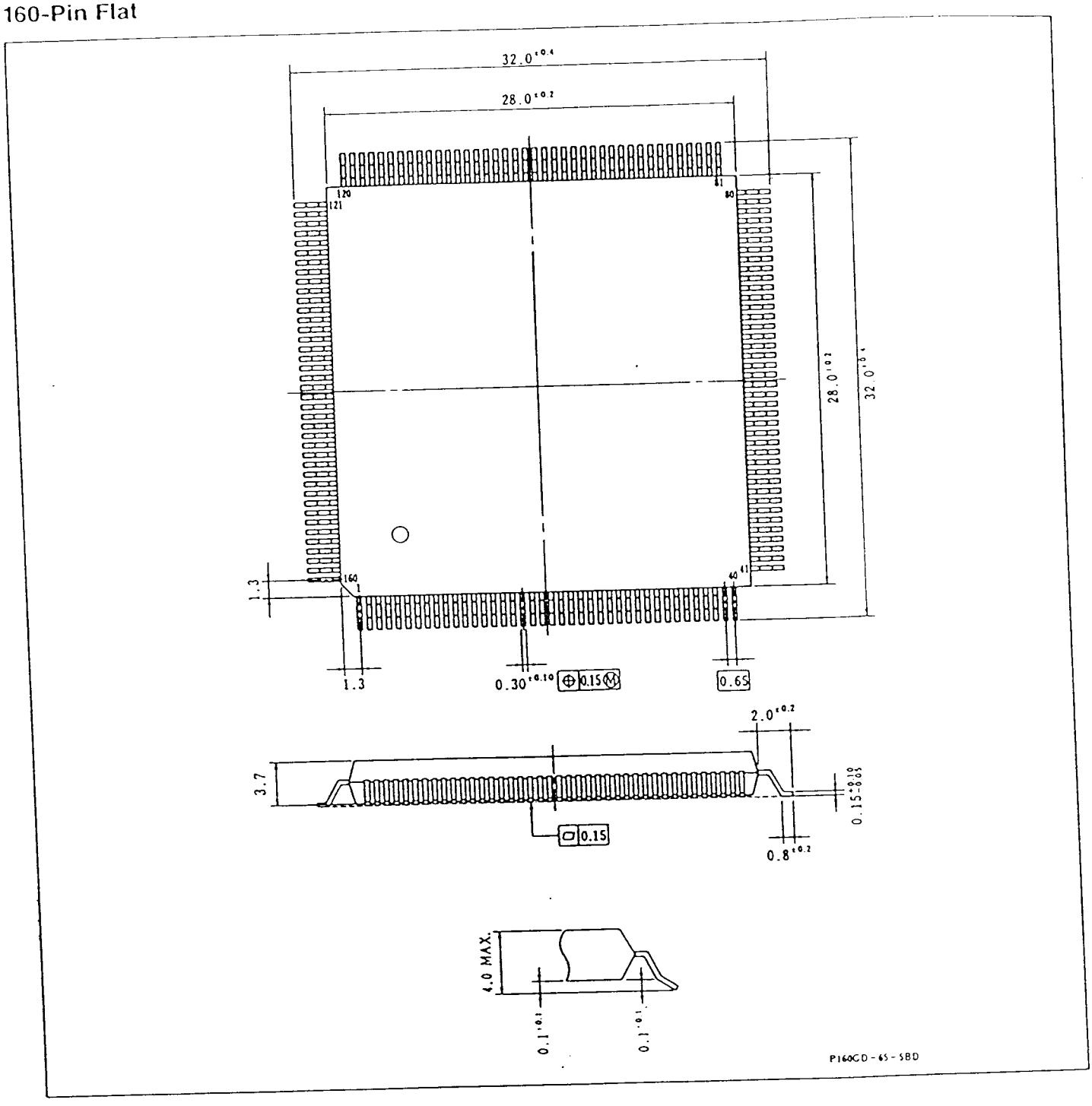
OPTi, Inc.
2700 Augustine Drive, #165
Santa Clara, California 95054

Title: 82C382 PIN OUT

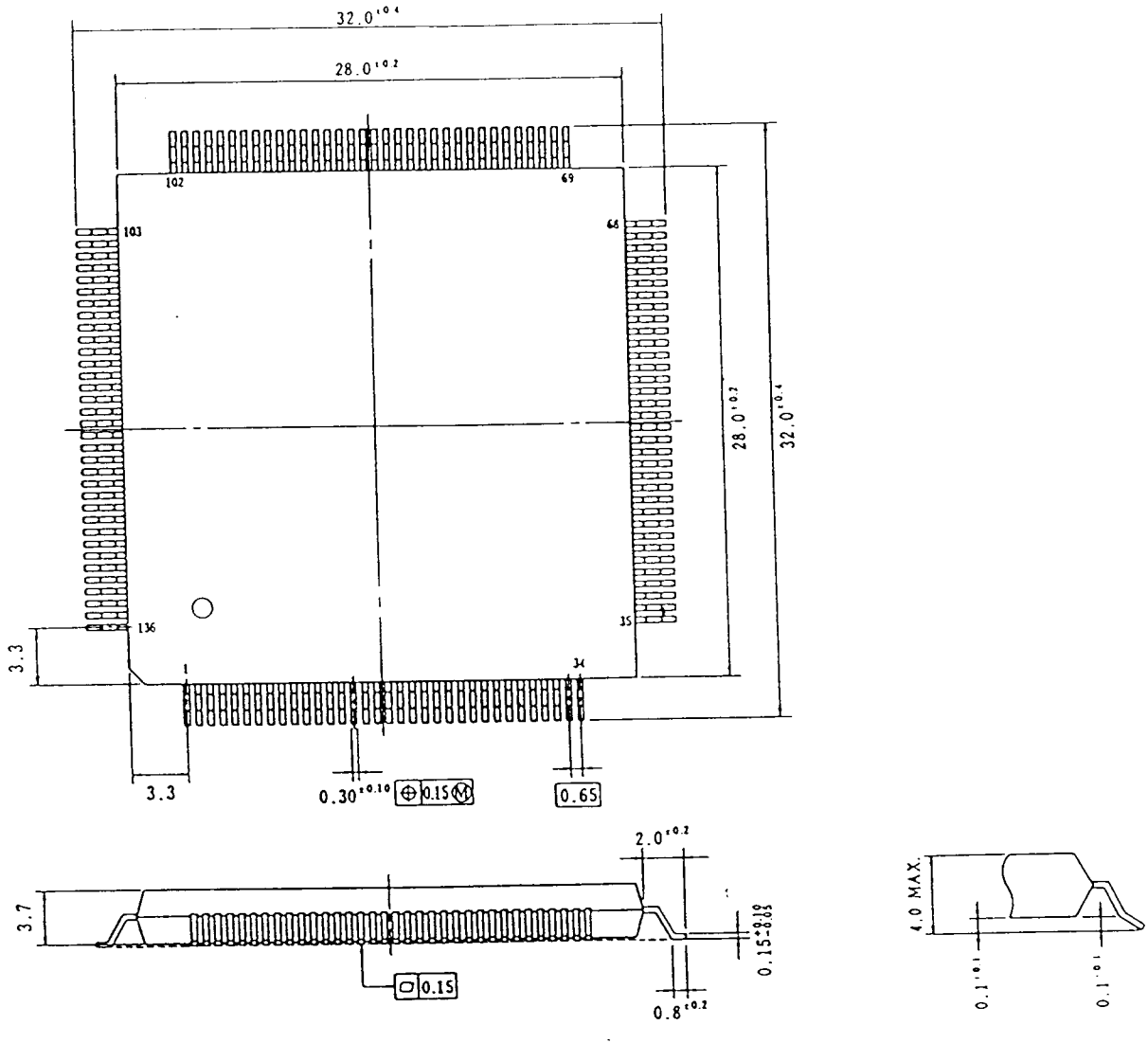
Size: A | Document Number | REV: B

Date: November 7, 1989 | Sheet | of

160-Pin Flat


32.0±0.4
28.0±0.2
120
121
81
80
160
1
40
41
28.0±0.2
32.0±0.4
1.3
1.3
0.30±0.10
0.15 M
0.65
2.0±0.2
3.7
0.15
0.8±0.2
0.15 +0.10 -0.05
4.0 MAX.
0.1±0.1
0.1±0.1
P160GD-65-SBD

136-Pin Flat


32.0±0.4
28.0±0.2
102
69
103
68
136
35
1
34
3.3
3.3
0.30±0.10
0.15 M
0.65
28.0±0.2
32.0±0.4
2.0±0.2
3.7
0.15 +0.10 -0.05
0.15
0.8±0.2
4.0 MAX.
0.1 +0.1 -0.1
0.1 +0.1 -0.1
P136GD-65-SBC

USER'S GUIDE
DK/HiD-386 HIGH INTEGRATION DIRECT MAPPED CACHE EVALUATION KIT

November 10, 1989
Rev 1.0

Table of Contents

A. Product Description

DK/HiD-386 is a complete development kit for high performance 25 and 33 MHz Cache 386/AT systems. The evaluation board has the following features:

1. 25 MHz system operation
2. Upgradeable to 33 MHz operation
3. 25 MHz 80386, socket for 387
4. 64KB of direct mapped Cache
5. 1 MB of memory on Memory Board, expandable to 16MB
6. 6 AT expansion slots
7. Diagnostic Hex Displays
8. Plug in modules for Custom Chips - 82C381/82C382
9. Diagnostic points for entire custom device pinouts
10. AMI 386/AT Evaluation BIOS ROM
11. 4-layer Baby AT form factor
12. Prototyping area
13. Diskette with the following files:
    1. 386A/385 & 386B/DM Schematics in ORCAD 3.1
    2. Device Libraries
    3. BIOS HEX files from AMI, AWARD, PHOENIX

B. Setup and Configuration

B.1 Basic Setup

To boot the DK/HiD-386, you need the following equipment:

1. AT compatible power supply
2. AT style keyboard
3. EGA card
4. EGA monitor
5. Floppy/Hard disk controller card
6. 5-1/4 high density floppy drive
7. Hard disk unit
8. Bootable DOS diskette
9. 1MB Memory Board

B.2 Default Configuration

The default values for the configuration registers are:

Config Reg	Value
0	00
1	01
10	01
11	E0
12	00
13	07

14	60
15	FF
16	F0
17	A1
18	E0
19	FF
1A	E0
1B	FF
1C	18

This default can be changed to user selected values by using the SETCFG program.

B.3 Using SETCFG to change configuration registers

The SETCFG.EXE program is designed to enable users to change the configuration registers of OPTi's 386/AT and 486/AT chipset consisting of 82C381/82C382 and 82C481/82C482 respectively. It works with any 386/AT BIOS which boots up with the chipset in default state; and since these chipsets are designed to boot up with any 386/AT BIOS, SETCFG should also be usable with any BIOS.

SETCFG provides the following functions:

1. Read and Write Configuration Registers - CfgRegs
2. Setup SHADOW RAM - ShadowRM
3. Change MEMORY Configuration - Memory_Cfg

HOW TO USE SETCFG

1. Boot up system in default mode with any 386/AT BIOS.

2. Put in Configuration disk and type:

SETCFG <CR>

You should see the sign-on screen with a command line and a description of the product. Read it.

3. Use the cursor arrows to move from command to command, and press <CR> in order to select a command. Select

CfgRegs<CR>

4. The screen clears. A box appears with 3 columns -

Config Reg New Value Old Value

The Old Value is the value that SETCFG has read from 82C381 and 82C382. The New Value is the value that you want to put

into the Configuration Register. Enter new values for each of the registers that needs to be changed. If a particular register does not need to be changed, then bypass it by using the cursor keys.

YOU MUST BE VERY VERY VERY CAREFUL WITH THE VALUES YOU PUT IN THE NEW VALUE COLUMN - IT CAN LOCK UP THE SYSTEM.

After all the new values have been put in, hit

<ESC>

SETCFG will update the values in the 82C381 and 82C382 configuration registers for all bits, EXCEPT:

Shadow Ram and Memory Configuration and Remapping

In order to verify this, select CfgRegs again. You should see that Old Value column has been updated with the New Values, except for Shadow Ram and Memory Configurations

5. In order to change Shadow Ram configuration register values, you must first select the right bits in the New Value column. Then select the ShadowRM command. In order to verify that Shadow RAM has been enabled, select the CfgRegs command again and see that the New Value Shadow Ram select bits have now been transferred to the Old Value column.

6. In order to change Memory Configurations and Remapping, you must first set the correct values in the New Value column under CfgRegs. Then select the Memory_Cfg command. You will be asked whether you are sure:

Do you want to reconfigure the memory with a SYSTEM RESET?(y/n)

If you answer "n <CR>" then SETCFG returns to the command string without making any changes. If you answer "y <CR>", then SETCFG sets up the new memory configurations and resets the system to enable the new memory configurations. When the system reboots, you will see the BIOS access the new memory configuration. If you have put incorrect values (or no values) in New Value for Memory Configuration, the system will hang up. You can also verify the memory configurations, by invoking SETCFG and examining CfgRegs.

B.4 Upgrading the Evaluation Kit to 33 MHz

The DK/HiD-386/AT can be upgraded from 25 MHz to 33 MHz. However, at 33 MHz, the Evaluation Kit is not warranteed to run over the entire operating range. This information is provided so that you can evaluate the viability of developing your own 33 MHz system. Note, at 33 MHz, proper design and layout of timing sensitive signal, like System

Clock become very critical to reliable operation. You must pay attention to timing, layout and FCC issues, in order to have a production worthy 33 MHz system. The changes that have to be made are:

-Oscillator from 50 MHz to 66 MHz
-CPU from 80386-25 to 80386-33
-Tag SRAM from 25ns to 15ns
-Comparator from 11ns to 5.5ns
-Cache SRAM from 35ns to 25ns
-DRAM from 100ns to 80ns for 1WS Write, 60ns for 0WS Write

Note: For 33 MHz Cache designs, controlling the clock waveform is very important. Please check the clock waveform and tweak it in order to implement a reliable system.

C. Trouble shooting

C.1 Error Codes

There are 2 diagnostic LEDs on the Evaluation Board. These LEDs display the status of execution of the BIOS during boot-up. See the respective BIOS manual for the specific description of the error code. For example, if you are using the AMI Evaluation BIOS that is on the Evaluation Board, then refer to Appendix C of the AMI BIOS PLUS User Manual.

D. Compatibility Test Report

OPTi has a compatibility testing program to ensure that OPTi products are compatible with industry standard hardware and software products, used by Personal Computer users.

OPTi's suite of hardware and software products includes products that are very popular, as well as products that are known to have compatibility sensitivities. Software products range from word processors, desktop publishing, spreadsheets, data base managers, benchmarks, utilities, operating systems to compute-intensive CAD software. Hardware products cover the spectrum from multi-function I/O, graphics, memory expansion cards, peripheral controllers to networking environments. In addition, OPTi alpha site OEMs provide intensive compatibility testing.

OPTi's goal is to provide its PC Compatible OEM's products a reputation for being on-par with COMPAQ in compatibility.

Testing Environment

The reference system configuration is:

1. Compaq Deskpro 25, 80386 at 25 MHz
2. 80385 Cache Controller with 32KB Cache
3. 8 MB of Main Memory
4. 1.2 MB 5-1/4" Floppy
5. 80 MB ESDI Hard Disk
6. Paradise 16-bit VGA
7. Compaq standard Keyboard

The target HiD/386 configuration is:

1. DK/HiD-386/AT Evaluation Board, 80386 at 25 MHz
2. Direct Mapped 64 KB Cache
3. 16 MB of Main Memory
4. 1.2 MB 5-1/4" Floppy
5. 40 MB ST506 Hard Disk
6. Paradise 16-bit VGA
7. AT compatible generic Keyboard

Testing Methodology

The basic configuration of HiD/386:

16MB of 80 ns DRAM SIMs
640KB of Conventional Memory, 15MB of Extended Memory
4 way page interleaved
64 KB Cache enabled with 16 byte line size
0 Wait State Write @25 MHz, 1 Wait State Write @ 33MHz
Video and System BIOS Shadowed

Software testing consists of configuring and installing the product, invoking and testing the various functions of the products.

Hardware testing consists of configuring and installing hardware on the target system; and exercising the hardware through diagnostic routines. For testing add-on memory boards, the Main Memory would be reduced appropriately.

The results are marked P (Pass), F (Fail), - (Not Applicable).

Results

All products tested were found to be compatible with the results produced by the reference system. See tables A and B for the detailed results.

Revised: January 24, 1990
Revision: 4

Item	Quantity	Reference	Part	Decal
1	2	J11,J12	PS CON	
2	61	C2,C3,C4,C20,C31,C32,C36, C37,C40,C45,C47,C49,C51, C52,C53,C54,C55,C56,C57, C58,C59,C60,C67,C68,C71, C72,C73,C76,C77,C78,C79, C81,C83,C84,C85,C86,C87, C91,C93,C96,C97,C99,C104, C105,C107,C108,C112,C113, C114,C115,C116,C117,C118, C119,C120,C123,C124,C125, C126,C127,C129	0.1UF	DCAP
3	26	C12,C10,C13,C14,C15,C16, C17,C18,C23,C33,C34,C35, C38,C39,C41,C42,C43,C44, C46,C48,C50,C62,C69,C75, C95,C98	10UF TANT	TANCAP
4	4	C121,C70,C92,C134	0.001UF	DCAP
5	2	C143,C136	1UF	DCAP
7	1	C82	1.0UF	DCAP
8	3	U16,U31,U37	74F08	DIP14\300
9	1	U6	7407	DIP14\300
10	1	U11	74F32	DIP14\300
11	1	U1	74LS14	DIP14\300
12	1	U26	80386	PGA\132P
13	10	RP14,RP9,RP12,RP13,RP15, RP16,RP17,RP18,RP19,RP22	RSIP9 10K	SIP\10P
14	1	R39	510	AXIAL
15	1	R38	2K	AXIAL
16	1	U25	3167/387	PGA\121P
17	2	JP2,JP1	2-W JUMP	SIP\2P
18	27	R40,R1,R2,R5,R12,R13,R15, R16,R17,R18,R21,R22,R28, R29,R30,R34,R35,R36,R37, R42,R48,R51,R53,R54,R55,	10K	AXIAL

Item	Quantity	Reference	Part	
		R58,R59		
19	8	U41,U38,U39,U40,U60,U61, U62,U63	8KX8	DIP20\300
20	12	RP20,RP1,RP2,RP3,RP4,RP5, RP6,RP7,RP8,RP10,RP11, RP21	RSIP7 10K	SIP\8P
21	7	U59,U27,U34,U50,U51,U53, U58	74F244	DIP20\300
22	4	JP4,JP3,JP5,JP6	3-W JUMP	SIP\3P
23	1	U36	74F86	DIP14\300
24	1	U33	74F139	DIP14\300
25	6	U19,U9,U10,U14,U17,U18	74ALS245	DIP20\300
26	16	R44,RA1,RA2,RA3,RA4,RA5, RA6,RA7,RA8,R23,R24,R41, R43,R45,R46,R47	33	AXIAL
27	1	U12	74ALS244	DIP20\300
28	1	J24	CON-4	SIP\4P
29	1	U29	50MHZ	OSCILATOR DIP TYPE
30	1	U30	27512	DIP28\600
31	1	Y2	14.3MHZ	CRYSTAL
32	1	R49	1M	AXIAL
33	1	R50	10	AXIAL
34	1	C111	5-50PF	DCAP
35	3	C109,C5,C110	22PF	DCAP
36	1	C135	27PF	DCAP
37	1	U28	82C381	SMD-136PIN
38	1	R56	33	AXIAL
39	2	C65,C89	10UF	TANCAP
40	4	R33,R9,R32,R52	4.7K	AXIAL

Item	Quantity	Reference	Part	
42	1	R31	100	AXIAL
43	1	U20	TL7705A	DIP8\300
44	1	U32	74F00	DIP14\300
45	1	U5	74F04	DIP14\300
46	1	U35	82C382	SMD-160PIN
47	1	U55	74LS245	DIP20\300
48	1	U15	74ALS373	DIP20\300
49	4	U22,U21,U23,U24	74F245	DIP20\300
50	9	J21,J1,J2,J3,J4,J5,J6,J7, J8	CON-31X2	62PIN BUS CONNECTOR
51	9	J22,J13,J14,J15,J16,J17, J18,J19,J20	CON-18X2	36PIN BUS CONNECTOR
52	1	U13	82C206	SMD-84PIN
53	1	Y1	32.8K	CRYSTAL
54	1	J10	BAT CON	SIP\4P
55	2	CR3,CR2	1N4148	AXIAL
56	1	Q2	2N3904	
57	1	Q1	2N3906	
58	2	U8,U7	74LS373	DIP20\300
59	2	R10,R11	470	AXIAL
60	1	U4	8042	DIP40\600
61	2	J23,J9	CON-5	J23:SIP,5P J9:KEYBOARD CONNECTOR
62	2	L1,L2	FERRITE BEAD	AXIAL
63	3	C22,C9,C21	470PF	DCAP
64	1	R57	150 1/4W	AXIAL
65	1	C11	CER 0.1UF	DCAP
66	1	R7	10K	AXIAL

Item	Quantity	Reference	Part	
68	1	C8	0.0047UF	DCAP
69	2	C6,C7	0.1UF	DCAP
70	1	C19	10UF 25V	TANCAP
71	1	R4	2M	AXIAL
72	1	R6	51K	AXIAL
73	1	U3	MC14069	DIP14\300
74	1	R20	51	AXIAL
75	4	R14,R25,R26,R27	330	AXIAL
76	1	R60	100 1/4W	AXIAL
77	1	CR4	LED	
78	1	CR1	1N914	AXIAL
79	1	C1	TANT 10UF	TANCAP
80	1	U52	74F521	DIP20\300
81	1	U57	16KX1 SRAM	DIP20\300
82	2	U56,U54	16KX4 W/O	DIP22\300
83	1	SW1	SW PUSHBUTTON	SIP\2P
84	1	R3	51	AXIAL
85	1	U2	74F74	DIP14
86	8	U49,U42,U43,U44,U45,U46, U47,U48	SIM	SIM MOUDLE

The Product Evaluation on Compatibility Check List

Product Name: OPTi 82C381/82C382 Revision B

I. Software Compatibility

Software Name	Version	Result
PC DOS	3.3	Pass
IBM OS/2	1.1	Pass
SCO XENIX SYSTEM V/386	2.2.3	Pass
PC-MOS 386	2.10	Pass
DESQVIEW	2.25	Pass
MS. WINDOWS/386	2.03	Pass
AUTOCAD	10.0	Pass
LOTUS 123	2.01	Pass
IBM DIAGNOSTICS	2.04	Pass
PCTOOLS	5.10	Pass
QAPLUS	3.01	Pass
CROSSTALK		Pass
PROCOMM		Pass
PARADOX3		Pass
DBASE III	1.1	Pass
FRAMEWORK II	1.1	Pass
PC LABS BENCHMARK	4.2	Pass
POWER METER	1.2,1.5	Pass
LANDMARK	.99,1.14	Pass
CKECKIT		Pass
CORETEST		Pass
IBM ADVANCED DIAGNOSTICS		Pass
BUS MASTER/DMA DIAGNOSTICS		Pass
FLIGHT SIMULATOR3		Pass
DUGDIGGER		Pass
WORD	4.0	Pass
WORDPERFECT	4.2	Pass
QUATTRO		Pass
SYMPHONY	2	Pass
PAGEMAKER		Pass
VENTURA WITH LIM 4.0	2.0	Pass
QEMM		Pass
386MAX		Pass
LIM386		Pass
SEMMS		Pass
IBM PC/DOS	3.3,4.0	Pass
MICROSOFT OS/2	1.10	Pass
DESQVIEW 386		Pass
THEOS 386	3.0	Pass
ORCAD	1.2,3.2	Pass
WORKVIEW		Pass
MCAD		Pass
ORCAD-PCB LAYOUT	1.2	Pass
ABEL		Pass

Software Name		Result
XTREE	1.0	Pass
PCTOOLS	4.24	Pass

II. Hardware Compatibility

A. Disk Controller	Result
UPC Controller	Pass
DC2 MEM Controller	Pass
UDC MFM Controller	Pass
ADAPTEC 2322 ESDI Controller	Pass
ADAPTEC 2732 RLL Controller	Pass
DTC 5287 RLL Controller	Pass
EVEREX Controller	Pass
WD-1003 WA2(ST-506)	Pass
Seagate ST225 Hard Disk	Pass
Archive 2150L Tape Drive	Pass
ADAPTEC AHA-1540 scsi (Master Card)	Pass
WD SCSI (Slave Card)	Pass
Cirrus Logic 1:1	Pass
NCL SCSI	Pass
DTC 5280i rev C +2 Controller	Pass

B. Video Card	Result
Hercules Adapter	Pass
DGP Card	Pass
LEGA Card	Pass
DEGA Card	Pass
CEGA Card	Pass
CVGA Cirrus 8-bit VGA	Pass
MVGA C&T 16-bit VGA	Pass
Paradise VGA Card	Pass
Tseng-Lab VGA Card	Pass
C&T EGA	Pass
Genoa EGA	Pass
Video 7 VGA Deluxe	Pass
Video 7 Fastwrite VGA	Pass
Orchid Designer 8-bit/16-bit	Pass
Matrox Graphics	Pass
Pixelworks	Pass
IBM VGA	Pass

C. Communication	Result
Internal Modem	Pass
Hayes 2400B External Modem	Pass

D. Networking	Result
3COM 8/16-bit Ethernet Station	Pass
Novell Advanced Netware 2.12	Pass
- NE 2000	Pass
- Etherlink Plus 3C505	Pass
- Novell DCB Card	Pass
Novell Server	Pass
3COM 3+ Share/Etherlink Plus 3C505	Pass

E. Miscellaneous	Result
80387 Coprocessor	Pass
NEC Display Monitor	Pass
Sony Display Monitor	Pass
Mouse Systems Serial Mouse	Pass
Centronics Printer Port	Pass
IOS/IOSA Card	Pass
ARCNET Card	Pass
Intel Above Board	Pass
AST Rampage Card	Pass
BOCARAM	Pass
Everex 10000	Pass
JRAM-AT4	