PAGE MODE MEMORY CONTROLLER

SL9350

PRELIMINARY

FEATURES

- **16, 20, 25 MHz Options.**
- **Enhanced fast page mode design.**
- **Programmable wait state options.**
- **Shadow Ram feature.**
- **Supports 16 M byte of on board memory.**
- **Can use 256K x 1, 1 Meg x 1, and 256K x 4 DRAMs or a mix.**
- **Supports 100 ns DRAMs at 16 MHz and 80 ns at 20 MHz.**
- **Automatic remapping of 640K - 1 M RAM to top of the address space.**
- **Advance CMOS Technology.**
- **100 pin Flatpack.**

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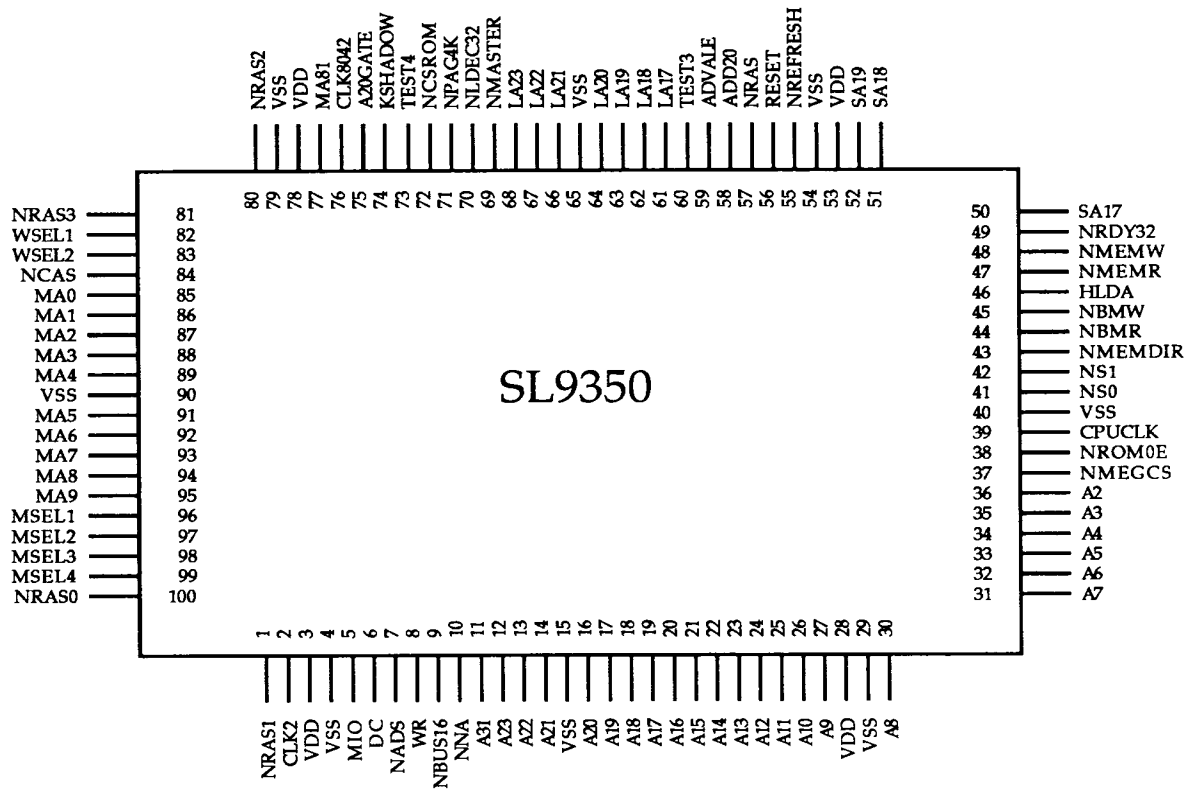
PINOUT



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PIN DESCRIPTION SL9350

SYMBOL	PIN	TYPE	DESCRIPTION
A2-A16	36,35,34,33, 32,31,30,27, 26,25,24,23, 22,21,20	I	CPU address bus.
A17-A23	19,18,17,16, 14,13,12	I/O	CPU address bus.
A31	11	I/O	CPU address bus.
A20GATE	75	I/O	CPUA20 is forced low when A20GATE is low and is transmitted as generated by CPU when A20GATE is high.
ADD20	58	O	Decoded 20-bit address bit used to generate address decode for 1 M RAMs.
ADVALE	59	I	Advanced address latch enable from memory controller. It latches local bus address for the system bus.
CLK2	2	I	Double frequency clock signal for synchronous operation. It is divided by two to get the processor clock.
CLK8042	76	I	7 MHz clock, generates 10µs RAS TIMOUT.
CPUCLK	39	I	Derived from CPUCLK2. It is half the frequency of CLK2.
DC	6	I	Status signal. Differentiates between Data and Control instructions.
HLDA	46	I	Asserted to signal that the CPU has relinquished control of the bus to the requesting device.
KSHADOW	74	I	Keyboard controller selectable option for Shadow RAMs.
LA17-LA23	61,62,63,64, 66,67,68	I/O	Local address bus.
MA0-MA9	85,86,87,88, 89,91,92,93, 94,95	O	RAM address bus.
MA81	77	O	RAM address select pin for 1M RAMs.
MIO	5	I	Memory Input/Output is the signal from the CPU. When high, it indicates a memory cycle, when low it indicates an I/O cycle. It is being used to generate memory and I/O signals for the system.

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PIN DESCRIPTION SL9350 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
MSEL1-4	96,97,98,99	I	On-board Fast RAM memory size and type select.
NADS	7	I	Low assert address status signal. Asserted when Address Bus outputs are valid.
NBMR	44	O	Buffered Memory Read signal.
NBMW	45	O	Buffered Memory Write signal.
NBUS16	9	O	Bus size 16. Activates 16-bit data bus operation; data is transferred on the lower 16 bits of the data bus and an extra cycle is provided for transfers of more than 16 bits.
NCSROM	72	O	Low assert read only memory chip select.
NLDEC32	70	I	Decode signal for on-board local high-speed RAM.
NMASTER	69	I	Asserted when an external device has control of the AT Bus.
NMCAS	84	O	Memory column address strobe. Asserted when either CPU or DMA is accessing the memory.
NMEGCS	37	O	Select decode for lower 1M of RAM.
NMEMDIR	43	O	Direction select between D Bus and MD Bus. Read when low, generated by AT system controller SL9010, write when high for non 32-bit.
NMEMR	47	I	Read memory.
NMEMW	48	I	Write memory.
NNA	10	I	Next address. Asserted for address pipe-lining. Enables CPU to put out address and status signals for the next Bus cycle during the current cycle.
NPAG4K	71	I	Active low page size = 4K option; when 1M DRAMs are used. Left high for 256Ks or mixes.
NRAS	57	O	Low assert Row address strobe.
NRAS0-3	100,1,80,81	O	Row address strobes for Banks 0,1,2, &3 for the on-board memory. Generated during CPU or DMA cycle for memory access.

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PIN DESCRIPTION SL9350 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
NRDY32	49	O	Asserted one clock cycle after NNA is asserted at the end of a 32-bit memory cycle.
NREFRESH	55	I	On-board RAM refresh signal. Generated from REFREQ input.
NROM0E	38	O	Enables ROM output during ROM read cycles.
NS0,1	41,42	O	80286 compatible status signals for the AT system controller SL9010.
RESET	56	I	Active high reset from system controller.
SA17	50	O	System Address Bus.
SA18,19	51,52	I/O	System Address Bus.
TEST3	60	I	Optional disable for 684K - 1M [384K] remap.
TEST4	73	I	Test Pin - Not connected.
VDD	3,28,53,78	-	+5V. Power.
VSS	4,15,29,40, 54,65,79,90	-	0V. Ground.
WR	8	I	Status signal write when high.
WSEL1,2	82,83	I	Wait-state select options.

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DC CHARACTERISTICS SL9350

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA **
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA **
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD

NOTES:

* VIH = VDD, VIL = Vss

** With Certain restrictions on pin assignment.

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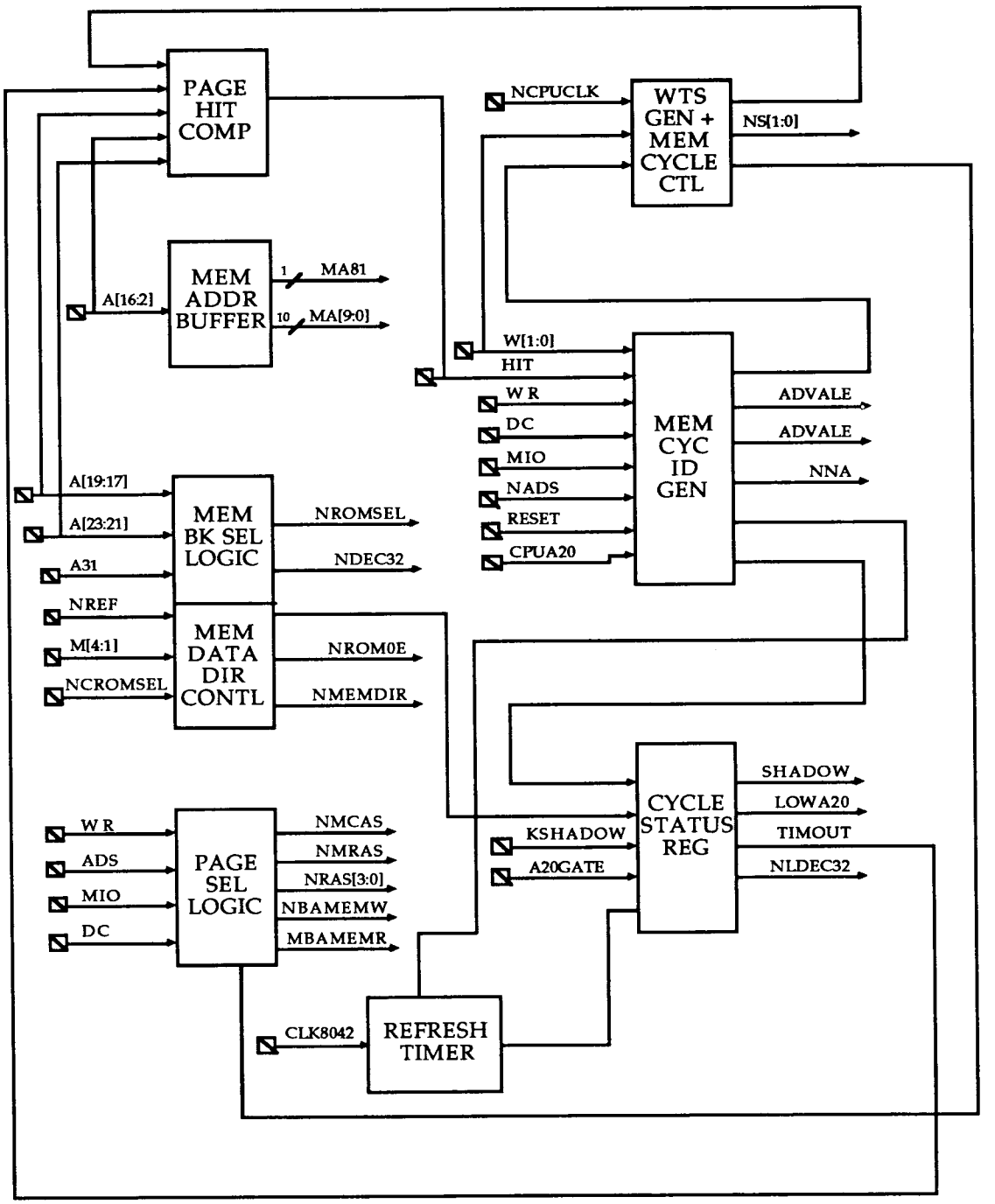
BLOCK DIAGRAM



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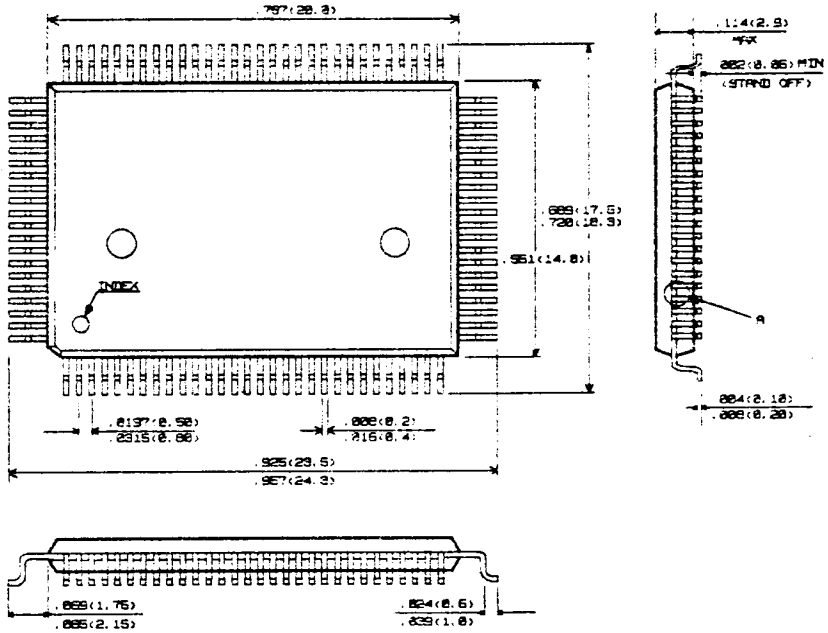
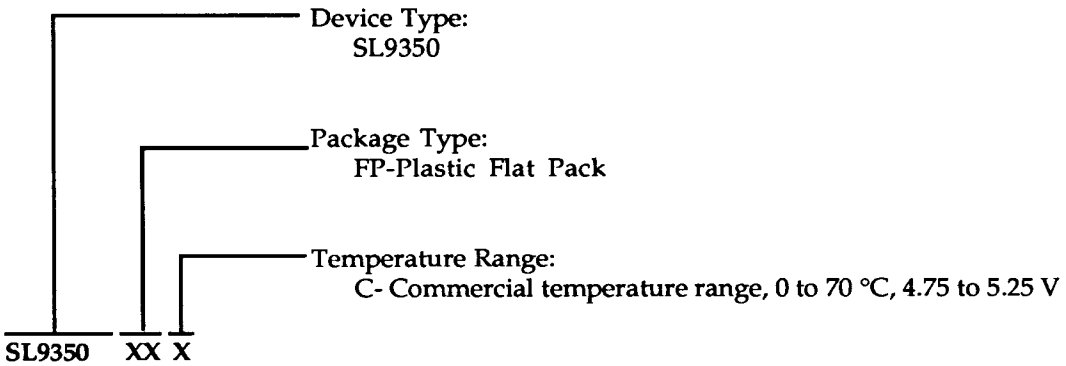
Package Information

100 Pin Flat Pack



ORDERING INFORMATION



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