LOGICSTAR

ADDRESS CONTROLLER
SL9025

PRELIMINARY

FEATURES

- **Supports 80386, 80386 SX (P9), and 80286-based AT designs.**
- **Address In to Address Out time is 15 ns.**
- **24 mA buffers.**
- **Include SA & XA buffers.**
- **Provides Refresh for 256K, 1M or 4Mbit DRAM chips.**
- **Advance CMOS Technology.**
- **100 pin Flatpack.**

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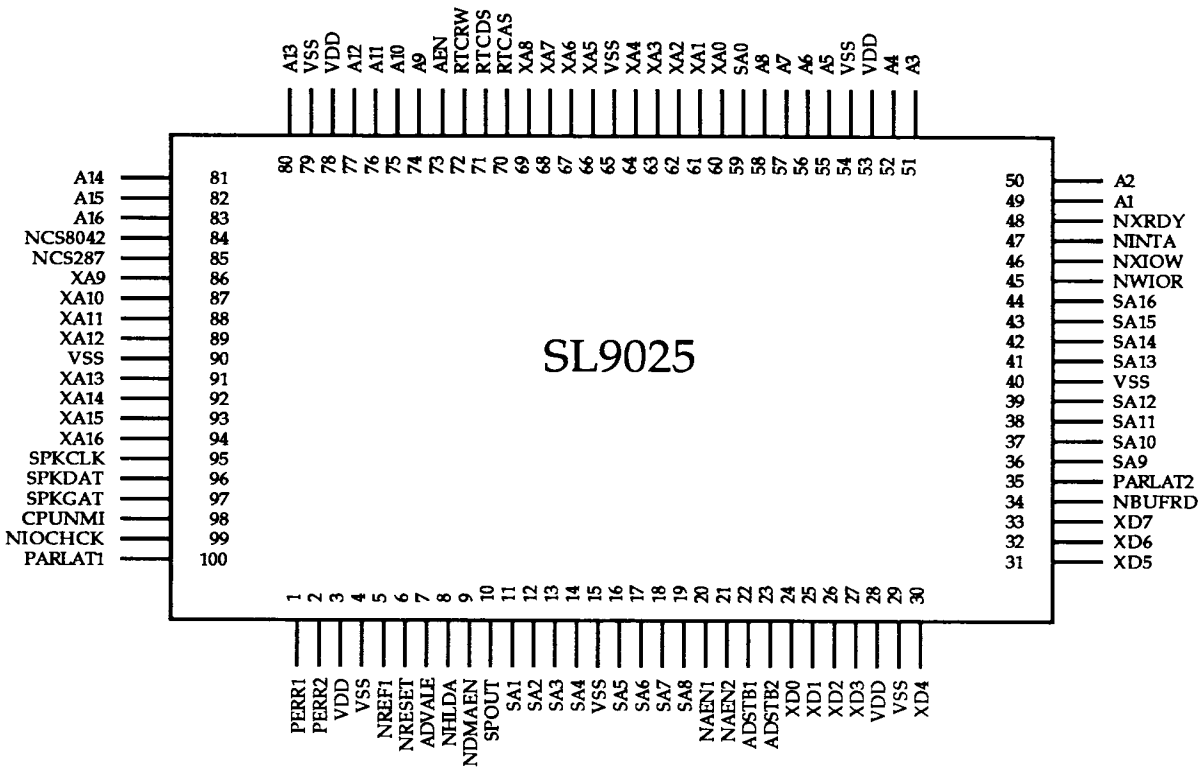
PINOUT



PIN DESCRIPTION SL9025

SYMBOL	PIN	TYPE	DESCRIPTION
A1-A16	49,50,51,52, 55,56,57,58, 74,75,76,77, 80,81,82,83	I/O	CPU Address bus.
ADSTB1,2	22,23	I	Address strobes to latch XD data from DMA controllers to XA Bus. ADSTB1 is active for 8-bit DMA transfers while ADSTB2 is active for 16-bit DMA transfers.
ADVALE	7	I	Advance address latch enable from memory controller. It latches local bus address for the system bus.
AEN	73	I	High for DMA cycle. Prevents DMA from accessing on-board peripherals. When low, enables data buffers between XD Bus and SD Bus.
CPUNMI	98	O	CPU non-maskable interrupt.
NAEN1,2	20,21	I	Adress enable 1 and 2. 8-bit and 16-bit DMA modes respectively.
NBUFFRD	34	O	Direction control for data buffer between SD Bus and XD Bus.
NCS287	85	I/O	Active low numeric processor chip select.
NCS8042	84	I/O	Keyboard controller chip select. Active low signal.
NDMAEN	9	I	DMA enable. When low, indicates a DMA cycle.
NHLDA	8	I	Hold acknowledge. Asserted by CPU. When high, indicates that the CPU has released the bus.
NINTA	47	I	Interrupt acknowledge. When active(low) indicates that the interrupt acknowledge is active.
NIOCHCK	99	I	I/O channel check. Active low signal from the AT bus. When low it indicates NOT ready condition and asserts wait states. When high it allows termination of AT bus cycle.

PIN DESCRIPTION SL9025 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
NREF1	5	I	Refresh cycle. Asserted low during RAM refresh cycles.
NRESET	6	I	Systems reset. Active low, generated by systems controller.
NXIOR	45	I	X Bus I/O Read.
NXIOW	46	I	X Bus I/O Write.
NXRDY	48	I	X ready. When low, indicates a peripheral bus cycle.
PARLAT1,2	100,35	I	Parity error from lower 16 bit mode.
PERR1,2	1,2	I	Parity error from lower and upper 16 bits.
RTCAS	70	O	Active high real time clock address strobe.
RTCDS	71	O	Active high real time clock data strobe.
RTCRW	72	O	Active high real time clock read cycle/ write cycle input.
SA0	59	O	System bus address A0.
SA1-SA16	11,12,13,14, 16,17,18,19, 36,37,38,39, 41,42,43,44	1/O	System address bus.
SPKCLK	95	O	Speaker clock.
SPKDAT	96	O	Speaker data active high output used to gate the timer tone signal to the speaker.
SPKGAT	97	O	Speaker gate enables timer tone signal to the speaker.
SPOUT	10	I	Speaker out to the speaker.
VDD	3,28,53,78	-	+5V. Power.
VSS	4,15,29,40, 54,65,79,90	-	0V. Ground.
XA0	60	I	Peripheral bus address A0.

PIN DESCRIPTION SL9025 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
XA1-XA16	61,62,63,64, 66,67,68,69, 86,87,88,89, 91,92,93,94	I/O	Peripheral address bus.
XD0-XD7	24,25,26,27, 30,31,32,33	I/O	Peripheral data bus.

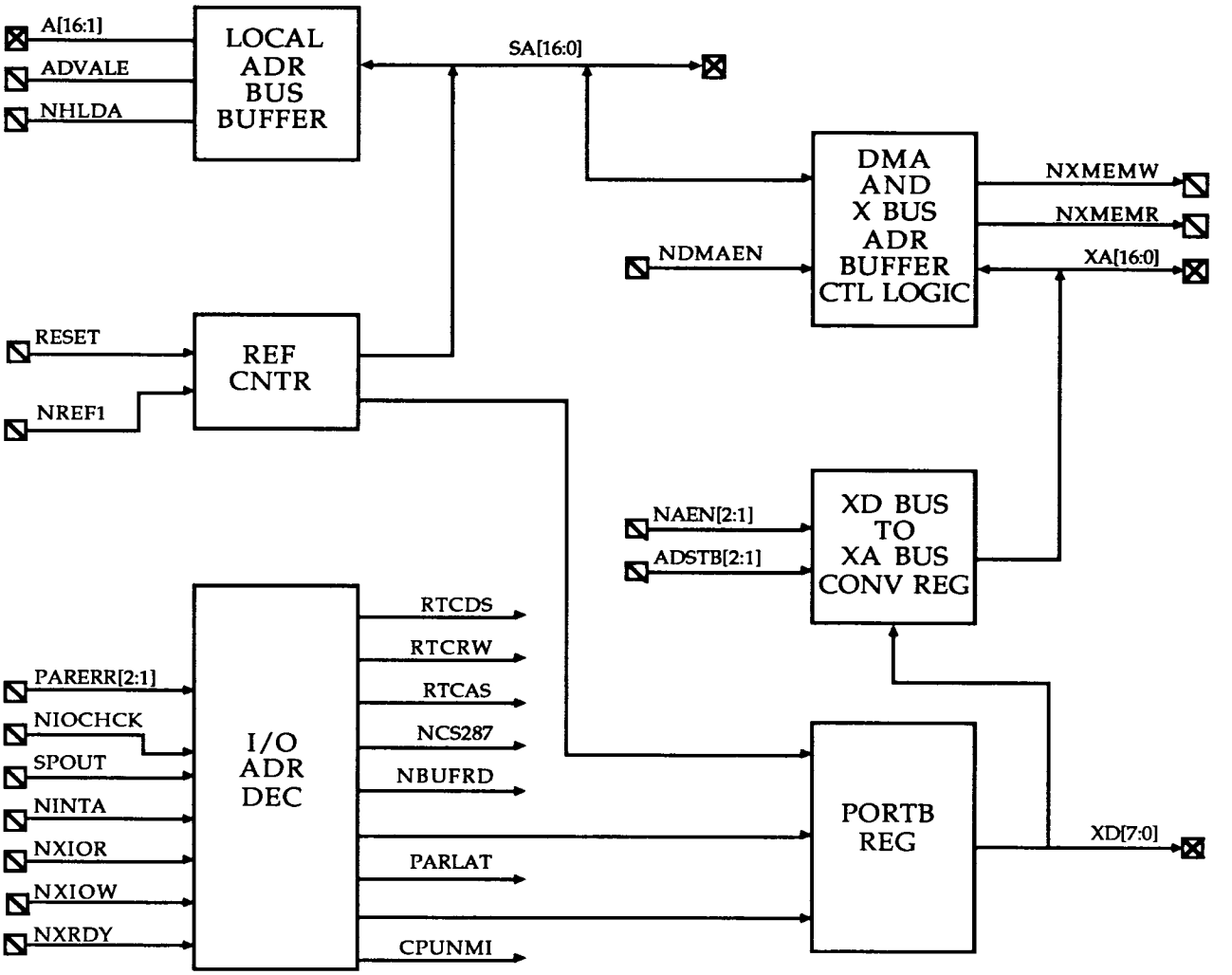
DC CHARACTERISTICS SL9025

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL		0.3VDD	V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD

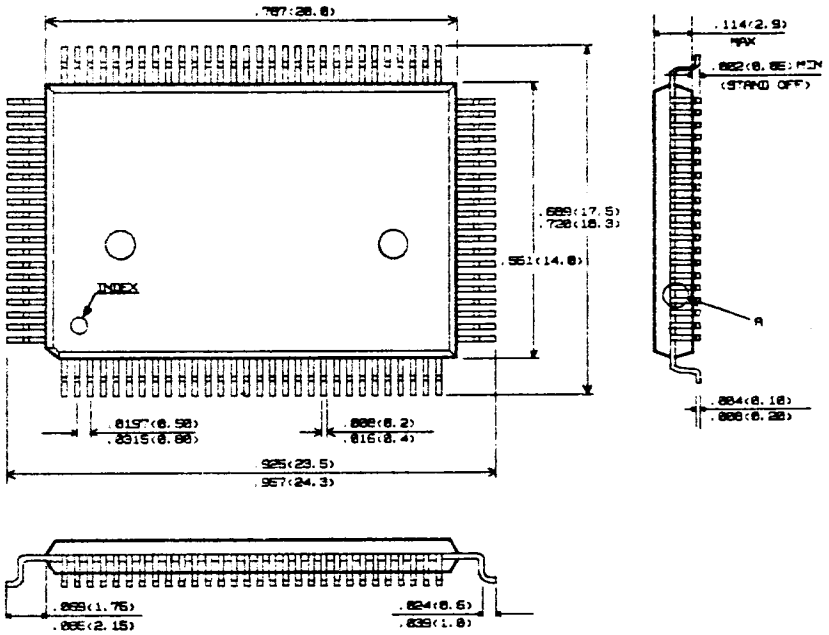
NOTES:
* VIH = VDD, VIL = Vss

BLOCK DIAGRAM

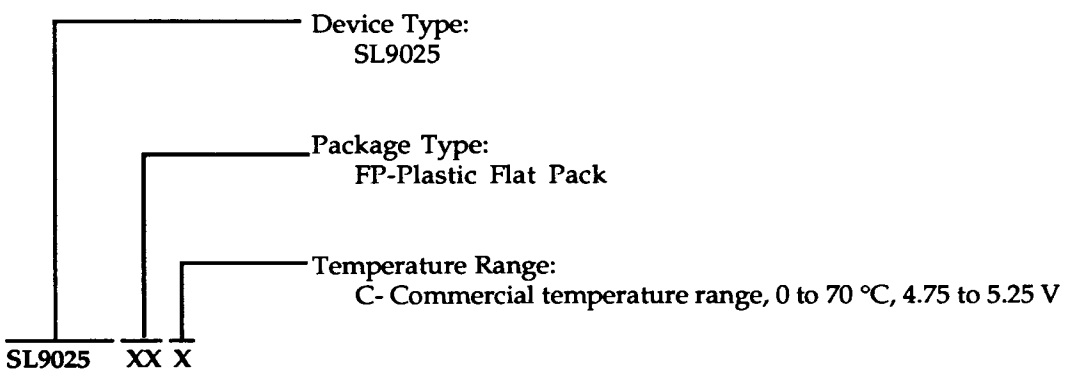


Package Information

100 Pin Flat Pack



ORDERING INFORMATION



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