LOGICSTAR

SYSTEM CONTROLLER
SL9010

PRELIMINARY

FEATURES

- **AT system control logic.**
- **Supports 80386, 80386 SX (P9), or 80286-based designs.**
- **16, 20, 25 MHz options.**
- **Clock switching and reset logic.**
- **Programmable wait states for Memory and I/O.**
- **Programmable command delays for Memory.**
- **Advanced ALE generation.**
- **Advanced Command generation.**
- **Advance CMOS Technology.**
- **100 pin Flatpack.**

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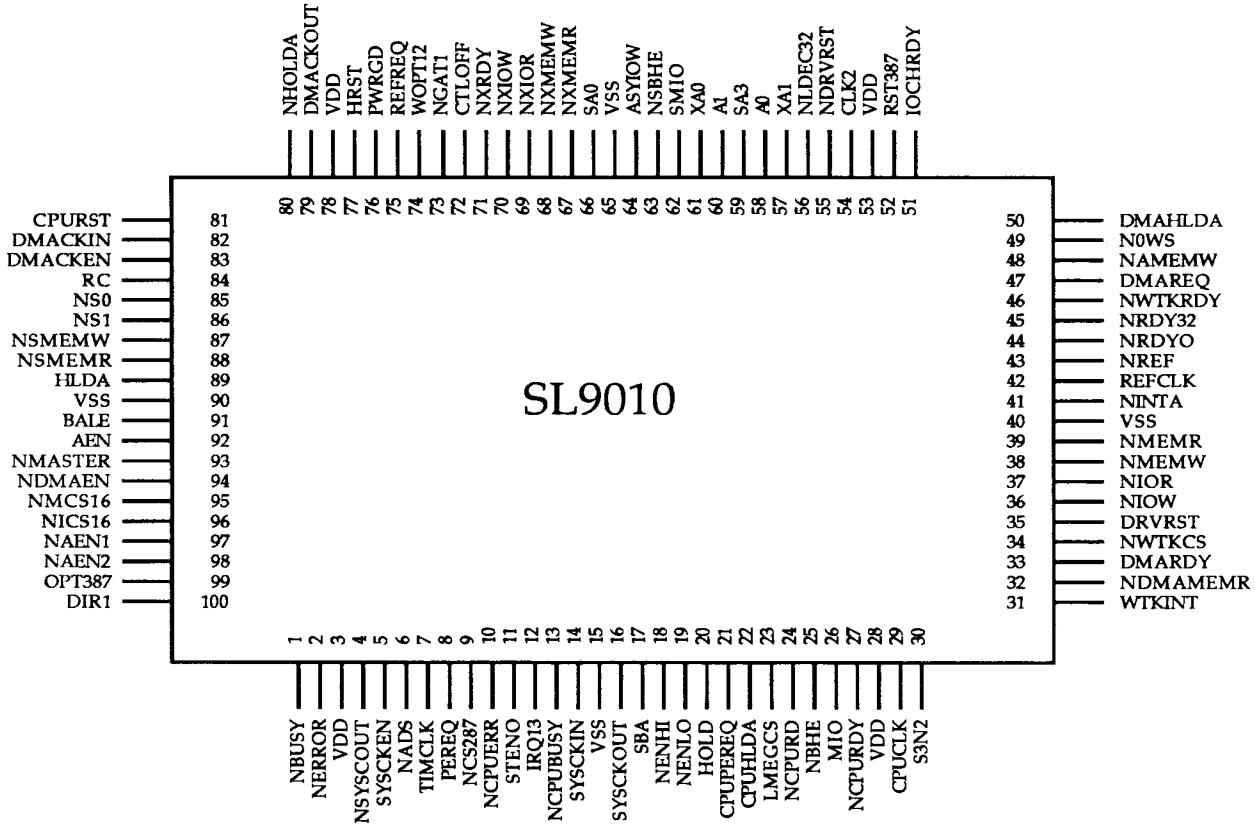
PINOUT



PIN DESCRIPTION SL9010

SYMBOL	PIN	TYPE	DESCRIPTION
A0,1	58,60	I	Local bus least significant address lines.
AEN	92	O	When low, enables data buffers between XD Bus and SD Bus. It is high during DMA cycles.
ASYIOW	64	O	Asynchronous Input/Output write is an active low output. It is asserted with NIOW but it is negated one CPUCLK later.
BALE	91	O	Buffered address latch enable.
CLK2	54	I	Input from clock chip. Has twice the frequency of the processor clock.
CPUCLK	29	I	Derived from CLK2. It is half the frequency of CLK2.
CPUHLDA	22	I	CPU hold acknowledge: It is an active high when a Bus cycle is granted in response to hold request(HOLD).
CPUPEREQ	21	O	CPU processor entension request. When active (high) it indicates to CPU that NPX is ready for data transfer to/ from its data FIFO. When FIFO is empty, this signal is negated.
CPURST	81	O	CPU reset. Active high output. When asserted it resets CPU.
CTLOFF	72	O	Control output flag. Rising edge clocks data from SD[7:0] to D[7:0] latches during Bus-conversion cycles.
DIR1	100	O	Direction 1. Controls data transfer between SD[7:0] and SD[15:8].
DMACKEN	83	I	DMA clock enable. Jumper input when low, selects external DMA clock [DMACKIN] for internal use. When high it selects internally generated DMA clock which is divided by 4 of CPUCLK.
DMACKIN	82	I	DMA Clock In is an optional external input for DMA clock. When this option is used the internally generated DMA clock is not used.
DMACKOUT	79	O	DMA clock out is generated by dividing CPU clock by 4. This output may be left unconnected if an external DMA clock source is used.
DMAHLDA	50	O	DMA hold acknowledge is asserted high during DMA cycles.

PIN DESCRIPTION SL9010 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
DMARDY	33	O	DMA ready is asserted high to indicate to the DMA that the current I/O read cycle may be negated.
DMAREQ	47	I	DMA request is asserted high to request a DMA cycle. It indicates hold request (HOLD) to the CPU for a DMA cycle to begin.
DRVRST	35	O	Device reset is an active high output. When asserted it resets the AT system.
HLDA	89	O	Hold acknowledge is an active high output. When asserted it indicates that CPU has released its control on the local bus in favor of another bus master device (DMA external master). The signal comes from the CPU.
HOLD	20	O	Hold is asserted high whenever another bus master device like DMA or an external master wants to become a bus master. The signal goes to the CPU.
HRST	77	I	Hardware reset is asserted high to generate systems reset. It is connected to the PCB's reset switch.
IOCHRDY	51	I/O	I/O channel ready is an active high input from the AT bus. When low it indicates a not ready condition and inserts wait states in AT I/O or AT memory cycles. It is an output during NPX reset cycle.
IRQ13	12	O	Interrupt request 13 is an active high output which indicates an interrupt fronm the numeric coprocessor.
LMEGCS	23	I	Lower 1 meg chip select is an active high input,when asserted it indicated that lower 1 meg memory is being selected
MIO	26	I	Memory Input/Output is the signal from the CPU. When high, it indicates a memory cycle, when low, it indicates an I/O cycle. It is being used to generate memory and I/O signals for the system.
NADS	6	I	Address strobe is an active low input generated by the CPU. When asserted it indicates the start of a bus cycle.
NAEN1,2	97,98	I	DMA enable 1,2 is an active low input. When NAEN1 is asserted low it indicates an 8-bit DMA cycle. When NAEN2 is asserted low it indicates a 16-bit DMA cycle. When they both are high it indicates that a non-DMA device owns the system's bus controls. They can not be low at the same time.

PIN DESCRIPTION SL9010 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NAMEMW	48	I	Advance memory write is an active low input. It is asserted for local memory write cycles.
NBHE	25	I	Byte high enable is an active low input signal which indicates the transfer of data on the high byte of the data bus. It is also asserted for 16-bit bus cycles.
NBUSY	1	I	NPX busy is an active low input from the NPX, indicating that it is currently executing a command. It is used to generate busy signal to the CPU.
NCPUBUSY	13	O	CPU busy is an active low output to the CPU indicating that the NPX is busy executing a command.
NCPUERR	10	O	CPU error is an active low output from the NPX to the CPU indicating that an unmarked error condition exists.
NCPURD	24	O	CPU read is an active low output when set the direction of high data byte between D Bus and SD Bus.
NCPURDY	27	O	CPU ready is an active low output which goes to CPU's ready input. When asserted, CPU terminates its current bus cycle.
NCS287	9	I	NPX chip select is an active low input which is asserted for I/O port addresses 00F0 and 00F1.
NDMAEN	94	O	DMA enable is an active low output. When asserted it indicates a DMA cycle is in progress; either 8-bit or 16-bit.
NDMAMEMR	32	I	DMA memory read is an active low input. It is asserted during DMA memory read cycle. This input is synchronized with the DMACLK and drives the output NXMEMR.
NDRVRST	55	O	Device reset is an active low output. When asserted it resets the AT system.
NENHI	18	O	Enable high byte is asserted low to enable High byte data transfer between D Bus and SD Bus.
NENLO	19	O	Enable low byte is asserted low to enable low byte data transfers between D Bus and SD Bus.
NERROR	2	I	NPX error is an active low input. When asserted it indicates that a non-markable interrupt has occured during the current command cycle.

PIN DESCRIPTION SL9010 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NGAT1	73	O	Gate 1 is asserted low to enable data buffer between high byte and low byte of SD Bus. It is used in bus conversion cycles.
NHOLDA	80	O	Hold acknowledge is an active low output. When asserted it indicates that CPU has released its buses & controls on the local bus in favor of another bus master device (DMA/external master).
NICS16	96	I	Input/Output chip select 16 is an active low input. It is asserted from AT bus by a 16-bit I/O device to indicate a 16-bit bus cycle. When high it implies an 8-bit I/O transfer.
NINTA	41	O	Interrupt acknowledge is an active low output for the interrupt controller. It is also used to direct data from the XD bus to SD bus during and interrupt acknowledge cycle.
NIOR	37	I/O	Input/Output read is an active low bi-directional pin for the AT system's bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle.
NIOW	36	I/O	Input/Output write is an active low bi-directional pin for the AT system's bus. It is an output for CPU and DMA cycles and an input during an external master bus cycle.
NLDEC32	56	I	Local decode 32 is an active low input. When active it indicates a local 32 bit memory for 386 based systems and local 16-bit memory for 386SX based systems.
NMASTER	93	I	External master is an active low input from the AT bus. When asserted, indicates that an external master device is currently active.
NMCS16	95	I	Memory chip select 16 is an active low input from the AT bus. When asserted indicates a 16 bit memory cycle. When high it implies an 8-bit memory transfer.
NMEMR	39	I/O	Memory read is an active low bi-directional pin on the AT system's bus CPU, DMA and refresh cycles. It is an input when an external master is active on the AT bus.
NMEMW	38	I/O	Memory write is an active low bi-directional pin on the AT system's bus. It is an output CPU and DMA cycles. It is an input when an external master is active on the AT Bus.

PIN DESCRIPTION SL9010 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
N0WS	49	I	Zero wait state is an active low input from the AT system's bus. It causes immediate termination of a bus cycle.
NRDYO	44	I	Ready output is an active low input from the NPX to terminate an NPX bus cycle.
NRDY32	45	I	Ready 32 is an active low input. It is asserted for 32-bit local memory cycles and 16-bit ROM cycles for 386SX based systems it is asserted for 16-bit local memory cycles.
NREF	43	I/O	Refresh is an active low bi-directional pin. It is asserted during refresh cycle. It is an input at all other times.
NS0,1	85,86	I	Status1,0 is an active low input from the memory controller. It is used by the system to determine the type of bus cycle. (Write, read, ideal or INTA).
NSBHE	63	I/O	Byte high enable is an active low bi-directional pin for the AT bus. It indicates the transfer of data on the high byte of the data bus. It is also asserted for 16-bit bus cycles. It is an output for CPU and DMA cycles and an input for an external master cycle.
NSMEMR	88	O	Memory read is an active low tri-state output for the AT bus. It is an output for CPU, DMA and refresh cycles. It goes to tri-state when lower 1 meg memory is accessed.
NSMEMW	87	O	Memory write is an active low tri-state output for the AT bus. It is an output for CPU and DMA cycles. It goes tri-state when lower 1 meg memory is accessed.
NSYSCOUT	4	O	Low assert system clock out is an inverted version of SYSCOUT.
NWTKCS	34	I	WIETEK chip select is an active low input. When asseted it disables AT bus controller to allow NPX enough time to complete an NPX bus cycle.
NWTKRDY	46	I	WIETEK Ready is an active low input to terminate an NPX bus cycle.
NXIOR	69	I/O	Peripheral bus Input/Output read is an active low bi-directional pin. It is an output for CPU, refresh and an external master cycles. It is an external master cycle. It is an input for DMA cycles.
NXIOW	70	I/O	Peripheral bus Input/Output write is an active low bi-directional pin. It is an output for CPU, refresh and an external master cycles. It is an external master cycle. It is an input for DMA cycles.

PIN DESCRIPTION SL9010 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NXMEMR	67	I/O	Peripheral bus memory read is an active low bi-directional pin. It is an output for CPU, refresh and external master cycles. It is also an output for DMA cycles.
NXMEMW	68	I/O	Peripheral bus memory write is an active low bi-directional pin. It is an output for CPU, refresh and external master cycles. It is also an output for DMA cycles.
NXRDY	71	O	Ready is an active low output. When asserted it indicates termination of a CPU bus cycle. It also resets AT's bus cycle state machine.
OPT387	99	I	Option 387 is a jumper select input. When high, allows the NPX NBUSY to pass through to NCPUBUSY. Else TIMCLK appears on NCPUBUSY.
PEREQ	8	I	NPX peripheral request is an active high input. When asserted it indicates to the CPU that NPX is ready to transfer data to/ from it's data FIFO. When all data is written to or read from the data FIFO, PEREQ is negated.
PWRGD	76	I	Power good is an active high input from the power supply.
RC	84	I	External CPU reset is an active low input. When asserted it resets the CPU by generating CPURST. It may come from a debounce switch.
REFCLK	42	O	Refresh clock is an active low output asserted during refresh cycle for three SYSCKOUT cycles.
REFREQ	75	I	Refresh request is an active high input. When asserted, requests and starts a refresh cycle.
RST387	52	O	Reset 387 is an active high output. It is asserted when I/O port 00F1 is written into. The signal is active for 96 CPUCLK cycles.
S3N2	30	I	386/286 mode select. It is a jumper option. It is high for 386 or 386SX based systems and low for 286 based systems.
SA0	66	I/O	System's bus address 0-bit. It is a bi-directional pin.
SA3	59	I	System's bus address 3-bit. It is an input.
SBA	17	O	Select data buffer data. When high it selects latched SD Bus low byte data onto D Bus during bus conversion cycles.

PIN DESCRIPTION SL9010 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
SMIO	62	I/O	Memory Input/Output for the system bus. When high it indicates a memory cycle. When low it indicates an I/O cycle.
STENO	11	O	Status enable is an active high output. This pin serves as a chip select for the 387. When inactive, it forces NBUSY, PEREQ, NERROR and NRDYO outputs into floating state.
SYSCKEN	5	I	System clock enable is a jumper option. When high it selects internally generated SYSCKOUT for use inside SL9010. When low it selects external input SYSCKIN for use inside the chip.
SYSCKIN	14	I	System Clock In is an external input for system clock.
SYSCKOUT	16	O	System clock out is a free running system clock generated by dividing CPUCLK by 2. It synchronizes itself once to the CPUCLK upon power up during the first CPU cycle.
TIMCLK	7	I	Timer clock input from the clock chip.
VDD	3,28,53,78	-	+5V. Power
VSS	15,40,65,90	-	0V. Ground
WOPT12	74	I	Wait state option 1,2 is a jumper option. When high it allows 1 wait state for 16-bit memory/IO and 4 wait states for 8-bit memory/IO cycles. When low it allows 2 wait states for 16-bit memory/IO and 6 wait states for 8-bit memory/IO cycles.
WTKINT	31	I	WIETEK interrupt is an active high input which asserts IRQ13.
XA0	61	I/O	Peripheral bus address line 0 is a bi-directional pin. It is an output for CPU, refresh and external master cycles and an input for DMA cycles.
XA1	57	I	Peripheral bus address line 1 is an input used in generating NENLO & NENHI. It may be tied low for 386SX based systems.

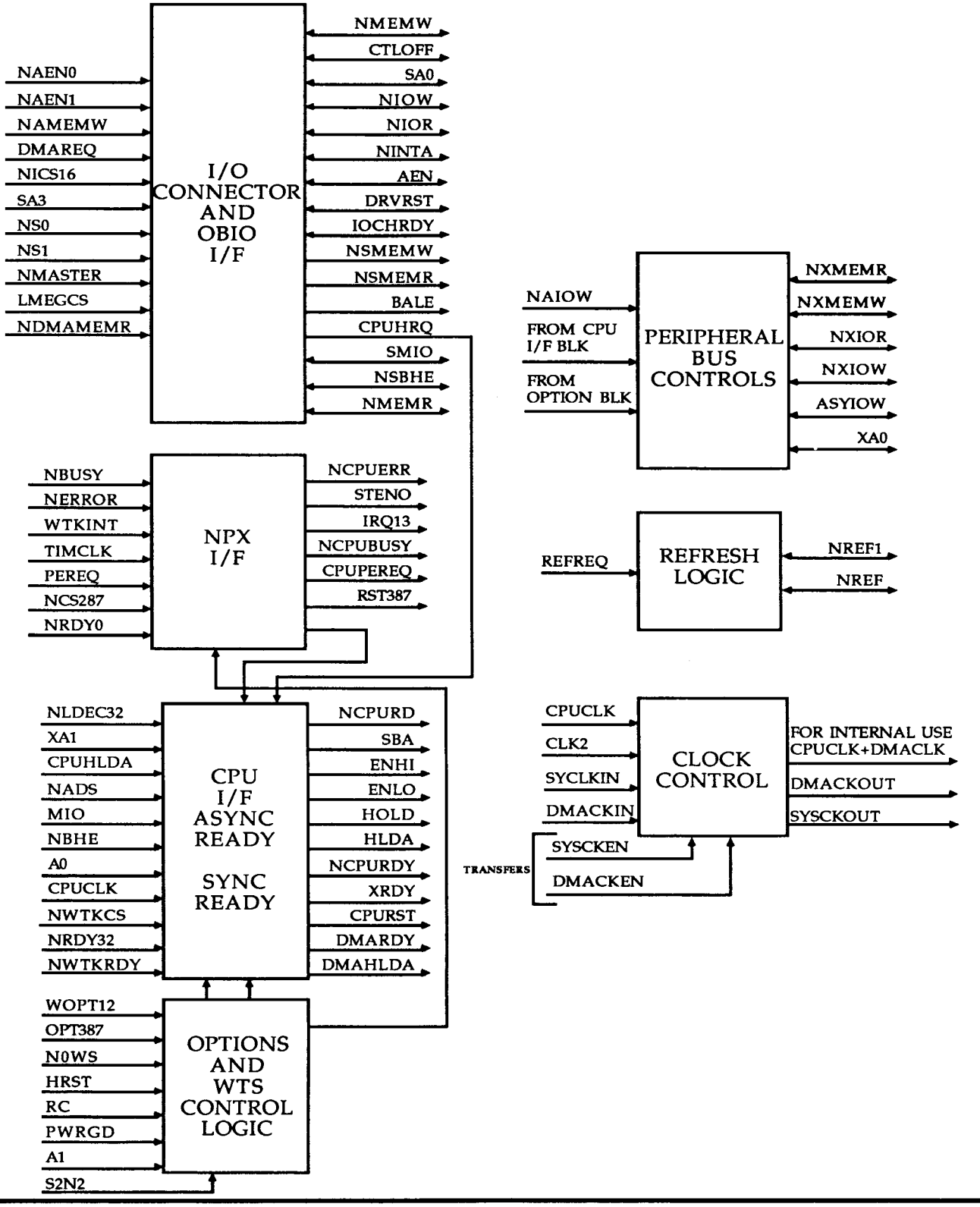
DC CHARACTERISTICS SL9010

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state*
Output High Voltage for Normal Output (IOL = 3.2 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 3.2 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	0.7VDD		V	
Input Low Voltage for CMOS Input	VIL	0.3VDD		V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD

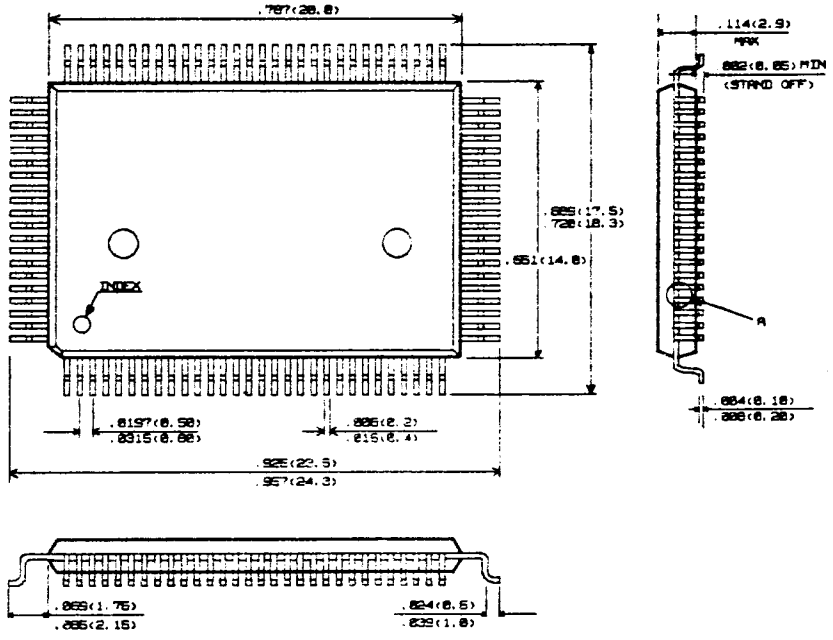
NOTES:
* VIH = VDD, VIL = Vss

BLOCK DIAGRAM

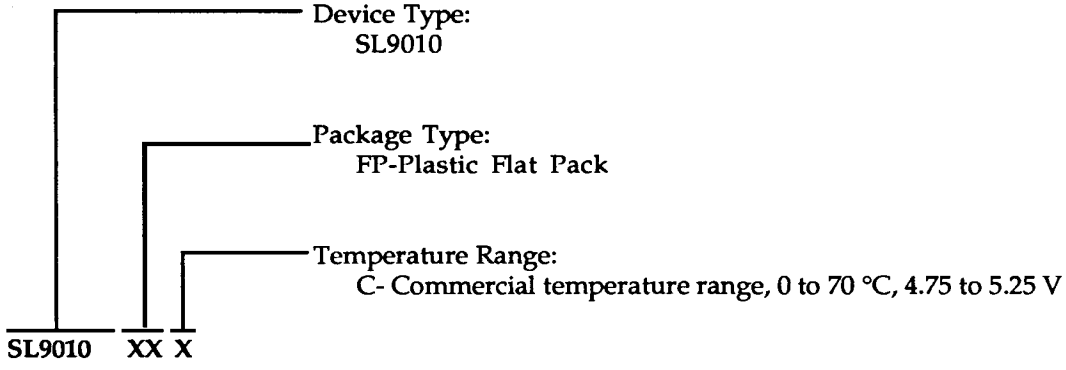


Package Information

100 Pin Plastic Flat Pack



ORDERING INFORMATION



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