# MONOGRAPHICS CONTROLLER

# SL7001

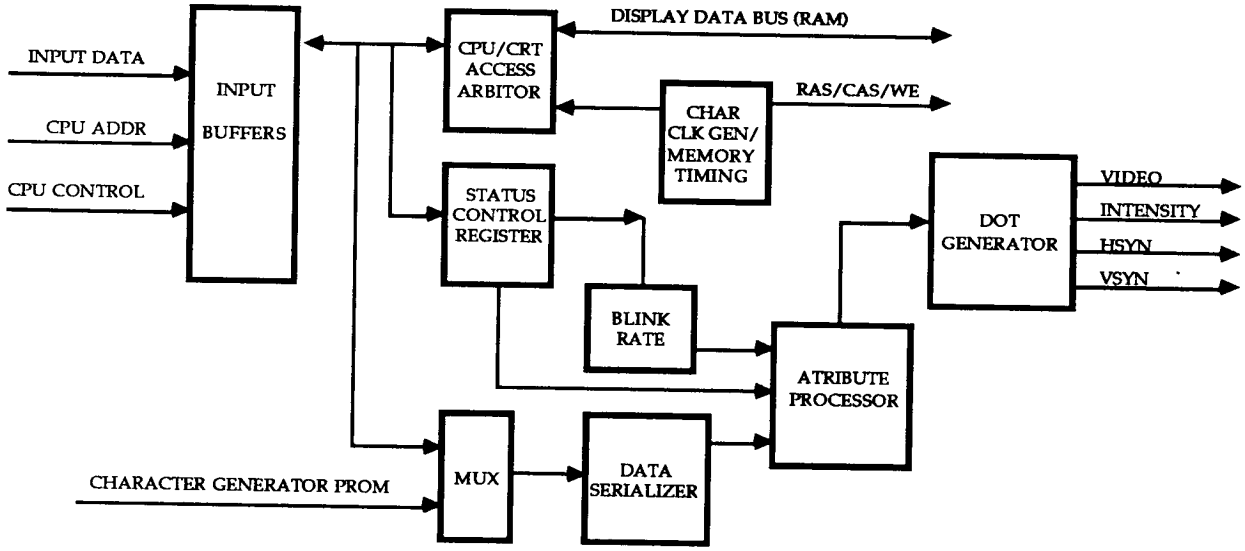
PRELIMINARY

005148

## FEATURES

- 100% Compatible with HERCULES Monochrome
- High Resolution: 720 X 350
- 100% Compatible with IBM MONO-TEXT Adaptor
- Runs Software Packages as LOTUS 1-2-3, SYMPHONY, FRAMEWORK and Others
- Bit-Map Graphics
- Ideal For Low Cost Graphics and Schematic Entry
- Implemented in High Speed, Low Power CMOS
- Available Now, in 84 PLCC

## FUNCTIONAL BLOCK DIAGRAM
## SL7001

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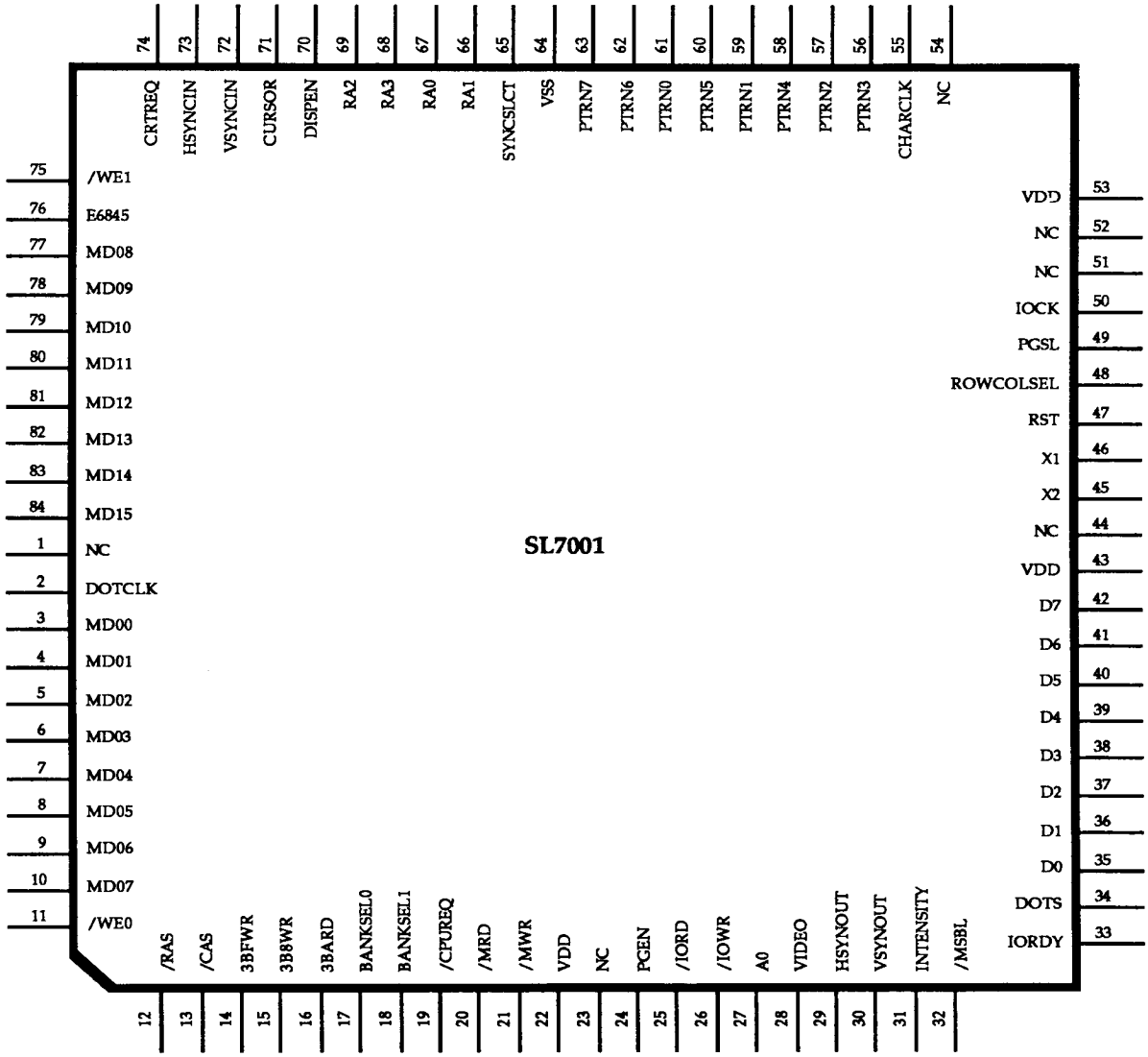


## PIN DESCRIPTION SL7001

| PIN | TYPE | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 35 - 42 | I/O | D0-D7 | Data bus signals to/from CPU |
| 3 - 10<br>77 - 84 | I/O | MD00 - MD15 | Display data bus signals from/to the graphic/alphanumeric RAM. In graphic mode the 16 bits are read and serialized for CRT display. In character mode, a character byte and attribute byte are read. |
| 16 | I | 3BARD | A low on this pin will enable the contents of the status register on D0 - D7. |
| 15 | I | 3B8WR | A low to high transition on this Pin will latch the data on the data bus to control register. |
| 47 | I | RST | A high on this pin will reset the logic on the chip. |
| 14 | I | 3BFWR | A low to high transition on this pin will latch the data on Data bus to the latch . |
| 72 | I | VSYNCIN | Vertical Sync Input. The output of a CRT controller (6845) may be connected on this pin. |
| 73 | I | HSYNCIN | Horizontal Sync Input. the horizontal Sync output of a CRT controller(6845) may be connected to this pin. |
| 70 | I | DISPEN | This input when low will disable the video output. |
| 71 | I | CURSOR | This input is used to generate a cursor in alphanumeric mode. This input in combination with UNDL & BLNK attributes of cursor will generate appropriate cursor shape & blink rate. |
| 78 | O | VIDEO | This pin provides the video ouput for the CRT. |
| 30 | O | /VSYNCOUT | This pin provides the vertical synchronization output for the CRT. |
| 24 | O | PGEN | This output selects between the RAM page 0 and RAM page 1. It is software selectable and bit 0 of the register may be loaded to select the required page. |
| 65 | I | SYNCSLCT | Strapping option for reading the status register sync bits. If zero, bit 0 & 7 of the status register will read the horizontal and vertical Sync; else will read dummy VSYNC and HYNC. This input is used to speed up software which waits for sync's before updating display. |
| 67,66,<br>69,68 | I | RA0-3 | In character display mode these inputs are used to determine the scan line address of the character Font, read from the character generator ROM. These inputs may be connected to a CRT controller (6845). |

## SL7001 PIN DESCRIPTION (Cont'd.)

| PIN | TYPE | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 17,18 | O | BANKSEL0, BANKSEL1 | Selects one of the four 8K graphic memory banks. |
| 12 | O | /RAS | Row address strobe signal for the graphic/alpha RAM. |
| 48 | O | ROWCOLSEL | This output signal is low at /RAS time . It changes to high one DOTCLK after RAS is asserted. |
| 46.45 | I | X1,X2 | These inputs may be used to connect a crystal. The crystal frequency should be the same as DOTCLK frequency. |
| 2 | O | DOTCLK | This output pin provides buffered DOT clock for external use. |
| 32 | I | /MSBL | This input may be connected to a valid memory address range decode of the graphic/alpha RAM. |
| 55 | O | CHARCLK | This clock is generated by dot clock. This clock is used as clock input to a CRT controller(6845). In character mode it is a DOTCLK/9. In graphic mode it is DOTCLK/16. |
| 33 | O | IORDY | During CPU access this signal goes low until the CPU access to the RAM is complete. This signal may be used to synchronize the CPU access cycle till the graphic/alpha RAM access is complete. |
| 19 | O | /CPUREQ | This output when Low signifies that a CPU access for the graphic/ alpha RAM is in progress. It may be used for enabling CPU address to the RAM. |
| 74 | O | CRTREQ | This output when High, signifies that CRT refesh access cycle is in progress. It may be used to enable the addresses from CRT controller (6845) to the RAM. |
| 13 | O | /CAS | Coulmn address strobe output. It may be connected to the CAS input of the graphic/alpha RAM. |
| 49 | O | PGSL | Page Select selects one of 32K page for display |
| 20 | I | /MRD | Memory read signal form CPU. |
| 21 | I | /MWR | Memory write signal form CPU |
| 31 | O | INTENSITY | Intensity Output |
| 29 | O | HSYNCOUT | Horizontal Sync Output for the CRT. |
| 11,75 | O | /WE0-1 | Write enables for bank 0 & bank 1. A low on /WE0 or /WE1 will write the data on MD00-07 or MD08-15 into the graphic /alpha RAM respectively. |

## PIN DESCRIPTION SL7001

| PIN | TYPE | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 27 | I | A0 | CPU address 0. |
| 76 | O | E6845 | This signal enables 6845 CRT controller. |
| 50 | I | IOCK | I/O Clock |
| 25 | I | /IORD | I/O read signal from CPU. |
| 26 | I | /IOWR | I/O write signal from CPU. |
| 34 | O | DOTS | Dots for the graphic/alpha. These dots are not processed through the attribute logic on chip. |
| 61,59, 57,56, 58,60, 62,63 | I | PTRN0-7 | PTRN0-7 are the input pattern which will show up on the screen in alpha mode. These inputs may be connected to cahracter pattern generation ROM. |
| 22,43, 53,54 | - | VDD | Power Supply |
| 64 | - | VSS | Ground |
| 51,52, 54 | - | N.C. | Must be pulled-up to VDD |
| 1,44, 23 | - | N.C. | |

## Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | VDD | VSS-0.3 | 6.5 | V |
| Input Voltage | VI | VSS-0.3 | VDD0.3 | V |
| Output Voltage | VO | VSS-0.3 | VDD0.3 | V |
| Operating Temperature | Top | - 20 | 75 | C |
| Storage Temperature | Tstg | - 55 | 150 | C |

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

## Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|
| Supply Voltage | VDD | 4.75 | 5.25 | V |
| Ambient Temperature | TA | 0 | 70 | C |

## DC Characteristics

| Parameter | Symbol | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Input Low Voltage (TTL) | VIL | | 0.8 | V | VDD=4.75V |
| Input High Voltage (TTL) | VIH | 2.2 | | V | VDD=5.25V |
| Input Low Voltage (CMOS) | VIL | | 1.35 | V | VDD=4.5V |
| Input High Voltage (CMOS) | VIH | 3.85 | | V | VDD=5.5V |
| Output Low Voltage | VOL1 | | 0.4 | V | IOL=6mA |
| Output High Voltage | VOH | 2.4 | | V | IOH=-4mA |
| Input Low Current | IIL | | -200 | uA | VI=0.5V, VDD=5.25V |
| Input High Current | IIH | | 20 | uA | VI=2.4V, VDD=5.25V |
| Input Leakage Current | II | | 25 | uA | VI=5.5V, VDD=5.25V |
| Output Leakage Current | IOZ | | 40 | uA | VO=VDD,VSS |
| Output HI-Z Leak Current | IOZ1 | -100 | 100 | uA | 3-State Output Pins |
| Output HI-Z Current | IOZ2 | -300 | 120 | uA | Bidirectional Pins |

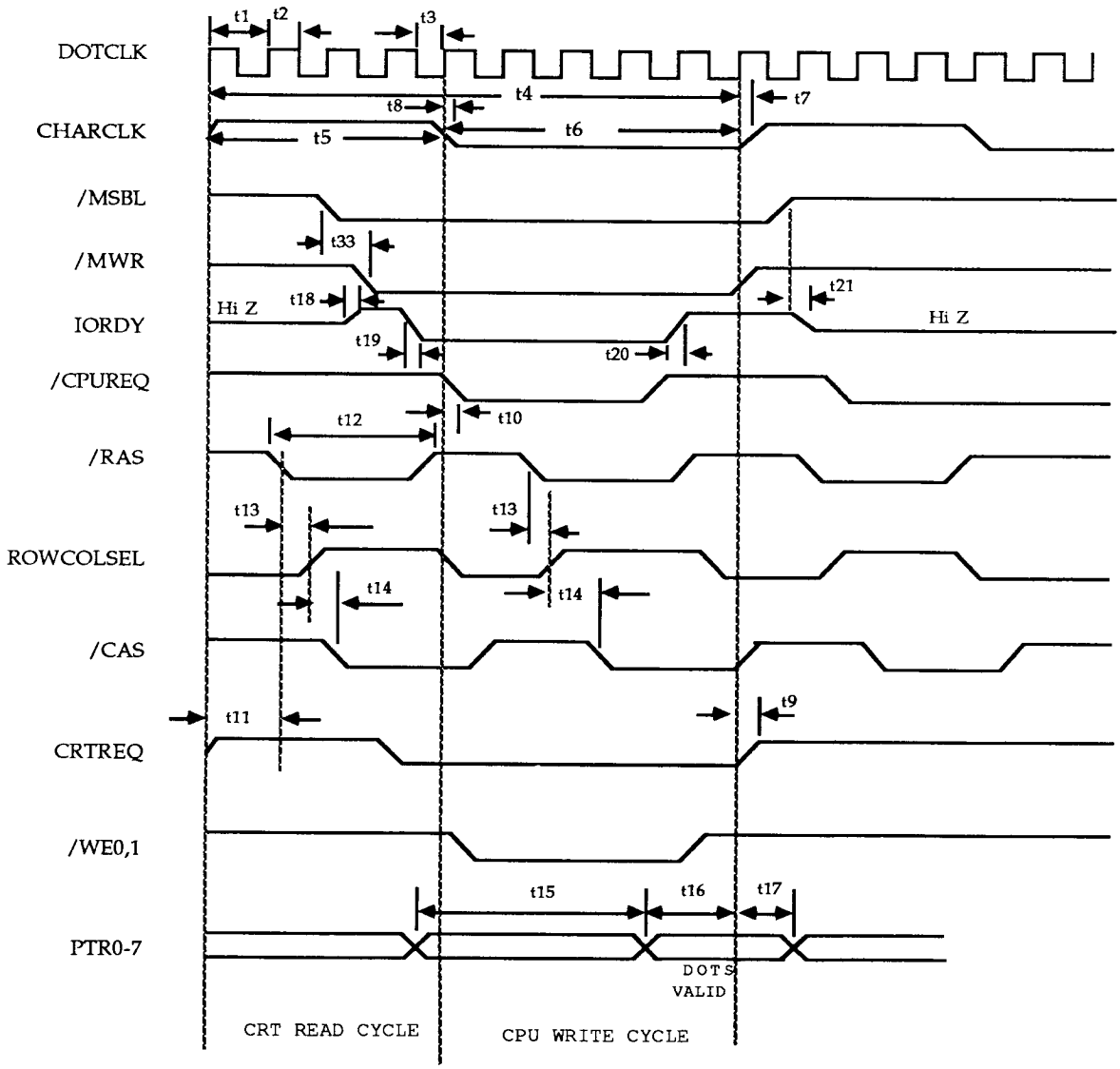
## AC Characteristics SL7001

(TA = 0 ° C to 70 ° C, VDD=5V±5%)

| Sym | Description | Min. | Max. | Units |
|---|---|---|---|---|
| t1 | DOTCLK period for alpha mode | 60 | | ns |
| t2 | DOTCLK high period for alpha mode | 25 | 35 | ns |
| t3 | DOTCLK low period for alpha mode | 25 | 35 | ns |
| t4 | CHARCLK clock for alpha mode | 9t1 | | - |
| t5 | CHARCLK high period for alpha mode | 4t1 | | - |
| t6 | CHARCLK low period for alpha mode | 5t1 | | - |
| t7 | DOTCLK high to CHARCLK high | 10 | | ns |
| t8 | DOTCLK high to CHARCLK low | 10 | | ns |
| t9 | DOTCLK high to CRTREQ high | 10 | | ns |
| t10 | DOTCLK high to CPUREQ low | 5 | | ns |
| t11 | CRTREQ high to /RAS low | t1-8 | | ns |
| t12 | /RAS pulse width | 2.5t1 | | - |
| t13 | /RAS low to ROWCOLSEL high | t2+5 | | ns |
| t14 | ROWCOLSEL high to /CAS low | t2+5 | | ns |
| t15 | Character PROM access time | 4t1 | | - |
| t16 | Data set-up time for PTRN | 10 | | ns |
| t17 | Data hold time for PTRN | 10 | | ns |
| t18 | /MSBL active to IORDY high | 10 | | ns |
| t19 | /MRD active to IORDY low | 10 | | ns |
| t20 | /CPUREQ inactive to IORDY high | 5 | | ns |
| t21 | /MSBL inactive to IORDY tri-state | 10 | | ns |
| t22 | Write command pulse width | 25 | | ns |
| t23 | Write data hold time after command is active | 10 | | ns |
| t24 | Read command pulse width | 25 | | ns |
| t25 | Read command active to data valid | 10 | | ns |
| t26 | Read command inactive to data invalid | 10 | | ns |
| t27 | DOTCLK period for graphic mode | 60 | | ns |
| t28 | DOTCLK high period for graphic mode | 25 | 35 | ns |
| t29 | DOTCLK low period for graphic mode | 25 | 35 | ns |
| t30 | CHARCLK for graphics mode | 16t1 | | - |
| t31 | Graphic data load clock high time | 8t1 | | - |
| t32 | Graphic data load clock low time | 8t1 | | - |
| t33 | MSBL to MWR set-up time | 10 | | ns |

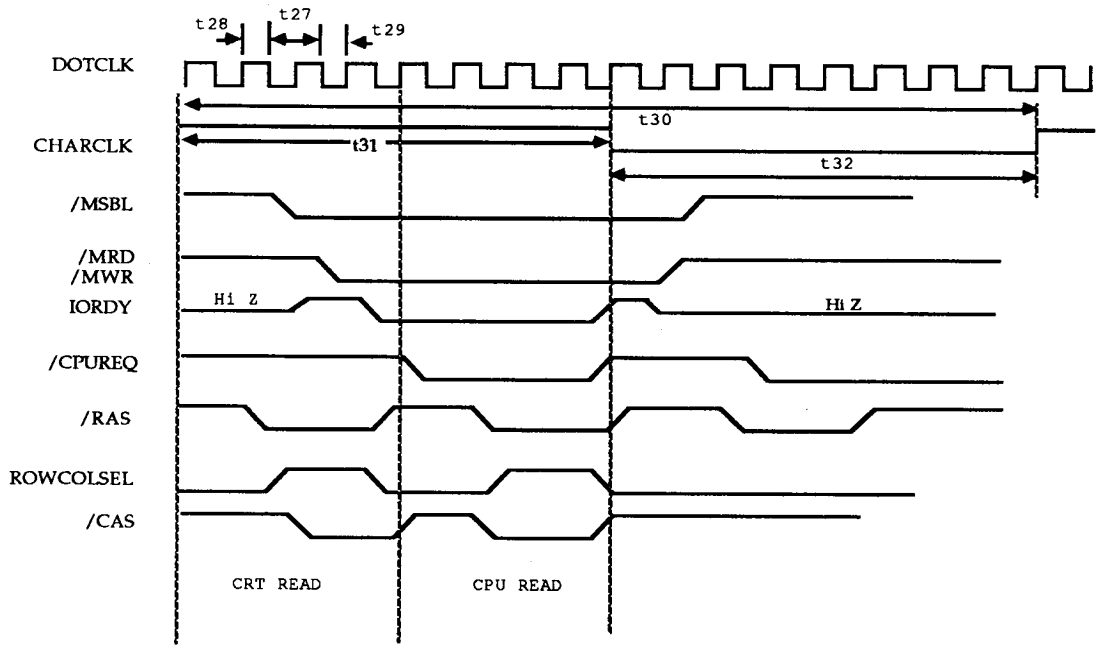
## AC TIMING DIAGRAMS SL7001

Alpha Numeric Mode



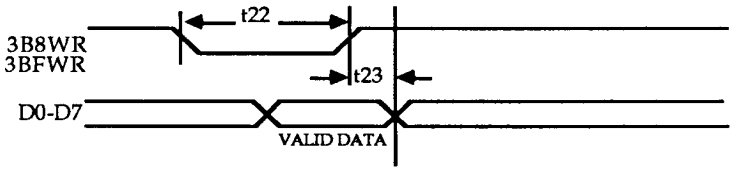
## AC TIMING DIAGRAMS SL7001 (Cont'd.)

Graphics Mode

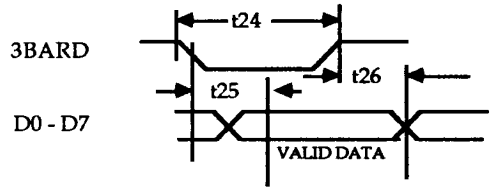


## AC TIMING DIAGRAMS SL7001 (Cont'd.)

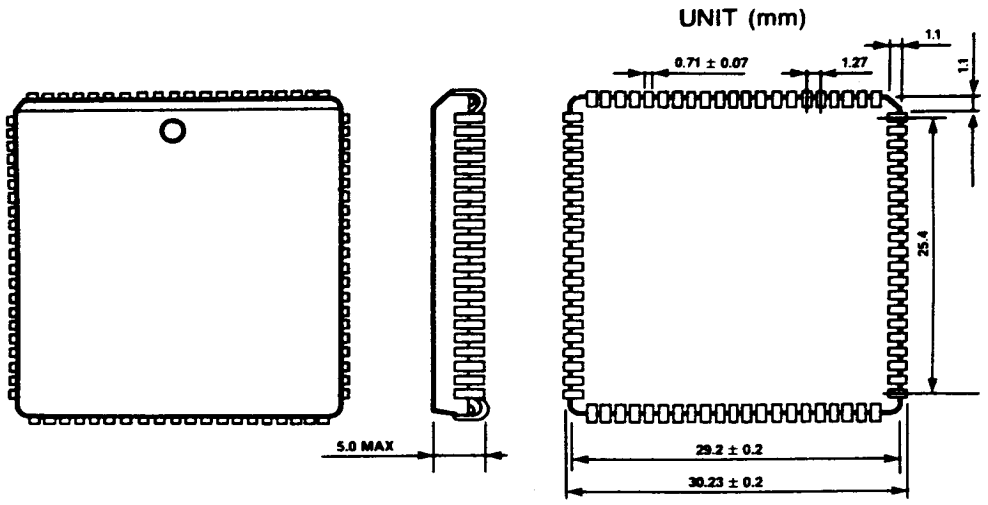
REGISTER WRITE TIMING



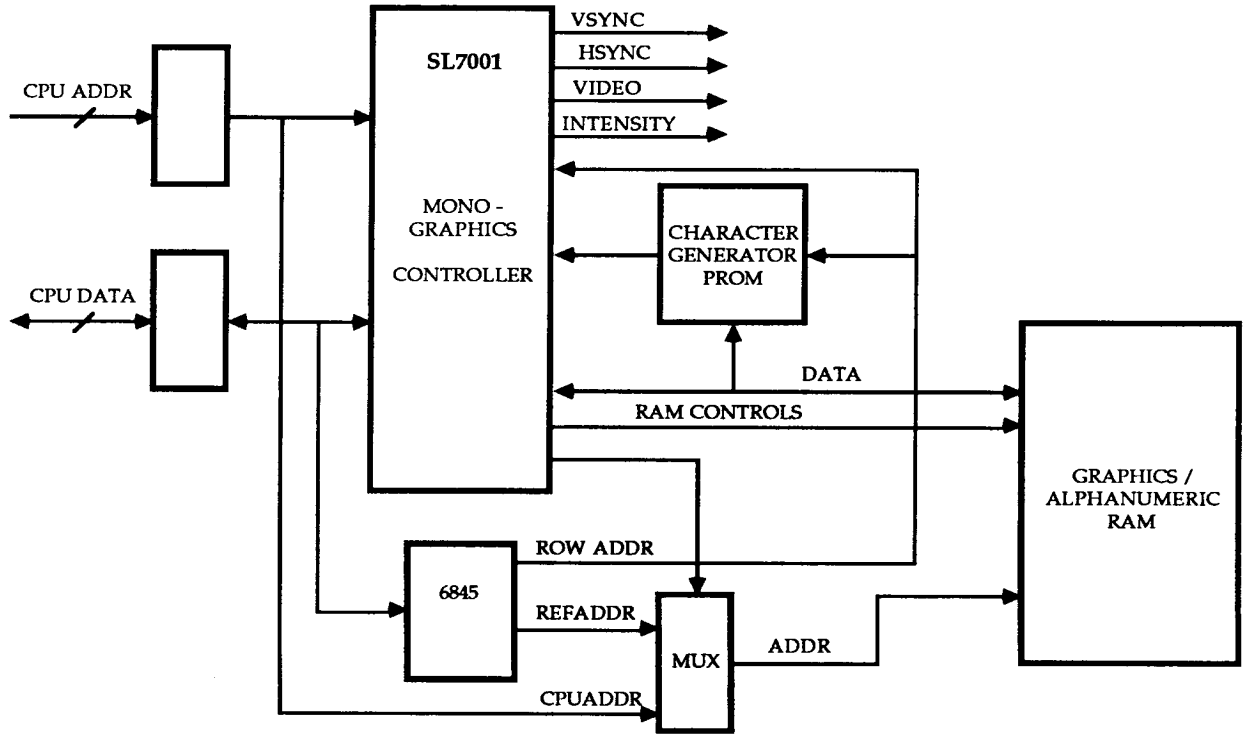

REGISTER READ TIMING



## Package information



## SYSTEM APPLICATION

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