MEMORY MAPPER FOR PC-AT

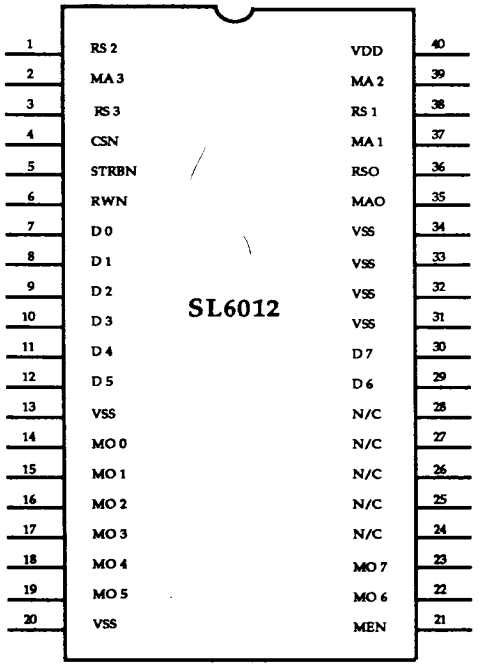
SL6012

PRELIMINARY

FEATURES

- **Expands 4 Address Lines to 8 Address Lines**
- **Designed for PC / AT Paged Memory Mapping**
- **3-State Map Outputs**
- **High Speed Low Power CMOS**
- **Pin-to-Pin replacement for 74LS612 on PC / AT designs**

PIN OUT



DESCRIPTION

The SL6012 Memory Mapper is intended for use in PC-AT design. It can expand an address bus by 4 bits. In PC-AT applications, 4 bits of the source address are used to select 1 of 16, eight bit map registers. These registers are normally programmed (through software) with the starting address of each memory page. The register data is output directly for use as the most significant bits of the expanded address bus. The 8 bits from the SL6012 are used along with the unused source address bits to form the expanded address bus.

As shown in Table 1, the SL6012 has three modes of operation; read, write and map. Data may be written into, or read from the Memory Mapper when chip select CSN is low. The register select inputs (RS0 through RS3) select one of the sixteen map registers. When RWN is low, data is written into a register from the data bus. When RWN is high data is output from a Memory Mapper register to the data bus.

The map mode of operation is selected when chip select CSN is high. In this mode, the register data selected by the map address inputs (MA0 through MA3) will be available on the map outputs (MO0 through MO7). Note that the map registers are addressed by either the RS inputs or the MA inputs depending upon the operating mode. When MEN (Map Enable) is low the map outputs (MO0-MO7) are active. When MEN is high, the map outputs are at high impedance.

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PIN DESCRIPTION

SYMBOL	PIN	TYPE	DESCRIPTION
D0 - D7	7-12, 29 - 30	I/O	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0 - RS3 when CSN is low. Mode controlled by RWN.
RS0 - RS3	1,3,36,38	I	Register select inputs for I/O operations.
RWN	6	I	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
STRBN	5	I	Strobe input used to enter data into the selected map register during I/O operations. Minimum pulse width =75nS.
CSN	4	I	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
MA0 - MA3	2,35,37,39	I	Map address inputs to select one of 16 map registers when in map mode (CSN is high).
MO0 - MO7	14 - 19,22 ,23	O	Map outputs present the map register contents to the system memory address bus in the map mode.
MEN	21	I	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
NC	24 - 28		No connect.
VDD	40		5- V power supply.
VSS	13,20,31 - 34		Ground.

FUNCTIONAL DIAGRAM

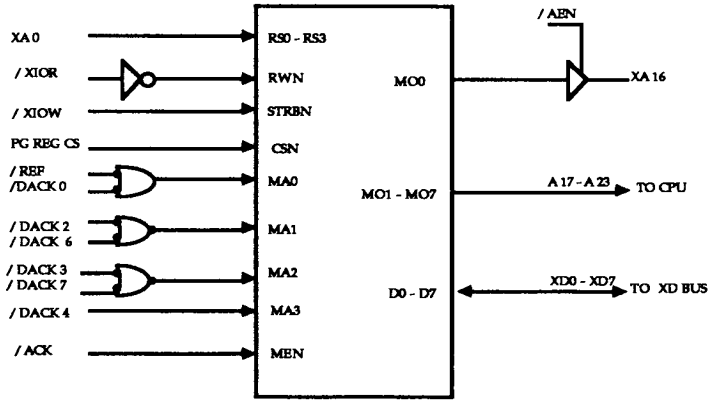


TABLE 1.

CSN	RWN	MODE
0	0	Write to register selected by RSx inputs.
0	1	Read from register selected RSx inputs.
1	X	Output on MOx the register selected by MAx inputs

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	VDD		7.0	V
Input Voltage	VI	- 0.5	5.5	V
Output Voltage	VO	- 0.5	5.5	V
Operating Temperature	Top	- 25	85	C
Storage Temperature	Tstg	- 40	125	C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

DC CHARACTERISTICS

(TA = 0° C to 70° C, VDD = 5V ± 5%)

Parameter	Symbol	Min.	Max.	Units	Conditions
High-level input voltage	VIH	2		V	
Low-level input voltage	VIL		0.8	V	
High-level output voltage / current	VOH	2.4		V	VDD=MIN, VIH=2V, VI =0.8 V / IOH= 4mA
Low - level output voltage / current	VOL		0.4	V	VDD=MIN, VIH=2V, VOL=0.8V, IOL=8mA
Off-state output current, high-level voltage applied	IOZH		20	µA	VDD=MAX, VIH=2V, VIL=0.8V VO = 2.7V
Off-state output current, low - level voltage applied	IOZL		- 20	µA	VDD=MAX, VIH=2V, VIL=0.8V VO = 0.4V
High-level input current	IIH	- 20	20	µA	VDD=MAX, VI=2.7V to VDD
Low-level input current	IIL		-25	µA	VDD = MAX, VI = 0.4V
Short circuit output current	IOS	-30	-130	mA	VDD = MAX (Note)
Supply current	IDD		20	mA	VDD = MAX

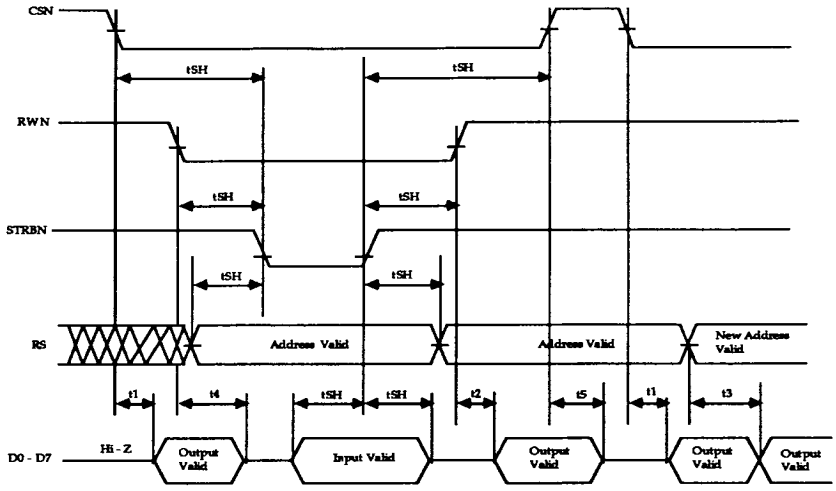
Note: Not more than one output should be shorted at a time, and duration of the short - circuit should not exceed one second.

AC CHARACTERISTICS

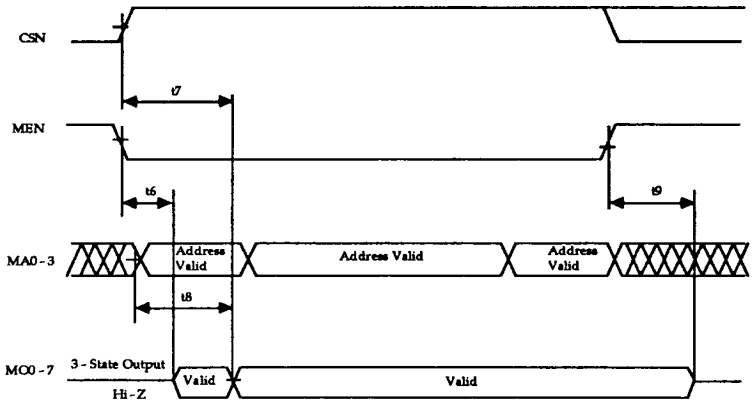
(TA = 0° C to 70° C, VDD = 5V ± 5%)

Symbol	Description	Min.	Max.	Units
t1	CSN LOW to Data bus Access (enable) time		50	ns
t2	RWN HIGH to Data bus (D0 - D7) Access (enable) time		35	ns
t3	RS to Data bus (D0 - D7) access time		75	ns
t4	RWN LOW to Data bus (D0 - D7) disable time		50	ns
t5	CSN HIGH to Data bus (D0 - D7) disable time		65	ns
t6	MEN LOW to Map outputs (MO0 - MO7) Access (enable) time		30	ns
t7	CSN HIGH to Map outputs (MO0 - MO7) Access time		50	ns
t8	MA to Map outputs (MO0 - MO7) Access time		70	ns
t9	MEN HIGH to Map outputs (MO0 - MO7) disable time		25	ns
tSH	SETUP and HOLD times recommended (see Waveforms)	20	—	ns

WRITE AND READ MODES



MAP MODE



ORDERING INFORMATION

Device Type:

Package Type:
PD - Plastic DIP

Temperature Range:
C - Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

SL6012 XX X

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