ADDRESS & DATA BUS BUFFERS
SL6003, SL6004, SL6005

PC / AT COMPATIBLE CHIP-SET

PRELIMINARY

The SL6003 provides address latches and control buffers for the PC / AT system. Control signals from the SL6001 are buffered by the SL6003 and tri-stated for the expansion and the I/O buses. This device also provides the system status and control ports. The SL6003 has been implemented in bipolar technology and is available in a 68-pin PLCC package.

The SL6004 buffers the lower address lines of the expansion bus, I/O bus and memory bus. In addition to buffering memory addresses, the SL6004 provides the row/column multiplexing and refresh signals for up to 1 meg DRAMS. The SL6004 has been implemented in bipolar technology and is available in a 68-pin PLCC package.

The SL6005 has been designed to provide logic to transfer 16-Bit data of the 80286 to and from 8-Bit devices. The device also provides low/high byte translation latches, data buffers, parity generation and error checking for the PC / AT. The SL6005 has been implemented in bipolar technology and is available in a 68-pin PLCC package.

Functional Description SL6003

Figure 1 illustrates a block diagram of the SL6003. As shown in the figure, the SL6003 provides drivers and buffers for the CPU, System and Local I/O control buses. The memory read, write and the I/O read write signals are bidirectional. The direction and control of the bus is determined by the /DMAEN and the /MASTER inputs. The chip also provides the buffer and drive capability for the high address bus signals, A17-A23. The direction and control is provided by the CPU Hold Acknowledge and ALE inputs. The SL6003 includes status latches that can be written into and read through /PORTWR and /PORTRD signals.

SL6003 Pin Description

Symbol	Pin	Type	Description
AEN	43	O	Address ENable is an output signal for the expansion bus. When LOW it indicates that another master on the expansion bus has made a request by activating /MASTER.
ALE	48	I	Address Latch Enable from the SL6001, used to latch the address bus signals.
A20GATE	22	I	When A20 GATE is LOW, A20 on the CPU address bus is forced LOW. When A20GATE is HIGH, A20 is transmitted as generated by the CPU.
A23-A17	24-30	I/O	CPU Address bits 17 through 23. As input these pins are forced by the CPU address bus. As outputs A17- A23 are output on these pins.
BALE	44	O	Buffered ALE signal for the devices on the expansion bus. SA0-SA19 are latched on the falling edge of BALE. During DMA cycles, BALE is forced high by CPUHLDA going HIGH.
/BHE	21	I	Bus High Enable signal is connected to /BHE output of the CPU. It indicates the transfer of data on the upper half of the data bus. In conjunction with the A0 polarity it determines whether the access is on a word or byte boundary. The coding of BHE and A0 follows the 80286 coding scheme.

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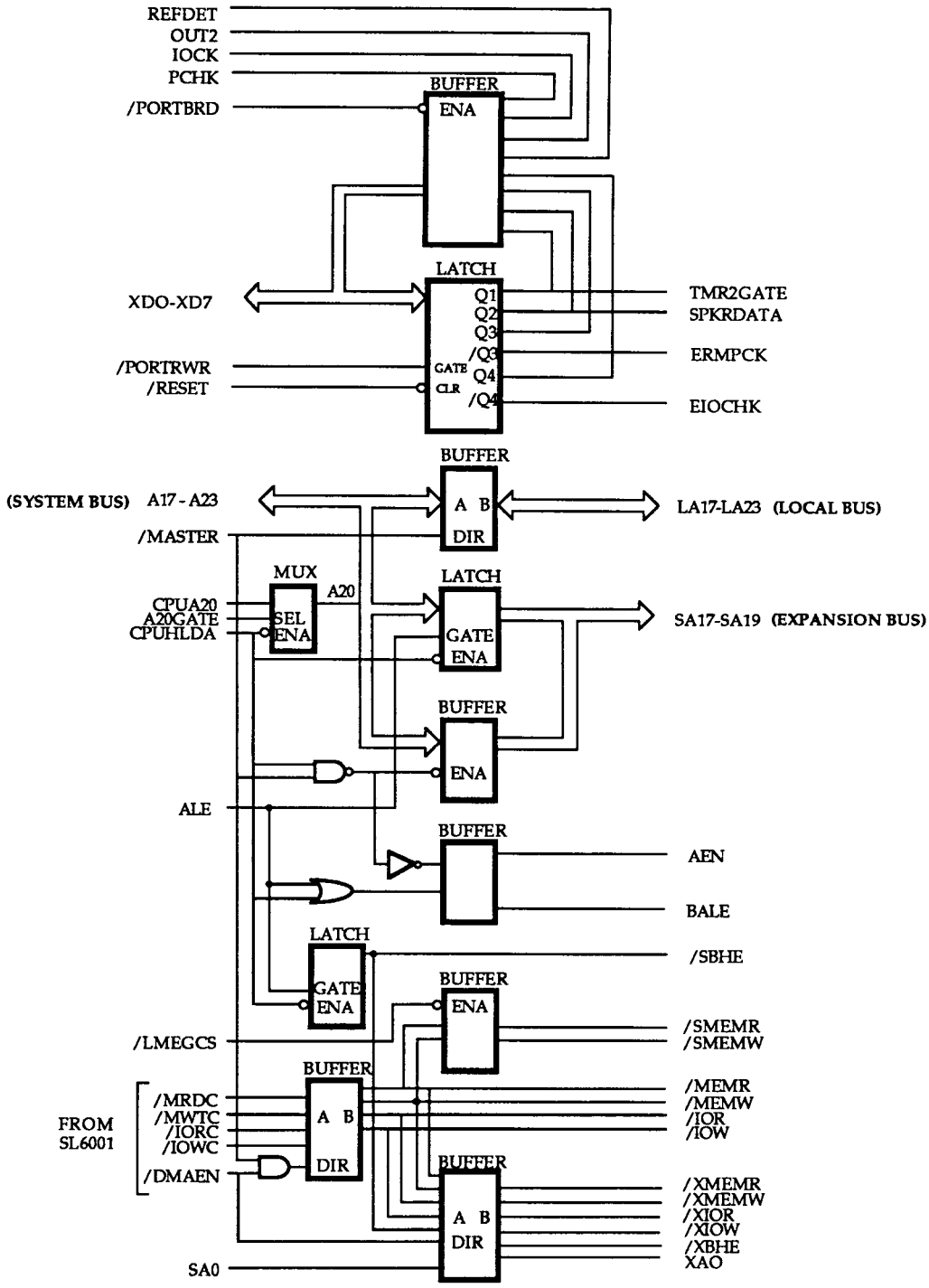


Figure 1. Functional Block Diagram SL6003

Pin Description SL6003 (Cont'd.)

Symbol	Pin	Type	Description
CPUA20	23	I	CPUA20 transmitted as A20 after being conditioned by the A20GATE signal.
CPUHLDA	45	I	CPU HoLD Acknowledge signal is used to control the direction of the address and control signal transceivers. A HIGH on the CPUHLDA is interpreted as a DMA cycle.
/DMAEN	31	I	DMA Address ENable is used to condition the transceivers for the peripheral control signals. (MEMR, MEMW, IOR, IOW, XA0) to be output on the system control bus.
EIOCHK	57	O	Enable I/O CHecK output is used to enable the I/O Check (/IOC) from the I/O expansion bus to be latched into SL6001.
ERMPCK	58	O	Enable RaM Parity ChecK allows the SL6001 to latch the parity error and output as PCHK signal for the SL6003.
IOCK	54	I/O	I/O Channel ChecK from SL6001 is sampled by PORT B Read Command.
/IOR	6	I/O	Expansion bus Input/Output Read command. The read cycle can be initiated by the CPU or DMA controller, or by a DMA controller resident on the I/O channel.
/IORC	14	I/O	I/O Read signal generated by the CPU through the SL6001.
/IOWC	15	I/O	I/O Write signal generated by the CPU through the SL6001.
/IOW	7	I/O	Expansion bus Input/Output Write command. The write cycle can be initiated by the CPU or DMA controller, or by a DMA controller resident on the I/O channel.
LA23-17	36-42	I/O	Local address bus LA17-23 is controlled by the /MASTER signal. When /MASTER is HIGH the system bus forces the A17-A23 addresses on the Local bus. When /MASTER is LOW the system bus forces the addresses on the expansion bus. LA17 -LA23 gives the system up to 16 Mbytes of addressability. LA17-LA19 are valid when bus ALE signal BALE, is high. LA17-LA19 are not latched during CPU cycles and do not stay valid for the entire cycle. They are used to generate memory decodes for 1 wait-state memory cycles. The I/O add-on adapter boards must latch these signals on the falling edge of BALE signal.
/LMEGCS	47	I	Low MEGabyte Chip Select is generated by SL6002. When active, it indicates that low megabyte memory address space is being accessed.
/MASTER	46	I	Master is generated by the devices on the expansion bus. A LOW indicates that another device on the expansion bus is active. After /MASTER is forced low by an I/O device, the I/O CPU must wait for one system clock period before forcing the address and data lines. The /MASTER signal must not be held low for more than 15 microseconds, or else data in the system memory may be lost due to lack of a refresh cycle.

Pin Description SL6003 (Cont'd.)

Symbol	Pin	Type	Description
/MEMR	4	I/O	Extended expansion bus, MEMory Read, command active on all memory read cycles.
/MEMW	5	I/O	Extended expansion bus, MEMory Write, command active on all memory write cycles.
/MRDC	12	I/O	Memory ReaD signal generated by the CPU through SL6001.
/MWTC	13	I/O	Memory WriTe signal generated by the CPU through SL6001 .
OUT2	55	I	OUT2 is the output from the Timer 8254, sampled by a PORT B Read Command.
PCHK	53	I	Parity CHecK from SL6001 is sampled by PORT B Read command.
/PORTBRD	50	I	Port B ReaD is active when the CPU reads PORT B latch, to store the status conditions.
/PORTBWR	51	I	Port B WRite is active when the CPU outputs the data to the PORT B latch.
REFDET	56	I	REFresh DETect is generated by the SL6001, sampled by a PORT B read command.
/RESET	49	I	Active Low Signal used to reset the Port B latch.
SA0	8	I/O	Address 0 of the CPU bus. The I/O pin outputs the A0 from the CPU during local CPU cycles. The expansion bus can force the A0 on this pin during the period when another master on the expansion bus has the control.
SA17-19	32-34	O	Expansion bus addresses SA17-19 are output from the system bus during a memory or an I/O cycle.
/SBHE	10	I/O	Bus High Enable signal from or to the Expansion Bus is active when the high byte transfer is taking place.
/SMEMR	2	O	Expansion bus MEMory Read Command, active when low 1 megabyte memory space is addressed.
/SMEMW	3	O	Expansion bus MEMory Write Command, active when low 1 megabyte memory space is addressed.
SPKRDATA	59	O	SPeaKeR DATA output is used to allow the 8254 tone signal to be output to the speaker.
TMR2GATE	60	O	TiMeR 2 GATEs signal enables the timer on 8254 Timer to generate the tone signal for the speaker.
VDD	18,52	-	Power Supply.
VSS	1,35	-	Ground.
XA0	9	I/O	Address 0 from the local I/O bus. In DMA cycle the XA0 is forced by the DMA controller. During CPU read cycle the XA0 is forced by the CPU.
/XBHE	11	I/O	Bus High Enable to or from the peripheral bus is active when high byte transfer is taking place.
XD0-XD3	68-65	I/O	Bidirectional peripheral data bits 0 - 3 are used as inputs to PORT B Latch and outputs from PORT B status buffer.
XD4-XD7	64-61	O	Outputs only from PORT B status buffer.

Pin Description SL6003 (Cont'd.)

Symbol	Pin	Type	Description
/XIOR	19	I/O	I/O Read signal for the peripheral bus. As an output, it is used to read the internal registers of the peripheral controllers. As an input, it is forced by the DMA controller to access data from a peripheral device.
/XIOW	20	I/O	I/O Write signal for the peripheral bus. As an output it is used to write to the internal registers of the peripheral controllers. As an input it is forced by the DMA controller to write data to a peripheral device.
/XMEMR	16	I/O	MEMory Read signal from and to the peripheral bus. The Read is forced by the CPU during read of the peripheral devices. The DMA controller forces this pin as input to read data from a memory location or memory to memory transfer.
/XMEMW	17	I/O	MEMory Write signal from and to the peripheral bus. The Write is forced (as an output) by the CPU during write to the peripheral devices. The DMA controller forces this pin as input to write data to a memory location or memory to memory transfer.

Absolute Maximum Ratings SL6003, SL6004, SL6005

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	VDD	-	7.0	V
Input Voltage	VI	-0.5	5.5	V
Output Voltage	VO	-0.5	5.5	V
Operating Temperature	Top	-25	85	C
Storage Temperature	Tstg	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the Operating Conditions.

DC Characteristics SL6003, SL6004, SL6005

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Parameters	Symbol	Min.	Max.	Units	Conditions
Input Low Voltage	VIL		0.8	V	
Input High Voltage	VIH	2.0		V	
Output Low Voltage	VOL1		0.5	V	IOL=10 mA (Note 1)
Output Low Voltage	VOL2		0.5	V	IOL=24mA (Note 2)
Output High Voltage	VOH	2.4		V	IOH=3.3mA (Note 3)
Input Low Current	IIL		-200	uA	VI=0.5V, VDD=5.25V
Input High Current	IIH		20	uA	VI=2.4V, VDD=5.25V
Input High Current	II		200	uA	VI=5.5V, VDD=5.25V
Output Short Circuit Current	IOS	-15	-100	mA	VO=0V
Input Clamp Voltage	VIC		-1.5	V	II=-18mA, VDD=4.75V
Power Supply Current	IDD	140	230	mA	SL6003
	IDD	170	285	mA	SL6004
	IDD	180	300	mA	SL6005
Output HI-Z Leak Current	IOZ1	-100	100	uA	3-State Output Pins
Output HI-Z Current	IOZ2	-300	120	uA	Bidirectional Pins

NOTES

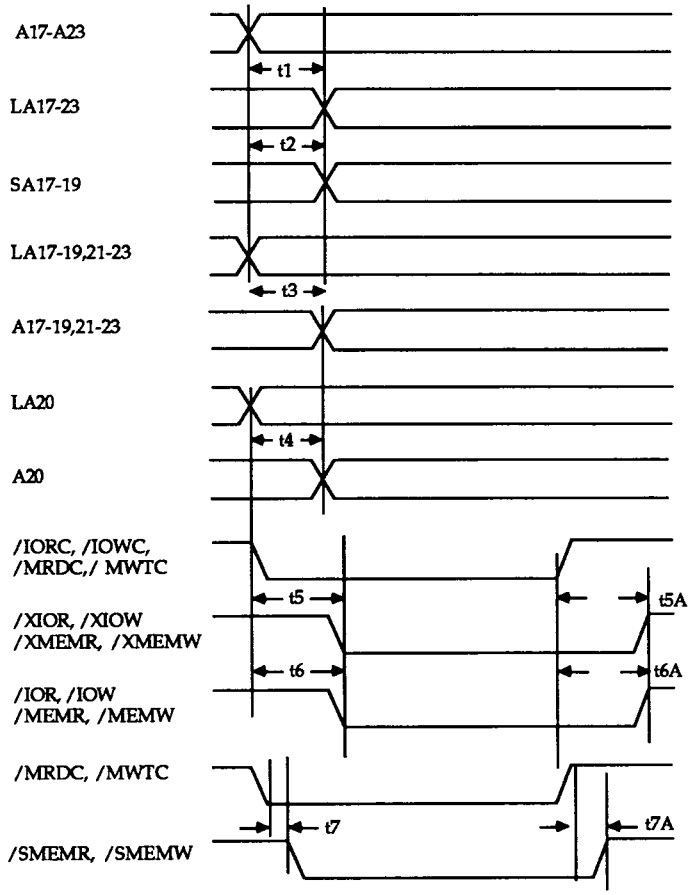
1. All non-system and non-extended system bus outputs only.
2. All system bus and extended system bus outputs, LA17-19, SA17-19, BALE, /SMEMR, /SMEMW, /SBHE, /MEMR, /MEMW, /IOR, /IOW, AEN and SA0 of SL6003; SA0 - SA16 of SL6004; and SD0 - SD15 of SL6005 have IOL = 24 mA @ VOL = 0.5V.
3. All outputs and bidirectional pins.

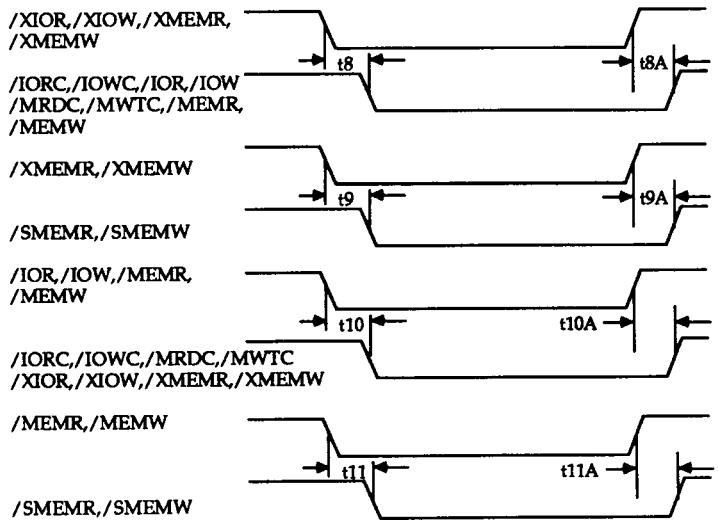
AC CHARACTERISTICS SL6003

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

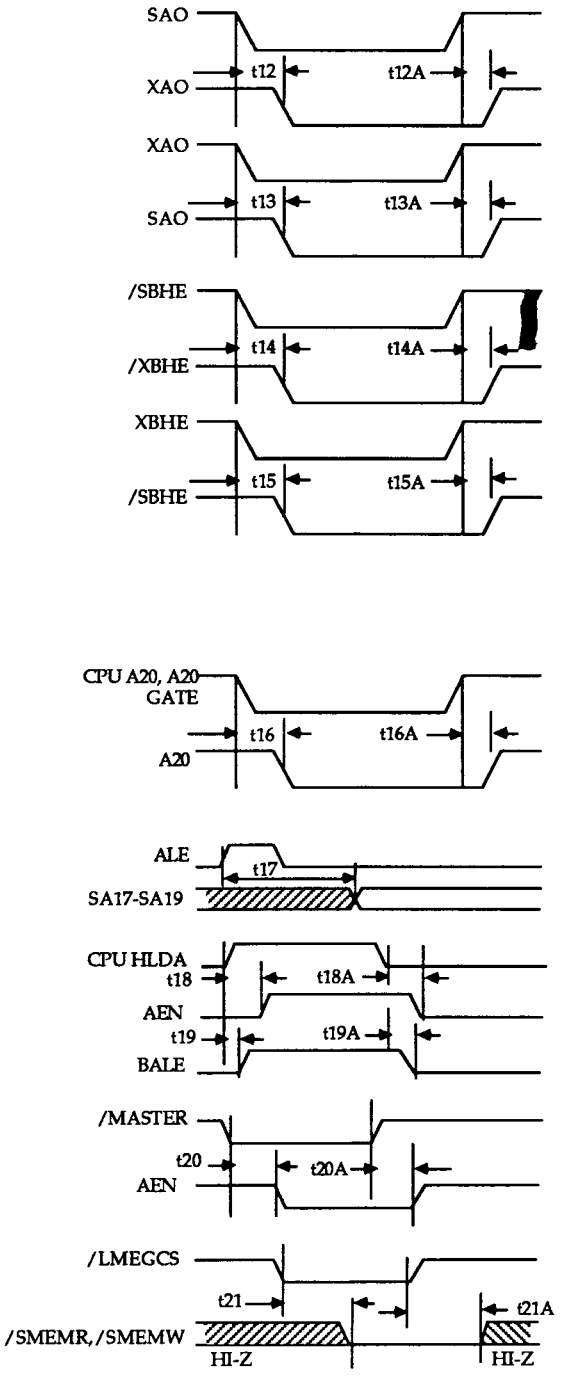
Symbol	Description	Min.	Max.	Units
t1	A Bus to L Bus Address Delay	4	19	ns
t2	A Bus to S Bus Address Delay	4	19	ns
t3	L Bus to A Bus Address Delay	4	19	ns
t4	L Bus A20 to A Bus A20 Delay	4	22	ns
t5	CPU Control to Local I/O Control Delay (H-L)	5	22	ns
t5A	CPU Control to Local I/O Control Delay (L-H)	5	20	ns
t6	CPU Control to Extended System I/O Control Delay (H-L)	5	24	ns
t6A	CPU Control to Extended System I/O Control Delay (L-H)	5	20	ns
t7	CPU /MEMR, /MEMW, to System /SMEMR, /SMEMW Delay (H-L)	5	22	ns
t7A	CPU /MEMR, /MEMW, to System /SMEMR, /SMEMW Delay (L-H)	5	20	ns
t8	Local I/O CTRL to CPU, System I/O CTRL Delay (H-L)	5	22	ns
t8A	Local I/O CTRL to CPU, System I/O CTRL Delay (L-H)	5	22	ns
t9	Local I/O /XMEMR, /XMEMW, to /SMEMR, /SMEMW Delay (H-L)	4	21	ns
t9A	Local I/O /XMEMR, /XMEMW, to /SMEMR, /SMEMW Delay (L-H)	4	17	ns
t10	Expansion I/O CTRL to CPU, Local I/O CTRL Delay(H-L)	5	22	ns
t10A	Expansion I/O CTRL to CPU, Local I/O CTRL Delay (L-H)	5	20	ns
t11	Extended System /MEMR, /MEMW to /SMEMR, /SMEMW Delay (H-L)	5	22	ns
t11A	Extended System /MEMR, /MEMW to /SMEMR, /SMEMW Delay (L-H)	5	20	ns
t12	System SA0 to Local I/O A0 Delay (H-L)	3	15	ns
t12A	System SA0 to Local I/O A0 Delay (L-H)	4	19	ns
t13	Local I/O XA0 to System SA0 Delay (H-L)	3	15	ns
t13A	Local I/O XA0 to System SA0 Delay (L-H)	3	17	ns
t14	System SBHE to Local XBHE Delay (H-L)	5	21	ns
t14A	System SBHE to Local XBHE Delay (L-H)	5	24	ns
t15	Local I/O XBHE to System SBHE Delay (H-L)	5	21	ns
t15A	Local I/O XBHE to System SBHE Delay (L-H)	5	21	ns
t16	CPU Address A20, A20GATE to A20 Delay (H-L)	5	19	ns
t16A	CPU Address A20, A20GATE to A20 Delay (L-H)	5	19	ns
t17	**ALE to System Address SA17-19 Valid Delay**	**5**	**21**	**ns**
t18	CPUHLDA to AEN Delay (H-L)	5	21	ns
t18A	CPUHLDA to AEN Delay (L-H)	5	23	ns
t19	CPUHLDA to BALE Delay (H-L)	4	19	ns
t19A	CPUHLDA to BALE Delay (L-H)	4	19	ns
t20	System /MASTER to AEN Delay (H-L)	5	23	ns
t20A	System /MASTER to AEN Delay (L-H)	5	21	ns
t21	Low Memory /LMEGCS Active to /SMEMR, /SMEMW Valid	5	22	ns
t21A	Low Memory /LMEGCS In-Active to /SMEMR, /SMEMW HI-Z	5	19	ns

AC TIMING DIAGRAMS SL6003





AC TIMING DIAGRAMS SL6003



Functional Description SL6004

Figure 2 illustrates a block diagram of the SL6004. The chip provides buffering and the drive for the address signals A1-A16 as well as the drivers for the memory address bus MA0-MA7. The direction and control for the Address buffers for A1-A16 are provided by the CPU Hold Acknowledge and /DMAEN inputs. The refresh addresses are provided by a 9 bit refresh counter, which is enabled by the /REFEN input. The addresses for the memory are multiplexed as shown in the figure. The SA0 output is active only during the refresh cycle.

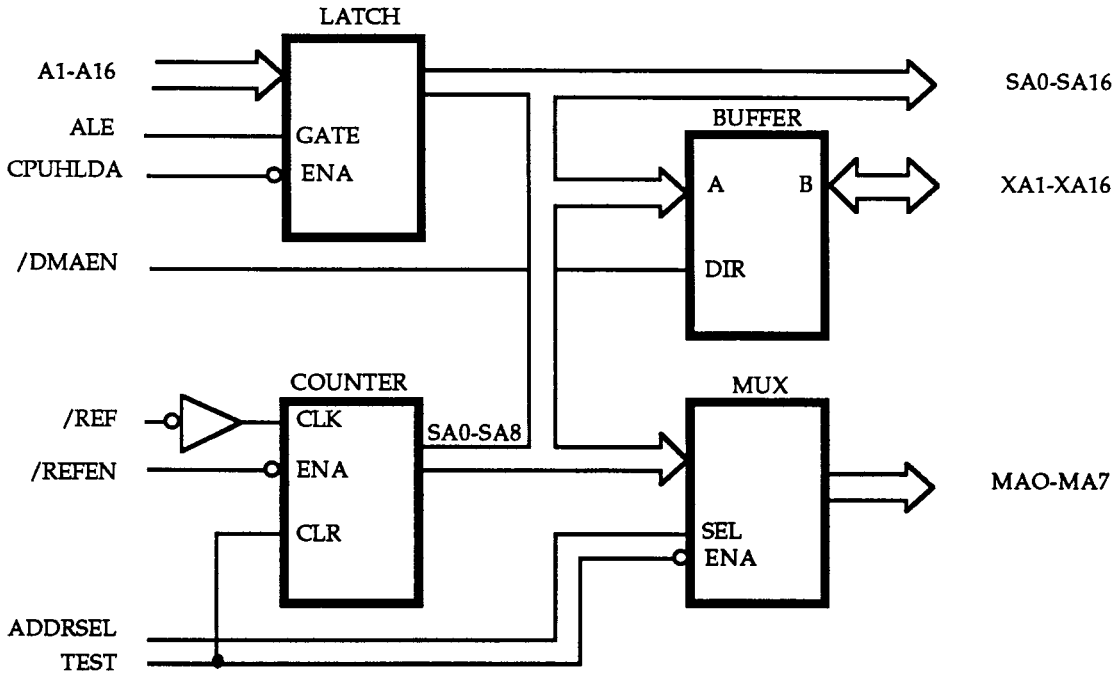


Figure 2. Functional Block Diagram SL6004

Pin Description SL6004

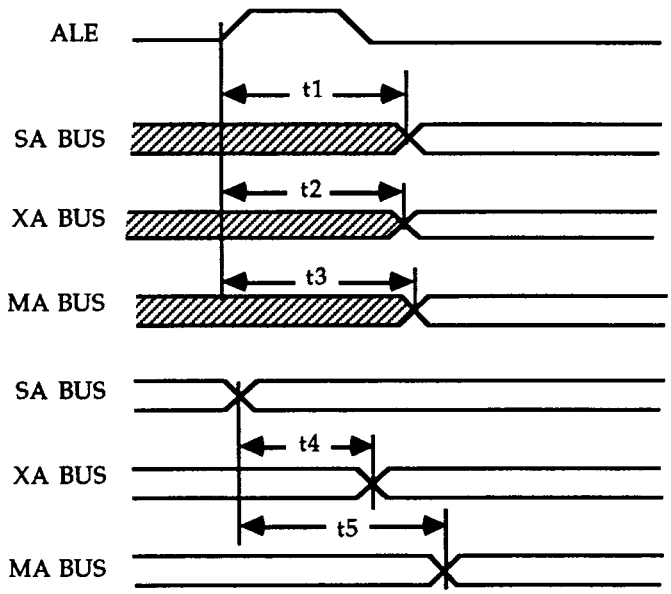
Symbol	Pin	Type	Description
A1-A13	5-17	I	CPU address signals 1-16.
A14-A16	19-21	I	
ADDRSEL	46	I	ADDress SELect multiplexes the memory address between the system addresses and the addresses generated by the refresh counter.
ALE	22	I	Address Latch Enable from the SL6001.
CPUHLDA	25	I	CPU Hold Acknowledge is generated by the CPU in response to a Hold Request from a DMA controller. The SL6004 is used to tri-state the SA bus, allowing the XA bus to drive the address bus.
/DMAEN	45	I	DMA ENable is generated by the SL6001 when a DMA cycle is underway. It is used by the SL6004 to condition the address transceiver in the proper direction.
MA0-MA4	64-68	O	Address signals 0-7 for addressing the memory.
MA5-MA7	2-4	O	
/REF	23	I	REFresh is generated by the SL6001 to initiate a refresh cycle for the DRAMs.
/REFEN	44	I	REFresh ENable is generated by the SL6001 and allows a refresh cycle to be initiated.
SA0	26	O	Address 0 for the refresh memory.
SA1-8	27-34	I/O	Expansion bus addresss bits 1-16 .
SA9-16	36-43	I/O	
TEST (RESET)	24	I	Test, when HIGH, resets the refresh counter and tri-states the memory addresses MA0-7. This will allow another device to access the memory. In normal operation the TEST pin must be pulled LOW.
VDD	18,52	-	Power Supply.
VSS	1,35	-	Ground.
XA1-5	47-51	I/O	Peripheral addresses 1-16 for the local I/O bus.
XA6-16	53-63	I/O	

AC Characteristics SL6004

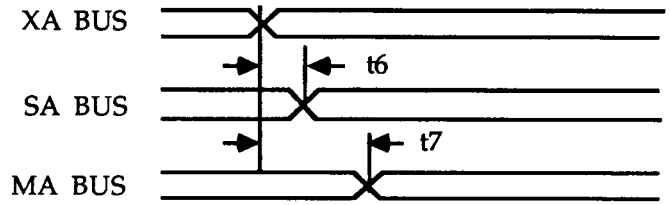
(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

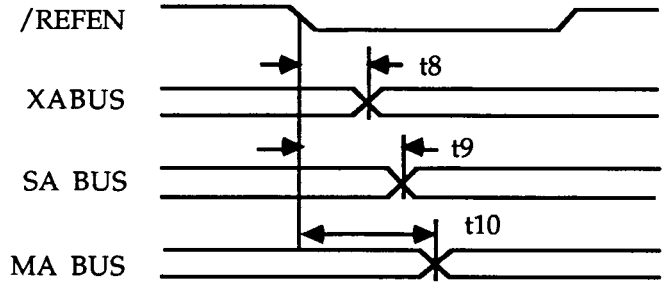
Symbol	Description	Min.	Max.	Units
t1	ALE to System Address Bus Delay	8	30	ns
t2	**ALE to Local I/O Address Bus Delay (XA Bus)**	**8**	**25**	**ns**
t3	**ALE to Memory Address Bus Delay**	**8**	**30**	**ns**
t4	System Address Bus to Local I/O Address Bus Delay (XA Bus)	5	25	ns
t5	System Address Bus to Memory Address Bus Delay	5	29	ns
t6	Local I/O Bus to System Address Bus Delay	6	29	ns
t7	Local I/O Bus to Memory Address Bus Delay	6	29	ns
t8	/REFEN Active to Local I/O Address Bus Valid Delay	8	34	ns
t9	/REFEN Active to System Address Bus Delay	9	38	ns
t10	/REFEN Active to Memory Address Bus Delay	9	38	ns
t11	/REFEN In-Active to System Address Bus HI-Z Delay	5	23	ns
t12	/REFEN to SA0 Valid Delay	7	27	ns
t13	/REFEN to SA0 HI-Z Delay	5	23	ns
t14	Test Enable to Memory Address Bus Valid Delay	7	28	ns
t15	Test Enable to Memory Address Bus HI-Z Delay	6	25	ns
t16	ADDRSEL to Address Valid	5	27	ns

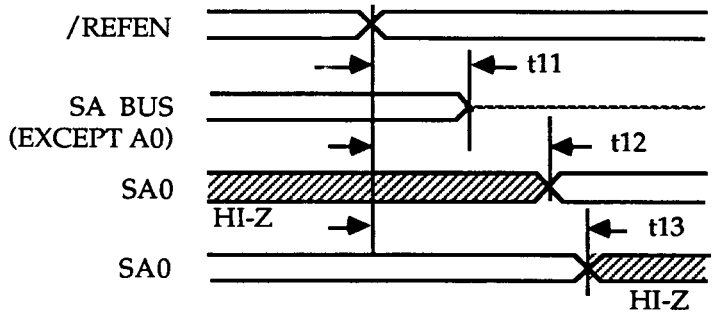
AC TIMING DIAGRAMS SL6004

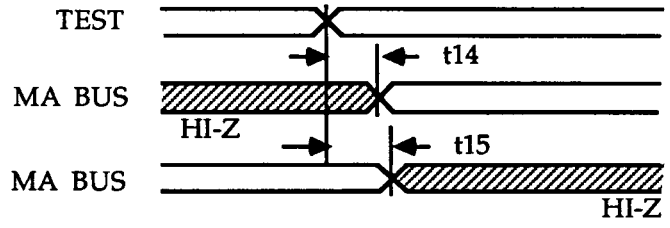


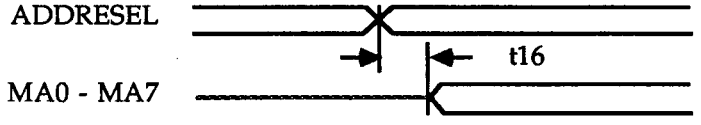
AC TIMING DIAGRAMS SL6004











Functional Description SL6005

Figure 3 illustrates the block diagram of SL6005. The chip provides the data bus buffers and drivers for D0-D15. The data buses: CPU bus (D0-D15), System bus (SD0-SD15), and Memory Data bus (MD0-MD15); are controlled by the DT/R, /DSDEN0, /DSDEN1, /XBHE, AND XA0 inputs. The low byte to high byte conversion logic is also implemented on this chip and is controlled by the /ENHLB and DIRHLB inputs. The chip also includes logic for the parity generation and error checking. The parity is computed on the memory data bus signals and output as MDPIN0 and MDPIN1. During a read cycle, the parity check is completed on the data read from the memory and the parity bits MDPOUT0 and MDPOUT1. On a parity error, the /PAR output is activated.

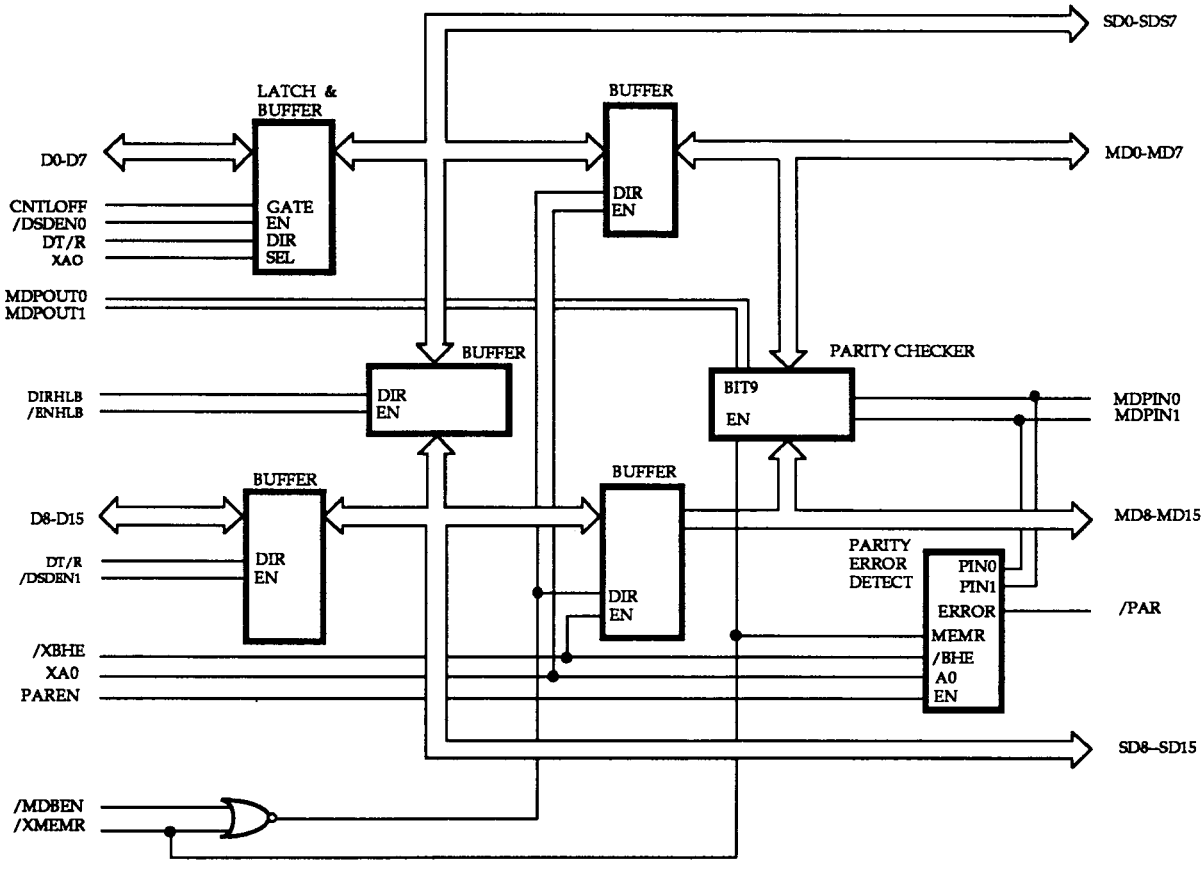


Figure 3. Functional Block Diagram SL6005

Pin Description SL6005

Symbol	Type	Pin	Description
CNTLOFF	I	50	Control Off, generated by the SL6001, is used to enable low byte data bus latch during byte access.
D0-D7 D8-D15	10-17 19-26	I/O I/O	CPU data bus signals from/to the CPU.
DIRHLB	44	I	DIRHLB, generated by SL6001, controls the direction of low to high byte conversion during data transfers to and from 8 bit peripherals.
/DSDEN0 /DSDEN1	46,47	I	Data Strobe Enable 0 and 1, generated by SL6001, enables the data transceivers connected to the LOW and HIGH data bytes.
$\overline{DT/R}$	I	45	Data Transmit/Receive, generated by the SL6001, determines the direction of data to and from memory. HIGH indicates a write cycle and LOW indicates a read cycle.
/ENHLB	54	I	Enable High to Low Byte conversion in conjunction with DIRHLB signal, generated by SL6001.
MD0-7 MD8-15	61-68 2-9	I/O I/O	Memory data bus for the on board memory.
/MDBEN	55	I	Memory Data Bus Enable, generated by SL6002, enables the data bus transceivers connected to the memory devices.
MDPIN0 MDPIN1	60,58	O	Memory Data Parity In 0 and 1 are the parity bits written to the memory banks 0 and 1 during a memory write cycle.
MDPOUT0 MDPOUT1	59,57	I	Memory Data Parity Out 0 and 1 are the parity bits read from the memory banks 0 and 1. They are used to compute the parity during a read cycle.
/PAR	56	O	Parity signal, when low, signifies a parity error on a memory read cycle.
PAREN	53	I	Parity Enable allows the parity check to be done during read from the memory.
SD0-SD7 SD8-SD15	27-34 36-43	I/O I/O	System Data bus for the expansion bus. Its direction is determined by $\overline{DT/R}$ signal from the SL6001.
VDD	18,52	-	Power Supply.
VSS	1,35	-	Ground.
XA0	48	I	Address signal 0 for the peripheral bus, generated by the SL6003, is used to condition the bus transceiver for the memory data bus.
/XBHE	49	I	Bus High Enable, generated by SL6003, is used to condition the bus transceiver for the memory data bus, and is active during a high byte transfer.
/XMEMR	51	I	Memory Read, generated by SL6003, is used to enable the parity generation logic on the device, and to set the direction on the output transceiver for the memory data bus.

AC Characteristics SL6005

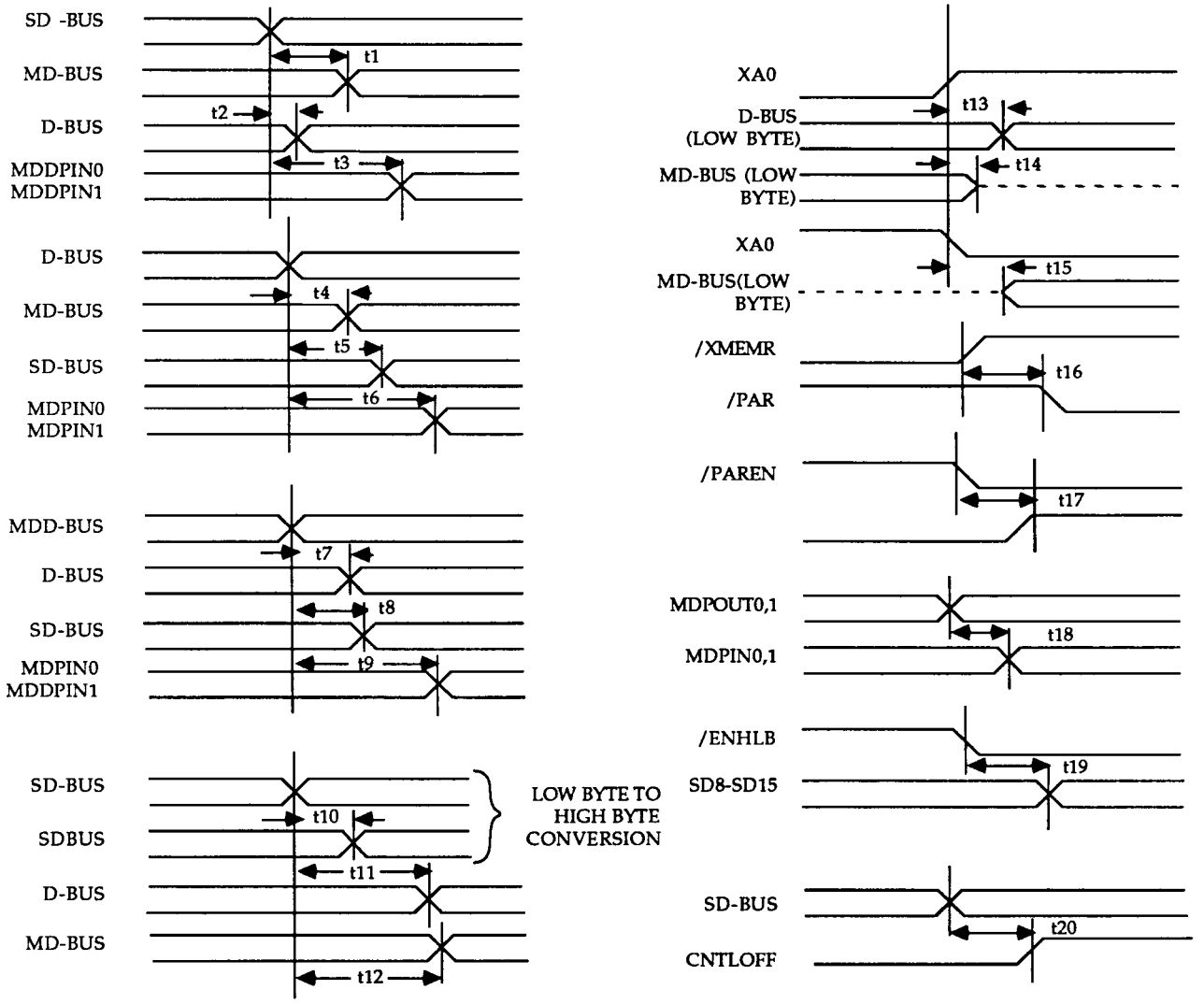
(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Symbol	Description	Min.	Max.	Units
t1	System Data Bus to Memory Bus Delay	8	31	ns
t2	System Data Bus to CPU Data Bus Delay	8	31	ns
t3	System Data Bus to Parity Bits MDPIN0, 1 Output	12	39	ns
t4	CPU Data Bus to Memory Data Bus Delay	8	29	ns
t5	CPU Data Bus to System Data Bus Delay	5	24	ns
t6	CPU Data Bus to Parity Bits MDPIN0, MDPIN1 Output	12	30	ns
t7	**Memory Data Bus to CPU Data Bus Delay**	**6**	**18**	**ns**
t8	Memory Data Bus to System Data Bus Delay	6	27	ns
t9	Memory Data Bus to Parity Bits MDPIN0, 1 Output	10	37	ns
t10	System Data Bus Low Byte to High Byte Conversion	8	32	ns
t11	System Bus to CPU Data Bus Hi-Lo Byte Conversion	10	32	ns
t12	System Bus to Mem Data Bus Hi-Lo Byte Conversion	10	34	ns
t13	XA0 to CPU Data Bus Low Byte Delay	8	29	ns
t14	XA0 to Memory Data Bus HI-Z	6	26	ns
t15	XA0 to Memory Data Bus Address Valid	8	29	ns
t16	/XMEMR Going High to Parity Delay	7	28	ns
t17	/PAREN to Parity Delay	4	19	ns
t18	Parity Input Bits to Parity Output Bits Delay	12	39	ns
t19	/ENHLB to SD8-SD15 Delay	–	29	ns
t20	SD Bus to CNTLOFF setup time	10		ns

Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	CL(pF)	R1(Ω)	RL(Ω)	SW1	SW2
Propagation Delay Time	Totem pole 3-State Bidirectional	tPLH tPHL	50	-	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	tPLH tPHL	50	0.5K	-	ON	OFF
Disable Time	3-state Bidirectional	tPLZ tPHZ	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	tPZL tPZH	50	0.5K	1.0K	ON OFF	ON ON

AC TIMING DIAGRAMS



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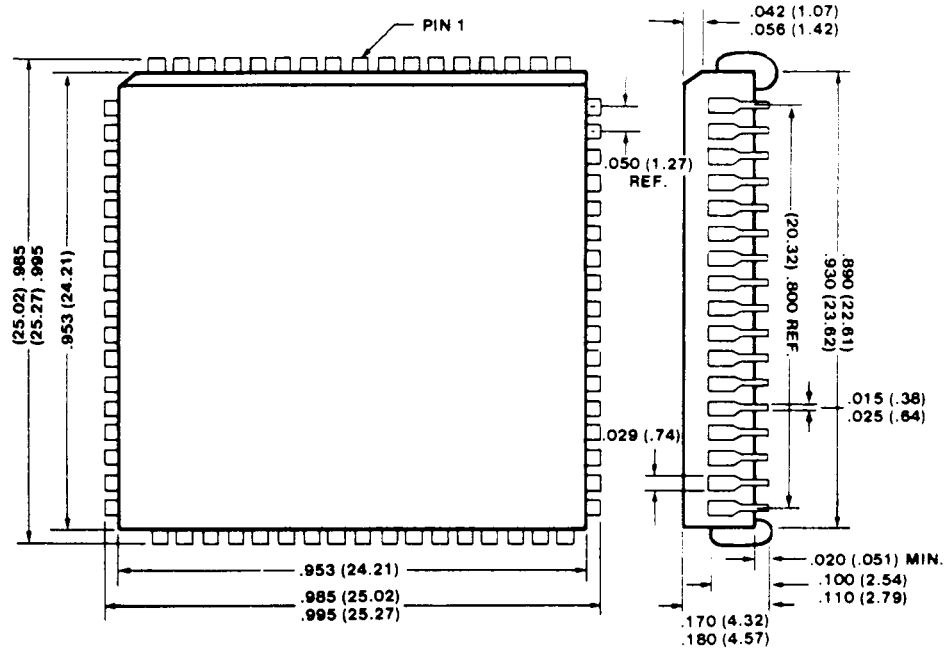
Package Information

68 PIN PLASTIC LEADED CHIP CARRIER



ORDERING INFORMATION

Device Type:
SL6003 -- System Buffer-1
SL6004 -- System Buffer-2
SL6005 -- System Buffer-3

Package Type:
PL- Plastic LCC

Temperature Range:
C- Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

SL600X XX X

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