The SL6001 is used to control the PC /AT system's control system timing, coprocessor interface and NMI detection while the SL6002 decodes RAM/ROM accesses, parity checking and I/O decode logic. The SL6001 generates signals used throughout the system for control timing. All bus cycles are timed and decoded by this device. The SL6001 has been implemented in CMOS technology and offered in an 84 pin plastic PLCC package.

The SL6002 is used for ROM addressing as well as provide RAS/CAS enables for the system RAM. The Real Time Clock and system control/status port is also controlled by the SL6002. The SL6002 has been implemented in CMOS technology and is available in a 48 pin dual in-line plastic package.

FUNCTIONAL DESCRIPTION SL6001

The various functional blocks contained within the SL6001 as shown in figure 1 are discussed below:

Clock Generation and Reset/Ready Synchronization

Two oscillators are contained in the Clock Generation circuitry. Both oscillators use an external crystal, in parallel, to generate the base operating frequency. X1 and X2 are the crystal connections for the CPU Clock Oscillator. X11 and X12 are the crystal connections for the Video Clock Oscillator. A consideration, for the CPU Clock; the crystal oscillator frequency should be twice the operating frequency of the CPU (e.g., 20MHz crystal for a 10MHz CPU). A consideration for the Video Clock; the crystal oscillator frequency should be 14.31818MHz to maintain IBM PC/AT compatibility. The recommended circuit is shown in figure 2. Notice the additional trimmer capacitor, in the video clock oscillator, that can be adjusted to eliminate unwanted color shifts in video signals.

The Video Clock oscillator generates two clock signals. The signal, OSC, is buffered for the system bus expansion connectors and the signal OSC/12 is used by the counter timer. Note: the signal, OSC, should be externally buffered to prevent overloading. The signal, OSC/12, is generated by dividing the 14.31818 oscillator frequency by twelve.

The CPU Clock oscillator generates the remaining four clock signals. The PROCCLCK, SYSCLK, DMACLK and PCLK signals determine how fast the computer operates.

The PROCCLK signal's frequency is equal to the CPU clock oscillator and it drives the CPU and math co-processor. PROCCLK is properly buffered to meet the clock input requirements of the 80286 CPU and 80287 Math coprocessor without external buffering. The 80286 and 80287 requirements are 3.08 volts minimum, V_{IH}.

The signal, SYSCLK, is 1/2 the frequency of PROCCLK while DMACLK is 1/4 the frequency. SYSCLK and DMACLK are synchronized to the CPU's internal clock upon a system reset. After a reset, SYSCLK and DMACLK are held low until after the CPU asserts Status (S1=0) at the beginning of the first cycle. SYSCLK and DMACLK will make a positive transition on the falling edge of PROCCLK, in Phase 1 of the next CPU bus cycle following T_S. This relationship is illustrated in SL6001 timing diagrams.

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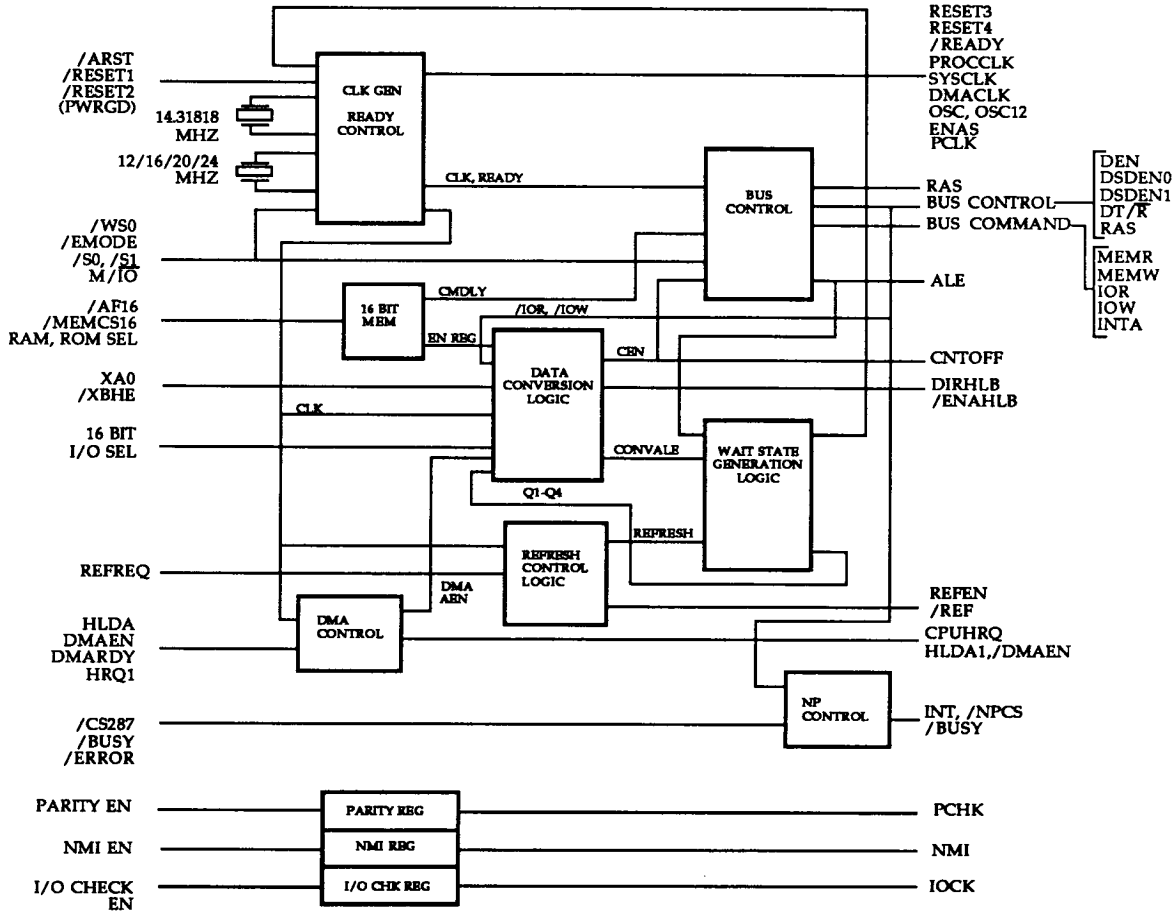

Figure 1. Functional Block Diagram SL6001

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The signal, PCLK, also has a frequency that is 1/2 the frequency of PROCCLK. PCLK has no phase relationship to the CPU's internal clock. /ARST is a separate reset line which clears the PCLK signal.

The SL6001 provides two reset signals. Both signals, RESET4 and RESET3, are active high signals and are derived from /RESET1. RESET3 is the CPU reset signal and can also be used as a general system reset. Additionally, if a shutdown condition is detected by the CPU, RESET3 is asserted for 16 cycles of PROCCLK and then deasserted. In this case, RESET3 is synchronous with PROCCLK, ensuring proper CPU operation. RESET4 is a synchronous reset signal for general system reset. RESET3 and RESET4 meet the setup and hold times of the 80286.

The input signal, /RESET1, is intended as the Power Good input for the system. /RESET1 is internally buffered with a Schmitt trigger, has a typical input hystersis of 1 volt and may be connected to a RC network to generate the proper power-on-reset. /RESET1 should be low when power is applied to the system. It should remain low for a minimum 5 msec after all voltages have stabalized and PROCCLK has reached the specified DC and AC parameters.

The CPU may also be reset by the /RESET2 input. A specific keystroke combination, when detected by the keyboard processor, will activate /RESET2. When activated, RESET3, the CPU reset signal, is asserted and will remain asserted for 16 cycles of PROCCLK after /RESET2 is deasserted.

The address strobe enable signal for the Clock/Calendar, /ENAS, is generated by SL6001. To prevent spurious writes to the Clock/Calendar during power up/down conditions, /ENAS is deasserted when /RESET1 is active. /ENAS is asserted after the CPU starts its first status cycle.

The SL6001 generates a signal, /READY, to allow the CPU to operate with slower devices such as memories and peripherals. /READY is synchronous with PROCCLK output. /READY may be asserted by asserting the input, /WSO. /WSO must be externally synchronized for proper operation. For further information on control of /READY, refer to sections "Wait State" and "Conversion Logic". The output /READY signal is an open drain output. An external pull-up resistor, greater than 900Ω but less than 1000Ω, to VDD should be used to ensure proper rise and fall times.

Conversion Logic

16 bit transfers to and from 8 bit peripheral I/O or memory devices are supported by the Conversion Logic Section of the SL6001. When necessary, the Conversion Logic signals the Wait State Control Logic to place the CPU in a wait state by deasserting /READY. The conversion is performed by controlling the LSA LSA0 and Cross-over Control output signals, DIRHLB and /ENHLB. Once first byte has been transferred, the currently active control signal is interrupted while the states of LSA0 and cross-over Buffer Control Signals are changed. Control is then re-enabled.

Wait State Control

The Wait State Control logic matches the speed of various I/O and memory devices to the speed of the CPU. When necessary, wait states are inserted in the CPU bus cycle by deasserting the /READY

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Table 1. Bus Cycle Status Definition

M/IO	/S1	/SO	Type of Bus Cycle
0	0	0	Interrupt acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
X	1	1	None; idle
1	0	0	Halt shutdown
1	0	1	Memory read
1	1	0	Memory write

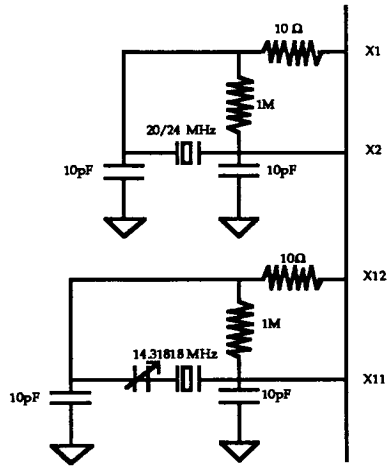

Figure 2. Recommended Oscillator Circuit

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signal generated by the SL6001. As mentioned earlier, /READY is an open drain output. The external pull-up resistor will force /READY high to a not ready condition. The bus cycle will be completed when /READY is reasserted. See figure 3 for an 8 bit and 8/16 bit I/O cycle diagram.

Several defaults have been defined to determine the number of wait states for I/O and memory devices. During memory cycles, defined by asserting /AF16 or /MEMCS16, one wait state is inserted. If the input signal, /WS0, is asserted, no wait states are inserted. During an 8 bit I/O cycle, four wait states are inserted. This can be shortened to two or three wait states by asserting WS2 or WS3. WS2 and WS3 are externally decoded. During a 16 bit I/O cycle, defined by asserting /IOCS16, one wait state is asserted. Four wait states are inserted during an I/O cycle utilizing the expansion bus. This can be extended by asserting IOCHRDY low. Wait states will be inserted until IOCHRDY is deasserted. IOCHRDY should not be held low for more than 2.5µsec.

Command and Control Signal Generation

I/O and Memory control signals are generated in the Command and Control Signal Section. Command signals are /MEMR, /MEMW, /IOR, /IOW, and /INTA. They are decoded by the CPU status signals and indicate the type of bus cycle. The control signals are ALE, DT/$\overline{R}$, DEN, /DSDEN0, /DSDEN1 and RAS. They are also decoded by the CPU status signals and latch the address bus, enable the data buffers and determine the direction of the data flow. The CPU status signals are M/$\overline{IO}$, /S0 and /S1 and are controlled by the 80286 processor. Refer to Table 1 for the CPU status lines and their correspoding type of bus cycle.

There are three bus states in an 80286 internal state machine. The first state is the idle state, (T_i). When the CPU is not in the process of a bus cycle a (T_i) state exists and all command and control signals are inactive. The second state is the status state, (T_S). When either signal, /S0 or /S1, is asserted, a bus cycle is started and a (T_S) state begins. The control signal, ALE, is active during the (T_S) state, and returns low at the end of the (T_S) state. The third state is the command state, (T_C). The command is decoded and appropriate command signal is asserted during the (Tc) state. If an internal Delay condition exists the appropriate command will be asserted one cycle of PROCCLK later than normal. An internal Delay condition exists on all memory cycles, when /AF16 and /MEMCS16 are high, and all I/O cycles (including INTA).

The control signals DT/$\overline{R}$, DEN, /DSDEN0 and , /DSDEN1 control the data bus. DT/$\overline{R}$ determines the direction data will flow. DEN is an enable for the tri-state control line of the transciever data buffers. /DSDEN0 is an enable, and in conjunction with A0, controls the lower 8 bits of the data bus. /DSDEN1 is also an enable, and in conjunction with BHE, controls the upper 8 bits of the data bus. The independent control lines, /DSDEN0 and /DSDEN1, allow for 8 bit to 16 bit data conversions.

The SL6001 incorporates an enhanced mode signal, /EMODE. When asserted, the RAS and ALE signals will become active earlier. The signal, ALE, used to latch the address bus, will become active asynchronous to the status signals S0 and S1. This allows the address to be latched as soon as posssible. The signal, RAS, also becomes active earlier which extends the memory cycle. Lower speed memories can be used in this configuration while the same CPU clock rate is maintained. If the signal, /EMODE, is deasserted, the standard IBM PC / AT timing for the ALE and RAS signals is used.

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DMA and Refresh Logic

Refresh is performed using the same method as the DMA controller to request control of CPU data and address bus. During memory refresh, the CPU is in a hold condition. After the refresh cycle has finished, the CPU is released from the hold condition. To ensure there is no contention between a hold request for a refresh cycle and a hold request from the DMA controller, the refresh request signal, REFREQ, is clocked on the falling edge of the DMACLK and DMA request signal, HRQ1, is clocked on the rising edge.

The REFREQ input to the SL6001 is positive edge triggered. The Refresh request will be internally latched if the minimum low and high times are met. Once the REFREQ signal is latched, the CPU hold request signal, CPUHRQ will be asserted on the falling edge of the DMACLK. When the CPU asserts HLDA, the hold request is acknowledged, and the command bus is tri-stated.

The command signals, /MEMR, /MEMW, /IOR, /IOW and /INTA should have external pull-up resistor to VDD to ensure they are inactive while tri-stated. After HLDA is asserted, /REF is asserted and REFDET will toggle. The signal /REF, an open drain output, initiates the refresh cycle. The signal, REFDET, changes state at the beginning of each refresh cycle. On the next rising edge of SYSCLK, /REFEN is asserted. The signal /REFEN will enable the refresh counter outputs to memory during the refresh cycle. The signals, RAS and /MEMR, are asserted one cycle of SYSCLK later and will remain active for two cycles of SYSCLK. The hold request is then removed when the signal CPUHRQ is deasserted. The signal, /MEMR, will return to the tri-state condition if the CPU has not regained control of the command bus after one cycle of SYSCLK.

As mentioned above, hold requests from the DMA controller are handled in the same manner. When a DMA request has been received, the DMA controller asserts HRQ1. Then, on the rising edge of DMACLK, the CPU hold request, CPUHRQ, is asserted. When the CPU asserts HLDA, the hold request is acknowledged and the CPU has suspended operation.The SL6001 will assert HLDA1 and tri-state the command bus. The DMA controller is in control of the system and can begin a bus cycle. If necessary, a wait state can be inserted in the DMA cycle. One possibility is to (OR) /MEMR and /IOR together and apply the output the DRC input of the SL6001. This will provide a Low to High transition early in the DMA cycle and extend the cycle by one DMACLK. The DMA cycle can be extended further, by the I/O device, by deasserting IOCHRDY. The DMA controller will be held in a wait state until IOCHRDY is reasserted.

Numerical Processor Control

The SL6001 provides the interface for the 80287 Math Coprocessor. Decoding for select and reset of the 80287, handling the /BUSY and /ERROR signals from the 80287 to the CPU and generating interrupt signals for error handling are provided by the SL6001. The signal, CS287, is an externally generated input for the SL6001. It should be asserted when the I/O addresses 0F0H-0FFH are active and is used internal to the SL6001 to generate the signals, /NPCS, the 80287 chip select, and RES287, the 80287 reset signal. Also generated is a clear signal to reset the latched signal, BUSY287. BUSY287 results form an error condition. Refer to Table 2 for specific I/O addresses and their definitions.

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Table 2

Hex address	Description
070	NMI Mask
0F0	Clear Numerical Processor Busy
0F1	Reset Numerical Processor Busy
0F8-0FF	Numerical Processor Chip Select

The signal, /BUSY, is generated by the 80287 when a command to perform a task is detected. When the SL6001 detects that /BUSY is asserted, the output signal, /BUSY287 is asserted for the CPU. Normally, /BUSY is passed through to the /BUSY287 output and /BUSY287 is deasserted when /BUSY is deasserted. During this busy period, the 80287 is performing its task. If an error is detected, the 80287 will assert input signal, /ERROR, of the SL6001. The /ERROR signal will latch the /BUSY287 output and the signal, CPINT, is asserted. Both signals will remain active until cleared by an I/O write cycle to address 0F0H (Clear Numerical Processor Busy) or 0F1H (Reset Numerical Processor Busy). Resetting the 80287 is handled by the output signal, RES287, of the SL6001. RES287 is asserted by a system reset or an I/O write cycle to address 0F1H (Reset Numerical Processor Busy). RES287 is active for the duration of the I/O write cycle or the duration of the system reset signal.

Numerical and Error Logic

The SL6001 performs the latching and enabling of I/O and parity error conditions. A non-maskable interrupt to the CPU will be generated if NMI is enabled. Enabling and disenabling the NMI interrupt is accomplished by asserting the input signal, /NMICS, input of the SL6001. The falling edge of /NMICS will latch the state of the input data bit, XD7. If XD7 is high, NMI is enabled. There are two status signal, IOCK and PCHK, that can be used to determine the source of error if a non-maskable interrupt has been generated. The signal, IOCK, is asserted if the input enable signal, ENIOC, is asserted and I/O error signal, /IOC is asserted. The signal, PCHK, is asserted if the input enable signal, ERMPCK, is asserted and the memory parity error signal, /PAR, is asserted.

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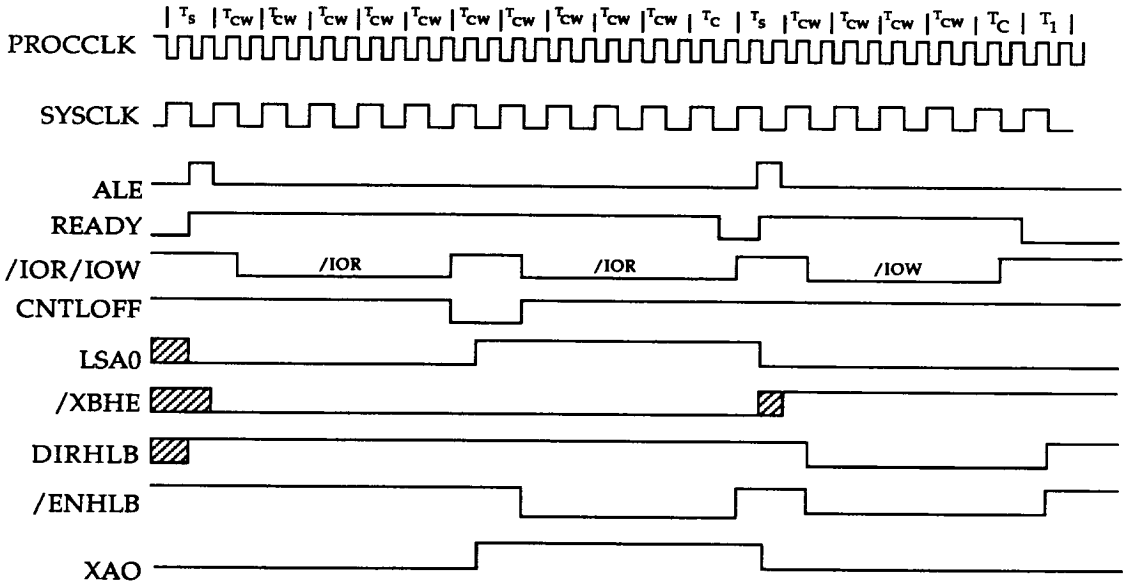

Figure 3. I/O Cycle Sequencer

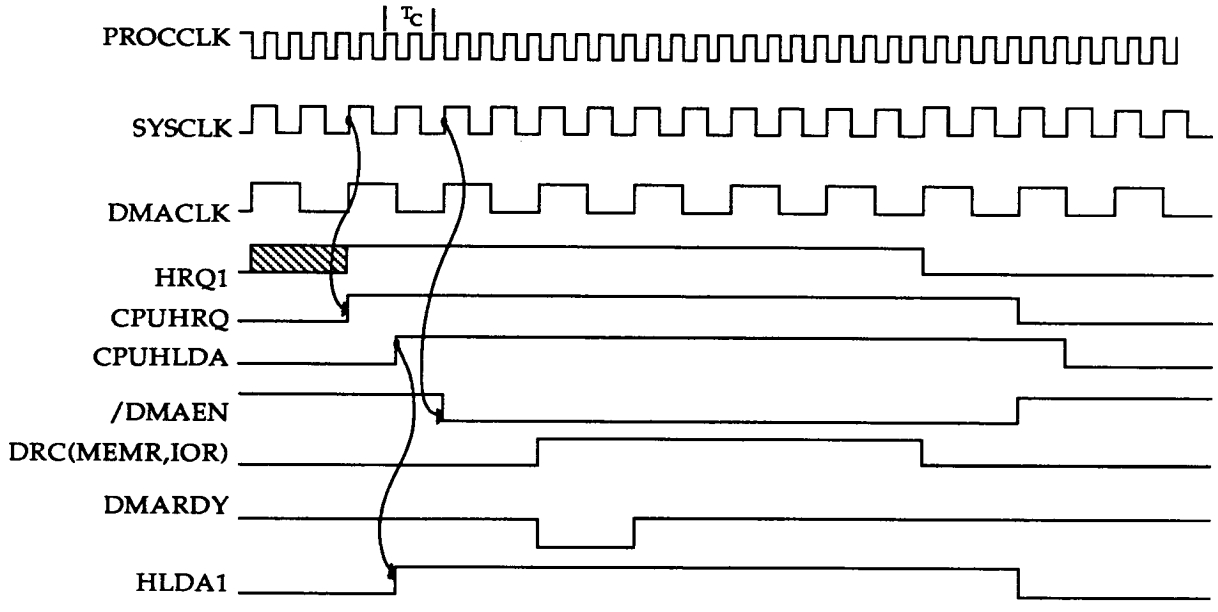

Figure 4. DMA Cycle Sequence

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Pin Description SL6001

Symbol	Pin	Type	Description
A0	73	I	Address bit 0 of the CPU address bus. Used to generate the enable signal for the data transceivers.
A1	14	I	Demultiplexed address bit 1 of the CPU address bus. Used to detect the "shutdown" condition of the CPU.
/AEN1	53	I	Address ENable 1: Active Low, generated by one of the two DMA controllers. Enables the address latches for 8 bit transfers.
/AEN2	54	I	Address ENable 2: Active low, generated by one of the two DMA controllers. Enables the address latches for 16 bit transfers.
/AF16	26	I	Active Low, asserted when 16 bit memory accesses are made. Used to inhibit the command delays for memory access by I/O devices.
ALE	50	O	Address Latch Enable: Active High, controls the address latches during a bus cycle. Not used for a halt bus cycle.
/ARST	10	I	Asynchronous ReSeT: Active Low, used for test purposes only. Resets the PCLK signal to a known state. Normally is pulled through a 10K resistor to VDD.
/BUSY	70	I	Active Low, indicates the 80287 is processing a command. Used to generate the /BUSY287 signal that goes to the CPU.
/BUSY287	67	O	Active Low, output goes to the CPU. Indicates the operating condition of the math coprocessor.
CNTLOFF	58	O	CoNTroLOFF: Active High, to enable the low byte data bus latch during byte accesses. When Low, HLDA asserted, tri-states the command outputs.

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Pin Description SL6001 (Cont'd.)

Symbol	Pin	Type	Description
CPINT	66	O	CoProcessor INTerrupt: Active High, the interrupt request from the math co-processor. Connected to interrupt request 13 of the Interrupt controller.
/CS287	71	I	Chip Select 287: Active Low, on I/O decode signal used to generate /NPCS and RES287 for 287 math co-processor.
CPUHRQ	33	O	CPU Hold ReQuest: Active High, indicates to the CPU that a DMA transfer is requested or a memory refresh cycle is requested.
DEN	51	O	Date ENable: Active High, enables the data transceivers to the local bus.
DIRHLB	59	O	DIRection for High to Low Byte and low to high byte conversion during data transfers to and from 8 bit peripherals. Also referred to as DIR245.
DMACLK	6	O	DMA CLocK: Clock source for the DMA controller. Synchronized to the CPU clock, SYSCLK, and the frequency is half the frequency of SYSCLK.
/DMAEN	55	O	DMA Address ENable: Active Low, is active when any I/O device is making a DMA access to system memory.
DMARDY	32	O	DMA ReaDY: Active High, used to extend memory read and write cycles for slower devices during a DMA cycle. When low, wait states are inserted.
DRC	29	I	DMA Ready Clock: Active High, used to generate the DMARDY signal for DMA controller.
/DSDEN0	41	O	Data Strobe Data ENable 0: Active Low, enables the data transceivers connected to the low byte data bus. Active when DEN is active. When /NPCS is active, this signal is disabled.

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Pin Description SL6001 (Cont'd.)

Symbol	Pin	Type	Description
/DSDEN1	40	O	Data Strobe Data ENable 1: Active Low, enables the data transceivers connected to the high byte data bus. Active when DEN is active. When /NPCS is active, this signal is disabled.
DT/$\overline{R}$	39	O	Data Transmit/Receive: Determines the data direction to and from the local data bus. DEN is inactive when DT/$\overline{R}$ is high when no bus cycle is active.
/EMODE	52	I	Early MODE: Active low, selects the early generation of the signals ALE and RAS.
/ENAS	9	O	ENable Address Strobe: Active Low, enables the Address Strobe input of the MC146818 Real Time Clock. At the first read status input, when /S1 goes low, /ENAS goes low.
/ENHLB	60	O	ENable High to Low Byte perform the high to low byte conversion with DIRHLB signal. If A0=0, word transfers take place and conversion does not occur. Also referred to as GATE245.
ENIOC	20	I	I/O Check Enable: Enables the generation of the IOCK output when the input signal /IOC is asserted.
ERMPCK	21	I	RAM Parity CheckK Enable: Enables the generation of the PCHK output when the input signal /PAR is asserted.
/ERROR	69	I	Active low, indicates an error condition from the 80287 math co-processor.
HLDA	28	I	HoLD Acknowledge: Active High, generated by the CPU granting control for a DMA or memory refresh cycle. When active, /IOR, /IOW, /MEMR, /MEMW and /INTA are tri-stated if CNTLOFF is Low.

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Pin Description SL6001 (Cont'd.)

Symbol	Pin	Type	Description
HLDA1	31	O	HoLD Acknowledge1: Active High, follows the state of HLDA, indicates to the DMA controller to begin the DMA cycle.
HRQ1	30	I	Hold ReQuest 1 : Active High, from the DMA controller, requesting control for DMA cycle. Used to generate CPUHRQ for the CPU.
/INTA	49	O	INTerrupt Acknowledge: Active Low, when received by the Interrupt controller, will output the interrupt vector on to the data bus. When HLDA is asserted and CNTLOFF is low, /INTA is tri-stated.
/IOC	22	I	I/O Check: Active low, generates the IOCK output if ENIOC is asserted. IOC indicates an error condition from an I/O device.
IOCHRDY	34	I	I/O CHannel ReaDY: When Low, wait states are inserted in I/O or memory access by an I/O device. When High, the memory or I/O cycle will process until complete.
IOCK	17	O	I/O CheckK: Active when the input signal, /IOC, is active. IOCK will generate a non-maskable interrupt for the CPU and is stored in Port B as a status bit.
/IOCS16	74	I	I/O Chip Select 16 : Active Low, indicates 16 bit, 1 wait state I/O cycle.
/IOR	45	I/O	I/O Read: Active Low, indicates an I/O read cycle is in progress. When HLDA is asserted and CNTLOFF is low, /IOR is tri-stated.
/IOW	46	I/O	I/O Write: Active Low, indicates an I/O write cycle is in progress. When HLDA is asserted and CNTLOFF is low, /IOW is tri-stated.

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Pin Description SL6001 (Cont'd.)

Symbol	Pin	Type	Description
LSA0	56	O	Address 0: Low for word accesses.
/MEMCS16	25	I	MEMory Chip Select 16: Active Low, indicates 16 bit, 1 wait state memory cycle. Decoded from address LA17-LA23.
M/IO	27	I	Memory/Input-Output: Generated by the CPU to generate the /MEMR, /MEMW, /IOR, /IOW signals. High indicates a memory access, low indicates an I/O access.
/MEMR	48	I/O	MEMory Read: Instructs a memory device place data on the data bus during the read cycle. When HLDA is asserted and CNTLOFF is low, /MEMR is tri-stated.
/MEMW	47	I/O	MEMory Write: Instructs a memory device to store the data on the data bus during a write cycle. When HLDA is asserted and CNTLOFF is low, /MEMW is tri-stated.
NMI	16	O	Non Maskable Interrupt: Active High, connected to the CPU. Indicates a memory parity or I/O error.
/NMICS	23	I	Non Maskable Interrupt Chip Select: Active Low, enable the output signal, NMI.
/NPCS	65	O	Numerical Processor Chip Select: Active Low, connects to the NPSI input of the 80287 math co-processor.
OSC	79	O	OScillator Clock: Buffered clock with same frequency as the crystal frequency at inputs X11 and X12.
OSC/12	78	O	OScillator Clock /12: Buffered clock with a frequency 1/12 the frequency at inputs X11 and X12.

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Pin Description SL6001 (Cont'd.)

Symbol	Pin	Type	Description
/PAR	24	I	PARity error: Active Low, indicates a memory parity error. Used to generate the output signal PCHK.
PCHK	18	O	Parity CHecK: Active High, indicates a memory parity error. Used to generate a non maskable interrupt to the CPU.
PCLK	7	O	Peripheral ClocK: Clocking signal for the peripheral controllers; the frequency is half the frequency of PROCCLK.
PROCCLK	83	O	PROCessor CLocK: The clock signal for CPU. The frequency is half the clock frequency at crystal inputs X1 and X2.
/Q1WS	57	O	One Wait State: Active High, inserts 1 wait state by being active during phase 2 of the CPU bus cycle following the Ts state .
RAS	44	O	Row Address Select: Active high, generates the RAS and CAS signals for memory cycles.
/READY	8	O	Ready: Active low, indicates the current bus cycle will be completed. Controlled by signals /S0, /S1, /WS0 and /RESET1. /READY is an open collector output, requiring an external pull up resistor.
/REF	38	I/O	REFresh: Active Low, initiates a refresh cycle for dynamic memory devices. As an input, can force a refresh cycle from I/O device. /REF is an open drain signal requiring an external pull-up resistor.
/REFDET	36	O	REFresh DETect: Changes state when a refresh cycle is initiated. Can be used to monitor the refresh cycle execution.

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Pin Description SL6001 (Cont'd.)

Symbol	Pin	Type	Description
/REFEN	37	O	REF ENable: Active Low, starts a refresh counter to provide address for memory refresh cycles.
REFREQ	35	I	REFresh REQuest Input: Indicates a refresh cycle should be initiated. Generated by the Timer controller every 15 microseconds.
RES287	68	O	RESET 80287: Active High, resets the 80287 math co-processor.
/RESET1	80	I	Connected to the Power Good signal or an external reset switch. When low, used to generate system reset signals RESET3 and RESET4.
/RESET2	11	I	Generated by the 8042 Universal Peripheral Interface. An active low, will generate a CPU reset through RESET3.
RESET3	77	O	The CPU reset signal. RESET3 is active when /RESET1 or /RESET2 is active. /RESET3 is also active when a HALT status is generated by the CPU by forcing M/IO, /S0, /S1 and A1 Low.
RESET4	4	O	The system reset signal. Active when /RESET1 is active and synchronized the clock signal, PROCCLK.
S0, S1	12,13	I	Status: Generated by the CPU, decoded to determine the type of bus cycle. Pull up resistors should be used on these signals.
SYSCLK	5	O	SYStem CLocK: the frequency is half the frequency of the clock signal, PROCCLK. Synchronized to the processor T-states.
VDD	42,84		Power Supply.

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Pin Description SL6001 (Cont'd.)

Symbol	Pin	Type	Description
VSS	1,43,64		Ground.
/WS0	15	I	Zero Wait State: Active Low, indicates no wait states will be used in memory access. Set up and hold times to the clock must be met.
WS2	76	I	Two Wait States: Active High, indicates I/O accesses will have two wait states inserted into the bus cycle. WS2 may be generated by I/O address decoders.
WS3	75	I	Three wait States: Active High, indicates I/O accesses will have three wait states inserted into the bus cycle. WS3 may be generated by I/O address decoders.
X1, X2	2,3	I	Crystal Inputs for parallel resonant fundamental frequency crystal. The crystal frequency must be twice the desired frequency of the clock signal PROCCLK. X1 may be used as a TTL clock input.
X11, X12	82,81	I	Crystal inputs for parallel resonant fundamental mode frequency crystal. Used to generate the clock signals OSC and OSC/12. X11 may be used as a TTL clock input.
XA0	62	I/O	Address 0: Used to decode the interrupt controller commands issued by the CPU.
XA3	72	I	Address 3: Used to generate the chip select signal, /NPCS, for the 80287 math co-processor.
/XBHE	61	I/O	Bus High Enable: Active Low, enables the high byte data bus to pass through the data bus tranceivers.
XD7	19	I	Data Bus 7: Bit 7 of the peripheral data bus used to generate the non-maskable interrupt enable for the CPU.

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Absolute Maximum Ratings SL6001, SL6002

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	VDD	-	7.0	V
Input Voltage	VI	-0.5	5.5	V
Output Voltage	VO	-0.5	5.5	V
Operating Temperature	Top	-25	85	C
Storage Temperature	Tstg	-40	125	C

NOTE: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the Operating Conditions.

DC Characteristics SL6001, SL6002

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Parameters	Symbol	Min.	Max.	Units	Conditions
Input Low Voltage	VIL		0.8	V	
Input High Voltage	VIH	2.0		V	
Output Low Voltage	VOL		0.45	V	IOL=8 mA (Note 1)
Output High Voltage	VOH	2.4		V	IOH (Note 1)
Input Current	IIL		±10	uA	0<VIN<VDD
Output Short Circuit Current	IOS	TBD	TBD	mA	VO=0V
Input Clamp Voltage	VIC		TBD	V	
Power Supply Current	IDD		20	mA	@ 20 MHz Clock (Pin 2 of SL6001)
Output HI-Z Leak Current	IOZ1		±10	uA	0.45<VOUT<VDD
PROCCLK Output Low Voltage	VOLC		0.45	V	@ IOL = 5 mA
PROCCLK Output High Voltage	VOHC	4.0		V	@ IOH = -1 mA

NOTE: Pins 44, 83 only. Pins 3, 5, 8, 38, 45-50, 55, 61, 62, 65, 78, 79, and 81 have IOL = 4 mA. All other outputs and I/O pins have IOL = 2 mA. In all cases IOL = IOH = for the pin.

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AC Characteristics SL6001

(TA = 0 °C to 70 °C, VDD = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t1	PROCCLK period, (Note 2)	40	250	ns
t2	PROCCLK low time	11	125	ns
t3	PROCCLK high time	18	135	ns
t4	M/$\overline{IO}$, /S0, /S1 hold time, (PROCCLK Load = 50pf)	1		ns
t5	M/$\overline{IO}$, /S0, /S1 set-up time	20		ns
t6	ALE active delay (/EMODE = 1), (Note1)	5	15	ns
t7	ALE inactive delay (Note 1)	5	15	ns
t8	ALE delay from Status (/EMODE = 0), (Note1)	5	24	ns
t9	RAS active delay (/EMODE = 1), (Note1)	10	30	ns
t10	RAS inactive delay (/EMODE = 1), (Note 1)	10	35	ns
t11	RAS active delay (/EMODE = 0)	5	15	ns
t12	RAS inactive delay (/EMODE = 0)	5	15	ns
t13	/WS0 set-up time, (PROCCLK Load = 50pf)	20		ns
t14	/WS0 hold time, (PROCCLK Load = 50pf)	0		ns
t15	Command active delay, (Note 1)	8	20	ns
t16	Command inactive delay, (Note 1)	8	20	ns
t17	DT/$\overline{R}$ active delay, (Note 1)	7	13	ns
t18	DT/$\overline{R}$ inactive delay, (Note 1)	5	9	ns
t19	DEN active delay from DT/$\overline{R}$ low (Read), (Note 1)	0	7	ns
t20	DEN inactive delay, (Note 1)	5	20	ns
t21	/DSDEN0, /DSDEN1 active delay from DEN active, (Note 1)	2	10	ns
t22	/DSDEN0, /DSDEN1 inactive from DEN inactive, (Note 1)	-2	-6	ns
t23	XA0, /XBHE set-up from DEN active	5		ns
t24	XA0, /XBHE set-up from DEN inactive	0		ns
t25	DEN active delay (Write) (Note 1)	7	13	ns
t26	DEN inactive delay (Write) (Note 1)	5	20	ns
t27	/AF16, /MEMCS16 set-up time	20		ns
t28	/AF16, /MEMCS16 hold time	0		ns
t29	/RESET1 hold time , (PROCCLK Load = 50pf)	10		ns
t30	/RESET1 set-up time, (PROCCLK Load = 50pf)	28		ns
t31	RESET4 delay, (Note 1)		15	ns
t32	/ENAS delay, (Note 1)		15	ns
t33	SYSCLK delay, (Note 1)		12	ns
t34	DMACLK delay from SYSCLK , (Note 1)		10	ns
t35	RESET3 delay, (Note 1)	5	15	ns
t36	RESET3 delay (Shut-down detected), (Note 1)	5	20	ns

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AC Characteristics SL6001 (Cont'd.)

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t37	PCLK delay, (Note 1)		10	ns
t38	OSC/12 delay from OSC, (Note 1)		15	ns
t39	/DSDEN0, /DSDEN1 active delay from DT/$\overline{R}$, (Note 1)	3	10	ns
t40	DT/$\overline{R}$ inactive delay from /DSDEN0, /DSDEN1, (Note 1)	-3	-7	ns
t41	CPUHRQ active delay (due to REFREQ) from DMACLK (DMACLK Load = 50pf)		25	ns
t42	CPUHRQ inactive delay from SYSCLK		25	ns
t43	/REF active delay from HLDA, (Note 3)		25	ns
t44	/REF inactive delay from SYSCLK, (Note 3)		25	ns
t45	HLDA1, /REF active delay from SYSCLK		25	ns
t46	REFDET delay from /REF		10	ns
t47	/REFEN active delay from SYSCLK		25	ns
t48	/REFEN inactive delay from SYSCLK		15	ns
t49	/MEMR tri-state delay from HLDA		30	ns
t50	/MEMR tri-state delay from SYSCLK		20	ns
t51	/MEMR (Refresh) active delay from SYSCLK		20	ns
t52	/MEMR (Refresh) inactive delay from SYSCLK		20	ns
t53	REFREQ set-up to DMACLK	25		ns
t54	REFREQ width	25		ns
t55	IOCHRDY Set-up to PROCCLK	25		ns
t60	HRQ1 set-up to DMACLK, (DMACLK load = 50 pF)	15		ns
t61	HLDA1 active, inactive delay from HLDA		30	ns
t62	HLDA1 inactive delay from SYSCLK		30	ns
t63	AEN1, AEN2 set-up from DRC	25		ns
t64	DRC set-up time from DMACLK	25		ns
t65	DMARDY delay from DRC		35	ns
t66	DMARDY delay from DMACLK		30	ns
t67	HRQ1 hold time from DMACLK	1		ns
t68	DRC hold time from DMACLK	1		ns
t69	AEN1, AEN2 hold time from DMARDY	1		ns
t70	/READY inactive delay, (Note 3)		6	ns
t71	/READY active delay, (Note 3)		8	ns
t72	A0 set-up time from PROCCLK	5		ns
t73	A0 hold time from PROCCLK	15		ns
t74	LSA0 delay		30	ns
t75	Q1WS delay		20	ns
t76	WS2, WS3 set-up time	20		ns
t77	WS2, WS3 hold time	0		ns

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AC Characteristics SL6001 (Cont'd.)

(TA = 0 °C to 70 °C, VDD = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t78	CTLOFF active delay		35	ns
t79	CTLOFF inactive delay		35	ns
t80	/ENAHLB, DIRHLB inactive delay from /IOR, /IOW		25	ns
t81	DIRHLB delay from PPROCLK (high byte /IOW)		25	ns
t82	XA0, /XBHE set-up from ALE trailing edge	0		ns
t83	/IOCS16 inactive set-up to /IOR, /IOW active	5		ns
t84	/IOCS16 hold time from /IOR, /IOW inactive	2		ns
t85	XD7 set-up time with respect to /NMICS	10		ns
t86	XD7 hold time with respect to /NMICS	1		ns
t87	/NPCS active delay from XA3, /INTA, /CS287		35	ns
t88	/NPCS inactive delay from XA3, /INTA, /CS287		30	ns
t89	CPINT delay from /BUSY, /ERROR low, (Note 4)		30	ns
t90	CPINT inactive delay from /ERROR high, (Note 5)		30	ns
t91	Overlap of /BUSY and /ERROR (both low)	10		ns
t92	/BUSY287 active delay from /BUSY		30	ns
t93	/BUSY287 inactive delay from /BUSY		30	ns
t94	/IOCS16 active set-up to PROCCLK		25	ns
t95	/ERROR hold-time with respect to /BUSY	0		ns
t96	/BUSY active pulse width	15		ns
t97	/ERROR setup with respect to /BUSY	5		ns
t98	/ERROR min low pulse width	10		ns
t99	/BUSY287 delay from /IOW		30	ns
t100	XA0, XA3, /CS287 set-up time with respect to /IOW	10		ns
t101	XA0, XA3, /CS287 hold time with respect to /IOW	1		ns
t102	RES287 active delay from /IOW		30	ns
t103	RES287 inactive delay from /IOW		30	ns
t104	CPUHRQ inactive delay from /INTA		25	ns
t105	CPUHRQ active delay from /IOW		25	ns
t106	/PAR, /IOC low pulse width	10		ns
t107	IOCK, PCK, NMI delay		30	ns
t108	IOCK, PCK, NMI delay from ENIOC, ENPCHK low		30	ns
t109	ENIOC, ENPCHK min low width	10		ns

NOTES:

1. Pin capacitive load = 50pf; TTL levels
2. Measured from VOL = 0.6V VOH = 3.6V
3. /READY and /REF are open drain outputs; times specified are from high impedance to active and active to high impedance. Actual times will depend on value of external resistor used.
4. /BUSY and /ERROR have to be both low for CPINT active transition.
5. Load capacitance = 85 pf on all outputs except stated otherwise.

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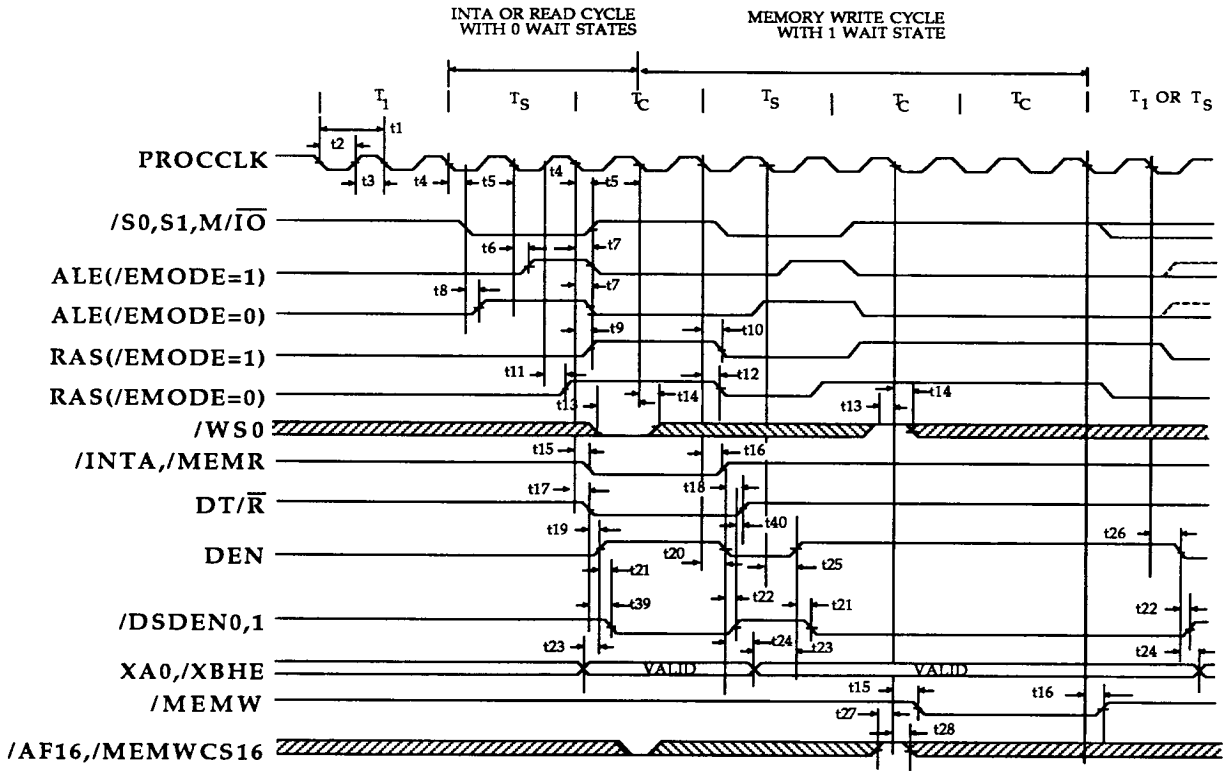
AC TIMING DIAGRAMS SL6001



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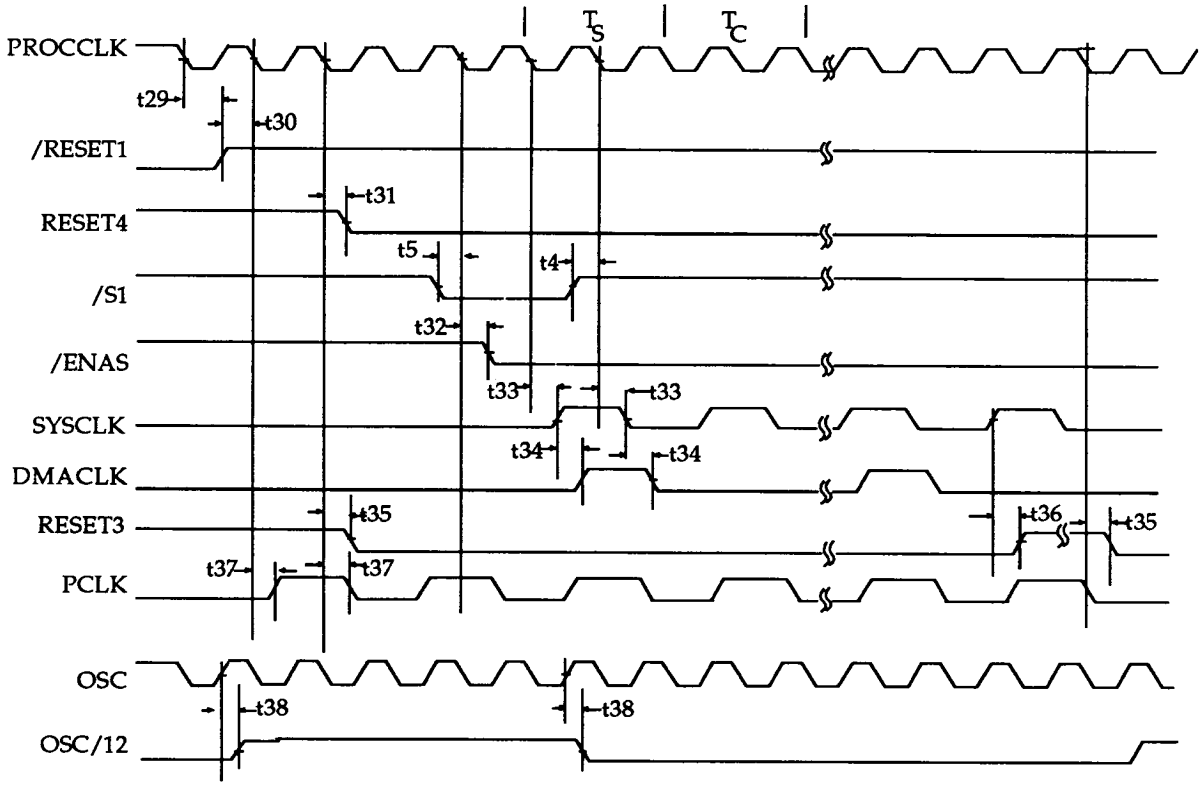
AC TIMING DIAGRAMS SL6001



NOTE

1. /RESET is an asynchronous input and the timings are shown only to guarantee signal recognition on that clock cycle instead of the next one.
2. RESET3 is shown going high due to an internally detected shut down condition and will return low 16 PRCK cycle later.

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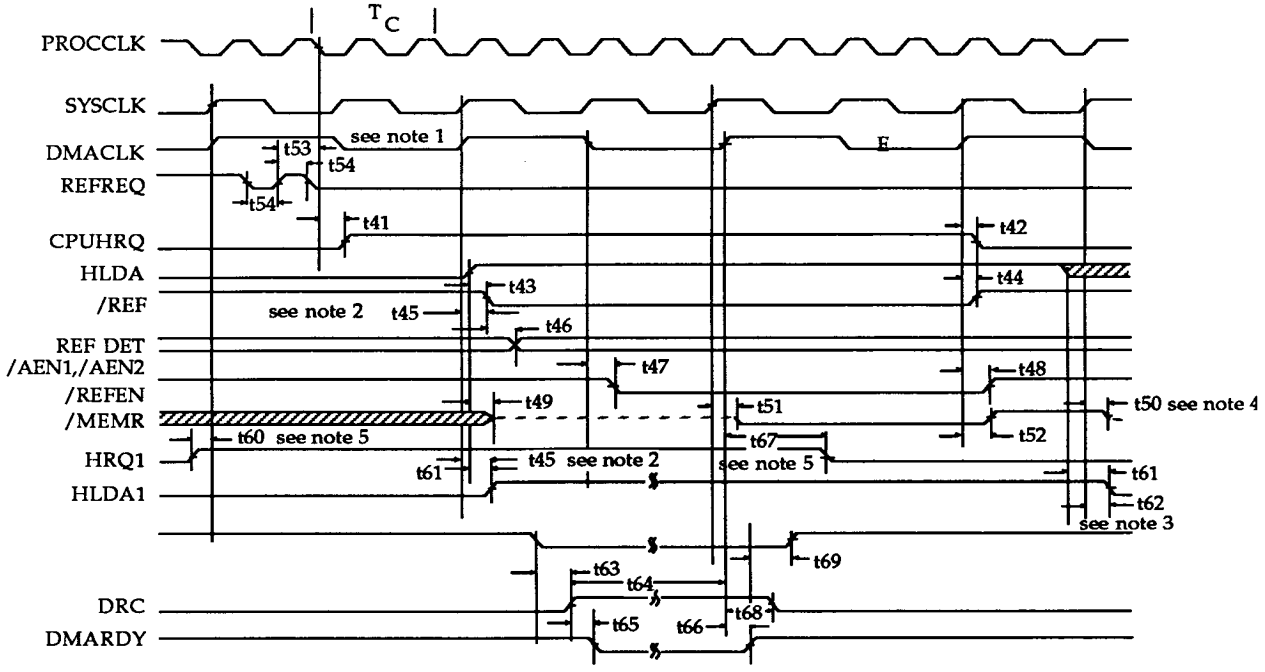
AC TIMING DIAGRAMS SL6001



NOTE

1. REFREQ is an asynchronous input and the timing from the high going edge of REFREQ to the low going edge of DMACLK is only to guarantee starting a refresh cycle on that clock cycle instead of the next one.
2. This timing parameter is shown because /REF & HLDA1 are inhibited until this time. After this point CPU HLDA will enable /REF or HLDA1.
3. HLDA1 will be deasserted at this time by SYSCLK if HLDA is still active.
4. /MEMR will tri-state at this time if HLDA is still active.
5. Set-up and hold times are shown only to guarantee signal recognition on this clock edge.

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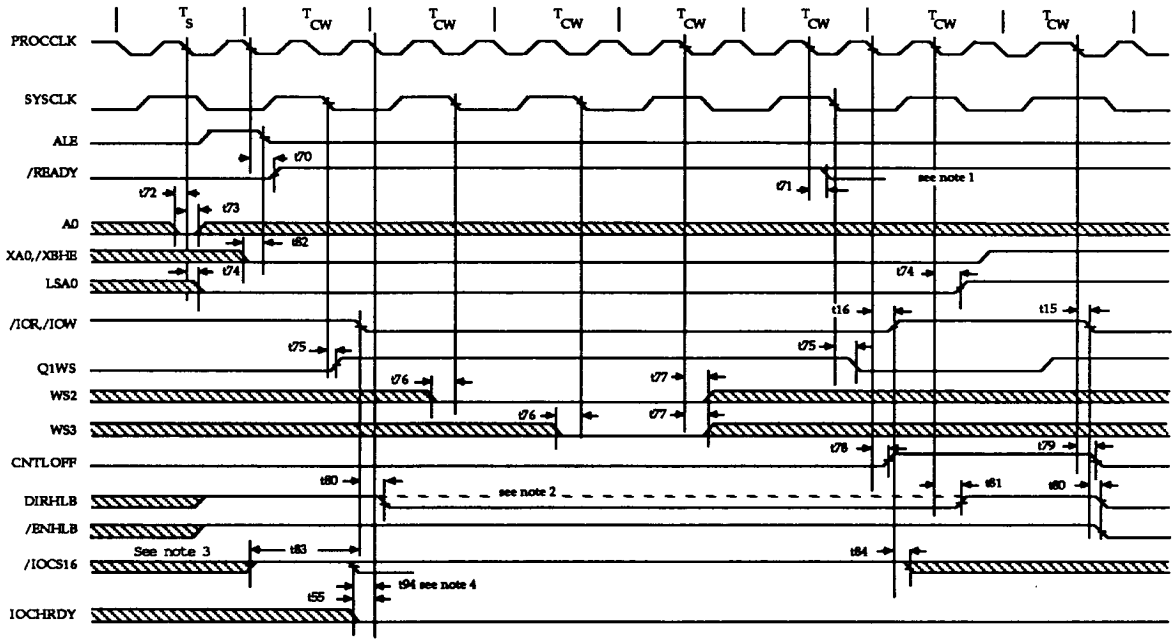
AC TIMING DIAGRAMS SL6001



NOTE
1. READY asserted here on 8-bit transfer to 8-bit peripheral.
2. DIRHLB shown for I/O write cycle: dotted line for I/O read cycle.
3. /IOCS16 inactive setup to /IOR, /IOW is to prevent one wait state operation.
4. /IOCS16 active setup to PROCCLK is to ensure that no conversion will take place.

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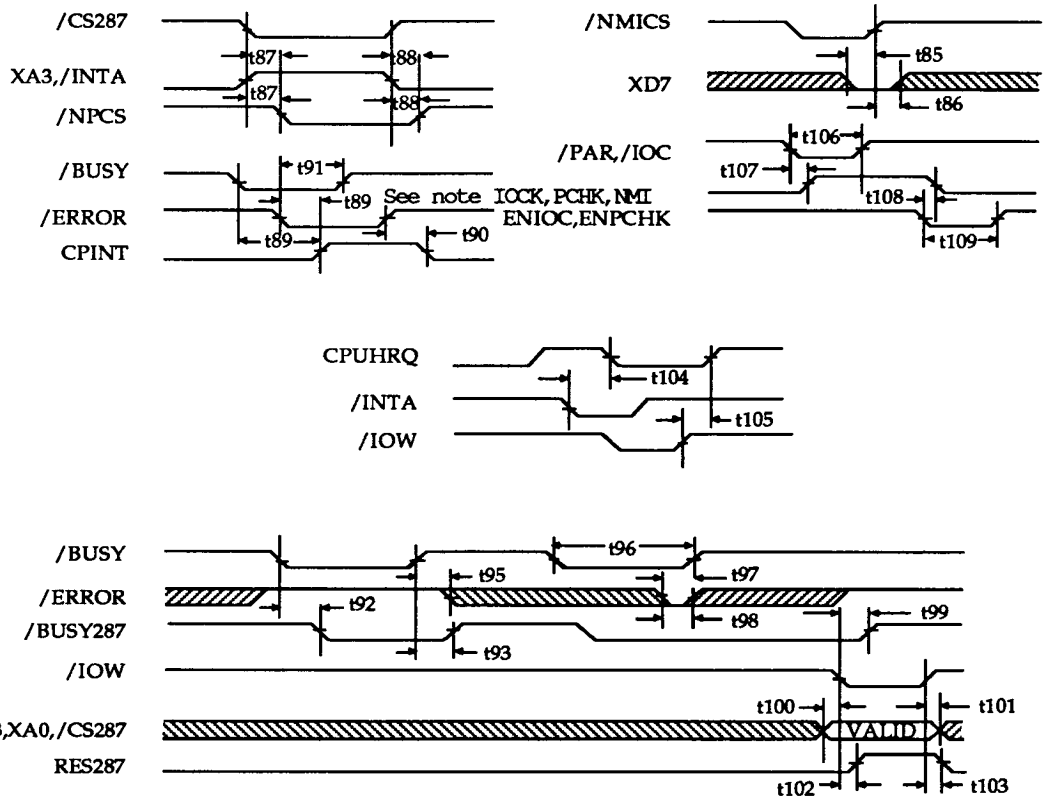
AC TIMING DIAGRAMS SL6001



NOTE
1. /BUSY and /ERROR both have to be low for CPINT to be active.

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Functional Description SL6002

The SL6002 contains the following blocks:

I/O Decode Logic

The SL6002 provides the signals to control the Clock - Calendar, Status - Control Port, NMI Enable Latch and Keyboard Controller.

Three signals are generated to control the Clock-Calendar. The signal, SRTAS, latches the address to the Clock - Calendar. The signal, SRTDS, latches the data to/from the Clock - Calendar. The signal, SRTRW, determines the direction of the data transfer. Gating of SRTAS with Q1WS and /ENAS is performed to ensure proper latching of the register address by the Clock - Calendar. The signals Q1WS and /ENAS are generated by the SL6001.

Two signals are generated to control the Status - Control Port. The signal, /PORTBRD, enable the status information onto the data bus. The signal, /PORTBWR, latches the contents of the data bus into the control port.

The signal, NMICS, controls the enabling and disabling of the NMI Enable latch. The signal, /8042CS, selects the keyboard controller.

IBM PC / AT compatibility is maintained for all decoded control signals generated by the SL6002. Refer to Table 3 for a list of I/O addresses and their corresponding outputs.

ROM/RAM Decode & Latch

The SL6002 provides the circuitry, to decode the CPU address bus and to control the ROMs and RAMs used on the system mother board. To accomodate various RAM devices, a user configureable decode is provided by strapping input signals, SEL0, SEL1, and SEL2. These systems can be configured for 64k, 256k or 1M RAM devices. System memory can be configured from 128k bytes to 2M bytes of RAM. Refer to Table 4 for the strapping options and their definitions.

The SL6002 provides support for memory refresh. During a refresh cycle, when the input REF is asserted , the outputs RAS0 and RAS1 are activated, the outputs CAS0, and CAS1 are inhibited and the current address bus state is ignored.

The SL6002 generates the ROM chip select signal, /LCSROM. It is asserted when the appropriate address range is detected and the input signal REF is inactive. Refer to Table 4 for appropriate address range for /LCSROM.

The SL6002 generates two signals used as memory buffer signals. The signal /LMEGCS is active when a memory access is made to an address below 100000H or when the input signal REF is active. The signal /MDBEN is used for memory data bus buffer control. This signal is active when the signal CAS0 and CAS1 or /LCSROM is active. /MDBEN may be externally ANDed with /MEMR to generate the directional control signal for the memory data buffer.

The SL6002 internal latch is controlled by input signals, HLDA and ALE. The output of this latch drives the signals RAS0, RAS1, CAS0, CAS1, /LMEGCS, /LCSROM and /MDBEN. When ALE is asserted, during a CPU memory cycle, the outputs from the memory decoder are passed to the outputs of the latch. When ALE is deasserted, the memory decoder outputs are latched for the remainder of the cycle. When HLDA is asserted, the outputs from the memory decoder are passed to the outputs of the latch but force /LCSROM inactive regardless of the outputs of the memory decoder.

The SL6002 generates one output from the memory decoder which is not latched. The signal, /AF16, is used by external circuitry to indicate a 16 bit memory transfer. It may also be used to generate wait states.

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Parity Error Detection Logic

The SL6002 generates the parity error signal, /PAR, used by the SL6001 to generate a non-maskable interrupt. The input signals to derive, /PAR, MDPIN0 and MDPIN1 are generated from the Parity Generator/Check. MDPIN0 is derived from the low byte (D0-D7) and MDPIN1 is derived from the high byte (D8-D15).

The signal, /PAR, is asserted when MDPIN0 is high and XA0 is low or, when MDPIN1 is high and XBHE is low on the rising edge of /XMEMR.

To provide for memory expansion beyond what is decoded by the SL6002, the input signal /UCAS is provided. The signal, /UCAS, when asserted will cause the output signal, PAREN, active. This enables the Parity Error detection Logic. If an error condition is detected on the rising edge of /XMEMR, /PAR is asserted.

Table 3.

INPUTS					OUTPUTS						
/PPICS	XAO	XA4	/XIOR	/XIOW	/NMICS	/PORTBRD	/PORTBWR	/8042CS	SRTDS	SRTAS*	SRTRW
1	X	X	X	X	1	1	1	1	1	0	1
0	0	0	X	X	1	1	1	0	1	0	1
0	1	0	0	X	1	0	1	1	1	0	1
0	1	0	X	0	1	1	0	1	1	0	1
0	0	1	X	0	0	1	1	1	1	1	1
0	1	1	X	0	1	1	1	1	1	0	0
0	1	1	0	X	1	1	1	1	0	0	1

X = Don't Care, 0 = TTL Low, 1 = TTL High
*Note: This condition assumes Q1WS and /ENAS are true.

Table 4.

Select Input			RAM Address Range		RAM Type		ROM Address Range	
SEL2	SEL1	SEL0	RAS0/CAS0	RAS1/CAS1	BANK0	BANK1	Low Addr. Range	High Addr. Range
1	0	0	000000h-01FFFFh	020000h-03FFFFh	64K	64K	0E0000h-0FFFFFh	FE0000h-FFFFFFh
1	0	1	000000h-07FFFFh		256K	NONE	0E0000h-0FFFFFh	FE0000h-FFFFFFh
1	1	0	000000h-07FFFFh	080000h-09FFFFh	256K	64K	0E0000h-0FFFFFh	FE0000h-FFFFFFh
1	1	1	000000h-07FFFFh	100000h-17FFFFh	256K	256K	0E0000h-0FFFFFh	FE0000h-FFFFFFh
0	X	X	000000h-07FFFFh	100000h-2FFFFFh	1M	1M	0E0000h-0FFFFFh	FE0000h-FFFFFFh

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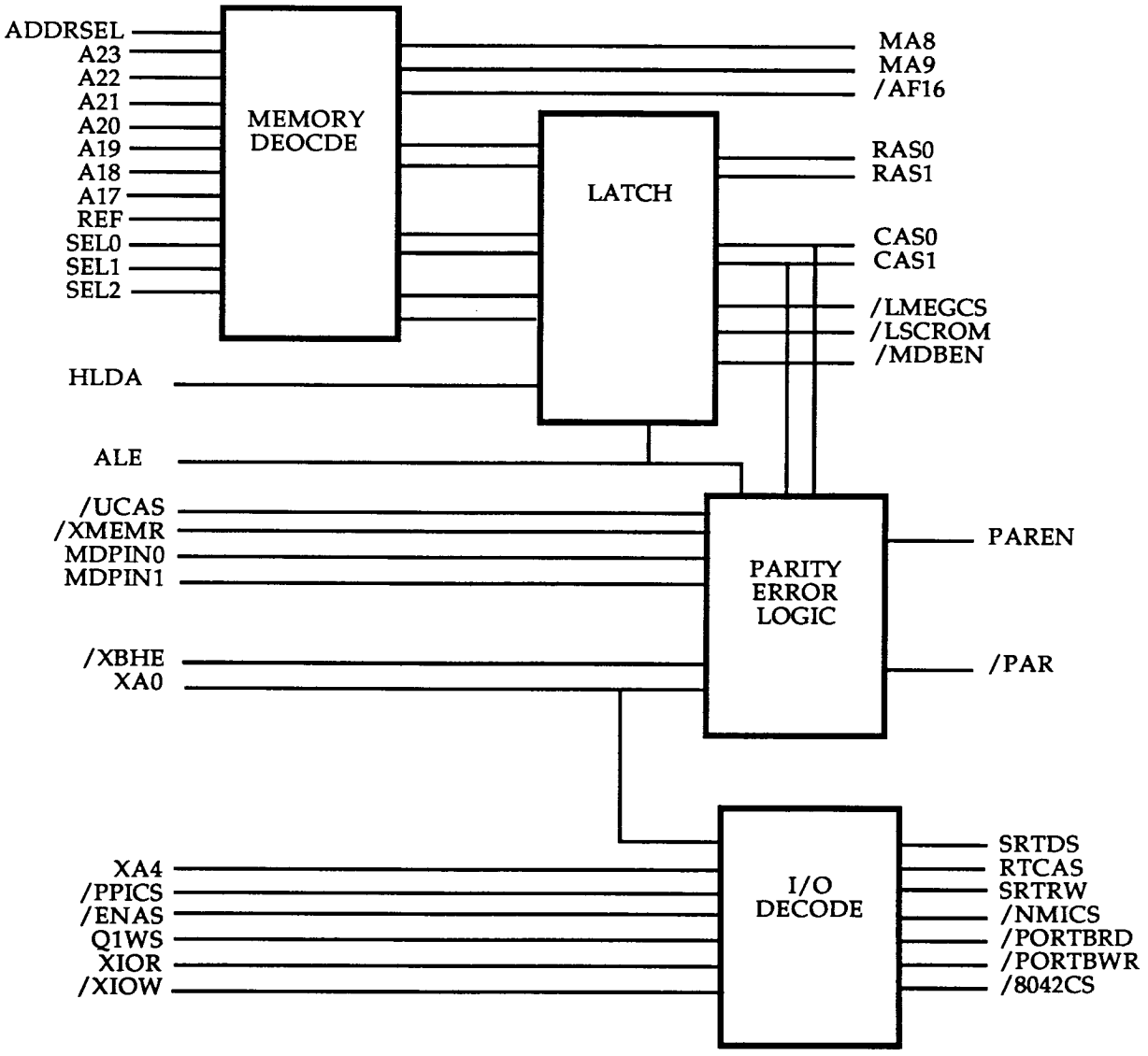

Figure 5. Functional Block Diagram SL6002

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Pin Description SL6002

Symbol	Pin	Type	Description
A17 -A23	40-34	I	Address Bus from CPU addresss bus.
ADDRSEL	19	I	ADDress SELect: Active high, passess addresses A18 and A20 to output signals, MA8 and MA9.
/AF16	4	O	Active low, indicates a 16 bit memory access. Also used to insert wait states or slower I/O devices.
ALE	14	I	Address Latch Enable: Active high, latches the low order address signals and RAS/CAS signals from the memory decode.
CAS0,CAS1	45,44	O	Column Addres Select: Select the low and high byte address signals on memory cycles.
/ENAS	15	I	Enable Address Strobe: Active low, the address strobe signal for the real time clock device, MC146818.
HLDA	13	I	HoLD Acknowledge: Active high, indicates the CPU has given control of the command bus for DMA or refresh cycle.
/LCSROM	2	O	ROM Chip Select: Active low, when ROM/PROM/EPROM address space is accessed.
/LMEGCS	3	O	Low MEG Chip Select: Active low, when memory below 1M Byte is accessed. If memory accesses above 1 M byte are made, /LMEGCS can disable certain read/write signals on the I/O connector.
MA8,MA9	31,43	O	High Memory Address Bit: Generated from address lines A17,A18, A19 and A20 in conjunction with the input signal, ADDRSEL.
MDBEN	5	O	Memory Data Bus ENable: Active low, sets the direction of the data bus buffers used for memory transfers.
MDPIN0, MDPIN1	9,8	I	Memory Data Parity INput 0,1: Parity bit for low and high bytes of memory.
/NMICS	23	O	NMI Chip Select: Active low, enables the non-maskable interrupt to the CPU.
/PAR	6	O	PARity: Active low, indicates a parity error has been detected.
PAREN	41	O	PARity ENable: Active high during a parity check cycle.

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Pin Description SL6002 (Cont'd.)

Symbol	Pin	Type	Description
/PORTBRD	22	O	PORT B ReaD: Active low indicates a read cycle to status port B.
/PORTBWR	21	O	PORT B WRite: Active low indicates a write cycle to status port B.
/PPICS	30	I	Programmable Peripherals Interface Chip Select: Active low, used to select the 8042 peripheral Interface Device.
Q1WS	16	I	Q1 Wait State: Active high, extends the Real Time Clock address strobe , RTCAS by one wait state.
RAMSEL0 RAMSEL1 RAMSEL2	10 11 7	I	RAM SELect 0,1,2: Select the Ram devices and amount of RAM on the system motherboard.

RAMSE0	RAMSEL1	RAMSEL2	RAM Memory
0	0	1	256K
0	0	1	640K
1	0	1	512K
1	1	1	1024K
X	X	0	2048K

RAS0,RAS1	47,46	O	Row Address Select 0,1: Selects the low and high memory bank respectively.
REF	12	I	REFresh; Active high, initiates a refresh cycle for the dynamic RAMS.
RTCAS	27	O	Real Time Clock address Strobe.
SRTDS	25	O	Real Time Clock Data Strobe.
SRTRW	26	O	Real Time Clock Read/Write: Active high indicates a read operation, active low indicates a write operation.
/UCAS	42	I	User CAS: Active low, enables parity generation logic when addressing memory beyond the addressing of the SL6002. Supports parity checking for externally selected to the externally generated CAS signal.
VDD	48		Power supply.
VSS	1,24		Ground.

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Pin Description SL6002 (Cont'd.)

Symbol	Pin	Type	Description
XA0	29	I	Address 0: Address bit 0 used to detect parity errors on the low data byte.
XA4	28	I	Address 4: Address bit 4, used to generate chip selects and data strobes for peripheral devices.
XBHE	32	I	Bus High Enable: used to detect parity errors on the high data byte.
/XIOR, /XIOW	17,18	I	I/O Read and Write: Active low used to generate read and write signals for peripheral devices and other I/O ports in the system.
/XMEMR	33	I	Memory Read: Active read Low, instructs the memory to place the data on the data bus. Also controls the direction of the data flow through the data bus buffers.

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AC Characteristics SL6002

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t1	Address, RAMSEL & REF setup to ALE going inactive	25		ns
t2	Address & RAMSEL hold time from ALE inactive	0		ns
t3	REF hold time from ALE inactive	0		ns
t4	REF hold time from HLDA inactive	0		ns
t5	RAS valid from Address, RAMSEL & REF valid		35	ns
t6	Address setup to ALE going active for ALE to control RAS	25		ns
t7	RAS delay from ALE active		20	ns
t8	CAS valid from Address, RAMSEL & REF valid		35	ns
t9	Address setup to ALE going active for ALE to control CAS	25		ns
t10	CAS delay from ALE active		30	ns
t11	RAS active delay from HLDA active during REF cycle		30	ns
t12	CAS inactive delay from HDLA active during REF cycle		30	ns
t13	/AF16 valid from address valid		35	ns
t14	/LCSROM valid from Address & REF valid		40	ns
t15	Address setup to ALE going active for ALE to control /LCSROM	25		ns
t16	/LCSROM delay from ALE active		35	ns
t17	/MDBEN valid from ALE inactive		30	ns
t18	/MDBEN hold time from ALE going active	5		ns
t19	/LCSROM inactive from HLDA active		30	ns
t20	/LCSROM active from HLDA inactive		30	ns
t21	/PAR inactive from ALE active		25	ns
t22	/PAR active from XMEMR inactive		15	ns
t23	REF setup to HLDA going active	15		ns
t24	MDPIN0, MDPIN1, /XBHE & XA0 hold time from /XMEMR inactive	0		ns
t25	MDPIN0, MDPIN1, /XBHE & XA0 setup time to /XMEMR gong inactive	10		ns
t26	/LMEGCS valid from Address & REF valid		40	ns
t27	Address setup to ALE going active for ALE to control /LMEGCS	25		ns
t28	/LMEGCS valid from ALE active		30	ns
t29	/LMEGCS active from HLDA active during REF cycle		30	ns
t30	PAREN valid from ALE inactive		20	ns
t31	PAREN inactive from ALE active	5	20	ns
t32	PAREN active from /UCAS active		25	ns
t33	PAREN inactive from /UCAS inactive	5	25	ns
t34	/PORTBRD, /PORTBWR, SRTDS or SRTDW active (low) from XA0 and XA4 valid		35	ns
t35	/PORTBRD, /PORTBWR, SRTDS or SRTDW inactive (high) from XA0 and XA4 invalid	5		ns
t36	/PORTBRD, /PORTBWR, SRTDS or SRTDW active (low) from /XIOR or /XIOW active		35	ns
t37	/PORTBRD, /PORTBWR, SRTDS or SRTDW inactive (high) from /XIOR or /XIOW inactive	5		ns
t38	/PORTBRD, /PORTBWR, SRTDS or SRTRW active from /PPICS active		35	ns
t39	/PORTBRD, /PORTBWR, SRTDS or SRTRW inactive from /PPICS inactive		5	ns

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AC Characteristics SL6002 (Cont'd.)

(TA = 0 °C to 70 °C, VDD = 5V ± 5%)

Sym	Description	Min.	Max.	Units
t40	/8042CS active from /PPICS active		35	ns
t41	/8042CS inactive from /PPICS inactive	5		ns
t42	/8042CS active from XA0 & XA4 valid		35	ns
t43	/8042CS inactive from XA0 & XA4 invalid	5		ns
t44	SRTAS active from XA0 & XA4 valid		35	ns
t45	SRTAS inactive from XA0 & XA4 invalid	5	35	ns
t46	SRTAS active from /ENAS active		35	ns
t47	SRTAS inactive from /ENAS inactive	5	35	ns
t48	SRTAS active from Q1WS active		35	ns
t49	SRTAS inactive from Q1WS inactive	5	35	ns
t50	SRTAS active from /XIOW active		35	ns
t51	SRTAS inactive from /XIOW inactive	5	35	ns

Output Test Conditions:

RAS0, 1
CAS0, 1
/MDBEN
/AF16
/LCSROM
/LMEGCS

CL = 85pF
IOL = 4 mA
IOH = 4 mA

/PAR
PAREN
/PORTBRD
/PORTBWR
SRTDS
SRTRW
/8042CS
SRTAS

CL = 50pF
IOL = 2 mA
IOH = 2 mA

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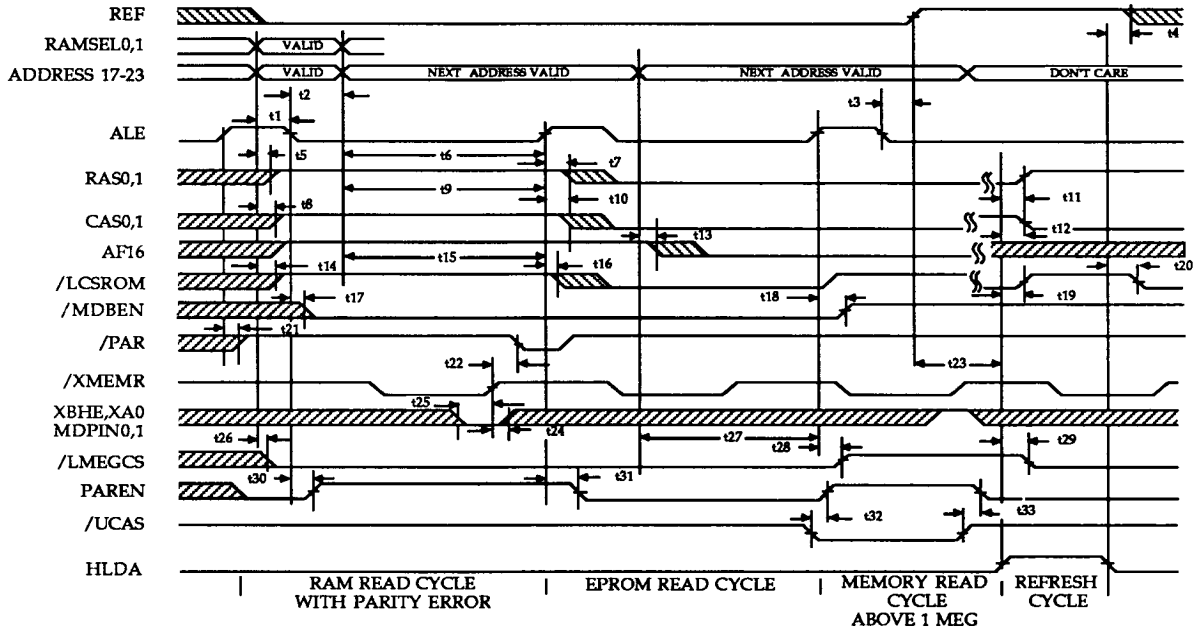
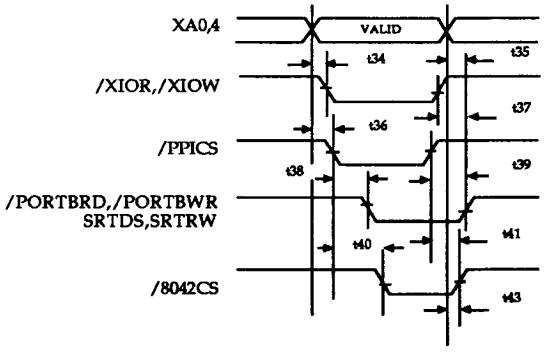
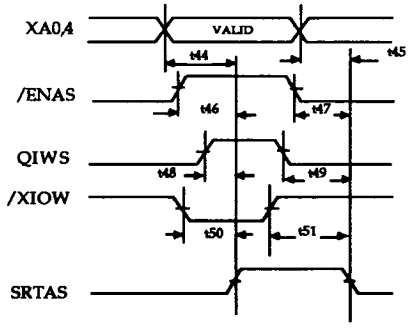
AC TIMING DIAGRAMS SL6002







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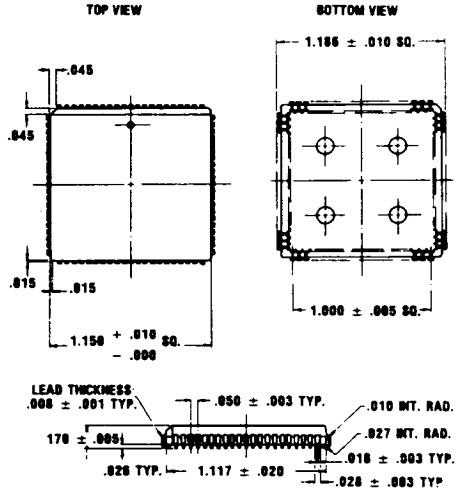
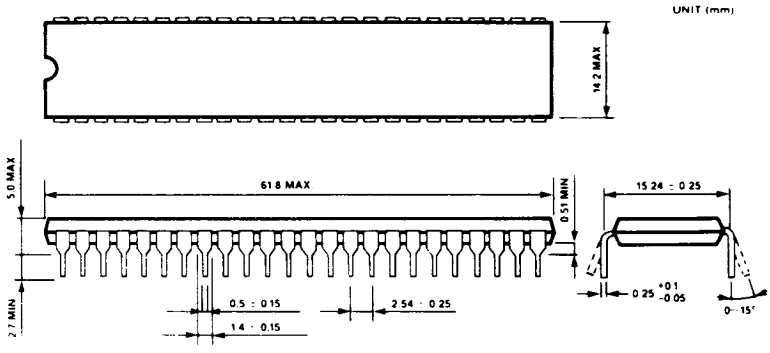
Package Information

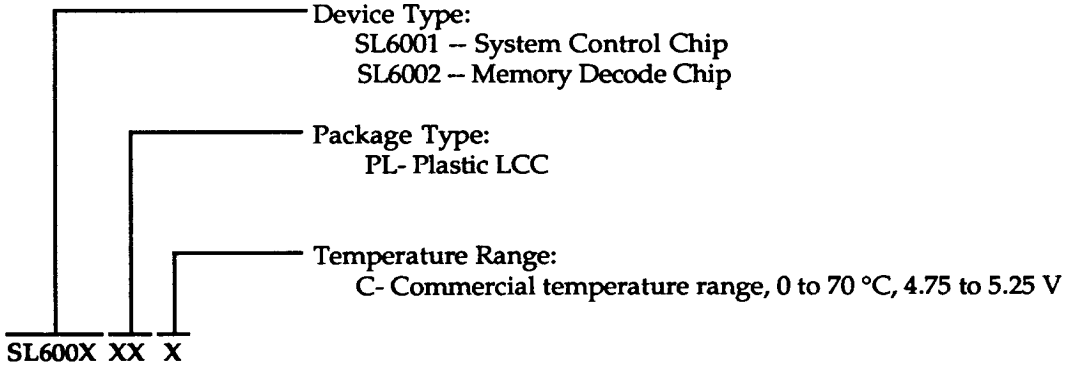
84-PIN PLASTIC LEADED CHIP CARRIER



48-PIN PLASTIC DUAL-IN-LINE PACKAGE



ORDERING INFORMATION



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