PRELIMINARY

INTEL 430VX PCISET
82437VX SYSTEM CONTROLLER (TVX) AND 82438VX DATA PATH UNIT (TDX)

- Supports All 3V Pentium® Processors
- PCI 2.1 Compliant
- Integrated DRAM Controller
  - 64-Bit Path to Memory
  - 4 MB to 128 MB of Main memory
  - EDO/Fast Page Mode DRAM Support (6-2-2-2 Reads at 66 MHz)
  - 5 RAS Lines
  - Support for Symmetrical and Asymmetrical DRAMs
  - Supports SDRAM (x-1-1-1 at 66 MHz)
  - Buffering for 3-1-1-1 Posted Writes, DWord and Burst Merging
  - Supports Mixed Memory Technologies (EDO/SPM/SDRAM)
  - Supports 3V or 5V DRAMs
  - External Buffers on MA Lines are Not Required
- Integrated Second Level Cache Controller
  - Direct Mapped Organization
  - Supports 256-KB and 512-KB Pipelined Burst, DRAM Cache and Standard SRAM
  - Cache Hit Read/Write Cycle Timings at 3-1-1-1 with Burst or DRAM Cache SRAM
  - Back-to-Back Read/Write Cycles at 3-1-1-1-1-1-1-1
  - Supports Write-Back
- Fully Synchronous 25/30/33 MHz PCI Bus Interface
  - 5 PCI Bus Masters (including PIIX3)
  - Converts Back-to-Back sequential PCI Memory Writes to PCI Burst Writes
  - CPU-to-PCI Memory Writes Posting
  - PCI-to-DRAM Read Prefetching
  - PCI-to-DRAM Posting
  - Multi-Transaction Timer to Support Multiple Short PCI Transactions
- Shared Memory Buffer Architecture (SMBA) Support
  - Support Graphics Controller through a 2-Wire Protocol
  - Supports 1 Row of DRAM (EDO/FPM/SDRAM)
  - Enhanced Performance Features Specific to SMBA
- Supports the Universal Serial Bus (USB)
- 208-Pin QFP System Controller (TVX), two 100-Pin QFP Data Paths (TDX)

The Intel 430VX PCIset consists of the 82437VX System Controller (TVX), two 82438VX Data Paths (TDX), and the PCI ISA IDE Xcelerator (PIIX3). The PCIset forms a Host-to-PCI bridge and provides the second level cache control and a full function 64-bit data path to main memory. The TVX integrates the cache and main memory DRAM control functions and provides bus control for transfers between the CPU, cache, main memory, and the PCI Bus. The second level (L2) cache controller supports a write-back cache policy for cache sizes of 256 Kbytes and 512 Kbytes. Cacheless designs are also supported. The cache memory can be implemented with standard, pipelined burst, or DRAM Cache SRAMs. An external Tag RAM is used for the address tag and an internal Tag RAM for the cache line status bits. For the TVX's DRAM controller, five rows are supported for up to 128 Mbytes of main memory. The Shared Memory Buffer Architecture (SMBA) 2-wire interface allows a graphics controller to use an area of system memory as its frame buffer. The Intel 430VX PCIset has been enhanced through additional buffers, programmable timers, and burst and DWord merging and optimized DRAM timings to maintain a high level of performance when used in a SMBA environment. Using the snoop ahead feature, the TVX allows PCI masters to achieve full PCI bandwidth. The TDXs provide the data paths between the CPU/cache, main memory, and PCI. For increased system performance, the TDXs contain read prefetch and posted write buffers.

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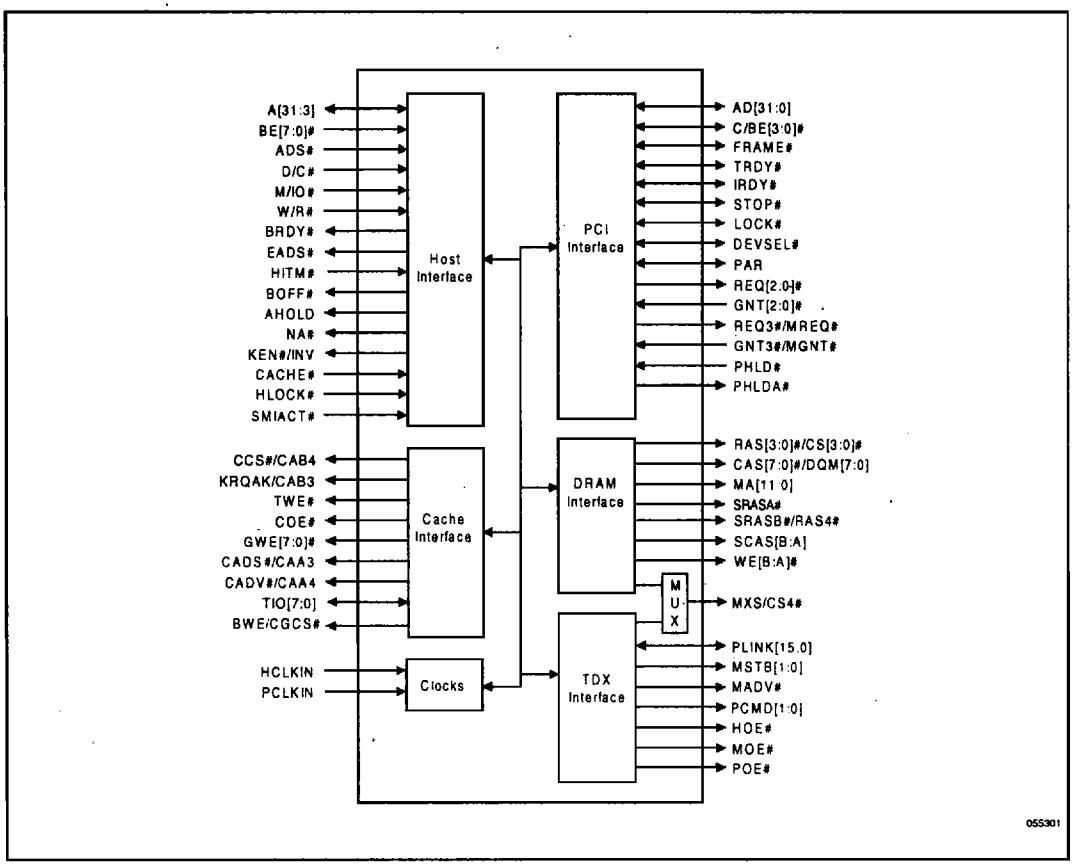
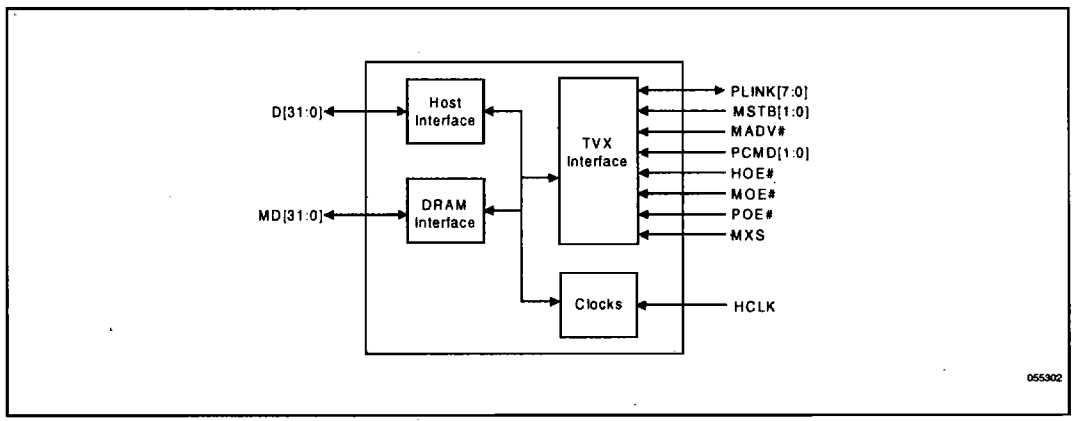


82437VX TVX Simplified Block Diagram



82438VX TDX Simplified Block Diagram

1.0. ARCHITECTURE OVERVIEW OF TSC/TDP

The Intel 430VX PCIset (Figure 1) consists of the 82437VX System Controller (TVX), two 82438VX Data Path (TDX) units, and the PCI IDE ISA Xcelerator (PIIX3). The TVX and two TDXs form a Host-to-PCI bridge. The PIIX3 is a multi-function PCI device providing a PCI-to-ISA bridge, a fast IDE interface, an APIC interface, and a host/hub controller for the Universal Serial Bus (USB). The PIIX3 also provides power management.

The two TDXs provide a 64-bit data path to the host and to main memory and provide a 16-bit data path (PLINK) between the TVX and TDX. PLINK provides the data path for CPU to PCI accesses and for PCI to main memory accesses. The TVX and TDX bus interfaces are designed for 3V and 5V busses. The Intel 430VX PCIset connects directly to the Pentium® processor 3V host bus; The Intel 430VX PCIset connects directly to 5V or 3V main memory DRAMs; and the TVX connects directly to the 5V PCI Bus.

The TVX and TDX interface with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus. The Intel 430VX PCIset implements a Shared Memory Buffer Architecture (SMBA) handshake 2-wire protocol that allows a graphics controller to use a portion of system memory as its frame buffer region. In addition, the PLINK bus is used to connect the PCI bus with the TDX, through the TVX (see Figure 1).

DRAM Interface

The DRAM interface is a 64-bit data path that supports Standard Page Mode (SPM), Extended Data Out (EDO), and Synchronous DRAM (SDRAM) memory. The DRAM interface supports 4 Mbytes to 128 Mbytes of system memory with five RAS lines and also supports symmetrical and asymmetrical addressing for 512Kx32, 1Mx32, 2Mx32, and 4Mx32 deep SIMM modules (single- and double- sided). The TVX supports SDRAM 1Mx 64, 2Mx 64, and 4Mx 64 deep DIMM modules (asymmetrical single- and double- sided). The Intel 430VX PCIset does not support parity and requires that x32 and x64 SIMMs/DIMMs be used.

Second Level Cache

The TVX supports a write-back cache policy providing all necessary snoop functions and inquire cycles. The second level cache is direct mapped and supports both a 256-Kbyte or 512-Kbyte SRAM configuration using pipelined burst, DRAM Cache, or standard SRAMs. DRAM Cache is a DRAM based cache alternative to piplined burst SRAM. Its pinout is a superset of pipeline burst and conforms to the standard pipeline burst footprint. One chipset signal (KRQAK), two system signals (H/WR# and RESET#), and one DRAM Cache specific signal (M/S#) are the only signal differenences between pipeline burst SRAM and DRAM Cache. The Pipeline burst or DRAM Cache configuration performance is 3-1-1-1 for read/write cycles; back-to-back reads can maintain a 3-1-1-1-1-1-1-1 transfer rate.

TDX

Two TDXs create a 64-bit CPU memory data path. The TDXs also interface to the 16-bit PLINK inter-chip bus on the TVX for PCI transactions. The combination of the 64-bit memory path and the 16-bit PLINK bus make the TDXs a cost effective solution, providing optimal CPU-to-main memory performance, while maintaining a small package footprint (100 pins each).

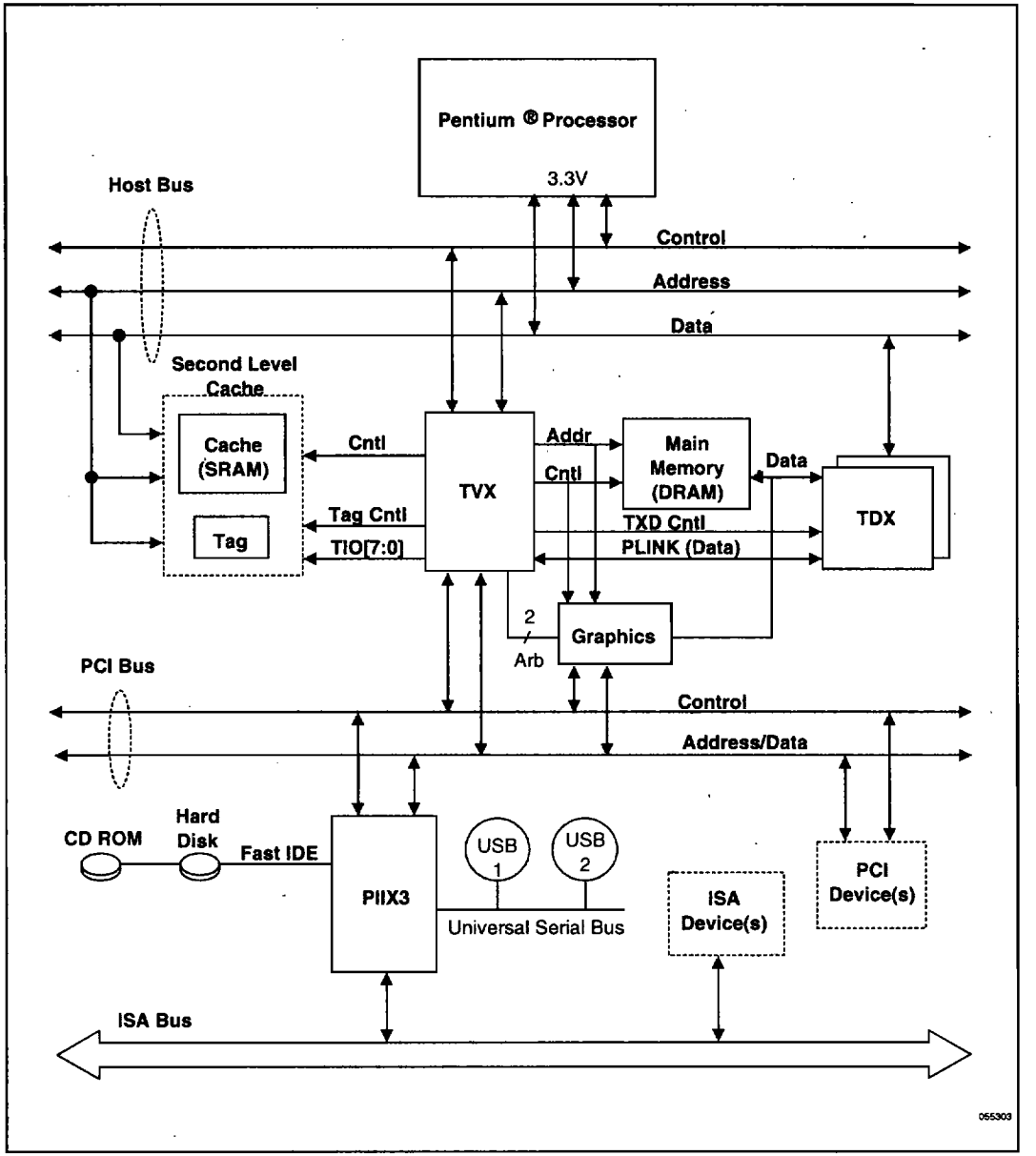


Figure 1. Intel 430VX PCIset System Block Diagram

PCI Interface

The PCI interface is 2.1 compliant and supports up to four PCI bus masters in addition to the PIIX3 bus master requests. The TVX and TDXs together provide the interface between PCI and main memory; however, only the TVX connects to the PCI bus.

Buffers

The TVX and TDXs together contain three sets of buffers for optimizing data flow. A DRAM write buffer is provided for CPU-to-main memory writes, second level cache write-back cycles, and PCI-to-main memory transfers. This buffer is used to achieve 3-1-1-1 posted writes to main memory, and also provides DWord merging and burst merging for CPU to main memory write cycles. Buffering is provided for PCI-to-main memory writes. A buffer is provided for CPU-to-PCI writes to maximize the bandwidth for graphic writes to the PCI bus in a non-SMBA system. In addition, PCI-to-main memory read pre-fetch buffering permits up to two lines of data to be prefetched at an x-2-2-2 rate.

Shared Memory Buffer Architecture (SMBA)

The Intel 430VX PCIset provides a hardware interface that allows a graphics controller to access an area of system memory as a frame buffer. This reduces system cost by eliminating the need to have separate memory for the graphics subsystem. Two signals are used to arbitrate ownership of DRAM (DRAM address and control signals). The Intel 430VX PCIset has been enhanced as follows to maintain a high level of performance when used in a SMBA environment:

- Buffering for improved CPU and PCI posting and PCI pre-fetching
- Programmable timers to maximize performance and establish a balance between the graphics controller and the system (regulates read and write accesses to DRAM)
- Burst merging and DWord merging for efficient DRAM writes
- Optimized DRAM Read timings

System Clocking

The processor, secondary cache, main memory subsystem, and PLINK bus all run synchronously to the host clock. The host clock frequencies supported are 50 MHz, 60 MHz, and 66 MHz. The PCI clock runs synchronously at half the host clock frequency. The TVX and TDXs have a host clock input and the TVX has a PCI clock input. These clocks come from an external source and have a maximum clock skew requirement with respect to each other.

2.0. SIGNAL DESCRIPTION

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used extensively. This is done to avoid confusion when working with a mixture of "active-low" and "active-high" signals. The term **assert**, or **assertion** indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term **negate**, or **negation** indicates that a signal is inactive.

In the Type column 3V/5V indicates that the signal drives 3.3V levels as an output and is 5V tolerant as an input. All 3V outputs can drive 5V TTL inputs. PCI signals are compliant with the PCI 5.0V Signaling Environment DC and AC Specifications.

The following notations are used to describe the signal and type:

I	Input pin
O	Output pin
OD	Open Drain Output pin. This requires a pull-up to the VCC of the processor core
I/O	Bi-directional Input/Output pin

2.1. TVX Signals

2.1.1. HOST INTERFACE

Name	Type	Description
A[31:3]	I/O 3V	**Address Bus.** A[31:3] connects to the address bus of the CPU. During CPU cycles A[31:3] are inputs. The TVX drives A[31:3] during inquire cycles on behalf of PCI initiators. A27 has an internal pulldown resistor.
BE[7:0]#	I 3V	**Byte Enables.** The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes must be provided to the CPU if the cycle is a cacheable read, regardless of the state of BE[7:0]#.
ADS#	I 3V	**Address Status.** The CPU asserts ADS# to indicate that a new bus cycle is being driven.
BRDY#	O 3V	**Bus Ready.** The TVX asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
NA#	O 3V	**Next Address.** When burst SRAMs are used in the second level cache or the second level cache is disabled, the TVX asserts NA# in T2 during CPU write cycles and with the first assertion of BRDY# during CPU line fills. NA# is never asserted if the L2 cache is enabled with asynchronous SRAMs.
AHOLD	O 3V	**Address Hold.** The TVX asserts AHOLD when a PCI initiator is performing a cycle to DRAM. AHOLD is held for the duration of the PCI burst transfer. The TVX negates AHOLD when the completion of the PCI to DRAM read or write cycles complete and during PCI peer transfers.
EADS#	O 3V	**External Address Strobe.** Asserted by the TVX to inquire the first level cache when servicing PCI master references to main memory.

Name	Type	Description
BOFF#	O 3V	**Back Off.** Asserted by the TVX when required to terminate a CPU cycle that was in progress.
HITM#	I 3V	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.
M/IO#, D/C#, W/R#	I 3V	**Memory/IO; Data/Control; Write/Read.** Asserted by the CPU with ADS# to indicate the type of cycle that the system needs to perform.
HLOCK#	I 3V	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic (i.e., no PCI activity to main memory is allowed).
CACHE#	I 3V	**Cacheable.** Asserted by the CPU during a read cycle to indicate the CPU will perform a burst line fill. Asserted by the CPU during a write cycle to indicate the CPU will perform a burst write-back cycle. If CACHE# is asserted to indicate cacheability, the TVX will assert KEN# either with the first BRDY#, or with NA# if NA# is asserted before the first BRDY#.
KEN#/INV	O 3V	**Cache Enable.** KEN#/INV functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV will be driven high during the 1st BRDY# or NA# assertion of a *non-L1-cacheable* CPU read cycle. KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write(read) snoop cycle. Note that KEN#/INV operation during snoop cycles is independent of the FLCE bit programming.
SMIACT#	I 3V	**System Management Interrupt Active.** SMIACT# is asserted by the CPU when it is in system management mode as a result of an SMI. This signal must be sampled active with ADS# for the processor to access the SMM space of DRAM, located at A0000h, after SMM space has been loaded and locked by BIOS at system boot.

NOTES:

All of the signals in the host interface are described in the Pentium processor data sheet. The preceding table highlights Intel 430VX PCIset specific uses of these signals.

2.1.2. DRAM INTERFACE

Name	Type	Description
RAS[3:0]#/ CS[3:0]#	O 3V	**Row Address Strobe(EDO/SPM).** RAS[3:0]# select the DRAM row. **Chip Select (SDRAM).** CS[3:0]# activate the SDRAM to accept any command when it is low.
MXS/**CS4#**	O 3V	**Chip Select 4 (SDRAM).** CS4# is multiplexed with the MXS TVX-to-TDX interface signal. If SDRAM is detected in the 5th ROW at power up, MXS/CS4# becomes CS4#. If EDO/SPM DRAM or no DRAM is detected in the 5th Row, MXS/CS4# becomes MXS. Note: if 5 rows of SDRAM is implemented, MXS at the TDX must be tied high with a 1 KΩ pullup resistor.
CAS[7:0]#/ DQM[7:0]	O 3V	**Column Address Strobe(EDO/SPM).** CAS[7:0]# select which bytes are affected by a DRAM cycle. These signals have internal pullup resistors. **Input/Output Data Mask (SDRAM).** DQM[7:0] act as synchronized output enables during a read cycle and a byte mask during a write cycle. The read cycles require Tdqz clock latency before the functions are actually performed. In case of a write cycle, word mask functions are performed in the same cycle (0 clock latency).
SRASA# SRASB#/ RAS4#	O 3V	**SDRAM Row Address Strobe (SDRAM)/Row address 4.** SRAS[B:A]# latch row address on the positive edge of the clock with SRAS[B:A]# low. These signals enable row access and Precharge. Two copies are provided for loading purposes. If EDO or SPM DRAM is detected in the 5th ROW at power up, SRASB#/RAS4# becomes RAS4#. If SDRAM or no DRAM is detected in the 5th Row, SRASB#/RAS4# becomes SRASB#.
SCAS[B:A]#	O 3V	**SDRAM Column Address Strobe (SDRAM).** SCAS[B:A]# latch column address on the positive edge of the clock with SCAS[B:A]# low. These signals enable column access. Two copies provided for loading purposes.
MA[11:0]	O 3V	**Memory Address (EDO/SPM/SDRAM).** This is the row and column address for DRAM.
WE[B:A]#	O 3V	**Write Enable(EDO/SPM/SDRAM).** This is the write enable pin for the DRAMs. Two copies provided for loading purposes. This signal has an internal pullup resistor.

2.1.3. SECONDARY CACHE INTERFACE

Name	Type	Description
CADV#/ CAA4	O 3V	**Cache Advance/Cache Address 4 (copy A).** This pin has two modes. The CADV# mode is used when the second level cache consists of burst SRAM's. In this mode assertion causes the BSRAM in the secondary cache to advance to the next QWord in the cache line. The CAA4 mode is used when the second level cache consists of standard asynchronous SRAMs. In this mode the signal is used to sequence through the QWords in a cache line during a burst operation.

Name	Type	Description
CADS#/ CAA3	O 3V	**Cache Address Strobe/Cache Address 3 (copy A).** This pin has two modes. The CADS# mode is used when the second level cache consists of burst SRAMs. In this mode assertion causes the BSRAM in the secondary cache to load the BSRAM address register from the BSRAM address pins. The CAA3 mode is used when the second level cache consists of standard asynchronous SRAMs. In this mode the signal is used to sequence through the QWords in a cache line during a burst operation.
KRQAK/ CAB3	I/O 3V	**DRAM Cache Refresh Request and Acknowledge/Cache Address 3 (copy B).** This pin has two modes. One mode is used when the DRAM Cache SRAM is in the system. In this mode, KRQAK is a bidirectional refresh request/acknowledge. The CAB3 function is used when the second level cache consists of standard asynchronous SRAMs. In this mode, CAB3 is used to sequence through the QWords in a cache line during a burst operation. This signal has an internal pulldown resistor.
CCS#/ CAB4	O 3V	**Cache Chip Select/Cache Address (copy B).** A second level cache consisting of burst SRAMs will power up, if necessary, and perform an access if this signal is asserted when CADS# is asserted. A second level cache consisting of burst SRAMs will power down if this signal is negated when CADS# is asserted. When CCS# is negated a second level cache consisting of burst SRAMs ignores ADS#. If CCS# is asserted when ADS# is asserted a second level cache consisting of burst SRAMs will power up, if necessary, and perform an access. CAB4 is used to sequence through the QWords in a cache line during a burst operation when using standard asynchronous SRAM.
COE#	O 3V	**Cache Output Enable.** The secondary cache data RAMs drive the CPUs data bus when COE# is asserted.
GWE#	O 3V	**Global-Write Enable.** When the L2 RAM type is Pipelined Burst, GWE# asserted causes a QWord to be written into the secondary cache data RAMs if they are powered up. It is used for L2 line fills. When the L2 RAM type is standard asynchronous SRAM, GWE# is asserted for all L2 writes, including L2-cacheable CPU writes and L2 line fills.
BWE#/ CGCS#	O 3V	**Byte-Write Enable/Cache Global Chip Select.** When the L2 RAM type is Pipelined Burst, this pin functions as a byte write enable. When GWE#=1, the assertion of BWE# causes the byte lanes that are enabled via the CPU's HBE[7:0]# signals to be written to the secondary cache data RAMs, if they are powered up. Note that HBE[7:0]# are directly connected to the PBSRAMs. When the L2 RAM type is standard asynchronous RAMs, this pin acts as a global chip select. CGCS# is asserted for all L2 reads and L2 line fills. For L2 writes, it is deasserted. Note that some external logic is required for a standard asynchronous SRAM L2 implementation. See the Secondary Cache Interface section.
TIO[7:0]	I/O 3\5V	**Tag Address.** These are inputs during CPU accesses and outputs during second level cache line fills and the second level cache line invalidates due to inquire cycles. TIO[7:0] contain the second level tag address for a 256-Kbyte second level caches. TIO[6:0] contains the second level tag address and TIO7 contains the second level cache valid bit for 512-Kbyte caches. These signals have internal pulldown resistors.
TWE#	O 3V	**Tag Write Enable.** When asserted, new state and tag addresses are written into the external tag.

2.1.4. PCI INTERFACE

Name	Type	Description
AD[31:0]	I/O 3/5V	**Address/Data.** The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks.
C/BE[3:0]#	I/O 3/5V	**Command/Byte Enable.** The command is driven with FRAME# assertion, byte enables corresponding to supplied or requested data is driven on following clocks.
FRAME#	I/O 3/5V	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 3/5V	**Device Select.** This signal is driven by the TVX when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 3/5V	**Initiator Ready.** Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 3/5V	**Target Ready.** Asserted when the target is ready for a data transfer.
STOP#	I/O 3/5V	**Stop.** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 3/5V	**Lock.** Used to establish, maintain, and release resource locks on PCI.
REQ[2:0]#	I 5V	**Request.** PCI master requests for PCI.
REQ3#/ MREQ#	I 5V	**Request.** PCI master requests for PCI. This signal is also multiplexed with the graphics controller DRAM request line.
GNT[2:0]#	O 3V	**PCI Grant.** Permission is given to the master to use PCI.
GNT3#/ MGNT#	O 3V	**PCI Grant.** Permission is given to the master to use PCI. This signal is also multiplexed with the graphics controller DRAM grant line.
PHLD#	I 5V	**PCI Hold.** This signal comes from PIIX3. It is the PIIX3 request for PCI.
PHLDA#	O 3V	**PCI Hold Acknowledge.** This signal is driven by the TVX to grant PCI to PIIX3.
PAR	I/O 3/5V	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].

NOTES:
All signals in the PCI interface conform to the PCI Rev 2.1 specification.

2.1.5. TDX INTERFACE

Name	Type	Description
PLINK[15:0]	I/O 3V	**PCI Link.** This is the data path between the CPU/DRAM and PCI. Each TDX connects to one byte of this bus.
MSTB[1:0]	O 3V	**Memory Strobe.** Controls the data flow and data merging in the DRAM write buffer.
MADV#	O 3V	**Memory Advance.** For memory write cycles, assertion causes a QWord to be drained from the DRAM write buffer and the next data to be made available to the MD pins of the TDXs. For memory read cycles, assertion causes a QWord to be latched into the DRAM input register. It is also used to indicate a PCI to DRAM read.
PCMD[1:0]	O 3V	**PLINK Command.** This field controls how data is loaded into the DRAM to PCI buffer, and PLINK input and output registers.
MXS/CS4#	O 3V	**Mux Select/Chip Select 4 (SDRAM).** When the MXS function is enabled, this signal provides speed path parameters to the TDX for CPU and PCI accesses to/from DRAM. If SDRAM is detected in the 5th ROW at power up, MXS/CS4# becomes CS4#. If EDO/SPM DRAM or no DRAM is detected in the 5th Row, MXS/CS4# becomes MXS. Note: if 5 rows of SDRAM is implemented, MXS at the TDX must be tied high with a 1 KΩ pullup resistor.
HOE#	O 3V	**Host Output Enable.** This signal is used as the output enable for the host data buus.
MOE#	O 3V	**Memory Output Enable.** This signal is used as the output enable for the memory data bus.
POE#	O 3V	**PLINK Output Enable.** This signal is used as the output enable for the PLINK Data Bus and selects the DRAM mux and PLINK input mux.

2.1.6. CLOCK, RESET, AND TEST

Name	Type	Description
HCLKIN	I 3V	**Host Clock In.** This signal pin receives a buffered host clock. This should be the same clock net that is delivered to the CPU (50 MHz, 60 MHz, and 66 MHz frequencies are supported). The TVX internal logic uses this signal.
PCLKIN	I 5V	**PCI Clock In.** This signal pin receives a buffered divide-by-2 host clock. The TVX internal logic uses this signal.
CPURST	I 3V	**Reset.** When asserted, this signal asynchronously resets the TVX. The PCI signals also tri-state compliant to PCI Rev 2.1 specification.

2.2. TDX Signals

2.2.1 Data Interface Signals

2.2.1. DATA INTERFACE SIGNALS

Name	Type	Description
HD[31:0]	I/O 3V	**Host Data.** These signals are connected to the CPU data bus. The CPU data bus is interleaved between the TDX every byte, effectively creating an even and an odd TDX. The TDXs do not need to know which they are.
MD[31:0]	I/O 3\5V	**Memory Data.** These signals are connected to the DRAM data bus. The DRAM data bus is interleaved between the TDXs every byte, effectively creating an even and an odd TDX. The TDXs do not need to know which they are.
PLINK[7:0]	I/O 3V	**PCI Link.** These signals are connected to the PLINK data bus on the TVX. This is the data path between the CPU/DRAM and PCI. PCI to DRAM Reads and CPU to PCI writes are driven onto these pins by the TDX. CPU to PCI reads and PCI to DRAM writes are received on this bus by the TDX. Each TDX connects to one byte of this bus.

2.2.2. TVX INTERFACE SIGNALS

Name	Type	Description
MSTB[1:0]	I 3V	**Memory Strobe.** See TDX Signals in the TVX Signal description.
MADV#	I 3V	**Memory Advance.** See TDX Signals in the TVX Signal description.
MXS	I 3V	**Mux Select.** See TDX Signals in the TVX Signal description.
PCMD[1:0]	I 3V	**PLINK Command.** See TDX Signals in the TVX Signal description.
HOE#	I 3V	**Host Output Enable.** See TDX Signals in the TVX Signal description.
MOE#	I 3V	**Memory Output Enable.** See TDX Signals in the TVX Signal description.
POE#	I 3V	**PLINK Output Enable.** See TDX Signals in the TVX Signal description.

2.2.3. CLOCK SIGNAL

Name	Type	Description
HCLK	I 3V	**Host Clock.** Primary clock input used to drive the part.

2.3. TVX Strapping Pins

Name	Pin Name	Description
SCS	A[31:30]	**Secondary Cache Size** as described in the Cache Control Register (bits [7:6]).
L2RAMT	A[29:28]	**Initial L2 RAM Type** as described in the Cache Control Register (bits [5:4]). There are no pullup/pulldown resistors implemented in the A[29:28] I/O buffers.
FD	A27	**Frequency Detection.** BIOS can use this bit to determine if the system is 60 MHz (external pullup) or 66 MHz (no strapping is present) as described in the DRAM Control Register (bit 0). Bit 0 is initialized with the inverted value of pin A27 after reset negation. The A27 input buffer includes a weak pulldown resistor that forces DDR[0] to default to 1 if no strapping is present.
DCD	KRQAK	**DRAM Cache Detection.** After reset negation, this bit is sampled to detect if DRAM cache L2 is present in the system. A 4.7K pull-up must be connected to the pin, if DRAM cache is in the system. If sampled high, DRAM cache is in the system. A weak pulldown is provided internally on this pin. A configuration bit (bit 5 in the CCE register, 53h) is provided for BIOS detection.

2.4. Signal States During A Hard Reset

The following table shows the state of all TVX and TDX output and bi-directional signals during hard reset (CPURST asserted).

Table 1. Signal State During Hard Reset

Signal	State
TVX	
A[31:27]	Input
A[26:3]	Low
BRDY#	High
NA#	High
AHOLD	High
EADS#	High
BOFF#	High
KEN#/INV	Low
RAS[2:0]#/CS[2:0]#	Low
RAS3#/CS3#	Tri-state
CAS[7:0]#/DQM[7:0]	Tri-state
SRASA#	High
SRASB#/RAS4#	Tri-state
SCASA#	High
SCASB#	Tri-state
MA[11:0]	Tri-state
WEA#	High
WEB#	Tri-state
CADV#/CAA4	High
CADS#/CAA3	High
CCS#/CAB4	Low
KRQAK/CAB3	Input
COE#	High
GWE#	High
BWE#/CGCS#	High

Signal	State
TIO[7:0]	Tri-state
TWE#	Low
AD[31:0]	Low
C/BE[3:0]#	Low
FRAME#	Tri-state
DEVSEL#	Tri-state
IRDY#	Tri-state
TRDY#	Tri-state
STOP#	Tri-state
LOCK#	Tri-state
GNT[2:0]#	Tri-state
GNT3#/MGNT#	Tri-state
PHLDA#	High
PAR	Low
PLINK[15:0]	Tri-state
MSTB[1:0]	Low
MADV#	High
PCMD[1:0]	Low
MXS/CS4#	Tri-state
HOE#	High
MOE#	High
POE#	Low
TDX	
HD[31:0]	Tri-state
MD[31:0]	Tri-state
PLINK[7:0]	Tri-state

3.0. REGISTER DESCRIPTION

The TVX contains two sets of software accessible registers (I/O Mapped and Configuration registers), accessed via the Host CPU I/O address space. The I/O Mapped registers control access to PCI configuration space. Configuration Registers reside in PCI configuration space and specify PCI configuration, DRAM configuration, cache configuration, operating parameters, and optional system features.

The TVX internal registers (both I/O Mapped and Configuration registers) are only accessible by the Host CPU and cannot be accessed by PCI masters. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFADD which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). The following nomenclature is used for access attributes.

RO **Read Only**. If a register is read only, writes to this register have no effect.

R/W **Read/Write**. A register with this attribute can be read and written.

R/WC **Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Some of the TVX registers described in this section contain reserved bits. Software must deal correctly with *fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not* rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.

In addition to reserved bits within a register, the TVX contains address locations in the PCI configuration space that are marked "Reserved" (Table 1). The TVX responds to accesses to these address locations by completing the Host cycle. Software should not write to reserved TVX configuration locations in the device-specific region (above address offset 3Fh).

During a hard reset (CPURST asserted), the TVX sets its internal configuration registers to predetermined **default** states. *The default state represents the minimum functionality feature set required to successfully* bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, cache configuration, operating parameters and optional system features that are applicable, and to program the TVX registers accordingly.

3.1. I/O Mapped Registers

The TVX contains two registers that reside in the CPU I/O address space—the Configuration Address (CONFADD) Register and the Configuration Data (CONFDATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.1.1. CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address:	0CF8h (Accessed as a DWord)
Default Value:	00000000h
Access:	Read/Write

CONFADD is a 32-bit register accessed only when referenced as a DWord. A Byte or Word reference will "pass through" the Configuration Address Register to the PCI Bus. The CONFADD Register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Description
31	**Configuration Enable (CONE).** 1=Enable. 0=Disable.
30:24	**Reserved.**
23:16	**Bus Number (BUSNUM).** When BUSNUM is programmed to 00h, the target of the configuration cycle is either the TVX or the PCI Bus that is directly connected to the TVX, depending on the Device Number field. If the Bus Number is programmed to 00h and the TVX is not the target, a type 0 configuration cycle is generated on PCI. If the Bus Number is non-zero, a type 1 configuration cycle is generated on PCI with the Bus Number mapped to AD[23:16] during the address phase.
15:11	**Device Number (DEVNUM).** This field selects one agent on the PCI Bus selected by the Bus Number. During a Type 1 Configuration cycle, this field is mapped to AD[15:11]. During a Type 0 configuration cycle, this field is decoded and one of AD[31:11] is driven to 1. The TVX is always Device Number 0.
10:8	**Function Number (FUNCNUM).** This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The TVX responds to configuration cycles with a function number of 000b; all other function number values attempting access to the TVX (Device Number = 0, Bus Number = 0) generate a type 0 configuration cycle on the PCI Bus with no IDSEL asserted, which results in a master abort.
7:2	**Register Number (REGNUM).** This field selects one register within a particular bus, device, and function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	**Reserved.**

3.1.2. CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write

CONFDATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Description
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFADD is 1, any I/O reference in the CONFDATA I/O space is mapped to configuration space using the contents of CONFADD.

3.2. PCI Configuration Registers

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported by the Pentium processor, configuration space is not supported. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The TVX only supports Mechanism #1 (both type 0 and 1 accesses). Table 1 shows the TVX configuration space.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register, a DWord I/O write cycle is used to place a value into CONFADD that specifies the PCI Bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. Then, CONFDATA becomes a window onto four bytes of configuration space specified by the contents of CONFADD. Read/write accesses to CONFDATA generates a PCI configuration cycle to the address specified by CONFADD.

Type 0 Access: If the Bus Number field of CONFADD is 0, a type 0 configuration cycle is generated on PCI. CONFADD[10:2] is mapped directly to AD[10:2]. The Device Number field of CONFADD is decoded onto AD[31:11]. The TVX is Device #0 and does not pass its configuration cycles to PCI. Thus, AD11 is never asserted. (For accesses to device #1, AD12 is asserted, etc., to Device #20 which asserts AD31.) Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which results in a master abort.

Type 1 Access: If the Bus Number field of CONFADD is non-zero, a type 1 configuration cycle is generated on PCI. CONFADD[23:2] are mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

Table 2. TVX Configuration Space

Address	Mnemonic	Register Name	Access
00–01h	VID	Vendor Identification	RO
02–03h	DID	Device Identification	RO
04–05h	PCICMD	Command Register	R/W
06–07h	PCISTS	Status Register	RO, /WC
08h	RID	Revision Identification	RO
09–0Bh	CLASSC	Class Code	RO
0Ch	—	Reserved	—
0Dh	MLT	Master Latency Timer	R/W
0Eh	HEDT	Header Type	RO
0Fh	BIST	BIST Register	R/W
10–4Eh	—	Reserved	—
4Fh	ACON	Arbitration Control	R/W
50h	PCON	PCI Control	R/W
51h	—	Reserved	—
52h	CC	Cache Control	R/W
53h	CCE	Cache Control Extended	R/W

Table 2. TVX Configuration Space

Address	Mnemonic	Register Name	Access
54–55h	SDRAMC	SDRAM Control	R/W
55h	—	Reserved	—
56h	DRAMEC	DRAM Extended Control	R/W
57h	DRAMC	DRAM Control	R/W
58h	DRAMT	DRAM Timing	R/W
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	R/W
60–64h	DRB[3:0]	DRAM Row Boundary (5 registers)	R/W
65–66h	—	Reserved	—
67h	DRTH	DRAM Row Type High	R/W
68h	DRT	DRAM Row Type Low	R/W
69h	TRDT	PCI TRDY Timer	R/W
70h	MTT	Multi-Transaction Timer	R/W
71h	—	Reserved	—
72h	SMRAM	System Management RAM Control	R/W
73h	SMBCR	Shared Memory Buffer Control	R/W
74h	SMBSA	Shared Memory Buffer Start Address	R/W
76–77h	—	Reserved	—
78h	GCRLT	Graphics Controller Latency Timers	R/W
79–FFh	—	Reserved	—

3.2.1. VID—VENDOR IDENTIFICATION REGISTER

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number.** This is a 16-bit value assigned to Intel.

3.2.2. DID—DEVICE IDENTIFICATION REGISTER

Address Offset: 02–03h
Default Value: 7030h
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number.** This is a 16-bit value assigned to the TVX.

3.2.3. PCICMD—PCI COMMAND REGISTER

Address Offset: 04–05h
Default: 0006h
Access: Read/Write

This 16-bit register provides basic control over the TVX's ability to respond to PCI cycles. The PCICMD Register in the TVX enables and disables the assertion of SERR# and PCI master accesses to main memory.

Bit	Descriptions
15:10	**Reserved.**
9	**Fast Back-to-Back (FB2B). (Not Implemented)** This bit is hardwired to 0.
8	**SERR# Enable (SERRE). (Not Implemented)** This bit is hardwired to 0.
7	**Address/Data Stepping. (Not Implemented)** This bit is hardwired to 0.
6	**Parity Error Enable (PERRE). (Not Implemented)** This bit is hardwired to 0.
5	**Video Pallet Snooping (VPS). (Not Implemented)** This bit is hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE). (Not Implemented)** This bit is hardwired to 0. The TVX will never use the Memory Write and Invalidate PCI command.
3	**Special Cycle Enable (SCE). (Not Implemented)** This bit is hardwired to 0, as the TVX does not respond to PCI special cycles.
2	**Bus Master Enable (BME). (Not Implemented)** The TVX does not support disabling of its bus master capability on the PCI Bus. This bit is hardwired to 1.
1	**Memory Access Enable (MAE).** 1=Enable PCI master access to main memory, if the PCI address selects enabled DRAM space; 0=Disable (TVX does not respond to main memory accesses).
0	**I/O Access Enable (IOAE). (Not Implemented)** This bit is hardwired to 0. The TVX does not respond to PCI I/O cycles.

3.2.4. PCISTS—PCI STATUS REGISTER

Address Offset: 06–07h
Default Value: 0200h
Access: Read Only, Read/Write Clear

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort. PCISTS also indicates the DEVSEL# timing that has been set by the TVX hardware.

Bit	Descriptions
15	**Detected Parity Error (DPE). (Not Implemented)** This bit is hardwired to 1.
14	**Signaled System Error (SSE). (Not Implemented)** This bit is hardwired to 0.
13	**Received Master Abort Status (RMAS)—R/WC.** When the TVX terminates a Host-to-PCI transaction (TVX is a PCI master) with an unexpected master abort, this bit is set to 1. Note that master abort is the normal and expected termination of PCI special cycles. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS)—R/WC.** When a TVX-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. Software resets RTAS to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS). (Not Implemented)** This bit is hardwired to 0. The TVX never terminates a PCI cycle with a target abort.
10:9	**DEVSEL# Timing (DEVT)—RO.** This 2-bit field indicates the timing of the DEVSEL# signal when the TVX responds as a target, and is hard-wired to the value 01b (medium) to indicate the slowest time that DEVSEL# is generated.
8	**Data Parity Detected (DPD). (Not Implemented)** This bit is hardwired to 0.
7	**Fast Back-to-Back (FB2B). (Not Implemented)** This bit is hardwired to 0.
6	**User Defined Format (UDF). (Not Implemented)** This bit is hardwired to 0.
5	**66 MHz PCI Capable (66C). (Not Implemented)** This bit is hardwired to 0.
4:0	**Reserved.**

3.2.5. RID—REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: 00h (A0 stepping)
Access: Read Only

This register contains the revision number of the TVX. These bits are read only and writes to this register have no effect. For the A-0 Stepping, this value is 00h.

Bit	Description
7:0	**Revision Identification Number.** This is an 8-bit value that indicates the revision identification number for the TVX.

3.2.6. CLASSC—CLASS CODE REGISTER

Address Offset: 09–0Bh
Default Value: 060000h
Access: Read Only

This register contains the device programming interface information related to the Sub-Class code and Base-Class code definition for the TVX. This register also identifies the Base-Class code and the function Sub-Class in relation to the Base-Class code.

Bit	Description
23:16	**Base-Class Code (BCC).** 06=Bridge device.
15:8	**Sub-Class Code (SCC).** 00h=Host bridge.
7:0	**Programming Interface (PI).** 00h = Hardwired as a host-to-PCI bridge.

3.2.7. HEDT—HEADER TYPE REGISTER

Address Offset: 0Eh
Default Value: 00h
Access: Read Only

The Header Type Register identifies the TVX as a single-function device.

Bit	Description
7:0	**Device Type (DEVICET).** 00h=Single-function PCI device.

3.2.8. MLT—MASTER LATENCY TIMER REGISTER

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write

MLT is an 8-bit register that controls the amount of time the TVX, as a bus master, can burst data on the PCI Bus. The Count Value is an 8-bit quantity. However, MLT[2:0] are hardwired to 0. MLT is used to guarantee the host CPU a minimum amount of the system resources as described in the PCI Bus Arbitration section.

Bit	Description
7:3	**Master Latency Timer Count Value.** The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks) allotted to the TVX, after which it must surrender the bus as soon as other PCI masters request the bus. The default value of MLT is 00h or 0 PCI clocks.
2:0	**Reserved.** Hardwired to 0.

3.2.9. BIST—BIST REGISTER

Address Offset: 0Fh
Default Value: 00h
Access: Read/Write

The Built In Self Test (BIST) function is not supported by the TVX. Writes to this register have no affect.

Bit	Descriptions
7	**BIST Supported—RO.** 0=Disable the BIST function.
6	**Start BIST.** This function is not supported and writes have no affect.
5:4	**Reserved.**
3:0	**Completion Code—RO.** This field always returns 0 when read and writes have no affect.

3.2.10. ACON—ARBITRATION CONTROL REGISTER

Address Offset: 4Fh
Default Value: 00h
Access: Read/Write

The ACON Register enables and disables features related to PCI arbitration and PCI 2.1 compliance.

Bit	Description
7	**Extended CPU-to-PIIX PHLDA# Signaling Enable (XPLDE).** When XPLDE=1, the TVX adds the following additional signalling to singal PHLDA# (i.e., in addition to the normal CPU/PIIX PHOLD/PHLDA# protocol): 1. When the TVX begins a PCI read/write transaction, it asserts PHLDA# for 1 PCLK within the address phase of the transaction. 2. If the CPU is attemp[ting a LOCKed cycle and lock has been established (i.e., PLOCK# was negated in the address phase), PHLDA# remains asserted for one additional clock following the address phase.
6:4	**Reserved.**
3	**CPU Priority Enable (CPE).** 1=CPU gets PCI Bus after two PCI slots (SMBA design). 0=three PCI slots (Non-SMBA design).
2:0	**Reserved.**

3.2.11. PCON—PCI CONTROL

Address Offset: 50h
Default Value: 00h
Access: Read/Write

The PCON Register enables/disables features related to PCI Bus that is not already covered in the required PCI configuration space.

Bit	Description
7:4	**Reserved.**
3	**PCI Concurrency Enable (PCE).** 1 = CPU can access DRAM and L2 while a non-PIIX3 PCI master is targeting peer PCI devices. 0 (default) = CPU is held off of the bus during all PCI master cycles. This bit should be set to 1 by the BIOS during normal operation.
2:0	**Reserved.**

3.2.12. CC—CACHE CONTROL REGISTER

Address Offset: 52h
Default Value: SSSS0010 (S = Strapping option)
Access: Read/Write

This 8-bit register defines the secondary cache operations. The CC Register enables/disables the second level cache, adjusts cache size, selects the cache write policy, selects the caching policy when CACHE# is negated on reads, informs the TVX how the SRAMs are connected, and defines the cache SRAM type. After a hard reset, CC[7:4] reflect the signal levels on the Host address lines A[31:28].

Bit	Description
7:6	**Secondary Cache Size (SCS).** This field reflects the inverted signal level on the A[31:30] pins at the rising edge of the CPURST signal. The default values can be overwritten with subsequent writes to the CC Register. The options are: **Bits[7:6] Secondary Cache Size** 0 0 Cache not populated 0 1 256 Kbytes 1 0 512 Kbytes 1 1 Reserved 1. When SCS=00, the secondary cache is disabled. 2. To enable the L2 cache, SCS must be non-zero and the FLCE bit must be 1. (L2 cache cannot be enabled unless the L1 cache is also enabled)

Bit	Description
5:4	**L2 RAM Type (L2RAMT).** This field reflects the inverted signal level on the A[29:28] pins at the rising edge of the CPURST signal. The reset values can be overwritten with subsequent writes to the CC Register. The options are: **Bits[5:4] SRAM Type** 0 0 Pipelined Burst SRAM or DRAM Cache 0 1 Reserved 1 0 Async SRAM 1 1 Two banks of Pipelined Burst SRAM or DRAM Cache **NOTE** When 512K Pipelined Burst SRAM L2 mode is selected (via SCS and L2RAMT), NA# is delayed one HCLK during burst reads from L2 to ensure that the active bank is not deselected too early by pipelining a cycle to the opposite bank. It is an illegal combination to use asynchronous SRAMs with SDRAMs. BIOS should ensure this combination is not selected when programming this register.
3	**NA Disable (NAD).** When NAD=1, the TVX's NA# pin is never asserted. When NAD=0, NA# assertion is dependent on the cache type and size selected (via SRAMT[SCS]). Note that NAD must be set to 1 if the NA pin of the TVX is not connected to the processor. This bit should be reset to 0 for normal operation in systems that connect NA# to the processor.
2	**Reserved.**
1	**Secondary Cache Force Miss or Invalidate (SCFMI).** When SCFMI=1, the L2 hit/miss detection is disabled, and all tag lookups result in a miss. If the L2 is enabled, the cycle is processed as a miss. If the L2 is populated but disabled (FLCE=0) and SCFMI=1, any CPU read cycle invalidates the selected tag entry. When SCFMI=0, normal L2 cache hit/miss detection and cycle processing occurs. Software can flush the cache (cause all modified lines to be written back to main memory) by setting SCFMI to 1 with the L2 cache enabled (SCS≠00 and FLCE=1), and reading all L2 cache tag address locations.
0	**First Level Cache Enable (FLCE):** FLCE enables/disables the first level cache. When FLCE=1, the TVX responds to CPU cycles with KEN# asserted for cacheable memory cycles. When FLCE=0, KEN# is always negated and line fills to either the first level or L2 cache are prevented. Note that, when FLCE=1 and SCFMI=1, writes to the cache are also forced as misses. Thus, it is possible to create incoherent data between main memory and the L2 cache. A summary of FLCE/SCFMI bit interactions is as follows: **FLCE SCFMI L2 Cache Result** 0 0 Disabled 0 1 Disabled; tag invalidate on reads 1 0 Normal L2 cache operation (dependent on SCS) 1 1 Enabled; miss forced on reads/writes

3.2.13. CCE—CACHE CONTROL EXTENDED REGISTER

Address Offset: 53h
Default Value: 14h
Access: Read/Write (bit 5 is read only)

This register defines the refresh rate, in HCLKs, for the DRAM Cache implementation. The register also provides a read only bit for DRAM Cache presence detection. The value of this bit directly reflects the strapping on the KRQAK pin, as determined at reset.

Bit	Description
7:6	**Reserved.**
5	**DRAM Cache Detect (DCD)—RO.** 1 = DRAM Cache present. 0=DRAM Cache not present. This read only bit directly reflects the strapping on the KRQAK pin, as determined at reset.
4:0	**DRAM Cache Refresh Timer (DCRT) —R/W.** These bits determine the time TVX remains idle, in HCLks, during a DRAM cache refresh sequence. The default value sets the refresh timer to 20 HCLKs.

3.2.14. SDRAMC—SDRAM CONTROL REGISTER

Address Offset: 54–55h
Default Value: 0000h
Access: Read/Write

This register controls the SDRAM mode, CAS# latency, RAS# timing, and SDRAM Turbo enable/disable.

Bit	Description
15:9	**Reserved.**
8:6	**Special SDRAM Mode Select (SSMS).** This field selects 1 of 4 special SDRAM modes used for testing and initialization. The NOP command must be programmed first before any other command can be issued. After the DRAM detection process has completed, bits [8:6] must remain at "000" during normal DRAM operation. **Bits [8:6] Mode** 000 **Normal SDRAM mode (default).** 001 **NOP Command Enable (NOPCE).** Forces all CPU cycles to DRAM to generate a SDRAM NOP command on the memory interface. 010 **All Banks Precharge Command Enable (ABPCE).** CPU cycles to DRAM are converted to an all banks precharge command on the memory interface. 011 **Mode Register Command Enable (MRCE).** CPU cycles to DRAM are converted to MRS commands to the memory interface. The command is driven on the MA[11:0] lines: MA[2:0]=010 for burst of 4 mode, MA3=1 for interleave wrap type mode. MA4=the value in the CAS# Latency bit, MA[6:5]=01, and MA[11:7]=00000. BIOS selects an appropriate host address for each Row of memory such that the right commands are generated on the Memory Address MA[11:0] lines. BIOS needs to be cognizant of the mapping of the host addresses to memory addresses (e.g., a hostaddress of 1D0h sets up the Mode registers in Row 0 of SDRAM with Burst length of 4, Wrap type of interleaved. and CAS latency of 3). 100 **CBR Cycle Enable(CBRC).** 100= CPU cycles to DRAM are converted to SDRAM CBR refresh cycles on the memory interface. 101 **Reserved** 11X **Reserved**
5	**Reserved.**
4	**CAS# Latency (CL).** 1=CAS# latency of 2 for all SDRAM cycles. 0=CAS# latency of 3. RAS# to CAS# delay is also controlled by this bit. When programmed for 2 clock CAS# latency, a RAS# to CAS# delay of 2 HCLKs is provided. When programmed for 3 clock CAS# latency, a RAS# to CAS# delay of 3 HCLKs is provided.
3	**RAS# Timing (RT).** This bit controls RAS# precharge, RAS# active to precharge time and Refresh to RAS# active delay (in HCLKs): **Bit3 RAS# precharge RAS# active to precharge Refresh to RAS# active** 0 3 5 8 1 3 4 7
2:0	**Reserved.**

The following table lists the CAS# latency, RAS# precharge, RAS# active to precharge, and refresh to RAS# active requirements for the various speed grades.

Table 3. SDRAM Timing Values vs Speed Upgrades

Speed Grade (MHz)	CAS# Latency HLCKs	Frequency (Mhz)	RAS# Precharge Required (Trp)	RAS# Active to Precharge Required (Tras)	Refresh to RAS# Active Required (Trc)
66.67 MHz	3	50/60/66 MHz	3 HCLKs	5 HCLKs	8 HCLKs
66.67 MHz	2	50/60/66 MHz	3 HCLKs	5 HCLKs	8 HCLKs
50 MHz	2	50 MHz	3 HCLKs	4 HCLKs	7 HCLKs

3.2.15. DRAMEC—DRAM EXTENDED CONTROL REGISTER

Address Offset: 56h
Default Value: 52h
Access: Read/Write

This 8-bit register contains additional controls for main memory DRAM operating modes and features.

Bit	Description
7	**Reserved.**
6	**Refresh RAS# Assertion (RRA).** 1=5 clocks (default). 0=4 clocks. This bit controls the number of clocks RAS# is asserted for Refresh cycles.
5	**Fast EDO Path Select(FEPS).** When FEPS=1, a fast path is selected for CPU-to-DRAM read cycles for the leadoff. This is valid for EDO DRAMs only in both a cache and a cacheless system. The fast path is selected by assertion of MXS pin. This result in a 1 HCLK pull-in for all read leadoff latencies for EDO DRAMs. (i.e., Page hits, Page misses and Row Misses). The selection of the Fast Path for the burst cycles depends on the value of DRAM Read Burst Timing (DRBT). The Fast Path is selected for the Burst cycles only if DRBT =10 (x222). The slow path is selected for the burst cycles if DRBT = 11 (x322). The FEPS bit should not be set to 1 by BIOS if the EDO Burst rate is either x333, x444, or Asynchronous cache is in the system.
4	**Speculative Leadoff Disable (SLD).** 1= Speculative leadoff disabled (default) . 0= Speculative leadoff enabled. This bit defaults to 1 (disabled), and should be set to 0 in a system without an L2 cache. In a system with an L2 cache, this bit should be set to 1.
3	**Reserved.**
2:1	**Memory Address Drive Strength (MAD).** This field controls the strength of the output buffers driving the MA pins. If one or two rows of memory are populated, set this field to 01 (10 mA). Otherwise, set the field to 10 (16 mA). **Bit [2:1] MA[11:0]** 00 Reserved 01 10 mA (default) 10 16 mA 11 Reserved
0	**DRAM Symmetry Detect Mode (DSDM).** If set to 1, this bit forces some of the MA lines to a fixed value to allow software to detect DRAM symmetry type on a row by row basis.

3.2.16. DRAMC—DRAM CONTROL REGISTER

Address Offset: 57h
Default Value: 01h
Access: Read/Write

This 8-bit register controls main memory DRAM operating modes and features.

Bit	Description
7:6	**Hole Enable (HEN).** This field enables a memory hole in DRAM space. CPU cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole are ignored by the TVX (no DEVSEL#). Note that a selected hole is not remapped. Also, note that this hole enable overrides the SMBA address range if any overlap occurs. (i.e., The hole will exist within the SMBA range). **Bits[7:6] Hole Enabled** 00 None 01 512 Kbytes – 640 Kbytes 10 15 Mbytes – 16 Mbytes 11 14 Mbytes – 16 Mbytes
5:4	**Reserved.**
3	**EDO Detect Mode Enable (EDME).** This bit, if set to a 1, enables a special timing mode for BIOS to detect EDO DRAM type on a bank-by-bank basis. Once all DRAM row banks have been tested for EDO, the EDME bit should be set to 0. Otherwise, performance will be seriously impacted.
2:0	**DRAM Refresh Rate (DRR).** The DRAM refresh rate is adjusted according to the frequency selected by this field. Note that refresh is also disabled via this field, and that disabling refresh results in the eventual loss of DRAM data. **Bits[2:0] Host Bus Frequency** 000 Refresh Disabled 001 50 MHz 010 60 MHz 011 66 MHz 1XX Reserved DRR(0) is initialized to the inverted signal level on A27 at the rising edge of reset. Since the A27 pin contains an internal weak pull-down, unless an external resistor exists, the field will be initialized identical to the 82430FX PCIset. Subsequent writes to this field will override the reset strap value. BIOS can use the value in DRR[0] to determine if the system is 60 MHz (external pullup) or 66 MHz (no strapping).

3.2.17. DRAMT—DRAM TIMING REGISTER

Address Offset: 58h
Default Value: 00h
Access: Read/Write

This 8-bit register controls main memory DRAM timings. For SDRAM specific timing control, see the SDRAMC register.

Bit	Description
7	**Fast MA to RAS# Delay (FMRD).** 1=1 clock (MA setup to RAS# assertion). 0=2 clocks. The DRAM Row Miss timings are controlled by FMRD. Note that FMRD timing adjustments are independent of DLT timing adjustment.
6:5	**DRAM Read Burst Timing (DRBT).** The DRAM read burst timings are controlled by the DRBT field. Slower rates may be required in certain system designs to support layouts with longer trace lengths or slower memories. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-bank basis, as indicated by the DRT register. The x322 timings for EDO burst rate should be used only when FEPS=1 (DRAMEC register) and the timings for the EDO Burst rate for X222 have a negative margin. This forces the MXS to be negated after the leadoff, thus, selecting the fast path for the leadoff and the slow path for the Burst cycles. When FEPS=1 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the fast path for both leadoff and the burst cycles. When FEPS=0 and the EDO Burst rate is set to x222, the EDO read cycle is selected through the slow path for both leadoff and the burst cycles. **DRBT** — **EDO Burst Rate** — **SPM Burst Rate** 00 — x444 — x444 01 — x333 — x444 10 — x222 — x333 11 — x322 — x333 **NOTE** For systems with five rows of memory, at 66 MHz with 60 ns memory or 60 MHz with 70 ns memory, the DRBT field must be set to 01.
4:3	**DRAM Write Burst Timing (DWBT).** The DRAM write burst timings are controlled by the DWBT field. Slower rates may be required in certain system designs to support layouts with longer trace lengths or slower memories. Most system designs will be able to use one of the faster burst mode timings. **DWBT** — **EDO/SPM Burst Rate** 00 — x444 01 — x333 10 — x222 11 — Reserved
2	**Fast RAS to CAS Delay (FRCD).** 1=2 clocks (RAS active to CAS active delay). 0=3 clocks. The DRAM row and page miss leadoff timings are controlled by the FRCD bit. The slower timing may be required in certain system designs to support layouts with longer trace lengths or slower memories. Note that FRCD timing adjustments are independent to DLT timing adjustments.

Bit	Description
1:0	**DRAM Leadoff Timing (DLT).** The DRAM leadoff timings are controlled by the DLT bits. Slower leadoffs may be required in certain system designs to support layouts with longer trace lengths or slower memories. The row miss leadoff timings are summarized below for EDO/SPM reads and writes. Changing DLT effects the Row Miss and Page Miss timings only (e.g., DLT=01 is one clock faster than DLT=00 on Row Miss and Page Miss timings). These bits control MA setup to CAS# assertion. DLT does not effect page hit timings (e.g., DLT=00 or DLT=01 have same page hit timings for reads and writes; e.g., for reads it would be (10-3 = 7) clocks for DLT=00 or DLT=01). **DLT — Read Leadoff — Write Leadoff — RAS# Precharge** 00 — 11 — 7 — 3 01 — 10 — 6 — 3 10 — 11 — 7 — 4 11 — 10 — 6 — 4 FRCD, SLE, FEPS and FMRD bits have cumulative effect on the leadoff timings. The above leadoff represent timings with FRCD=0, SLE=0, FEPS=0 and FMRD = 0. Refer to the "EDO/SPM leadoff timing calculation" table under DRAM Performance Section to see the effect of these bits on the leadoff.

3.2.18. PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0])

Address Offset: PAM0 (59h) —PAM6 (5Fh)
Default Value: 00h
Attribute: Read/Write

The TVX allows programmable memory and cacheability attributes on 14 memory segments of various sizes in the 640-Kbyteto 1-Mbyte address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Three bits are used to specify L1 cacheability and memory attributes for each memory segment. These attributes are:

RE **Read Enable.** When RE=1, the CPU read accesses to the corresponding memory segment are directed to main memory. Conversely, when RE=0, the CPU read accesses are directed to PCI.

WE **Write Enable.** When WE=1, the CPU write accesses to the corresponding memory segment are directed to main memory. Conversely, when WE=0, the CPU write accesses are directed to PCI.

CE **Cache Enable.** When CE=1, the corresponding memory segment is L1 cacheable. CE must not be set to 1 when RE is reset to 0 for any particular memory segment. When CE=1 and WE=0, the corresponding memory segment is cached in the first level cache only on CPU code read cycles.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE=1 and WE=0, the segment is Read Only. The characteristics for memory segments with these read/write attributes are described in Table 4.

Table 4. Attribute Definition

Read/Write Attribute	Definition
Read Only	Read cycles: CPU cycles are serviced by the DRAM in a normal manner. Write cycles: CPU initiated write cycles are ignored by the DRAM interface as well as the cache. Instead, the cycles are passed to PCI for termination. Areas marked as Read Only are L1 cacheable for Code accesses only. These regions are not cached in the second level cache.
Write Only	Read cycles: All read cycles are ignored by the DRAM interface as well as the second level cache. CPU-initiated read cycles are passed onto PCI for termination. The write only state can be used while copying the contents of a ROM, accessible on PCI, to main memory for shadowing, as in the case of BIOS shadowing. Write cycles: CPU write cycles are serviced by the DRAM and L2 cache in a normal manner.
Read/Write	This is the normal operating mode of main memory. Both read and write cycles from the CPU and PCI are serviced by the DRAM and L2 cache interface.
Disabled	All read and write cycles to this area are ignored by the DRAM and cache interface. These cycles are forwarded to PCI for termination.

Each PAM Register controls two regions, typically 16 Kbytes in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in Table 5.

PCI master access to DRAM space is also controlled by the PAM Registers. When the PAM programming indicates a region is writeable, PCI master writes are accepted (DEVSEL# generated). When the PAM programming indicates a region is readable, PCI master reads are accepted. When a PCI write to a non-writeable DRAM region, or a PCI read to a non-readable DRAM region is seen, the TVX does not accept the cycle (DEVSEL# is not asserted). PCI master accesses to enable memory hole regions are not accepted.

Table 5. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Cache Enable	Bits [5, 1] Write Enable	Bits [4, 0] Read Enable	Description
x	x	0	0	DRAM disabled, accesses directed to PCI
x	0	0	1	read only, DRAM write protected, non-cacheable
x	1	0	1	read only, DRAM write protected, L1 cacheable for code accesses only
x	0	1	0	write only
x	0	1	1	read/write, non-cacheable
x	1	1	1	read/write, cacheable

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process the BIOS can be shadowed in main memory to increase the system performance. When a BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The CPU then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

Table 6. PAM Registers and Associated Memory Segments

PAM Reg	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	CE	WE	RE	0F0000–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	CE	WE	RE	0C0000–0C3FFFh	ISA Add-on BIOS	5Ah
PAM1[7:4]	R	CE	WE	RE	0C4000–0C7FFFh	ISA Add-on BIOS	5Ah
PAM2[3:0]	R	CE	WE	RE	0C8000–0CBFFFh	ISA Add-on BIOS	5Bh
PAM2[7:4]	R	CE	WE	RE	0CC000–0CFFFFh	ISA Add-on BIOS	5Bh
PAM3[3:0]	R	CE	WE	RE	0D0000–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	CE	WE	RE	0D4000–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	CE	WE	RE	0D8000–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	CE	WE	RE	0DC000–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	CE	WE	RE	0E0000–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	CE	WE	RE	0E4000–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	CE	WE	RE	0E8000–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	CE	WE	RE	0EC000–0EFFFFh	BIOS Extension	5Fh

NOTE:
The CE bit should not be changed while the L2 cache is enabled.

DOS Application Area (00000–9FFFh)
Read, write, and cacheability attributes are always enabled and are not programmable for the 0 - 640-Kbyte DOS application region.

Video Buffer Area (A0000–BFFFFh)
This 128-Kbyte area is not controlled by attribute bits. CPU-initiated cycles in this region are always forwarded to PCI for termination. This area is not cacheable.

Expansion Area (C0000–DFFFFh)
This 128-Kbyte area is divided into eight 16-Kbyte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Memory that is disabled is not remapped. Cacheability status can also be specified for each segment.

Extended System BIOS Area (E0000–EFFFFh)
This 64-Kbyte area is divided into four 16-Kbyte segments. Each segment can be assigned independent cacheability, read, and write attributes. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000–FFFFFh)
This area is a single 64-Kbyte segment. This segment can be assigned cacheability, read, and write attributes. When disabled, this segment is not remapped.

Extended Memory Area (100000–FFFFFFFFh)
The extended memory area can be split into several parts;

- Flash BIOS area from 4 Gbytes to 4 Gbytes minus 512 Kbytes (aliased on ISA at 16 Mbytes minus 15.5 Mbytes)
- DRAM Memory from 1 Mbyte to a maximum of 512 Mbytes
- PCI Memory space from the top of DRAM to 4 Gbytes minus 512 Kbytes

On power-up or reset the CPU vectors to the Flash BIOS area, mapped in the range of 4 Gbytes to 4 Gbytes minus 512 Kbytes. This area is physically mapped on the expansion bus. Since these addresses are in the upper 4-Gbyte range, the request is directed to PCI.

The DRAM memory space can occupy extended memory from a minimum of 1 Mbyte up to 512 Mbytes. This memory is cacheable. PCI memory space from the top of main memory to 4 Gbytes is always non-cacheable.

3.2.19. DRB—DRAM ROW BOUNDARY REGISTERS

Address Offset: 60h (DRB0)—64h (DRB4)
Default Value: 02h
Access: Read/Write

The TVX supports 5 rows of DRAM. Each row is 64 bits wide. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 4-Mbyte granularity. If the 5th row is implemented, it must be fixed at 8MB (using 1Mx16 devices), in a SMBA system and can be set to either 8MB (using 1Mx16 deivces) or 16MB (using 2Mx8 devices), in a non-SMBA system. Refer to the 5th row discussion in the DRAM section for addtional information on 5th Row support.

DRB0 = Total amount of memory in row 0 (in 4 Mbytes)
DRB1 = Total amount of memory in row 0 + row 1 (in 4 Mbytes)
DRB2 = Total amount of memory in row 0 + row 1 + row 2 (in 4 Mbytes)
DRB3 = Total amount of memory in row 0 + row 1 + row 2 + row 3 (in 4 Mbytes)
DRB4 = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in 4 Mbytes)

The DRAM array can be configured with 512kx32, 1Mx32, 2Mx32, and 4Mx32, SIMMs. Each register defines an address range that causes a particular RAS# line to be asserted (e.g. if the first DRAM row is 8 Mbytes in size, then accesses within the 0 to 8-Mbyte range causes RAS0# to be asserted).

Bit	Description
7:6	**Reserved.**
5:0	**Row Boundary Address.** This 6-bit value is compared against address lines A[27:22] to determine the upper address limit of a particular row. (i.e., DRB minus previous DRB = row size).

Row Boundary Address

These 6-bit values represent the upper address limits of the 4 rows (i.e., this row minus previous row = row size). Unpopulated rows have a value equal to the previous row (row size = 0). DRB4 reflects the maximum amount of DRAM in the system. The top of memory is determined by the value written into DRB4. DRB4 should not be programmed to a value greater than 128 Mbytes.

Note that the total memory supported is limited to 128 Mbytes even though it is possible to populate the 5 rows with up to 160 Mbyte. This limit must be ensured by the system BIOS. If the system detects more than 128 Mbytes in a SMBA system, then it must program one of the DRB's [3:0], except DRB4, with a lesser value so that the total system memory adds up to 128 Mbyte. In a non-SMBA system (5th row fixed at 8

Mbyte), memory may be trimmed from any DRAM row in order to bring the total to 128 Mbytes or less. When possible, BIOS should take away from the slowest DRAM row in a 5 row mixed FPM/EDO system. In a non-SMBA system (5th row fixed at 16 Mbytes), the BIOS must disable the 5th row of memory.

NOTE

The Intel 430VX PCIset only supports the 5th row fixed at 8 Mbyte, in a SMBA system.

Example #1 (memory exceeding 128 Mbytes)

Five DRAM row ,SMBA system: The first 4 rows have 32 Mbytes each and the 5th row has 8 Mbytes of memory for a total of 136 Mbytes. BIOS must program one of the first four Rows with 24 Mbytes to ensure that the 5th row is fully accessable.

Example #2 (memory exceeding 128 Mbytes)

Five DRAM row, non-SMBA system (5th row fixed at 8 Mbytes): Rows 0 to 3 are fast EDO DRAM (32 Mbytes per row), row 4 is 8 Mbytes of FPM DRAM (slower than the EDO) for a total of 136 Mbytes. The BIOS in this case programs DRB4 to the same value as DRB3, effectively eliminating the 8 Mbytes in row 4. BIOS reports the memory size as 128 Mbytes only (128 Mbytes is always the maximum).

Example #3 (memory exceeding 128 Mbytes)

Five DRAM row, non-SMBA system (5th row fixed at 16 Mbytes): Rows 0 to 3 are fast EDO DRAM (32 Mbytes per row) and row 4 is 16 Mbytes of EDO DRAM for a total of 144 Mbytes. The BIOS, in this case, programs DRB4 to the same value as DRB3, effectively eliminating the 16 Mbytes in row 4. BIOS reports the memory size as 128 Mbytes only (128 Mbytes is always the maximum).

As an example of a general purpose configuration where 4 physical rows are configured for either single-sided or double-sided SIMMs, the memory array would be configured like the one shown in Figure 2. In this configuration, the TVX drives two RAS# signals directly to the SIMM rows. If single-sided SIMMs are populated, the even RAS# signal is used and the odd RAS# is not connected. If double-sided SIMMs are used, both RAS# signals are used.

NOTE

In a SMBA (four RAS) system, RAS3# should be mapped to the front of SIMM 3 and 2. This mapping allows a single-sided SIMM to be used for SIMMs 2 and 3 in an SMBA system (i.e., last DRAM row must always be occupied in an SMBA system).

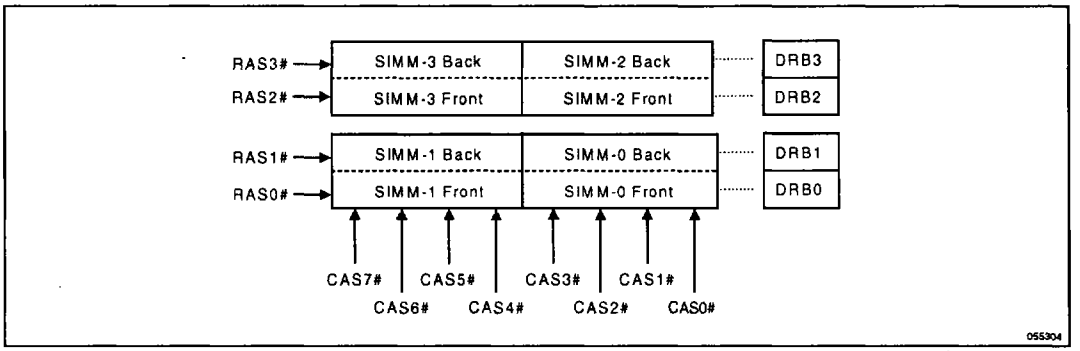


Figure 2. SIMMs and Corresponding DRB Registers

The following 3 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided SIMMs on a motherboard having a total of four, 8-byte or eight, 4-byte SIMM sockets.

Example #1

The memory array is populated with four single-sided 1MB x 32 SIMMs (16 Mbytes of DRAM). Two SIMMs are required for each populated row making each populated row 8 Mbytes in size.

DRB0 = 02h populated (2 SIMMs, 8 Mbytes this row)
DRB1 = 04h populated (2 SIMMs, 8 Mbytes this row)
DRB2 = 04h empty row
DRB3 = 04h empty row
DRB4 = 04h row 4 functionality not implemented (i.e. no memory in 5th row)

Example #2

As an another example, the memory array is populated with two 2-Mbyte x 32 double-sided SIMMs (one row), and four 4-Mbyte x 32 single-sided SIMMs (two rows), yielding a total of 96 Mbytes of DRAM. The DRB registers are programmed as follows:

DRB0 = 04h populated with 16 Mbytes, 1/2 of double-sided SIMMs
DRB1 = 08h the other 16 Mbytes of the double-sided SIMMs
DRB2 = 10h populated with 32 Mbytes, one of the sided SIMMs
DRB3 = 18h the other 32 Mbytes of single-sided SIMMs
DRB4 = 04h row 4 functionality not implemented (i.e., no memory in 5th row)

Example #3

As another example in a SMB enabled system using row 3 as the shared DRAM row, the memory array is populated with two 2-Mbyte x 32 double-sided SIMMs (two rows), and two 4-Mbyte x 32 single-sided SIMMs (one row), yielding a total of 64 Mbytes of DRAM. The DRB registers are programmed as follows:

DRB0 = 08h 32 MBytes of single-sided SIMMs
DRB1 = 08h empty
DRB2 = 0Ch populated with 16 Mbytes, 1/2 of double-sided SIMMs
DRB3 = 10h the other 16 Mbytes of the double-sided SIMMs (shared row)
DRB4 = 10h row 4 functionality not implemented (ie. disabled)

3.2.20. DRTH—DRAM ROW TYPE REGISTER HIGH

Address Offset: 67h
Default Value: 11h
Access: Read/Write

This 8-bit register identifies the type of DRAM used in row 4 (EDO, SPM, or SDRAM), and for EDO DRAMs or SDRAMs, should be programmed by BIOS for optimum performance. The Intel 430VX PCIset uses these bits to determine the correct cycle timing to use before a DRAM cycle is run and also to enable Row 4 (i.e., RAS4# or CS4# functionality muxing on TVX pins SRASB#/RAS4# or MXS/CS4#, respectively). If these bits are changed from their default value of 11h, row 4 is assumed to be present in the system.

Bit	Description
7:5	**Reserved.**
4	**See bits [4,0] below.**
3:1	**Reserved.**

Bit	Description
4,0	**DRAM Row Type (DRT).** The DRT bits select the DRAM type installed in physical DRAM Row 4. **Bits [4,0] DRAM Type value defintions** 0,0 SPM DRAM 0,1 EDO DRAM 1,0 SDRAM 1,1 Row 4 signalling via TVX MXS, SRASB# pins disabled

3.2.21. DRTL—DRAM ROW TYPE REGISTER LOW

Address Offset: 68h
Default Value: 00h
Access: Read/Write

The DRT Register identifies the type of DRAM used in each row; EDO, SPM (standard page mode), or SDRAM (synchronous DRAM) used in rows 0-3. This register should be programmed by BIOS for optimum performance if EDO DRAMs or SDRAMs are used. The hardware uses these bits to determine the correct cycle timing to use before a DRAM cycle is run.

Bit	Description
7:0	**DRAM Row Type (DRT).** These bits select the DRAM type installed in each physical DRAM Row. Each one-of-four bit pairs in this register corresponds to the DRAM row identified by the corresponding DRB Register. **DRT Bits DRAM Row** 7,3 3 6,2 2 5,1 1 4,0 0 **DRT DRAM Type value definitions:** 0,0 SPM DRAM 0,1 EDO DRAM 1,0 SDRAM 1,1 reserved

3.2.22. TRDT—PCI TRDY TIMER

Address Offset: 69h
Default Value: 03h
Access: Read/Write

Software programs this register to limit the number of PCI wait-states the TVX adds during the burst portion of a PCI master read or write cycle targeted for the TVX. The TVX response time, in PCI clocks, does not exceed the programmable count value in this register. The default value is set to meet the maximum allowable time per the PCI 2.0 specification.

Bit	Description
7:3	**Reserved.**
2:0	**TRDY Time-Out Value (TTOV).** This field contains the TRDY time-out value for PCI master read and write cycles targeted for the TVX. **Bits [2:0] — Time-Out Value (In PCICLKs)** 000 — 2 001 — 4 010 — 6 011 — 8 (default) 1xx — Reserved

3.2.23. MTT—MULTI-TRANSACTION TIMER REGISTER

Address Offset: 70h
Default Value: 20h
Access: Read/Write

This register controls the amount of time that the TVX's arbiter allows a PCI initiator to perform multiple transactions on the PCI bus. The MTT guarantees the minimum time (measured in PCLKs) that the PCI agent retains the ownership of the PCI bus from the initial assertion of grant.

Bit	Description
7:2	**MTT Count Value.** The number of clocks programmed in the MTT represents the guaranteed time slice (in PCLKs) allotted to the current agent, after which the TVX will grant the bus as soon as another PCI agent requests the bus. The value of 00h disables this function. The count value should be set to multiples of 4 (i.e., 2 lsbs are ignored).
1:0	**Reserved.** Hardwired to 0. (i.e., counter has a resolution of 4 PCLKs)

3.2.24. SMRAM—SYSTEM MANAGEMENT RAM CONTROL REGISTER

Address Offset: 72h
Default Value: 02h
Access: Read/Write

The System Management RAM Control Register controls how accesses to this space are treated. The Open, Close, and Lock SMRAM Space bits function only when the SMRAM enable bit is set to a 1. Also, the OPEN bit should be reset before the LOCK bit is set.

Bit	Description
7	**Reserved.**
6	**SMM Space Open (DOPEN).** When DOPEN=1 and DLCK=0, SMM space DRAM is made visible even when SMIACT# is negated. This is intended to help BIOS initialize SMM space. Software should ensure that DOPEN=1 is mutually exclusive with DCLS=1. When DLCK is set to a 1, DOPEN is reset to 0 and becomes read only.
5	**SMM Space Closed (DCLS).** When DCLS=1 SMM space DRAM is not accessible to data references, even if SMIACT# is asserted. Code references may still access SMM space DRAM. This allows SMM software to reference "through" SMM space to update the display even when SMM space is mapped over the VGA range. Software should ensure that DOPEN = 1 is mutually exclusive with DCLS = 1.
4	**SMM Space Locked (DLCK).** When DLCK is set to a 1, then DOPEN is set to 0 and both DLCK and DOPEN become read only. DLCK can be set to 1 but can only be cleared by a power-on reset. The combination of DLCK and DOPEN provide convenience with security. The BIOS can use the DOPEN function to initialize SMM space and then use DLCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the DOPEN function.
3	**SMRAM Enable (SMRAME).** When SMRAME=1, the SMRAM function is enabled, providing 128 Kbytes of DRAM accessible at the A0000h address while in SMM (ADS# with SMIACT#).
2:0	**SMM Space Base Segment (DBASESEG).** This field programs the location of SMM space. "SMM DRAM" is not remapped. It is simply "made visible" if the conditions are right to access SMM space. Otherwise, the access is forwarded to PCI. DBASESEG=010 is the only allowable setting, which selects the SMM space as A0000-BFFFFh. All other values are reserved. PCI initiators are not allowed access to SMM space.

NOTES:
Table 7 summarizes the operation of SMRAM space cycles targeting SMI space addresses (A-segment).

Table 7. SMRAM Space Cycles

SMRAME	DLCK	DCLS	DOPEN	SMIACT#	Code Fetch	Data Reference
0	X	X	X	X	PCI	PCI
1	0	0	0	0	DRAM	DRAM
1	0	X	0	1	PCI	PCI
1	0	0	1	X	DRAM	DRAM
1	0	1	0	0	DRAM	PCI
1	0	1	1	X	INVALID	INVALID
1	1	0	X	0	DRAM	DRAM
1	1	X	X	1	PCI	PCI
1	1	1	X	0	DRAM	PCI

3.2.25. SMBCR—SMB CONTROL REGISTER

Address Offset: 73h
Default Value: 00h
Access: Read/Write

This 8-bit register controls the shared memory buffer structure.

Bit	Description
7:2	**Reserved.**
1	**Shared Memory Buffer Enable (SMBE).** When SMBE=1 and SMBR=1, the DRAM address range defined between SMBSA and top of memory becomes the shared memory buffer area with read, write, and non-cacheable attributes. The TVX multiplexed REQ3#/MREQ# and GNT3#/MGNT# pins have the SMBA MREQ# and MGNT# functions, correspondingly. When SMBE=0, the REQ3#/GNT3# pins on the TVX are treated as a fourth PCI master request pair.
0	**Shared Memory Buffer Access Re-direct (SMBR).** When SMBE=1 and SMBR=0 and a valid SMBA range has been defined by the SMBSA and top of memory values (i.e., non-zero range), the SMBA range effectively becomes a 'hole' in system DRAM memory. All accesses to this hole are passed on to the PCI bus for termination. This can be used to re-direct CPU accesses to the video frame buffer across the PCI bus into the video controller itself.

3.2.26. SMBSA—SMB START ADDRESS

Address Offset: 74h
Default Value: 0Eh
Access: Read/Write

This 8-bit register defines the system DRAM start address for the shared memory buffer structure. Only values for system address bits A[26:19] are used giving a possible starting address from 0–128 Mbytes on a 0.5-Mbyte boundary. The SMBA end address is implied from the top-of-memory value, or just before the beginning of an enabled PCI Hole (bits [7:6] of DRAMC Register) at 14 or 15 Mbytes, when top-of-memory is at 16 Mbytes.

NOTE

The SMBSA Register should never be programmed with the values 00h or 01h (lower 1-Mbyte area). The default value of 0Eh is for a 1-Mbyte SMBA area in an 8-Mbyte system DRAM configuration.

Example A: For a shared memory buffer size of 2.5 Mbytes in a 16-Mbyte system with no PCI Hole enabled, the SMBA value is set to a 13.5-Mbyte start address value or 1Bh.

Example B: For a shared memory buffer size of 1 Mbyte in a 16-Mbyte system with a 1-Mbyte PCI Hole enabled, the SMBA value is set to a 14-Mbyte start address value (top-of-DRAM minus 2 Mbytes) or 1Ch.

Bit	Description
7:0	**SMB Start Address (SMBSA).** Bits [7:0] correspond to A[26:19], respectively.

3.2.27. GCLT—GRAPHICS CONTROLLER LATENCY TIMER

Address Offset: 78h
Default Value: 23h
Access: Read/Write

The GCLT Register controls the graphics controller MREQ# (high priority GC request) to MGNT# maximum latency. This register is used to program the Latency timer for PCI read cycles to DRAM and CPU/PCI master single write cycles to DRAM.

Bit	Description
7:6	**Reserved.**
5:3	**GC Latency For PCI Reads (GCLTR).** This field is used to program the GC latency timer for PCI master read cycles to DRAM. The DRAM cycle breaks to allow the GC accesses to DRAM when the DRAM-to-PCI buffers are full or when this timer times-out, which ever occurs first. **Bits [5:3] / Latency (In HCLKs) / Bits [5:3] / Latency (In HCLKs)** 000 / 0 / 100 / 16 (default) 001 / 4 / 101 / 20 010 / 8 / 110 / 24 011 / 12 / 111 / 28
2:0	**GC Latency For CPU/PCI Writes (GCLTW).** These bits are used to program the GC latency timer for PCI master single write and CPU single write cycles to DRAM. The DRAM cycle breaks to allow the GC access to DRAM when this timer times-out, or the DWBs become empty, or a burst write is encountered before the timer times out, which ever occurs first. **Bits [2:0] / Latency (In HCLKs) / Bits [2:0] / Latency (In HCLKs)** 000 / 0 / 100 / 16 001 / 4 / 101 / 20 010 / 8 / 110 / 24 011 / 12 (default) / 111 / 28

4.0. FUNCTIONAL DESCRIPTION

This section describes the host, PCI, secondary cache, and DRAM interfaces, The section also describes system arbitration and the Shared Memory Buffer Architecture (SMBA).

4.1. Host Interface

The Host Interface of the TVX is designed to support the Pentium processor with bus speeds of 50 MHz, 60 MHz, and 66 MHz. The Intel 430VX PCIset supports the Pentium processor with a full 64-bit data bus, 32-bit address bus, and associated internal write-back cache logic. Host bus addresses are decoded by the TVX for accesses to main memory, PCI memory, and PCI I/O. The TVX also supports the pipelined addressing capability of the Pentium processor.

4.2. PCI Interface

The TVX integrates a high performance interface to the PCI local bus taking full advantage of the high bandwidth and low latency of PCI. The TVX is fully PCI 2.1 Compliant. Five PCI masters are supported by the integrated arbiter including a PCI-to-ISA bridge and four general PCI masters. The TVX acts as a PCI master for CPU accesses to PCI. The PCI Bus is clocked at one half the frequency of the CPU clock. This divided synchronous interface minimizes latency for CPU-to-PCI cycles and PCI-to-main memory cycles.

The TVX/TDXs integrate posted write buffers for CPU memory writes to PCI. Back-to-back sequential memory writes to PCI are converted to burst writes on PCI. This feature allows the CPU to continue posting DWord writes at the maximum bandwidth for the Pentium processor for the highest possible transfer rates to the graphics frame buffer.

Read prefetch and write posting buffers in the TVX/TDXs enable PCI masters to access main memory at up to 120 MB/second. The TVX incorporates a snoop-ahead feature that allows PCI masters to continue bursting on both reads and writes even as the bursts cross cache line boundaries.

4.3. Secondary Cache Interface

The TVX integrates a high performance write-back second level cache controller using internal/external tags and provides a full first level and second level cache coherency mechanism. The second level cache is direct mapped, non-sectored, and supports a write-back cache policy. Cache lines are allocated on read misses (no write allocate).

The second level cache can be configured for either 256-Kbyte or 512-Kbyte cache sizes using Pipelined Synchronous Burst SRAMs, DRAM Cache, or Asynchronous SRAM. The DRAM Cache is a replacement for the standard pipeline burst SRAM. One additional PCIset pin (KRQAK), two system signals (H/WR# and RESET#), and one DRAM Cache specific signal (M/S#; strapped at the DRAM Cache device) are required to support DRAM Cache. The DRAM Cache conforms to the standard pipeline burst footprint. Refer to the Pipeline burst and DRAM Cache diagrams below for additional information.

For the 256-Kbyte configurations, an 8kx8 standard Asynchronous SRAM is used to store the tags. For the 512-Kbyte configurations, a 16kx8 standard Asynchronous SRAM is used to store the tags and the valid bits.

A second level cache line is 32 bytes wide. In the 256-Kbyte configurations, the second level cache contains 8k lines, while the 512-Kbyte configurations contain 16k lines. Valid and modified status bits are kept on a per-line basis. Cacheability of the entire memory space in first level cache is supported For the second level cache, only the lower 64 Mbytes of main memory are cacheable (only main memory controlled by the TVX DRAM interface is cached). PCI memory is not cached. The DRAM region between the SMB start address register and Top of Memory is also not cached when SMB (Shared memory buffer) is enabled. Table 8 shows the different standard SRAM access time requirements for different host clock frequencies.

Table 8. SRAM Access Time Requirements

Host Clock Frequency (MHz)	Std SRAM Access Time (ns)	Burst SRAM Clock-to-Output Access Time (ns)	Tag RAM Cycle Time (ns)
50	20	20	20
60	17	15	15
66	15	9	15

Figure 3 through Figure 5 show the connections between the TVX and the external tag RAM and data SRAM.

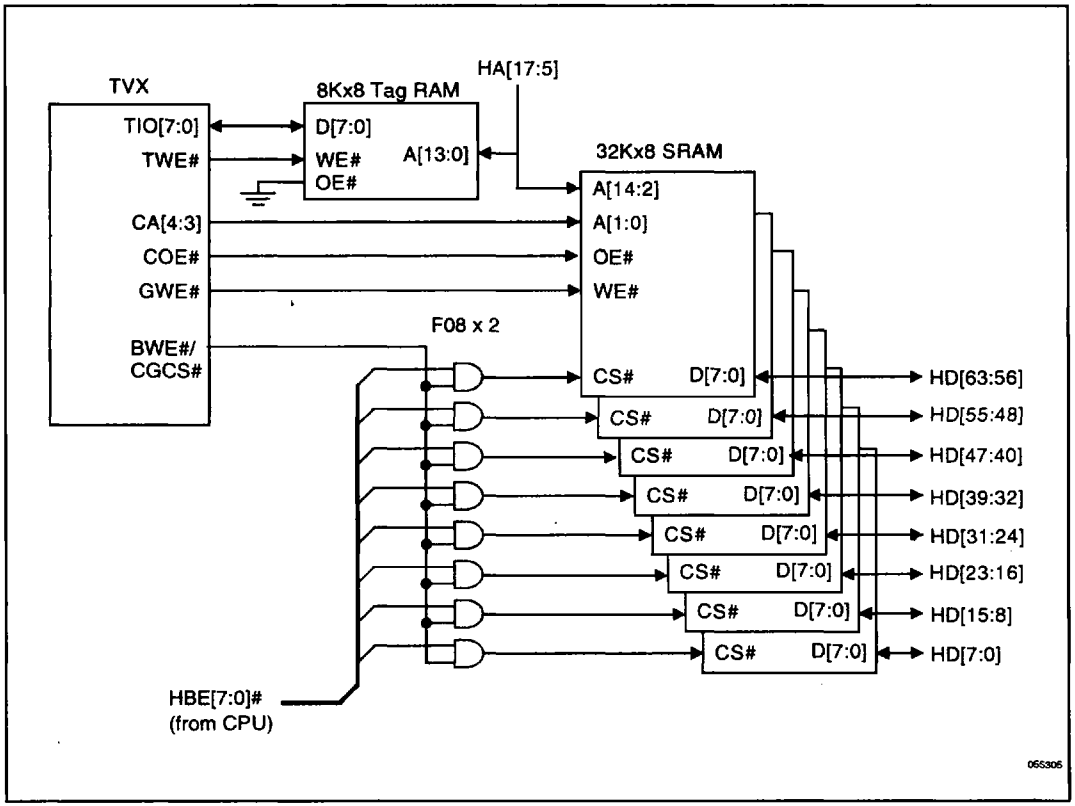
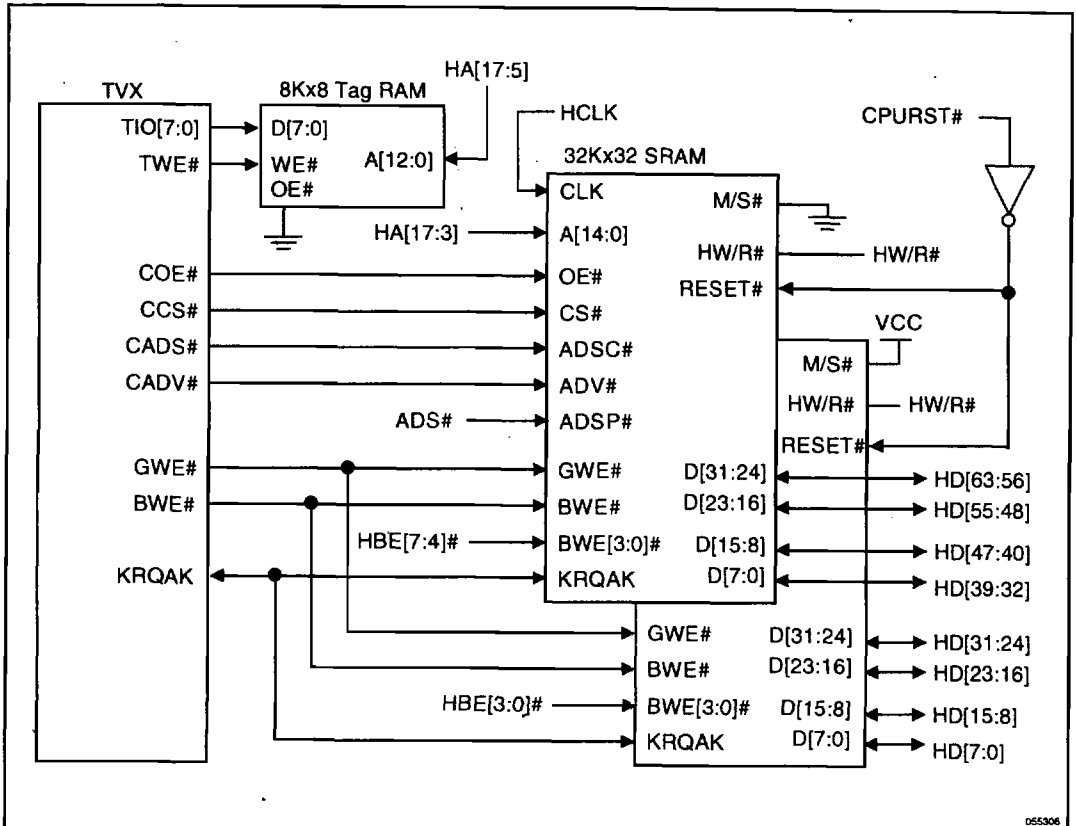


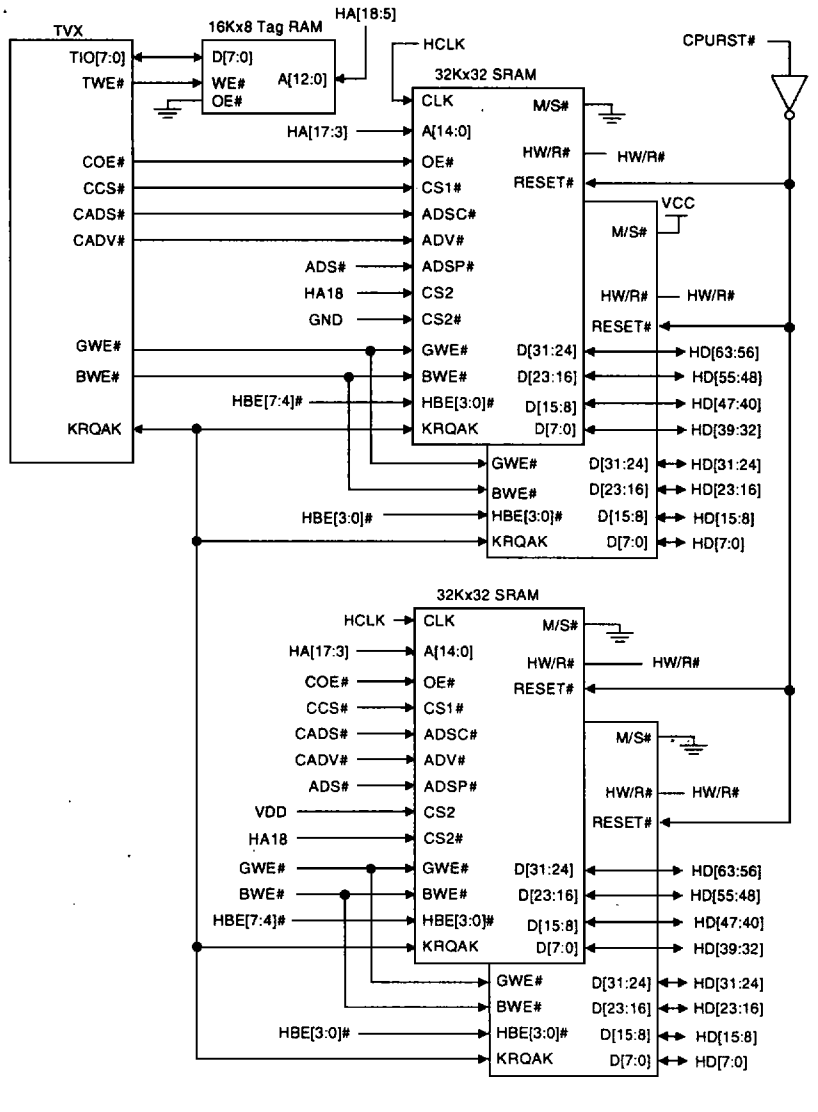
Figure 3. TVX Connections to 256-Kbyte Second Level Cache with Asynchronous SRAM



NOTES:

KRQAK (and the 4.7KΩ resistor on the KRQAK signal), M/S#, RESET# (and inverter on the RESET# signal), and H/WR# are only present for DRAM Cache Mode. M/S# is a master/slave strapping requirement used by the DRAM Cache to determine which device will drive the KRQAK signal during a refresh. The device that is strapped high (master), is the device that drives KRQAK. All other DRAM Cache devices monitor this signal.

Figure 4. TVX Connections to 256-Kbyte Second Level Cache with Pipelined Burst



NOTES:

KRQAK (and the 4.7KΩ resistor on the KRQAK signal), M/S#, RESET# (and inverter on the RESET# signal), and H/WR# are only present for DRAM Cache Mode. M/S# is a master/slave strapping requirement used by the DRAM Cache to determine which device will drive the KRQAK signal during a refresh. The device that is strapped high (master), is the device that drives KRQAK. All other DRAM Cache devices monitor this signal.

Figure 5. TVX Connections for 512-Kbyte Second Level Cache with Pipelined Burst SRAM

4.3.1. CLOCK LATENCIES

Table 9 and Table 10 list the latencies for various processor transfers to and from the second level cache.

Table 9. Second Level Cache Latencies (Asynchronous SRAM)

Cycle Type	HCLK Count
Burst Read	3-2-2-2
Burst Write (write-back)	4-3-3-3
Single Read	3
Single Write	4
Back-to-Back Burst Reads	3-2-2-2,3-2-2-2 (note 1)

NOTE:

1. The back to back cycles do not account for CPU idle clocks between cycles.

Table 10. Second Level Cache Latencies (Pipelined Burst SRAM or DRAM Cache)

Cycle Type	HCLK Count
Burst Read	3-1-1-1
Burst Write (write-back)	3-1-1-1
Single Read	3
Single Write	3
Pipelined Back-to-Back Burst Reads	3-1-1-1,1-1-1-1 (note 1)

NOTE:

1. The back to back cycles do not account for CPU idle clocks between cycles.

4.3.2. SNOOP CYCLES

Snoop cycles are used to maintain coherency between the caches (first and second level) and main memory. The TVX generates a snoop (or inquire) cycle to probe the first level and second level caches when a PCI master attempts to access main memory. Snoop cycles are performed by driving the PCI master address onto the host address bus and asserting EADS#.

To maintain optimum PCI bandwidth to main memory, the TVX utilizes a "snoop ahead" algorithm. Once the snoop for the first cache line of a transfer has completed, the TVX automatically snoops the next sequential cache line. This algorithm enables the TVX to continue burst transfers across cache line boundaries.

Reads

If the snoop cycle generates a first level cache hit to a modified line, the line in the first level cache is written back to main memory (via the DRAM posted write buffers). The line in the second level cache (if it exists) is invalidated. Note that the line in the first level cache is not invalidated if the INV pin on the CPU is tied to the KEN# signal from the TVX. The TVX drives KEN#/INV low with EADS# assertion during PCI master read cycles.

At the same time as the first level snoop cycle, the TVX performs a tag look-up to determine whether the addressed memory is in the second level cache. If the snoop cycle generates a second level cache hit to a modified line and there was not a hit in the first level cache (HITM# not asserted), the second level cache line

is written back to main memory (via the DRAM posted write buffers) and changed to the "clean" state. The PCI master read completes after the data has been written back to main memory.

Writes
PCI Master write cycles never result in a write directly into the second level cache. A snoop hit to a modified line in either the first or second caches results in a write-back of that line to main memory. If both the first and second level caches have modified lines, the line is written back from the first level cache. In all cases, lines in the first and second level caches are invalidated and the PCI write to main memory occurs after the writeback completes. A PCI master write snoop hit to an unmodified line in either the first or second level caches results in the line being invalidated. The TVX drives KEN#/INV with EADS# assertion during PCI master write cycles.

4.4. DRAM Interface

The TVX integrates a DRAM controller that supports a 64-bit memory array from 4 to 128 Mbytes of main memory. Extended Data Out (EDO), standard page mode (SPM), and synchronous DRAM (SDRAM) are supported. The TVX does not support parity and requires that non-parity SIMMS and DIMMS be used. The TVX generates the DRAM control signals and multiplexed addresses for the DRAM array and controls the data flow through the TDXs. For CPU-to-DRAM cycles the address flows through the TVX and data flows through the TDXs. For PCI or ISA cycles to memory, the address flows through the TVX and data flows to the TDXs through the TVX and PLINK bus. The TVX and TDX DRAM interfaces are synchronous to the CPU clock. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the TVX configuration register description. A brief overview of the registers that configure the DRAM interface is provided in this section.

The TVX supports industry standard 32-bit wide memory modules with EDO and SPM. The twelve multiplexed address lines (MA[11:0]) allow the TVX to support 512Kx32, 1Mx32, 2Mx32, and 4Mx32 SIMM's, with both symmetrical and asymmetrical addressing. Five RAS# lines support up to five rows of DRAM. If the 5th RAS# line is supported, certain restrictions are placed on the system (refer to the DRAM Organization section), Eight CAS# lines allow byte control over the array. The TVX targets 60 ns DRAMs and supports both single and double-sided SIMM's. The TVX also provides an automatic CBR refresh, at a rate of 1 refresh per 15.6 microseconds at 66, 60, and 50 MHz.

The TVX supports unbuffered DIMM Modules with SDRAMs. The twelve multiplexed address lines (MA[11:0]) allow the TVX to support 1Mx64, 2Mx64, and 4Mx64 DIMM's. Five CS# lines support up to five rows of SDRAM. If the 5th CS# line is supported, certain restrictions are placed on the system (refer to the DRAM Organization section). Eight DQM lines allow byte control over the array. The TVX supports 50, 60 and 66 MHz SDRAMs and supports both single and double-sided DIMM's. The TVX also provides an automatic CBR refresh, at a rate of 1 refresh per 15.6 microseconds at 66, 60, and 50 MHz.

The DRAM interface is configured by the DRAM Control (DRAMC) Register, the DRAM Extended Control (DRAMEC) Register, DRAM Timing (DRAMT) Register, SDRAM Control (SDRAMC) Register, the four DRAM Row Boundary (DRB) Registers, and the DRAM Row Type (DRT) Registers. The four DRB Registers define the size of each row in the memory array, enabling the TVX to assert the proper RAS# line for accesses to the array.

Seven Programmable Attribute Map (PAM) Registers specify the cacheability, PCI enable, and read/write status of the memory space between 640 Kbytes and 1 Mbyte. Each PAM Register defines a specific address area enabling the system to selectively mark specific memory ranges as cacheable, read-only, write-only, read/write, or disabled. When a memory range is disabled, all CPU accesses to that range are forwarded to PCI.

The TVX also supports one of two memory holes (512-Kbyte to 640-Kbyte or 14/15 Mbytes to 16 Mbytes). Accesses to the memory holes are forwarded to PCI. The memory hole can be enabled/disabled through the DRAM Control Register. All other memory from 1 Mbyte to the top of memory is read/write and cacheable.

The SMRAM memory space is controlled by the SMRAM Control Register. This register enables, opens, closes, or locks SMRAM space.

4.4.1. DRAM ORGANIZATION

The Intel 430VX PCIset supports EDO, SPM, and SDRAM. In a four row system, all of these DRAM types can be mixed and matched on a row-by-row basis. In a 5 row system, EDO/SPM can not be mixed with SDRAM. Refer to the "Four Row System" and "Five Row System" sections below, for specific details.

NOTE

SDRAM is not supported in the row the graphics controller uses in a Shared Memory Buffer Architecture (SMBA) configuration. SDRAM with EDO is supported in a SMBA configuration, if SDRAM is not populated in the SMBA DRAM row.

Four Row System

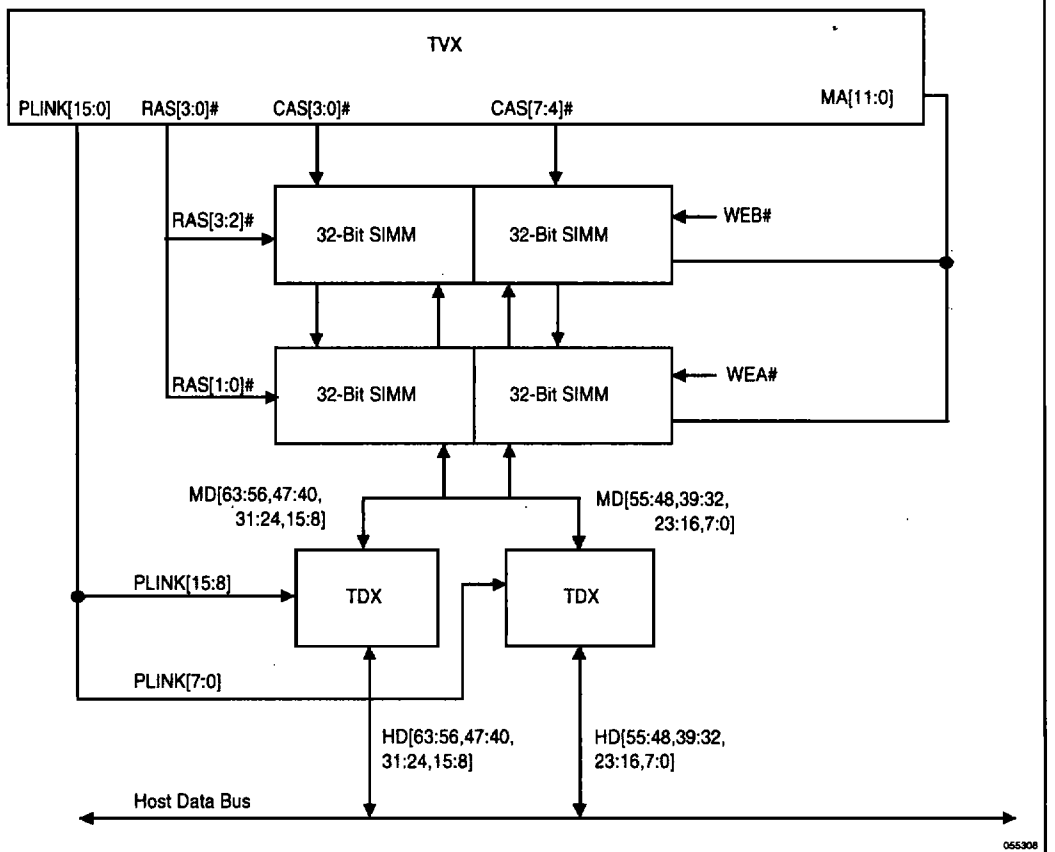
Figure 6 illustrates a 4-SIMM configuration that supports 4 double-sided SIMM's. A row in the DRAM array is made up of two SIMM's that share a common RAS# line. Within any given row, the two SIMMs must be of the same size. Among the four rows, SIMM densities can be mixed in any order. Each row is controlled by up to 8 CAS lines. EDO and standard page mode DRAM's can be mixed between rows; however, a given row must contain only one type of DRAM. When DRAM types are mixed (EDO and standard page mode) each row runs optimized for that particular type of DRAM. Figure 8 illustrates a 2-DIMM SDRAM system.

The rules for SIMM population are as follows:

- SIMM sockets can be populated in any order (i.e., memory for RAS0# does not have to be populated before memory for RAS3# is used).
- SIMM socket pairs need to be populated with the same densities on a row per row basis. For example, SIMM sockets for RAS0# should be populated with identical densities. However, SIMM sockets for RAS3# can be populated with different densities than the SIMM socket pair for RAS0#.
- EDO's and standard page mode can both be used on a row per row basis. However, only one type should be used per SIMM socket pair. For example, SIMM sockets for RAS[0]# can be populated with EDO's while SIMM sockets for RAS[3]# can be populated with standard page mode.

The rules for SDRAM population are as follows:

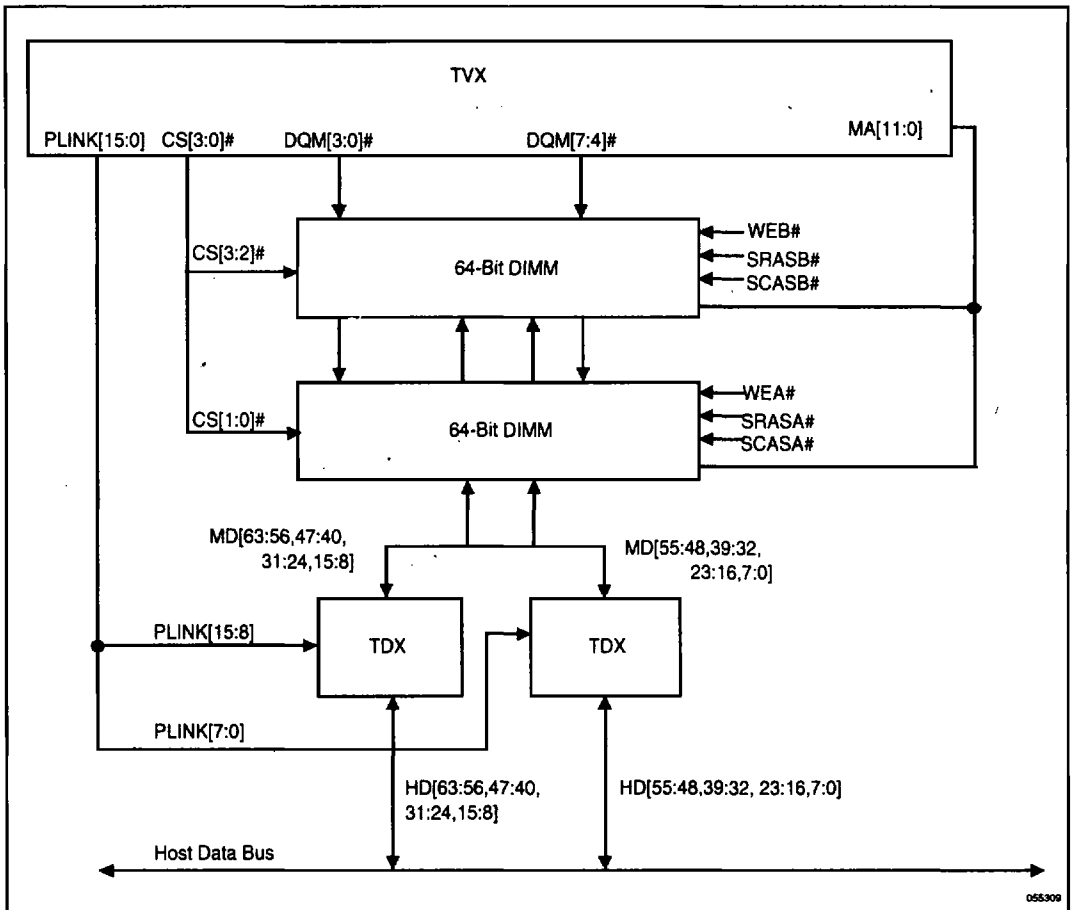
- DIMMs can be populated in any order (e.g., row 0 does not need to be populated before row 3 is used).
- SDRAMs can be mixed with EDO/SPM on a row per row basis (e.g., row 0 can be populated with SDRAMs while row 3 can be populated with EDO/SPM). TVX runs with optimized timings on a row per row basis.



NOTES:

1. External buffers on the MA lines have been integrated in the Intel 430VX PCIset.
2. Two copies of WE# are provided for loading purposes only.

Figure 6. SIMM Socket With EDO/SPM



NOTES:

1. External buffers on the MA lines have been integrated in the Intel 430VX PCIset.
2. Two copies of WE#, SRAS#, and SCAS# are provided for loading purposes only.

Figure 7. DIMM Socket With SDRAM

Five ROW System

Support for a 5th row enables memory to be soldered on the motherboard, in addition to providing 4 rows of memory upgradability. Mixing of memory types is allowed on a row per row basis for a system with 4 rows of memory. If the 5th row is used, certain restrictions are placed on the system. These restrictions are shown below:

- The 5th row is intended to be implemented with DRAM devices that are soldered down on the motherboard. If a DIMM or a SIMM is used in the 5th ROW, it should not be used as an upgrade path by the end user, as the size and type of DRAM that can be implemented in the 5th row is limited. (see the following bullets).
- All 5 rows must be either all EDO/SPM type DRAM or all SDRAM (i.e., EDO and SPM can be mixed on a row per row basis but EDO/SPM cannot be mixed with SDRAMs).
- There is a restriction on DRAM timings when 5 rows of memory are populated. At 66 MHz with 60 ns memory or 60 MHz with 70 ns memory, the burst rate must be set to X-3-3-3 EDO, x-4-4-4 FPM (bits[6:5]=01, DRAMT register, 58h).
- In a SMBA design, the size of the 5th row of memory must be fixed at 8 Mbytes using 1Mx16 devices, due to loading limitations. In a non-SMBA design, the 5th row can be implemented using 2Mx8 (fixed at 16M) or 1Mx16 devices (fixed at 8M). Note that the 16M in the 5th row is supported in non-SMBA designs only.
- Note that the total memory supported is limited to 128 Mbytes, even though it is possible to populate the 5 rows with up to 136 Mbytes (in a SMBA design) or 144 Mbytes (in a non-SMBA design). This limit must be ensured by the system BIOS.
  - — If the first four rows have 32 Mbytes each and the 5th row has 8 Mbytes of memory for a total of 136 Mbytes, BIOS must program one of the first four rows with 24 Mbytes to ensure that the 5th row is fully accessable.
  - — If the first four rows of memory have 32 Mbytes each, and the 5th row has 16 Mbytes, BIOS must disable the 5th row of memory via the DRB's. Also, if the 5th row of memory has 16 Mbytes and the other four rows of memory have 1Mx4 (8 Mbytes per row) or 4Mx4 (32 Mbytes per row), BIOS must add wait-states to the memory array. The wait-states added slows the read and write leadoff and burst timings by one clock.

For a 5 row SPM/EDO DRAM implementation, SCASB#/RAS4# is used as the RAS4# signal to provide the 5th RAS# signal. For a 5 row SDRAM implementation, MXS/CS4# is used as the CS4# signal to provide the 5th CS# signal. Both RAS4# and CS4# have an internal pullup resistor in the TVX.

Figure 8 shows an EDO/FPM system with 5 rows of memory, using 1Mx16 devices (8M). If 2Mx8 devices are used (fixed at 16M), the WEB# line can be connected to four devices in the 5th row, and the WEB# can be connected to the remaining four devices in the 5th row. In general, the WEA# and WEB# lines should be distributed as equally as possible in the DRAM subsystem.

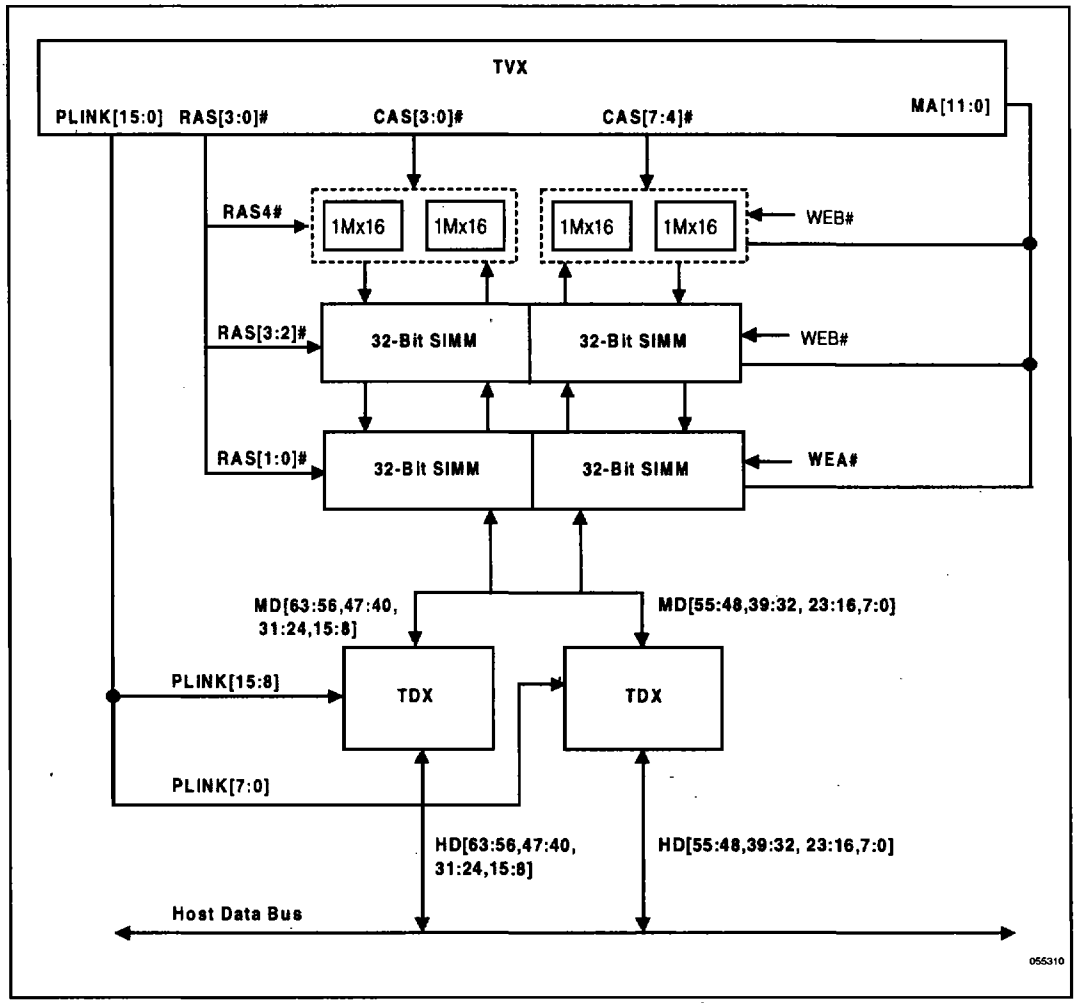


Figure 8. 5 ROW Example using EDO/FPM

Table 11 provides a summary of the characteristics of memory configurations supported by the TVX. Minimum values listed are obtained with single-sided SIMMs and maximum values are obtained with double-sided SIMMs. Note that, for a 64-bit wide memory array, a minimum of two 32-bit wide DRAM SIMM configuration is required. The minimum values used are also the smallest upgradable memory size.

Table 11. Minimum (Upgradable) and Maximum Memory Size for each configuration (EDO/SPM)

DRAM Tech.	DRAM Density	DRAM Width	DRAM SIMM		DRAM	Address Size		DRAM Size	
			SS x32	DS x32	Addressing	Row	Column	Min. (1 row)	Max. (4 rows)
4Mbit	512K	8/32	512K	1M	Asymmetric	10	9	4 MB	16 MB
	1M	4	1M	2M	Symmetric	10	10	8 MB	32 MB
	1M	4	1M	2M	Asymmetric	12	8	8 MB	32 MB
16Mbit	1M	16	1M	2M	Symmetric	10	10	8 MB	32 MB
	1M	16	1M	2M	Asymmetric	12	8	8 MB	32 MB
	2M	8	2M	4M	Asymmetric	11	10	16 MB	64 MB
	4M	4	4M	8M	Symmetric	11	11	32 MB	128 MB
	4M	4	4M	8M	Asymmetric	12	10	32 MB	128 MB

Table 12 provides a summary of the characteristics of memory configurations supported by the TVX. Minimum values listed are obtained with single-sided DIMMs and maximum values are obtained with double-sided DIMMs. The minimum values used are also the smallest upgradable memory size.

Table 12. Minimum (Upgradable) and Maximum Memory Size for each configuration(SDRAM)

SDRAM Tech.	SDRAM Density	SDRAM Width	DRAM DIMM		DRAM	Address Size		DRAM Size	
			SS x64	DS x64	Addressing	Row	Column	Min. (1 row)	Max. (4 rows)
16Mbit	1M	16	1M	2M	Asymmetric	12	8	8 MB	32 MB
	2M	8	2M	4M	Asymmetric	12	9	16 MB	64 MB
	4M(note)	4	4M	8M	Asymmetric	12	10	32 MB	128 MB

The memory organization (Figure 9) represents the maximum 128 Mbytes of address space. Accesses to memory space above top of DRAM, video buffer, or the memory gaps (if enabled) are forwarded to PCI. These regions are not cacheable. Below 1 Mbyte there are several memory segments that have selectable cacheability. The DRAM space occupied by the video buffer or the memory space gaps is not remapped and is therefore "lost". Refer to the Shared Memory Buffer Architecture (SMBA) section for details on SMBA System memory mapping.

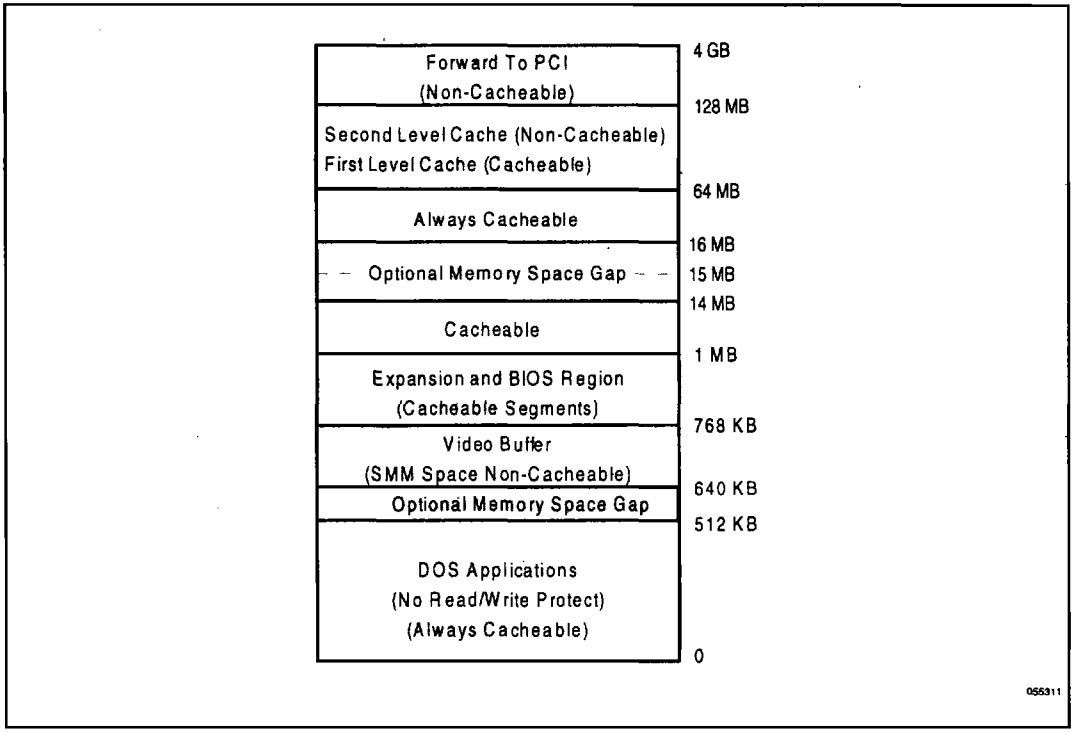


Figure 9. Memory Space Organization

4.4.2. DRAM ADDRESS TRANSLATION

The multiplexed row/column address to the DRAM memory array is provided by the MA[11:0] signals. The MA[11:0] bits are derived from the host address bus as defined by Table 13. The TVX has a 2-Kbyte page size. However, the address map has been defined to support a 4k page size from the graphics controller's perspective, in a SMBA design. The page offset address is driven over the MA[7:0] lines when driving the column address. The MA[11:0] lines are translated from the host address lines A[24:3] for all memory accesses.

Table 13. DRAM Address Translation for EDO/SPM/SDRAM

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A11	A11/ "V"	A11/ A24	A11/ A22/ A23	A10	A9	A8	A7	A6	A5	A4	A3

NOTES:
V=Valid level (either 0 or 1) used for SDRAMs. During the initialization sequence, it is 1 and during normal mode of operation, it is 0.

4.4.3. DRAM PAGING

The DRAM page is kept open when the CPU host bus is non-idle or the PCI interface owns the bus.

4.4.4. EDO MODE

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge. Note that standard page mode DRAM tri-states the memory data when CAS# negates to precharge. With EDO, the CAS# precharge overlaps the memory data valid time. This allows CAS# to negate earlier while still satisfying the memory data valid window time.

4.4.5. SDRAM MODE

The Intel 430VX PCIset supports all of the features and timings as shown in the "SDRAM PC" specification. The objective of the "SDRAM PC" specification is to enable low cost and easily manufacturable SDRAMs for the main stream volume desktop PC's. There are three speed grade parts defined for the Intel 430VX PCIset (Table 14). All of the speed grades conform to the "SDRAM PC" specification. The three speed grades are as follows:

Table 14. SDRAM Speed Grades

Speed Grade	CAS latency	System Frequency
66.67 MHz (note)	3	50/60/66 MHz
66.67 MHz	2	50/60/66 MHz
50 MHz	2	50 MHz

SDRAM Mode Register

The Mode Register Set supported by TVX is as follows:

Bit	11	10	9	8	7	6, 5, 4	3	2, 1, 0
Value	0	0	0	0	0	CL	WT	BL

CAS Latency Field (CL)	
Bits (6:4)	CAS Latency
010	2
011	3
All Other	X

Wrap Type (WT)	
Bit 3	Type
0	X
1	Interleave

Burst Length (BL)	
Bits (2:0)	Burst Length
010	4
All Other	X

NOTES:

1. The CL bit is programmed as per the bit setting for the CL field of the TVX SDRAMC Register
2. The linear order addressing is not supported.
3. X=Don't Care. These modes are Don't Care for TVX specific implementation.

Command Truth Table

SDRAM commands supported by the TVX are:

- Mode Register Set (MRS)
- Activate Bank (ACT)
- Read Bank (READ)
- Write Bank (WRITE)
- Precharge All Banks (PALL)
- Deselect Device
- No Operation (NOP)
- Auto Refresh (REFR)

4.4.6. AUTO DETECTION

The SDRAM, FPM, and EDO detection is performed by BIOS. Note, that when accessing any of the DRAM related registers (i.e., 54h–68h), refresh should be turned off via the DRAMC Register.

4.4.7. DRAM PERFORMANCE

The DRAM performance is controlled by the DRAM timing register, processor pipelining, and by the type of DRAM used (EDO or standard page mode). Table 15 depicts both EDO and standard page mode optimum timings. For read cycles, clocks counts are measured from ADS# to BRDY#. For write cycles, the measurement is broken up into two parts. The first part consists of the rate of posting data in to the CPU to DRAM posted write buffers. This is measured from ADS# to BRDY#. The second part consists of the retire rate from posted write buffers to the DRAM. The leadoff for retiring is measured from the clock after BRDY# assertion to the CAS# assertion. Table 15 lists a performance summary for 60 ns EDO/SPM DRAMs.

Table 15. EDO/ Standard Page Mode Performance Summary (60ns DRAMs)

Processor Cycle Type (pipelined)	66 MHz[7] (Burst SRAM)	60 MHz (Burst SRAM)	50 MHz (Burst SRAM)	66 MHz (Asynch Cache)	DRAM TYPE
Burst Read Page Hit	6-2-2-2	5-2-2-2	5-2-2-2	7-3-3-3	EDO
Read Row Miss[1]	9-2-2-2	8-2-2-2	7-2-2-2	10-3-3-3	EDO
Read Page Miss	12-2-2-2	11-2-2-2	10-2-2-2	13-3-3-3	EDO
Back-to-Back Burst Reads Page Hit	6-2-2-2-3-2-2-2	5-2-2-2-3-2-2-2	5-2-2-2-3-2-2-2	7-3-3-3-7-3-3-3	EDO
Burst Read Page Hit	6-3-3-3	6-3-3-3	6-3-3-3	7-3-3-3	SPM
Burst Read Row Miss[1]	9-3-3-3	9-3-3-3	8-3-3-3	10-3-3-3	SPM
Burst Read Page Miss	12-3-3-3	12-3-3-3	11-3-3-3	13-3-3-3	SPM
Back-to-Back Burst Read Page Hit	6-3-3-3-3-3-3-3	6-3-3-3-3-3-3-3	6-3-3-3-3-3-3-3	7-3-3-3-7-3	SPM
Write Page Hit[2,3,4]	3	3	2	3	EDO/SPM
Write Row Miss[2,3,4]	6	6	5	6	EDO/SPM
Write Page Miss[2,3,4]	9	9	8	9	EDO/SPM

Table 15. EDO/ Standard Page Mode Performance Summary (60ns DRAMs)

Processor Cycle Type (pipelined)	66 MHz[7] (Burst SRAM)	60 MHz (Burst SRAM)	50 MHz (Burst SRAM)	66 MHz (Asynch Cache)	DRAM TYPE
Posted Write[3,4]	3-1-1-1	3-1-1-1	3-1-1-1	4-1-1-1	EDO/SPM
Write retire rate from Posted Write Buffer	-2-2-2	-2-2-2	-2-2-2	- -2-2-2	EDO/SPM
Single writes	2	2	2	2	EDO
Single writes	2	2	2	2	SPM
DRAMEC Register (offset 56h) Programming					
Bit 6 (RRA)	0	0	0	0	EDO/SPM
Bit 5(FEPS)	0	1	1	0	EDO
Bit 5(FEPS)	0	0	0	0	SPM
DRAMT Register (offset 58h) Programming					
Bit 7(FMRD)	1	1	1	1	EDO/SPM
Bits[6:5] (DRBT)[6]	2	2	2	2	EDO/SPM
Bit[4:3] (DWBT)	2	2	2	2	EDO/SPM
Bit 2 (FRCD)	0	0	1	0	EDO/SPM
Bits(1:0) (DLT)	1	1	1	1	EDO/SPM

NOTES:

1. The above row miss cycles assume that the new page is closed from the prior cycle. Due to the MA[11:0] to RAS# setup requirements, if the page is open, 2 clocks are added to the leadoff. If FMRD bit is set to 1, then only one clock is added to the leadoff.
2. This cycle timing assumes the write buffer(DWB) is empty.
3. Write timing is measured from the clock after BRDY# is returned to the CPU up to CAS# assertion for that cycle.
4. Write data is always posted as 3-1-1-1 (ADS# to BRDY#, if buffer is empty) with burst or pipelined burst second level cache SRAMs (or cacheless operation). For Asynchronous SRAMs, write data is posted as 4-1-1-1.
5. Bit 5 in the DRAMEC register must be set to 0 if the EDO/FPM burst rate is set to x333 or x444, or an asynchronous cache in the system.
6. If an L2 asynchronous cache is in the system, do not set the DRBT bit to 3.
7. There is a restriction on the DRAM timings when 5 rows of memory are populated. At 66 MHz with 60 ns memory or 60 MHz with 70 ns memory, the burst rate must be set to x-3-3-3 EDO, x-4-4-4 SPM (register 58h, bits[6:5]=01h.

Table 16. EDO AND SPM LEADOFF TIMING CALCULATION

DLT[1]	Read leadoff	Write Leadoff	RAS# Precharge	FRCD[2]	Fast RAS to CAS		Leadoff	FEPS[3]	Leadoff
0	11	7	3	0	3		0	0	0
1	10	6	3	1	2		-1	1	-1
2	11	7	4						
3	10	6	4						

NOTES:

1. DLT bits represent the row miss leadoff for EDO/SPM reads and writes. These leadoff represent timings with FRCD=0, SLE=0 and FEPS=0. Page hits can be calculated by subtracting RAS# precharge from row misses (10 - 3 =7) and page misses can be calculated by adding the RAS# precharge time to Row Misses.

   DLT effects the row miss and page miss timings only (e.g., DLT= 1 is one clock faster than DLT=0 on row miss and page miss timings). These bits control MA setup to CAS# assertion.

   DLT does not effect page hit timings (e.g., DLT=0 or DLT=1 have same page hit timings for reads and writes). In both cases it would be 7 (10-3) clocks.
2. FRCD bit effects the row miss and page miss timings for EDO/SPM reads and writes. FRCD bits have subtractive effect on DLT bits (e.g., if DLT=1 and FRCD=1, read row miss leadoff timing is 9 (10 -1) clocks).
3. FEPS bit effects the page miss, row miss and page hit timings for EDO reads only. FEPS bits have subtractive effect on DLT bits (e.g., if DLT=1 and FEPS=1, then read row miss leadoff timing is 9 (10-1) clocks).

Table 17. SDRAM Performance Summary

Processor Cycle type	50/60/66 MHz	50/60/66 MHz	50 MHz
	CL=3[1]	CL=2[2]	CL=2[3]
Burst Read Page Hit	7-1-1-1	6-1-1-1	6-1-1-1
Read row Miss	10-1-1-1	8-1-1-1	8-1-1-1
Read Page Miss	13-1-1-1	11-1-1-1	11-1-1-1
Back-to-Back Burst Reads Page Hit	7-1-1-1 2-1-1-1.	6-1-1-1 2-1-1-1.	6-1-1-1 2-1-1-1.
Write Page Hit	3	3	3
Write Row Miss	6	5	5
Write Page Miss	9	8	8
Posted Write	3-1-1-1	3-1-1-1	3-1-1-1
Write retire rate from Posted Write Buffer	-1-1-1	-1-1-1	-1-1-1
SDRAMC Register (offset 54–55h) Programming			
Bit 4 (CL)	0	1	1
Bit 3 (RT)	0	0	1

NOTES:
1. Parts are of Speed Grade 66.67 MHz with CAS latency =3
2. Parts are of Speed Grade 66.67 MHz with CAS latency =2
3. Parts are of Speed Grade 50 MHz with CAS latency =2
4. Asynch SRAMs are not supported with SDRAMs.
5. The row miss cycles assume that the new page is closed from the prior cycle.

4.4.8. DRAM REFRESH

TVX supports CBR refresh only and generates refresh requests. The rate at which requests are generated is determined by the value in the DRAM Refresh Rate field of the DRAM Control Register. When a refresh request is generated, it is placed in a four entry queue. DRAM high level priority refresh is set after four refreshes are accumulated. If one of the refresh is serviced after the high level priority refresh is set, the priority level of the Refresh changes from high to low.

There is also a "smart refresh" algorithm implemented in the refresh controller. Refresh is only performed on banks that are populated. The refresh controller determines which banks are populated through the DRB registers.

4.4.9. SYSTEM MANAGEMENT RAM

The TVX supports the use of main memory as System Management RAM (SMRAM) enabling the use of System Management Mode. When this function is disabled, the TVX memory map is defined by the DRB and PAM Registers. When SMRAM is enabled, the TVX reserves the video buffer area (A and B segments) of main memory for use as SMRAM.

SMRAM is placed at A0000—BFFFFh via the SMRAM Space Register. Enhanced SMRAM features can also be enabled via this register. PCI masters can not access SMRAM when it is programmed to the video buffer area (A and B segments).

When the TVX detects a CPU stop grant special cycle, it generates a PCI Stop Grant Special cycle, with 0002h in the message field (AD[15:0]) and 0012h in the message dependent data field (AD[31:16]) during the first data phase (IRDY# asserted).

4.5. TDXs and the PLINK Interface

The TDXs provide the data path for host-to-DRAM, PCI-to-DRAM, and host-to-PCI cycles. Two TDXs are required for the Intel 430VX PCIset. The TDXs are divided into two identical units. The TVX controls the data flow through the TDXs with signals PCMD[1:0], HOE#, POE#, MOE#, MSTB[1:0], MXS, and MADV#.

The TDXs have three data path interfaces; the host bus HD[63:0]. the memory bus MD[63:0], and the PLINK[15:0] bus between the TDX and TVX. The data paths for the TDXs are interleaved on byte boundaries (Figure 10). Byte lanes 0, 2, 4, and 6 from the host CPU data bus connects to the even order TDX and byte lanes 1, 3, 5, and 7 connects to the odd order TDX. PLINK[7:0] connects to the even order TDX and PLINK[15:8] connects to the odd order TDX.

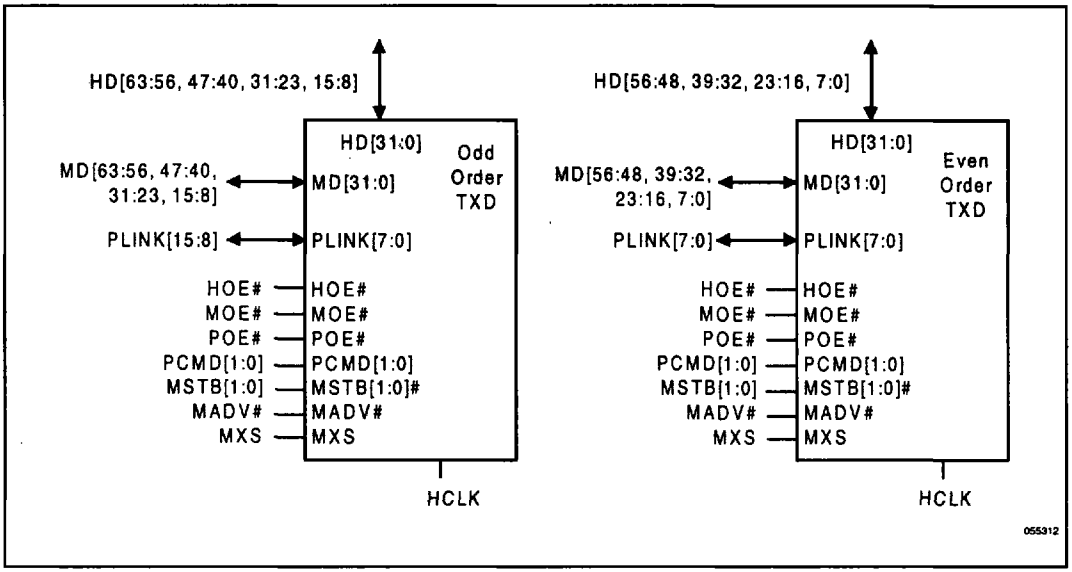


Figure 10. TDX 64-Bit Data Path Partitioning

4.6. System Arbitration

The TVX's PCI Bus arbiter allows PCI peer-to-peer traffic concurrent with CPU main memory/second level cache cycles. The arbiter supports five PCI masters (Figure 11). REQ[3:0]#/GNT[3:0]# are used by PCI masters other than the PCI-to-ISA expansion bridge (PIIX3). PHLD#/PHLDA# are the arbitration request/grant signals for the PIIX3 and provide guaranteed access time capability for ISA masters. PHLD#/PHLDA# also optimize system performance based on PIIX3 known policies. PCI request/grant pair three is multiplexed and used as the SMBA request/grant pair when the SMBA is enabled.

A bit in the PCON register is used to select between a priority scheme that counts three PCI grants (mode 0) or two PCI grants (mode 1) to decide when it is time to let the host in. Mode 0 is intended to be used in a system when SMBA is disabled and mode 1 is intended to be used in a system with SMBA.

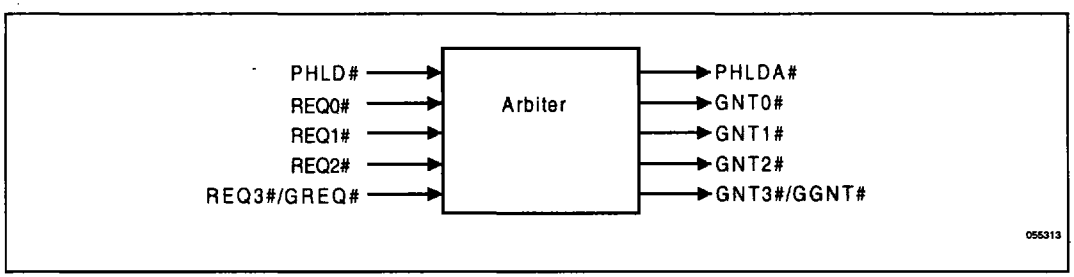
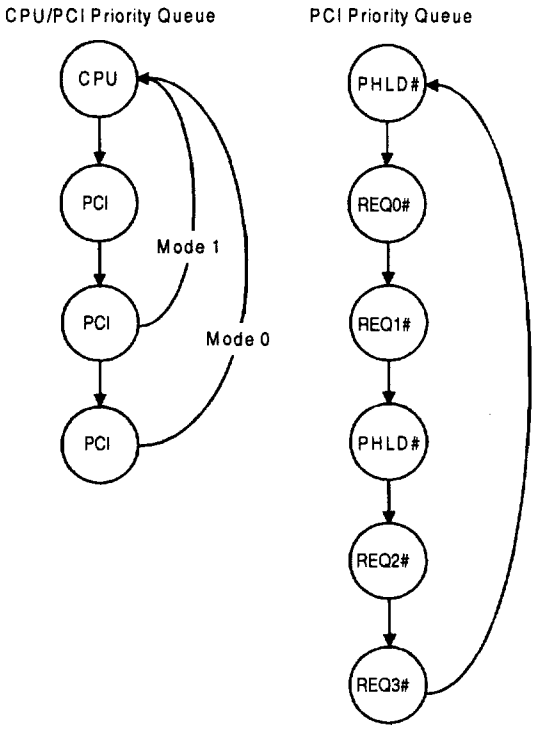


Figure 11. PCI Bus Arbiter

4.6.1. PRIORITY SCHEME AND BUS GRANT

The TVX PCI arbitration provides two arbitration schemes (mode 0 and 1) as programmed in the PCON Register. The highest priority requester is determined by a fixed order queue together with a highest priority pointer. Although the priority ring is fixed, the highest priority pointer moves to determine which PCI agent is at the top (and bottom) of the queue. The arbiter counts three grant assertions (mode 0) or two grant assertions (mode 1) to requesters different than the one it is currently granting (and all grants within Multi-Transaction Timer count are collapsed to one) to determine when it's time for host access.

The grant signals (GNTx#) are normally negated after recognition of FRAME# assertion or 16 PCLKs from grant assertion, if no cycle has started.



NOTES:

1. In the PCI Priority Queue, the last agent granted is always dropped to the bottom of the queue for the next arbitration cycle, but the order of the chain is always preserved.
2. In the PCI Priority Queue, if PHLD is at the bottom of the queue, the upper PHLD slot is masked. This prevents back-to-back grants, if other PCI requests are pending.
3. In the CPU/PCI priority Queue, the CPU is granted high priority status after 3 (mode 0) or 2 (mode 1) consecutive PCI grants. If three (two) consecutive PCI grants have not been counted down, the CPU can be granted the bus as the low priority agent.

Figure 12. Arbitration Priority Rotation

4.6.2. MULTI-TRANSACTION TIMER (MTT)

The priority chain algorithm has been enhanced by the Multi-Transaction Timer (MTT) mechanism. Once a PCI agent is granted, the MTT is started. The timer counts down in PCI clocks from its preset value to zero. Until the timer expires, that agent is promoted to being the highest priority PCI agent for the next grant event.

4.6.3. CPU POLICIES

The CPU never explicitly requests the bus. Instead, the arbiter grants the bus to the CPU when:

- the CPU is the highest priority
- PCI agents do not require main memory (peer-to-peer transfers or bus idle) and the PCI bus is not currently locked by a PCI master

When the CPU is granted as highest priority, the MLT timer is used to guarantee a minimum amount of system resources to the CPU before another requesting PCI agent is granted. An AHOLD mechanism controls granting the bus to the CPU.

4.7. Shared Memory Buffer Architecture

The TVX provides a shared memory buffer interface allowing the frame buffer of an on-board video controller to be implemented using main memory instead of dedicated video memory. The TVX contains a two-wire, dual priority arbitration scheme. Both the TVX and graphics controller (GC) drive the system DRAM interface directly. DRAM address, data, and control signals are alternately driven and tri-stated in a controlled manner. When the SMB area is enabled (via the SMBCR Register), the TVX PCI REQ3#/GNT3# pin pair are used as the SMB MREQ#/MGNT# arbitration signals.

The shared memory buffer resides in a programmable CPU address range between the value programmed in the SMBSA Register and the top-of-memory. The top of main memory is the highest address indicated by the DRAM Row boundary 4 (DRB4) Register.

NOTE

SDRAM is not supported in the row the graphics controller uses in a SMBA configuration. SDRAM with EDO is supported in a SMBA configuration, if SDRAM is not populated in the SMBA DRAM row.

4.7.1. SMB SYSTEM MEMORY MAPPING

The Intel 430VX PCIset supports systems with either four rows of memory or five rows of memory (refer to the DRAM Interface section). In a 4-row system, row 3 is always populated and is located at the top of the physical address map. In a 5-row system, row 4 is always populated and located at the top of the physical address map. Figure 13 illustrates the physical address map for a system with four DRAM rows:

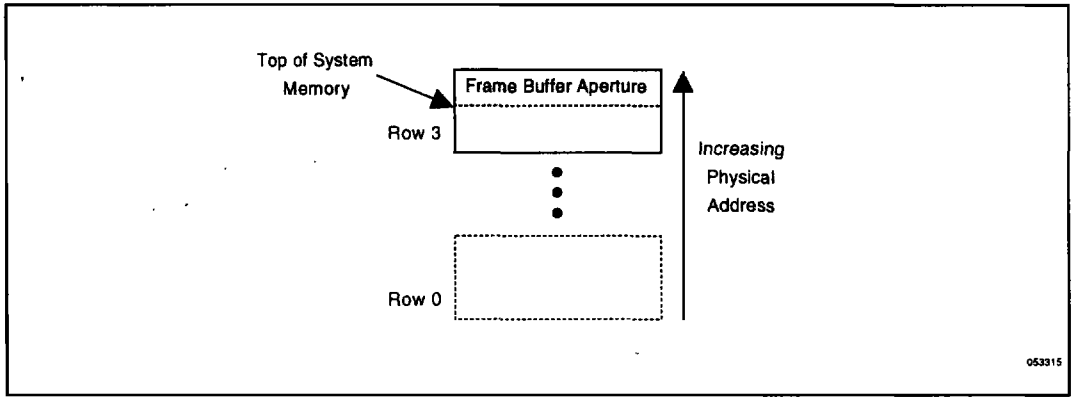


Figure 13. Physical Address Map for 4 Rows of DRAM

The top of system memory (Figure 14) refers to the top of memory reported to the operating system; memory above this may never be allocated by the operating system. The frame buffer aperture is located above the top of system memory.

Note that for systems with only 16 Mbytes of memory and that provide memory holes to support legacy devices that are mapped between 14 Mbytes and 16 Mbytes, the frame buffer must be mapped below the memory hole. The Intel 430VX PCIset supports 1-Mbyte or 2-Mbyte memory holes sizes. A 1-Mbyte hole is located from 15–16 Mbytes and 2-Mbyte holes is located from 14–16 Mbytes. For example, for a 1-Mbyte frame buffer and a memory hole of 2 Mbtes, the frame buffer must be mapped from 13–14 Mbytes and the memory hole is from 14–16 Mbytes. The top of system memory is 13 Mbytes. The GC obtains the size and location of SMB areas through the BIOS services. The Intel 430VX PCIset also supports an option that allows overlap between the SMB area and the memory hole. In this case, the Intel 430VX PCIset gives priority to the hole over the SMB area. All the CPU cycles within the hole and SMB area are forwarded down to PCI. The physical addresses for the hole should not be decoded by the GC on the PCI bus. The graphics driver should ensure that the CPU generates addresses above the top of DRAM. Figure 14 illustrates the mapping of the memory hole with the frame buffer mapped below the memory hole.

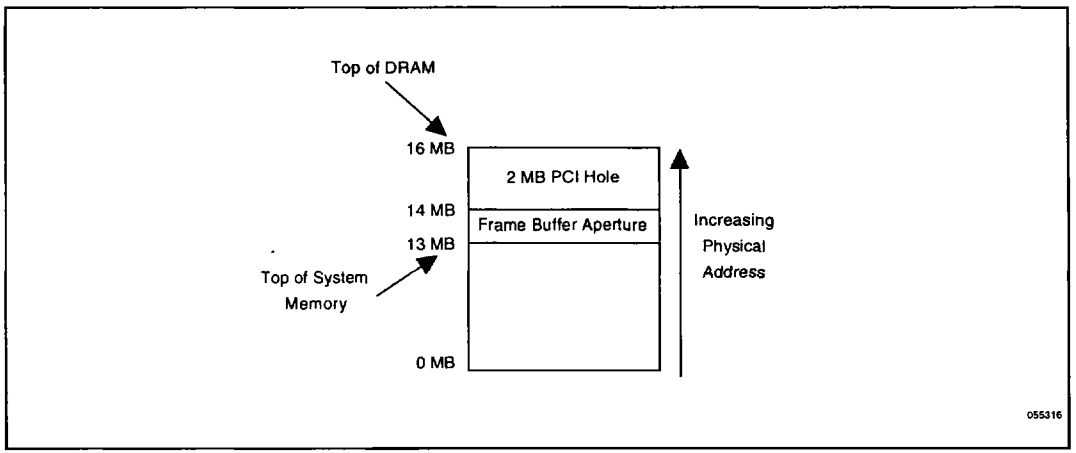


Figure 14. Frame Buffer with PCI Hole Enabled with 16-Mbyte system DRAM

4.7.2. CPU ACCESS TO SMB

The CPU has access to the entire DRAM address space including SMB. The system DRAM within the SMB address range is non-cacheable.

Note that the CPU may access the frame buffer via three different mechanisms. If the aperture is closed, addresses to the FB aperture directly above top of system memory are forwarded to PCI by the TVX. If the aperture is open, the TVX accesses the FB region above top of system memory directly. Bit 0 in the SMBCR register is used to direct CPU accesses to the FB aperature to either PCI or main memory. Also, the relocatable address range specified in the Device Independent Configuration Space can be used and the TVX forwards these cycles to PCI.

4.7.3. PCI MASTER ACCESS TO SMB

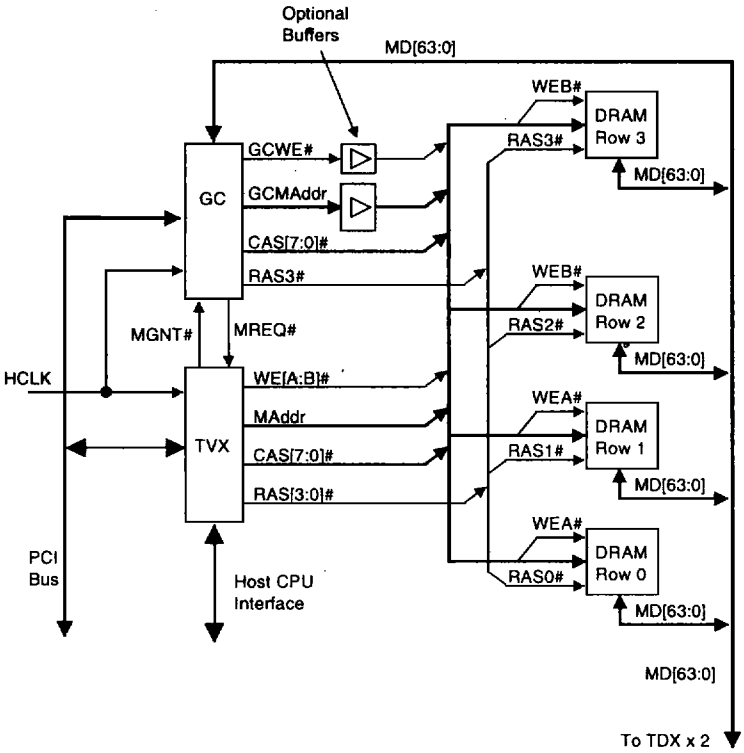
When the SMB space is enabled (Aperture can be either open or close) the TVX never responds to PCI master memory read/write cycles whose address fall above the top of main memory. Instead, these PCI cycles must be serviced by the GC which also resides on the PCI bus as a PCI slave (i.e., the GC should assert DEVSEL# to claim these cycles). The GC must map its frame buffer within the PCI address space at the same location it resides within the CPU address space.

4.7.4. GC (GRAPHICS CONTROLLER) ACCESS TO SMB

When the SMB space is enabled, the GC may have access to the frame buffer for screen refresh and draw operations directly at the DRAM interface through the MREQ#/MGNT# handshake mechanism. GC buffer-to-DRAM address bit mapping for the shared DRAM row(s) must match the TVX implementation for a one-to-one linear correspondence. The address mapping for the TVX is provided in the DRAM Interface Section.

4.7.5. SMB INTERFACE

Figure 15 shows the interconnection of TVX, GC, and memory using the EDO/SPM signals, in a 4-row system. In a 5-row system, the graphics controller would be connected to row 5 (i.e., RAS4#). Refer to the DRAM Organization section, in the DRAM Interface section, for additional details on a 5-row implementation.

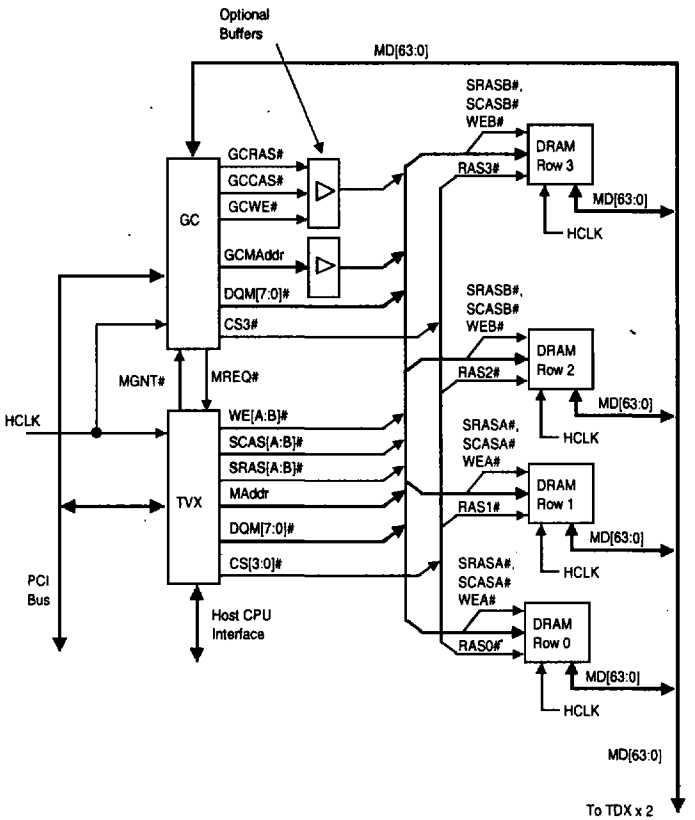


NOTES:

1. The rows of memory shown above represent logical rows. In an actual system, double sided SIMMs would be used. There are two SIMMs per row for a 64-bit memory interface.
2. If double-sided SIMM sockets are used on the motherboard, then the RAS3# from the GC and TVX should be tied to the first bank of the double-sided SIMM and RAS2# from the TVX should be tied to the second bank of the double-sided SIMM. This is required for supporting single-sided SIMMs populated in the double-sided SIMM sockets.
3. TVX provides two copies of WE# signal. Therefore, the GCWE# signal from GC needs to drive only two rows of memory.
4. The host bus clock is used by both the TVX and the GC to ensure correct operation of the synchronous memory bus arbitration protocol.
5. The buffers shown on GCMAddr and GCWE# are optional for loading purposes. The use of these buffers will degrade performance, take up real estate on the mother board, and also add to the system cost. The use of these external buffers is not recommended. TVX is designed to work with the memory array with integrated buffers.

Figure 15. SMB Interconnect for EDO/SPM Signals

Figure 16 shows the interconnection of TVX, GC, and memory using the SDRAM signals, in a 4-row system. In a 5-row system, the graphics controller would be connected to row 5 (i.e. CS5#). Refer to the DRAM Organization section, in the DRAM Interface section, for additional details on a 5-row implementation.



NOTES:

1. The rows of memory shown above represent logical rows. In an actual system, double-sided DIMMs would be used.
2. If a double-sided DIMM sockets are used on the motherboard, then the CS3# from the GC and TVX should be tied to the first bank of the double-sided DIMM and CS2# from the TVX should be tied to the second bank of the double-sided DIMM. This is required for supporting single-sided DIMMs populated in the double-sided DIMM sockets.
3. TVX provides two copies of WE#, SRAS#, and SCAS# signals. Therefore, the GCWE#, GCSRAS#, and GCSCAS# signals from GC needs to drive only two rows of memory.
4. The host bus clock is used by the TVX, the GC, and the SDRAM to ensure correct operation of the synchronous memory bus arbitration protocol. The memory interface of the GC must run at the same frequency as the host clock frequency.
5. The buffers shown on GCCAS#, GCRAS#, GCMAddr and GCWE# are optional for loading purposes. The use of these buffers will degrade performance, take up real estate on the mother board, and also add to the system cost. The use of these external buffers is not recommended. TVX is designed to work with the memory array with integrated buffers. (version buffered of the DIMMs is also not supported.)

Figure 16. SMB Interconnect for SDRAM Signals

4.7.6. SMBA ARBITRATION

The TVX SMBA arbitration mechanism uses a two-wire MREQ#/MGNT# protocol. The protocol signaling is synchronous to HCLK. The SMBA arbitration mechanism provides the following features:

- The TVX is the default owner (i.e., parked on the main memory DRAM bus)
- The GC has the ability to signal a low priority request or a high priority request using the MREQ# signal. The low priority request allows the system performance impact to be minimized, preventing unnecessary system resource stalls during non-critical GC accesses (i.e., performing draw operations or topping off of the GC's refresh FIFO). The high priority request provides a guaranteed latency for critical operations and should be used to prevent GC FIFO underruns or when visible graphics degradation occurs if the bus can not be acquired immediately (i.e., to prevent visible artifacts if the drawing engine is starving due to not being able to acquire the bus via a low priority request).
- The maximum latency seen by the graphics controller when asserting a high priority request is approximately 400ns (This is programmable. Refer to the TVX-to-GC Latency Control Management Section). The maximum latency seen for a low priority request is non-determinant since the TVX only responds to a low priority request if there are no CPU, PCI, or high priority refresh requests pending.

4.7.7. TVX-TO-GC LATENCY CONTROL MANAGEMENT

It is imperative that the memory controller (TVX) and graphics controller be sensitive to each other's latency and bandwidth requirements since overall system performance, visible artifacts, and/or limited functionality may result. This is an area where differentiation can play a large role in improving overall system capabilities and performance.

The Intel 430VX PCIset has been designed to make efficient use of the memory bus when it is the owner and to release the bus to the graphics controller with minimal latency. To help control this latency the TVX provides a programmable timer (GCLT Register) that limits the number of non-GC DRAM cycles that can be completed after a high priority GC request has been sampled on the MREQ# pin. This timer maximizes efficient use of the TVX buffering so that non-GC cycles that involve main memory can continue on during GC DRAM accesses, using up available internal buffering.

The programmable GC latency timer is used to determine when to give up DRAM (on PCI reads and CPU/PCI writes) when a high priority GC request is asserted. For PCI reads, the idea is to give up the bus (only after the GC high priority request has been sampled active), as soon as DRAM is not being used efficiently (i.e., PCI Pre-fetch buffers are full), or the GC latency timer times-out, which ever occurs first. For PCI-to-DRAM single writes, the DRAM is relinquished when the GC latency timer times-out (after the current cycle has been written to DRAM from the DRAM write buffers), or the DRAM write buffers become empty, whichever occurs first. The GC latency timer is used for PCI-to-DRAM reads (burst or single), PCI-to-DRAM single writes (Note: CPU/PCI burst writes always break on line boundaries when a high priority GC request is active), and CPU-to-DRAM single writes.

The GC latency timer begins counting when the GC high priority request is sampled active and a PCI master is reading or writing to DRAM or the CPU is writing to DRAM. The timer can be programmed to 0, 4, 8, 12, 16, 20, 24, and 28 HCLKs (defaults to 12 for CPU/PCI writes and 16 for PCI reads). For PCI reads, the default value will guarantee that at least a line will be read from DRAM before DRAM is given to the GC. For PCI/CPU single writes, the idea is to allow four single writes (page hits) to drain from the DRAM Write Buffers before giving DRAM to the GC. This potentially opens up the DRAM write buffers for posting when the GC has DRAM. The default values for this timer are set to guarantee that the maximum latency seen by the graphics controller is approximately 400ns. The programmability is provided for performance timing purposes. Programmability in the TRDY timer (TPDT Register) has also been provided for performance timing purposes. The TRDY timer is used to determine how long the Intel 430VX PCIset waits before disconnecting the PCI transfer.

4.8. Clock Generation and Distribution

The TVX and CPU should be clocked from one clock driver output to minimize skew between the CPU and TVX. The TDXs should share another clock driver output.

4.8.1. RESET SEQUENCING

The TVX is asynchronously reset by the CPU RESET signal. After RESET is negated, the TVX resets the two TDXs by driving HOE#=MOE#=POE#=1 and MADV#=0 for two HCLKs. The TVX changes HOE#, MOE#, POE# and MADV# to their default value synchronous to HCLK.

Arbiter (Central Resource) Functions on Reset

The TVX arbiter includes support for PCI central resource functions. These functions include driving the AD[31:0], C/BE[3:0]#, and PAR signals when no one is granted the PCI bus and the bus is idle. The TVX drives 0s on these signals during these times, plus during RESET.

5.0. PINOUT AND PACKAGE INFORMATION

5.1. TVX Pinout

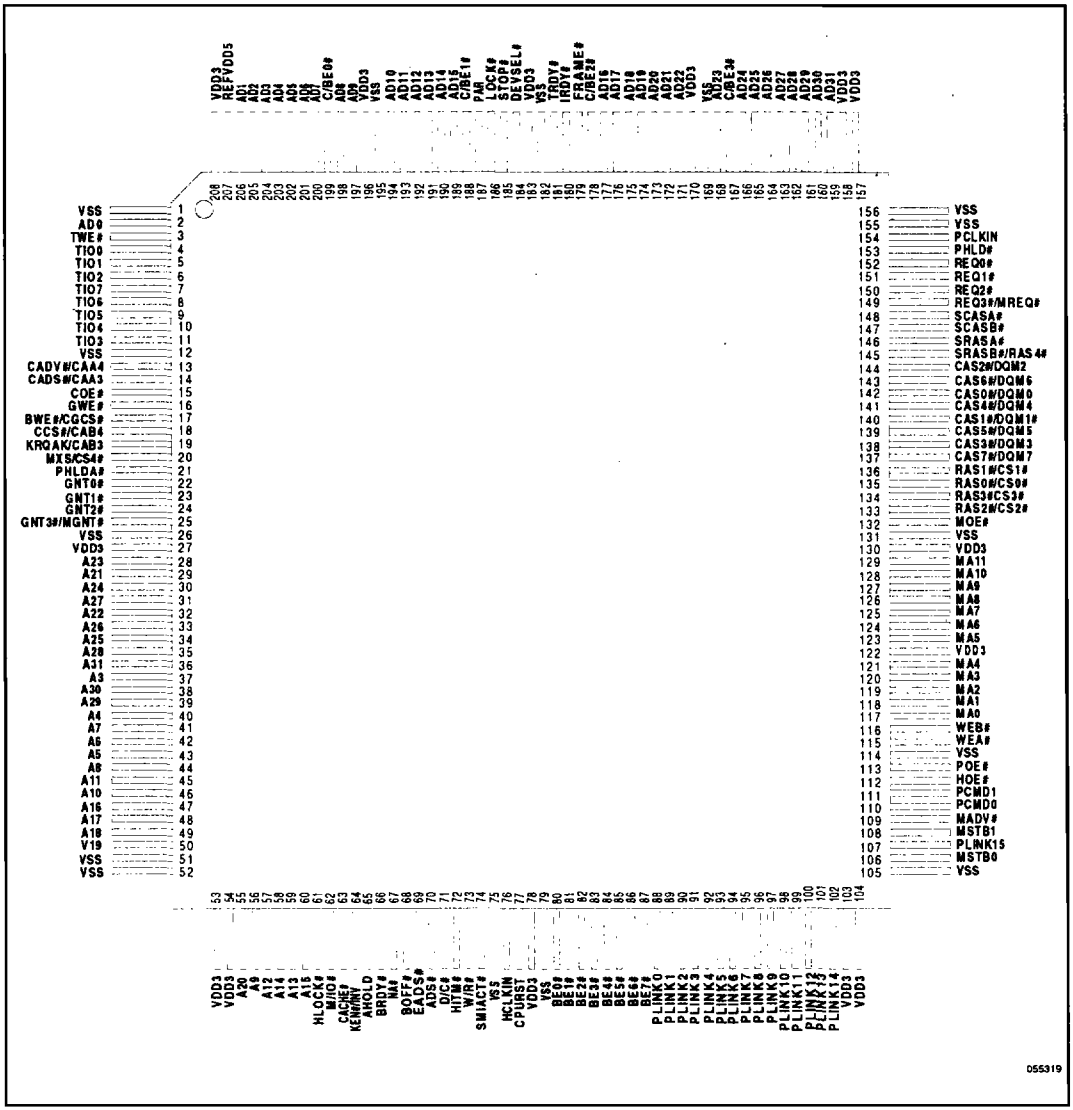


Figure 17. TVX Pinout

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
A3	37	I/O
A4	40	I/O
A5	43	I/O
A6	42	I/O
A7	41	I/O
A8	44	I/O
A9	56	I/O
A10	46	I/O
A11	45	I/O
A12	57	I/O
A13	59	I/O
A14	58	I/O
A15	60	I/O
A16	47	I/O
A17	48	I/O
A18	49	I/O
A19	50	I/O
A20	55	I/O
A21	29	I/O
A22	32	I/O
A23	28	I/O
A24	30	I/O
A25	34	I/O
A26	33	I/O
A27	31	I/O
A28	35	I/O
A29	39	I/O
A30	38	I/O
A31	36	I/O

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
AD0	2	I/O
AD01	206	I/O
AD02	205	I/O
AD03	204	I/O
AD04	203	I/O
AD05	202	I/O
AD06	201	I/O
AD07	200	I/O
AD08	198	I/O
AD09	197	I/O
AD10	194	I/O
AD11	193	I/O
AD12	192	I/O
AD13	191	I/O
AD14	190	I/O
AD15	189	I/O
AD16	177	I/O
AD17	176	I/O
AD18	175	I/O
AD19	174	I/O
AD20	173	I/O
AD21	172	I/O
AD22	171	I/O
AD23	168	I/O
AD24	166	I/O
AD25	165	I/O
AD26	164	I/O
AD27	163	I/O
AD28	162	I/O

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
AD29	161	I/O
AD30	160	I/O
AD31	159	I/O
ADS#	70	I
AHOLD	65	O
BE0#	80	I
BE1#	81	I
BE2#	82	I
BE3#	83	I
BE4#	84	I
BE5#	85	I
BE6#	86	I
BE7#	87	I
BOFF#	68	O
BRDY#	66	O
BWE#/CGCS#	17	O
C/BE0#	199	I/O
C/BE1#	188	I/O
C/BE2#	178	I/O
C/BE3#	167	I/O
CACHE#	63	I
CADS#/CAA3	14	O
CADV#/CAA4	13	O
CAS0#/DQM0	142	O
CAS1#/DQM1	140	O
CAS2#/DQM2	144	O
CAS3#/DQM3	138	O
CAS4#/DQM4	141	O
CAS5#/DQM5	139	O

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
CAS6#/DQM6	143	O
CAS7#/DQM7	137	O
CCS#/CAB4	18	O
COE#	15	O
CPURST	77	I
D/C#	71	I
DEVSEL#	184	I/O
EADS#	69	O
FRAME#	179	I/O
GNT0#	22	O
GNT1#	23	O
GNT2#	24	O
GNT3#/MGNT#	25	O
GWE#	16	O
HCLKIN	76	I
HITM#	72	I
HLOCK#	61	I
HOE#	112	O
IRDY#	180	I/O
KEN#/INV	64	O
KRQAK/CAB3	19	I/O
LOCK#	186	I/O
M/IO#	62	I
MA0	117	O
MA1	118	O
MA2	119	O
MA3	120	O
MA4	121	O
MA5	123	O
MA6	124	O

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
MA7	125	O
MA8	126	O
MA09	127	O
MA10	128	O
MA11	129	O
MADV#	109	O
MOE#	132	O
MSTB0	106	O
MSTB1	108	O
MXS/CS4#	20	O
NA#	67	O
PAR	187	I/O
PCLKIN	154	I
PCMD0	110	O
PCMD1	111	O
PHLD#	153	I
PHLDA#	21	O
PLINK00	88	I/O
PLINK1	89	I/O
PLINK2	90	I/O
PLINK3	91	I/O
PLINK4	92	I/O
PLINK5	93	I/O
PLINK6	94	I/O
PLINK7	95	I/O
PLINK8	96	I/O
PLINK9	97	I/O
PLINK10	98	I/O
PLINK11	99	I/O
PLINK12	100	I/O

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
PLINK13	101	I/O
PLINK14	102	I/O
PLINK15	107	I/O
POE#	113	O
RAS0#/CS0#	135	O
RAS1#/CS1#	136	O
RAS2#/CS2#	133	O
RAS3#/CS3#	134	O
REFVDD5	207	—
REQ0#	152	I
REQ1#	151	I
REQ2#	150	I
REQ3#/MREQ#	149	I
SCASA#	148	O
SCASB#	147	O
SMIACT#	74	I
SRASA#	146	O
SRASB#/RAS4#	145	O
STOP#	185	I/O
TIO0	4	I/O
TIO1	5	I/O
TIO2	6	I/O
TIO3	11	I/O
TIO4	10	I/O
TIO5	9	I/O
TIO6	8	I/O
TIO7	7	I/O
TRDY#	181	I/O
TWE#	3	O
VDD3	27	—

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
VDD3	53	—
VDD3	54	—
VDD3	78	—
VDD3	103	—
VDD3	104	—
VDD3	122	—
VDD3	130	—
VDD3	157	—
VDD3	158	—
VDD3	170	—
VDD3	183	—

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
VDD3	196	—
VDD3	208	—
VSS	1	—
VSS	12	—
VSS	26	—
VSS	51	—
VSS	52	—
VSS	75	—
VSS	79	—
VSS	105	—
VSS	114	—

Table 18. TVX Alphabetical Pin List

Name	Pin	Type
VSS	131	—
VSS	155	—
VSS	156	—
VSS	169	—
VSS	182	—
VSS	195	—
W/R#	73	I
WEA#	115	O
WEB#	116	O

5.2. TDX Pinout

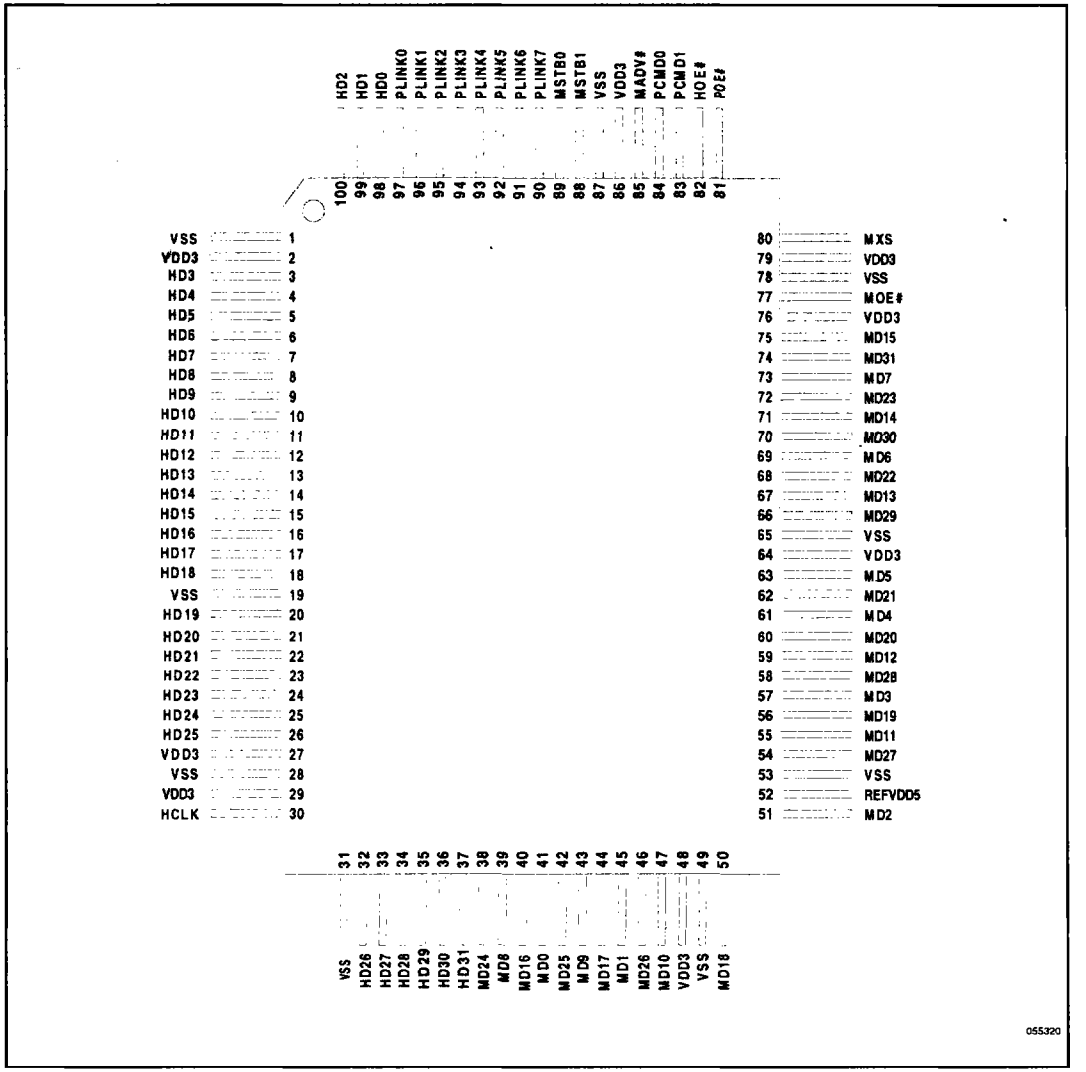


Figure 18. TDX Pinout

Table 19. TDX Alphabetical Pin List

Name	Pin	Type
HCLK	30	I
HD0	98	I/O
HD1	99	I/O
HD2	100	I/O
HD3	3	I/O
HD4	4	I/O
HD5	5	I/O
HD6	6	I/O
HD7	7	I/O
HD8	8	I/O
HD9	9	I/O
HD10	10	I/O
HD11	11	I/O
HD12	12	I/O
HD13	13	I/O
HD14	14	I/O
HD15	15	I/O
HD16	16	I/O
HD17	17	I/O
HD18	18	I/O
HD19	20	I/O
HD20	21	I/O
HD21	22	I/O
HD22	23	I/O
HD23	24	I/O
HD24	25	I/O
HD25	26	I/O
HD26	32	I/O
HD27	33	I/O

Table 19. TDX Alphabetical Pin List

Name	Pin	Type
HD28	34	I/O
HD29	35	I/O
HD30	36	I/O
HD31	37	I/O
HOE#	82	I
MADV#	85	I
MD0	41	I/O
MD1	45	I/O
MD2	51	I/O
MD3	57	I/O
MD4	61	I/O
MD5	63	I/O
MD6	69	I/O
MD7	73	I/O
MD8	39	I/O
MD9	43	I/O
MD10	47	I/O
MD11	55	I/O
MD12	59	I/O
MD13	67	I/O
MD14	71	I/O
MD15	75	I/O
MD16	40	I/O
MD17	44	I/O
MD18	50	I/O
MD19	56	I/O
MD20	60	I/O
MD21	62	I/O
MD22	68	I/O

Table 19. TDX Alphabetical Pin List

Name	Pin	Type
MD23	72	I/O
MD24	38	I/O
MD25	42	I/O
MD26	46	I/O
MD27	54	I/O
MD28	58	I/O
MD29	66	I/O
MD30	70	I/O
MD31	74	I/O
MOE#	77	I
MSTB0	89	I
MSTB1	88	I
MXS	80	I
PCMD0	84	I
PCMD1	83	I
PLINK0	97	I/O
PLINK1	96	I/O
PLINK2	95	I/O
PLINK3	94	I/O
PLINK4	93	I/O
PLINK5	92	I/O
PLINK6	91	I/O
PLINK7	90	I/O
POE#	81	I
REFVDD5	52	—
VDD3	2	—
VDD3	27	—
VDD3	29	—
VDD3	48	—

Table 19. TDX Alphabetical Pin List

Name	Pin	Type
VDD3	64	—
VDD3	76	—
VDD3	79	—
VDD3	86	—
VSS	1	—

Table 19. TDX Alphabetical Pin List

Name	Pin	Type
VSS	19	—
VSS	28	—
VSS	31	—
VSS	49	—
VSS	53	—

Table 19. TDX Alphabetical Pin List

Name	Pin	Type
VSS	65	—
VSS	78	—
VSS	87	—

5.3. TVX Package Dimensions

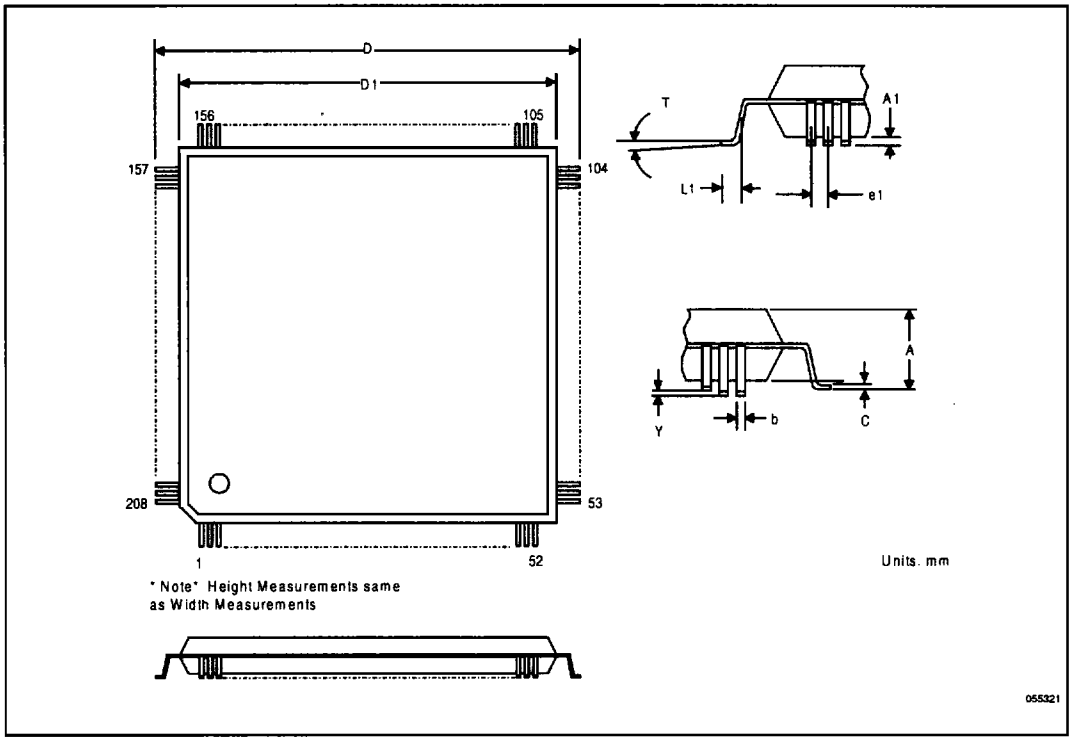


Figure 19. TVX Package Dimensions (208-Pin QFP)

Table 20. TVX Package Dimensions (208-Pin QFP)

Symbol	Description	Value (mm)
A	Seating Height	4.25 (max)
A1	Stand-off	0.05 (min); 0.40 (max)
b	Lead Width	0.2 ± 0.10
C	Lead Thickness	0.15 +0.1/-0.05
D	Package Length and Width, including pins	30.6 ± 0.4
D1	Package Length and Width, excluding pins	28 ± 0.2
e1	Linear Lead Pitch	0.5 ± 0.1
Y	Lead Coplanarity	0.08 (max)
L1	Foot Length	0.5 ± 0.2
T	Lead Angle	0° - 10°

5.4. TDX Package Dimensions

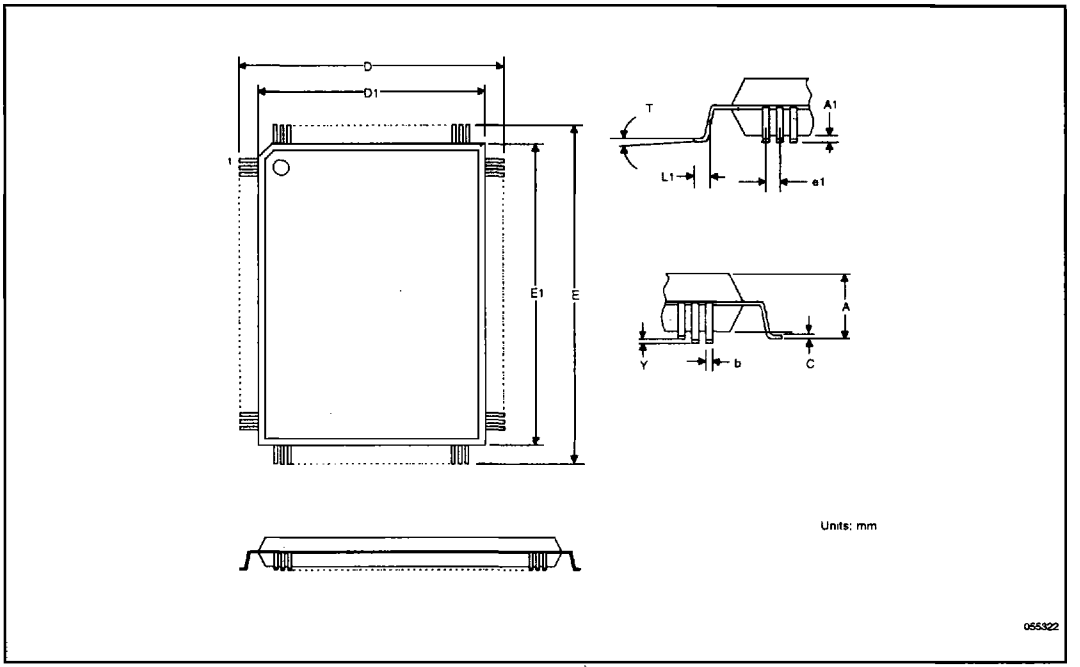


Figure 20. TDX Package Dimensions (100-Pin QFP)

Table 21. TDX Package Dimensions (100-Pin QFP)

Symbol	Description	Value (mm)
A	Seating Height	3.3 (max)
A1	Stand-off	0.0 (min); 0.50 (max)
b	Lead Width	0.3 ± 0.10
C	Lead Thickness	0.15 +0.1/-0.05
D	Package Width, including pins	17.9 ± 0.4
D1	Package Width, excluding pins	14 ± 0.2
E	Package Length, including pins	23.9 ± 0.4
E1	Package Length, excluding pins	20 ± 0.2
e1	Linear Lead Pitch	0.65 ± 0.12
Y	Lead Coplanarity	0.1 (max)
L1	Foot Length	0.8 ± 0.2
T	Lead Angle	0^{o} - 10^{o}

6.0. TESTABILITY

6.1. 82437VX TVX Testability

The test modes of TVX are summarized briefly in the following table and are described in detail in the later sections.

The test modes are decoded from REQ[3:0]# and qualified with the CPURST pin. TVX test mode selection is asynchronous. These signals need to remain in their respective states for the duration of the test mode

Table 22. TVX Test Mode Summary

Test Mode	Detection of Mode	Description
NAND Tree	CPURST = '1' AND REQ[2:0]# = "000"	Enable NAND chain
IDCODE A	CPURST = '1' AND REQ[2:0]# = "110"	Drive out Revision ID and Device ID on AD lines
IDCODE B	CPURST = '1' AND REQ[2:0]# = "010"	Drive out Manufacturing ID on AD lines
TRISTATE MODE	CPURST = '1' AND REQ[2:0]# = "100"	Float all outputs and disable pullups, pull downs

6.1.1. TVX NAND TREE MODE

Two NAND trees are provided in the TVX for Automated Test Equipment (ATE) board level testing. The NAND trees allow the tester to test the connectivity of each of the TVX signal pins. While in NAND tree mode, all TVX drivers except for GNT2# and GNT1# are tri-stated. The NAND tree outputs are on GNT2# and GNT1#. NAND chain testing should be performed at 1 MHz (1000 ns ATE tester period). Allow 1000ns for the input signals to propagate to the NAND tree outputs.

NAND chain #1 begins at MA8 and is routed counter-clockwise around the chip to its output on GNT1#. NAND chain #2 begins at MA7 and is routed clockwise around the chip to its output on GNT2#. The NAND chain skips CPURST, REQ2#, REQ1#, and REQ0# which are used to detect the NAND tree test mode.

Enter the NAND chain mode by driving CPURST to 1 and REQ[2:0]# = 000. To perform the NAND tree test after entering this mode, all pins included in the NAND trees should be driven to 1. Beginning at the tree output nearest the respective observability points (i.e. start with GNT0# and GNT3#), walk a zero toward the end of each chain. As pins are toggled, the resulting ripple is observed on the corresponding NAND tree's output. Since the NAND tree test mode is selected asynchronously, REQ[2:0]# and CPURST must be stable for the duration of the test.

Table 23. TVX NAND TREE ONE

Tree output	Pin #	Pin Name	Comments
	23	GNT1#	GNT1# is output of NAND chain #1
1	22	GNT0#	Last input to chain. This pin is logically closest to GNT1#, output of chain 1.
2	21	PHLDA#	
3	20	MXS/ CS4#	
4	19	KRQAK CAB3	
5	18	CCS#/ CAB4	
6	17	BWE#/ CGCS#	
7	16	GWE#	
8	15	COE#	
9	14	CADS#/ CAA3	
10	13	CADV#/ CAA4	
11	11	TIO3	
12	10	TIO4	
13	9	TIO5	
14	8	TIO6	
15	7	TIO7	
16	6	TIO2	
17	5	TIO1	
18	4	TIO0	
19	3	TWE#	
20	2	AD0	
21	206	AD1	
22	205	AD2	

Table 23. TVX NAND TREE ONE

Tree output	Pin #	Pin Name	Comments
23	204	AD3	
24	203	AD4	
25	202	AD5	
26	201	AD6	
27	200	AD7	
28	199	C/BE0#	
29	198	AD8	
30	197	AD9	
31	194	AD10	
32	193	AD11	
33	192	AD12	
34	191	AD13	
35	190	AD14	
36	189	AD15	
37	188	C/BE1#	
38	187	PAR	
39	186	LOCK#	
40	185	STOP#	
41	184	DEVSEL#	
42	181	TRDY#	
43	180	IRDY#	
44	179	FRAME#	
45	178	C/BE2#	
46	177	AD16	
47	176	AD17	
48	175	AD18	
49	174	AD19	
50	173	AD20	
51	172	AD21	

Table 23. TVX NAND TREE ONE

Tree output	Pin #	Pin Name	Comments
52	171	AD22	
53	168	AD23	
54	167	C/BE3#	
55	166	AD24	
56	165	AD25	
57	164	AD26	
58	163	AD27	
59	162	AD28	
60	161	AD29	
61	160	AD30	
62	159	AD31	
63	154	PCLKIN	
64	153	PHLD#	
65	149	REQ3#	
66	148	SCASA#	
67	147	SCASB#	
68	146	SRASA#	
69	145	SRASB#/ RAS4#	
70	144	CAS2#/ DQM2	
71	143	CAS6#/ DQM6	
72	142	CAS0#/ DQM0	

Table 23. TVX NAND TREE ONE

Tree output	Pin #	Pin Name	Comments
73	141	CAS4#/ DQM4	
74	140	CAS1#/ DQM1	
75	139	CAS5#/ DQM5	
76	138	CAS3#/ DQM3	
77	137	CAS7#/ DQM7	
78	136	RAS1#/ CS1#	
79	135	RAS0#/ CS0#	
80	134	RAS3#/ CS3#	
81	133	RAS2#/ CS2#	
82	132	MOE#	
83	129	MA11	
84	128	MA10	
85	127	MA9	
86	126	MA8	MA8 is input to NAND chain #1. First input in the chain, logically farthest from output point at GNT1#

Table 24. TVX NAND TREE TWO

Tree output	Pin #	Pin Name	Comments
	24	GNT2#	GNT2# is the output of NAND chain #2
1	25	GNT3#/ MGNT#	Last input to chain. This pin is logically closest to GNT2#, output of chain 2.
2	28	A23	
3	29	A21	
4	30	A24	
5	31	A27	
6	32	A22	
7	33	A26	
8	34	A25	
9	35	A28	
10	36	A31	
11	37	A3	
12	38	A30	
13	39	A29	
14	40	A4	
15	41	A7	
16	42	A6	
17	43	A5	
18	44	A8	
19	45	A11	
20	46	A10	
21	47	A16	
22	48	A17	
23	49	A18	
24	50	A19	

Table 24. TVX NAND TREE TWO

Tree output	Pin #	Pin Name	Comments
25	55	A20	
26	56	A9	
27	57	A12	
28	58	A14	
29	59	A13	
30	60	A15	
31	61	HLOCK#	
32	62	M/IO#	
33	63	CACHE#	
34	64	KEN#/INV	
35	65	AHOLD	
36	66	BRDY#	
37	67	NA#	
38	68	BOFF#	
39	69	EADS#	
40	70	ADS#	
41	71	D/C#	
42	72	HITM#	
43	73	W/R#	
44	74	SMIACT#	
45	76	HCLKIN	
46	80	BE0#	
47	81	BE1#	
48	82	BE2#	
49	83	BE3#	
50	84	BE4#	
51	85	BE5#	
52	86	BE6#	
53	87	BE7#	
54	88	PLINK0	

Table 24. TVX NAND TREE TWO

Tree output	Pin #	Pin Name	Comments
55	89	PLINK1	
56	90	PLINK2	
57	91	PLINK3	
58	92	PLINK4	
59	93	PLINK5	
60	94	PLINK6	
61	95	PLINK7	
62	96	PLINK8	
63	97	PLINK9	
64	98	PLINK10	
65	99	PLINK11	
66	100	PLINK12	
67	101	PLINK13	
68	102	PLINK14	
69	106	MSTB0#	
70	107	PLINK15	
71	108	MSTB1#	
72	109	MADV#	

Table 24. TVX NAND TREE TWO

Tree output	Pin #	Pin Name	Comments
73	110	PCMD0	
74	111	PCMD1	
75	112	HOE#	
76	113	POE#	
77	115	WEA#	
78	116	WEB#	
79	117	MA0	
80	118	MA1	
81	119	MA2	
82	120	MA3	
83	121	MA4	
84	123	MA5	
85	124	MA6	
86	125	MA7	MA7 is input to NAND chain #2. First input in the chain, logically farthest from output point at GNT2#.

Figure 22 is a schematic of the NAND Tree 1 circuitry. Figure 23 is a schematic of the NAND Tree 2 circuitry.

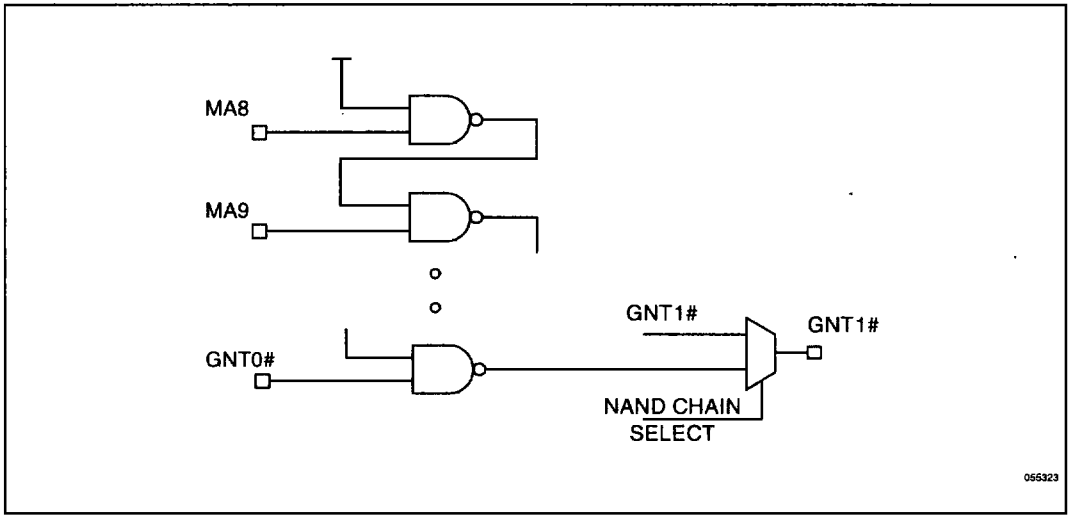


Figure 21. 82437VX NAND Tree Diagram

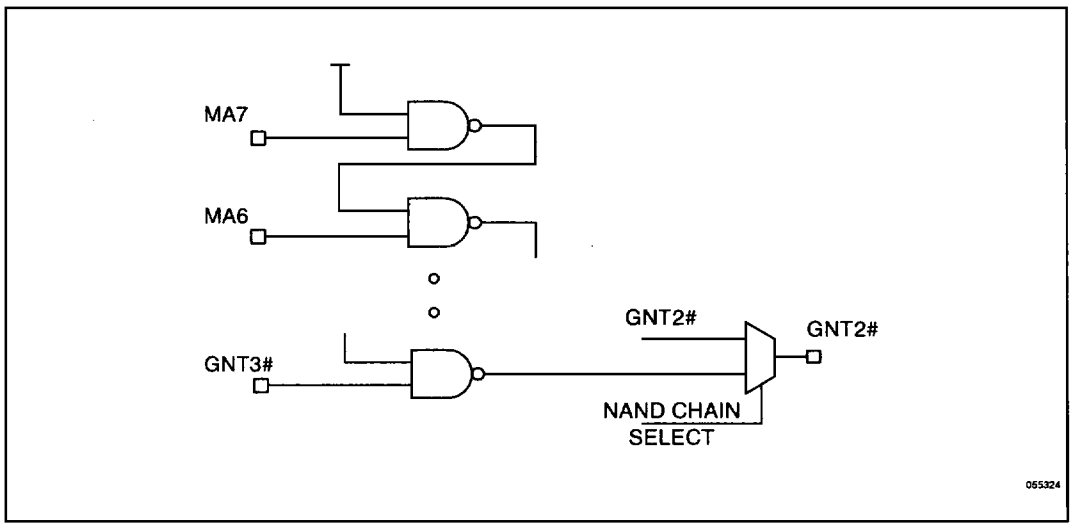


Figure 22. 82437VX NAND Tree Diagram

6.1.2. TVX ID CODE EXTRACTION

The two ID Code test modes provide a simple method of checking information stored in the TVX's read-only configuration registers at 02–03h and 08h. Like the other test modes, ID CODE is entered when TVX detects particular patterns on REQ[2:0]# with CPURST active. Selection of this mode is asynchronous; when REQ# pattern changes or CPURST is negated, the ID CODE mode is exited.

Table 25. TVX ID Code Test Modes

MODE	REQ[2:0]# detect pattern	Action
ID CODE A	110	Device ID driven on AD[31:16] (contents config reg 02-03h). Revision ID driven on AD[7:0] (contents config reg 08h)
ID CODE B	010	Manufacturing ID driven on AD[31:0]

6.1.3. TVX TRI-STATE MODE

Tri-state mode is entered when TVX detects 100 on REQ[2:0]# and CPURST is active. In this mode all TVX output drivers are tri-stated and internal buffer pull-ups and pull-downs are disabled. Selection of this mode is asynchronous; when REQ# pattern changes or CPURST is negated, the TRISTATE mode is exited.

6.2. 82438VX TDX Testability

For the TDX, test modes are selected following synchronous detection of the TDX reset combination on HOE#, MOE#, POE#, and MADV#. Value on MSTB[1:0] selects the Test Mode from the test options available.

Table 26. TDX Test Mode Summary

Test Mode	Detection of Mode	Description
NAND Tree	1. Detect RESET (i.e., two samples of HOE#, MOE#, POE# = 111 and MADV# = 0, with MSTB[1:0] = 00.) 2. Hold HCLK = 0 during NAND chain toggle.	Enable NAND chain, observe output on MD0
Manufacturing ID Code	1. Detect RESET (i.e., two samples of HOE#, MOE#, POE# = 111 and MADV# = 0, with MSTB[1:0] = 01.) 2. Perform walking one sequence from HD0 to HD19.	Drive out Manufacturing ID and part revision on MD0 in response to sequence driven in on HD[19:0]
TRISTATE MODE	1. Detect RESET (i.e., two samples of HOE#, MOE#, POE# = 111 and MADV# = 0.) 2. Negate MADV# to 1 while continuing to drive HOE#, MOE# and POE# to 111. Main busses will remain in tri-state mode.	Float all outputs
Pull-down Disable	1. Detect RESET (i.e., two samples of HOE#, MOE#, POE# = 111 and MADV# = 0, with MSTB[1:0] = 11.) 2. Pulldowns will remain disabled until another reset is detected.	Disable pull-downs

6.2.1. TDX NAND TREE MODE

The TDX has a single NAND tree provided for board level connectivity testing. While in NAND tree mode, all TDX pins except MD0 are tri-stated. The NAND tree output is observed on MD0 (pin 41). NAND chain testing should be performed at 1 MHz (1000 ns ATE tester period). Allow 1000ns for the input signals to propagate to the NAND tree outputs.

The NAND chain begins at HD3 and is routed counterclockwise around the part, ending at HD2. The NAND chain skips HCLK. HCLK connectivity is verified by correctly detecting RESET and entering NAND chain mode.

After entering NAND chain mode, drive all NAND chain inputs, including HOE#, POE#, MOE#, and MADV#, to 1. Since this test mode is synchronously evoked, HCLK should be driven to 0 for the duration of the test. Clocking the part causes the TDX to exit NAND tree test mode. Starting at HD2, walk a zero back through the chain toward the origin at HD3. As each pin is toggled, the resultant ripple is observed on MD0.

Table 27. TDX NAND Tree

Tree Output	PIN	Pin Name	Comments
	41	MD0	Output of NAND Chain, test mode observability point
	100	HD2	Last input pin to NAND chain, logically closest to chain output. Output observed on MD0
	99	HD1	
	98	HD0	
	97	PLINK0	
	96	PLINK1	
	95	PLINK2	
	94	PLINK3	
	93	PLINK4	
	92	PLINK5	
	91	PLINK6	
	90	PLINK7	
	89	MSTB0	
	88	MSTB1	
	85	MADV#	
	84	PCMD0	
	83	PCMD1	

Table 27. TDX NAND Tree

Tree Output	PIN	Pin Name	Comments
	82	HOE#	
	81	POE#	
	80	MXS	
	77	MOE#	
	75	MD15	
	74	MD31	
	73	MD7	
	72	MD23	
	71	MD14	
	70	MD30	
	69	MD6	
	68	MD22	
	67	MD13	
	66	MD29	
	63	MD5	
	62	MD21	
	61	MD4	
	60	MD20	
	59	MD12	
	58	MD28	
	57	MD3	

Table 27. TDX NAND Tree

Tree Output	PIN	Pin Name	Comments
	56	MD19	
	55	MD11	
	54	MD27	
	51	MD2	
	50	MD18	
	47	MD10	
	46	MD26	
	45	MD1	
	44	MD17	
	43	MD9	
	42	MD25	
	40	MD16	
	39	MD8	
	38	MD24	
	37	HD31	
	36	HD30	
	35	HD29	
	34	HD28	
	33	HD27	
	32	HD26	
	26	HD25	
	25	HD24	
	24	HD23	
	23	HD22	

Table 27. TDX NAND Tree

Tree Output	PIN	Pin Name	Comments
	22	HD21	
	21	HD20	
	20	HD19	
	18	HD18	
	17	HD17	
	15	HD16	
	15	HD15	
	14	HD14	
	13	HD13	
	12	HD12	
	11	HD11	
	10	HD10	
	9	HD9	
	8	HD8	
	7	HD7	
	6	HD6	
	5	HD5	
	4	HD4	
	3	HD3	Start of NAND Chain. HD3 is at the logical end of the chain, furthest from the output point at MD0

Figure 23 is a schematic of the NAND Tree circuitry.

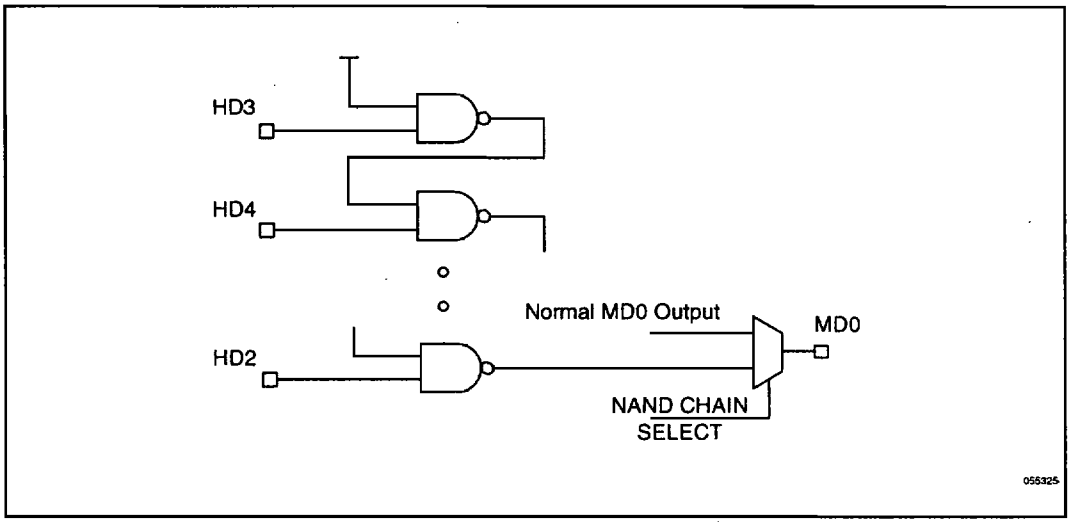


Figure 23. 82438VX NAND-Tree Diagram

6.2.2. TDX ID CODE EXTRACTION

The TDX does not have any addressable register space. Revision identification and manufacturing ID are obtainable only through use of a test mode. To enter this mode, MSTB[1:0] should be held to '01' while resetting the part. Apply 00000h to HD[19:0]. Walk a one, once per test cycle, ascending from HD0 to HD19. The combined revision ID and manufacturing ID are sequenced out on MD0. The resultant binary stream is broken down as follows:

Bit 19 bit 16	bit 15 bit 0
Revision ID	**Manufacturing ID**

The Revision ID (bits [19:16]) for TDX A-0 is 0h. The Manufacturing ID (bits [15:0]) will read 0F20h, identical to the TVX.

6.2.3. TDX TRI-STATE MODE

The HD, MD, and PLINK bus buffer control is provided at the periphery through HOE#, MOE# and POE# respectively. Following the normal reset sequence, where HOE#, MOE#, and POE#=111 and MADV#=0 for two consecutive HCLK's, MADV# can be negated to 1 and the TDX remains in tri-state mode. Normally, MSTB[1:0] are driven to 00 during reset. If these pins are driven to 11 during reset, the pull down resistors on the HD and MD busses are also disabled. The HD and MD pull downs can be re-enabled using the normal reset sequence where MSTB[1:0] are 00.