82424ZX CACHE AND DRAM CONTROLLER (CDC)

- Supports 25/33 MHz Intel486™ SX, Intel487™ SX, Intel486 DX, Intel486 DX2, IntelDX4™, OverDrive™ for Intel486 and OverDrive for DX2 Processors
- Fully Backward Compatible with Intel 82424TX
- Synchronous, 25/33 MHz PCI Bus Interface Capable of Supporting Bus Masters
- Supports OverDrive Upgrade Socket
- Programmable Attribute Map for First 1 MByte of Main Memory
- Posted Write Buffers for Improved Performance
- Integrated DRAM Controller
  - 2 to 160 MByte Main Memory Using 70 ns Fast Page Mode SIMM Memory
  - Decoupled Refresh Cycles to Reduce DRAM Access Latency
- Integrated Cache Controller
  - Write-Through and Write-Back Cache Options
  - 64 KB, 128 KB, 256 KB, and 512 KB Cache Sizes Using Standard SRAMS
  - Burst Line Fill of 2-1-1-1 from Secondary Cache at 25 and 33 MHz
  - Zero Wait-State Write to L2 Cache for a Cache Write Hit
  - Main Memory Posting at Zero Wait-States, Enabling Optimum Write-Through Cache Performance
  - Concurrent Cache Line Replacement from Secondary Cache in Write-Back Mode
- PCI Bridge
  - Translates CPU Cycles into PCI Bus Cycles
  - Translates Back-to-Back Sequential Memory Write Cycles into PCI Burst Cycles
  - Separate PCI-to-Main Memory Port Allows Concurrent/Independent CPU and PCI Bus Operations
  - Zero Wait-State Write Posting into the DPU for Fast Graphics Transfers
  - Integrated Snoop Filter
- Complete Support for SL Enhanced Intel486 CPUs
  - SMM Space Remapping to TOM, A0000 and B0000 Segments
  - Stop Grant Cycle Translation from Host-to-PCI Bus

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The 82424ZX Cache DRAM Controller (CDC) integrates the cache and main memory DRAM control functions and provides the address paths and bus control for transfers between the Host (CPU/cache), main memory, and the Peripheral Component Interconnect (PCI) Bus. The 82424ZX is completely backward compatible with the 82424TX. The Dual-ported architecture permits concurrent operations on the Host and PCI Buses. The cache controller supports both write-through and write-back cache policies and cache sizes from 64 to 512 KBytes. The cache memory can be implemented using standard asynchronous SRAMs. The dual-ported main memory DRAM controller interfaces DRAM to the Host Bus and the PCI Bus. The CDC supports a two-way interleaved DRAM organization for optimum performance. The CDC is intended to be used with the 82423TX Data Path Unit (DPU). The DPU provides 32-bit data paths between the Host, main memory, and the PCI. Together, these two components provide a full function dual-port data path connection to main memory and form a Host/PCI Bridge.

The complete document for this product can be ordered by calling 1-800-548-4725 and ask for order number 290467.

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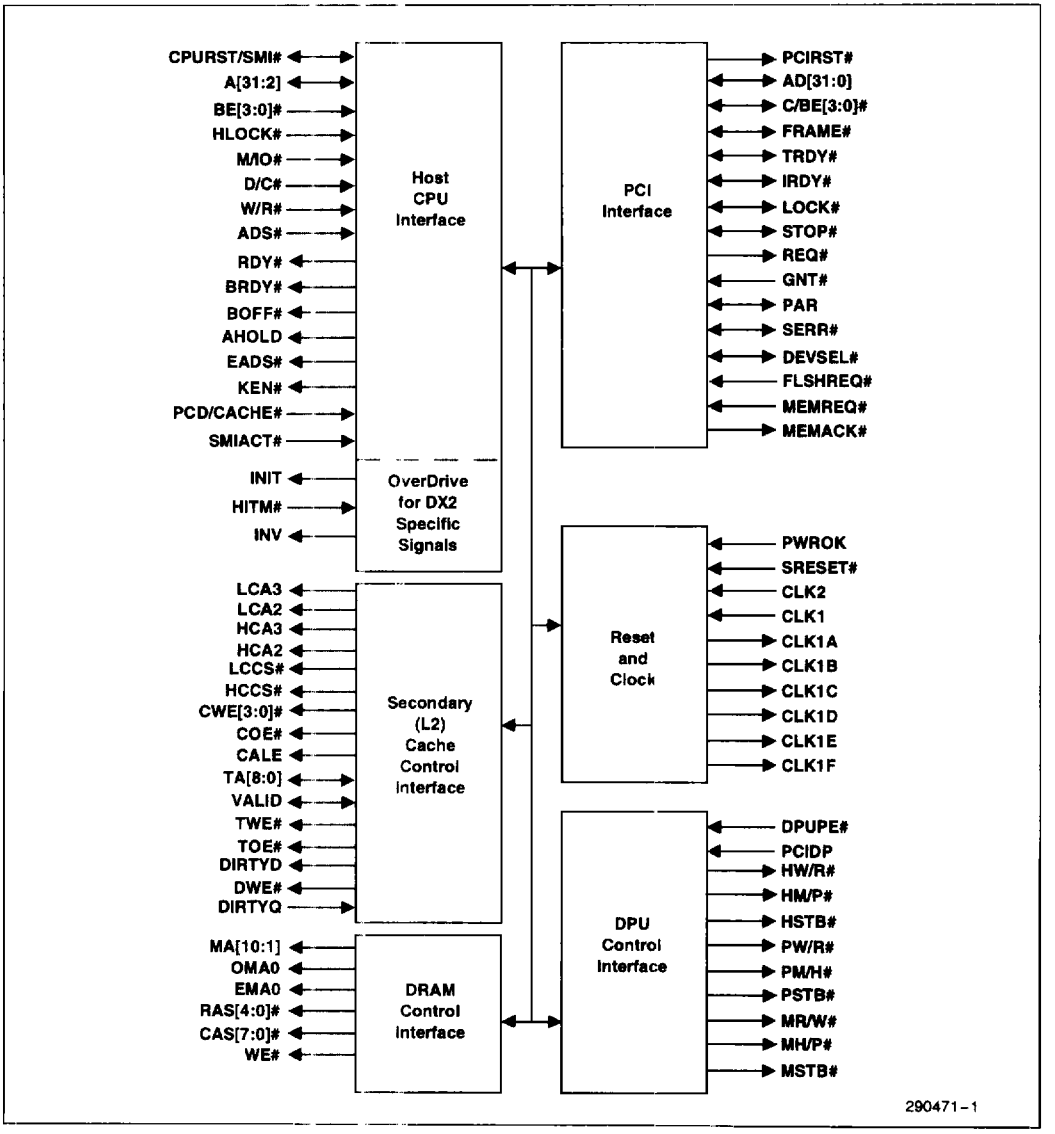

Simplified CDC Block Diagram