INTEL 82420 PCI CHIP SET

- **Highly Integrated**
  - **— 82424TX—Cache DRAM Controller (CDC) Integrates an L2 Cache Controller with Write-Through or Write-Back Cache Options, DRAM Controller, Intel486™ CPU and PCI Interface, Reset and Clock, and a DPU Control Interface**
  - **— 82423TX—Data Path Unit (DPU) Integrates the Host Data, Memory Data and PCI Data Interface, DPU Control/Parity and Four Deep Posted Write Buffers**
  - **— 82378IB—System I/O (SIO) Integrates the PCI and ISA Interface, Arbitration and Address Decode, a 32-Bit Fast DMA Controller, Data Buffers, 14 Level Programmable Interrupt Controller, Three Programmable Timer/Counters, Local I/O Support for Major Utility-Bus Functions and Non-Maskable Interrupt Logic**
- **High Performance**
  - **— Peripheral Component Interconnect (PCI) for Glueless Peripheral Interface**
  - **— Supports Compatible, Type A, B or F DMA Cycles**
  - **— Concurrent Operation between PCI Bus Masters and CPU**
  - **— Concurrent Copyback during Linefill**
  - **— L2 Cache Configurable in Write-Back or Write-Through Modes**
  - **— Supports 4-1-2-1 DRAM Accesses**
- **High Flexibility**
  - **— Supports Intel486™ SX, Intel486™ DX, Intel486™ DX2 and OverDrive™ Processors**
  - **— 64K, 128K, 256K and 512K Cache Sizes**
  - **— 2M to 128M Memory**
  - **— 60 ns and 70 ns Fast Page DRAMs**
  - **— 256K x 4, 1M x 4 and 4M x 4 DRAMs**
- **Modular Architecture**
  - **— Partitioning Logically and Electrically Isolates the PCI Bus. This Allows System Designers to Completely Reuse the PCI and I/O Subsystems across Multiple CPU Generations.**
  - **— Systems will be Modular for ISA, EISA and Other Expansion Buses**

Intel's first PCI Fast Local Bus chip set is designed to allow a glueless interface for high performance peripherals such as LAN, SCSI, Graphics and Video onto a fast local bus. Integration of these peripherals onto PCI provides the foundation to define a new class of Professional Business PCs.

The 82420 PCI Chip Set is comprised of three components: the Cache DRAM Controller (CDC), Data Path Unit (DPU) and the System I/O (SIO). The CDC and DPU provide the core system architecture while the SIO is a PCI Master/Slave agent which bridges the core architecture to the ISA standard expansion bus. The chip set will support the i486 CPU family as well as Intel's future OverDrive processor for the Intel486 DX2 with Write-Back or Write-Through caching capability.

The Cache DRAM Controller is a dual ported device with one port as the Host port and the other being the PCI port. The CDC integrates the functionality of a second level cache controller with an integrated comparator, a DRAM controller and a PCI bus controller. The CDC integrates a 4 deep buffer for posting CPU cycles to DRAM or PCI.

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The Data Path Unit is a tri-ported device with Host, DRAM and PCI interfaces. The DPU allows for concurrent activities between the Host and PCI bus. The DPU integrates a four deep posted write buffer which works in conjunction with the four deep address buffer inside the CDC. The DPU's posted write buffers allow the CPU write cycles to be executed as 0 wait state write cycles.

The System I/O is a dual ported device which acts as a bridge between the PCI and standard I/O bus. This component will be reusable across Saturn and future Intel PCI chip sets. The S10 integrates the functionality of an ISA controller, PCI controller, Fast 32-bit DMA controller and standard system I/O functions. The SIO will be replaced by a two chip solution to support the EISA expansion bus.