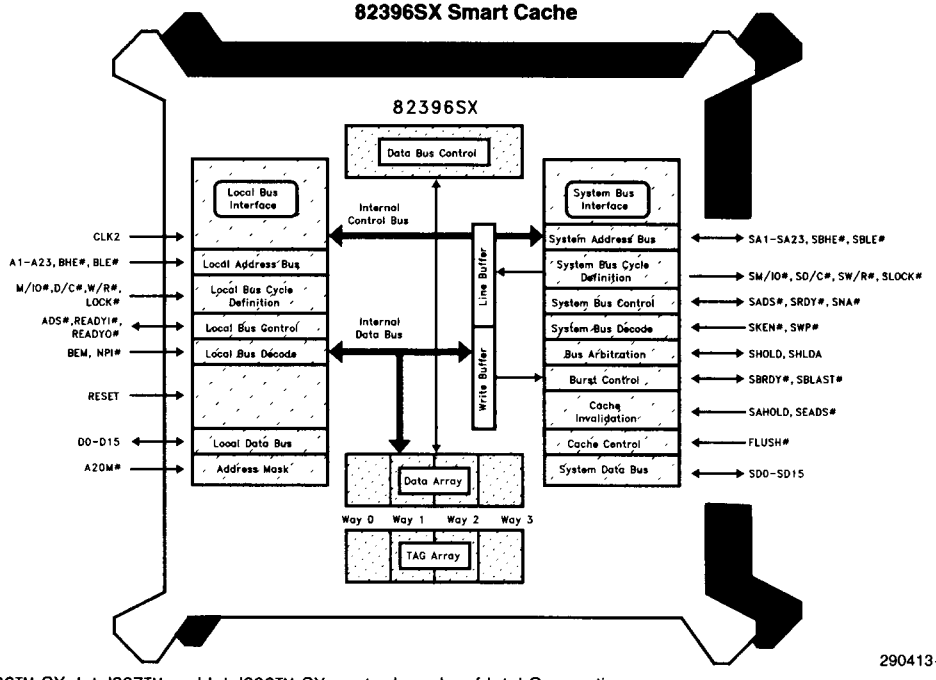
82396SX SMART CACHE

- **Optimized Intel386™ SX Microprocessor Companion**
- **4 Way SET Associative with Pseudo LRU Algorithm**
- **Write Buffer Architecture**
- **Integrated 4 Word Write Buffer**
- **Integrated Intel387™ SX Math Coprocessor Decode Logic**
- **132 Lead PQFP Package**
- **Intel486™ SX Microprocessor like Burst**
- **Integrated 16 KB Data RAM**
- **16-Byte Line Size**
- **Dual Bus Architecture — Snooping Maintains Cache Coherency**
- **20 MHz Clock**
- **Concurrent Line Buffer Cacheing**
- **1K of TAG RAM**
- **Non-Sectored Architecture**

The 82396SX Smart Cache (part number 82396SX) is a low cost, single chip, 16-bit peripheral for Intel's i386™ SX Microprocessor. By storing frequently accessed code or data from main memory the 82396SX Smart Cache enables the i386™ SX Microprocessor to run at near zero wait states. The dual bus architecture allows another bus master to access the System Bus while the i386™ SX Microprocessor operates out of the 82396SX Smart Cache on the Local Bus. The 82396SX Smart Cache has a snooping mechanism which maintains cache coherency with main memory during these cycles.

The 82396SX Smart Cache is completely software transparent, protecting the integrity of system software. The advanced architectural features of the 82596SX Smart Cache offer high performance with a cache data RAM size that can be integrated on a single chip, offering the board space and cost savings needed in an i386™ SX Microprocessor based system.

82396SX Smart Cache



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82396SX Smart Cache

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0.0 DESIGNER SUMMARY

0.1 Pin Out

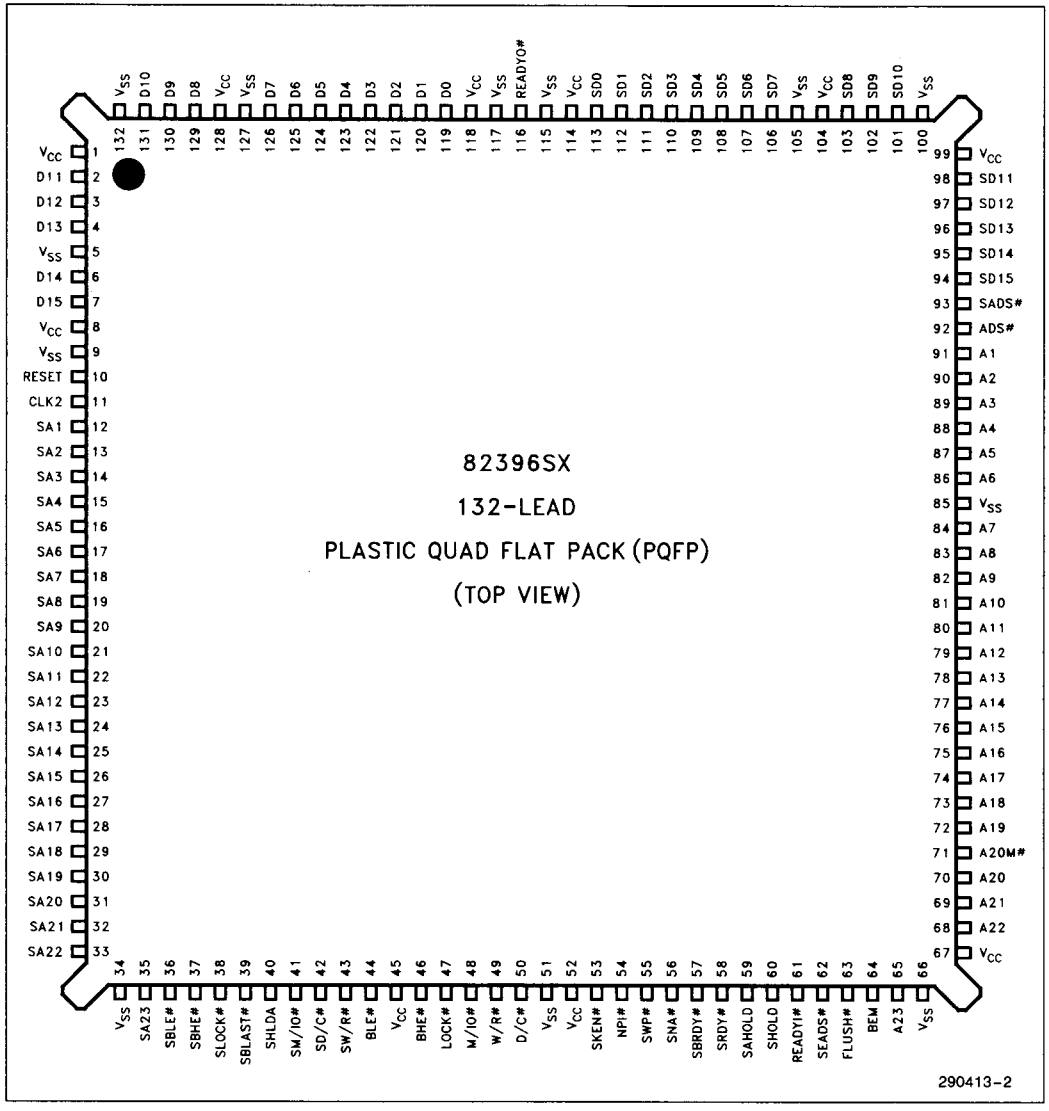

Figure 0.1 82396SX Smart Cache 132 Lead PQFP Package Pin Orientation

Table 0.1 82396SX Smart Cache 132 Pin PQFP Pin Description

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	V_{CC}	34	V_{SS}	67	V_{CC}	100	V_{SS}
2	D11	35	SA23	68	A22	101	SD10
3	D12	36	SBLE#	69	A21	102	SD9
4	D13	37	SBHE#	70	A20	103	SD8
5	V_{SS}	38	SLOCK#	71	A20M#	104	V_{CC}
6	D14	39	SBLAST#	72	A19	105	V_{SS}
7	D15	40	SHLDA	73	A18	106	SD7
8	V_{CC}	41	SM/IO#	74	A17	107	SD6
9	V_{SS}	42	SD/C#	75	A16	108	SD5
10	RESET	43	SW/R#	76	A15	109	SD4
11	CLK2	44	BLE#	77	A14	110	SD3
12	SA1	45	V_{CC}	78	A13	111	SD2
13	SA2	46	BHE#	79	A12	112	SD1
14	SA3	47	LOCK#	80	A11	113	SD0
15	SA4	48	M/IO#	81	A10	114	V_{CC}
16	SA5	49	W/R#	82	A9	115	V_{SS}
17	SA6	50	D/C#	83	A8	116	READYO#
18	SA7	51	V_{SS}	84	A7	117	V_{SS}
19	SA8	52	V_{CC}	85	V_{SS}	118	V_{CC}
20	SA9	53	SKEN#	86	A6	119	D0
21	SA10	54	NPI#	87	A5	120	D1
22	SA11	55	SWP#	88	A4	121	D2
23	SA12	56	SNA#	89	A3	122	D3
24	SA13	57	SBRDY#	90	A2	123	D4
25	SA14	58	SRDY#	91	A1	124	D5
26	SA15	59	SAHOLD	92	ADS#	125	D6
27	SA16	60	SHOLD	93	SADS#	126	D7
28	SA17	61	READYI#	94	SD15	127	V_{SS}
29	SA18	62	SEADS#	95	SD14	128	V_{CC}
30	SA19	63	FLUSH#	96	SD13	129	D8
31	SA20	64	BEM	97	SD12	130	D9
32	SA21	65	A23	98	SD11	131	D10
33	SA22	66	V_{SS}	99	V_{CC}	132	V_{SS}

0.2 Quick Pin Reference

What follows is a brief pin description. For more details refer to Chapter 3.

Symbol	Type	Function
CLK2	I	This signal provides the fundamental timing for the 82396SX Smart Cache. All external timing parameters are specified with respect to the rising edge of CLK2.
Local Address Bus		
A[23:1]	I	A[23:1] are the Local Bus address lines. These signals along with the byte enable signals, define the physical area of memory or input/output space accessed.
BHE#, BLE#	I	The byte enable signals are used to determine which bytes are accessed in partial cache write cycles. These signals are ignored for Cache Read Hit cycles. For all System Bus memory read cycles (except the last seven cycles of a Line Fill), these signals are mirrored by the SBHE#, SBLE# signals. (See also SBHE#, SBLE# and BEM.)
Local Bus Cycle Definition		
W/R# D/C# M/IO#	I I I	The write/read, data/code and memory/input-output signals are the primary bus definition signals directly connected to the i386™ SX Microprocessor. They become valid as the ADS# signal is sampled active. The bus definition signals are not driven by the i386™ SX Microprocessor during bus hold and follow the timing of the address bus.
LOCK#	I	The Local Bus LOCK# signal indicates that the current bus cycle is LOCK#ed. LOCK#ed cycles are treated as non-cacheable cycles, except that LOCK#ed write hit cycles update the cache.
Local Bus Control		
ADS#	I	The address status pin, an output of the i386™ SX Microprocessor, indicates that new and valid information is currently available on the Local Bus. The signals that are valid when ADS# is activated are: A[23:1], BHE#, BLE#, W/R#, D/C#, M/IO#, LOCK#, NPI#, BEM
READYI#	I	This is the READY input signal seen by the Local Bus master. Typically it is a logical OR between the READYO# generated by the 82396SX Smart Cache and the READY# signal generated by the i387™ SX Math Coprocessor. It is used by the 82396SX Smart Cache, along with the ADS# signal, to keep track of the i386™ SX Microprocessor bus state.
READYO#	O	This is the Local Bus READY output that is used to terminate all types of i386™ SX Microprocessor bus cycles, except for i387™ SX Math Coprocessor cycles. Assertion of READYO# indicates the completion of the cycle on the Local Bus. The cycle can be concurrently running on the System Bus allowing the dual bus nature of the 82396SX Smart Cache to be utilized. The READYO# pin may serve as READY# for the i387™ SX Math Coprocessor.
Reset		
RESET	I	The RESET signal forces the 82396SX Smart Cache to begin execution at a known state. The RESET falling edge is used by the 82396SX Smart Cache to set the phase of its internal clock identical to the i386™ SX Microprocessors internal clock. RESET falling edge must satisfy the appropriate setup and hold times (T14, T15b) for proper chip operation. RESET must remain active for at least 1ms after the power supply and CLK2 input have reached their proper DC and AC specifications.
Local Data Bus		
D[15:0]	I/O	These are the Local Bus data lines of the 82396SX Smart Cache. They must be connected to the D[15:0] pins of the i386™ SX Microprocessor.
Local Bus Decode Pins		
NPI#	I	The No Post Input signal instructs the 82396SX Smart Cache that the write cycle currently in progress must not be posted in the write buffer. NPI# is sampled at the falling edge of CLK at the end of T1 (see Figure 5.1).

0.2 Quick Pin Reference (Continued)

Symbol	Type	Function
Local Bus Decode Pins (Continued)		
BEM	I	The Byte Enable Mask signal, when asserted, causes the local bus byte enable signals to be masked so that both system bus byte enables are asserted on memory read cycles. If BEM is asserted during cacheble read cycles and that cycle requires a Line Fill (cache read miss), then both bytes will be accessed during the first cycle of the Line Fill. If BEM is not used (tied low), the system must return valid data for both bytes on the first access of a Line Fill, because SBHE# and SBLE# will be the same as BHE# and BLE# during the first access of a Line Fill and are not always active.
Address Mask		
A20M#	I	Address bit 20 Mask when active, forces the A20 input as seen by the 82396SX Smart Cache to logic '0', regardless of the actual value on the A20 input pin. A20M# emulates the address wraparound at 1 MByte which occurs on the 8086. This pin is asynchronous but must meet setup and hold times (t47 and t48) to guarantee recognition in a specific clock. It must be asserted two clock cycles before ADS# is sampled active (see figure 5.3). It must be stable throughout Local Bus memory cycles.
System Address Bus		
SA[3:1] SA[23:4]	O I/O	These are the System Bus address lines of the 82396SX Smart Cache. When driven by the 82396SX Smart Cache, these signals, along with the System Bus byte enables define the physical area of memory or input/output space being accessed. During bus HOLD or address HOLD, the 20 MSB serve as inputs for the cache invalidation cycle.
SBHE#, SBLE#	O	These are the Byte Enable signals for the System Bus. When BEM is inactive, the 82396SX Smart Cache drives these pins identically to BHE# and BLE# in all System Bus cycles except Line Fills. In Line Fills these signals are driven identically to BHE# and BLE# for the first read cycle of the Line Fill. They are both driven active in the remaining cycles of the Line Fill. When BEM is active, the 82396SX Smart Cache will assert SBHE# and SBLE# for all non-locked memory read cycles.
System Bus Cycle Definition		
SW/R# SD/C# SM/IO#	O O O	The System Bus write/read, data/code and memory/input- output signals are the System Bus cycle definition pins. When the 82396SX Smart Cache is the System Bus master, it drives these signals identically to the i386™ SX Microprocessor cycle definition encoding.
SLOCK#	O	The System Bus LOCK signal indicates that the current cycle is LOCK#ed. The 82396SX Smart Cache has exclusive access to the System Bus across bus cycle boundries until this signal is negated. The 82396SX Smart Cache does not acknowledge a bus HOLD request while this signal is asserted. The 82396SX Smart Cache asserts SLOCK# when the System Bus is available and a LOCK#ed cycle was started on the Local Bus that requires System Bus service. SLOCK# is negated only after completion of all LOCK#ed System Bus cycles and negation of the LOCK# signal.
System Bus Control		
SADS#	O	The System Bus Address Status signal is used to indicate that new and valid information is currently being driven onto the System Bus. The signals that are valid when SADS# is driven low are: SA[23:1], SBHE#, SBLE#, SW/R#, SD/C#, SM/IO# and SLOCK#

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0.2 Quick Pin Reference (Continued)

Symbol	Type	Function
System Bus Control (Continued)		
SRDY#	I	The System Bus ReaDY# signal indicates that the current System Bus cycle is complete. When SRDY# is sampled asserted it indicates one of two things. In response to a read request it indicates that the external system has presented valid data on the system data bus. In response to a write request it indicates that the external system has accepted the 82396SX Smart Cache's data. This signal is ignored when the System Bus is in STi, STH, ST1 or ST1P states. At the first read cycle of a Line Fill SRDY#, SBRDY# and SNA# determine if the Line Fill will proceed as a burst/non-burst, pipelined/non-pipelined Line Fill. Once a burst Line Fill has started, if SRDY# is returned in the 2nd through the 7th word, the burst Line Fill will be interrupted and the cache will not be updated. The 1st word will already have been transferred to the CPU. In the 8th word of a Line Fill both SRDY# and SBRDY# have the same effect. They indicate the end of the Line Fill.
SNA#	I	The System Bus Next Address signal, when active, indicates that a pipelined address cycle will be executed. It is sampled by the 82396SX Smart Cache at the rising edge of CLK in ST2 and ST1P cycles. SNA# is ignored during the eighth word of the Line Fill. If this signal is sampled active for the first word of the Line Fill then burst Line Fills are disabled.
Bus Arbitration		
SHOLD	I	The System Bus HOLD request indicates that another master must have complete control of the entire System Bus. When SHOLD is sampled asserted the 82396SX Smart Cache completes the current System Bus cycle or sequence of LOCK#ed cycles, before driving SHLDA active. In the same clock that SHLDA went active all the System Bus outputs and I/O pins are floated (with the exception of SHLDA). The 82396SX Smart Cache stays in this state until SHOLD is negated. SHOLD is recognized during RESET.
SHLDA	O	The System Bus HOLD Acknowledge signal is driven active by the 82396SX Smart Cache in response to a hold request. It indicates that the 82396SX Smart Cache has given the bus to another System Bus master. It is driven active in the same clock that the 82396SX Smart Cache floats it's System Bus. When leaving a bus HOLD, SHLDA is driven inactive and the 82396SX Smart Cache resumes driving the bus in the same clock. The 82396SX Smart Cache is able to support CPU Local Bus activities during System Bus HOLD.
Burst Control		
SBRDY#	I	The System Bus Burst ReaDY signal performs the same function during a burst cycle that SRDY# does in a non-burst cycle. SBRDY# asserted indicates that the external system has presented valid data on the data pins in response to a burst Line Fill cycle. This signal is ignored when the System Bus is at STi, STH, ST1 or ST1P states. Note that in the eighth bus cycle of a Line Fill, SBRDY# and SRDY# have the same effect on the 82396SX Smart Cache. They indicate the end of the Line Fill. For all cycles other than burst Line Fills, SBRDY# and SRDY# have the same effect on the 82396SX Smart Cache.

0.2 Quick Pin Reference (Continued)

Symbol	Type	Function
Burst Control (Continued)		
SBLAST#	O	The System Bus Burst LAST cycle indicator signal indicates that the next time SBRDY# is returned the burst cycle is complete. It indicates to the external system that the next SBRDY# returned is treated as a normal SRDY# by the 82396SX Smart Cache. Another set of addresses will be driven with SADS# or the System Bus will go idle. SBLAST# is normally active. In a cache read miss cycle, which may proceed as a Line Fill, SBLAST# starts active. After determining whether or not the cycle is cacheable via SKEN#, SBLAST# is driven inactive. If it is a cacheable cycle, and SBRDY# terminates the first word of the Line Fill, a burst Line Fill, SBLAST# will be driven active when the data is valid for the eighth word of the Line Fill. If SRDY# terminates the first word of the Line Fill, a non-burst Line Fill, SBLAST# is driven active in the cycle where SRDY# was sampled active.
Cache Invalidation		
SAHOLD	I	The System Bus Address HOLD request allows another bus master access to the address bus of the 82396SX Smart Cache. This is to indicate the address of an external cycle for performing an internal cache directory lookup and invalidation cycle. In response to this signal the 82396SX Smart Cache stops driving the System Bus address pins in the next cycle. No HOLD Acknowledge is required. Other System Bus signals can remain active during address hold. The 82396SX Smart Cache does not initiate another bus cycle during address hold. This pin is recognized during RESET.
SEADS#	I	The System Bus External Address Strobe signal indicates that a valid external address has been driven onto the 82396SX Smart Cache System Bus address pins. This address will be used to perform an internal cache invalidation cycle. The maximum invalidation cycle rate is one every two clock cycles.
Cache Control		
FLUSH#	I	The FLUSH# pin, when sampled active for four clock cycles or more, causes the 82396SX Smart Cache to invalidate its entire TAG array. In addition, it is used to configure the 82396SX Smart Cache to enter various test modes. For details refer to chapter 7. This signal is asynchronous but must meet setup and hold times to guarantee recognition in any specific clock.
System Data Bus		
SD[15:0]	I/O	The System Bus Data lines of the 82396SX Smart Cache must be driven with appropriate setup and hold times for proper operation. These signals are driven by the 82396SX Smart Cache only during write cycles.
System Bus Decode Pins		
SKEN#	I	The System Cacheability Enable signal is used to determine if the current cycle running on the System Bus is cacheable or not. When the 82396SX Smart Cache generates a read cycle, SKEN# is sampled one clock before the first SBRDY# or SRDY# or one cycle before the first SNA# is sampled active (see chapter 6). If SKEN# is sampled active the cycle will be transformed into a Line Fill. Otherwise, the cache and cache directory will be unaffected. Note that SKEN# is ignored after the first cycle in a Line Fill. SKEN# is ignored for all System Bus cycles except for cache read miss cycles.
SWP#	I	The System Write Protect indicator signal is used to determine whether the current System Bus Line Fill cycle is write protected or not. In non-pipelined cycles, SWP# is sampled with the first SRDY# or SBRDY# of the Line Fill. In pipelined cycles, SWP# is sampled one clock phase after the first SNA# is sampled active (see figures 6.9-10). The Write Protect bit is sampled together with the TAG of each line in the 82396SX Smart Cache Cache Directory. In every cacheable write cycle the Write Protect bit is read. If active, the cycle will be a write protected cycle which is treated like a cacheable write miss cycle. It is buffered and it does not update the cache even if the addressed location is present in the cache.

1.0 82396SX SMART CACHE FUNCTIONAL OVERVIEW

1.1 Introduction

The primary function of a cache is to provide local storage for frequently accessed memory locations. The cache intercepts memory references and handles them directly without transferring the request to the System Bus. This results in lower traffic on the System Bus and decreases latency on the Local Bus. This leads to improved performance for a processor on the Local Bus. It also increases potential system performance by reducing each processor's demand for System Bus bandwidth, thus allowing more processors or system masters in the system. By providing fast access to frequently used code and data the cache is able to reduce the average memory access time of the i386™ SX Microprocessor based system.

The 82396SX Smart Cache is a single chip cache subsystem specifically designed for use with the i386™ SX Microprocessor. The 82396SX Smart Cache integrates 16KB cache, the Cache Directory and the cache control logic onto one chip. The cache is unified for code and data and is transparent to application software. The 82396SX Smart Cache provides a cache consistency mechanism which guarantees that the cache has the most recently updated version of the main memory. Consistency support has no performance impact on the i386™ SX Microprocessor. Section 1.2 covers all the 82396SX Smart Cache features.

The 82396SX Smart Cache architecture is similar to the i486™ SX Microprocessor's on-chip cache. The cache is four Way SET associative with Pseudo LRU (Least Recently Used) replacement algorithm. The

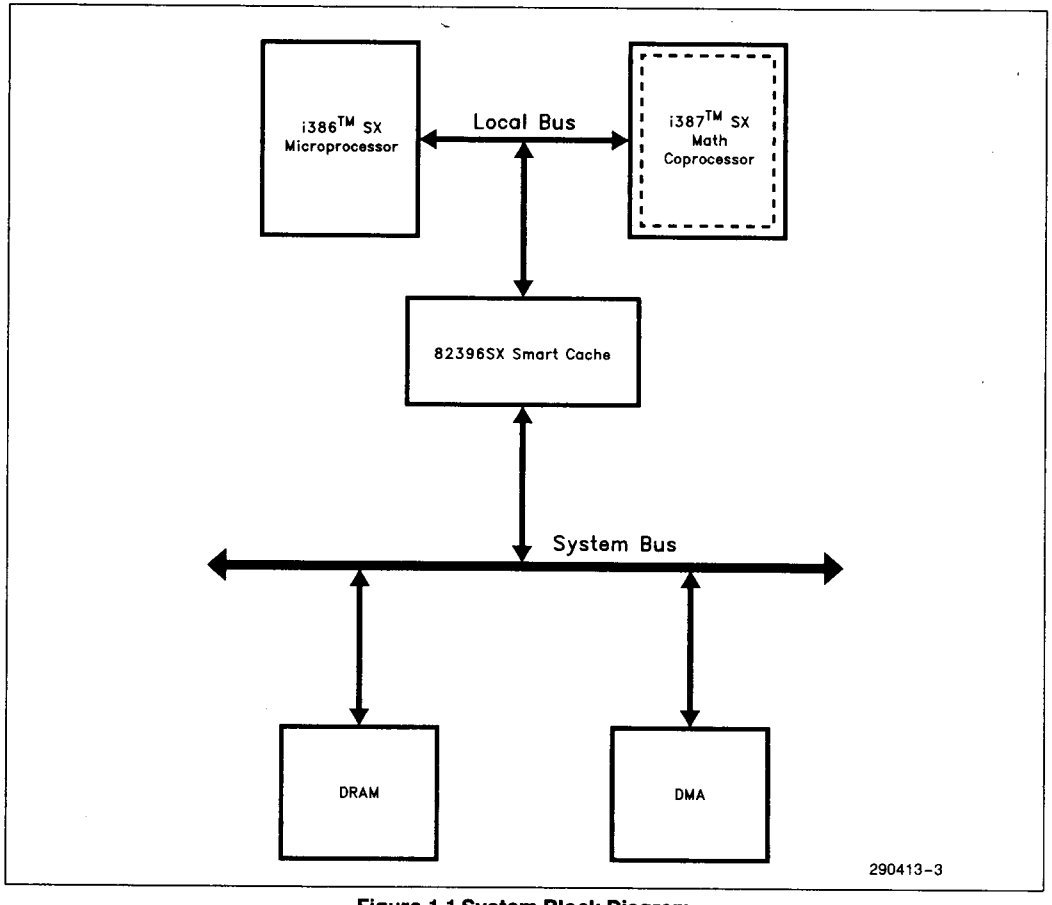

Figure 1.1 System Block Diagram

line size is 16B and a full line is retrieved from the memory for every cache miss. A TAG is associated with every 16B line. The 82396SX Smart Cache architecture allows for cache read hit cycles to run on the Local Bus even when the System Bus is not available. 82396SX Smart Cache incorporates a new write buffer cache architecture, which allows the i386™ SX Microprocessor to continue operation without waiting for write cycles to actually update the main memory.

A detailed description of the cache operation and parameters is included in Chapter 2.

The 82396SX Smart Cache has an interface to two electrically isolated busses. The interface to the i386™ SX Microprocessor bus is referred to as the Local Bus (LB) interface. The interface to the main memory and other system devices is referred to as the 82396SX Smart Cache System Bus (SB) interface. The SB interface emulates the i386™ SX Microprocessor. The SB interface, as does the i386™ SX Microprocessor, operates in pipeline mode.

In addition, it is enhanced by an optional burst mode for Line Fills. The burst mode provides faster line fills by allowing consecutive read cycles to be executed at a rate of up to one word per clock cycle. Several bus masters (or several 82396SX Smart Caches) can share the same System Bus and the arbitration is done via the SHOLD/SHLDA mechanism (similar to the i486™ SX Microprocessor).

Cache consistency is maintained by the SAHOLD/SEADS# snooping mechanism, similar to the i486™ SX Microprocessor. The 82396SX Smart Cache is able to run a zero wait state i386™ SX Microprocessor non-pipelined read cycle if the data exists in the cache. Memory write cycles can run with zero wait states if the write buffer is not full.

The 82396SX Smart Cache organization provides a higher hit rate than other standard configurations. The 82396SX Smart Cache, featuring the new high performance write buffer cache architecture, provides full concurrency between the electrically isolated Local Bus and System Bus. This allows the 82396SX Smart Cache to service read hit cycles on the Local Bus while running line fills or buffered write cycles on the System Bus.

1.2 Features

1.2.1 82385SX-LIKE FEATURES

— The 82396SX Smart Cache maps the entire physical address range of the i386™ SX Microprocessor (16MB) into an 16KB cache.

— Unified code and data cache.

— Cache attributes are handled by hardware. Thus the 82396SX Smart Cache is transparent to application software. This preserves the integrity of system software and protects the users software investment.

— Word and Byte writes, Word reads.

— Zero wait states in read hits and in buffered write cycles. All i386™ SX Microprocessor cycles are non-pipelined (Note: The i386™ SX Microprocessor must never be pipelined when used with the 82396SX Smart Cache - NA# must be tied to Vcc).

— A hardware cache FLUSH# option. The 82396SX Smart Cache will invalidate all the Tag Valid bits in the Cache Directory and clear the System Bus line buffer when FLUSH# is activated for a minimum of four CLK's.

— The 82396SX Smart Cache supports non-cacheable accesses.

— The 82396SX Smart Cache internally decodes the i387™ SX Math Coprocessor accesses as Local Bus cycles.

— The System Bus interface emulates a i386™ SX Microprocessor interface.

— The 82396SX Smart Cache supports pipelined and non-pipelined system interface.

— Provides cache consistency (snooping): The 82396SX Smart Cache monitors the System Bus address via SEADS# and invalidates the cache address if the System Bus address matches a cached location.

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1.2.2 NEW FEATURES

— 16KB on chip cache arranged in four banks, one bank for each way. In Read hit cycles, one word is read. In a write hit cycle, any byte within the word can be written. In a cache fill cycle, the whole line (16B) is written. This large line size increases the hit rate over smaller line size caches.

— Cache architecture similar to the i486™ SX Microprocessor cache: 4 Way set associative with Pseudo LRU replacement algorithm. Line size is 16B and a full line is retrieved from memory for every cache miss. A Tag Valid Bit and a Write Protect Bit are associated with every Line.

— New write buffer architecture with four word deep write buffer provides zero wait state memory write cycles. I/O, Halt/Shutdown and LOCK#ed writes are not buffered.

— Concurrent Line Buffer Cacheing: The 82396SX Smart Cache has a line buffer that is used as additional memory. Before data gets written to

the cache memory at the completion of a Line Fill it is stored in this buffer. Cache hit cycles to the line buffer can occur before the line is written to the cache.

— In i387™ SX Math Coprocessor accesses, the 82396SX Smart Cache drives the READYO# in one wait state if the READYI# was not driven in the previous clock.

  Note that the timing of the 82396SX Smart Cache's READYO# generation for i387™ SX Math Coprocessor cycles is incompatible with 80287 timing.

— An enhanced System Bus interface:

  a) Burst option is supported in line-fills similar to the i486™ SX Microprocessor. SBRDY# (System Burst READY) is provided in addition to SRDY#. A burst is always a 16 byte line fill (cache update) which is equivalent to eight word cycles.

  b) System cacheability attribute is provided (SKEN#). SKEN# is used to determine whether the current cycle is cacheable. It is used to qualify Line Fill requests.

  c) SHOLD/SHLDA system bus arbitration mechanism is supported. A Multi i386™ SX / 82396SX Smart Cache cluster can share the same System Bus via this mechanism.

  f) Cache invalidation cycles supported via SEADS#. This is used to provide cache coherency.

— Full Local Bus/System Bus concurrency is attained by:

  a) Servicing cache read hit cycles on the Local Bus while completing a Line Fill on the System Bus. The data requested by the i386™ SX Microprocessor is provided over the local bus as the first word of the Line Fill.

  b) Servicing cache read hit cycles on the Local Bus while executing buffered write cycles on the system bus.

  c) Servicing cache read hit cycles on the Local Bus while another bus master is running (DMA, other i386™ SX Microprocessor, 82396SX Smart Cache, i486™ SX Microprocessor, etc . . .) on the System Bus.

  d) Buffering write cycles on the Local Bus while the system bus is executing other cycles.

— Write protected areas are supported by the SWP# input. This enables caching of ROM space or shadowed ROM space.

— No Post Input (NPI#) provided for disabling of write buffers per cycle. This option supports memory mapped I/O designs.

— Byte Enable Mask (BEM) is provided to mask the processor byte enables during a memory read cycle.

— A20M# input provided for emulation of 8086 address wrap-around.

— SRAM test mode, in which the TAGRAM and the cache RAM are treated as standard SRAM, is provided. A Tristate Output test mode is also provided for system debugging. In this mode the 82396SX Smart Cache is isolated from the other devices in the board by floating all its outputs.

— Single chip, 132 lead PQFP package, 1 micron CHMOS-IV technology.

2.0 82396SX SMART CACHE SYSTEM DESCRIPTION

2.1 82396SX Smart Cache Organization

The on chip cache memory is a unified code and data cache. The cache organization is 4 Way SET Associative and each Line is 16 bytes wide (see Figure 2.1). The 16K bytes of cache memory are logically organized as 4 4KB banks (4: 1 bank for each Way). Each bank contains 256 16B lines (256: 1 line for each SET).

The Cache Directory is used to determine whether the data in the cache memory is valid for the address being accessed. The Cache Directory contains 256 TAG's (each TAG is 14-bits wide) for each Way, for a total of 1K TAG's (See Figure 2.2). With each 12 bit TAG Address there is a TAG Valid bit and a Write Protect bit. The Cache Directory also contains the LRU bits. The LRU bits are used to determine which Way to replace whenever the cache needs to be updated with a new line and all four ways contain valid data.

Table 2.1 lists the 82396SX Smart Cache organization.

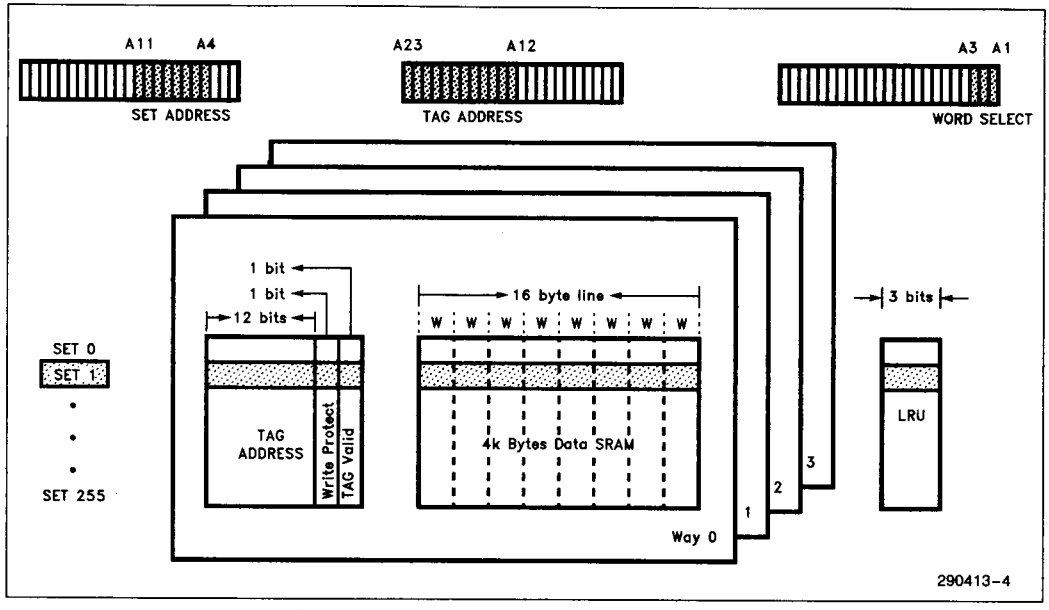

Figure 2.1. 82396SX Smart Cache Organization

Table 2.1 82396SX Smart Cache Organization

Cache Element	82396SX Size/Qty	Comments
TAG	1K	Total number of TAGs
SET	256	Cache Directory Offset
LRU	256x3	3 bits per SET address
Way	4	4 TAG's per SET address
Line Size	16B	8 Words
Sector Size	16B	8 words, one line per sector
Cache Size	16KB	
Cache Directory	—	TAG address, TAG Valid Bit, and Write Protect Bit for each Way for each SET address (256 SET's x 4 Ways), and LRU bits.
TAG Valid Bit	1K	1 for each TAG in the cache directory, indicates valid data is in the cache memory.
Write Protect Bit	1K	1 for each TAG in the cache directory, indicates that the address is write protected.

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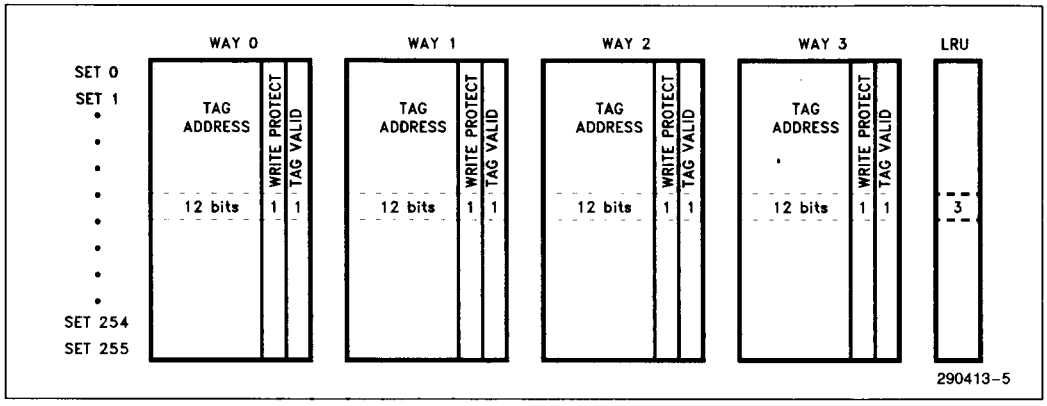

Figure 2.2. 82396SX Smart Cache Directory Organization

2.1.1 82396SX SMART CACHE STRUCTURE AND TERMINOLOGY

A detailed description of the 82396SX Smart Cache parameters are defined here.

A **Line** is the basic unit of data transferred between the cache and main memory. In the 82396SX Smart Cache each Line is 16B. A Line is also known as a transfer block. The decision of a cache "hit or miss" is determined on a per Line basis. A cache hit results when the TAG address of the current address being accessed matches the TAG address in the Cache Directory (see Figure 2.3) and the TAG Valid bit is set. The 82396SX Smart Cache has 1K Lines.

A **TAG** is a storage element of the Cache Directory with which the hit/miss decision is made. The TAG consists of the TAG address (A[23:12]), the TAG Valid bit and the Write Protect bit. Since many addresses map to a single line, the TAG is used to determine whether the data associated with the current address is present in the cache memory (a cache hit). This is done through a comparison of the TAG address bits of the current address with the four TAG address fields associated with the current address's SET. The four TAG Valid bits are also checked. Each line in the cache memory has a TAG associated with it.

A **TAG Valid Bit** is associated with each TAG address in the Cache Directory. It determines if the data held in the cache memory for the particular TAG address is valid. It is used to determine whether the data in the cache is a match to data in main memory.

A **Write Protect Bit** is also associated with each TAG address in the Cache Directory. This field determines if the cache memory can be written to. It is set by the SWP# pin during Line Fill cycles (see Chapter 6).

A **SET** address is a decoded portion of the Local Bus address that maps to 1 TAG address per Way in the Cache Directory. All the TAG's associated with a particular SET are simultaneously compared with the TAG field of the bus address to make the hit/miss decision. The 82396SX Smart Cache provides 256 SET addresses, each SET maps to four lines in the cache memory.

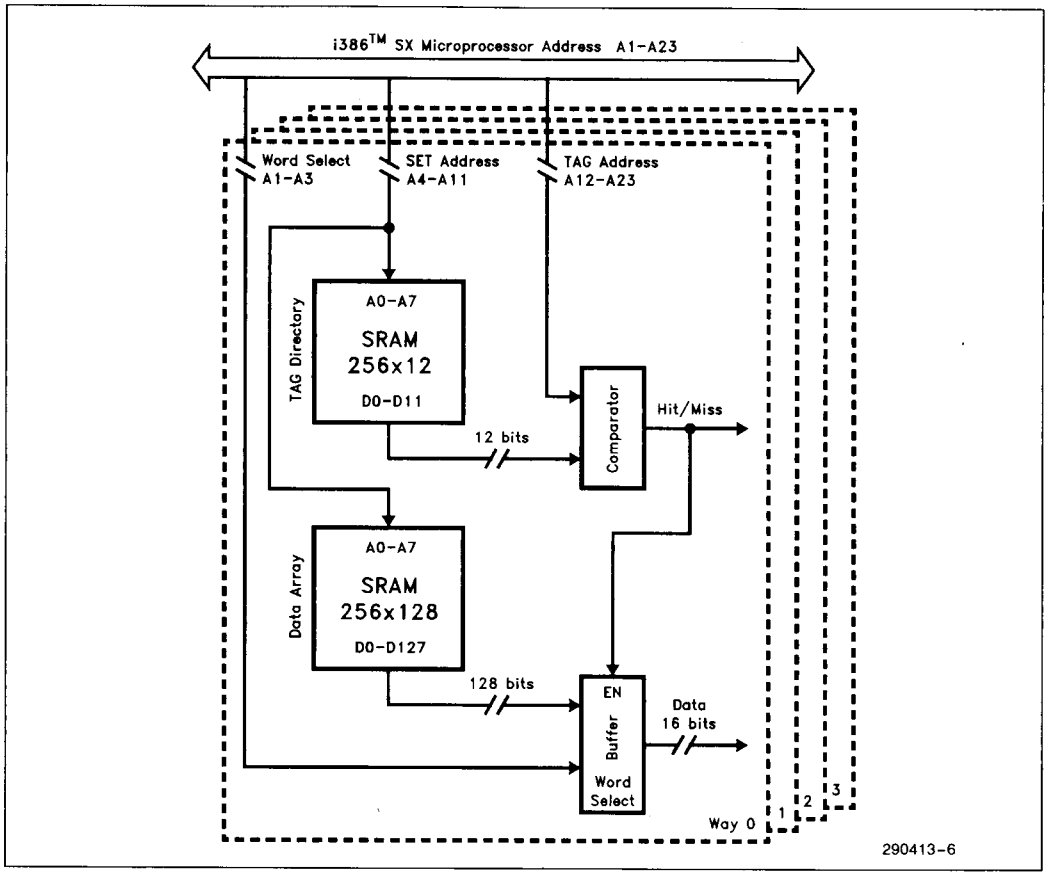

Figure 2.3. 82396SX Smart Cache Hit Logic

The term **Way** as in 4 Way SET Associative describes the degree of associativity of the cache system. Each Way provides TAG Address, TAG Valid bit, and Write Protect bit storage, 1 entry for each SET address. A simultaneous comparison of one TAG address from each Way with the bus address is done in order to make the hit/miss decision. The 82396SX Smart Cache is 4 Way SET Associative.

Other key 82396SX Smart Cache features include:

Cache Size - The 82396SX Smart Cache contains 16KB of cache memory. The cache is organized as four banks of 4KB. Each of the four banks corresponds to a particular Way.

Update Policy - The update policy deals with how main memory is updated when a cacheable write cycle is issued on the Local Bus. The 82396SX Smart Cache supports the write buffer policy, similar to the write through policy, which means that main memory is always updated in every write cycle. However, the cache is updated only when the write cycle hits the cache. Also, the 82396SX Smart Cache is able to cache write protected areas, e.g. ROMs, by preventing the cache update if the write cycle hits a write protected line. A write cycle to main memory is buffered as explained in Chapter 6.

Replacement - When a new line is needed to update the cache, the Tag Valid bits are checked to see if any of the four ways are available. If they are all valid it is necessary to replace an old line that is already in the cache. In the 82396SX Smart Cache, the Pseudo LRU (least recently used) algorithm is adopted. The Pseudo LRU algorithm targets the least recently used line associated with the SET for replacement. (See Section 2.2 for Pseudo LRU description.)

Consistency - The 82396SX Smart Cache contains hooks for a consistency mechanism. This is to guarantee that in systems with multiple caches (and/or with multiple bus masters) all processor requests result in returning correct and consistent data. Whenever a system bus master performs memory accesses to data which also exists in the cache, the System Bus master can invalidate that entry in the 82396SX Smart Cache. This invalidation is done by using SEADS# (description in Chapter 6).

The invalidation is performed by marking the TAG as invalid (the TAG Valid bit is cleared). Thus, the next time a Local Bus request is made to that location, the 82396SX Smart Cache accesses the main memory to get the most recent copy of the data.

2.2 Pseudo LRU Algorithm

When a line needs to be placed in the internal cache the 82396SX Smart Cache first checks to see if there is a non-valid line in the SET that can be replaced. The validity of a line is determined by the TAG Valid bit which is associated with this line. The order that is used for this check is Way 0, Way 1, Way 2, and Way 3. If all four lines associated with the SET are valid, a pseudo Least Recently Used algorithm is used to determine which line will be replaced. If a non-valid line is found, that line is marked for replacement. All the TAG Valid bits are cleared when the 82396SX Smart Cache is RESET or when the cache is FLUSHed. Three bits, B0, B1, and B2, are defined for each of the 256 SETs. These bits are called the LRU bits and are stored in the cache directory. The LRU bits are updated for every access to the cache.

If the most recent access to the cache was to Way 0 or Way 1 then B0 is set to 1. B0 is set to 0 if the most recent access was to Way 2 or Way 3. If the most recent access to Way 0 or Way 1 was to Way 0, B1 is set to 1. Else B1 is set to 0. If the most recent access to Way 2 or Way 3 was to Way 2, B2 is set to 1. Else B2 is set to 0.

The Pseudo LRU algorithm works in the following manner. When a line must be replaced, the cache will first select which of Way 0 and Way 1 or Way 2 and Way 3 was least recently used. Then the cache will select which of the two lines was least recently used and mark it for replacement. The decision tree is shown in Figure 2.4. When the 82396SX Smart Cache is RESET or the cache is FLUSHed all the LRU bits are cleared along with the TAG Valid bits.

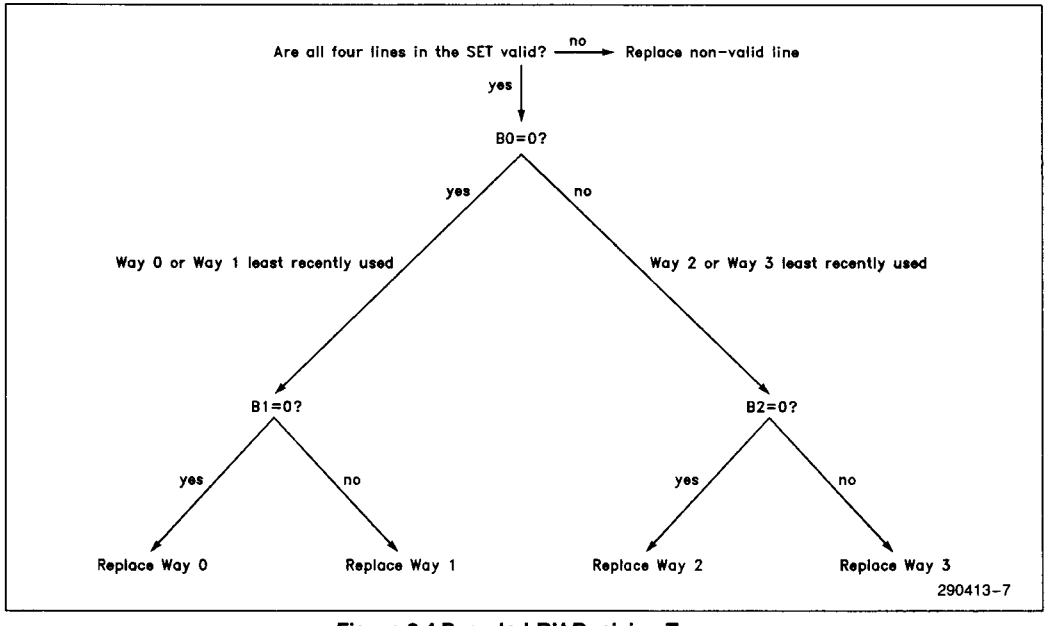

Figure 2.4 Pseudo LRU Decision Tree

2.3 Four Way Set Associative Cache Organization

The 82396SX Smart Cache is a four Way SET Associative cache. Figure 2.5 shows the 82396SX Smart Cache's cache organization. For each of the 256 SET's there are four TAG's, one for each Way. The address currently being accessed is decoded into the SET and TAG addresses. If the access was to address 001014h (SET = 01, TAG = 001h), the four TAG's in the Cache Directory associated with SET 01 are simultaneously compared with the TAG of the address being accessed. The TAG Valid bits are also checked. If the TAG's match and the TAG Valid bit is set, the access is a hit to the Way where the hit was detected, in this example the hit occurred in Way 1. The data would be retrieved from Way 1 of the cache memory. If the next access was to address 54801Eh (SET = 01, TAG = 548h), the comparison would be done and a TAG match would be found in Way 2. However in this case the TAG Valid bit is cleared so the access is a miss and the data will be retrieved from main memory. The cache memory will also be updated. It is helpful to notice that the main memory is broken into pages by the TAG size. In this case with a 12 bit TAG address there are 2^{12} pages. The smaller the TAG size the fewer pages main memory is broken into. The SET breaks down these memory pages. The larger the SET size the more lines per page.

The following is a description of the interaction between the i386™ SX Microprocessor, the 82396SX Smart Cache's cache and Cache Directory.

2.3.1 CACHE READ HITS

When the i386™ SX Microprocessor initiates a memory read cycle, the 82396SX Smart Cache uses the 8 bit SET address to select 1 of the 256 SET's in the Cache Directory. The four TAG's of this SET are simultaneously compared with address bits A[23:12]. The four TAG Valid bits are checked. If any comparison produces a hit the corresponding bank of internal SRAM supplies the 16 bits of data to the i386™ SX Microprocessor data bus based on the word select bits A3, A2 and A1. The LRU bits are then updated according to the Pseudo LRU algorithm.

2.3.2 CACHE READ MISSES

Like the cache read hit the 82396SX Smart Cache uses the 8 bit SET address to select the 4 TAG's for comparison. If none of these match or if the TAG Valid bit associated with a matching TAG address is cleared the cycle is a miss and the 82396SX Smart Cache retrieves the requested data from main memory. A Line Fill is simultaneously started to read the line of data from system memory and write the line of data into the cache in the Way designated by the LRU bits.

2.3.3 OTHER OPERATIONS THAT AFFECT THE CACHE AND CACHE DIRECTORY

Other operations that affect the cache and Cache Directory include write hits, snoop hits, cache FLUSHes and 82396SX Smart Cache RESETs. In write hits, the cache is updated along with main memory. The bank that detected the hit is the one that data is written to. The LRU bits are then adjusted according to the Pseudo LRU algorithm. When a cache invalidation cycle occurs (Snoop HIT) the tag valid bit is cleared. RESETs and cache FLUSHes clear all the TAG Valid bits.

2.4 Concurrent Line Buffer Cacheing

This feature of the 82396SX Smart Cache can be broken into two components, Concurrent Line Buffer and Line Buffer Cacheing.

A Concurrent Line Buffer has the property of returning the word requested by the i386™ SX Microprocessor after receiving the first word of the Line Fill. The Local Bus is then free to execute other cycles while the Line Fill is being completed on the System Bus. Line Buffer Cacheing indicates that the 82396SX Smart Cache serves i386™ SX Microprocessor cycles before it updates its Cache Directory. If the i386™ SX Microprocessor cycle is to a line which resides in the cache memory, the 82396SX Smart Cache will serve that cycle as a regular cache hit cycle. The cache memory and cache directory are not updated until after the Line Fill is complete (see sections 2.8 and 2.9). The 82396SX Smart Cache keeps the address and data of the retrieved line in an internal buffer, the System Bus line buffer.

Any i386™ SX Microprocessor read cycle to the same line will be serviced from the line buffer. Until the cache memory and cache directory are updated, any i386™ SX Microprocessor read cycle to a word, which has already been retrieved, will be serviced from the System Bus line buffer. On the other hand, any i386™ SX Microprocessor write cycle to the same line will be done to the cache memory after updating the line in the cache. In this case, the write cycle is buffered and the READYO# is activated after updating the line in the cache. However, if the line is Write Protected, the write cycle will be handled as if it is a miss cycle.

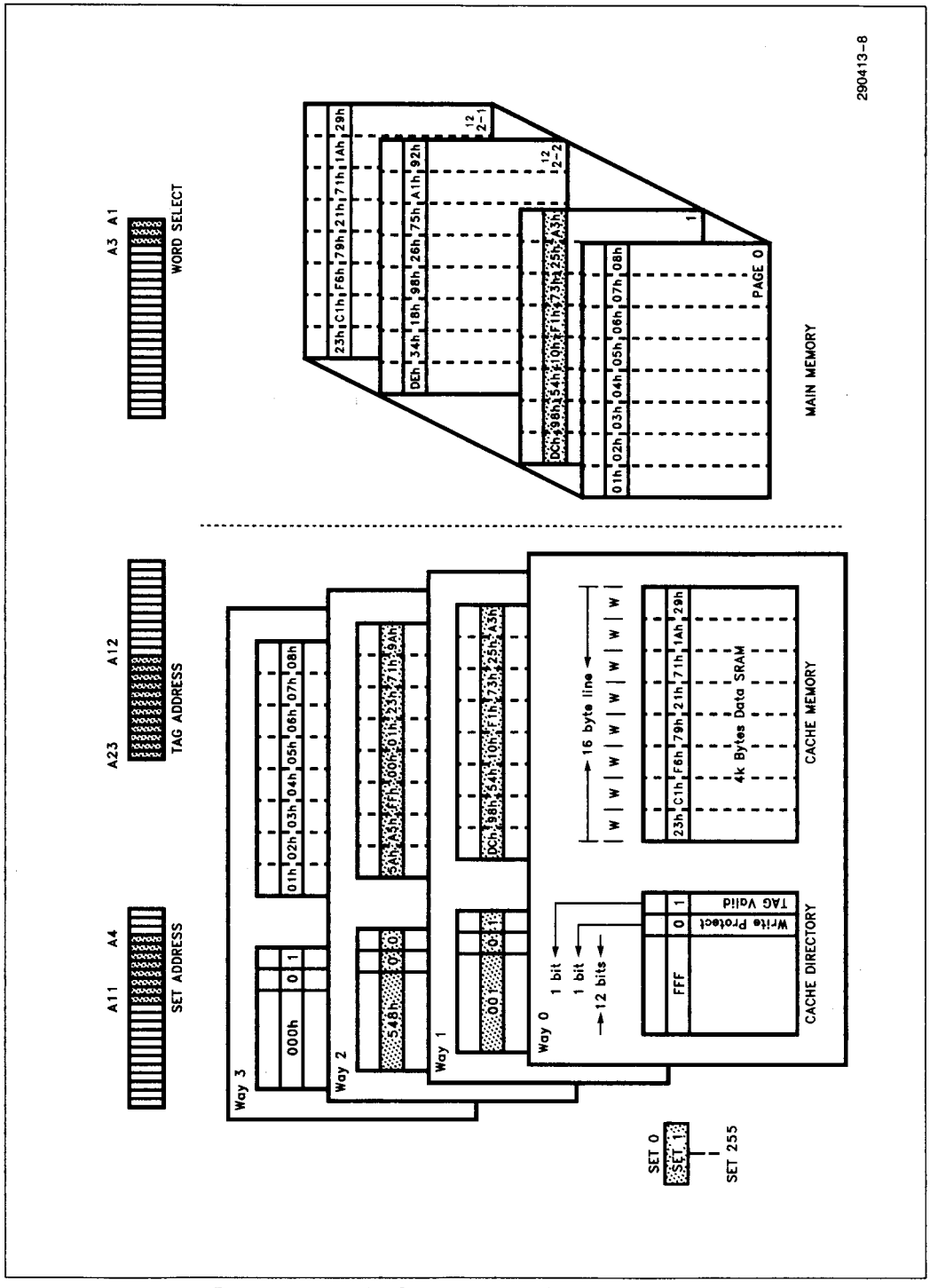

Figure 2.5 Four Way Set Associative Cache Organization

A snooping cycle to a line which has not been updated in the cache will invalidate the SB Line Buffer and will prevent the cache update. Also, cache FLUSH will invalidate the buffer. More details about invalidation cycles can be found in chapter 6.

2.5 Cache Control

The cache can be controlled via the SWP# pin. By asserting this pin during the first word in a Line Fill, the 82396SX Smart Cache sets the write protect bit in the Cache Directory making the entry protected from writes.

2.6 Cache Invalidation

Cache invalidation cycles are activated using the SEADS# pin. SAHOLD or SHLDA asserted conditions the most significant 20 bits of the 82396SX Smart Cache's system address bus (SA[23:4]) to accept an input. The 82396SX Smart Cache floats its system address bus in the clock immediately after SAHOLD was asserted, or in the clock SHLDA is activated. No address hold acknowledge is required for SAHOLD. SEADS# asserted and the rising edge of CLK2 indicate that the address on the System Bus is valid. SEADS# is not conditioned by SAHOLD or SHLDA being asserted. The 82396SX Smart Cache will read the address and perform an internal cache invalidation cycle to the address indicated. The internal cache invalidation cycle is serviced 1 cycle after SEADS# was sampled active (or 2 cycles after SEADS# was sampled active if there is contention between the Cache Directory Snoop (CDS) cycle and a Cache Directory Lookup (CDL) cycle, see 2.8 and Figure 2.6). To actually invalidate the address the 82396SX Smart Cache clears the tag valid bit.

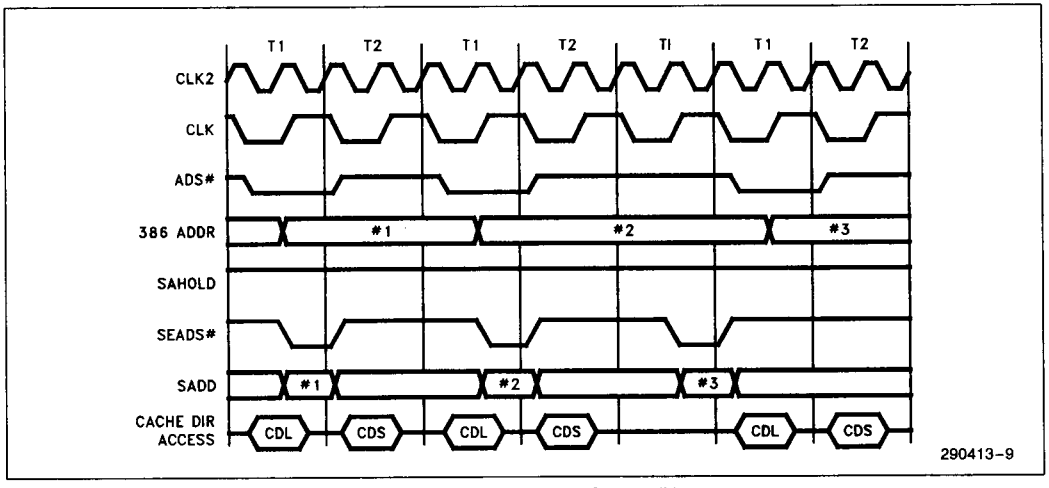

Figure 2.6 Interposing in the Cache Directory

5

2.7 Cache Flushing

The user has an option of clearing the cache by activating the FLUSH# input. When sampling the FLUSH# input low for at least four clocks, the 82396SX Smart Cache resets all the tag valid bits and the LRU bits of the Cache Directory. Thus, all the banks of the cache are invalidated. Also, the SB Line Buffer is invalidated. The FLUSH# input must have at least four CLK periods in order to be recognized. If FLUSH# is activated for longer than four CLKs, the 82396SX Smart Cache will handle all accesses as misses and it will not update the Cache Directory (the Cache Directory will be FLUSHed as long as the FLUSH# input is low). The cache is also FLUSHed during RESET. See Section 3.2.7.1.

2.8 Cache Directory Accesses and Arbitration

There are five types of accesses to the cache directory. Each access is a one clock cycle:

1) **Cache Directory Look-Up**
2) **Cache Directory Update**
3) **Cache Directory Snoop**
4) **Testability Accesses**
5) **Cache Directory FLUSH**

A description of each of these accesses follows:

1) **Cache Directory Look-up cycle (CDL):** A i386™ SX Microprocessor access in which the hit/miss decision is made. The Cache Directory is accessed by the i386™ SX Microprocessor address bus directly from the pins. CDL is executed whenever ADS# is activated, in both read and write cycles. The LRU bits are updated in every CDL hit cycle so the accessed "Way" becomes the most recently used. The LRU bits are read in every CDL miss cycle to indicate the "Way" to be updated in the Cache Directory Update cycle. Also, the WP bit is read.
2) **Cache Directory Update cycle (CDU):** A write cycle to the cache directory due to a previous miss. The CDU cycle can be caused by a TAG mismatch (either a Tag Address mismatch or a cleared TAG Valid bit). In both cases, the new TAG is written to the "Way" indicated by the LRU bits read by the previous CDL miss cycle. Also, the TAG Valid bit is turned on and the LRU algorithm is updated so the accessed "Way" becomes the most recently used. The WP bit is written according to the sampled SWP# input. The Cache Directory is accessed by the internally latched i386™ SX Microprocessor address bus. Simultaneously with the CDU cycle, the cache memory is updated.
3) **Cache Directory Snooping cycle (CDS):** A Cache Directory look-up cycle initiated by the System Bus, in response to an access to a memory location that is shared with another system master, followed by a conditional invalidation of the TAG Valid bit. If the look-up cycle results in a hit, the corresponding TAG Valid bit in the Way which detected the HIT will be cleared. CDS cycles do not affect the LRU bits. The Cache Directory is accessed by the internally latched System Bus address.
4) **Testability accesses (CDT):** Cache Directory read and write cycles performed in SRAM test mode. During the TEST accesses, the Cache Directory is read or written. No comparison is done. CDT cycles are used for debugging purposes so CDT cycles do not contend with other cycles. (See Section 7.1.)
5) **Cache Directory FLUSH cycle (CDF):** During RESET or as a result of a FLUSH# request generated by activating the FLUSH# input, all the TAG Valid bits and the LRU bits are cleared as well as the Line Buffer. CDF is one clock cycle wide if FLUSH# is active for four CLKs. If FLUSH# is activated longer the CDF cycle is N-3 CLKs, where N is the number of CLKs FLUSH# is activated for. The actual clearing of the valid bits occurs 7 CLKs after the activation of FLUSH#. Two clocks are for internal synchronization and four for recognizing FLUSH# asserted. It has higher priority than all other cycles. A CDF cycle may occur simultaneously with any other cycle but the result is always a FLUSH#ed Cache Directory.

The 82396SX Smart Cache performs the CDL cycle in T1 state. The CDU cycle, in general, is performed in the clock after the last SRDY# or SBRDY# of the Line Fill cycle. The CDS cycle is performed one clock after sampling the SEADS# active (see more details on snooping cycles in chapter 6). Supporting concurrent activities on local and system busses causes CDL cycles to be requested in any clock during the execution with a maximum rate of a CDL cycle every other clock.

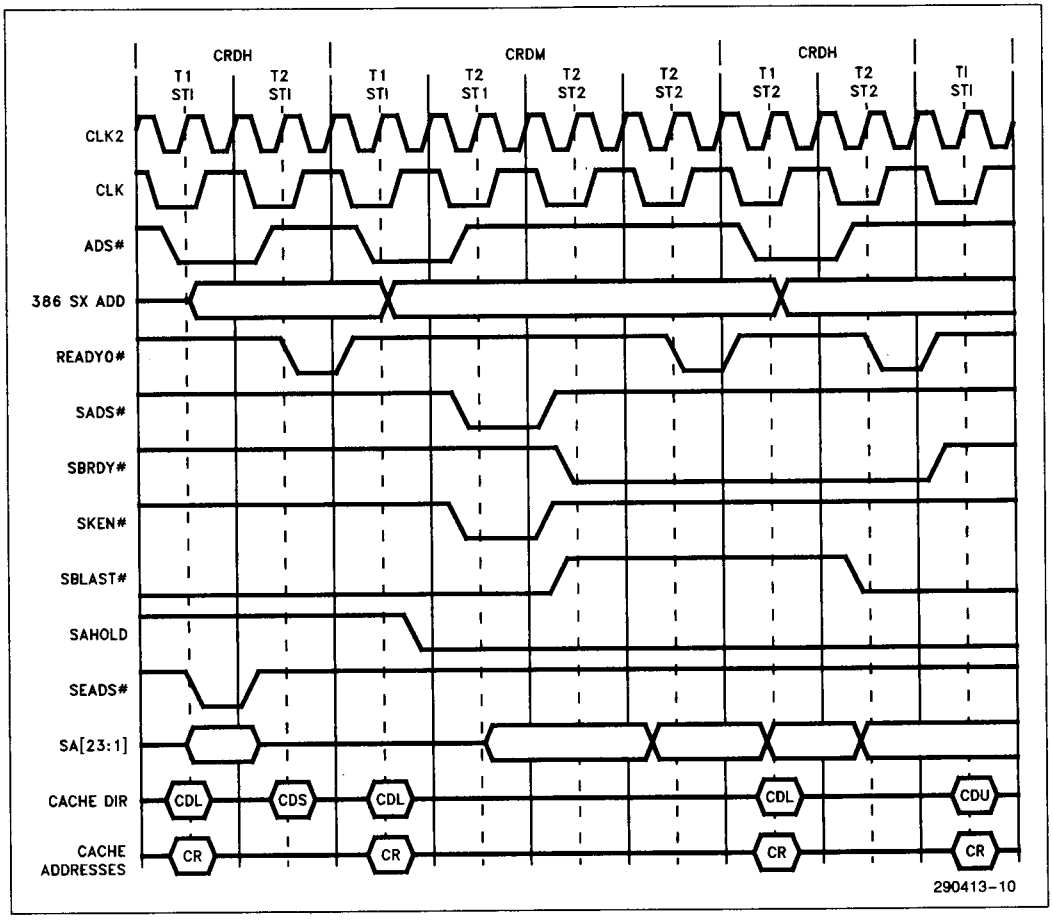

Figure 2.7 Cache Directory and Cache Accesses

The following arbitration mechanism guarantees resolution of any possible contention between CDL, CDU and CDS cycles:

1. The priority order is CDL, CDS and CDU. CDL has the highest priority, CDU has the lowest.
2. In case of simultaneous CDL and CDS cycles, the CDS will be delayed by one clock. So, the maximum latency in executing the invalidation cycle is two clocks after sampling the SEADS# active. Since the maximum rate of each of the CDL and the CDS cycles is one every other clock, the 82396SX Smart Cache is able to interpose the CDL and CDS cycles such that both are serviced. Figure 2.6 clarifies the interposing in the Cache Directory between the i386™ SX Microprocessor and the System Bus.
3. CDU cycle is executed in any clock after the last SRDY# or SBRDY# in which neither CDL nor CDS cycles are requested. The worst case is the case where immediately after the read miss, the i386™ SX Microprocessor runs consecutive read hits while the System Bus is running invalidation cycles every other clock. In this case, the CDU cycle is postponed until a free clock is inserted, which may occur due to slower look-up rate (in case of read miss, non-cacheable read,etc . . .), or due to a slower SEADS# rate.

Since every CDU cycle is synchronized with the cache update (CU - writing the retrieved line into the cache), a possible contention on the cache can occur between a cache update cycle and a cache write cycle (CW - cache is written due to a write hit cycle). In this case, the CW cycle is executed, and the CDU and CU cycles are delayed.

2.9 Cache Memory Description

The 82396SX Smart Cache memory is constructed of four banks,each bank is 2K words (4KB) and represents a "Way". For example, if the read cycle is to Way 0, bank 0 will be read. The basic cache element is a Line. The cache is able to write a full line or any byte within the line. Reads are done by word only.

There are four types of accesses to the cache data memory. Each access is a one clock cycle:

1) **Cache Read cycle**
2) **Cache Write cycle**
3) **Cache Update cycle**
4) **Testability Access**

A description of each type of access follows:

1) **Cache Read cycle (CR):** CR cycle occurs simultaneously with Cache Directory look-up cycle (CDL) if the cycle is a read. In case of a hit, the cache bank in which the hit was detected is read. In CR cycle, the A1-3 address lines select the requested word within the line.
2) **Cache Write cycle (CW):** CW cycle occurs one clock after the Cache Directory look-up cycle (CDL) if the cycle is a write hit and the WP bit is not set. The cache bank in which the hit was detected is updated. In CW cycle, the A1-3 address lines and BHE#, BLE# lines select the required bytes within the line to be written. For all write hit cycles, READYO# is returned simultaneously with the CW cycle unless the write buffer is full. When the write buffer is full the first cycle buffered must be completed on the system bus before READYO# can be asserted.
3) **Cache Update cycle (CU):** CU cycle occurs simultaneously with every Cache Directory update cycle (CDU). The full line is written.
4) **Testability accesses (CT):** cache read and write cycles performed by the 82396SX Smart Cache TEST machine. During the TEST accesses, the cache memory acts as a standard RAM. CT cycles are used for debugging purposes so CT cycles do not contend with other cycles.

The Cache Directory arbitration rules guarantee that contention will not occur in the cache accesses. This is since CR is synchronized with CDL cycle, CU is synchronized with CDU cycle, CW cannot occur simultaneously with CR cycles (ADS# not activated while READYO# is returned since i386™ SX Microprocessor is not pipelined) and finally the possible contention of CW and CU is resolved. See figure 2.7 for an example of Cache Directory and cache memory accesses during a typical cycle execution.

3.0 PIN DESCRIPTION

The 82396SX Smart Cache pins may be divided into 4 groups:

1. Local Bus interface pins
2. System Bus interface pins
3. Local Bus decode pins
4. System Bus decode pins

Some notes regarding these groups of pins follow:

1. All Pins - All input and I/O pins (when used as inputs) must be synchronous to CLK2, to guarantee proper operation. Exceptions are the RESET pin, where only the falling edge needs to be synchronous to CLK2, and A20M# and FLUSH# pins, which are asynchronous.
2. Local Bus Interface Pins - All Local Bus interface pins that have a corresponding i386™ SX Microprocessor signal (A1–23, W/R#, D/C#, M/IO#, LOCK#, and D0-15) must be connected directly to the corresponding i386™ SX Microprocessor pins.
3. Local / System Bus Decode Pins - These signals are generated by proper decoding of the Local and System Bus addresses. The decoding for the Local Bus decode pins, NPI# and BEM, must be static. The decoding for the System Bus Decode pins, SKEN# and SWP#, must be static over the line boundary. They must not change during a Line Fill. If a change in the decoding of any of these signals is made, the 82396SX Smart Cache must be FLUSH#ed or RESET.

3.1 Local Bus Interface Pins

3.1.1 i386™ SX MICROPROCESSOR/82396SX SMART CACHE CLOCK (CLK2 I)

This signal provides the fundamental timing for the 82396SX Smart Cache. The 82396SX Smart Cache, like the i386™ SX Microprocessor, divides CLK2 by two to generate the internal clock. The phase of the internal 82396SX Smart Cache clock is synchronized to the internal CPU clock phase by the RESET signal. All external timing parameters are specified with respect to the rising edge of CLK2. Dynamic frequency changes are not allowed.

3.1.2 LOCAL ADDRESS BUS

3.1.2.1 Local Bus Address Lines (A[23:1] I)

These signals, along with the byte enable signals, define the physical area of memory or I/O accessed.

3.1.2.2 Local Bus Byte Enables (BHE#,BLE# I)

These pins are used to determine which bytes are accessed in partial write cycles. On read-hit cycles those lines are ignored by the 82396SX Smart Cache. On write hit cycles they determine which bytes in the internal Cache SRAM must be updated, and passed to the System Bus along with the System Bus write cycle. If BEM is inactive, these signals are mirrored by SBHE# and SBLE# for all writes, non-cacheable reads and the first access of a Line Fill. These signals are active LOW.

3.1.3 LOCAL BUS CYCLE DEFINITION

3.1.3.1 Local Bus Cycle Definition Signals (W/R#,D/C#,M/IO# I)

The memory/input-output, data/code, write/read lines are the primary bus definition signals directly connected to the i386™ SX Microprocessor. These signals become valid as the ADS# signal is sampled asserted. The bus cycle type encoding is identical to that of the i386™ SX Microprocessor. The i386™ SX Microprocessor encoding is shown in table 5.1. The bus definition signals are not driven by the i386™ SX Microprocessor during bus hold and follow the timing of the address bus.

3.1.3.2 Local Bus Lock (LOCK# I)

This signal indicates a LOCK#ed cycle. LOCK#ed cycles are treated as non-cacheable cycles, except that LOCK#ed write hit cycles update the cache as well. LOCK#ed write cycles are not buffered.

The 82396SX Smart Cache asserts SLOCK# when the first LOCK#ed cycle is initiated on the System Bus. SLOCK# is deactivated only after all LOCK#ed System Bus cycles were executed, and LOCK# was deactivated.

3.1.4 LOCAL BUS CONTROL

3.1.4.1 Address Status (ADS# I)

The address status pin, an output of the i386™ SX Microprocessor, indicates that new, valid address and cycle definition information is currently available on the Local Bus. The signals that are valid when ADS# is activated are:

A(1-23), BHE#, BLE#, W/R#, D/C#, M/IO#, LOCK#, NPI# and BEM

3.1.4.2 Local Bus Ready (READYI# I)

This is the ready input signal seen by the Local Bus master. Typically it is a logical OR between the 82396SX Smart Cache generated READYO# signal and the i387™ SX Math Coprocessor READY# signal. It is used by the 82396SX Smart Cache, along with the ADS# signal, to keep track of the i386™ SX Microprocessor bus state. READYI# should not be driven active during T1 and should not be delayed from READYO# by one or more clocks.

3.1.4.3 Local Bus Ready Output (READYO# O)

This output is returned to the i386™ SX Microprocessor to terminate all types of i386™ SX Microprocessor bus cycles, except for Local Bus cycles.

The READYO# may serve as READY# signal for the i387™ SX Math Coprocessor. For details, refer to Chapter 5.

3.1.5 RESET (RESET I)

This signal forces the 82396SX Smart Cache to begin execution at a known state. The RESET falling edge is used by the 82396SX Smart Cache to set the phase of its internal clock identical to the i386™ SX Microprocessor internal clock. The RESET falling edge must satisfy the appropriate setup and hold times for proper chip operation. RESET must remain active for at least 1ms after power supply and CLK2 input have reached their proper DC and AC specifications.

The RESET input is used for two purposes: first, it RESETs the 82396SX Smart Cache and brings it to a known state. Second, it is used to synchronize the internal 82396SX Smart Cache clock phase to that of the i386™ SX Microprocessor.

On power up, RESET must be active for at least 1 millisecond after power has stabilized to a voltage within spec, and after CLK2 input has stabilized to voltage and frequency within spec. This is to allow the internal circuitry to stabilize. Otherwise, RESET must be active for at least 10 clock cycles.

No access to the 82396SX Smart Cache is allowed for 128 clock cycles after the RESET falling edge. During RESET, all other input pins are ignored, except SHOLD, and SAHOLD. Unlike the i386™ SX Microprocessor, the 82396SX Smart Cache can respond to a System Bus HOLD request by floating its bus and asserting SHLDA even while RESET is asserted. Also the 82396SX Smart Cache can respond to a System Bus address HOLD request by floating its address bus. The status of the 82396SX Smart Cache outputs during RESET is shown in Table 3.2.

The user must not drive SAHOLD and FLUSH# active during the two CLK2s prior to driving RESET inactive. If they do the Tristate Test Mode will be entered. The user must also insure that FLUSH# does not get activated for one CLK cycle while SAHOLD is deactivated for the same CLK cycle prior to RESET falling. If this condition exists a reserved mode will be entered (See Chapter 7).

3.1.6 LOCAL DATA BUS

3.1.6.1 Local Bus Data Lines (D[15:0] I/O)

These are the Local Bus data lines of the 82396SX Smart Cache and must be connected to the D[15:0] signals of the Local Bus.

3.1.7 LOCAL BUS DECODE PIN

3.1.7.1 No Post Input (NPI# I)

This signal instructs the 82396SX Smart Cache that the write cycle currently in progress must not be posted (buffered) in the write buffer. NPI# is sampled on the falling edge of CLK following the address change, see figure 5.1. NPI# is ignored during read cycles. This signal is active LOW.

3.1.7.2 Byte Enable Mask (BEM I)

The Byte Enable Mask signal, when asserted, causes the local bus byte enable signals to be masked so that both system bus byte enables are asserted on non-locked memory read cycles. If BEM is asserted during cacheable read cycles and that cycle requires a Line Fill (cache read miss), then both bytes will be accessed during the first cycle of the Line Fill. If BEM is not used (tied low), the system must return valid data for both bytes on the first access of a Line Fill to ensure that the cache stores valid data for both bytes in case the processor requested one. This signal is active HIGH.

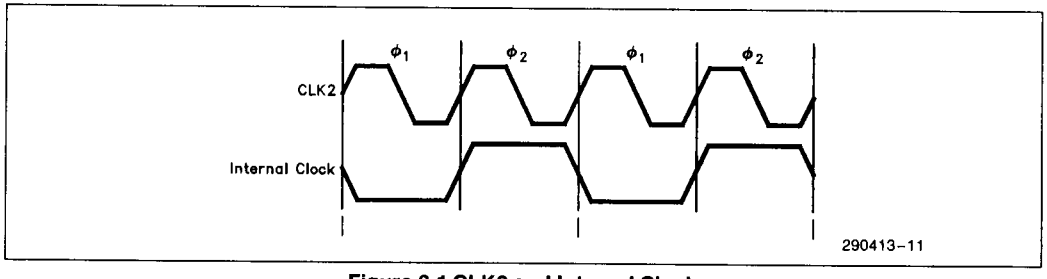

Figure 3.1 CLK2 and Internal Clock

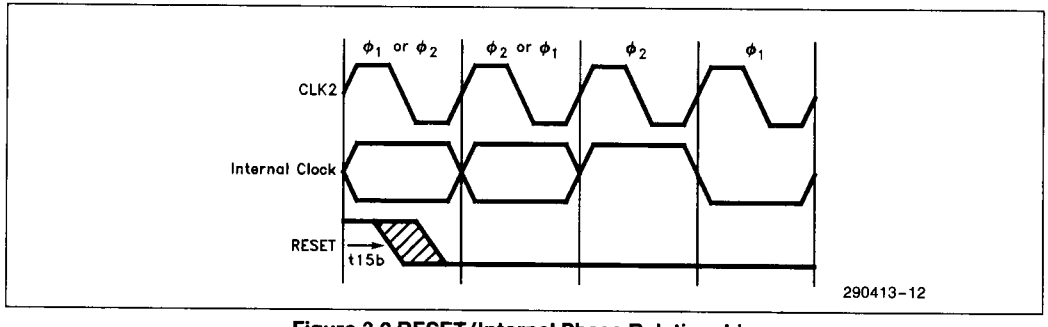

Figure 3.2 RESET/Internal Phase Relationship

3.1.8 ADDRESS MASK

3.1.8.1 Address Bit 20 Mask (A20M# I)

This pin, when active (low), forces the A20 input as seen by the 82396SX Smart Cache to logic '0', regardless of the actual value on the A20 input pin. It must be asserted two clock cycles before ADS# for proper operation. A20M# emulates the address wraparound at 1 Mbyte which occurs on the 8086. This pin is asynchronous but must meet setup and hold times to guarantee recognition in a specific clock. It must be stable throughout Local Bus memory cycles.

3.2 System Bus Interface Pins

3.2.1 SYSTEM ADDRESS BUS

3.2.1.1 System Bus Address Lines (SA[23:1] I/O *)

* SA1–3 are outputs only.

These are the SYSTEM BUS address lines of the 82396SX Smart Cache. When driven by the 82396SX Smart Cache, these signals, along with the System Bus byte enables define the physical area of memory or I/O accessed.

SA4-23 are always inputs and are sampled when SEADS# is active.

3.2.1.2 System Bus Byte High Enable and System Bus Byte Low Enable (SBHE#, SBLE# O)

These are the Byte Enable signals for the System Bus. When BEM is inactive the 82396SX Smart Cache drives these pins identically to BHE# and BLE# in all system bus cycles except Line Fills. In Line Fills these signals are driven identically to BHE# and BLE# in the first read cycle of the Line Fill. They are both driven active in the remaining cycles of the Line Fill. When BEM is active, the 82396SX Smart Cache will assert SBHE# and SBLE# for all non-locked memory read cycles. These signals are active LOW.

3.2.2 SYSTEM BUS CYCLE DEFINITION

3.2.2.1 System Bus Cycle Definition (SW/R#, SD/C#, SM/IO# O)

These are the System Bus cycle definition pins. When the 82396SX Smart Cache is the System Bus master, it drives these signals identically to the i386™ SX Microprocessor encoding.

3.2.2.2 System Bus Lock (SLOCK# O)

The System Bus LOCK pin is one of the bus cycle definition pins. It indicates that the current bus cycle is LOCK#ed: that the 82396SX Smart Cache (on behalf of the CPU) must be allowed exclusive access to the System Bus across bus cycle boundaries until this signal is de-asserted. The 82396SX Smart Cache does not acknowledge a bus hold request when this signal is asserted.

The 82396SX Smart Cache asserts SLOCK# when the first LOCK#ed cycle is initiated on the System Bus. SLOCK# is deactivated only after all LOCK#ed System Bus cycles were executed, and LOCK# was deactivated. SLOCK# is active LOW.

3.2.3 SYSTEM BUS CONTROL

3.2.3.1 System Bus Address Status (SADS# O)

The address status pin is used to indicate that new, valid address and cycle definition information is currently being driven onto the address, byte enable and cycle definition lines of the System Bus. SADS# can be used as an indication of a new cycle start. SADS# is driven active in the same clock as the addresses are driven. SADS# is not valid until a specified setup time before the CLK falling edge, and must be sampled by CLK falling edge before it is used by the system. This signal is active LOW.

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3.2.3.2 System Bus Ready (SRDY# I)

The SRDY# signal indicates that the current bus cycle is complete. When SRDY# is sampled asserted it indicates that the external system has presented valid data on the data pins in response to a read cycle or that the external system has accepted the 82396SX Smart Cache data in response to a write request. This signal is ignored when the SYSTEM BUS is at STi, STH, ST1 or ST1P states.

At the first read cycle of a Line Fill, if SBRDY# is returned active and both SRDY# and SNA# are returned inactive, a burst Line Fill will be executed. If SRDY# is returned active and SNA# is returned inactive, a non-burst non-pipelined Line Fill will be executed. If SNA# is returned active and SRDY# is inactive, a non-burst pipelined line fill will be executed. A non-burst, non-pipelined Line Fill is started if SRDY# or SBRDY# is active during ST2 together with SNA# active.

Once a burst Line Fill has started, if SRDY# is returned in the second through the seventh word of the transfer, the burst Line Fill will be interrupted and the cache will not be updated. The first word will already have been transferred to the CPU. Note that

in the last (eighth) bus cycle in a Line Fill, SBRDY# and SRDY# have the same effect on the 82396SX Smart Cache. They indicate the end of the Line Fill. This signal is active LOW.

3.2.3.3 System Bus Next Address (SNA# I)

This input, when active, indicates that a pipelined address cycle can be executed. It is sampled by the 82396SX Smart Cache in the same timing as the i386™ SX Microprocessor samples NA#. If this signal is sampled active, then SBRDY# is treated as SRDY#, i.e. burst Line Fills are disabled. This signal is ignored once a burst Line Fill has started as well as during the eighth word of a Line Fill.

3.2.4 BUS ARBITRATION

3.2.4.1 System Bus Hold Request (SHOLD I)

This signal allows another bus master complete control of the entire System Bus. In response to this pin, the 82396SX Smart Cache floats all its system bus interface output and input/output pins (With the Exception of SHLDA) and asserts SHLDA after completing its current bus cycle or sequence of LOCK#ed cycles. The 82396SX Smart Cache maintains its bus in this state until SHOLD is deasserted. SHOLD is active HIGH. SHOLD is recognized during reset.

3.2.4.2 System Bus Hold Acknowledge (SHLDA O)

This signal goes active in response to a hold request presented on the SHOLD pin and indicates that the 82396SX Smart Cache has given the bus to another System Bus master. It is driven active in the same clock that the 82396SX Smart Cache floats its bus. When leaving a bus hold, SHLDA is driven inactive in one clock and the 82396SX Smart Cache resumes driving the bus. Depending on internal requests the 82396SX Smart Cache may, or may not begin a System Bus cycle in the clock where SHLDA is driven inactive. The 82396SX Smart Cache is able to support CPU Local Bus activities during System Bus hold, since the internal cache is able to satisfy the majority of those requests. This signal is active HIGH.

3.2.5 BURST CONTROL

3.2.5.1 System Bus Burst Ready (SBRDY# I)

This signal performs the same function during a burst cycle that SRDY# does in a non-burst cycle. SBRDY# asserted indicates that the external system has presented valid data on the data pins in response to a burst Line Fill cycle. This signal is ignored when the SYSTEM BUS is at STi, STH, ST1 or ST1P states.

Note that in the last (eighth) bus cycle in a Line Fill, SBRDY# and SRDY# have the same effect on the 82396SX Smart Cache. They indicate the end of Line Fill. For all cycles that cannot run in burst, e.g. noncacheable cycles, non Line Fill cycles (or pipelined Line Fill), SBRDY# has the same effect on the 82396SX Smart Cache as the normal SRDY# pin. This signal is active LOW.

3.2.5.2 System Bus Burst Last Cycle Indicator (SBLAST# O)

The system burst last cycle signal indicates that the next time SBRDY# is returned the burst transfer is complete. In other words, it indicates to the external system that the next SBRDY# returned is treated as a normal SRDY# by the 82396SX Smart Cache, i.e., another set of addresses will be driven with SADS# or the SYSTEM BUS will go idle. SBLAST# is normally active. In a cache read miss cycle, which may proceed as a Line Fill, SBLAST# starts active and later follows SKEN# by one clock. SBLAST# is active during non-burst Line Fill cycles. Refer to Chapter 6 for more details. This signal is active LOW.

3.2.6 CACHE INVALIDATION

3.2.6.1 System Bus Address Hold (SAHOLD I)

This is the Address Hold request. It allows another bus master access to the address bus of the 82396SX Smart Cache in order to indicate the address of an external cycle for performing an internal Cache Directory lookup and invalidation cycle. In response to this signal, the 82396SX Smart Cache immediately (in the next cycle) stops driving the entire system address bus (SA[23:1]). Because the 82396SX Smart Cache always stops driving the address bus, in response to system bus address hold request, no hold acknowledge is required. Only the address bus will be floated during address hold, Other signals can remain active. For example, data can be returned for a previously specified bus cycle during address hold. The 82396SX Smart Cache does not initiate another bus cycle during address hold.

This pin is recognized during RESET. However, since the entire cache is invalidated by reset, any invalidation cycles run will be superfluous. This signal is active high.

3.2.6.2 System Bus External Address Strobe (SEADS# I)

This signal indicates that a valid external address has been driven onto the 82396SX Smart Cache pins and that this address must be used to perform an internal cache invalidation cycle. Maximum allowed invalidation cycle rate is one every two clock cycles. This signal is active LOW. SEADS# is a synchronous signal and has both setup and hold timing specifications referenced in CLK2.

3.2.7 CACHE CONTROL

3.2.7.1 Flush (FLUSH# I)

This pin, when sampled active for four clock cycles or more, causes the 82396SX Smart Cache to invalidate its entire Tag Array. In addition, it is used to configure the 82396SX Smart Cache to enter various test modes. For details refer to Chapter 7. This pin is asynchronous but must meet setup and hold times to guarantee recognition in any specific clock. This signal is active LOW.

Activation of FLUSH# does not prevent Line Fills. Although the TAG Valid bit will be cleared, the Line Fill can still occur on the System Bus. To prevent a Line Fill from occurring, the SKEN# signal must be deactivated.

3.2.8 SYSTEM DATA BUS

3.2.8.1 System Bus Data Lines (SD[15:0] I/O)

These are the SYSTEM BUS data lines of the 82396SX Smart Cache. The lines must be driven with appropriate setup and hold times for proper operation. These signals are driven by the 82396SX Smart Cache only during write cycles.

3.2.9 SYSTEM BUS DECODE PINS

3.2.9.1 System Cacheability Enable (SKEN# I)

This is the cache enable pin. It is used to determine whether the current cycle running on the System Bus is cacheable or not. When the 82396SX Smart Cache generates a read cycle that may be cached, this pin is sampled 1 CLK before the first SBRDY#, SRDY# or SNA# is sampled active (for detailed timing description, refer to Chapter 6). If sampled active, the cycle will be transformed into a Line Fill. Otherwise, the Cache and Cache Directory will be unaffected. Note that SKEN# is ignored after the first cycle in a Line Fill. SKEN# is ignored during all System Bus cycles except for cacheable read miss cycles. This signal is active LOW.

3.2.9.2 System Write Protect Indication (SWP# I)

This is the write protect indicator pin. It is used to determine whether the address of the current system bus Line Fill cycle is write protected or not.

In non-pipelined cycles, the SWP# is sampled with the first SRDY# or SBRDY# of a system Line Fill cycle. In pipelined cycles, SWP# is sampled at the last ST2 stage, or at ST1P; in other words, one clock phase after SNA# is sampled active.

The write protect indicator is sampled together with the TAG address of each line in the 82396SX Smart Cache Directory. In every cacheable write cycle, the write protect indicator is read. If active, the cycle will be a Write Protected cycle which is treated like cacheable write miss cycle. It is buffered and it does not update the cache even if the addressed location is present in the cache. The signal is active LOW.

3.3 Pinout Summary Tables

Table 3.1 Input Pins

Name	Function	Synchronous/ Asynchronous	Active Level
CLK2	Clock		
RESET	Reset	Asynchronous*	High
BHE#	Local Bus Byte High Enable	Synchronous	Low
BLE#	Local Bus Byte Low Enable	Synchronous	Low
A1–23	Local Bus Address Lines	Synchronous	—
W/R#	Local Bus Write/Read	Synchronous	—
D/C#	Local Bus Data/Code	Synchronous	—
M/IO#	Local Bus Memory/Input-Output	Synchronous	—
LOCK#	Local Bus LOCK	Synchronous	Low
ADS#	Local Bus Address Strobe	Synchronous	Low
READYI#	Local Bus READY	Synchronous	Low
NPI#	No Post Input	Synchronous	Low
BEM	Byte Enable Mask	Synchronous	High
FLUSH#	FLUSH# the 82396SX Smart Cache	Asynchronous	Low
A20M#	Address Bit 20 Mask	Asynchronous	Low
SHOLD	SYSTEM BUS Hold Request	Synchronous	High
SRDY#	SYSTEM BUS READY	Synchronous	Low
SNA#	SYSTEM BUS Next Address Indication	Synchronous	Low
SBRDY#	SYSTEM BUS Burst Ready	Synchronous	Low
SKEN#	System Cacheability Indication	Synchronous	Low
SWP#	System Write Protect Indication	Synchronous	Low
SAHOLD	SYSTEM BUS Address HOLD	Synchronous	High
SEADS#	SYSTEM BUS External Address Strobe	Synchronous	Low

* The falling edge of RESET needs to be synchronous to CLK2 but the rising edge is asynchronous.

Table 3.2 Output Pins

Name	Function	When Floated	State(3) at RESET	Active Level
SBHE#	SYSTEM BUS Byte High Enable	SHLDA	Low	Low
SBLE#	SYSTEM BUS Byte Low Enable	SHLDA	Low	Low
SADS#	SYSTEM BUS Address Strobe	SHLDA(1)	High	Low
SD/C#	SYSTEM BUS Data/Code	SHLDA	High	—
SM/IO#	SYSTEM BUS Memory/Input-Output	SHLDA	Low	—
SW/R#	SYSTEM BUS Write/Read	SHLDA	Low	—
SHLDA	SYSTEM BUS HOLD Acknowledge	—	Low(2)	High
SLOCK#	SYSTEM BUS LOCK	SHLDA	High	Low
SBLAST#	SYSTEM BUS Burst Last Cycle Indication	SHLDA	Low	Low
SA1–3	SYSTEM BUS Address (3 lowest order bits)	SHLDA/SAHOLD	High	—

(1) SADS# is driven high before it is floated in each first ST2/ST1P
(2) Unless SHOLD is asserted
(3) Provided SHOLD and SAHOLD are inactive

Table 3.3 Input-Output Pins

Name	Function	When Floated	State(1) at RESET	Active Level
D0–15	Local Data Bus(2)	Always Except READs	Z	—
SD0–15	System Data Bus(3)	Always Except WRITEs	Z	—
SA4–23	SYSTEM BUS Address (except the 3 lowest order bits)	SHLDA/SAHOLD	High	—
READYO#	Local Bus READY(2)		High	Low

(1) Provided SHOLD and SAHOLD are inactive
(2) This signal is driven only in T2
(3) This signal is driven only in ST2

4.0 BASIC FUNCTIONAL DESCRIPTION

The 82396SX Smart Cache has an interface to the i386™ SX Microprocessor (Local Bus) and to the System Bus. The System Bus interface emulates the i386™ SX Microprocessor bus such that the system will view the 82396SX Smart Cache as the front end of a i386™ SX Microprocessor. Some optional enhancements, like burst support, are provided to maximize the performance.

When ADS# is sampled active, the 82396SX Smart Cache decodes the i386™ SX Microprocessor cycle definition signals (M/IO#, D/C#, W/R# and LOCK#), as well as the Local Bus decode signal (NPI# and BEM), to determine how to respond. NPI# indicates that the current memory write cycle must not be buffered. In addition, the 82396SX Smart Cache internally decodes the i386™ SX Microprocessor accesses to the i387™ SX Math Coprocessor as Local Bus accesses. The result of the address, cycle definition and cycle qualification decoding is two categories of accesses, i387™ SX Math Coprocessor and 82396SX Smart Cache accesses. In i387™ SX Math Coprocessor accesses, the 82396SX Smart Cache drives the READYO# signal active after one wait state, if the READYI# was not sampled active.

Any 82396SX Smart Cache access can be either to a cacheable address or to a non-cacheable address. Non-cacheable addresses are all I/O and system accesses with SKEN# returned inactive. Non-cacheable cycles are all cycles to non-cacheable addresses, LOCK#ed read cycles and Halt/Shutdown cycles. All other cycles are cacheable. For more details about non-cacheable cycles, refer to Section 4.2. Non-cacheable cycles pass through the cache. They are always forwarded to the System Bus.

Cacheable read cycles can be either hit or miss. Cacheable read hit cycles are serviced by the internal cache and they don't require System Bus service. A cacheable read miss cycle generates a series of eight System Bus read cycles, called a Line Fill. Of the eight cycles, the first cycle is for reading the requested data while all eight are for filling the cache line. The System Bus has the ability to provide the system cacheability attribute to the 82396SX Smart Cache Line Fill request, via the SKEN# input, and the system write protection indicator, via the SWP# input. Refer to chapter 6 for more information about Line Fill cycles.

Cacheable write cycles, as any write cycles, are forwarded to the System Bus. The write buffer algorithm terminates the write cycle on the Local Bus, allowing the i386™ SX Microprocessor to continue processing in zero wait states, while the 82396SX Smart Cache executes the write cycles on the System Bus. All cacheable write hit cycles, except protected writes, update the cache on a byte basis i.e. only the selected bytes are updated. Cacheable write misses do not update the cache (the 82396SX Smart Cache does not allocate on writes). All cacheable write cycles, except LOCK#ed writes, are buffered (unless the NPI# pin is sampled active).

Cache consistency is provided by SEADS#. If any bus master performs a memory cycle which disturbs the data consistency, the address can be provided to the 82396SX Smart Cache by the other bus master using SAHOLD or SHOLD/SHLDA. Then, the 82396SX Smart Cache checks if that memory location resides in the cache. If it does, the 82396SX Smart Cache invalidates that line in the cache by marking it as invalid in the Cache Directory. The 82396SX Smart Cache interposes the Cache Directory between the i386™ SX Microprocessor and the System Bus such that the i386™ SX Microprocessor is not forced to wait due to snooping and none of the snooping cycles are missed due to i386™ SX Microprocessor accesses (see Figure 2.6).

Cacheability is resolved on the system side using the SKEN# input. SKEN# is sampled one clock before the first SRDY#/SBRDY# in non pipelined Line Fill cycles. In pipelined Line Fill cycles, SKEN# is sampled one clock phase before sampling SNA# active. SKEN# is always sampled at PHI1.

Note that the 82396SX Smart Cache does not support pipelining of the i386™ SX Microprocessor Local Bus. The NA# input on the i386™ SX Microprocessor must be tied to Vcc.

4.1 Cacheable Accesses

In a cacheable access, the 82396SX Smart Cache performs a cache directory look-up cycle. This is to determine if the requested data exists in the cache and to read the write protection bit. In parallel, the 82396SX Smart Cache performs a cache read cycle if the access is a read, or prepares the cache for a write cycle if the access is a write.

4.1.1 CACHEABLE READ HIT ACCESSES

If the Cache Directory look-up for a cacheable read access results in a hit (the requested data exists in the cache), the 82396SX Smart Cache drives the local data bus by the data provided from the internal cache. It also drives the i386™ SX Microprocessor READY# (by activating the 82396SX Smart Cache READYO#), so that the i386™ SX Microprocessor gets the required data directly from the cache without any wait states.

The 82396SX Smart Cache is a four Way set associative cache, so only one of the four ways (four banks) is selected to supply data to the i386™ SX Microprocessor. The Way in which the hit occurred will provide the data. Also, the replacement algorithm (LRU) is updated such that the Way in which the hit occurred is marked as the most recently used.

4.1.2 CACHEABLE READ MISS ACCESSES

READYO# is always activated in the first T2 of cache read miss cycles. In order to meet the timing requirements READYO# must be activated prior to the hit/miss decision. Once the hit/miss decision is made and the cycle is a miss, READYO# is deactivated. This activation only occurs prior to the max valid delay specification (t20 max). After the max valid delay spec, READYO# will always be stable. See Figure 4.0.

If the Cache Directory look-up results in a miss, the 82396SX Smart Cache transfers the request to the System Bus in order to read the data from the main memory and for updating the cache. A full line is updated in a cache update cycle. As a result of a cache miss, the 82396SX Smart Cache performs eight System Bus accesses to read eight words from the DRAM, and write the eight words to the cache. This is called a Line Fill cycle. The first word accessed in a Line Fill cycle is for the word which the i386™ SX Microprocessor requested and the 82396SX Smart Cache provides the data and drives the READYO# one clock after it gets the first word from the System Bus.

The 82396SX Smart Cache provides the option of supporting burst bus in order to minimize the latency of a line fill. Also, the 82396SX Smart Cache provides the SKEN# input, which, if inactive, converts a Line Fill cycle to a non-cacheable cycle. Write protection is also provided. The write protection indicator is stored together with the TAG Valid bit and the TAG field of every line in the Cache Directory. For more details refer to Chapter 6.

The 82396SX Smart Cache features Line Buffer cacheing. In a Line Fill the data for the eight words is stored in a buffer, the Line Buffer, as it is accumulated. After filling the Line Buffer, the 82396SX Smart Cache performs the Cache Update and the Cache Directory Update. If the access is a hit to the line buffer it can be serviced in zero wait states. The updated Way is the least recently used Way flagged by the Pseudo LRU algorithm during the Cache Directory Lookup cycle if all Ways are valid. If there is a non-valid Way it will be updated.

The SRDY# (System Bus READY#) active indicates the completion of the System Bus cycle and

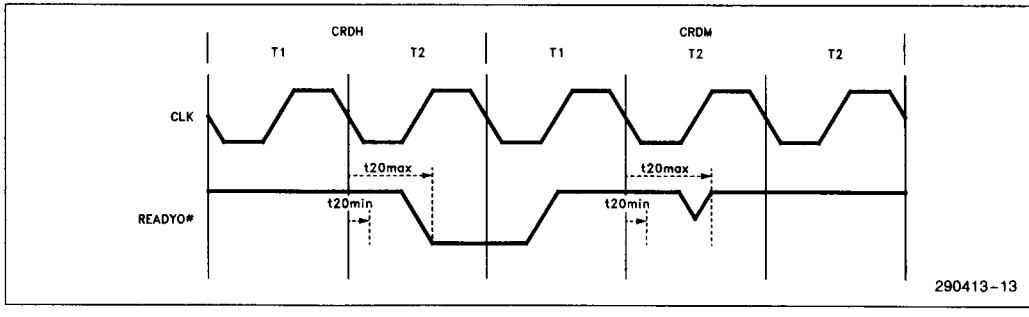

Figure 4.0 READYO# Behavior

SBRDY# (System Bus Burst READY#) active indicates the completion of a burst System Bus cycle. In a i386™ SX Microprocessor-like system, the 82396SX Smart Cache drives the i386™ SX Microprocessor READY# one clock after the first SRDY# and, in a burst system, one clock after the first SBRDY#. This frees up the Local Bus, allowing the i386™ SX Microprocessor to execute the next instruction, while filling the cache. So, during Line Fills, there is no advantage in driving the i386™ SX Microprocessor into the pipelined mode. **Therefore, the 82396SX Smart Cache does not drive the i386™ SX Microprocessor's NA# at all. NA# must be tied to VCC.**

4.1.2.1 Burst Bus

The 82396SX Smart Cache offers an option to minimize the latency in Line Fills. This option is the burst bus and is only applicable to Line Fill cycles. By generation of a burst bus compatible DRAM controller, one which generates SBRDY# and SBLAST# to take advantage of the 82396SX Smart Cache's burst feature, the number of cycles required for a Line Fill to be completed is significantly reduced. Details of burst Line Fills can be found in Chapter 6.

4.1.3 CACHE WRITE ACCESSES

The 82396SX Smart Cache supports the write buffer policy, which means that main memory is always updated in any write cycle. However, the cache is updated only when the write cycle hits the cache and the accessed address is not write protected. In cache write misses, the cache is not updated (allocation in writes is not supported).

The 82396SX Smart Cache has a write buffer of four words. Only the cacheable write cycles, except LOCK#ed writes, are buffered so, if the write buffer is not full, the 82396SX Smart Cache buffers the cycle. This means that the data, address and cycle definition signals are written in one entry of the write buffer and the 82396SX Smart Cache drives the READYO# in the first T2 so all the buffered write cycles run without wait states. If the write buffer is full, the 82396SX Smart Cache delays the READYO# until the completion of the execution of the first buffered write cycle. The execution of the buffered write cycles depends on the availability of the System Bus. In a non-buffered write cycle, e.g. I/O writes, the i386™ SX Microprocessor is forced to wait until the execution of all the buffered writes and the non-buffered write. READYO# is driven one clock after the SRDY# of the non-buffered write. More details about the write buffer can be found in Chapter 6.

In cacheable non-write protected write hit cycles, only the appropriate bytes within the line are updated. The updated bytes are selected by decoding A1–A3 and the BHE# and BLE# lines. The LRU is updated so that the hit Way is the most recently used, as in cache read hit cycles.

All cacheable writes, whether hits or misses, are executed on the System Bus. The System Bus write cycle address, data and cycle definition signals are the same as the i386™ SX Microprocessor signals. All buffered writes run with zero wait states if the write buffer is not full.

4.2 Noncacheable System Bus Accesses

Non-cacheable cycles are any of the following 82396SX Smart Cache cycles:

1) All I/O cycles.
2) All LOCK#ed read cycles.
3) Halt/Shutdown cycles.
4) SRAM mode cycles not addressing the internal cache or Tagram.

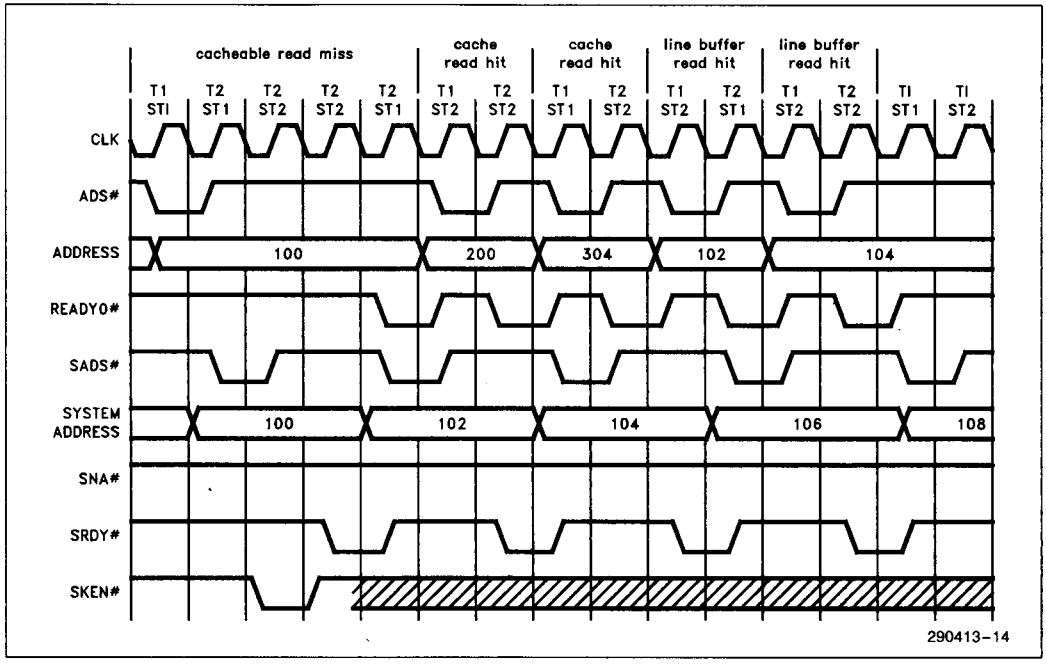

Figure 4.1 Read Hit Cycles During Line Fill

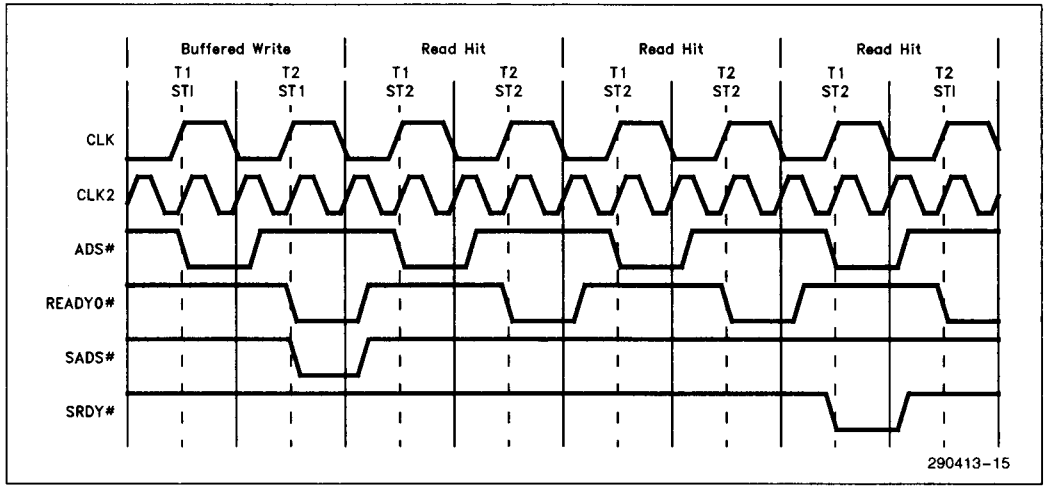

Figure 4.2 Cache Read Hit Cycles While Executing a Buffered Write on the System Bus.

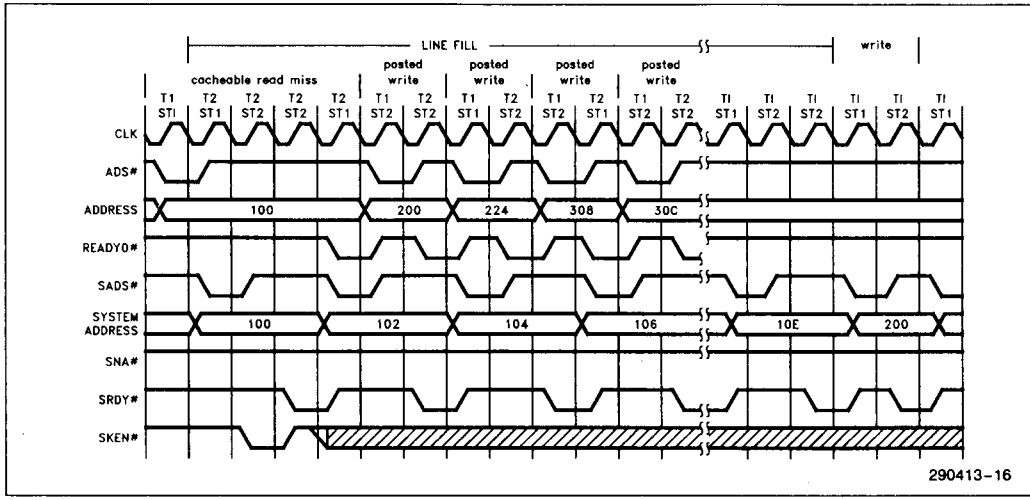

Figure 4.3 Buffered Write Cycles During a Line Fill

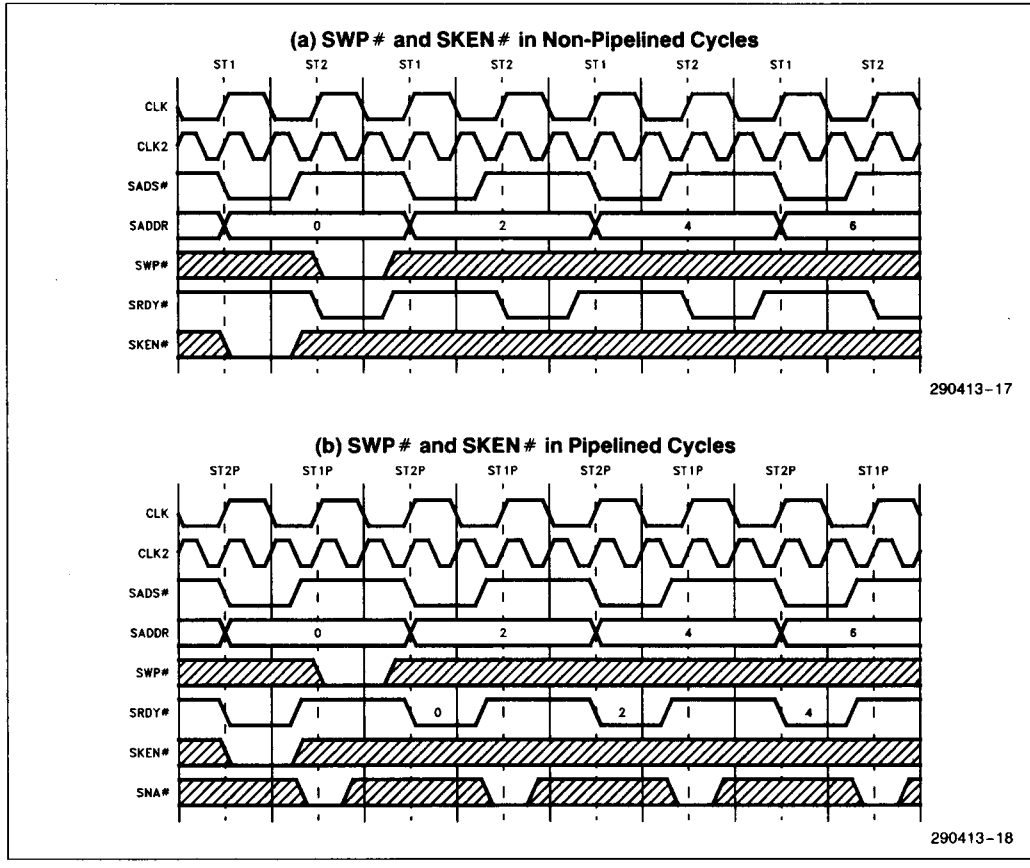

Figure 4.4 SWP# and SKEN# Timing

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Table 4.1 i386™ SX Microprocessor Bus Cycle Definition with Cacheability

M/IO#	D/C#	W/R#	i386™ SX Microprocessor Cycle Definition	Cacheable/ Non-Cacheable	Writes Posted
0	0	0	Interrupt Acknowledge	Non-cacheable	—
0	0	1	Undefined	—	—
0	1	0	I/O Read	Non-cacheable	—
0	1	1	I/O Write	Non-cacheable	No
1	0	0	Memory Code Read	Cacheable(1)	—
1	0	1	Halt/Shutdown	Non-cacheable	No
1	1	0	Memory Data Read	Cacheable(1)	—
1	1	1	Memory Data Write	Cacheable(1)	Yes(2)

NOTES:
1. Cacheability is controlled by SKEN# and SWP#.
2. Writes are not posted if NPI# is asserted.

All the above cycles are defined as non-cacheable by the Local Bus interface controller. In addition, Line Fill cycles in which the SKEN# was returned inactive are aborted. They are called Aborted Line Fills (ALF).

Non-cacheable cycles are never serviced from the cache and they don't update the cache. They are always referred to the System Bus. In non-cacheable cycles, the 82396SX Smart Cache transfers to the System Bus the exact i386™ SX Microprocessor bus cycle.

A description of LOCK#ed cycles can be found in Chapter 5.

4.3 Local and System Bus Concurrency

Concurrency between local and System Busses is supported in several cases:

1. Read hit cycles can run while executing a Line Fill on the System Bus. Refer to timing diagram 4.1.
2. Read hit cycles can run while executing buffered write cycles on System Bus. Refer to timing diagram 4.2.
3. Write cycles are buffered while the System Bus is running other cycles, including other buffered writes. They are also buffered when another bus master is using the System Bus (e.g. DMA, other CPU). Refer to timing diagrams 4.3 and 6.3.
4. Read hit cycles can run while another System Bus master is using the System Bus.

The first case is established by providing the data which the i386™ SX Microprocessor requested first and later the 82396SX Smart Cache continues filling its line while it is servicing new read hit cycles. The 82396SX Smart Cache updates its cache and cache directory after completing the System Bus Line Fill cycle. Meanwhile, any i386™ SX Microprocessor read cycles will be serviced from the cache if they hit the cache. In case the i386™ SX Microprocessor read cycles are consecutive such that the i386™ SX Microprocessor is requesting a word which belongs to the same line currently retrieved by the System Bus Line Fill cycle and the requested word was already retrieved, the 82396SX Smart Cache provides the requested word in zero wait states (a Line Buffer hit). If the requested word wasn't already retrieved, it will be read after completing the Line Fill.

The second and third cases are attained by having the 4 word deep write buffer which is described in chapter 6. The READYO# is driven active after latching the write cycle, so all buffered cycles will run without wait states on the Local Bus. This releases the i386™ SX Microprocessor to issue a new cycle, which can also run without wait states if it does not require system bus service. Two examples are in the case of a read hit cycle, or another buffered write cycle, which does not require immediate System Bus service. In the case of a write cycle to the same line currently retrieved, the write cycle will wait until the Line Fill is complete and then the selected bytes within the line are written in the cache. READYO# is returned after the cache is written.

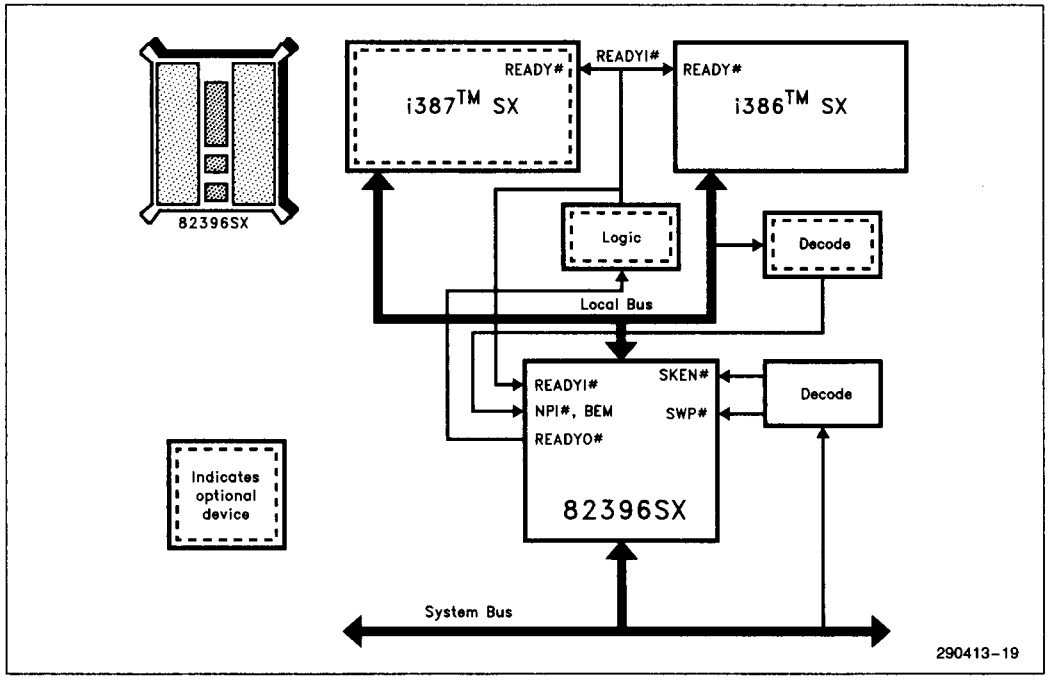


Figure 4.5 System Description

Whenever the System Bus is released to any bus master, the 82396SX Smart Cache activates the snooping function. The maximum rate of snooping cycles is a cycle every other clock. Although the snooping support requires accessing the 82396SX Smart Cache Directory, the 82396SX Smart Cache is able to interpose the cache directory accesses between the i386™ SX Microprocessor cycles and the snooping device such that zero wait state read hit cycles are supported. All the snooping cycles are also serviced. This is how the fourth case is provided. For more details, refer to Chapter 6.

4.4 Disabling the 82396SX Smart Cache

Cacheability is resolved by the SKEN# input from the system side. In order to disable the cache it is recommended to deactivate SKEN#, and assert FLUSH# (See Section 3.2.7.1). This would cause all memory reads to be detected as misses and to be transferred to the System Bus. In order to disable the write buffer, NPI# must be asserted.

5.0 PROCESSOR INTERFACE

The 82396SX Smart Cache runs synchronously with the i386™ SX Microprocessor. It is a slave on the Local Bus, and it buffers between the Local Bus and the System Bus. Most of the 82396SX Smart Cache cycles are serviced from the internal cache, and some (82396SX Smart Cache misses, non cacheable accesses, etc.) require an access to the System Bus to complete the transaction.

To achieve maximum performance, the 82396SX Smart Cache serves cache hits and buffered write cycles in zero wait-state, non- pipelined cycles. The 82396SX Smart Cache requires that the CPU is never driven to pipelined cycles, i.e. **the i386™ SX Microprocessor NA# input must be strapped to the inactive (high) state.**

The 82396SX Smart Cache is directly connected to all local bus address and data lines, byte enable lines, and bus cycle definition signals. The 82396SX Smart Cache returns READYO# to the i386™ SX Microprocessor, and keeps track of the i386™ SX Microprocessor cycle status by receiving READYI# (which is the i386™ SX Microprocessor READY#).

5.1 Hardware Interface

The 82396SX Smart Cache requires minimal hardware on the Local Bus. All that is needed is the i386™ SX Microprocessor and other Local Bus resources (i.e. i387™ SX Math Coprocessor) and the 82396SX Smart Cache. A decoder for generating NPI# (Non-Posted Input) and BEM (Byte Enable Mask) is optional. The SRAM and buffers have been integrated on chip to simplify the design. Refer to Figure 4.5.

5.2 Nonpipelined Local Bus

The 82396SX Smart Cache does not pipeline the Local Bus. READYO# gets returned to the i386™ SX Microprocessor one cycle after SRDY# or SBRDY# is driven into the 82396SX Smart Cache after the first word of a Line Fill. This allows the Local Bus to be free to execute i386™ SX Microprocessor cycles while the System Bus fills the cache line (see Chapter 6).This takes away the advantage gained by pipelining the Local Bus.

5.3 Local Bus Response to Hit Cycles

The 82396SX Smart Cache's Local Bus response to hit cycles are described here:

1) Cache Read Hit (CRDH) Cycle - READYO# gets returned in T2. The data is valid to the i386™ SX Microprocessor on the rising edge of CLK2.
2) Cache Write Hit (CWTH), Buffered - Like in CRDH cycles the 82396SX Smart Cache returns READYO# in T2 so that the cycle runs with zero wait states on the Local Bus. The write cycle is placed in the write buffer and will be performed when the System Bus is available. If the System Bus is on HOLD up to four write cycles can be buffered before introducing any wait states on the Local Bus.
3) CWTH, Non-Buffered - In the case of a non-buffered write hit cycle the write buffers can not be used so the i386™ SX Microprocessor must wait until the System Bus is free to do the write. READYO# is returned the cycle after SRDY# is driven to the 82396SX Smart Cache.

5.4 Local Bus Response to Miss Cycles

In a Cache Read Miss (CRDM) cycle a Line Fill is performed on the System Bus. READYO# is returned to the i386™ SX Microprocessor one cycle after SRDY# or SBRDY# for the first word of the Line Fill is driven into the 82396SX Smart Cache.

A Cache Write Miss (CWTM) cycle is forwarded to the System Bus consistent with the write buffer policy. The cache is not updated.

5.5 Local Bus Control Signals - ADS#, READYI#

ADS# and READYI# are the two bus control inputs used by the 82396SX Smart Cache to determine the status of the Local Bus cycle. ADS# denotes the beginning of a i386™ SX Microprocessor cycle and READYI# is the i386™ SX Microprocessor cycle terminator.

ADS# active and M/IO# = 1 invokes a look-up request to the 82396SX Smart Cache's cache directory; the look-up is performed in T1 state. The Cache Directory access is simultaneous with all other cycle qualification activities, this Way the hit/miss decision becomes the last in the cycle qualification process. This parallelism enhances performance, and enables the 82396SX Smart Cache to respond to ADS# within one clock period. If the cycle is non-cacheable, the hit/miss decision is ignored.

READYI# should not be driven active during T1 and should not be delayed from READYO# by one or more clocks.

5.6 82396SX Smart Cache's Response to the i386™ SX Microprocessor Cycles

Tables 5.2 - 5.4 show the 82396SX Smart Cache's response to the various i386™ SX Microprocessor cycles. They depict the activity in the internal cache, cache directory, the System Bus and write buffers in response to various cycle definition signals. Special cycles such as: LOCK, HALT/SHUTDOWN, WP, NPI are discussed separately below.

5.6.1 LOCKED CYCLES

The i386™ SX Microprocessor LOCK#ed cycles are all those cycles in which LOCK# is active. The 82396SX Smart Cache forces all LOCK#ed cycles to run on the System Bus. The 82396SX Smart Cache starts the LOCK#ed cycle after it has emptied its write buffers.

If the LOCK#ed cycle is cacheable the 82396SX Smart Cache will respond as follows (see Table 5.2):

Cache Read Miss (CRDM) - handled similar to a non cacheable cycle.

Cache Read Hit (CRDH) - handled similar to a non cacheable cycle (LRU bits are not updated).

Cache Write Miss (CWTM) - the cache is not updated, the write is not buffered.

Cache Write Hit (CWTH) - the cache is updated if the line is not write protected. The write is not buffered. Note that this write is not buffered even though it is cacheable. The LRU mechanism is updated.

If the LOCK#ed cycle is non-cacheable (e.g. IO cycle, INTA cycle) then it will be performed as a common non-cacheable cycle with the addition of asserting SLOCK# on the System Bus.

Conceptually, a LOCK# cycle on the Local Bus is reflected into an SLOCK# cycle on the System Bus. SLOCK# becomes inactive only after LOCK# has become inactive. If there are idle clocks in between the LOCK#ed cycles but LOCK# is still active - SLOCK# will remain active as well. **A consequence of this is that SLOCK# is negated one clock after LOCK# is negated.**

During LOCK#ed cycles on System Bus (i.e. when SLOCK# signal is active), the 82396SX Smart Cache does not acknowledge hold requests, so the whole sequence of LOCK#ed cycles will run without interruption by another master.

5.6.2 I/O, HALT/SHUTDOWN

I/O and HALT/SHUTDOWN cycles are handled as non-cacheable cycles. They are neither cached nor kept in the write buffer. The i386™ SX Microprocessor HALT/SHUTDOWN cycles are memory write cycles to code area (i.e. M/IO# = 1, D/C# = 0). The 82396SX Smart Cache completes I/O and HALT/SHUTDOWN cycles by returning READYO#, after receiving the SBRDY# or SRDY#.

5.6.3 NPI# CYCLES

NPI# cycles are all the i386™ SX Microprocessor memory write cycles in which NPI# is active. In response to a write cycle with NPI# active, the 82396SX Smart Cache first executes all pending write cycles in the write buffer (if any), and than executes the current write cycle on the System Bus. READYO# is returned to the CPU only after SRDY# for the current write cycle is returned to the 82396SX Smart Cache.

All NPI# cycles must have at least one wait state on the System Bus or be done to non-cacheable memory. NPI# is ignored for read cycles, as well as all write cycles that cannot be buffered.

5.6.4 NPI#/BEM TIMING

These inputs must be valid throughout the i386™ SX Microprocessor bus cycle, namely in T1 and all T2 states (See Figure 5.1).

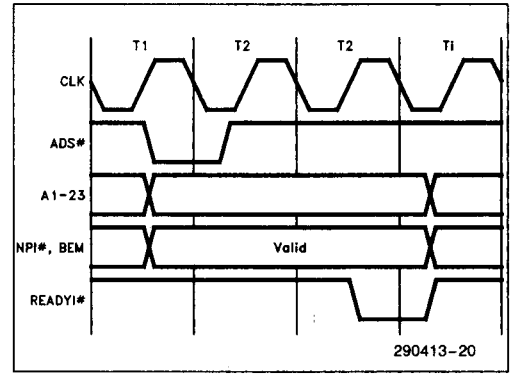


Figure 5.1 Valid Time of NPI# and BEM

5.7 82396SX Smart Cache READYO# Generation

The 82396SX Smart Cache READYO# generation rules are listed below:

CRDH cycles (non-LOCK#ed), READYO# is activated during the first T2 state, so the cycle runs with zero wait states.

CRDM cycles - READYO# is returned one clock after the first SRDY# or SBRDY# associated with this read cycle is returned.

Non cacheable reads - READYO# is returned one clock after SRDY# or SBRDY#.

All cacheable writes (with the exception of LOCK#ed writes) are buffered. These cycles may be divided into two categories:

(a) The first four write cycles - while the write buffer is not fully exploited. READYO# is returned with zero wait states. The address and the data are registered in the write buffer.

(b) When the write buffer is full - READYO# is delayed until one clock after the SRDY# or SBRDY# of the first write cycle in the buffer. In other words the fifth write waits until there is one vacant entry in the write buffer.

Non cacheable writes (plus LOCK#ed writes) - these writes are not buffered. READYO# is returned one clock after SRDY# or SBRDY# of the same cycle.

READYO# activation during SRAM test mode are listed in Chapter 7.

In all i387™ SX Math Coprocessor accesses, the 82396SX Smart Cache monitors the READYI#. If it wasn't activated immediately after ADS#, READYO# will be activated in the next clock i.e. a one wait state cycle. So, the 82396SX Smart Cache READYO# can be used to terminate any i387™ SX Math Coprocessor access.

Note that the timing of the 82396SX Smart Cache's READYO# generation for i387™ SX Math Coprocessor cycles is incompatible with 80287 timing. When activated, READYO# remains active until READYI# is sampled active. This procedure enables adding control logic to control the i386™ SX Microprocessor READYI# generation (see figure 5.2).

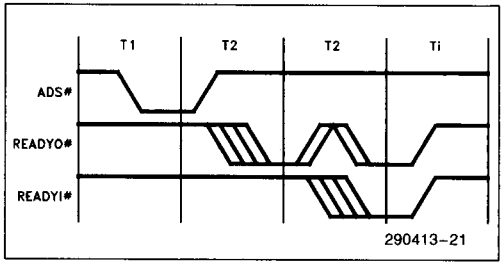


Figure 5.2 Externally Delayed READY

5.8 A20 Mask Signal

The A20M# signal is provided to allow for emulation of the address wraparound at 1 Mbyte which occurs on the 8086. A20M# pin is synchronized internally by the 82396SX Smart Cache, then ANDed with the A20 input pin. The product of synchronized A20M# and A20 is presented to the rest of the 82396SX Smart Cache logic, as shown in Figure 5.3. A20M# must be valid two clock cycles before ADS# is sampled active by the 82396SX Smart Cache, and must remain valid until after READYI# is sampled active (see Figure 5.4).

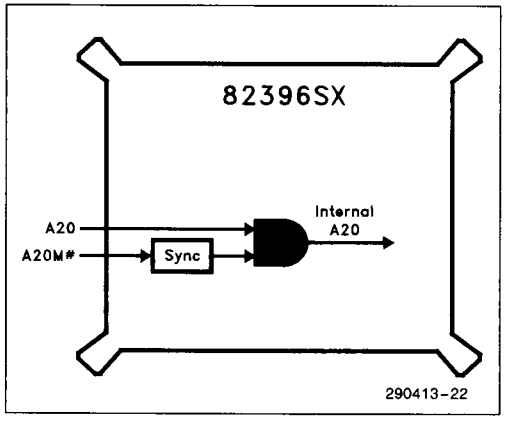


Figure 5.3 A20 Mask Logic

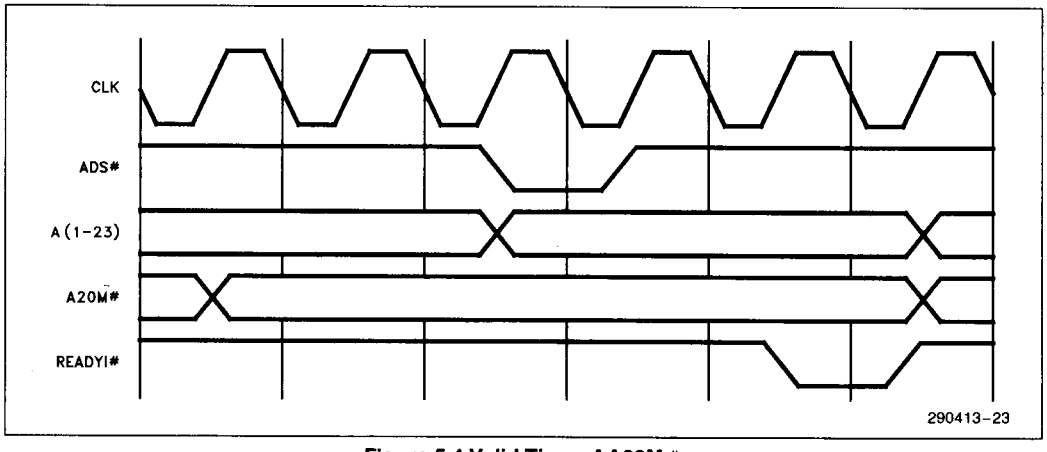


Figure 5.4 Valid Time of A20M#

5.9 82396SX Smart Cache Cycle Overview

Table 5.2 describes the activity in the cache, in the Tagram, on the System Bus and in the write buffers. The cycles are defined in table 5.1. Table 5.2 is sorted in a descending order. The more dominant the attribute the higher it is located. Table 5.2 is for non test modes.

Table 5.1 i386™ SX Microprocessor Bus Cycle Definition

M/IO#	D/C#	W/R#	i386™ SX Microprocessor Cycle Definition
0	0	0	Interrupt Acknowledge
0	0	1	Undefined
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Memory Code Read
1	0	1	Halt/Shutdown
1	1	0	Memory Data Read
1	1	1	Memory Data Write

Table 5.2 Activity by Functional Groupings

Cycle Type	WP	Cache	TAGRAM		System Bus	Posted Write	Comm.
			LRU	TAG			
1. 387 Cycles	N/A	-	-	-	-	N/A	
2. I/O Write, I/O Read, Halt/Shutdown, INTA, LOCK#ed Read	N/A	-	-	-	Non Cacheable Cycle	No	2
3. LOCK#ed Write Hit	YES		Update	-	Memory Write	No	2
4. LOCK#ed Write Hit	NO	Cache Write	Update	-	Memory Write	No	2
5. LOCK#ed Write Miss	N/A	-	-	-	Memory Write	No	2
6. Other Read Hit	N/A	Cache Read	Update	-	-	N/A	1
7. Other Read Miss SKEN# Active	N/A	Cache Write	Update	Update	Line Fill	N/A	2
8. Other Read Miss SKEN# Inactive	N/A	-	-	-	Noncacheable Read No Line Fill	N/A	2
9. Other Write Hit NPI# Inactive	Yes	-	Update	-	Memory Write	Yes	1
10. Other Write Hit NPI# Active	Yes	-	Update	-	Memory Write	No	2
11. Other Write Hit NPI# Inactive	No	Cache Write	Update	-	Memory Write	Yes	1
12. Other Write Hit NPI# Active	No	Cache Write	Update	-	Memory Write	No	2
13. Other Write Miss NPI# Inactive	N/A	-	-	-	Memory Write	Yes	1
14. Other Write Miss NPI# Active	N/A	-	-	-	Memory Write	No	2

5

Table 5.3 describes line buffer hit cycles. Hit/miss here means to the specific word in the line buffer.

Table 5.3

Cycle Type	WP	Cache	TAGRAM		System Bus	Posted Write	Comm.
			LRU	TAG			
15. LOCK#ed Write	Yes	-	-	-	Memory Write	No	2
16. LOCK#ed Write	No	Cache Write	-	-	Memory Write	No	4
17. Read Hit	N/A	LB Read	-	-	-	N/A	1
18. Read Miss	N/A	LB Read	-	-	-	N/A	3
19. Other Write NPI# Inactive	Yes	-	-	-	Memory Write	Yes	6
20. Other Write NPI# Active	Yes	-	-	-	Memory Write	No	2
21. Other Write NPI# Inactive	No	Cache Write	-	-	Memory Write	Yes	5
22. Other Write NPI# Active	No	Cache	-	-	Memory Write	No	4

Table 5.4 describes the line buffer hit cycles, when the Line Fill is interrupted (by: FLUSH#, snoop hit to the line buffer or interrupted burst, even if the Line Fill continues on the System Bus in the first two cases). The table includes only the cycles which wait to the end of the Line Fill or to the CPU cache update. Hit/miss here means to the specific word in the line buffer.

Table 5.4

Cycle Type	WP	Cache	TAGRAM		System Bus	Posted Write	Comm.
			LRU	TAG			
23. LOCK#ed Write	N/A	-	-	-	Memory Write	No	2
24. Read Miss (Restart)	N/A	Cache Write	Update	Replace	Line Fill	N/A	2
25. Other Write NPI# Inactive	N/A	-	-	-	Memory Write	Yes	5
26. Other Write NPI# Active	N/A	-	-	-	Memory Write	No	2

Table 5.5 depicts the 82396SX Smart Cache Test Cycles.

Table 5.5

Cycle Type	WP	A16	Cache	TAGRAM		System Bus	Posted Write	Comm.
				LRU	TAG			
27. High Impedance	N/A	N/A	-	-	-	-	N/A	
28. SRAM Mode Read Add 256K–512K	N/A	0	-	LRU RD	TAG RD	-	N/A	
29. SRAM Mode Read Add 256K–512K	N/A	1	Cache Read	-	-	-	N/A	
30. SRAM Mode Write Add 256K–512K	N/A	0	-	LRU WR	TAG WR	-	N/A	
31. SRAM Mode Write Add 256K–512K	N/A	1	Cache Write	-	-	-	N/A	
32. SRAM Mode Read Add < > 256K–512K	N/A	N/A	-	-	-	Noncacheable Cycle	No	2
33. SRAM Mode Write Add < > 256K–512K	N/A	N/A	-	-	-	Noncacheable Cycle	N/A	

Remarks for Tables 5-2 through 5-5:
1. READYO# is active in the first T2. (In read cycles, in write it depends if the write buffer is full).
2. READYO# is active one clock cycle after SRDY#/SBRDY# of this cycle is asserted. In case of Line Fill, READYO# is active one clock cycle after first SRDY#/SBRDY# of this cycle is asserted.
3. READYO# is active immediately after the current line fill is finished.
4. READYO# is active after the previous line fill and the write cycle are terminated by SRDY# or SBRDY#, and the cache is updated.
5. READYO# is active after the cache is updated for the previous Line Fill, or after the Line Fill is aborted.
6. READYO# is active on the third T2 (2 wait states) if the write buffer is not full.
7. "OTHER" means the cycle does not fall within the first five categories.

5

6.0 SYSTEM BUS INTERFACE

The System Bus (SB) interface is similar to the i386™ SX Microprocessor interface. It runs synchronously to the i386™ SX Microprocessor clock. In general, the interface is similar to the 82385SX in terms of: System Bus pipelining, snooping support, multi master arbitration support and write cycle buffering. In addition, the following enhancements are provided:

1) Line Fill buffer.
2) Optional burst Line Fill.
3) System cacheability attribute, SKEN#.
4) System Write Protection attribute, SWP#.
5) The SEADS# snooping mechanism to support concurrency on the System Bus and on the general purpose bus.
6) Four word write buffer (8 bytes).

The 82396SX Smart Cache System Bus interface has identical bus signals to the i386™ SX Microprocessor bus. It has the bus control signals (SADS#, SRDY# and SNA#), the cycle definition signals (SLOCK#, SW/R#, SD/C# and SM/IO#), the address and byte enable signals (SA[23:1], SBHE# and SBLE#) and the data signals (SD[15:0]). In addition, the 82396SX Smart Cache has the SBRDY# signal for burst support. The SKEN# signal is used for identifying system cacheability. The SWP# signal is used for identifying system write protection. The SEADS# signal is used for snooping support. The SHOLD and SHLDA signals are used for system arbitration. Also, the 82396SX Smart Cache provides a signal, SBLAST#, which when asserted, indicates that the current cycle is the last cycle in a burst transfer.

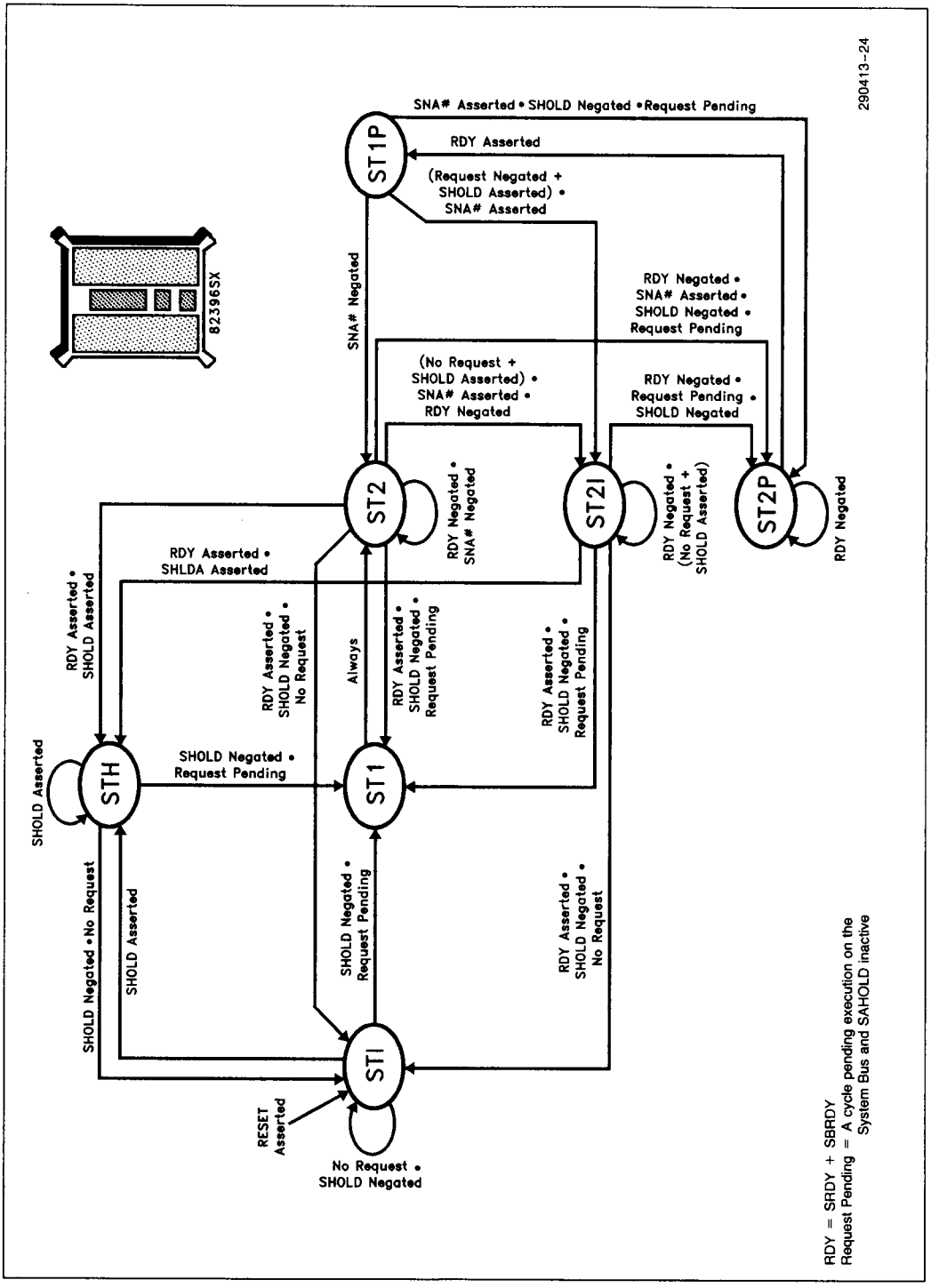


Figure 6.1 SB State Machine

The 82396SX Smart Cache System Bus interface can support any device, non cacheable, I/O or cacheable memory with any number of wait states (zero wait state non-posted writes are not allowed). The 82396SX Smart Cache is able to support one clock burst cycles. The 82396SX Smart Cache's System Bus state machine is similar to the i386™ SX Microprocessor bus state machine (refer to the "i386™ SX Microprocessor data sheet"). Note that during burst Line Fill, the 82396SX Smart Cache remains in ST2 state until SRDY# or SBRDY# is asserted for the eighth cycle of the burst transfer. Figure 6.1 describes the 82396SX's System Bus state machine.

6.1 System Bus Cycle Types

Following five types of SB cycles are supported:

1) Buffered write cycle
2) Non buffered write cycle
3) Buffered / non-buffered write protected cycles.
4) Non cacheable read cycle
5) Cacheable read cycle

6.1.1 BUFFERED WRITE CYCLE

All the cacheable write cycles, except LOCK#ed write cycles or non-buffered write cycles (as indicated by NPI# pin sampled active), are buffered. These cycles are terminated on the Local Bus before they are terminated on the System Bus.

Figures 6.2–6.3 include waveforms of several cases of buffered write cycles:

The 82396SX Smart Cache has a four word deep write buffer but 5 writes cycles can be buffered if one of the buffered writes is being executed.

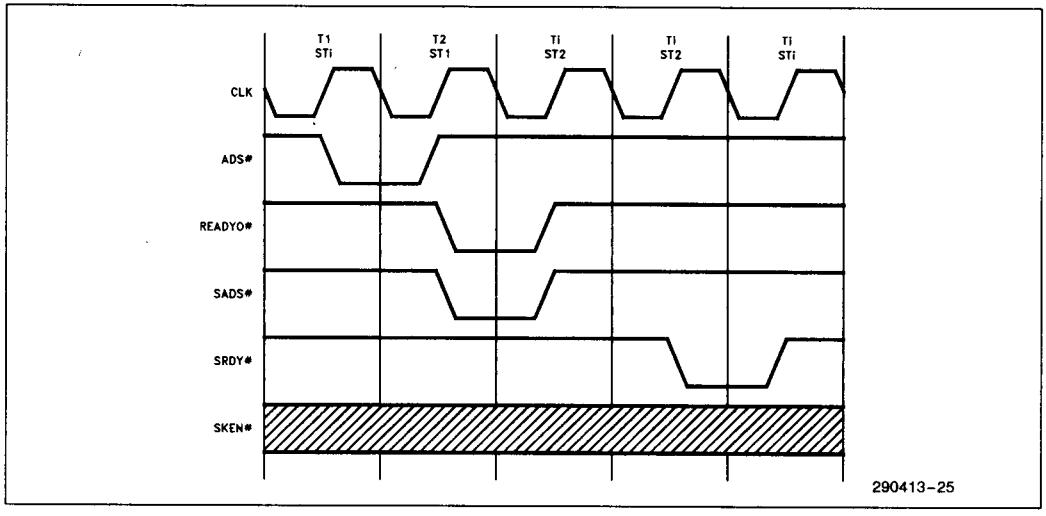
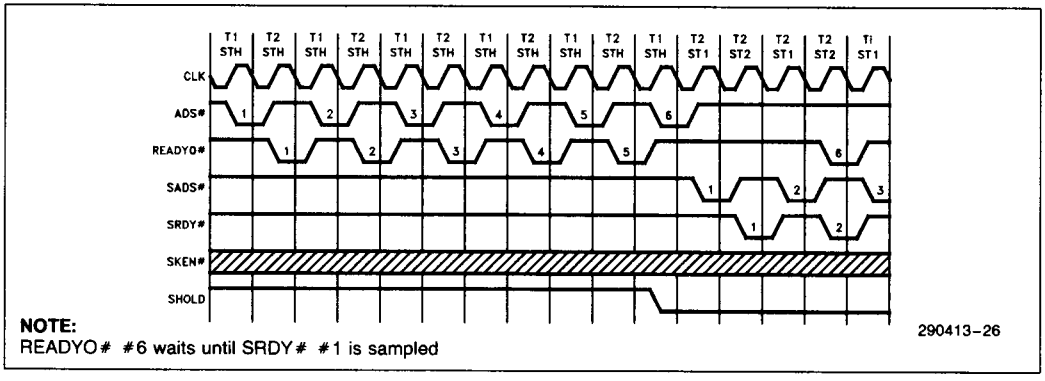


Figure 6.2 Single Buffered Write Cycle



NOTE:
READYO# #6 waits until SRDY# #1 is sampled

Figure 6.3 Multiple Buffered Write Cycles During System Bus HOLD

6.1.2 NON-BUFFERED WRITE CYCLE

These cycles are terminated on the System Bus one clock before they are terminated on the Local Bus. The following Figures (6.4 - 6.5) include waveforms of several cases of non buffered write cycles.

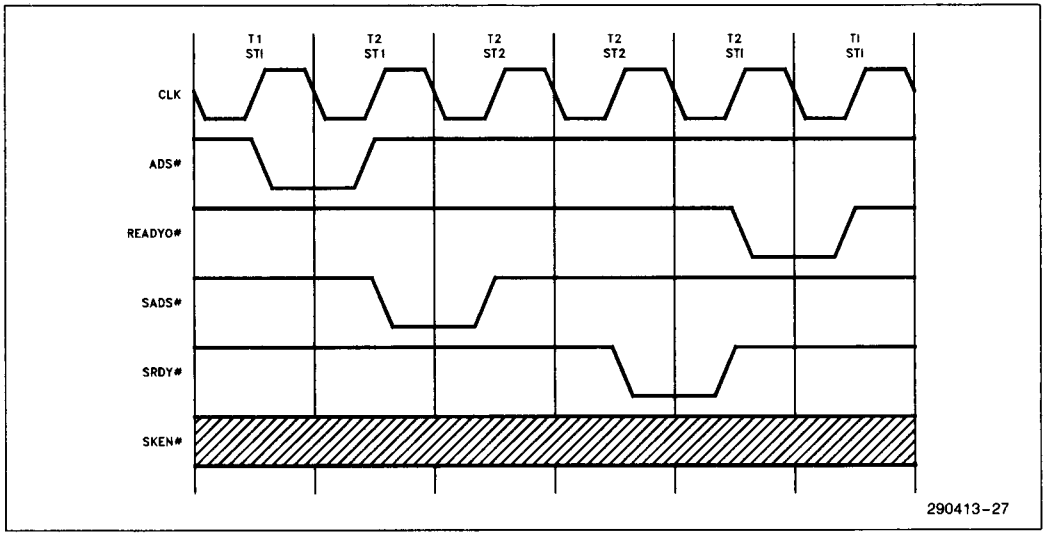
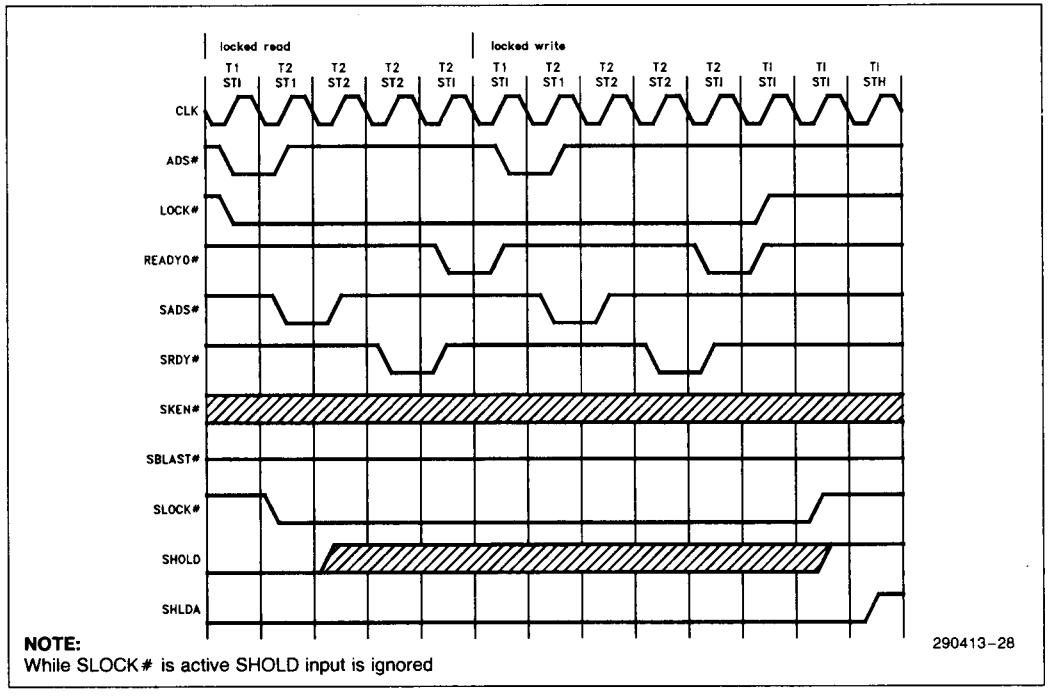


Figure 6.4 I/O Write Cycle



NOTE:
While SLOCK# is active SHOLD input is ignored

Figure 6.5 LOCKed "Read Modify Write" Cycle

6.1.3 WRITE PROTECTED CYCLES

The Write Protection attribute is provided by the System Bus SWP# input. The SWP# is sampled in every Line Fill cycle. The write protection bit in the Cache Directory is set accordingly, together with the TAG address and TAG Valid bit of every line. In every cacheable write cycle, the write protection indicator is read simultaneously with the Hit/Miss decision. If the write cycle is a hit and the write protection bit is set, the cache will not be updated. In all other cases, the write protection bit is ignored.

6.1.4 NON-CACHEABLE READ CYCLE

Non cacheable read cycles are terminated on the System Bus one clock before they are terminated on the Local Bus. The following Figures (6.6–6.7) include waveforms of several cases of non-cacheable read cycles.

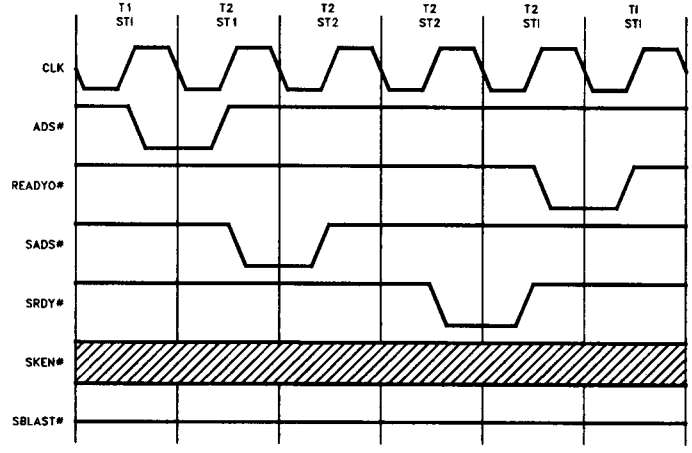
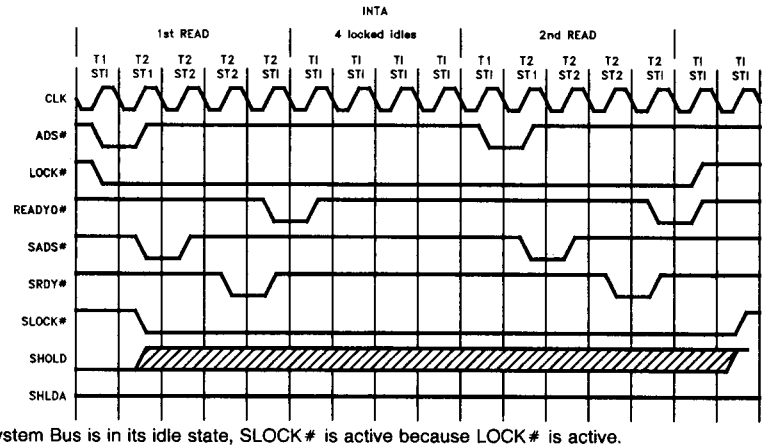


Figure 6.6 I/O Read Cycle (non-cacheable read cycle)



Even if the System Bus is in its idle state, SLOCK# is active because LOCK# is active.

NOTE:
While SLOCK# is active SHOLD input is ignored

Figure 6.7 INTA LOCKed Cycle (non-cacheable read cycle)

6.1.5 CACHEABLE READ MISS CYCLES

The 82396SX Smart Cache attempts to start a Line Fill for non LOCK#ed CRDM cycles. However, a Line Fill will be converted into a single read cycle if the access is indicated as non-cacheable by the SKEN# signal.

CRDM cycles start as a System Bus read cycle. READYO# is returned to the i386™ SX Microprocessor one clock cycle after System Bus read cycle is terminated.

One CLK cycle before the first SNA#, SRDY# or SBRDY# of the system read cycle the SKEN# input is sampled. If active, the read miss cycle continues as a Line Fill cycle, and seven additional words are read from the memory into the 82396SX Smart Cache. Also, the SWP# input will be sampled with the first SNA#, SRDY# or SBRDY# so the WP flag of the line will be updated in the Cache Directory.

6.1.5.1 Aborted Line Fill (ALF) Cycles

The System Bus can respond that the area of memory included in a particular request is non-cacheable, by returning SKEN# inactive. As soon as the 82396SX Smart Cache samples SKEN# inactive, it converts the cycle from a cache Line Fill, which requires seven additional read cycles to be completed, to a single cycle.

In this case SBLAST# will stay active. Also, the 82396SX Smart Cache will not generate another system cycle for the same Line Fill, because the cycle has already been finished by the first SBRDY# or SRDY# after SKEN# was sampled inactive.

Figure 6.8 includes waveforms of an ALF cycle.

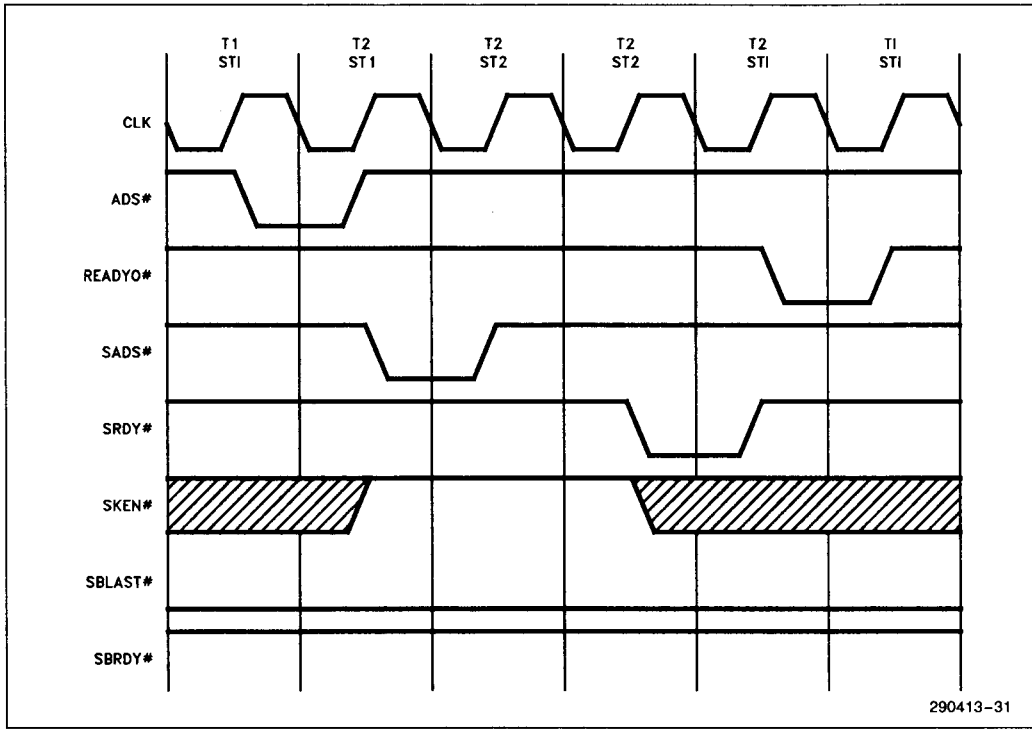


Figure 6.8 Aborted Line Fill Cycle

6.1.5.2 Line Fill Cycles

A Line Fill transfer consists of eight back to back read cycles. Three types of Line Fill cycles are supported:

1. Non pipeline, Non burst, SNA# inactive.
2. Pipelined, non burst, SNA# active.
3. Burst, non pipelined, SNA# inactive, SRDY# inactive, SBRDY# active.

Note that a pipelined burst cycle is not supported. When SNA# is sampled active, SBRDY# is treated as SRDY#.

The 82396SX Smart Cache supports burst cycles in system Line Fills only. Burst cycles are designed to allow fast line fills by allowing consecutive read cycles to be executed at a rate of one word per clock cycle. In burst cycles SADS# is pulsed for one clock cycle while the address and control lines are valid until the transfer is completed. SA1–3 are updated every bus cycle during the burst transfer.

The 82396SX Smart Cache starts the Line Fill as a normal read cycle, and waits for SBRDY# or SRDY# to be returned active. If SNA# is sampled active at least one clock cycle before either SBRDY# or SRDY#, the Line Fill will be non burst pipelined (see Figure 6.10). If SNA# is sampled active at the same clock cycle as SBRDY# or SRDY#, the line fill will be non-burst, non-pipelined.

If BEM is asserted during cacheable read cycles and that cycles requires a Line Fill (cache read miss), then both bytes will be accessed during the first cycle of the Line Fill. If BEM is not used (tied low), the system must return valid data for both bytes on the first access of a Line Fill, because SBHE# and SBLE# will be the same as BHE# and BLE# during the first access of a Line Fill and are not always active. System bus byte enables are driven active in the remaining cycles of the Line Fill (irrespective of the state of BEM).

If SKEN# is sampled inactive one clock before either SNA#, SBRDY# or SRDY#, then the access is considered non- cacheable and a Line Fill will not be executed (see Figure 6.8). Otherwise, if SRDY# is sampled active, the line fill cycle resumes as a non-burst sequence of seven more cycles (see Figure 6.9). Finally, if SBRDY# and SKEN# are sampled active (and SNA# and SRDY# are sampled inactive), then the Line Fill cycle will be a burst cycle (see Figures 6.11 - 6.12). If a system cannot support burst cycles, a non burst line fill must be requested by merely returning SRDY# instead of SBRDY#, in the first read cycle (see Figure 6.9). Once a burst cycle has started, it will not be aborted until it's completed, regardless if SKEN# is sampled inactive or SHOLD is sampled active, i.e. all eight words will be read from memory. However, the system may abort a burst Line Fill transfer before it's completed, by returning SRDY# active (instead of SBRDY#) for the second through the seventh word in a Line Fill transaction (see Figure 6.13). In this case the cache will not be updated. The first word will already have been transferred to the CPU.

Note that in the last (eighth) bus cycle in a Line Fill transfer, SBRDY# or SRDY# has the same effect on the 82396SX Smart Cache. That is to indicate the end of the Line Fill. For all cycles that cannot run in burst mode (non-Line Fill cycles or pipelined Line Fill cycles) SBRDY# has the same effect on the 82396SX Smart Cache as the normal SRDY# pin. SRDY# and SBRDY# are the same apart from their function during burst cycles.

The fastest burst cycle possible requires two clocks for the first data item to be returned to the 82396SX Smart Cache with subsequent data items returned every clock. Such a bus cycle is shown in Figure 6.11. An example of a burst cycle where two clocks are required for every burst item is shown in Figure 6.12. When initiating any read, the 82396SX Smart Cache presents the address for the data item requested. When the 82396SX Smart Cache converts this cycle into a cache Line Fill, the first data item returned must correspond to the address sent out by the 82396SX Smart Cache. This address is the original address that is requested by the i386™ SX Microprocessor. The 82396SX Smart Cache updates this address after each SBRDY# according to table 6.1 (SA1, SA2 and SA3 are updated). This is also true for non-burst Line Fill cycles. The 82396SX Smart Cache presents each request for data in an order determined by the first address in the transfer. For example, if the first address was 102, the next seven addresses in the burst will be 100, 106, 104, 10A, 108, 10E and 10C. The burst order used by the 82396SX Smart Cache is shown in Table 6.1. This remains true whether the external system responds with a sequence of normal bus cycles or with a burst cycle. An example of the sequencing of burst addresses is shown in Figure 6.12.

In the following cases, a Line Fill cycle will not update the cache:

1. Aborted burst: A burst cycle will be aborted if SRDY# is returned active in the second through the seventh bus cycle. The Line Fill will not resume, and the cache will not be updated.
2. Snoop hit to line buffer:

   If, during a Line Fill transfer, a snoop cycle is initiated after the first SRDY# or SBRDY#, and the address matches the address of the line being retrieved, the Line Fill cycle will continue as usual but the cache will not be updated.
3. FLUSH during Line Fill cycle: the Line Fill cycle will continue as usual, but the cache will not be updated.

Figures 6.9 - 6.13 include waveforms of several cases of Line Fill cycles.

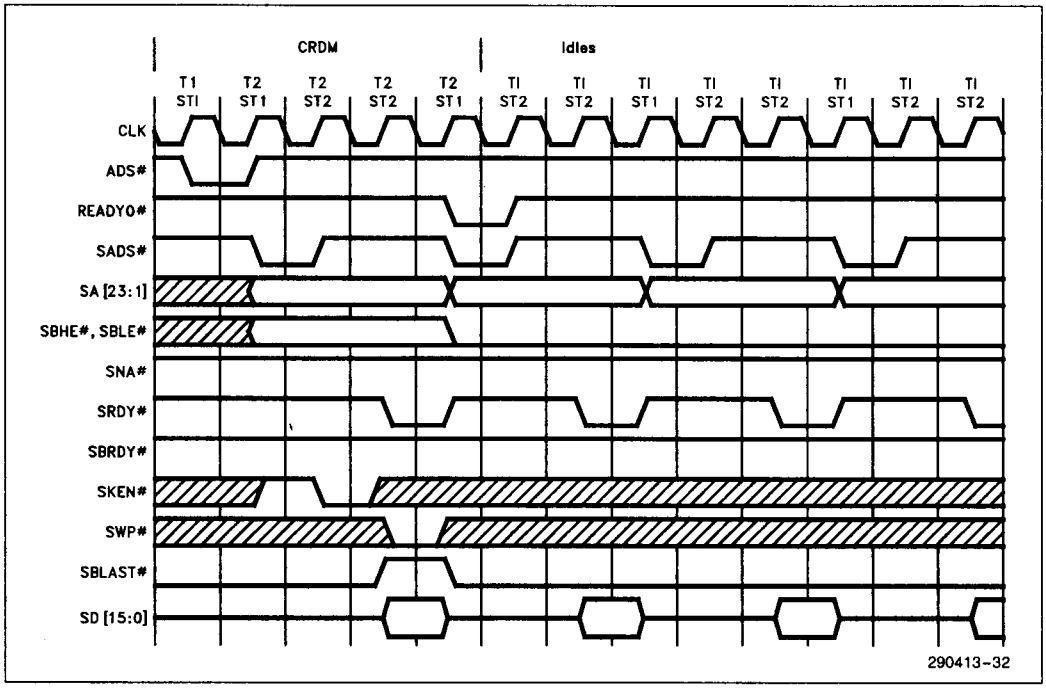


Figure 6.9 Line Fill without Burst or Pipeline (One Wait State—First Four Cycles Shown)

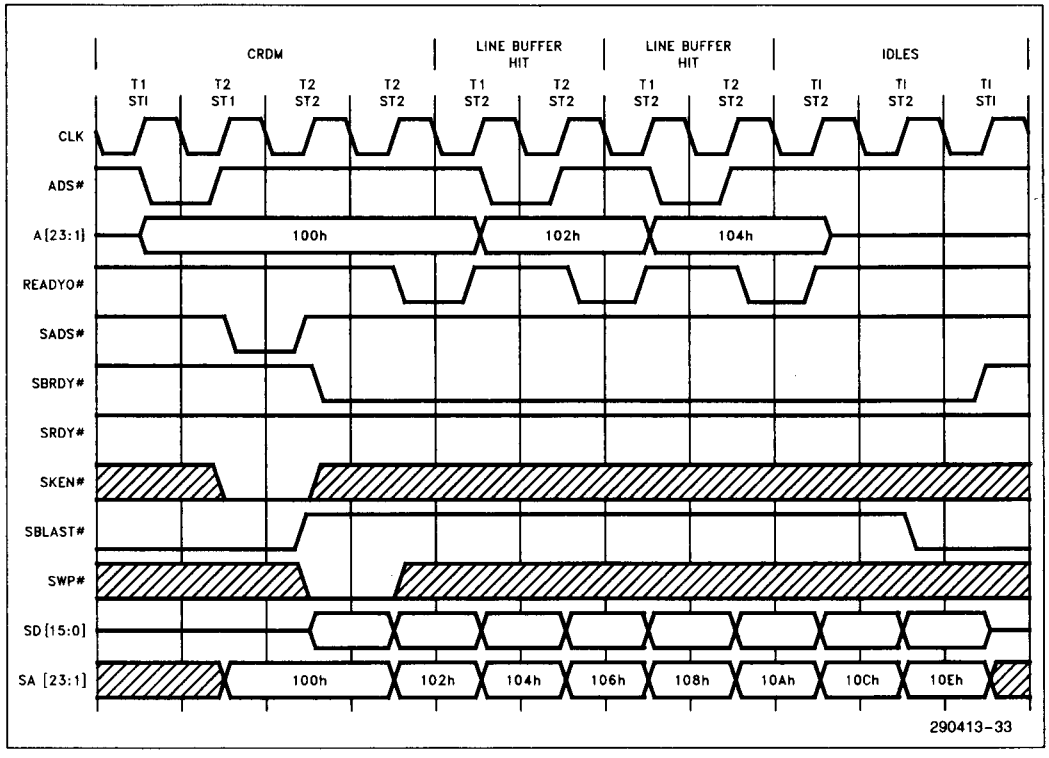


Figure 6.9A Burst Mode Line Fill Followed by Line Buffer Hit Cycles

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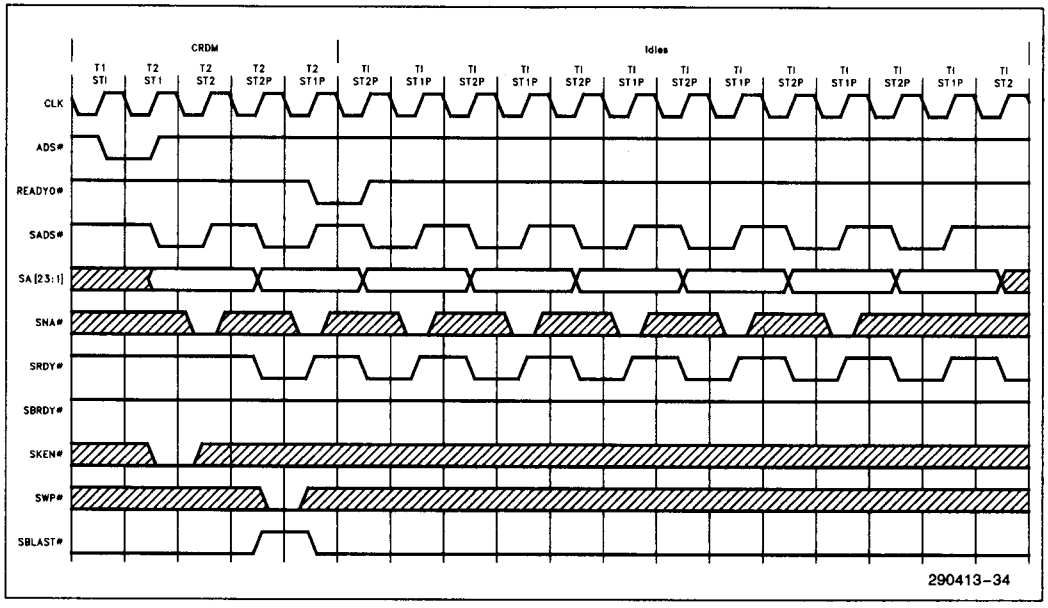

Figure 6.10 Pipelined Line Fill

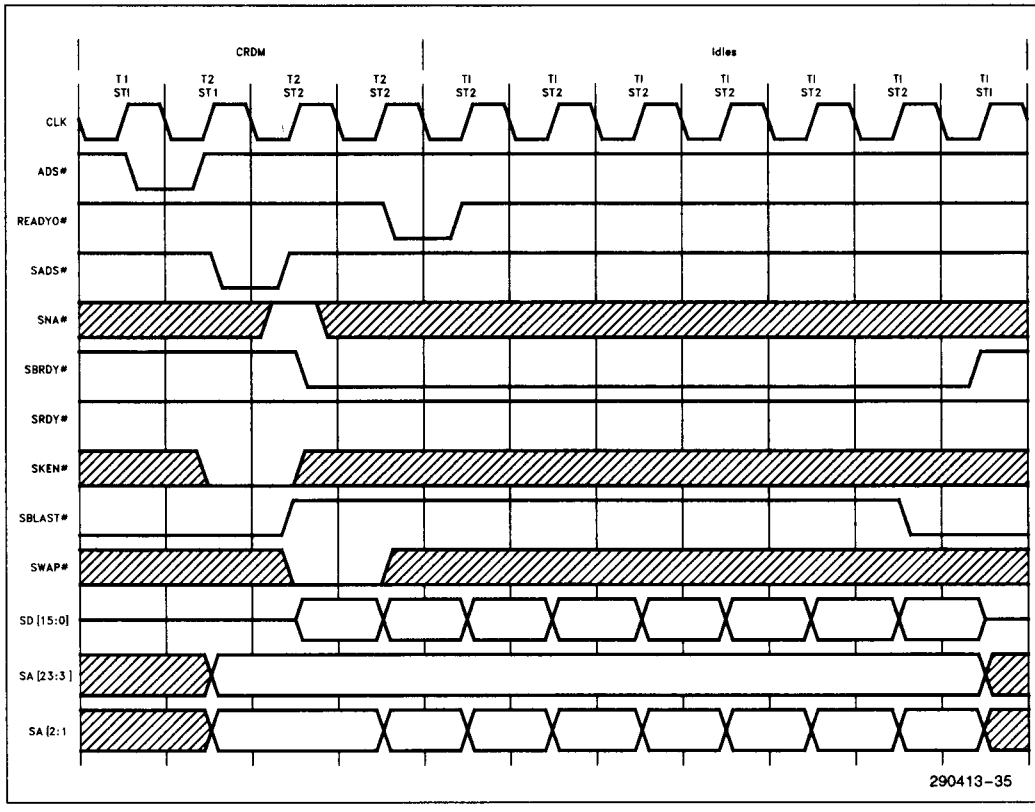

Figure 6.11 Fastest Burst Cycle (One Clock Burst)

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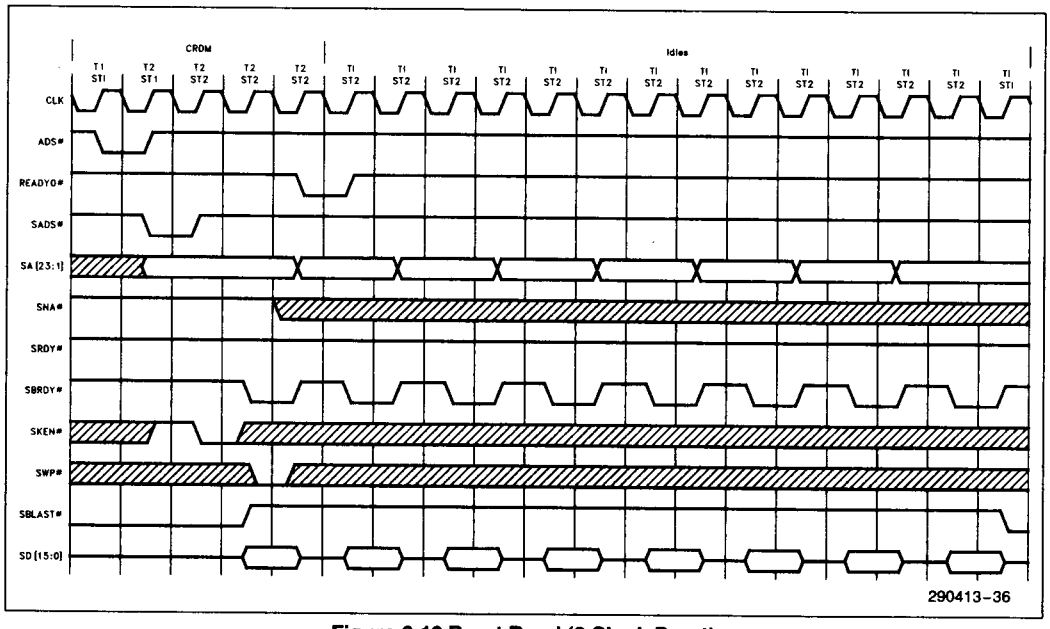

Figure 6.12 Burst Read (2 Clock Burst)

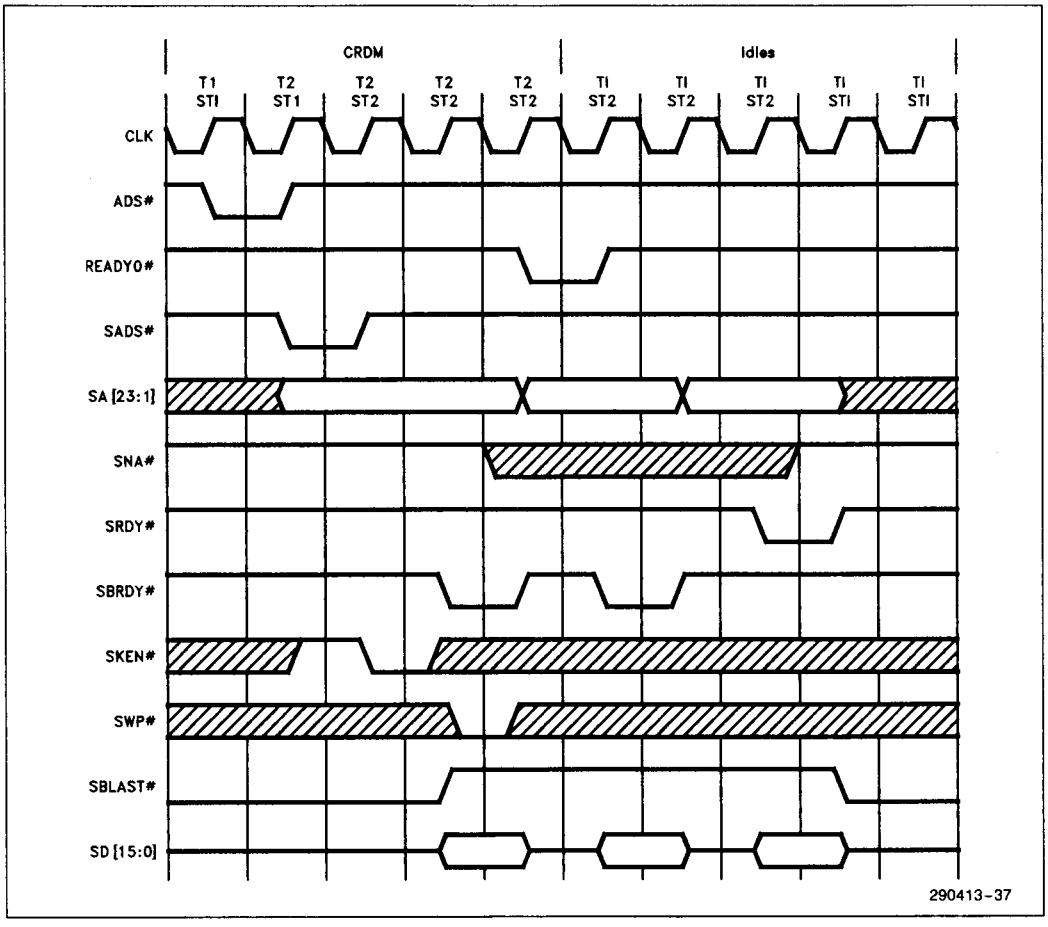

Figure 6.13 Interrupted Burst Read (2 Clock Burst)

Table 6.1 Line Fill Address Order

82396SX Smart Cache Line Fill Order (SA[3:1])							
Word within Line Fill							
1st	2nd	3rd	4th	5th	6th	7th	8th
0	2	4	6	8	A	C	E
2	0	6	4	A	8	E	C
4	6	0	2	C	E	8	A
6	4	2	0	E	C	A	8
8	A	C	E	0	2	4	6
A	8	E	C	2	0	6	4
C	E	8	A	4	6	0	2
E	C	A	8	6	4	2	0

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6.2 82396SX Smart Cache Latency In System Bus Accesses

The 82396SX Smart Cache acts as a buffer between the i386™ SX Microprocessor and the main memory causing some latency in initiating the System Bus cycle (SADS# delay from ADS#) and in completing the cycle (386 READYO# delay from SRDY# or SBRDY#). The 82396SX Smart Cache drives the SADS# one clock after the ADS#. In cacheable cycles, the 82396SX Smart Cache starts driving the SADS# before it decides whether the cycle is a cache hit or miss since the hit/miss decision is valid in the second clock (the first T2 cycle). In case the cycle is a hit, the 82396SX Smart Cache deactivates SADS#. This causes a glitch on the SADS# signal. For proper system functionality, SADS# must be sampled by the next clock edge. This signal will be stable by its maximum specification in all cycles.

At the end of a System Bus non-cacheable read cycle, or non- buffered write cycle, the 82396SX Smart Cache drives READYO# active one clock after SRDY# or SBRDY#. In a Line Fill cycle, READYO# is activated one clock after the first SBRDY# or SRDY# is sampled active. The setup timing requirements of SRDY# and system data force one wait state at the end of the cycle.

6.3 SHLDA Latency

For non-LOCK#ed cycles the worst case delay between SHOLD and SHLDA would be when SHOLD is activated during ST2P state, followed by a Line Fill. In this case, the HOLD request will be acknowledged only after the Line Fill is completed. In LOCKed cycles SHLDA will not be asserted until after SLOCK# is negated. The latency would be:

Latency = (Number of ST2P cycles) + (Number of Line Fill cycles) OR (Number of LOCK#ed cycles)

6.4 Cache Consistency Support

The 82396SX Smart Cache supports snooping using the SEADS# mechanism. Besides insuring the consistency, this mechanism provides multi processing support by having the 82396SX Smart Cache System Bus and the Local Bus running concurrently. SEADS# must be synchronized to CLK2 for proper operation.

The 82396SX Smart Cache will always float its address bus in the clock immediately following the one in which SAHOLD is received. Thus, no address hold acknowledge is required. When the address bus is floated, the rest of the 82396SX Smart Cache's System Bus will remain active, so that data can be received from a bus cycle that was already underway. Another bus cycle will not begin, and the SADS# signal will not be generated. However, multiple data transfers for burst cycles can occur during address holds.

SEADS# indicates that an external address is actually valid on the address inputs of the 82396SX Smart Cache. When this signal is activated, the 82396SX Smart Cache will read the external address and perform an internal cache invalidation cycle to the address indicated. The internal invalidation cycle occurs one clock after SEADS# is sampled active. In case of contention with i386™ SX Microprocessor look up, the invalidation is serviced two clocks after SEADS# was activated. The maximum rate of invalidation cycles is one every other clock. Multiple cache invalidations can occur in a single address hold transfer. SEADS# is not masked by SAHOLD inactive, so cache invalidations can occur during a normal bus cycle. Activate SEADS# only when SAHOLD or SHLDA are active.

If the 82396SX Smart Cache is running a line fill cycle and an invalidation is driven into the 82396SX Smart Cache in the same clock the first data is returned, or in any subsequent clock, the 82396SX Smart Cache will invalidate that line even if it is the same cache line that the 82396SX Smart Cache is currently filling.

SAHOLD in pipelined cycles: The activation of SAHOLD only causes the system address to be floated in the next clock without changing the behavior of pipelined cycles. If SAHOLD is activated before entering the ST2P state, the 82396SX Smart Cache will move into non-pipeline and drive the SADS# only after the deactivation of SAHOLD. However, if SAHOLD is asserted in the ST2P state and the Nth cycle has already started, the system address is floated but SADS# is kept active until SRDY# (for the N-1 th cycle) is returned. It is the system responsibility to latch the address bus. Note that the address driven on the System Bus after SAHOLD is deasserted (in pipelined cycles) depends on whether SNA# has been sampled active during the SAHOLD state and another cycle is pending. As seen

from Figure 6.14, the (N + 1)th address will be driven by the 82396SX Smart Cache once SAHOLD was deactivated and SNA# was sampled active, provided there is a cycle pending in the 82396SX Smart Cache. The following figures describe the 82396SX Smart Cache behavior in two cases. First, when SNA# is sampled active and second, in the case of SNA# sampled inactive.

Note that the maximum rate of snooping cycles is every other clock. The first clock edge in which SEADS# is sampled active causes the 82396SX Smart Cache to latch the system address bus and initiate a cache invalidation cycle. If SEADS# is driven active for more than one clock, only one snooping cycle will be initiated on the first clock edge at which SEADS# is sampled active. The SA[23:1] setup and hold timings are specified to the same clock edge in which SEADS# is sampled active.

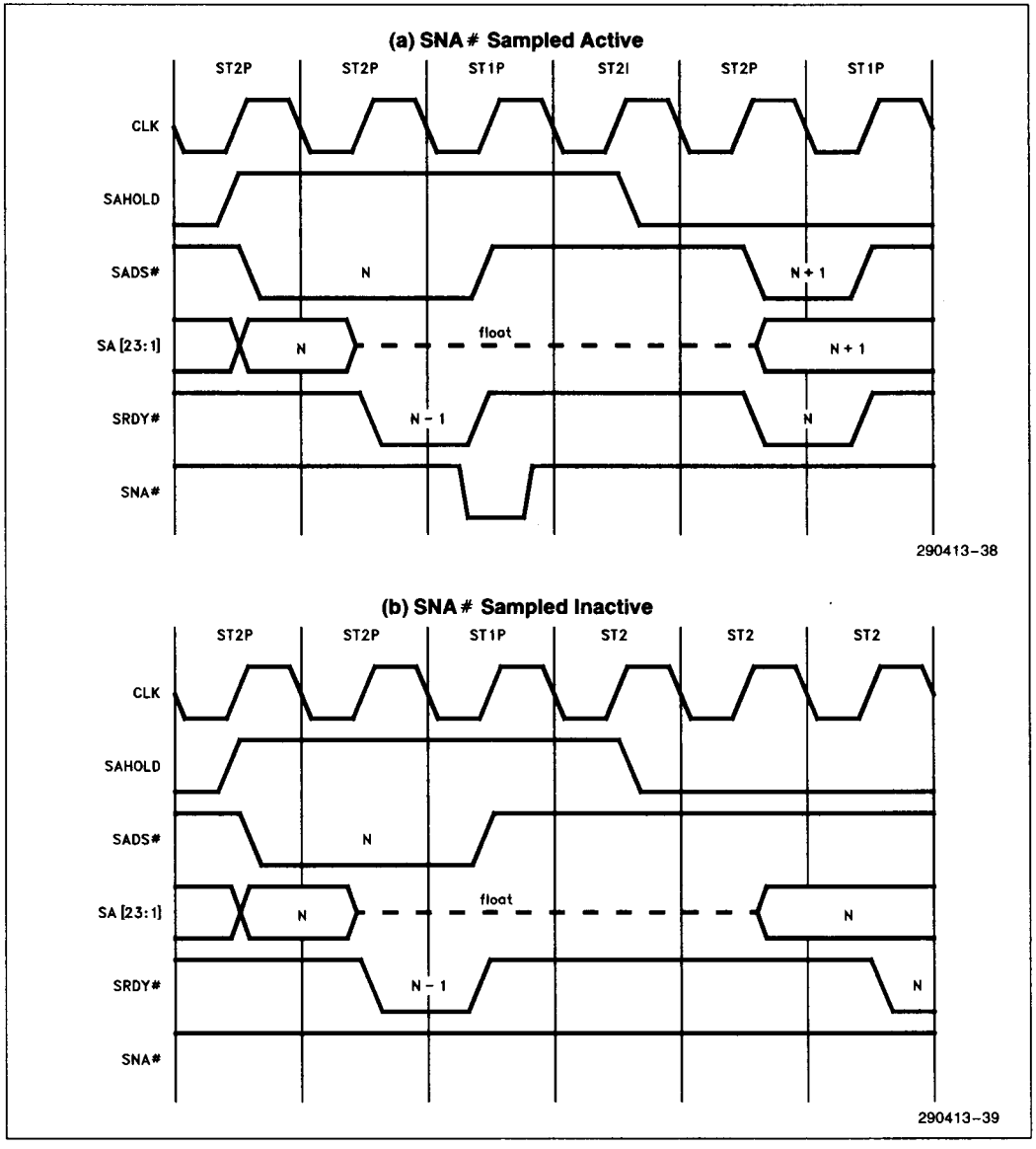


Figure 6.14 SAHOLD Behavior in Pipelined Cycles

6.5 Write Buffer

The 82396SX Smart Cache is able to internally store up to four write cycles (address, data and status information). All those write cycles will run without wait states on the Local Bus. They will run on the System Bus as soon as the bus is available. In case of a write cycle which cannot be stored since the buffer is full, the i386™ SX Microprocessor will be forced to wait until one of the buffered write cycles is completed. READYO# is returned two clocks after SRDY# or SBRDY# is asserted if the write buffer is full. If the write buffer is not full READYO# is returned one clock after SRDY# or SBRDY# is asserted.

All non cacheable write cycles and LOCK#ed writes are not buffered. In this case, the 82396SX Smart Cache will activate READYO# after getting the SRDY# for the non buffered cycle.

The write buffer maintains the exact original order of appearance of the Local Bus requests. It allows no reordering and no bypassing of any sort.

7.0 TESTABILITY FEATURES

This chapter discusses the requirements for properly testing an 82396SX Smart Cache based system after power up and during normal system operation.

Table 7.1 describes how to enter and exit the various 82396SX Smart Cache test modes.

7.1 SRAM Test Mode

This mode is invoked by driving the FLUSH# pin active for less than four clocks during normal operation. SRAM test mode may only be invoked when the 82396SX Smart Cache is in idle state, namely there is no cycle in progress, and no cycle is pending in the 82396SX Smart Cache. The 82396SX Smart Cache exits this mode with subsequent activation of the FLUSH# pin for minimum of one clock cycle. If FLUSH# is activated for at least four clock cycles during SRAM test mode, the 82396SX Smart Cache will FLUSH# its cache directory in addition to terminating the SRAM test mode.

SRAM test mode is provided for system diagnostics purposes. In this mode, the 82396SX Smart Cache cache and cache directory are treated as a standard SRAM. The 82396SX Smart Cache in the system is mapped into address space 256K-512K of the i386™ SX Microprocessor memory space, and allows the CPU non-cacheable, non- buffered access to the rest of the memory and address space. The 82396SX Smart Cache occupies 32KB of address space: 16KB for the cache and 16KB for the TAGRAM (not fully utilized). The 82396SX Smart Cache, in SRAM mode, will recognize i387™ SX Math Coprocessor cycles handle them the same as it does in its normal mode. This way, the CPU may

Table 7-1. Entering/Exiting the Various 82396SX Smart Cache Test Modes

Operating Mode	FLUSH#	SAHOLD	Comments
Tristate Test Mode	0	1	Sampled 1 CLK prior to RESET falling. Exit by next activation of RESET with FLUSH# and SAHOLD deactivated.
SRAM Test Mode	0	X	FLUSH# activation for less than four CLKs during normal mode. Exit with activation of FLUSH# for a minimum of one CLK.
Reserved Mode	0	0	Sampled 1 CLK prior to RESET falling.
Normal Mode	1	X	

execute code that tests the 82396SX Smart Cache as a regular memory component, with the only limitation that no code or data may reside in the memory space 256K-512K during this mode. During SRAM test mode, all accesses to memory space other than 256K-512K are handled exactly as in normal mode with the following exceptions:

1. All read cycles are non-cacheable - read hits are not serviced from the cache and read misses don't cause Line Fills.
2. All write cycles are not buffered.
3. All write cycles do not update the cache.
4. Snooping is disabled.

The local address pins indicate the 82396SX Smart Cache internal addresses. The partitioning is as follows:

- A17 = 1 is reserve in this space.
- A16 = 0 selects the cache directory. A16 = 1 select the cache.
- A15–14 select the "way".
- A11–A4 are the set address.
- A3–1 select a word in the line. Applicable in cache accesses (A16 = 1).

The user can write to any byte in any line in case of a cache write cycle and write to the Tagram fields in one Way in one Tagram write cycle. The memory mapping of the SRAM mode is the described in Table 7.2.

The address space allocated for either Tagram or Cache is 4096 (4K) addresses per way, as can be seen from Table 7.2. The address allocation within each 4K segment is shown in Tables 7.3 and 7.4.

The data presented on the 82396SX Smart Cache local data pins is the SRAM data input. The SRAM data output is also driven on the local data pins. The BHE#, BLE# pins indicate the bytes which must be written. During SRAM test mode, all the AC specifications are met. Figures 7.1 and 7.2 depict the SRAM mode read and write cycles respectively. Note that two wait states are inserted during SRAM test mode read cycles and one wait state is inserted in write cycles. The system may extend the number of wait states by gating READYO# for any number of clock cycles (1 clock cycle in Figure 7.1, 0 clock cycles in Figure 7.2).

The user can write to any byte in any line in case of a cache write cycle and write to specific Tagram fields in one way in one Tagram write cycle. The fields that can be written to are described in Table 7.5. The memory mapping of the SRAM test mode described in Table 7.2.

Table 7.2 SRAM Memory Map

Cache/Tagram	Way	Start Address
Cache	3	05C000h
Cache	2	058000h
Cache	1	054000h
Cache	0	050000h
Tagram	3	04C000h
Tagram	2	048000h
Tagram	1	044000h
Tagram	0	040000h

As can be seen from the above table, the address space allocated for either Tagram or Cache is 4096 (4K) addresses per way. The address allocation within each 4K segment is shown in Table 7.3 for the Cache and Table 7.4 for the Tagram.

Table 7.3 Cache Address Allocation

SET	Word	Start Address
255	7	FFE h
255	6	FFC h
255	5	FFA h
255	4	FF8 h
255	3	FF6 h
255	2	FF4 h
255	1	FF2 h
255	0	FF0 h
.	.	.
.	.	.
2	7	02E h
2	6	02C h
2	5	02A h
2	4	028 h
2	3	026 h
2	2	024 h
2	1	022 h
2	0	020 h
1	7	01E h
1	6	01C h
1	5	01A h
1	4	018 h
1	3	016 h
1	2	014 h
1	1	012 h
1	0	010 h
0	7	00E h
0	6	00C h
0	5	00A h
0	4	008 h
0	3	006 h
0	2	004 h
0	1	002 h
0	0	000 h

5

Table 7.4 Tagram Address Allocation

SET	Start Address	SET	Start Address	SET	Start Address
255	FFE h	2	02A h	1	014 h
255	FFC h	2	028 h	1	012 h
255	FFA h	2	026 h	1	010 h
255	FF8 h	2	024 h	0	00E h
255	FF6 h	2	022 h	0	00C h
255	FF4 h	2	020 h	0	00A h
255	FF2 h	1	01E h	0	008 h
255	FF0 h	1	01C h	0	006 h
.	.	1	01A h	0	004 h
.	.	1	018 h	0	002 h
2	02E h	1	016 h	0	000 h
2	02C h				

Table 7.5 SRAM Test Mode Cache Directory Bit Map
Format in Tagram Read/Writes:

Word Format in Tagram Write:

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LRU B2	LRU B1	LRU B0 & V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

(Data written to D13 writes to LRU bit B0 and to the Valid bit)

Word Format in Tagram Read:

Way 0

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LRU B0	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

Way 1

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LRU B1	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

Way 2

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LRU B2	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

Way 3

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

V = TAG Valid bit
WP = Write Protect bit
"0" - Indicates don't care bits. Writing to these bits will have no effect. When reading the Tagram these bits will have a value of 0.

NOTE:
In Tagram accesses, BHE# and BLE# are ignored in both read and write cycles.

The data presented on the 82396SX Smart Cache D[15:0] pins is the SRAM data input for write cycles and is also the SRAM data output for read cycles during the SRAM test mode. The BHE# and BLE# pins indicate the bytes which will be written to. During SRAM test mode all the AC specifications are met. Figures 7.1 and 7.2 depict the SRAM test mode read and write cycles respectively. The system may extend the number of wait states by gating READYO# for any number of clock cycles (one clock cycle in Figure 7.1, zero in Figure 7.2).

7.2 Tristate Output Test Mode

The 82396SX Smart Cache provides the option of isolating itself from other devices on the board for system debugging, by floating all it's outputs.

Output tristate mode is invoked by driving the SAHOLD and FLUSH# pins active during RESET. The 82396SX Smart Cache will remain in this mode after RESET is deactivated, if SAHOLD and FLUSH# pins are sampled active during the two CLK2s preceding the deactivation of RESET. The 82396SX Smart Cache exits this mode with the next activation of RESET with SAHOLD or FLUSH# driven inactive.

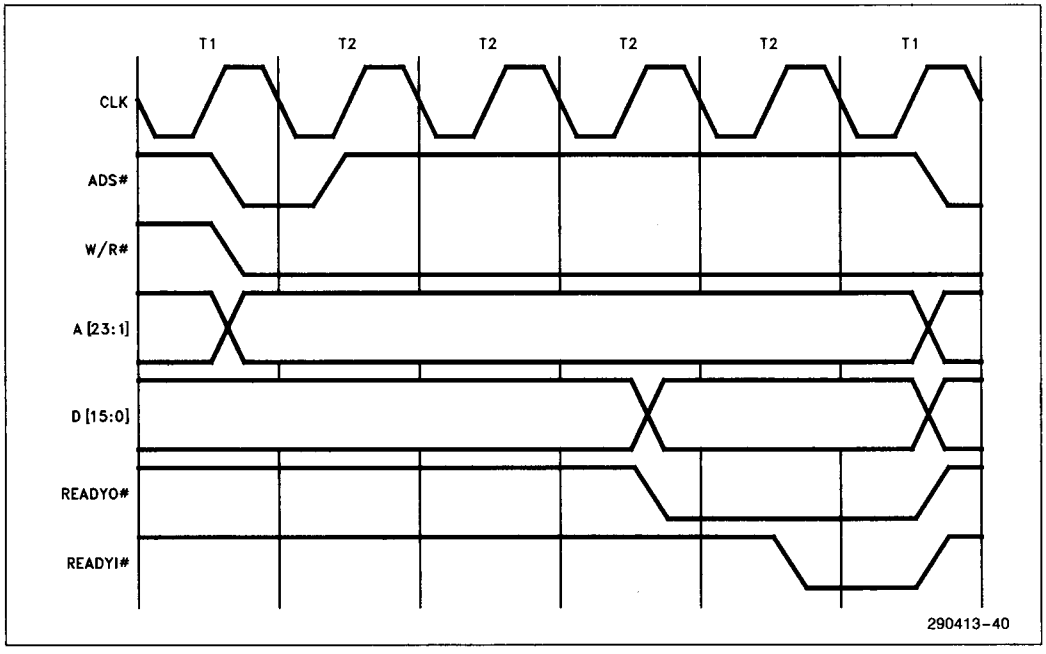


Figure 7.1 SRAM Mode Read Cycle

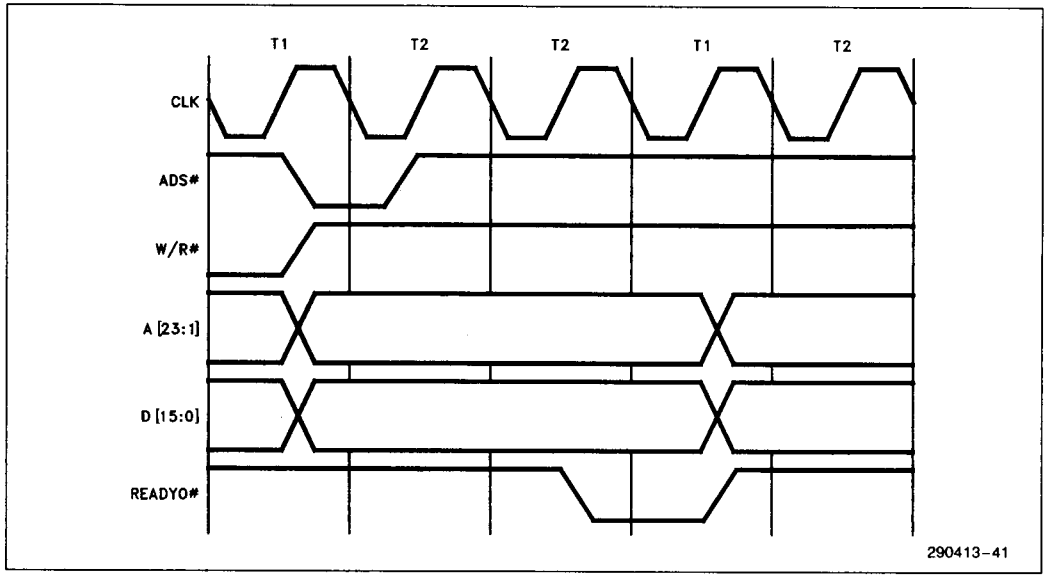


Figure 7.2 SRAM Mode Write Cycle

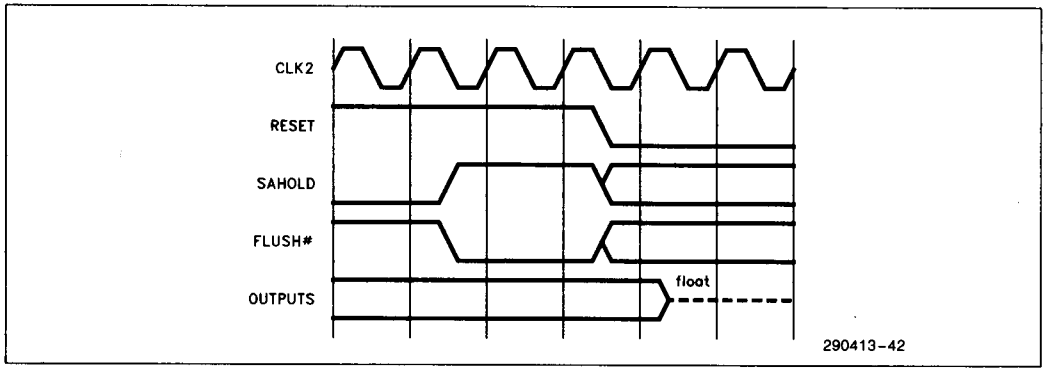


Figure 7.3 Entering the Tristate Test Mode

8.0 MECHANICAL DATA

8.1 Introduction

This chapter discusses the physical package and its connections.

8.2 Pin Assignment

The 82396SX Smart Cache pinout as viewed from the top side of the component is shown in Figure 0.1. V_{CC} and V_{SS} connections must be made to multiple V_{CC} and V_{SS} (GND) planes. Each V_{CC} and V_{SS} must be connected to the appropriate voltage level. The circuit board must contain V_{CC} and V_{SS} (GND) planes for power distribution and all V_{CC} and V_{SS} pins must be connected to the appropriate planes.

8.3 Package Dimensions and Mounting

The 82396SX Smart Cache package is a 132 lead plastic quad flat pack (PQFP). The pins are "fine pitch", 0.025 inches (0.635mm) center to center.

The PQFP device is intended to be surface mounted directly to the printed circuit board although sockets are available for this device.

8.4 Package Thermal Specification

The 82396SX Smart Cache is specified for operation when the case temperature is within the range of 0°C–85°C. The case temperature may be measured in any environment, to determine whether the 82396SX Smart Cache is within the specified operating range. The case temperature must be measured at the center of the top surface which is opposite the pins.

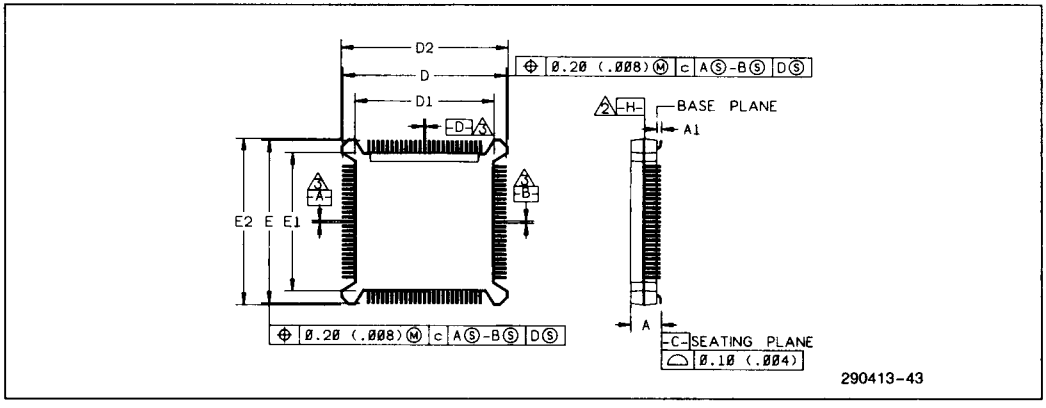


Figure 8.1 Principal Datums and Dimensions

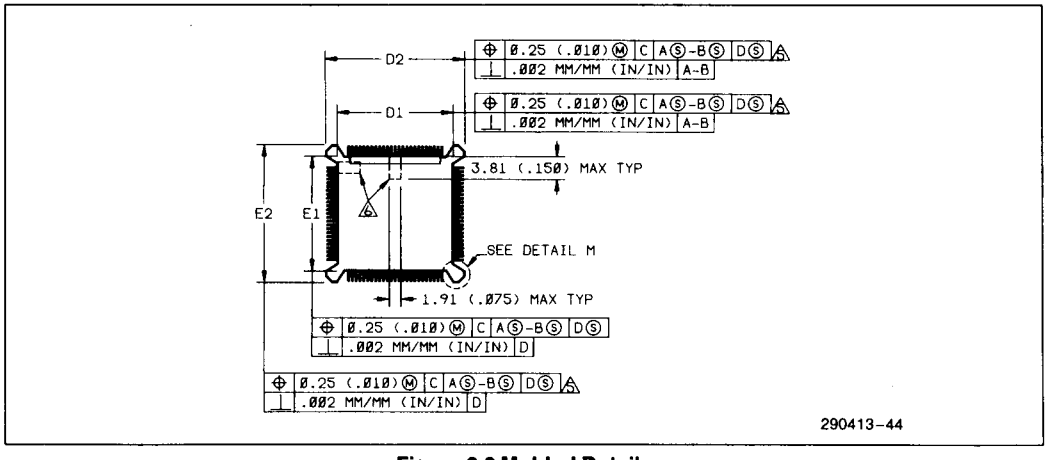


Figure 8.2 Molded Details

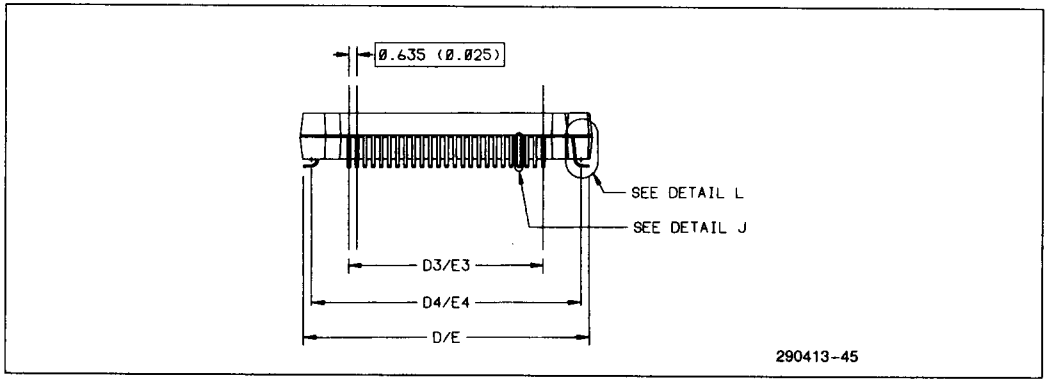


Figure 8.3 Terminal Details

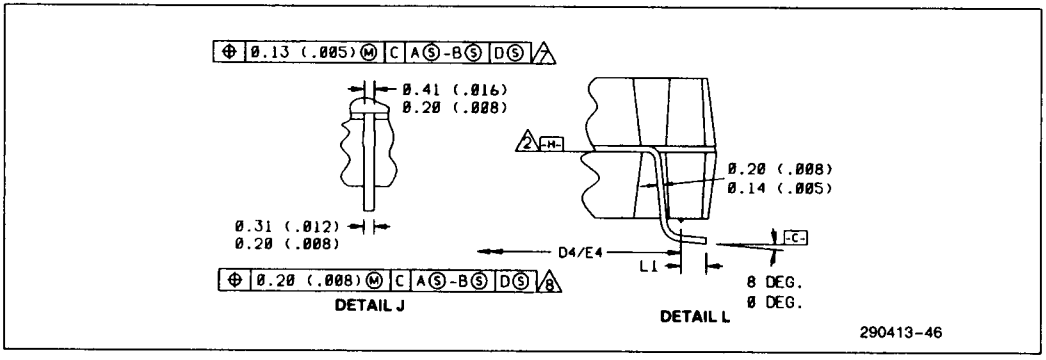


Figure 8.4 Typical Lead

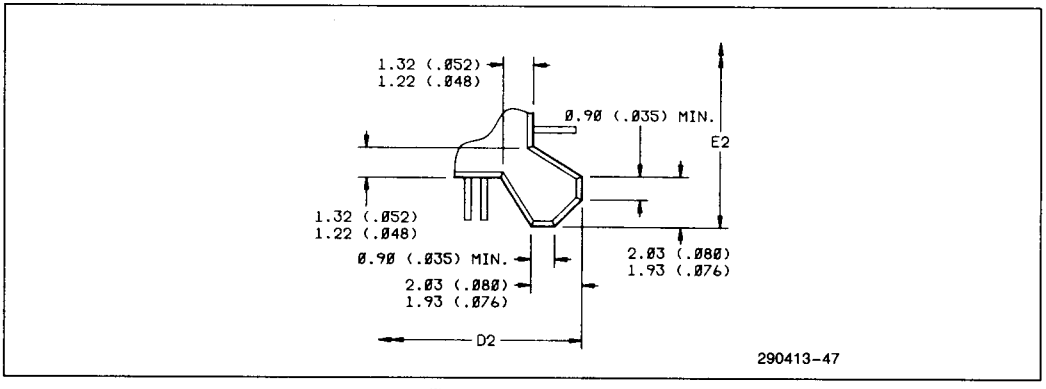


Figure 8.5 Detail M

Table 8.1 Symbol List for PQFP Package

Letter or Symbol	Description of Dimensions	Min (mm)	Max (mm)
A	Package Height: Distance from seating plane to the highest point of the body.	4.06	4.57
A1	Standoff: Distance from the seating plane to the base plane.	0.51	1.02
D/E	Overall Package Dimension: Lead tip to lead tip.	27.18	27.69
D1/E1	Plastic Body Dimension	24.05	24.21
D2/E2	Bumper Distance	27.86	28.01
D3/E3	Footprint	20.32 REF	
D4/E4	Footprint Radius Location	25.89	26.33
L1	Foot Length	0.51	0.76
N	Total Number of Leads	132	

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum plane -H- located at the mold parting line and coincident with the bottom of the lead where lead exits plastic body.
3. Datums A-B and -D- to be determined where center leads exit plastic body at datum plane -H-.
4. Controlling dimension, inch.
5. Dimensions D1,D2, E1 and E2 are measured at the mold parting line and do not include mold protrusion. Allowable mold protrusions of 0.25mm (0.010 in) per side.
6. Pin 1 identifier is located within one of the two zones indicated.
7. Measured at datum plane -H-.
8. Measured at seating plane datum -C-.

Table 8.2. 132 Lead Single Layer PQFP Package with Heat Spreader Typical Thermal Characteristics

Parameter	Thermal Resistance - °C/Watt							
	Airflow - LFM							
	0	50	100	200	400	600	800	1000
θ_{jc}	9	9	9	9	9	9	9	9
θ_{ja}	30	28.8	27.5	25	22	19.5	17.5	16.5

NOTES:
1. Table 2 applies to the 396SX Smart Cache PQFP plugged into the socket or soldered directly onto the board.
2. $\theta_{ca} = \theta_{ja} - \theta_{jc}$, where θ_{ca} is the case to ambient thermal resistance, θ_{ja} is the junction to ambient thermal resistance and θ_{jc} is the junction to case thermal resistance.

The ambient temperature must be controlled to prevent T_{CASE} from being violated. The ambient temperature can be calculated from the thermal resistance values with the following equations:

$$T_J = T_{CASE} + P * \theta_{jc}$$

$$T_{amb} = T_J - P * \theta_{ja}$$

$$T_{CASE} = T_{amb} + P * [\theta_{ja} - \theta_{jc}]$$

Values for θ_{ja} and θ_{jc} are given in Table 8.2 for the 132-lead single layer PQFP package with heat spreader at various airflow rates. Table 8.3 shows the maximum T_{amb} allowable (without exceeding T_{CASE}) at various airflows. Note that T_{amb} can be improved further by attaching 'fins' or a 'heat sink' to the package.

Table 8.3. Ambient Temperature Requirements

Using I_{CC2}	Ambient Temperature to not exceed T_{CASE} = 85°C							
	Airflow - LFM							
	0	50	100	200	400	600	800	1000
T_{amb} −25 MHz (°C)	45.6	48.0	50.3	55.0	60.6	65.3	69.1	70.9

NOTE:
The numbers in Table 8.3 were calculated using V_{CC} of 5.0V and an I_{CC} of 320 mA. This I_{CC} measurement is representative of the worst case I_{CC} at T_C = 85°C with the outputs unloaded.
1. These values have been either interpolated or extrapolated.

9.0 ELECTRICAL DATA

This chapter presents the A.C. and D.C. specifications for the 82396SX Smart Cache.

9.1 Power and Grounding

The 82396SX Smart Cache has a high clock frequency and 66 output buffers which can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, 10 Vcc and 12 Vss pins separately feed power to the functional units of the 82396SX Smart Cache.

Power and ground connections must be made to all external Vcc and Vss pins of the 82396SX Smart Cache. On the circuit board, all Vcc pins must be connected on a Vcc plane and all Vss pins must be connected on a GND plane.

9.1.1 POWER DECOUPLING RECOMMENDATIONS

A liberal amount of decoupling capacitors must be placed near the 82396SX Smart Cache. The 82396SX Smart Cache driving its 16 bit local and system data buses and 23 bit system address bus at high frequency can cause transient power surges, particularly when driving large capacitive loads. Low inductance capacitors and interconnects are recommended for the best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the 82396SX Smart Cache and the decoupling capacitors as much as possible.

9.1.2 RESISTOR RECOMMENDATIONS

The 82396SX Smart Cache does not have any internal pullup resistors. All unused inputs must be pulled up to a solid logic level through a 20 kΩ resistor. The outputs that require external pullup resistors are listed in Table 9.1. A particular designer may have reason to adjust the resistor values recommended here, or alter the use of pull-up resistors in other ways.

9.2 Absolute Maximum Ratings

Storage Temperature ..... −65°C to +150°C
Case Temperature under Bias ... −65°C to +110°C
Supply Voltage with
Respect to V_{SS} ..... −0.5V to +6.5V
Voltage on Other Pins ..... −0.5V to V_{CC} + 0.5V.

Table 9.1 Pullup Resistor Recommendations

Signal	Pullup Value	Purpose
SADS#	20KΩ ±10%	Lightly pull SADS# inactive while 82396SX Smart Cache is not driving it.
READYO#	20KΩ ±10%	Lightly pull READYO# inactive while 82396SX Smart Cache is not driving it.
SLOCK#	20KΩ ±10%	Lightly pull SLOCK# inactive for 82396SX Smart Cache SHOLD states.

9.3 D.C. Specifications T_{CASE} = 0°C to +85°C, V_{CC} = 5V ±5%

Table 9.2 DC Specifications

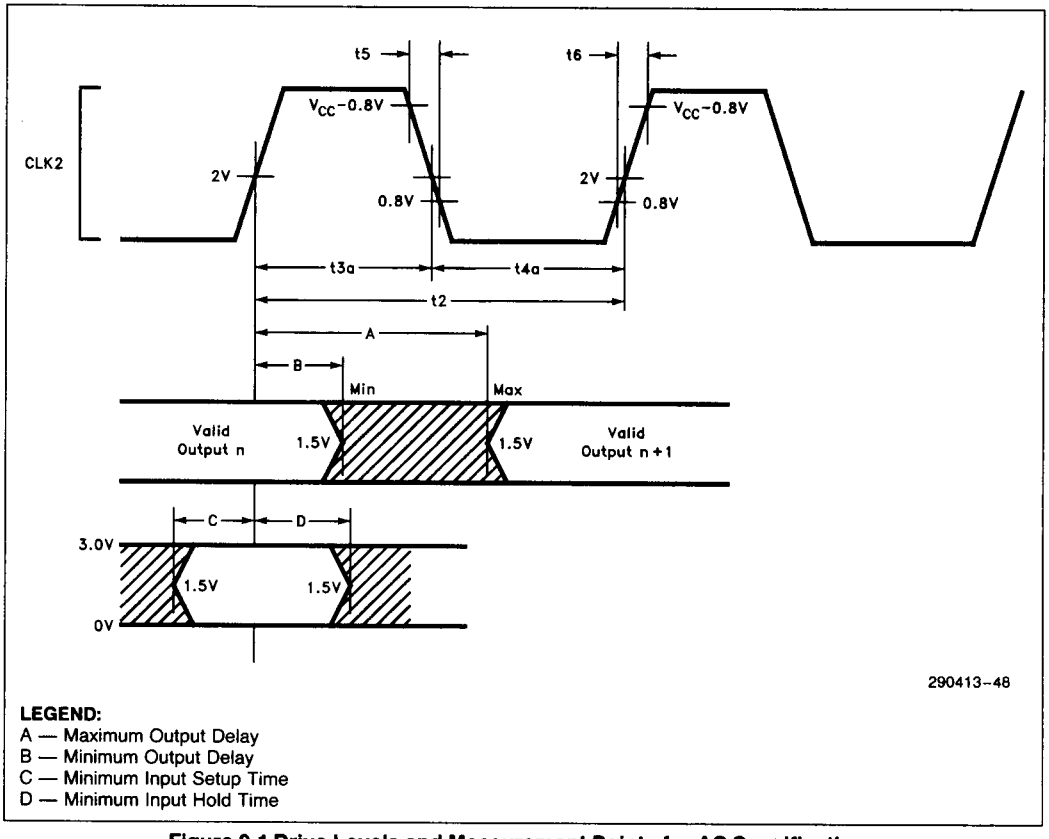
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Volt.	2.0	V_{CC} + 0.3	V	
V_{CIL}	CMOS Input Low	−0.3	0.8	V	See Note 6
V_{CIH}	CMOS Input High	V_{CC} − 0.8	V_{CC} + 0.3	V	See Note 6
V_{OL}	Output Low Volt.		0.45	V	See Note 1
V_{OH}	Output High Volt.	2.4		V	See Note 2
V_{COL}	CMOS Output Low Volt.		0.45	V	See Notes 1,7
V_{COH}	CMOS Output High Volt.	V_{CC} − 0.45		V	See Notes 2,7
I_{LI}	Input Leakage		± 15	μA	$0V < V_{IN} < V_{CC}$
I_{LO}	Output Leakage		±15	Ua	$0.45V < V_{OUT} < V_{CC}$
C_{IN}	Cap. Input		10	pF	See Note 4
I_{CC}	Power Supply Current @ 0°C		525	mA	See Note 3
I_{CC2}	Power Supply Current @ +85°C		320	mA	See Note 8

NOTES:
1) This parameter is measured at IOL = 4mA for all the outputs.
2) This parameter is measured at IOH = 1mA for all the outputs.
3) Measured with inputs driven to CMOS levels, V_{CC} = 5.25V, 0°C, using a test pattern consisting of 40% read, 40% write, and 20% idle cycles. Due to the self-heating of the part after power is applied, this I_{CC} value will be reduced in actual applications. Refer to Table 8.3 for the ambient temperature requirements.
4) CLK2 input capacitance is 20pF.
5) No activity on the Local/System Bus.
6) Applies to CLK2, READYO# inputs.
7) Applies to READYO# output.
8) I_{CC2} was calculated using V_{CC} of 5.0V at T_C = 85°C. This I_{CC} measurement is representative of the worst case I_{CC} at T_C = 85°C with the outputs unloaded. This is not 100% tested.

9.4 A.C. Characteristics

Some of the 82396SX Smart Cache AC parameters are clock- frequency dependent. Thus, while the part functions properly at the entire frequency range specified by the T1 spec, the AC parameters are guaranteed at one distinct frequency only: 20MHz.

- Functional operating range: V_{CC} = 5V ±5%, T_{CASE} = 0°C to 85°C.
- All AC parameters are measured relative to 1.5V for falling and rising, CLK2 is at 2V.
- All outputs tested at a 50 pF load. In case of overloaded signals, the derating factor is 1 ns for every extra 25 pF load.
- All parameters are referred to PHI1 unless otherwise noted.
- The reference figure of CLK2 parameters and AC measurements level is Figure 9.1 and RESET and internal phase is Figure 3.2.



LEGEND:
A — Maximum Output Delay
B — Minimum Output Delay
C — Minimum Input Setup Time
D — Minimum Input Hold Time

Figure 9.1 Drive Levels and Measurement Points for AC Specifications

9.4.1 A.C. CHARACTERISTICS TABLES T_{CASE} = 0°C to +85°C, V_{CC} = 5V ±5%

Table 9.3 Local Bus Signal AC Parameters

Symbol	Parameter	20 MHz		25 MHz		Units	Notes
		Min	Max	Min	Max		
t1	Operating Frequency	15.4	20	15.4	25	MHz	Internal CLK
t2	CLK2 Period	25	32.5	20	32.5	ns	
t3a	CLK2 High Time	8		7		ns	Measured at 2V
t3b	CLK2 High Time	5		4		ns	Measured at 3.7V
t4a	CLK2 Low Time	8		7		ns	Measured at 2V
t4b	CLK2 Low Time	6		5		ns	Measured at 0.8V
t5	CLK2 Fall Time		7		7	ns	Note 1
t6	CLK2 Rise Time		7		7	ns	Note 2
t7a	A[23:1] Setup Time	23		17		ns	
t7b	LOCK# Setup Time	14		14		ns	
t7c	BHE#, BLE# Setup Time	20		14		ns	
t8	A[23:1],BHE#,BLE#, LOCK# Hold Time	4		3		ns	
t9a	M/IO#,D/C#,W/R# Setup Time	22		17		ns	
t9b	ADS# Setup Time	23		17		ns	
t10	M/IO#,D/C#,W/R#, ADS# Hold Time	5		4		ns	
t11	READYI# Setup Time	11		9		ns	
t12	READYI# Hold Time	4		4		ns	
t13	BEM, NPI# Setup Time	10		9		ns	Note 7
t14	RESET Setup Time	12		10		ns	
t15a	BEM, NPI# Hold Time	3		1		ns	
t15b	RESET Hold Time	4		3		ns	
t16	D0–15 Setup Time	15		11		ns	
t17	D0–15 Hold Time	3		1		ns	
t18	D0–15 Valid Delay		39	7	32	ns	Note 8
t19	D0–15 Float Delay	6	25	4	22	ns	Note 5
t20	READYO# Valid Delay	4	32	4	22	ns	
t21	READYO# Float Delay		25			ns	Notes 4,5

Table 9.4 System Bus Signal AC Parameters

Symbol	Parameter	20 MHz		25 MHz		Units	Notes
		Min	Max	Min	Max		
t31	SA1-23, SBLE#, SBHE#, SLOCK#, SD/C#, SW/R#, SM/IO# Valid Delay	4	18	4	18	ns	
t31a	SADS# Valid Delay	4	18	4	19	ns	
t32	SA1-23, SBHE#, SBLE#, SLOCK#, SD/C#, SW/R#, SM/IO# Float Delay	4	30	4	30	ns	Note 5
t32a	SADS# Float Delay	4	30	4	30	ns	Notes 4,5
t33	SBLAST#,SHLDA Valid Delay	4	26	4	22	ns	
t34	SBLAST# Float Delay	4	30	4	30	ns	Note 5
t35	SD[15:0] Write Data Valid Del.	4	33	6	27	ns	Note 4
t36	SD[15:0] Float Delay	4	27	4	22	ns	Notes 4,5
t37	SA[23:4] Setup Time	10		9		ns	
t38	SA[23:4] Hold Time	4		4		ns	
t39	SD[15:0] Read Setup Time	9		7		ns	
t40	SD[15:0] Read Hold Time	5		5		ns	
t41	SNA# Setup Time	5		7		ns	Note 3
t42	SNA# Hold Time	12		4		ns	Note 3
t43a	SKEN# Setup Time	9		9		ns	
t43b	SHOLD,SAHOLD Setup Time	17		10		ns	
t43c	SWP# Setup Time	17		10		ns	
t44a	SHOLD, SWP# Hold Time	3		3		ns	
t44b	SKEN# Hold Time	4		4		ns	
t44c	SAHOLD Hold Time	4		4		ns	
t45a	SEADS# Setup Time	12		10		ns	
t45b	SRDY#,SBRDY# Setup Time	12		9		ns	
t46	SEADS#,SRDY#, SBRDY# Hold Time	4		4		ns	
t47	FLUSH,A20M# Setup Time	18		10		ns	Note 6
t48	FLUSH,A20M# Hold Time	3		3		ns	Note 6

NOTES:
1. Tf is Measured at 3.7V to 0.8V. Tf is not 100% tested.
2. Tr is Measured at 0.8V to 3.7V. Tr is not 100% tested.
3. The specification is relative to PHI2 i.e. signal sampled by PHI2.
4. The specification is relative to PHI2 i.e. signal driven by PHI2.
5. Float condition occurs when maximum output current becomes less than ILO in magnitude. Float delay is not 100% tested.
6. The signal is allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
7. The signal is not sampled. It must be valid through the entire cycle (as the Address lines).
8. For Data min Valid Delay see min float times (local data lines are floated in the next cycle after being driven active).

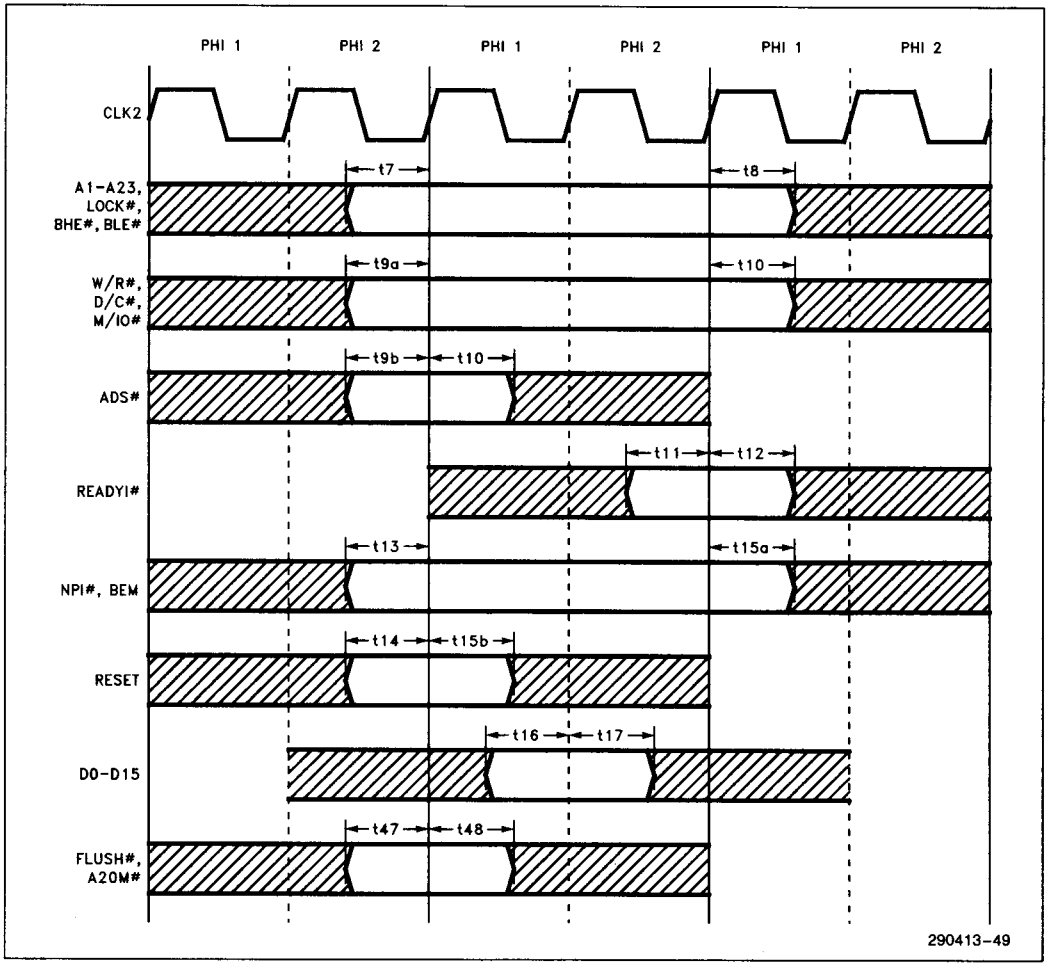


Figure 9.2 AC Timing Waveforms - Local Bus Input Setup and Hold Timing

5

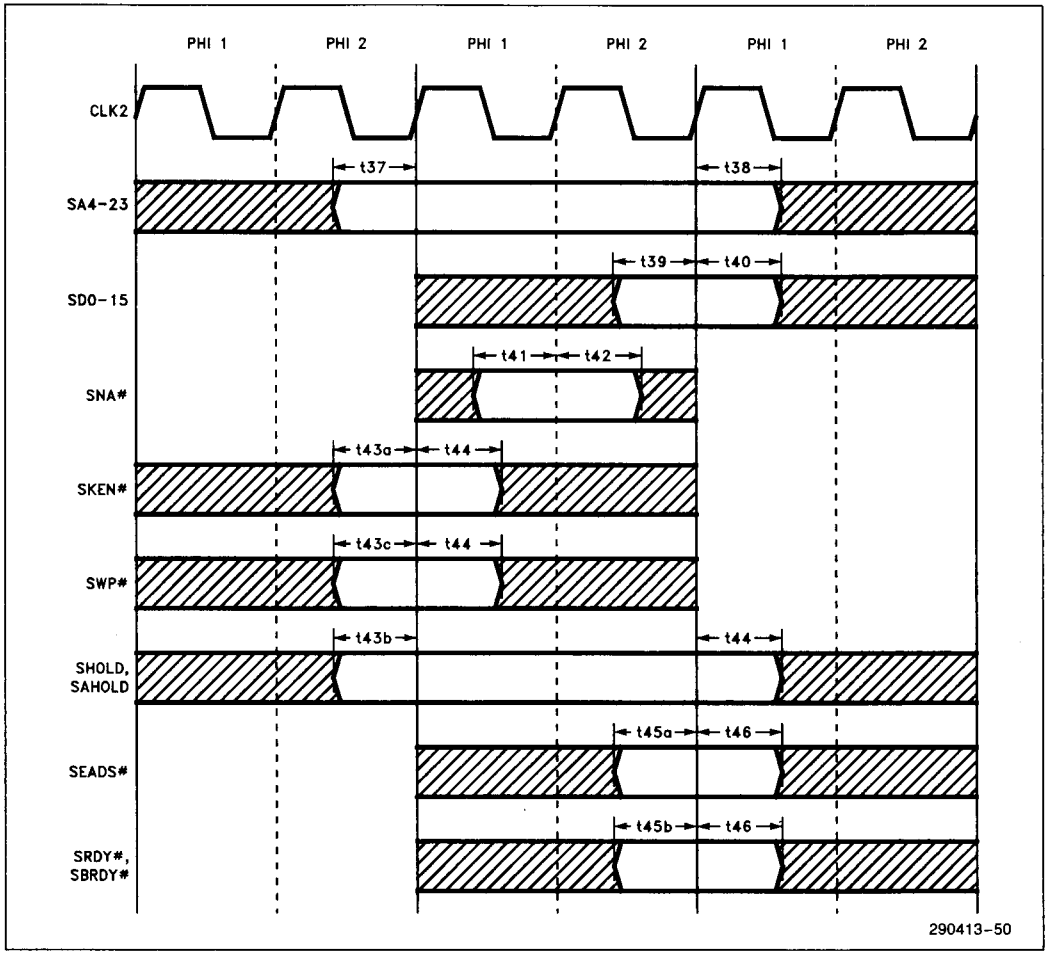


Figure 9.3 AC Timing Waveforms - System Bus Input Setup and Hold Timing

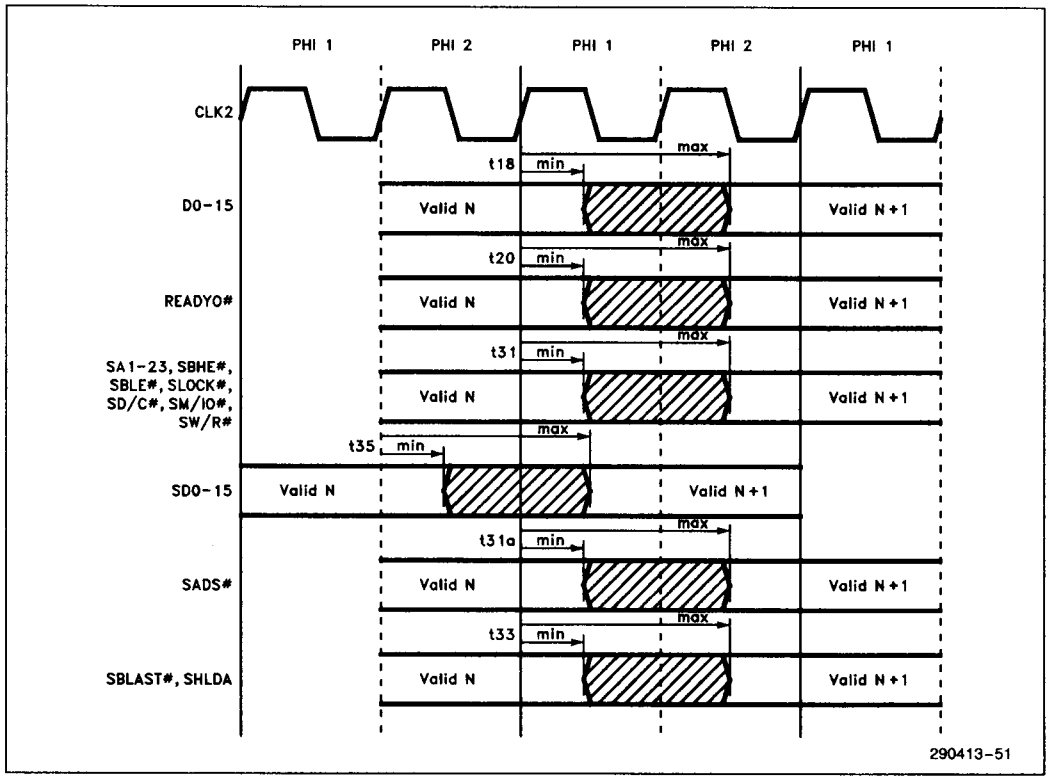


Figure 9.4 AC Timing Waveform - Output Valid Delay

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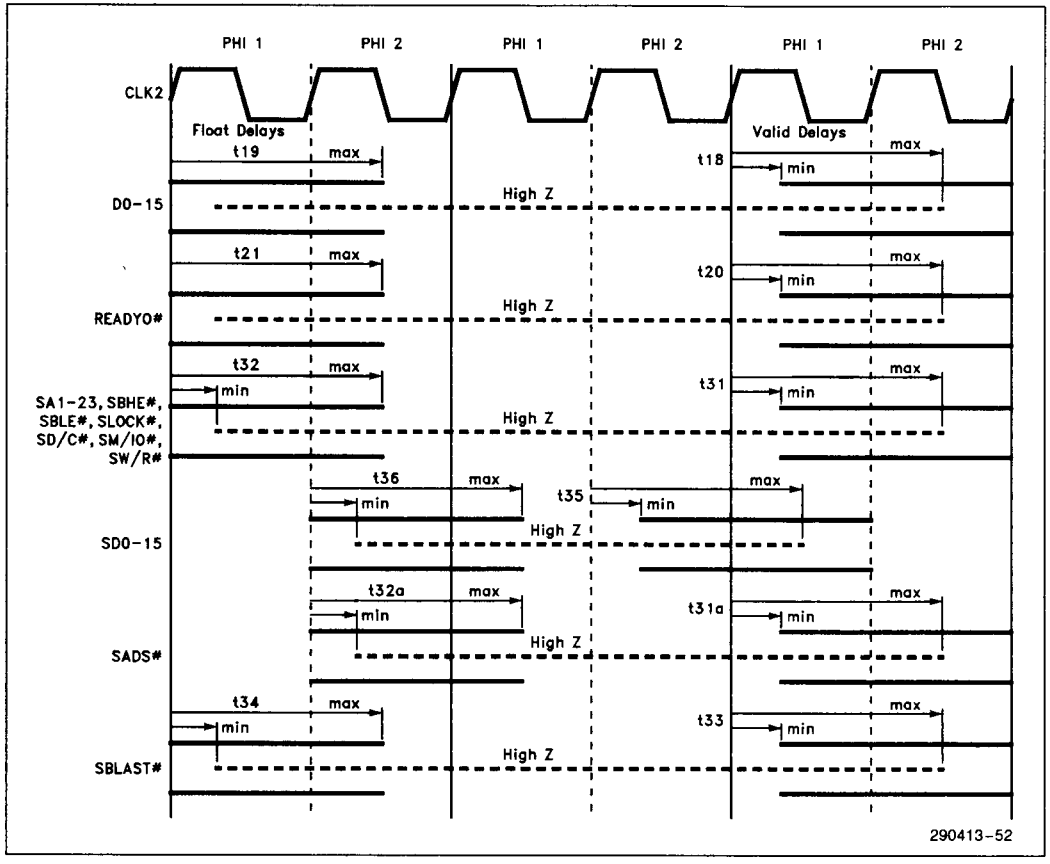

Figure 9.5 AC Timing Waveform - Output Float Delays

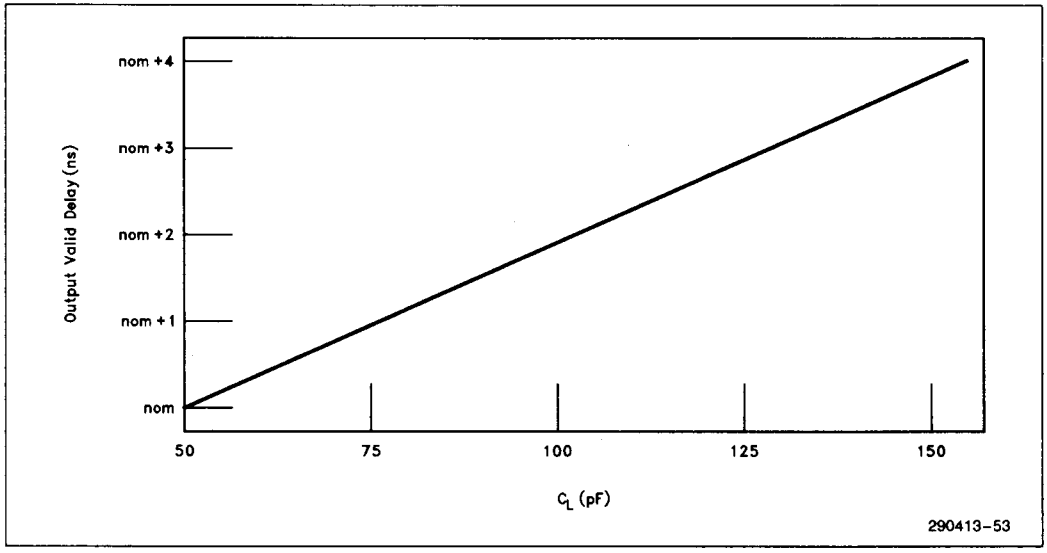

Figure 9.6 Typical Output Valid Delay vs Load Capacitance at Maximum Operating Temperature (C_L = 50 pF)

APPENDIX A

Term	Definition
AC	Alternating Current
ALF	Aborted Line Fill
B	Byte
CDF	Cache Directory FLUSH
CDL	Cache Directory Lookup
CDS	Cache Directory SNOOP
CDT	Testability Access
CDU	Cache Directory Update
CR	Cache Read
CW	Cache Write
CU	Cache Update
CT	Testability Access
CPU	Central Processing Unit
CHMOS	Complimentary High Performance Metal Oxide Semiconductor
CRDH	Cache Read Hit
CRDM	Cache Read Miss
CWTH	Cache Write Hit
DC	Direct Current
MSB	Most Significant Bit(s)
DRAM	Dynamic Random Access Memory
DMA	Direct Memory Access
DW	Double Word
GND	Ground
I/O	Input/Output
LB	Local Bus
LRU	Least Recently Used
PQFP	Plastic Quad Flat Pack

Term	Definition
RAM	Random Access Memory
SB	System Bus
TV	Tag Valid
WP	Write Protect
W	Word
xxK	xx thousand
xxKB	xx K Bytes
xxGB	xx Giga Bytes
xWS	xx Wait States
T1	Local Bus State
T2	Local Bus State
TI	Local Bus State
TH	Local Bus State
ST1	System Bus State
ST1P	System Bus State
ST2	System Bus State
ST2P	System Bus State
STI	System Bus State
STH	System Bus State
PHI1	1st CLK2 cycle in a 2 CLK2 CLK cycle
PHI2	2nd CLK2 cycle in a 2 CLK2 CLK cycle
C	Celsius
V	Volts
μA	10^{-6} Amps
mA	10^{-3} Amps
pF	10^{-12} Farads
MHz	10^{6} Hertz
ns	10^{-9} seconds

APPENDIX B

386 SMART CACHE TO 82396SX SMART CACHE DESIGN DIFFERENCES

The 82396SX Smart Cache has the same functional features as the 386 Smart Cache (82395DX) except as noted below.

Cache Architecture

Table B-1. 82395DX/82396SX Architectural Comparison

Feature	82395DX	82396SX
Cache Size	16K	16K
Associativity	4 Way	4 Way
Line Size	16B	16B
Lines/Sector	1	1
Write Buffer	4 DW	4 W
Expandability	to 32K or 64K	none
Line Fill	4DW serial burst or pipelined	8 W serial burst or pipelined
Address Bus's	A[31:2], SA[31:2]	A[23:1], SA[23:1]
Data Bus's	D[31:0], SD[31:0]	D[15:0], SD[15:0]
Bus Width	BE[3:0]#, SBE[3:0]#	BHE#, BLE#, SBHE#, SBLE#

82396SX Smart Cache Pin Definitions

The 82396SX Smart Cache will have the same pins as the 386 Smart Cache (82395DX) except as noted below.

SNENE# The 82396SX Smart Cache does not have an SNENE# pin. Page hit/miss decisions will be made by the DRAM controller.

LBA# Local Bus resources are not supported (the 82396SX Smart Cache will decode i387™ SX cycles and provide READYO# to the processor).

SBREQ SBREQ is not provided on the 82396SX Smart Cache.

SFHOLD# SFHOLD# is not provided on the 82396SX Smart Cache.

BE[3:0]# Replaced by BHE# and BLE#.

SBE[3:0]# Replaced by SBHE# and SBLE#.

BEM The 386 Smart Cache does not have BEM pin.

A[31:2] Modified to A[23:1] for the 16M address range of the 82396SX Smart Cache.

SA[31:2] Modified to SA[23:1] for the 16M address range of the 82396SX Smart Cache.

D[31:0] Modified to D[15:0] for the 16 bit data bus width of the 82396SX Smart Cache.

SD[31:0] Modified to SD[15:0] for the 16 bit system data bus width of the 82396SX Smart Cache.

82396SX Smart Cache Address Differences

Table B-2. 82396SX Smart Cache Address Differences

Device	TAG	SET	DW/W	Byte
82395DX	A[31:12]	A[11:4]	A[3:2]	BE[3:0]#
82396SX	A[23:12]	A[11:4]	A[3:1]	BHE#, BLE#

82396SX Smart Cache Line Fill Order

The Line Fill order for burst and non-burst Line Fill cycles is shown in Table B-3.

Table B-3. 82396SX Smart Cache Line Fill Order

82396SX Smart Cache Line Fill Order (SA[3:1])							
Word within Line Fill							
1st	2nd	3rd	4th	5th	6th	7th	8th
0	2	4	6	8	A	C	E
2	0	6	4	A	8	E	C
4	6	0	2	C	E	8	A
6	4	2	0	E	C	A	8
8	A	C	E	0	2	4	6
A	8	E	C	2	0	6	4
C	E	8	A	4	6	0	2
E	C	A	8	6	4	2	0

5

82396SX Smart Cache SRAM Test Mode

The following cache directory bits are accessed via the 16-bit data bus when the cache directory is selected during SRAM Test Mode.

Table B-4. SRAM Test Mode Cache Directory Bit Map

Word Format in Tagram Write:

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LRU B2	LRU B1	LRU B0 & V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

(Data written to D13 writes to LRU bit B0 and to the Valid bit)

Word Format in Tagram Read:

Way 0

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LRU B0	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

Way 1

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LRU B1	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

Way 2

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LRU B2	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

Way 3

Local Data Bus

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	V	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	WP

V = TAG Valid bit
WP = Write Protect bit
"0" - Indicates don't care bits. Writing to these bits will have no effect. When reading the Tagram these bits will have a value of 0.

NOTE:
In Tagram accesses, BHE# and BLE# are ignored in both read and write cycles.

82396SX SMART CACHE SRAM TEST MODE— ADDRESS MAPPING

The following tables show the address mapping for the SRAM test mode.

Table B-5. SRAM Test Mode Address Decoding Signals

Address Decoding - Local Address Pins

Cache/Tagram#	[A16]
Way	[A15:A14]
Set	[A11:A4]
Addr Space 256K-512K	[A23:A17]
Word	[A3:A1]
Byte	BHE#,BLE#
Unused	A[13:12] = 00

NOTE:
No code or data should reside between 256K-512K.

Table B-6. SRAM Test Mode Start Address Memory Map

Cache/Tagram	Way	Start Address
Cache	3	05C000h
Cache	2	058000h
Cache	1	054000h
Cache	0	050000h
Tagram	3	04C000h
Tagram	2	048000h
Tagram	1	044000h
Tagram	0	040000h

Table B-7. SRAM Test Mode Cache Address Allocation

SET	Word	Start Address
255	7	FFE h
255	6	FFC h
255	5	FFA h
255	4	FF8 h
255	3	FF6 h
255	2	FF4 h
255	1	FF2 h
255	0	FF0 h
.	.	.
.	.	.
2	7	02E h
2	6	02C h
2	5	02A h
2	4	028 h
2	3	026 h
2	2	024 h
2	1	022 h
2	0	020 h
1	7	01E h
1	6	01C h
1	5	01A h
1	4	018 h
1	3	016 h
1	2	014 h
1	1	012 h
1	0	010 h
0	7	00E h
0	6	00C h
0	5	00A h
0	4	008 h
0	3	006 h
0	2	004 h
0	1	002 h
0	0	000 h

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Table B-8. SRAM Test Mode Tagram Address Allocation

SET	Start Address
255	FFE h
255	FFC h
255	FFA h
255	FF8 h
255	FF6 h
255	FF4 h
255	FF2 h
255	FF0 h
.	.
.	.
2	02E h
2	02C h
2	02A h
2	028 h
2	026 h
2	024 h
2	022 h
2	020 h
1	01E h
1	01C h
1	01A h
1	018 h
1	016 h
1	014 h
1	012 h
1	010 h
0	00E h
0	00C h
0	00A h
0	008 h
0	006 h
0	004 h
0	002 h
0	000 h

82396SX Revision Summary

The following changes have been made since revision 001:

Section 3.2.6.2 New sentence added to end of section. This sentence reads, "SEADS# is a synchronous signal and has both setup and hold timing specifications referenced in CLK2.".

Section 8.4 Tables 8.2 and 8.3 were replaced with new information.

Section 9.4.1 Tables 9.3 and 9.4 have been updated with 25 MHz information.