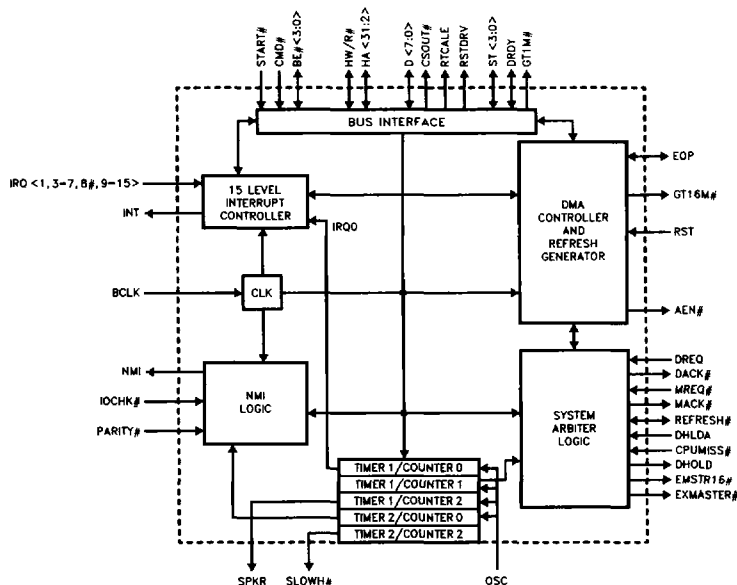


82357 INTEGRATED SYSTEM PERIPHERAL (ISP)

- Provides Enhanced DMA Functions
 - ISA/EISA DMA Compatible Cycles
 - All Transfers are Fly-By Transfers
 - 32-Bit Addressability
 - Seven Independently Programmable Channels
 - Provides Timing Control for 8-, 16-, and 32-Bit DMA Data Transfers
 - Provides Timing Control for Compatible, Type "A", Type "B", and Type "C" (Burst) Cycle Types
 - 33 Mbytes/sec Maximum Data Transfer Rate
 - Provides Refresh Address Generation
 - Supports Data Communication Devices and Other Devices That Work from a Ring Buffer in Memory
 - Incorporates the Functionality of Two 82C37A DMA Controllers
- Provides High Performance Arbitration
 - For CPU, EISA/ISA Bus Masters, DMA Channels, and Refresh
- Incorporates the Functionality of Two 82C59A Interrupt Controllers
 - 14 Independently Programmable Channels for Level-or-Edge Triggered Interrupts
- Five Programmable 16-Bit Counter/Timers
 - Generates Refresh Request Signal
 - System Timer Interrupt
 - Speaker Tone Output
 - Fail-Safe Timer
 - Periodic CPU Speed Control
 - 82C54 Programmable Interval Timer Compatible
- Provides Logic for Generation/Control of Non-Maskable Interrupts
 - Parity Errors for System and Expansion Board Memory
 - 8 μ s and 32 μ s Bus Timeout
 - Immediate NMI Interrupt via Software Control
 - Fail-Safe Timer
- 132-Pin PQFP Package
(See Packaging Spec: Order # 231369)



82357 Internal Block Diagram



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