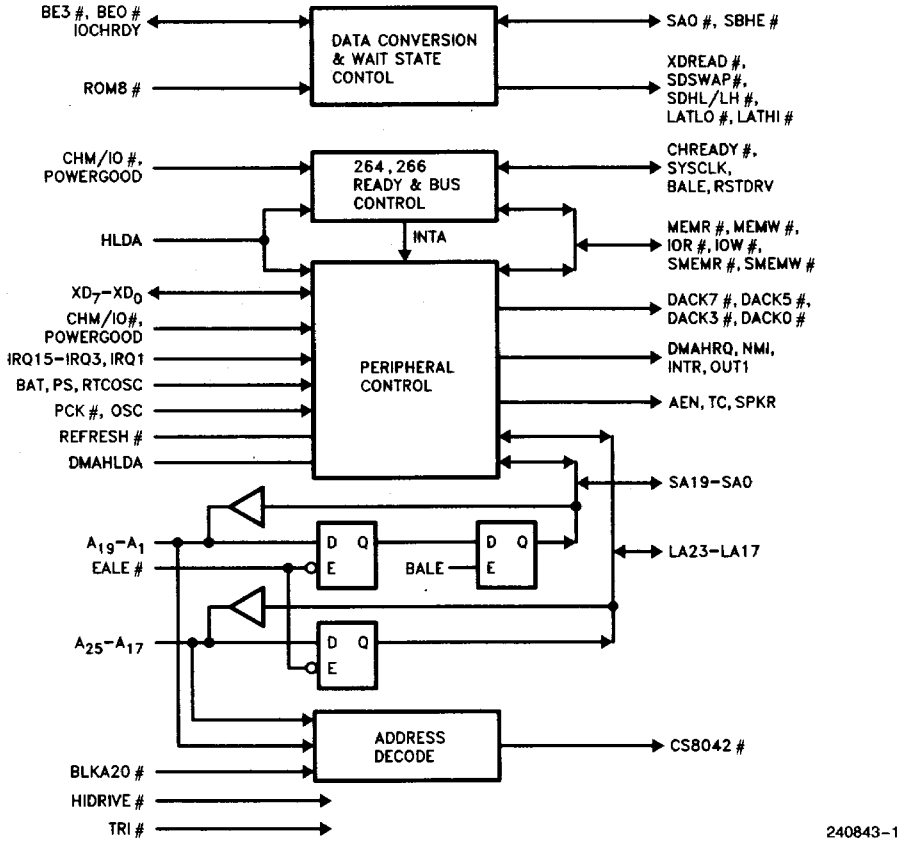
82344
ISA BUS CONTROLLER

The 82344 ISA Bus Controller replaces several of the LSI controllers used in PC/AT*-type designs with one single 160-pin quad flatpack. The Bus Controller provides the functions of DMA, page address register, timer, interrupt control, Port B logic, slot bus refresh address generation, and real time clock.

The Bus Controller directly drives the refresh addresses onto the AT slot address bus during refresh cycles in response to a refresh cycle command from the System Controller. To avoid problems with sensitive slot bus add-in cards, the Bus Controller features "bus quiet" mode. When no valid slot bus accesses are occurring, the SA bus and control lines do not change states. Rather, they retain their previous logic state.

Built-in sleep mode features work together with System Controller sleep features to provide a low power system idle state for extension of battery life in portable systems. When activated by the CPU via I/O write to an internal indexed configuration register, the DMA sybsystem clock is stopped and the AT slot bus remains in BUS QUIET state. The SYSCLK can be individually controlled. The interrupt controllers and the timers continue to operate. If an interrupt occurs due to an external source or any of the timers, the Bus Controller "wakes up" and in turn wakes the System Controller.

Block Diagram



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The upgraded DMA channels provide a superset of AT functionality by allowing DMA to the entire 64 Mbyte memory range of the 82340DX chip set. Additional functionality is provided via DMA wait state, clock, and —MEMR timing programmability.

A —HIDRIVE pin can be externally strapped to provide for 12 mA or 24 mA drive to the slot bus. If left open, an internal pull-up causes the drive current to default to 24 mA. This allows systems designed with one to four slots to select a lower drive level and reduce bus ringing. A —ROM8 pin selects the bus and bus size to use for BIOS ROM accesses. The choices are 8- or 16-bit wide ROMs.

A three-state test control pin has been added for board level testability.

The Bus Controller features several megacells, implemented in 1.5-micron CMOS technology, and is intended to work in 386™ SX or 386™ DX microprocessor-based systems with CPU clock speeds up to 33 MHz and bus speeds up to 16 MHz.

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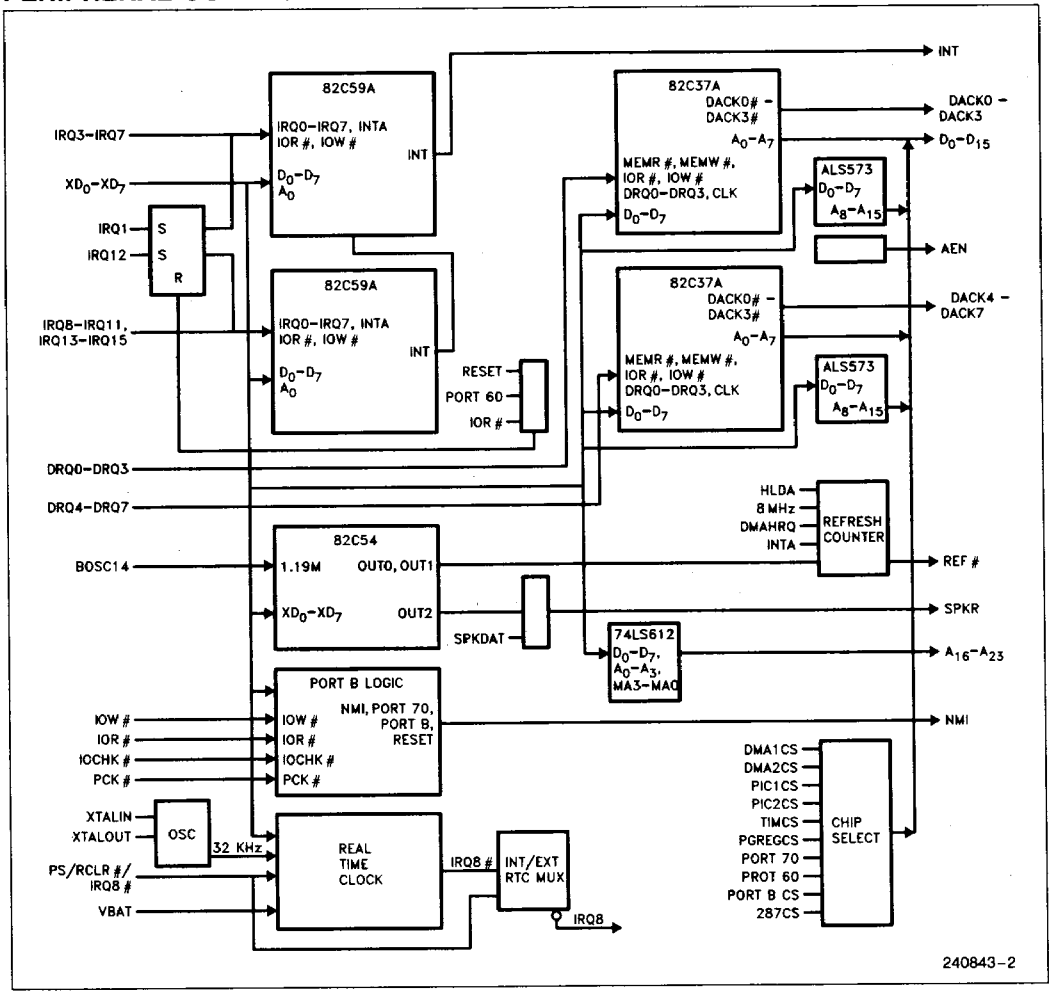
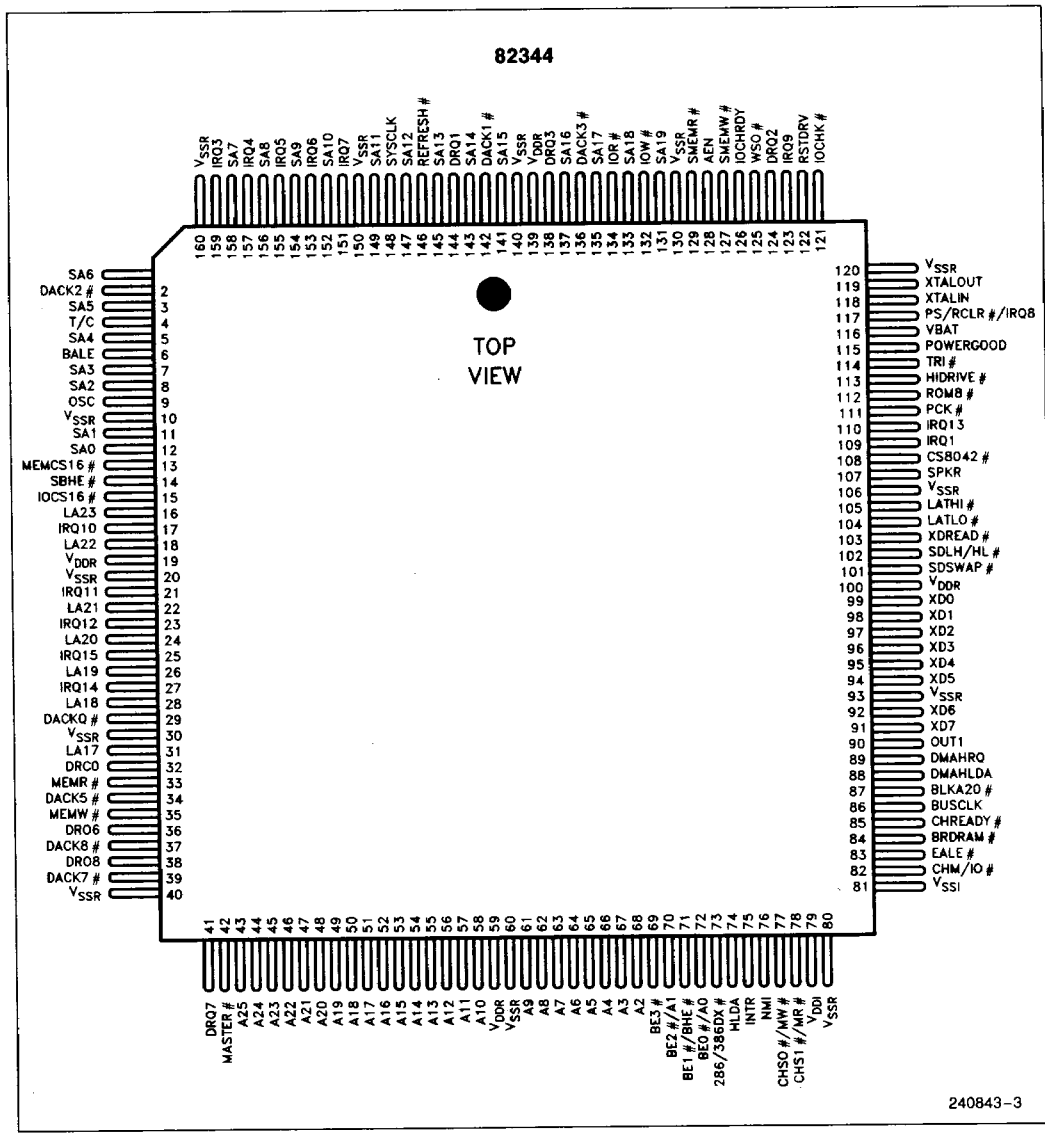
PERIPHERAL CONTROL BLOCK DIAGRAM




82344
TOP VIEW
1 SA6
2 DACK2 #
3 SA5
4 T/C
5 SA4
6 BALE
7 SA3
8 SA2
9 OSC
10 VSSR
11 SA1
12 SA0
13 MEMCS16 #
14 SBHE #
15 IOCS16 #
16 LA23
17 IRQ10
18 LA22
19 VDDR
20 VSSR
21 IRQ11
22 LA21
23 IRQ12
24 LA20
25 IRQ15
26 LA19
27 IRQ14
28 LA18
29 DACK0 #
30 VSSR
31 LA17
32 DRQ0
33 MEMR #
34 DACK5 #
35 MEMW #
36 DRQ6
37 DACK8 #
38 DRQ8
39 DACK7 #
40 VSSR
41 DRQ7
42 MASTER #
43 A25
44 A24
45 A23
46 A22
47 A21
48 A20
49 A19
50 A18
51 A17
52 A16
53 A15
54 A14
55 A13
56 A12
57 A11
58 A10
59 VDDR
60 VSSR
61 A9
62 A8
63 A7
64 A6
65 A5
66 A4
67 A3
68 A2
69 BE3 #
70 BE2 #/A1
71 BE1 #/BHE #
72 BE0 #/A0
73 286/386DX #
74 HLDA
75 INTR
76 NMI
77 CHSO #/MW #
78 CHS1 #/MR #
79 VDDI
80 VSSR
81 VSSI
82 CHM/IO #
83 EALE #
84 BRDRAM #
85 CHREADY #
86 BUSCLK
87 BLKA20 #
88 DMAHLDA
89 DMAHRQ
90 OUT1
91 XD7
92 XD6
93 VSSR
94 XD5
95 XD4
96 XD3
97 XD2
98 XD1
99 XD0
100 VDDR
101 SDSWAP #
102 SDLH/HL #
103 XDREAD #
104 LATLO #
105 LATHI #
106 VSSR
107 SPKR
108 CS8042 #
109 IRQ1
110 IRQ13
111 PCK #
112 ROM8 #
113 HIDRIVE #
114 TRI #
115 POWERGOOD
116 VBAT
117 PS/RCLR #/IRQ8
118 XTALIN
119 XTALOUT
120 VSSR
121 IOCHK #
122 RSTDRV
123 IRQ9
124 DRQ2
125 WSO #
126 IOCHRDY
127 SMEMW #
128 AEN
129 SMEMR #
130 VSSR
131 SA19
132 IOW #
133 SA18
134 IOR #
135 SA17
136 DACK3 #
137 SA16
138 DRQ3
139 VDDR
140 VSSR
141 SA15
142 DACK1 #
143 SA14
144 DRQ1
145 SA13
146 REFRESH #
147 SA12
148 SYSCLK
149 SA11
150 VSSR
151 IRQ7
152 SA10
153 IRQ6
154 SA9
155 IRQ5
156 SA8
157 IRQ4
158 SA7
159 IRQ3
160 VSSR
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SIGNAL DESCRIPTIONS

Name	Pin Number	Type	Description
CPU INTERFACE			
A25, A24	43–44	O-TS	Address Bus—These pins are outputs during DMA, master, or standard refresh modes. They are high impedance at all other times. A25 and A24 are driven from the alternate 612 registers during DMA and refresh cycles and are driven low during master cycles.
A23–A2	45–58, 61–68	IO-TTL	Address Bus—These pins are outputs during DMA, master, or standard refresh modes. They are inputs at all other times. As inputs, they are passed to the SA and LA buses and A15–A2 are used to address I/O registers internal to the bus control chip. As outputs, they are driven from different sources depending on which mode the Bus Controller is in. While in refresh mode, these pins are driven from the 612 and refresh address counter. While in DMA mode, they are driven from the 612 and DMA controller subsection. If the Bus Controller is in master mode, the pins A23–A17 are driven from the inputs LA23–LA17 and the pins A16–A2 are driven from the inputs SA16–SA2.
—BE3	69	IO-TTL	Byte Enable 3, active low—This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0 and —SBHE. As an output in 386DX mode SA1, SA0, and —SBHE are used to determine the value of —BE3. This pin should be left unconnected when using this part in 286 mode. The pin has an internal pull-up.
—BE2/A1	70	IO-TTL	Byte Enable 2, active low, or A1—This pin has a dual function depending on the state of the 286/–386DX input. If 286/–386DX is high (286 mode), then the pin is treated as address bit 1. If 286/–386DX is low (386DX mode), the pin is treated as —BE2. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386DX mode, it is decoded along with the other byte enable signals to generate SA1, SA0, and —SBHE. As an output in 386DX mode. SA1, SA0, and —SBHE are used to determine the value of —BE2. When in 286 mode, it is interpreted as address A1 and passed to SA1. As an output in 286 mode it is driven from the SA1 input.
—BE1/—BHE	71	IO-TTL	Byte Enable 1 or Byte High Enable, active low—This pin has a dual function depending on the state of the 286/—386DX input. If 286/—386DX is high (286 mode), then the pin is treated as —BHE. If 286/—386 is low (386 mode), the pin is treated as —BE1. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386 mode, it is decoded along with the other byte enable signals to generate SA1, SA0, and —SBHE. As an output in 386 mode, SA1, SA0, and —SBHE are used to determine the value of —BE1. When in 286 mode, it is interpreted as —BHE and passed to —SBHE. As an output in 286 mode, it is driven from the —SBHE input.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
CPU INTERFACE (Continued)			
—BE0/A0	72	IO-TTL	Byte Enable 0, active low, or A0—This pin has a dual function depending on the state of the 286/—386DX input. If 286/—386DX is high (286 mode), then the pin is treated as address bit 0. If 286/—386DX is low (386 mode), the pin is treated as —BE0. This pin is an output during DMA, master, or standard refresh modes. It is an input at all other times. As an input in 386 mode, it is decoded along with the other Byte Enable signals to generate SA1, SA0, and —SBHE. As an output in 386 mode, SA1, SA0, and —SBHE are used to determine the value of —BE0. When in 286 mode, it is interpreted as A0 and passed to SA0. As an output in 286 mode, it is driven from the SA0 input.
286/—386DX	73	I-TPU	CPU is 286 or 386DX—This pin defines the type of address bus to which the bus controller chip is interfaced. If the pin is tied high, the address bus is assumed to be emulating 286 signals. In this mode, A25, A24, and —BE3 would be left unconnected. The pins —BE2/A1, —BE1/—BHE and —BE0/A0 would take on the 286 functions. If the pin is tied low, A25, A24 can be used to generate up to 64 Mbyte addressing for DMA, and the byte enable pins will take on the normal 386DX addressing functions. This pin has an internal pull-up to cause the chip to default to 286 mode if left unconnected. This pin is a hard wiring option and must not be changed dynamically during operation. When strapped for 286 mode, the Bus Controller is assumed to be interfaced to the 82343 System Controller which in turn may be strapped for 286 or 386SX operation. The 82344 is strapped for 286 operation when used with the 82343 strapped for 386SX operation.
HLDA	74	I-TTL	Hold Acknowledge—This is the hold acknowledge pin directly from the CPU. It is used to control direction on address and command pins. When HLDA is low, the Bus Controller is defined as being in the CPU mode. In the CPU mode, the local address bus (A bus) pins are inputs. The system address bus (SA and LA) pins along with the command pins (—MEMR, —MEMW, —IOR and —IOW) are outputs. When HLDA is high, the Bus Controller can be in DMA, refresh, or master modes. In both DMA and refresh modes, the commands and all address buses (A, SA and LA) are outputs. In master mode, the commands and system address bus (SA and LA) pins are inputs and the local address bus (A bus) pins are outputs. The SA bus is passed directly to the A bus except bits 17, 18, and 19 are ignored. LA23–LA17 is passed directly to A23–A17.
INTR	75	O	Interrupt Request—INTR is used to interrupt the CPU and is generated by the 8259 megacells any time a valid interrupt request input is received.
NMI	76	O	Non-Maskable Interrupt—This output is used to drive the NMI input to the CPU. This signal is asserted by either a parity error (indicated by —PCK being asserted after the ENPARCK bit in Port B has been asserted), or an I/O channel error (indicated by —IOCHCK being asserted after the ENIOCK bit in Port B has been asserted). The NMI output is enabled by writing a 0 to bit D7 of I/O port 70h. NMI is disabled on reset.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
SYSTEM CONTROLLER INTERFACE			
—CHS0/—MW	77	IO-TTL	Channel Status 0 or active low Memory Write—This input is used along with —CHS1 and CHM/—IO to determine what type of bus cycle the Bus Controller is to perform. This input has the same meaning and timing requirements as the S0 signal for a 286 microprocessor. —CHS0 going active indicates a write cycle unless —CHS1 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the System Controller. It is then a —MEMW signal for DMA or bus master access to system memory.
—CHS1/—MR	78	IO-TTL	Channel Status 1 or active low Memory Read—This input is used along with —CHS0 and CHM/—IO to determine the bus cycle type. This input has the same meaning and timing requirements as the S1 signal for a 286 microprocessor —CHS1 going active indicates a read cycle unless —CHS0 is also active. When both status inputs are active it indicates an interrupt acknowledge cycle. This input is synchronized to the BUSCLK input. Activation of CPUHLDA reverses this signal to become an output to the System Controller. It is then a —MEMR signal for DMA or bus master access to system memory.
CHM/—IO	82	I-TTL	Channel Memory or active low I/O select—This input is used along with —CHS0 and —CHS1 to determine the bus cycle type. This input has the same meaning and timing requirements as the M/—IO signal for a 286 microprocessor. CHM/—IO is sampled anytime —CHS0 or —CHS1 is active. If sampled high, it indicates a memory read or write cycle. If sampled low, an I/O read or write cycle should be executed. This input is synchronized to the BUSCLK input.
—EALE	83	I-TTL	Early Address Latch Enable, active low—This input is used to latch the A25–A2 and Byte Enable signals. The latches are open when —EALE is low and hold their value when —EALE is high. The latched addresses are fed directly to the LA23–LA17 bus to provide more address setup time on the bus before a command goes active. The lower latched addresses are latched again with an internal ALE signal as soon as —CHS0 or —CHS1 is sampled active and fed to the SA19–SA0 and —SBHE outputs. In a 386DX system, this input is connected directly to the —ADS output from the CPU. In a 286 system, this input is connected to the —EALE output from the 82343 System Controller.
—BRDRAM	84	I-TTL	On-board DRAM, active low—An input from the System Controller indicating that the on-board DRAM is being addressed.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
SYSTEM CONTROLLER INTERFACE (Continued)			
—CHREADY	85	O	Channel Ready, active low—This output is maintained in the active state when no bus accesses are active. This indicates that the Bus Controller is ready to accept a new command. During normal bus accesses, —CHREADY is negated as soon as a valid bus requested is sampled on the —CHS0 and —CHS1 inputs. It is asserted again to indicate that the Bus Controller is ready to complete the current cycle. The bus command signals are then terminated on the next falling edge of the BUSCLK input.
BUSCLK	86	I-CMOS	Bus Clock—This is the main clock input for the Bus Controller. It runs at twice the frequency desired for the SYSCLK output. All inputs are synchronous with the falling edge of this input.
—BLKA20	87	I-TTL	Block A20, active low—This input is used while CPUHLDA is low to force the LA20 and SA20 outputs low anytime it is active. When —BLKA20 is negated LA20 and SA20 are generated from A20.
DMAHRQ	89	O	Hold Request—This output is generated by the DMA controller any time a valid DMA request is received. It is connected to the DMAHRQ pin on the System Controller.
DMAHLDA	88	I-TTL	DMA Hold Acknowledge—An input from the System Controller which indicates that the current hold acknowledge state is for the DMA controller or other bus master.
OUT1	90	O	Output 1—Indicates a refresh request to the System Controller. This is the 15 μs output of timer channel 1.
ROM INTERFACE			
—ROM8	112	I-TPU	8/16 bit ROM select—This input indicates the width of the ROM BIOS. If —ROM8 is low, the Bus Controller chip generates 8- to 16-bit conversions for ROM accesses. Data buffer controls are generated assuming the ROM is on the MD bus. If —ROM8 is high, data buffer controls are generated assuming 16-bit wide ROMs are on the MD bus.
BUS INTERFACE			
—IOR	134	IO-TTL	I/O Read, active low—This signal is an input when CPUHLDA is high and —MASTER is low. It is an output at all other times. When CPUHLDA is low, —IOR is driven from the 288 bus controller megacell. When CPUHLDA is high and —MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10 KΩ pull-up resistor.
—IOW	132	IO-TTL	I/O Write, active low—This signal is an input when CPUHLDA is high and —MASTER is low. It is an output at all other times. When CPUHLDA is low, —IOW is driven from the 288 bus controller megacell. When CPUHLDA is high and —MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10 KΩ pull-up resistor.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
BUS INTERFACE (Continued)			
—MEMR	33	IO-TTL	Memory Read, active low—This signal is an input when CPUHLDA is high and —MASTER is low. It is an output at all other times. When CPUHLDA is low, —MEMR is driven from the 288 bus controller megacell. When CPUHLDA is high and —MASTER is high, it is driven by the 8237 DMA controller megacells. This signal does not pulse low for DMA addresses above 16 Mbytes. DMA above 16 Mbytes is only performed to the system board, never to the slot bus. This pin requires an external 10 KΩ pull-up resistor.
—MEMW	35	IO-TTL	Memory Write, active low—This signal is an input when CPUHLDA is high and —MASTER is low. It is an output at all other times. When CPUHLDA is low, —MEMW is driven from the 288 bus controller megacell. When CPUHLDA is high and —MASTER is high, it is driven by the 8237 DMA controller megacells. This pin requires an external 10 KΩ pull-up resistor.
—SMEMR	129	IO-TTL	Memory Read, active low—This signal is an input when CPUHLDA is high and —MASTER is low. It is an output at all other times. When CPUHLDA is low, —MEMR is driven from the 288 bus controller megacell. When CPUHLDA is high and —MASTER is high, it is driven by the 8237 DMA controller megacells. —SMEMR is active on memory read cycles to addresses below 1 Mbyte. This pin requires an external 10 KΩ pull-up resistor.
—SMEMW	127	IO-TTL	Memory Write, active low—This signal is an input when CPUHLDA is high and —MASTER is low. It is an output at all other times. When CPUHLDA is low, —MEMW is driven from the 288 bus controller megacell. When CPUHLDA is high and —MASTER is high, it is driven by the 8237 DMA controller megacells. —SMEMW is active on memory write cycles to addresses below 1 Mbyte. This pin requires an external 10 KΩ pull-up resistor.
LA23–LA17	16, 18, 22, 24, 26, 28, 31	IO-TTL	Latchable Address bus—This bus in an input when CPUHLDA is high and —MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the LA bus is driven by the latched values for the A bus. When CPUHLDA is high and —MASTER is high, the SA bus is driven by the 612 memory mapper for DMA cycles and normal refresh. The LA bus is latched internally with the —EALE input.
SA19–SA0	131, 133, 135, 137, 141, 143, 145, 147, 149, 152, 154, 156, 158, 1, 3, 5, 7, 8, 11, 12	IO-TTL	System Address bus—This bus is an input when CPUHLDA is high and —MASTER is low. It is an output bus at all other times. When CPUHLDA is low, the SA bus is driven by the latched values from the A bus. When CPUHLDA is high and —MASTER is high, the SA bus is driven by the 8237 DMA controller megacells or refresh address generator. The SA bus will become valid in the middle of the status cycle generated by the —CHS0 and —CHS1 inputs. They are latched with an internally generated ALE signal.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
BUS INTERFACE (Continued)			
—SBHE	14	IO-TTL	System Byte High Enable, active low—This pin is controlled the same way as the SA bus. It is generated from a decode of the —BE inputs in CPU mode. It is forced low for 16-bit DMA cycles and forced to the opposite value of SA0 for 8-bit DMA cycles.
—REFRESH	146	IT-OD	Refresh signal, active low—This I/O signal is pulled low whenever a decoupled refresh command is received from the System Controller. It is used as an input to sense refresh requests from external sources such as the System Controller for coupled refesh cycles or bus masters. It is used internally to clock the refresh address counter and select a location in the memory mapper which drives A23–A17. —REFRESH is an open drain output capable of sinking 24 mA and requires an external pull-up resistor.
SYSCLK	148	O	System Clock—This output is half the frequency of the BUSCLK input. The bus control outputs BALE and the —IOR, —IOW, —MEMR and —MEMW are synchronized to SYSCLK.
OSC	9	I-TTL	Oscillator—This is the buffered input of the external 14.318 MHz oscillator.
RSTDRV	122	O	Reset Drive, active high—This output is a system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSCLK input.
BALE	6	O	Buffered Address Latch Enable, active high—A pulse which is generated at the beginning of any bus cycle initiated from the CPU. BALE is forced high anytime CPUHLDA is high.
AEN	128	O	Address Enable—This output goes high anytime the inputs CPUHLDA and —MASTER are both high.
T/C	4	O	Terminal Count—This output indicates that one of the DMA channels terminal count has been reached. This signal directly drives the system bus.
—DACK7- —DACK5, —DACK3- —DACK0	39, 37, 34, 136, 2, 142, 29	O	DMA Acknowledge, active low—These outputs are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is set active low on reset. Since the 8237 megacells are internally cascaded together, the polarity of the —DACK signals must not be changed. This signal directly drives the system bus.
DRQ7–DRQ5 DRQ3–DRQ0	41, 38, 36, 138, 124, 144, 32	I-TSPU	DMA Request—These asynchronous inputs are used by an external device to indicate when they need service from the internal DMA controllers. DRQ0–DRQ3 are used for transfers from 8-bit I/O adapters to/from system memory. DRQ5–DRQ7 are used for transfers from 16-bit I/O adapters to/from system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together. All DRQ pins have internal pull-ups.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
BUS INTERFACE (Continued)			
IRQ15–IRQ9, IRQ7–IRQ3, IRQ1	25, 27, 110, 23, 21, 17, 123, 151, 153, 155, 157, 159, 109	I-TPSU	Internal Request—These are the asynchronous interrupt request inputs for the 8259 megacells. IRQ0, IRQ2, and IRQ8 are not available as external inputs to the chip, but are used internally. IRQ0 is connected to the output of the 8254 counter 0. IRQ2 is used to cascade the two 8259 megacells together. IRQ8 is output from the RTC megacell to the 8259 megacell. All IRQ input pins are active high and have internal pull-ups.
—MASTER	42	I-TTL	Master, active low—This input is used by an external device to disable the internal DMA controllers and get access to the system bus. When asserted it indicates that an external bus master has control of the bus.
—MEMCS16	13	I-TTL	Memory Chip Select 16-bit—This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System Controller requests a 16-bit memory cycle and —MEMCS16 is sampled high.
—IOCS16	15	I-TTL	I/O Chip Select 16-bit—This input is used to determine when a 16-bit to 8-bit conversion is needed for CPU accesses. A 16 to 8 conversion is done anytime the System Controller requests a 16-bit I/O cycle and —IOCS16 is sampled high.
—IOCHK	121	I-TTL	I/O Channel Check, active low—This input is used to indicate that an error has taken place on the I/O bus. If I/O checking is enabled, an —IOCHK assertion by a peripheral device generates an NMI to the processor. The state of the —IOCHK signal is read as data bit D6 of the Port B register.
IOCHRDY	126	I-TTL	I/O Channel Ready—This input is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles intiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data, or strobe-in write data in this amount of time must use —IOCHRDY to extend these cycles.
—WS0	125	I-TTL	Wait State 0, active low—This input is pulled low by a peripheral on the S bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWERGOOD	115	I-TSPU	System power on reset—This input signals that power to the board is stable. A Schmitt-trigger input is used. This allows the input to be connected directly to an RC network.
PERIPHERAL INTERFACE			
—CS8042	108	O	Chip select for 8042. This output is active any time an SA address is decoded at 60h or 64h. It is intended to be connected to the chip select of the keyboard controller. If BUSCTL[6] = 1, this pin is also active for RTC accesses at 70h and 71h. This is for use when the internal RTC is disabled and an external RTC is used.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
PERIPHERAL INTERFACE (Continued)			
XTALIN	118	I-CMOS	Crystal Input—An internal oscillator input for the real time clock crystal. It requires a 32.768 KHz external crystal or stand-alone oscillator.
XTALOUT	119	O	Crystal Output—An internal oscillator output for the real time clock crystal. See XTALIN. This pin is a no connect when an external oscillator is used.
PS/—RCLR/ IRQ8	117	I-TSPU	The Power Sense input (active high) is used to reset the status of the Valid RAM and Time (VRT) bit. This bit is used to indicate that the power has failed, and that the contents of the RTC may not be valid. This pin is connected to an external RC network. When BUSCTL[6] = 1, this pin becomes —IRQ8 input for use with an external RTC.
VBAT	116	I	Voltage Battery—Connected to the RTC hold-up battery between 2.4 and 5V.
SPKR	107	O	Speaker—This output drives an externally buffered speaker. This signal is created by gating the output of timer 2. Bit 1 of Port B, 61H, is used to enable the speaker output, and bit 0 is used to gate the output timer.
DATA BUFFER INTERFACE			
XD7–XD0	91, 92, 94–99	IO-TTL	Peripheral data bus—The bidirectional X data bus outputs data on an INTA cycle or I/O read cycle to any valid address within the Bus Controller. It is configured as an input at all other times.
—SDSWAP	101	O	System Data Swap, active low during some 8-bit accesses—It indicates that the data on the SD bus must be swapped from low byte to high byte or vice versa depending on the state of the SDLH/—HL pin. —SDSWAP is active for 8-bit DMA cycles when an odd address access occurs for data more than one byte wide. For non-DMA accesses. —SDSWAP is active for any bus cycle to an 8-bit peripheral that is addressing the odd byte.
SDLH/—HL	102	O	System Data Low to High, or High to Low—This signal is used to determine which direction data bytes must be swapped when —SDSWAP is active. When SDLH/—HL is high, it indicates that data on the low byte must be transferred to the high byte. When SDLH/—HL is low, it indicates that data on the high byte must be transferred to the low byte. SDLH/—HL is low for 8-bit DMA memory read cycles. For non-DMA accesses, SDLH/—HL is low for any memory write or I/O write when —SBHE is low. SDLH/—HL is high at all other times.
—XDREAD	103	O	Peripheral Data Read—This output is active low any time an INTA cycle occurs or an I/O read occurs to the address space from 0000h to 00FFh, which is defined as being resident on the peripheral bus.

SIGNAL DESCRIPTIONS (Continued)

Name	Pin Number	Type	Description
DATA BUFFER INTERFACE (Continued)			
—LATLO	104	O	Latch Low byte—This output is generated for all I/O read and memory read bus accesses to the low byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and Bus Controller.
—LATHI	105	O	Latch High byte—This output is generated for all I/O read and memory read bus accesses to the high byte. It is active with the same timing as the read command and returns high at the same time as the read command. This signal latches the data into the data buffer chip so that it can be presented to the CPU at a later time. This step is required due to the asynchronous interface between the System Controller and Bus Controller.
—PCK	111	I-TPU	Party Check input, active low with pull-up—Indicates that a parity error has occurred in the on-board memory array. Assertion of this signal (if enabled) generates an NMI to the processor. The state of the —PCK signal is read as data bit D7 of the Port B register.
—HIDRIVE	113	I-TPU	High Drive Enable—This pin is a wire strap option. When this input is low, all bus drivers defined with an IOL spec of 24 mA will sink the full 24 mA of current. When this input is high, all pins defined as 24 mA have the output low drive capability cut in half to 12 mA. Note that all AC specifications are done with the outputs in the high drive mode and a 200 pF capacitive load —HIDRIVE has an internal pull-up and can be left unconnected if 12 mA drive is desired. It is tied low if 24 mA drive is desired.
TEST MODE PIN			
—TRI	114	I-TPU	Three-state—This pin is used to control the three-state drive of all outputs and bidirectional pins on the chip. If this pin is pulled low, all pins on the chip except XTALOUT are in a high impedance mode. This is useful during system test when test equipment or other chips drive the signals or for hardware fault tolerant applications. —TRI has an internal pull-up.
POWER AND GROUND PINS The power connections are split into an internal supply for the core-logic, and a pad-ring supply for the I/O drivers. Each supply should be individually bypassed wih decoupling capacitors.			
VDDR	19, 59, 100, 139	PWR	Pad-ring power connection, nominally + 5V. These pins along with the VSSR pins should be separately bypassed.
VSSR	10, 20, 30, 40, 60, 80, 93, 106, 120, 130, 140, 150, 160	GND	Pad-ring ground connection, nominally 0V. These pins along with the VDDR pins should be separately bypassed.
VDDI	79	PWR	Internal core-logic power connection, nominally + 5V. This pin along with the VSSI pin should be separately bypassed.
VSSI	81	GND	Internal core-logic ground connection, nominally 0V. This pin along with the VDDI pin should be separately bypassed.

Signal Type Legend

Signal Code	Signal Type
I-TTL	TTL Level Input
I-TPD	Input with 30 KΩ Pull-Down Resistor
I-TPU	Input with 30 KΩ Pull-Up Resistor
I-TSPU	Schmitt-Trigger Input with 30 KΩ Pull-Up Resistor
I-CMOS	CMOS Level Input
IO-TTL	TTL Level Input/Output
IT-OD	TTL Level Input/Open Drain Output
IO-OD	Input or Open Drain, Slow Turn On
O	CMOS and TTL Level Compatible Output
O-TTL	TTL Level Output
O-TS	Three-State Level Output
I1	Input used for Testing Purposes
GND	Ground
PWR	Power