82343
SYSTEM CONTROLLER/DATA BUFFER

The 82343 contains the system control and data buffering functions in a 160-pin quad flatpack.

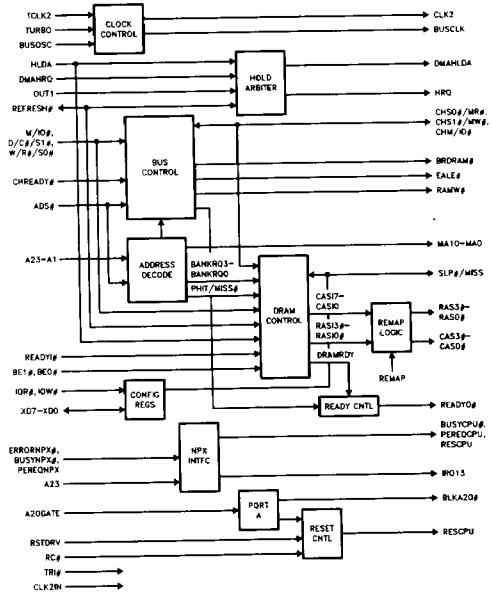
The 82343's functions are highly programmable via a set of internal configuration registers. Defaults on reset for the configuration registers mimic the compatibility requirements of the original IBM PC/AT* as closely as possible. The power-up defaults allow any possible configuration of the system to boot at the CPU's rated speed. However, operational capabilities may be temporarily reduced until the configuration registers are set to mirror the true system configuration. This normally occurs during BIOS power-on self-test in a manner completely transparent to the user.

The 82343 is designed to perform in systems running up to 20 MHz. Built-in page-mode operation, two- or four-way interleaving, and fully programmable memory timing allow the PC designer to maximize system performance using low cost DRAMs. Programmable memory timing allows the system to be setup to perfectly match the requirements of the chosen DRAMs; standard or custom. These adjustments can often be made without incurring the penalty of additional wait states.

The system controller handles system board refresh directly and also controls the timing of slot bus refresh which is actually performed by the 82344 ISA Bus Controller. Refresh may be performed in coupled or decoupled mode. The former method is the standard PC/AT-compatible mode where on- and off-board refreshes are performed synchronously. In decoupled mode, the timing of on- and off-board refreshes is independent. Both may be programmed for independent, slower than normal rates. This allows use of low power, slow refresh DRAMs. The 82343 controls all timing in both modes. In all cases, refreshes are staggered to minimize power supply loading and attendant noise on the V_{DD} and ground pins. In sleep mode, refresh switches to CAS# before RAS# refresh for maximum power savings.

The physical banks of DRAM can be logically reordered through one of the indexed configuration registers. This DRAM remap option is useful in order to map out bad DRAM banks allowing continued use of a system until repairs are convenient. It also allows DRAM bank combinations not in the supported memory maps to be logically moved into a supported configuration without physically moving memory components. This unique, programmable function

Block Diagram



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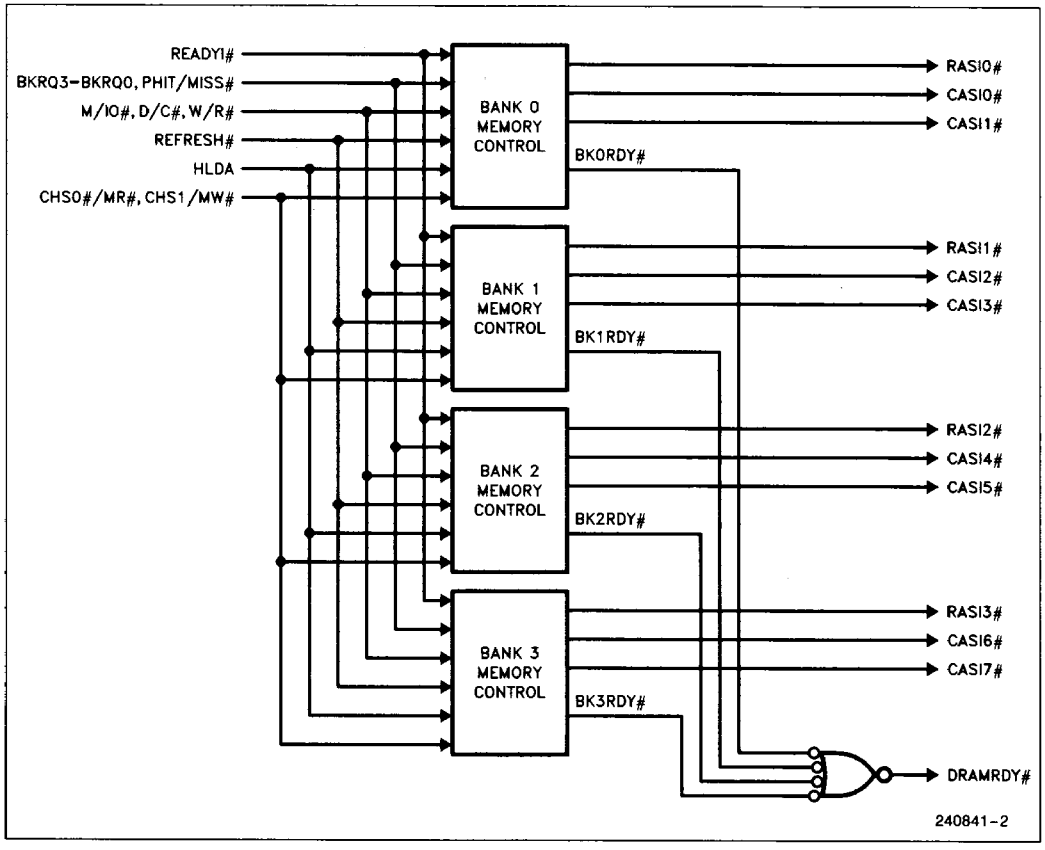
performs this task by switching the internal RAS# and CAS# signals between the external RAS# and CAS# pins. This allows internal row and column addresses generated for DRAM bank 0, for example, to be routed to any one of the four on-board DRAM banks.

Full EEMS support is provided in hardware for the complete LIM EMS 4.0 standard. Seventy-two mapping registers provide a standard and an alternate set of 36 registers each. The system allows backfill down to 256k for EEMS support and provides 24 mapping registers covering this space. Twelve of the 36 are page registers which cover the EMS space from C0000h to E0000h. These twelve registers can alternatively be mapped in the A0000–BFFFFh and D0000–DFFFFh range by changing a configuration bit in the 82343. All registers are capable of translating over the complete 32 Mbyte range of on-board DRAM. Users preferring an alternate plug-in EMS solution, can disable the on-board EMS system as well as system board DRAM, as required, down to 256k.

Shadowing features are supported on all 16k boundaries between 640k and 1M. Simultaneous EMS use, shadowed ROM, and direct system board access is possible in non-overlapping fashion throughout this memory space. Control over four access options is provided.

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow setup mode. Read ROM or slot bus, write system board DRAM.

These controls are overridden by EMS in segments for which it is enabled.

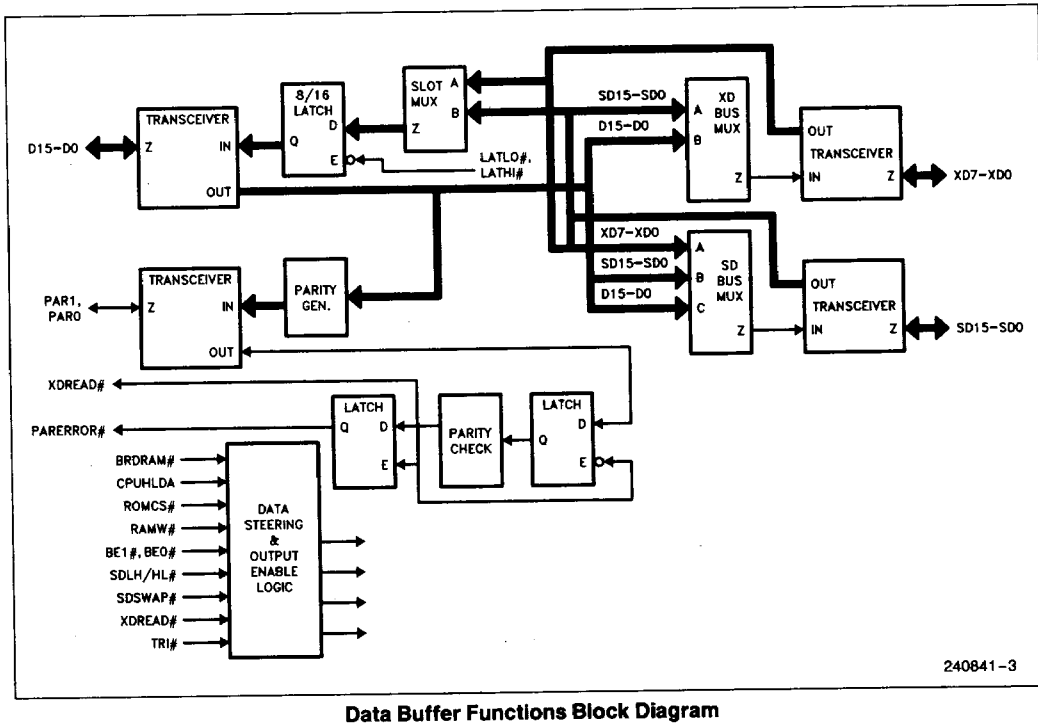


Memory Controller Block Diagram

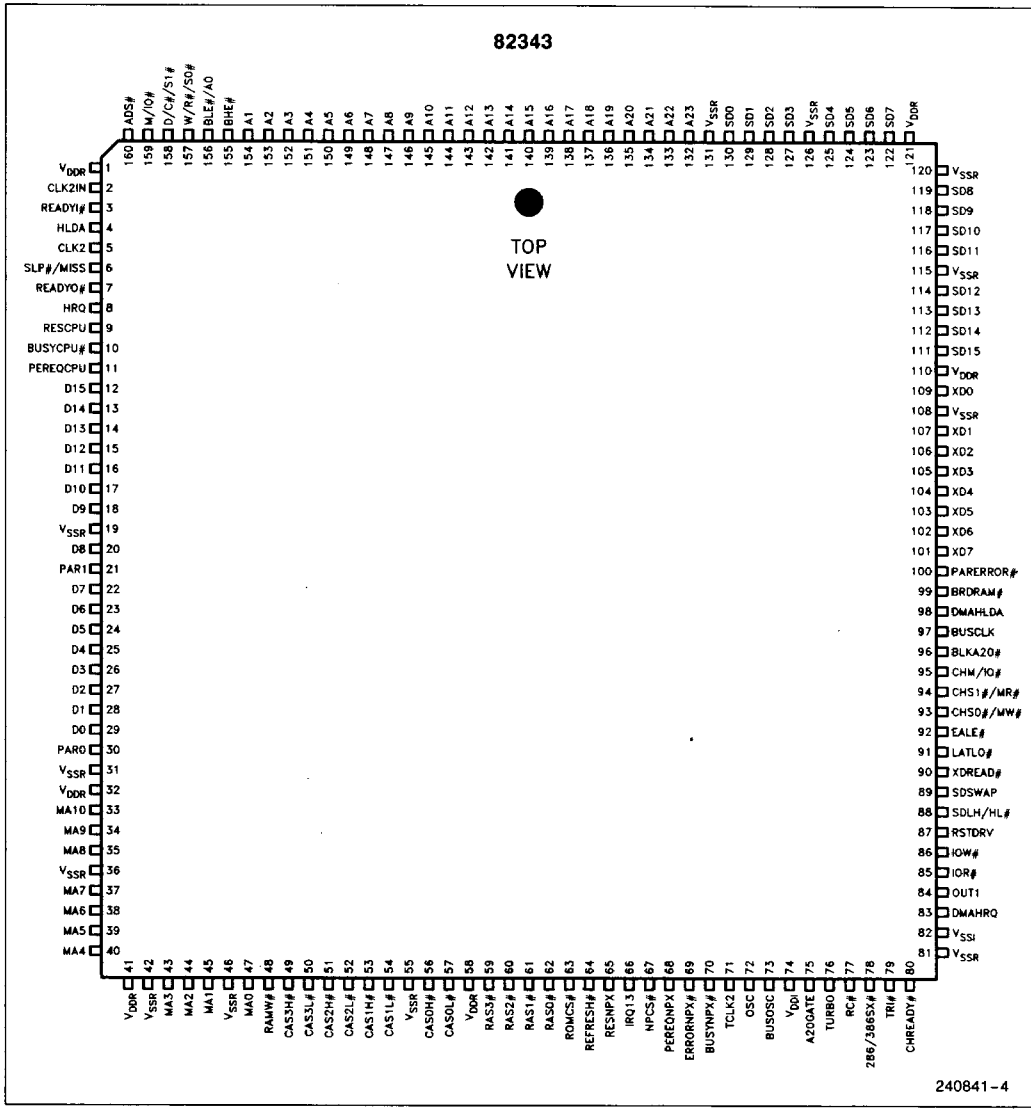
The System Controller is used to program the desired operational mode of the AT bus. Based on this programming, it provides the bus clock and signalling interface to the Bus Controller. The bus may run synchronously with the CPU's CLK2 or asynchronously via an external oscillator. A programmable divider conditions the selected BUSCLK source providing divide by 1, 2, 3 or 4.

The 82343 also performs all of the data buffering functions required for a 386™SX-based PC/AT-compatible system. Under the control of the CPU, the data buffer chip routes data to and from the CPU's D bus, XD bus, and slots (SD bus). The parity is checked for D bus DRAM read operations. When reading from ROM, the XD bus or the SD bus, the data can be converted from 8 bits wide to 16. The data is latched for synchronization with the CPU. Parity is generated for all data written to the D bus. The 82343 provides the data conversion necessary for 16-bit writes to 8-bit devices on the XD or SD buses.

Under the control of DMA or a bus master, the 82343 allows 8- or 16-bit data to be routed to and from the XD bus. The chip also is capable of performing high to low and low to high byte swaps on the SD bus. For transfers between two peripherals on the slot bus the outputs of the 82343 are disabled. The chip also provides the feature of a single input, TRI#, to disable all of its outputs for board level testability.



Data Buffer Functions Block Diagram


82343
TOP
VIEW
1 VDDR
2 CLK2IN
3 READYI#
4 HLDA
5 CLK2
6 SLP#/MISS
7 READYO#
8 HRQ
9 RESCPU
10 BUSYCPU#
11 PEREQCPU
12 D15
13 D14
14 D13
15 D12
16 D11
17 D10
18 D9
19 VSSR
20 D8
21 PAR1
22 D7
23 D6
24 D5
25 D4
26 D3
27 D2
28 D1
29 D0
30 PAR0
31 VSSR
32 VDDR
33 MA10
34 MA9
35 MA8
36 VSSR
37 MA7
38 MA6
39 MA5
40 MA4
41 VDDR
42 VSSR
43 MA3
44 MA2
45 MA1
46 VSSR
47 MA0
48 RAMW#
49 CAS3H#
50 CAS3L#
51 CAS2H#
52 CAS2L#
53 CAS1H#
54 CAS1L#
55 VSSR
56 CAS0H#
57 CAS0L#
58 VDDR
59 RAS3#
60 RAS2#
61 RAS1#
62 RAS0#
63 ROMCS#
64 REFRESH#
65 RESNPX
66 IRQ13
67 NPCS#
68 PEREQNPX
69 ERRORNPX#
70 BUSYNPX#
71 TCLK2
72 OSC
73 BUSOSC
74 VDDI
75 A20GATE
76 TURBO
77 RC#
78 286/386SX#
79 TRI#
80 CHREADY#
81 VSSR
82 VSSI
83 DMAHRQ
84 OUT1
85 IOR#
86 IOW#
87 RSTDRV
88 SDLH/HL#
89 SDSWAP
90 XDREAD#
91 LATLO#
92 EALE#
93 CHS0#/MW#
94 CHS1#/MR#
95 CHM/IO#
96 BLKA20#
97 BUSCLK
98 DMAHLDA
99 BRDRAM#
100 PARERROR#
101 XD7
102 XD6
103 XD5
104 XD4
105 XD3
106 XD2
107 XD1
108 VSSR
109 XD0
110 VDDR
111 SD15
112 SD14
113 SD13
114 SD12
115 VSSR
116 SD11
117 SD10
118 SD9
119 SD8
120 VSSR
121 VDDR
122 SD7
123 SD6
124 SD5
125 SD4
126 VSSR
127 SD3
128 SD2
129 SD1
130 SD0
131 VSSR
132 A23
133 A22
134 A21
135 A20
136 A19
137 A18
138 A17
139 A16
140 A15
141 A14
142 A13
143 A12
144 A11
145 A10
146 A9
147 A8
148 A7
149 A6
150 A5
151 A4
152 A3
153 A2
154 A1
155 BHE#
156 BLE#/A0
157 W/R#/S0#
158 D/C#/S1#
159 M/IO#
160 ADS#
240841-4

Pin Diagram

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS			
A23–1	132–154	I-TTL	**ADDRESS BITS 23 THROUGH 1:** Driven by the CPU when the CPU is bus master. They are driven by the Bus Controller whenever HLDA is active. These bits allow direct access of up to 16 Mbytes of local memory.
BHE#	155	I-TTL	**BYTE HIGH ENABLE, ACTIVE LOW:** This signal is driven by the CPU or the 82344. It is used to select the upper byte of a 16-bit wide memory location.
BLE#/A0	156	I-TTL	**BYTE LOW ENABLE, ACTIVE LOW, OR A0:** In 386SX mode this signal is BLE#, in 286 mode it is A0 and is driven by the CPU or the Bus Controller. It is used to select the lower byte of a 16-bit wide memory location.
W/R#/S0#	157	I-TPU	**WRITE OR ACTIVE LOW READ ENABLE, OR S0:** W/R# is driven by the CPU in 386SX mode, S0# in 286 mode. This signal is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. The bus cycle types include interrupt acknowledge, halt shutdown, I/O reads and writes, memory data reads and writes, and memory code reads. This pin is pulled up internally.
D/C#/S1#	158	I-TPU	**DATA OR ACTIVE LOW CODE ENABLE, OR S1:** D/C# is driven by the CPU in 386SX mode or S1# in 286 mode. This signal is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. See W/R#/S0# definition for bus cycle types. This pin is pulled up internally.
M/I#/O	159	I-TPU	**MEMORY OR ACTIVE LOW I/O ENABLE:** Driven by the CPU, M/IO# is decoded with the remaining CPU control signals to indicate the type of bus cycle requested. See W/R#/S0# definition for bus cycle types. This pin is pulled up internally.
ADS#	160	I-TPU	**ADDRESS STROBE, ACTIVE LOW:** This signal is driven by the 386SX as an indicator that the address and control signals currently supplied by the CPU are valid. It is used internally to indicate that the data and command are valid and determine the beginning of a memory cycle. This pin is a no connect in 286 mode. An internal pull up resistor keeps it inactive during 286 mode.
CLK2IN	2	I-CMOS	This is the main clock input to the System Controller and it should be connected to the CLK2 signal that is output by the System Controller. This signal is used internally to clock the System Controller logic.
TCLK2	71	I-TTL	This input is connected to a crystal oscillator whose frequency is equal to two times the system frequency. The TTL level oscillator output is converted internally to CMOS levels and sent to the CLK2 output.
CLK2	5	O	This output signal is CMOS level converted TCLK2 signal. It is output to the CPU and other on-board logic for synchronization.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS (Continued)			
SLP#/MISS	6	IO−od	As a "power on reset" default this bit is an output that reflects the inverse state of the SLEEP[7] configuration register bit. It is active low when sleep mode is active. Sleep mode is activated by setting SLEEP[7] = 1. When configuration register CTRL1[0] = 1 this pin becomes a MISS output for use with a future product.
READYO#	7	O	**READY OUT, ACTIVE LOW:** This signal is an indication that the current memory or I/O bus cycle is complete. It is generated from the internal DRAM controller or the synchronized version of CHREADY# for slot bus accesses. Outside the chip it is ORed with any other local bus I/O or master. The culmination of these ORed READY signals is sent to the CPU and is also connected to the System Controller's READYI# input.
READYI#	3	I-TTL	**READY INPUT, ACTIVE LOW:** This signal is the ORed READY signals from the coprocessor or other optional add-in devices and from the 82343's READY# input.
HLDA	4	I-TTL	**HOLD ACKNOWLEDGE, ACTIVE HIGH:** This signal is issued by the CPU in response to the HRQ driven by the System Controller. It indicates that the CPU is floating its outputs to the high impedance state, so that another master can take control of the bus. When HLDA is active, the memory control is generated from CHS1#/MR# and CHS0#/MW# rather than CPU status signals.
HRQ	8	O	**HOLD REQUEST, ACTIVE HIGH:** This output is driven by the System Controller to the CPU. It indicates that a master, such as a DMA or AT channel master, is requesting control of the bus. HRQ is a result of the DMAHRQ input or a coupled refresh cycle. It is synched to CLK2.
RESCPU	9	O	**RESET CPU, ACTIVE HIGH:** An output signal that is sent to the CPU by the System Controller. It is issued in response to the control bit for software reset located in the Port A register or a dummy read to IO port EFh. It is also issued in response to signals on the RSTDRV or RC inputs and in response to System Controller's detection of a shutdown command. In all cases it is synched to CLK2.
BUSYCPU#	10	O	**BUSY CPU, ACTIVE LOW:** An output signal that is sent to the CPU. The state of BUSYNPX# is always passed through to BUSYCPU# indicating that the NPX is processing a command. ON occurrence of an ERRORNPX# signal, it is latched and held active until occurrence of a write to ports F0h, F1h, or RESNPX. The former case is the normal mechanism used to reset the active latched signal. The latter two are resets. Since ERRORNPX# generates IRQ13 for PC/AT-compatibility, BUSYCPU# is held active to prevent software access of the coprocessor until the interrupt service routine writes F0h.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
CPU INTERFACE SIGNALS (Continued)			
PEREQCPU	11	O	**PROCESSOR EXTENSION REQUEST, ACTIVE HIGH:** An output signal sent to the CPU in response to a PEREQNPX which is issued by the coprocessor to the System Controller. It indicates to the CPU that the coprocessor is requesting a data operand to be sent to or from memory by the CPU. For PC/AT-compatibility PEREQCPU is returned active on occurrence of ERRORNPX# after BUSYNPX# has gone inactive. A write to F0h by the interrupt 13 handler returns control of the PEREQCPU signal to directly follow the PEREQNPX input.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
RAMW#	48	O	**RAM ACTIVE LOW WRITE/ ACTIVE HIGH READ:** This output to the DRAM memory is to control the direction of data flow of the on-board memory. It is a result of the address and bus control decode. It is active during memory write cycles and high at all other times.
MA10–MA0	33–35 37–40, 43–45, 47	O	**MEMORY ADDRESSES 10 THROUGH 0:** These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the CPU bus addresses. They allow addressing of up to 8 Mbytes per DRAM bank.
RASBK3# – RASBK0#	59–62	O	**ROW ADDRESS BANK 0 THROUGH 3, ACTIVE LOW:** These signals are sent to their respective RAM banks to strobe in the row address during on-board memory bus cycles. The active period for this signal is fully programmable.
CAS7# – CAS0#	49–54 56, 57	O	**COLUMN ADDRESS, STROBE, ACTIVE LOW:** These signals are sent to their respective RAM banks to strobe in the column address during on-board memory bus cycles. There is a CAS# signal for upper and lower bytes of each of the four 16-bit DRAM memory banks. The active period for this signal is completely programmable. For clarity, alternate names may also be used for these signals as shown in the following table where the digit in the "Alternate Name" indicates the DRAM bank the signal drives, L indicates it drives the low byte, and H indicates it drives the high byte. **Standard Name** — **Alternate Name** CAS0# — CAS0L# CAS1# — CAS0H# CAS2# — CAS1L# CAS3# — CAS1H# CAS4# — CAS2L# CAS5# — CAS2H# CAS6# — CAS3L# CAS7# — CAS3H#

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS (Continued)			
REFRESH#	64	I-CMOS/ O-OD	**REFRESH SIGNAL, ACTIVE LOW:** This output is used by the System Controller to initiate an off-board DRAM refresh operation in coupled refresh mode. In decoupled mode, the Bus Controller drives refresh active to indicate to the System Controller that it has decoded a refresh request command and is initiating an off-board refresh cycle.
ROMCS#	63	O	**ROM CHIP SELECT:** This output is active in CPU mode only (CPUHLDA is negated). It is active anytime the address on the A bus selects the address range between FF0000h–FFFFFFh during a memory read cycle. It is also active 0E0000h–0FFFFFh and between FE0000–FEFFFF when RAMMAP[7] = 1, the default condition. When RAMMAP[7] = 0, accesses in these two regions are directed to the slot bus. "Holes" can be opened in this lower decode range by activation of shadow or EMS windows in this region; i.e., when 16k shadow or EMS windows are activated in this region, ROMCS# is not generated.
COPROCESSOR SIGNALS			
PEREQNPX	68	I-TPD	**COPROCESSOR EXTENSION REQUEST, ACTIVE HIGH:** This input signal is driven by the coprocessor and indicates that it needs transfer of data operands to or from memory. For PC/AT-compatibility this signal is also gated with the internal ERROR/ BUSY control logic before being output to the CPU as PEREQCPU during NPX interrupts.
ERRORNPX#	69	I-TPU	**ERROR COPROCESSOR, ACTIVE LOW:** An input signal from the coprocessor indicating that an error has occurred in the previous instruction. This signal is internally gated and latched with BUSYNPX# to produce IRQ13.
BUSYNPX#	70	I-TPU	**BUSY COPROCESSOR, ACTIVE LOW:** An input signal that is driven by the coprocessor to indicate that it is currently executing a previous instruction and is not ready to accept another. This signal is decoded internally to produce IRQ13 and to control PEREQCPU.
RESNPX	65	O	**RESET COPROCESSOR:** This output is connected to the coprocessor reset input. It is triggered through an internally generated system reset or via a write to port F1h. In the case of a system reset, the CPURESET signal is also activated. Write to port F1h only resets the coprocessor. A software FNINT signal must occur after an F1h generated reset in a 386SX system, otherwise the 387SX is not initialized to the same state that a 287 is placed in by a hardware reset alone. For compatibility, the F1 reset may be disabled by setting bit 6 of the MISCSET register to 1.
IRQ13	66	O	**INTERRUPT REQUEST, ACTIVE HIGH:** This output is driven to the Bus Controller to indicate that an error has occurred within the coprocessor. This signal is decode of the BUSYNPX# and ERRORNPX# inputs.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
COPROCESSOR SIGNALS (Continued)			
NPCS#	67	O	**COPROCESSOR CHIP SELECT:** Provides decoding of the 287 coprocessor's I/O space. This is the entire F8h to FFh region when Zenith Data Systems-Special Features are disabled. When ZDS-SF are enabled, only I/O accesses to F8h, FAh, FCh, and FEh cause NPCS# to be active. This signal is a don't care pin for 387SX operation since the 386SX provides this function using A23.
BUS CONTROL SIGNALS			
CHREADY#	80	I-CMOS	**CHANNEL READY, ACTIVE LOW:** An input issued by the Bus Controller as an indication that the current channel bus cycle is complete. This signal is synchronized internally then combined with ready signals from the coprocessor and DRAM controller to form the final version of READYO# which is sent to the CPU.
CHS0#/MW#	93	IO-TTL	**CHANNEL SELECT 0 OR MEMORY WRITE, ACTIVE LOW:** This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with CHS1# and CHM/IO# and decoded, the bus cycle type is defined for the Bus Controller. Activation of CPUHLDA reverses this signal to become an input from the Bus Controller. It is then a MEMW# signal for the DMA or bus master to access system memory.
CHS1#/MR#	94	IO-TTL	**CHANNEL SELECT 1 OR MEMORY READ, ACTIVE LOW:** This signal is a decode of the CPU's bus control signals and is sent to the Bus Controller. When combined with CHS0# and CHM/IO# and decoded, the bus cycle type is defined for the Bus Controller. Activation of CPUHLDA reverses this signal to become an input from the Bus Controller. It is then a MEMR# signal for the DMA or bus master to access system memory.
CHM/IO#	95	O	**CHANNEL MEMORY I/O:** This signal is a decode of the M/IO# signal sent by the CPU to the System Controller. It is an indicator that the current bus cycle is a channel access. When combined with CHS0#, and CHM/IO# and decoded, the bus cycle type is defined for the Bus Controller.
BLKA20#	96	O	**BLOCK A20, ACTIVE LOW:** An output driven to the Bus Controller to deactivate address bit 20. It is a decode of the A20GATE signal and Port A bit 1 indicating the dividing line of the 1 Mbyte memory boundary. Port A bit 1 may be directly written or set by a dummy read of I/O port EEh. BLKA20# is forced high when HLDA is active.
BUSOSC	73	I-TTL	**BUS OSCILLATOR:** This signal is supplied from an external oscillator. It is supplied to the Bus Controller when the System Controller's internal configuration registers are set for asynchronous slot bus mode. This signal is two times the AT bus clock speed (SYSCLK).
BUSCLK	97	O	**BUS CLOCK:** This is the source clock used by the the Bus Controller to drive the slot bus. It is two times the AT bus clock (SYSCLK). It is programmable division from CLK2 or from an external oscillator when the System Controller is set up for a synchronous mode.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
BUS CONTROL SIGNALS (Continued)			
DMAHRQ	83	I-CMOS	**DMA HOLD REQUEST, ACTIVE HIGH:** This signal is an input sent by the Bus Controller. It is internally synchronized by the System Controller before it is sent out to the CPU by the HRQ signal. It is the indicator of the DMA controller or other bus master's desire to control the bus.
DMAHLDA	98	O	**DMA HOLD ACKNOWLEDGE:** An output sent to the Bus Controller which indicates that the current hold acknowledge state is for the DMA controller or other bus master.
BRDRAM#	99	O	**BOARD DRAM, ACTIVE LOW:** An output to Bus Controller and Data Buffer to indicate that on-board DRAM is being addressed.
EALE#	92	O	**EARLY ADDRESS LATCH ENABLE, ACTIVE LOW:** This output is sent to the Bus Controller in order latch the A23–A1 and byte enable signals. In 286 mode, this signal is generated internally by decode of the CPU status signals. In 386SX mode, the 82343's ADS# input is gated directly to the EALE# output.
OUT1	84	I-CMOS	Indicates a refresh request from the Bus Controller. This signal is provided by the 8254 megacell.
PERIPHERAL INTERFACE SIGNALS			
A20GATE	75	I-TTL	**ADDRESS BIT 20 ENABLE:** An input from the keyboard controller that is used internally along with Port A bit 1 to determine if address bit 20 from the CPU is true or gated low. It also determines the state of BLKA20#.
TURBO	76	I-TTL	**TURBO, ACTIVE HIGH:** This input to the System Controller determines the speed at which the system board operates. This input signal is normally the externally ANDed signal from the keyboard controller and a turbo switch. It is internally ANDed with a software settable latch. When high, operation is at full speed. When low, CLK2 is divided by the value coded in configuration register MISCSET. A range is provided that allows slow operation at, or below 8 MHz for any valid CPU speed. Slow speed takes precedence. When any one request for slow mode is present, slow mode is active. Turbo mode is active only when all TURBO requests are active.
RC#	77	I-TTL	**RESET CONTROL, ACTIVE LOW:** The falling edge of this signal causes a RESCPU signal. RC# is generated by the keyboard controller and its inverse is ORed with Port A bit 0 to form RESCPU.
BUS INTERFACE SIGNALS			
OSC	72	I-TTL	**OSCILLATOR:** This is the buffered input of the external 14.318 MHz oscillator.
IOR#	85	I-TTL	**I/O READ, ACTIVE LOW:** Driven by the Bus Controller to indicate to the System Controller that an I/O read cycle is occurring on the bus. Whenever an I/O cycle occurs, the memory interface signals are inactive.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
BUS INTERFACE SIGNALS (Continued)			
IOW#	86	I-TTL	**I/O WRITE, ACTIVE LOW:** Driven by the Bus Controller to indicate to the System Controller than an I/O write cycle is occurring on the bus. Whenever an I/O cycle occurs, the memory interface signals are inactive.
RSTDRV	87	I-TTL	**RESET DRIVE, ACTIVE HIGH:** This signal is output by the Bus Controller. It indicates that a hardware reset signal has been activated. This is the same signal which is output to the channel. This signal is used to reset internal logic and to derive the RESCPU which is output by the System Controller.
SDLH/HL#	88	I-TTL	**SYSTEM DATA BUS LOW TO HIGH/HIGH TO LOW SWAP:** This signal is driven by the Bus Controller. It is used to establish the direction of byte swaps. (Similar to DIR245 in the existing PC/AT-type chip sets.)
SDSWAP	89	I-TTL	**SYSTEM DATA BUS BYTE SWAP ENABLE:** This signal is driven by the Bus Controller. It is the qualifying signal needed for SDLH/HL#. (Used to be called GATE245 on the existing PC/AT-type chip sets.)
XDREAD#	90	I-TTL	**PERIPHERAL DATA BUS (XD BUS) READ:** This signal is driven by the Bus Controller and it determines the direction of the XD bus data flow. (It is analogous to the XDATADIR control pin on the existing PC/AT-type chip sets). When this signal is high, the XD Bus is output enabled.
LATLO#	91	I-TTL	**SD BUS LOW BYTE LATCH:** This signal is needed to latch the SD bus low byte to the local data bus until the CPU is ready to sample the bus. This signal is driven by the Bus Controller.
D15–D0	12–18, 20, 22–29	IO-TTL	**CPU DATA BUS:** This is the data bus directly connected to the CPU. It is also referred to as the local data bus.
SD15–0	111–114, 116–119, 122–125, 127–130	IO-TTL	**SYSTEM DATA BUS:** This bus connects directly to the slots. It is used to transfer data to/from local and system devices.
XD7–XD0	101–107, 109	IO-TTL	**PERIPHERAL DATA BUS:** This bus is connected to the Bus Controller and the System Controller. These I/O's are used to read and write to on-board 8-bit peripherals.
PAR1, PAR0	21, 30	IO-TTL	**PARITY BIT BYTES 1 AND 0:** These bits are generated by the parity generation circuitry. They are written to memory along with their corresponding bytes during memory write operations. During memory read operations, these bits become inputs and are used along with their respective data bytes to determine if a parity error has occurred.
PARERROR#	100	O	**PARITY ERROR, ACTIVE LOW:** This signal is the result of a parity check on the read from on-board memory.
286/386SX#	78	I-TPU	**286 OR 386SX MODE:** Tied high or left open to allow internal logic to switch to 286/287 compatibility mode. If grounded, the 82343 System Controller/Data Buffer switches into 386SX/387SX compatibility mode.

SIGNAL DESCRIPTIONS (Continued)

Signal Name	Pin Number	Signal Type	Signal Description
TEST MODE PIN			
TRI#	79	I1	**THREE-STATE:** This pin is used to drive all outputs to a high impedance state. When TRI# is low, all outputs and bidirectional pins are three-stated. TRI# is internally pulled up.
POWER AND GROUND PINS The power connections are split into an internal supply for the core-logic, and a pad-ring supply for the I/O drivers. Each supply should be individually bypassed with decoupling capacitors.			
VDDR	1, 32, 41, 110, 58, 121	PWR	Pad-ring power connection, nominally + 5V. These pins along with the VSSR pins should be separately bypassed.
VSSR	19, 31, 36, 42, 46, 55, 81, 108, 115, 120, 126, 131	GND	Pad-ring ground connection, nominally 0V. These pins along with the VDDR pins should be separately bypassed.
VDDI	74	PWR	Internal core-logic power connection, nominally + 5V. This pin along with the VSSI pin should be separately bypassed.
VSSI	82	GND	Internal core-logic ground connection, nominally 0V. This pin along with the VDDI pin should be separately bypassed.

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SIGNAL TYPE LEGEND

Signal Code	Signal Type	Signal Code	Signal Type
I-TTL	TTL Level Input	IO-OD	Input or Open Drain, Slow Turn On
I-TPD	Input with 30 kΩ Pull-Down Resistor	O	CMOS and TTL Level Compatible Output
I-TPU	Input with 30 kΩ Pull-Up Resistor	O-TTL	TTL Level Output
I-TSPU	Schmitt-Trigger Input with 30 kΩ Pull-Up Resistor	O-TS	Three-State Level Output
I-CMOS	CMOS Level Input	I1	Input Used for Testing Purposes
IO-TTL	TTL Level Input/Output	GND	Ground
IT-OD	TTL Level Input/Open Drain Output	PWR	Power