T-52-33-21

Headland Technology

HTK340
Shasta 486 Chip Set

Features

General
- Support for 486SX/DX/DX2 CPU
- 2 - 184 pin PQFP devices
- Local bus interface
- 16, 20, 25 and 33MHz CPU speeds
- Fully static operation
- Weitek 4167 supported
- System and Video BIOS on single ROM
- Uses 0.7 Micron HCMOS process

ISA Controller
- AT Compatible
- Syncronized 8MHz ISA bus
- Posted backplane memory writes
- 10 or 16 bit I/O mapping
- Integrated 8237s, 8259s and 8254 functionality
- Fast gate A20/Fast reset

Write Buffer
- 4 deep on-chip buffer
- Byte gathering
- Out of order operation
- Full or partial write buffer hits

DRAM Controller
- Line burst capability from DRAM to 80486
- 256K/1M/4M/16M DRAMs
- Mixed memory types
- EMS 4.0
- Hidden refresh operation
- 256MB Maximum system memory
- Staggered refresh
- Shadowing in 16KB increments between 640KB and 1MB
- Remapping
- Fast paging
- 2 or 4 way interleaving

HTK340 System Block Diagram

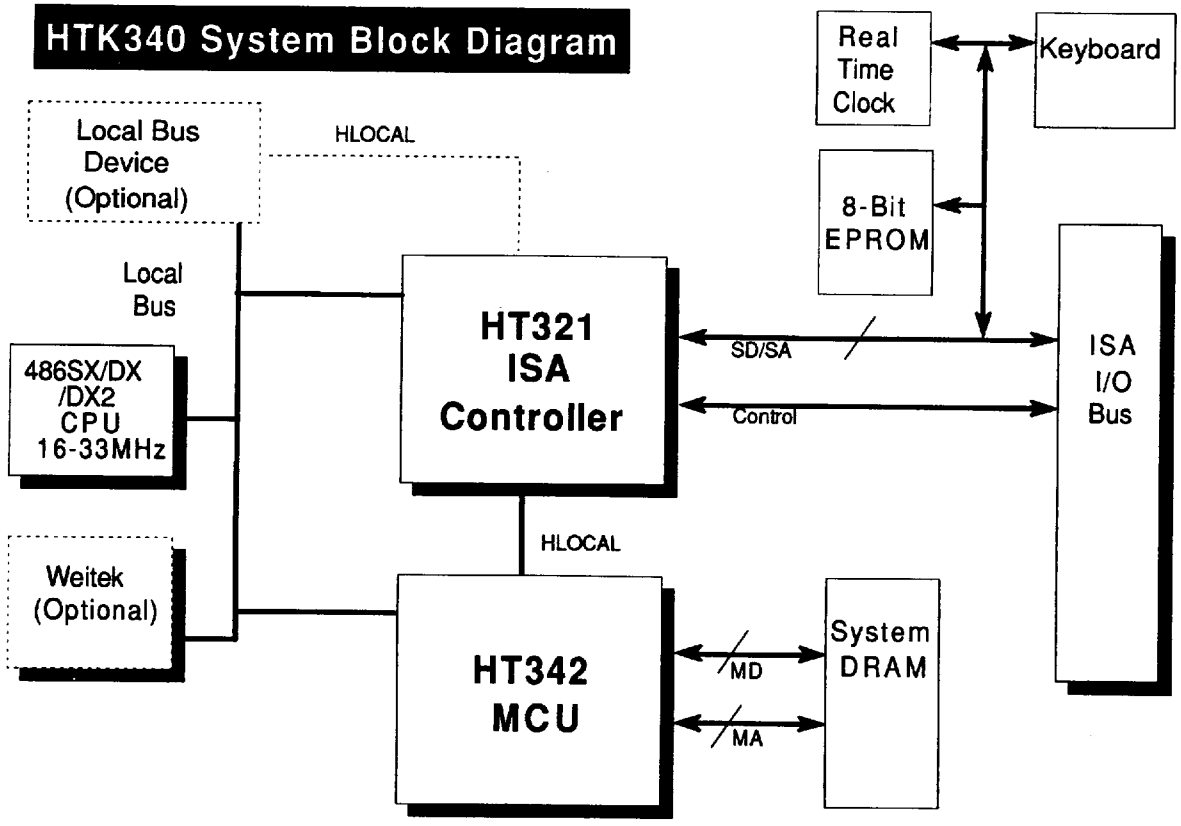


Figure 2.1 - HTK340 Computer System Block Diagram

General Description

The HTK340 chip set is a two chip, high performance, cost-effective solution for the 80486SX™ DX,™ and DX2™ processing environments. In its minimum configuration, this highly integrated chip set requires only four external TTL devices to implement a fully compatible IBM PC/AT™ system at speeds up to 33MHz.

The HTK340 is based upon Headland's HTK320 Bus Architecture and consists of the HT321-ISA Bus Controller and the HT342-Memory Control Unit (MCU). Both chips are packaged in 184 pin plastic quad flat packs.

The HTK340 is unique in that it provides performance approximating that of large secondary cache systems, including the highest performance write back cache architectures, without any external cache. Secondary cache solutions should be considered in applications that make use of multi-tasking and large model operating systems. The Headland HT44 secondary cache was designed to meet the cost and performance objectives for these applications. The key to this level of performance is the 4-level deep write buffer, which includes byte gathering for up to 32-bit DRAM writes.

Due to the effectiveness of the primary cache internal to the 80486™, most of the bus activity in a PC/AT compatible environment consists of writes. Indeed, this write activity consists almost exclusively of writes of either bytes or words (16 bit entities). In addition, much of this write activity is into sequential memory locations. The byte gathering feature of the buffer has the effect of reducing the number of memory accesses required. Since the 80486 can always write into the buffer with zero wait states (assuming the buffer is not full), and the buffer can empty faster than it can be filled for most write activity, the net effect is that the writes from the CPU never cause a wait state.

The HTK340 can support Peripheral Devices such as VGA or SCSI on the local processor bus, or any other devices that are designed to work within the 80486 bus protocol and timing. By eliminating the ISA backplane bottleneck, system designers can greatly improve the performance of functions such as graphics generation and disk access.

The HTK340 supports up to 4 banks of DRAM, configurable as 1-4 banks. This flexible memory architecture allows for any memory type, from 256K to 16M devices, in any bank. Maximum system performance is achieved from the DRAM banks through various means, including interleaving of memory banks and/or paging, and CAS before RAS refresh. The memory can also be tuned to maximum potential through the use of extensive DRAM timing control registers. These controls include: precharge time, access time on reads, active time on writes, as well as CAS and RAS delays. In addition, further system performance is gained by separate timing parameters on the read and write cycles which allow system designers to take maximum advantage of the pipelined structure of the chip set.

The HTK340 also supports extensive mapping registers, which allow system designers to take maximum advantage of system memory. The chip set supports Shadow/Remap in 16K blocks between the 640K and 1M boundaries, and eliminates the requirement for external decoding logic by supporting 26 programmable non-cache regions. Devices which meet HTK340 local bus requirements may be implemented without external TTL. The mapping structure of the HTK340 provides for a single 8-bit EPROM to be used for both the System and Video BIOS, further reducing system chip count and cost.

HT321 Functional Description

This section provides the functional description of the HT321 within the Shasta Chip Set environment. The main duty of the HT321 is to interface the 8-MHz ISA backplane with the high speed Shasta Local Bus. The HT321 provides all the functional blocks necessary for AT Compatible backplane timing, Address/Data Buffering and Latching, as well as circuit equivalents of two Intel 8237's in cascade mode, two 8259's in cascade mode, and an 8254. The HT321 is designed for '486 systems that operate between 16 and 40MHz.

In the Shasta chip set architecture, the HT321 is the default device for CPU generated cycles, meaning that if no other LOCAL BUS device responds to the current cycle, then the HT321 will be selected to respond and terminate the cycle. The HLOCAL* input provides the information necessary for the HT321 to determine whether or not to respond to the current cycle. Alternatively, if a Local Device cannot support the "HLOCAL*" feature, the HT321 can be programmed for a "decode hole" within its I/O and/or MEMORY map so that when any address matches the Programmed Hole, the HT321 will ignore the cycle allowing another device to respond. One I/O and MEMORY hole may be programmed within the HT321 at any given time.

The HT321 becomes the Master Device in the System during DMA cycles, whereby the HT321 will generate all the address and control information necessary for the Shasta local bus, just as the CPU does for regular cycles. As Master during DMA cycles, the HT321 provides cycle information to both the Shasta Local Bus and the Backplane. If a Local Bus Device does not respond to this cycle, then the HT321 will assume the DMA cycle is for a backplane device and adjust accordingly.

Oulined below are the major features of the HT321:

- 184 PQFP package.
- Up to 33 MHz operation.
- Fully AT-compatible 8 MHz ISA bus interface.
- Posted backplane memory writes.
- Interfaces to 8 or 16-bit ROM's.
- Ability to map video BIOS into same physical device as system BIOS.
- Internal DMA Page Registers
- Extended DMA Page Registers.
- Port_92 functionality.
- 1 micron technology.
- Shasta architecture compatible.
- Performs all ISA bus address and data buffering.
- Built-in Intel™ equivalents for:
  - i) 8237 DMA controllers.
  - ii) 8259 PIC's (interrupt controllers).
  - iii) 8254 PIT (timer).
- Chip-select outputs for Real Time Clock and Keyboard interfacing.

Within the HT321 there are seven (7) major functional blocks (see Figure 2.2). These blocks include:

1. RESETS & CLOCK_GEN
2. LOCAL_BUS INTERFACE
3. ADDRESS BUFFERS & LATCHES
4. DATA BUFFERS & LATCHES
5. ISA BACKPLANE CONTROLLER
6. I/O DECODE & CONFIGURATION MODULE
7. MEGAFUNCTIONS

A Functional Description for each of these blocks follows.

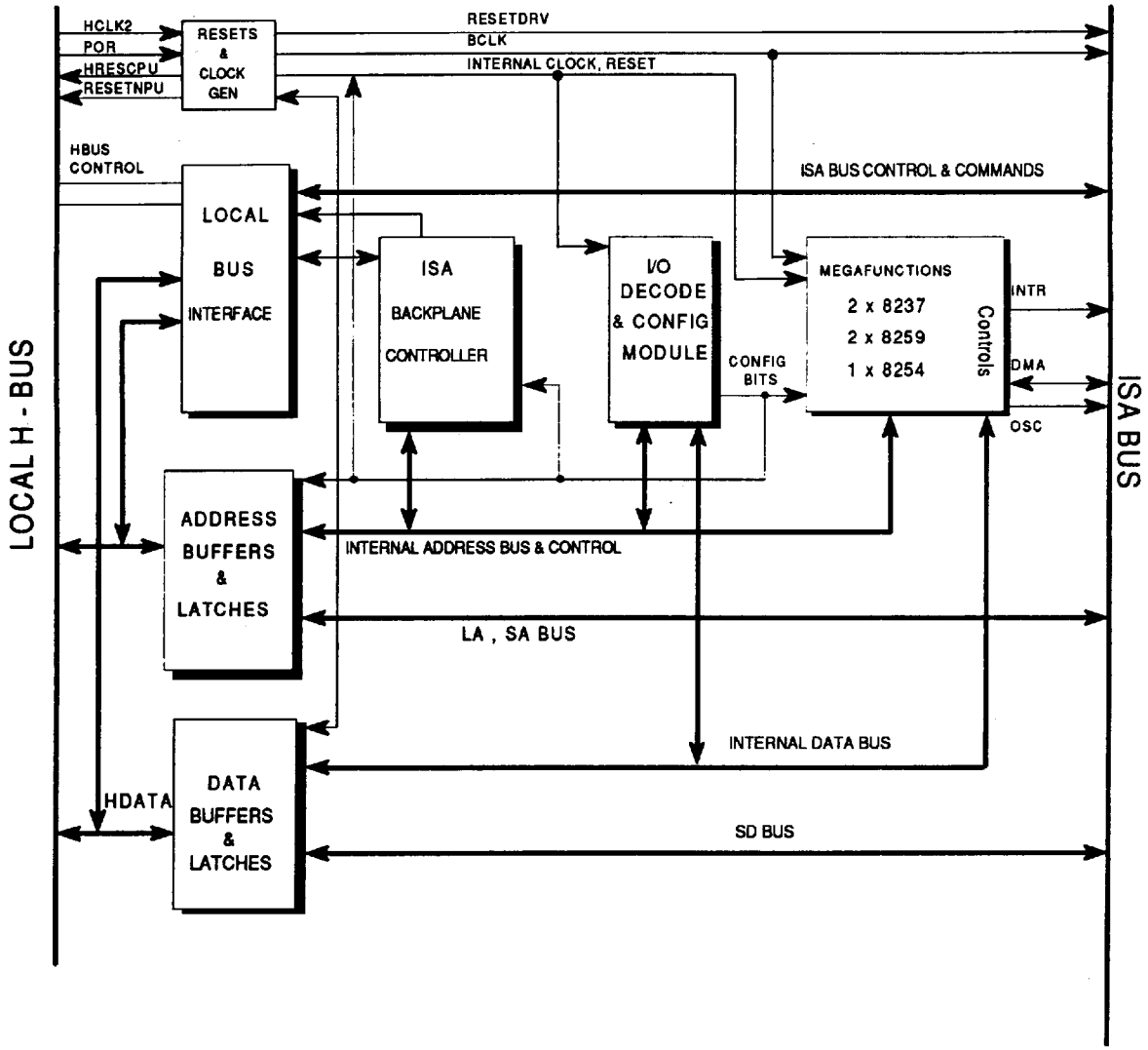


Figure 2.2 - HT321 ISA Controller Internal Block Diagram

HT321 Functional Description

1. Resets & Clock Generation

This module is responsible for generating all the Internal or External Resets and Backplane Clocks required by the Shasta HT321. The output signal pins directly affected by this module include BCLK (P68), HRESCPU (P170), RESETNPU (P51) and RESET-DRV (P76).

Clock Generation:

The primary incoming reference clock signal is HCLK, which is used to derive BCLK and INTERNAL_CLK. INTERNAL_CLK is a buffered version of the HCLK signal and is used to clock all the internal state machines of the HT321, whereas BCLK is produced by division of the HCLK signal by Programmable Ratios of 2, 3, 4, 5, 6, or 8. This Divide Ratio is selected via INDEX 01 of the HT321, where the system bus speed can be programmed to produce a 50% duty cycle 8.0 - 8.33 MHz BCLK signal that is then available to the ISA Backplane. Figure 2.3 shows the timing relationships between HCLK and BCLK for different settings of INDEX 01. The BCLK signal is further made available to clock the internally cascaded Intel 8237 DMA Controller equivalents. The user has the choice of supplying the internal 8237's with the 8 MHz BCLK signal directly or dividing this BCLK signal in half to supply the AT standard 4MHz clock to the 8237 DMA functions. Frequency selection for the 8237 clock is programmed via INDEX 06 of the HT321.

The AT Backplane signal, OSC, which is a 14.318 MHz Color Burst Frequency is used within this module to produce the Internal Clock of the Intel equivalent 8254 Timer function. This clock is simply the OSC input divided by 12 to produce the required 1.19MHz clock signal.

Resets:

POR is the primary reset signal input. It indicates either a POWER-ON or HARD RESET situation. Once this signal goes active (high), all internal circuits are reset to their initial default state and the HRESCPU, RESETNPU and RESETDRV signals are asserted to initialize all external system devices.

HRESCPU is the reset required by the 486 processor (CLREXPTION) to reset it to its initial state. This signal is produced synchronously using the HCLK input. Figure 2.4 shows the basic timing relationship between HCLK and HRESCPU. See the AC Timing Specifications Section for detailed timing of this signal. HRESCPU will also be generated for a keyboard initiated reset sequence via the RC(P77) input or the PORT_92 FAST_RC programmable function.

RESETNPU is the signal required to initialize the optional system Co-processor. The timing of this signal is identical to the HRESCPU and is only generated as a result of POR or by an I/O write cycle to 0F1H. An I/O write to 0F1H,which produces a RESETNPU pulse,defaults to Enabled at Power-on .

RESETDRV is the ISA Backplane reset signal. This Reset signal is Synchronized to the BCLK clock and is produced only during the POR sequence. RESETDRV is driven active high after the falling edge of POR for more than 80 HCLKs in Rev. C or earlier. For Rev. D or later, RESETDRV is active during POR as well. See Fig. 2.4 for details.

Figures 2.4, 2.5, and 2.6, show the timing relationships between HCLK and the Reset signals described.

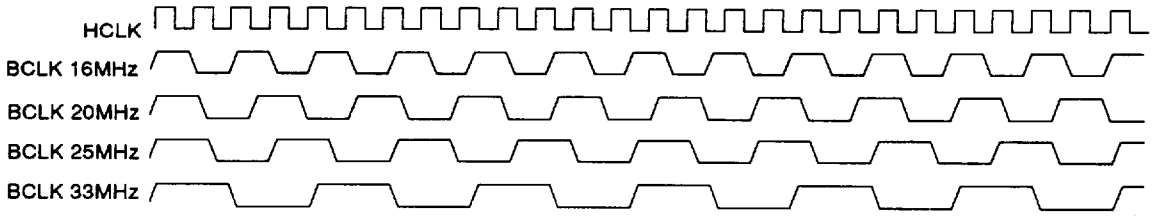


Figure 2.3 - Backplane Clocking (BCLK)

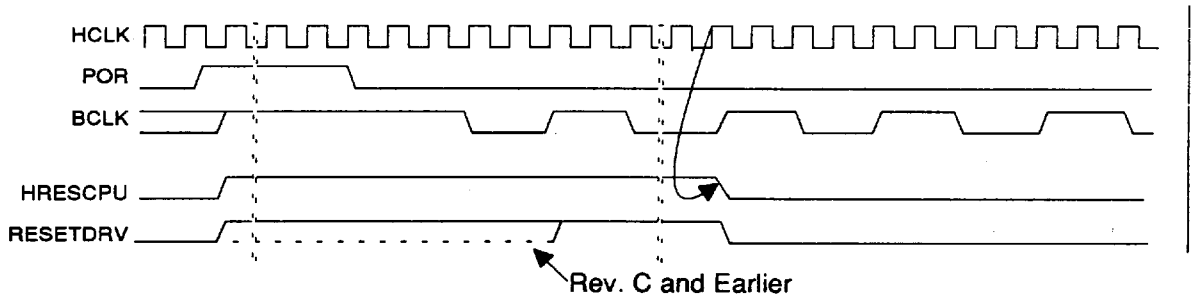


Figure 2.4 - Resets from Initial Power-On

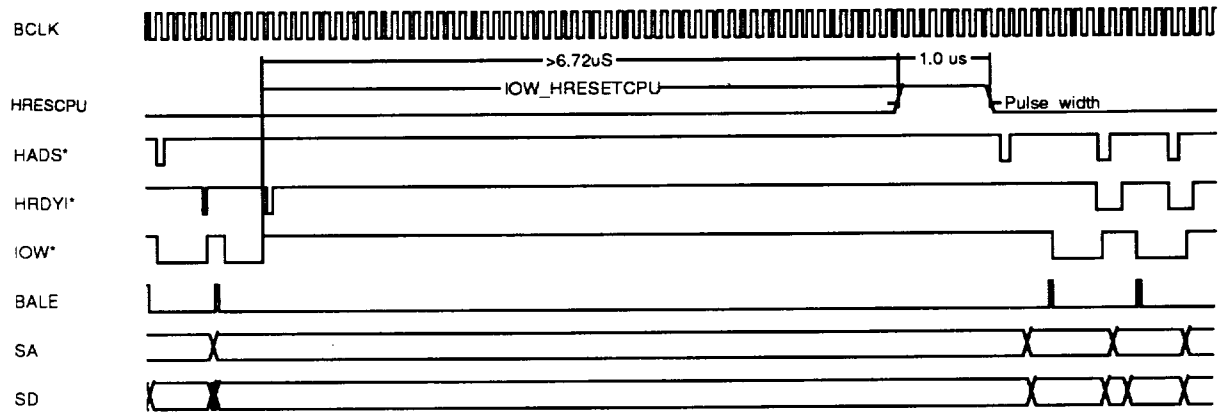


Figure 2.5 - Port 92 Reset Sequence

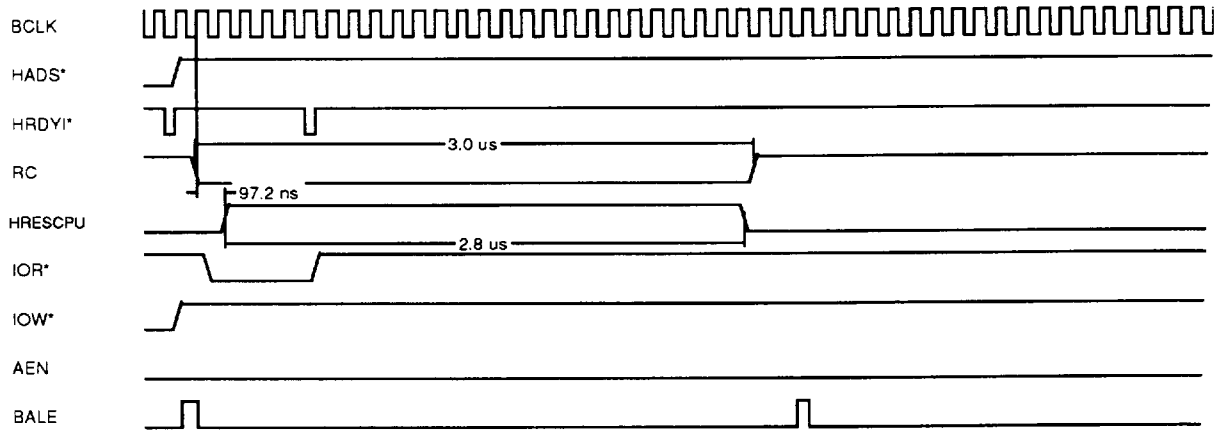


Figure 2.6 - Keyboard Reset Cycle

2. Local Bus Interface

The LOCAL BUS INTERFACE module interfaces the HT321 with the Shasta Local Bus Control Signals. These signals include HA(P38-25,22-10), HBEN*(P40-43), HHLDA (P168), HADS*(P44), HRDY*(P39), HRDYI*(P165), HMIO(P175), HDC (P174), HWR(P173) and HLOCAL*(P167). For CPU initiated transfers, this module must synchronize Shasta cycles with the ISA Backplane cycles and, during DMA transfers, this module is responsible for generating all the Shasta Bus Control Signals.

The LOCAL_BUS_INTERFACE module must monitor the Shasta Bus to determine when a HT321 cycle is required. HADS* is the Control Signal in a '486 system which indicates Start-of-Cycle to all Local Bus devices. One HCLK2 after HADS* initiates Start-of-Cycle, the HLOCAL* signal is sampled to determine if another Local Device has responded to the cycle. If at this time the HLOCAL* signal is true (low), the HT321 performs no action for the cycle. However, if the HLOCAL* is false (high), the HT321 must respond to the cycle, and the LOCAL_BUS_INTERFACE module will pass the request on to the ISA BACKPLANE CONTROLLER section of the chip. Signals including HA[31, 27:2], HBEN*[3:0], HMIO, HDC and HWR are sampled and gated to the rest of the ISA chip. At the conclusion of the ISA cycle, the ISA BACKPLANE CONTROLLER section indicates completion by issuing a READY pulse to the LOCAL_BUS_INTERFACE module. This READY appears on the Shasta Local Bus as HRDY* from the HT321. When HRDYI* is returned to the HT321 chip, the real end-of-cycle occurs and the HT321 returns to monitoring the Shasta Local Bus for further ISA cycles. Figure 2.11 shows the fundamental timing relationships between HCLK and Shasta Local Bus signals attached to the HT321. This diagram specifically shows timing for CPU initiated cycles.

For DMA initiated cycles, the '486 CPU enters a Hold State in response to the HOLDREQ Signal of the HT321. When the CPU has completed its current tasks and can relinquish the Shasta bus, it will assert the HHLDA signal, this is gated to the Cycle Arbiter of the LOCAL_BUS_INTERFACE module. Only when activity is determined complete on the Shasta Bus and ISA Backplane Bus is the HHLDA signal gated to the rest of the ISA Chip. For regular DMA cycles, the internal DMA Controller of the ISA Chip will assert the ISA Backplane Command combinations (IOR*/MEMW*, MEMR*/IOW*) which are detected by the LOCAL BUS INTERFACE. DMA to/from Local Memory is the only non-MASTER Mode activity supported by the Shasta architecture; when a MEMR* or MEMW* Command is detected, the LOCAL_BUS_INTERFACE module asserts an HADS* pulse on the Shasta bus, the cycle status information (HMIO, HDC, HWR) is decoded and asserted on the Shasta Bus at this time, where it remains valid until the Backplane Commands are de-asserted. HLOCAL* is sampled one HCLK after HADS* to determine if the cycle initiated is for a Shasta Local Bus device. In this manner, all cycles on the Shasta Local Bus look identical, whether they are initiated by DMA or '486 CPU. Figure 2.7 shows the timing of HT321 initiated Shasta cycles during DMA transfers.

For DMA MASTER mode cycles, events follow the sequence described above, but Backplane MASTER mode devices may have access to I/O as well as Memory locations on the Shasta Local Bus. Therefore, during MASTER mode Cycles, when any Backplane command is detected by the LOCAL_BUS_INTERFACE module, a HADS* pulse will be generated for the Shasta Bus (Reference HT321 Index 06H). Figure 2.9 shows a MASTER Mode Memory Write Cycle to Shasta local memory, whereas Figure 2.8 shows the timing relationships for a MASTER Mode Read Cycle from local memory.

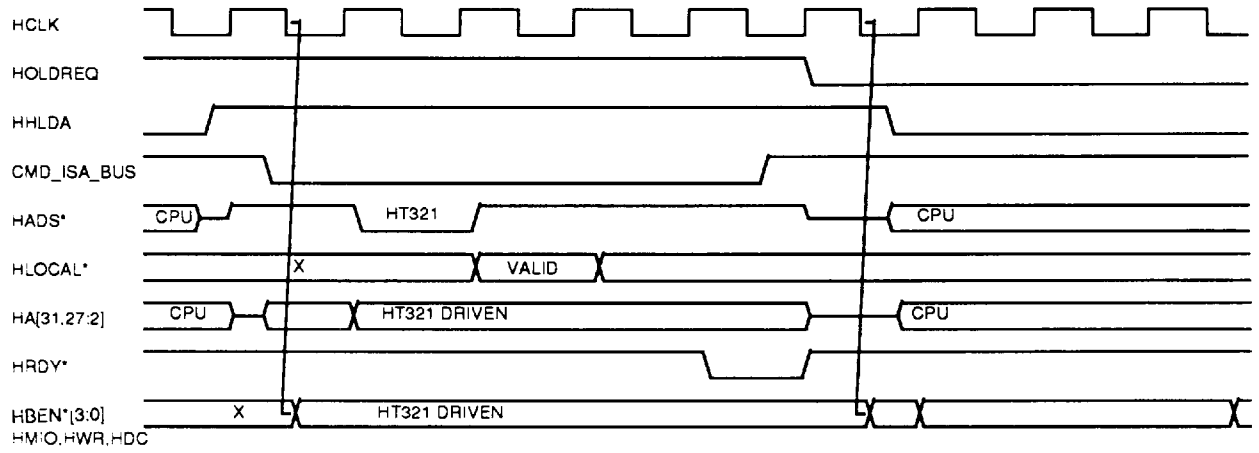


Figure 2.7 - DMA Cycle on the Local Bus

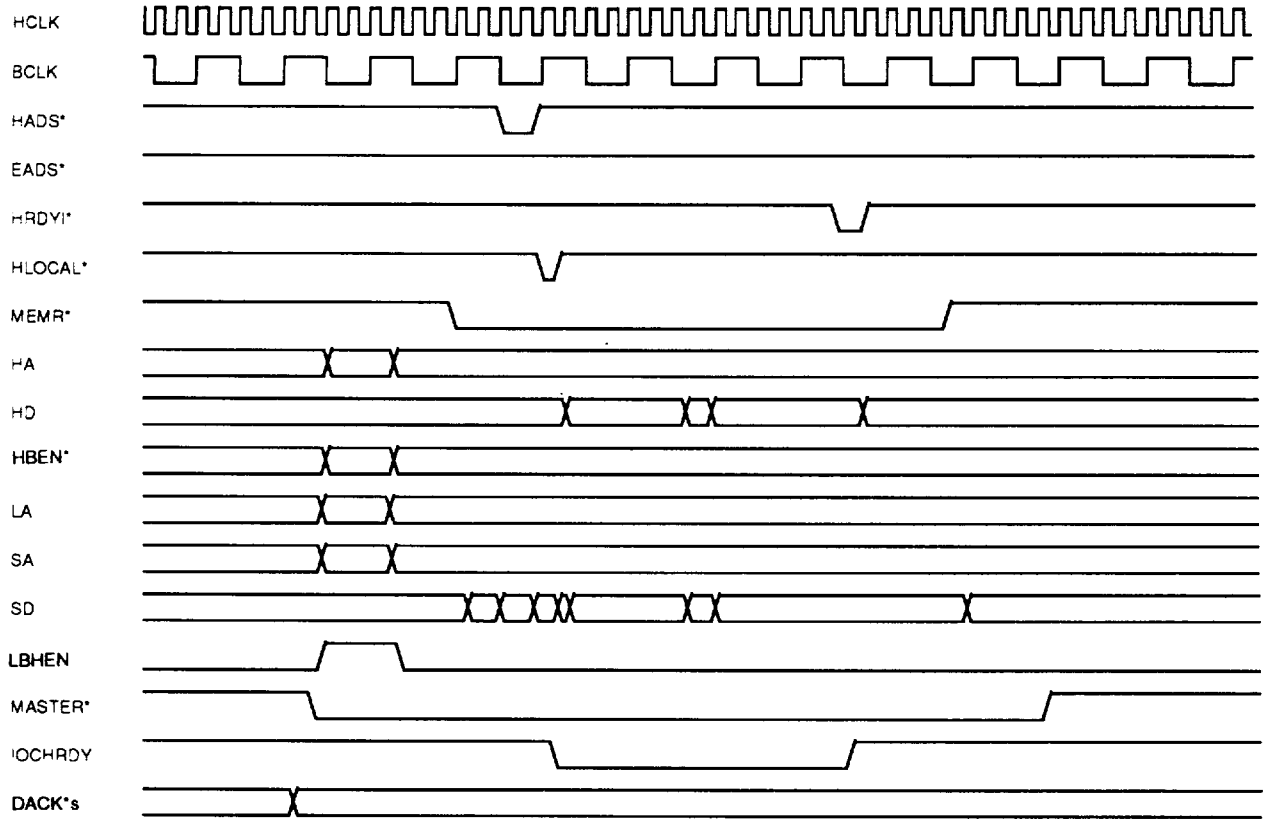


Figure 2.8 - Master Mode Memory Read Cycle to a Local Device

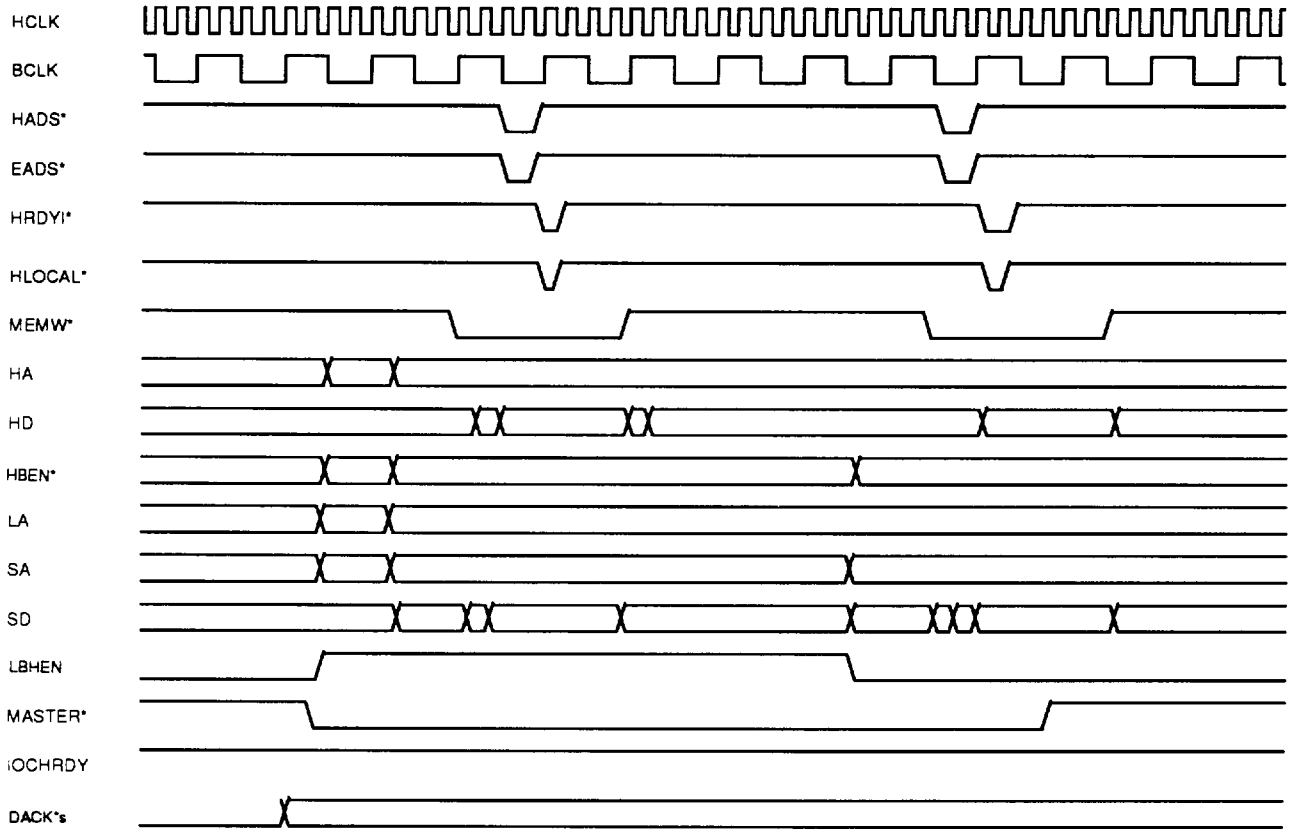


Figure 2.9 - Master Mode Memory Write Cycle to a Local Device

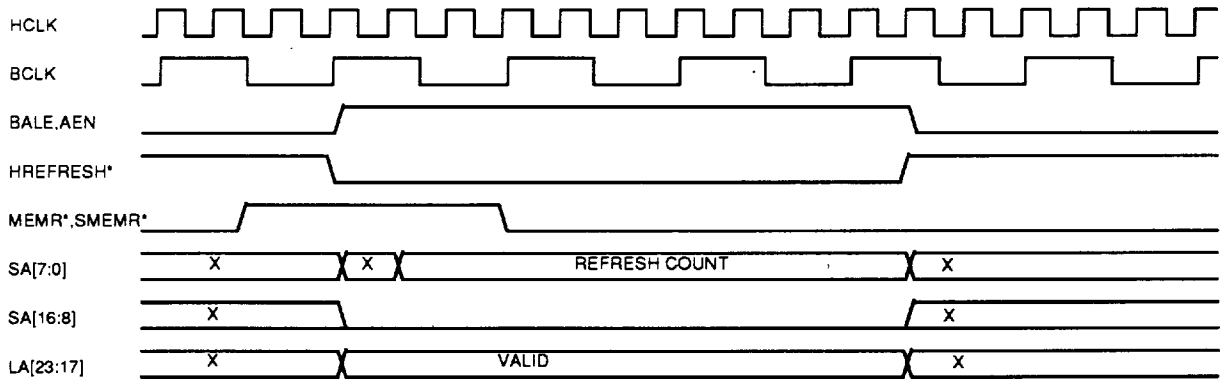


Figure 2.10 - HREFRESH* Timing

3. ADDRESS BUFFERS & LATCHES

This module is responsible for providing the necessary ISA Backplane SA[19:0] (P136-129,126-117,114-113), LBHEN*(P137) and LA[23:17](P112-106) Address Signals during ISA Cycles initiated by the CPU. During DMA cycles, this module will provide the HA [31, 27:2] and HBEN*[3:0] Shasta Local Bus signals.

For CPU initiated cycles, the SA[19:2] lines are produced from the incoming HA[19:2] signals and gated to the ISA backplane when BALE is true(high). On the falling edge of BALE, ISA Compatible Backplane devices may latch the SA address signals since they are then stable and will remain stable for the entire cycle or until another BALE is generated. Shasta Local bus signals HBEN*[3:0] generate SA1, SA0 and LBHEN*. The significance of these SA address lines depends on the number of bytes requested by the system and whether the target data is located at an odd address. The ISA Backplane LA[23:17] address lines are asserted 1 HCLK after HADS* is sampled true, by the HT321. These Signals are equivalent to the HA[23:17] input address signals. These LA address lines remain valid until HRDYI* is returned to the HT321 signifying the end of the current cycle.

During REFRESH* cycles, SA[7:0] are driven by the internal refresh counter of the HT321 and contain the Refresh Address. SA[15:8] are asserted to logic 0. SA[19:16] and LA[23:17] are controlled by the current programmed value of the Internal DMA PAGE Register at location 8FH. Typically, this register is set to 00 in an AT system. HA address lines are not driven by the HT321 during REFRESH* cycles. The Backplane signal BALE is true(high) for the duration of the cycle. The sequence of a REFRESH* cycle is shown in Figure 2.10.

During DMA cycles, SA[15:0] and LBHEN* signals are generated by the Internal Intel 8237 equivalent that has control for the cycle. The significance of SA[19:16] and LA[23:17] signals is controlled by the DMA PAGE register (I/O location 80-8FH) of the acknowledged DMA channel. The value is programmed by application software or BIOS. BALE is always true(high) for the duration of a DMA cycle. A typical DMA transfer cycle, as seen on the ISA Backplane, is shown in Figure 2.25. In this diagram, the DMA clock is set to BCLK/2 (INDEX 06H). A MASTER mode transfer cycle from an ISA Backplane memory device is shown in Figure 2.24. In this case, the HLOCAL* was not generated by any Shasta Local device. Therefore, the whole transfer takes place on the ISA Backplane.

HA[23:2] and HBEN*[3:0] lines are asserted by the HT321 during DMA cycles and are the equivalent of the Backplane SA and LA signals. To provide DMA access to the full Local Memory range of a Shasta System, Extended DMA PAGE REGISTERS located at I/O address 480-48FH are implemented in the HT321. These registers are controlled via INDEX 06 of the HT321 Registers. When enabled, they contain the HA[31:24] Address values required for the Extended DMA transfer. The Extended DMA Page Registers provide for DMA access to/from any location within the Shasta system local memory map. The timing of the HA and HBEN* signals produced during DMA cycles is equivalent to '486 processor timing; that is, the addresses are valid when HADS* is generated by the HT321 and remain valid until HRDYI* is returned by the System to terminate the cycle in progress.

4. DATA BUFFERS & LATCHES

This module is responsible for routing Data to and from the ISA Backplane SD[15:0] and the Shasta Local Data Bus HD[15:0]. If Data Bridging is required during the current cycle, this module will provide it. For ISA Backplane requests which require more than one cycle to access the data required by the CPU, temporary storage exists within this module to hold the gathered data until all the data is processed.

The HT321 is limited to a 16 bit transfer of data for any given cycle. To signal this fact to the CPU, BS16* is generated by the HT321 for any CPU cycle requesting data transfer on the upper half of the CPU data bus HD[31:16]. Figure 2.12 shows the timing for the generation of the BS16* signal by the HT321 chip.

For CPU initiated WRITE cycles to the ISA Backplane, data is placed on the HD[15:0] inputs of the HT321 and then routed through the chip to the SD[15:0] of the Backplane Bus. For 16-bit devices on the backplane, no Data bridging is required in the HT321 Chip. For 8-Bit ISA Compatible devices, the incoming data is routed automatically to the lower half of the SD bus (SD[7:0]). MEMCS16* and IOCS16* are the backplane signals monitored by the HT321 to determine whether the ISA Backplane device responding is 16- or 8-Bit. For CPU WRITES of 16-bits of data to an 8-Bit Backplane device, the incoming HD[15:0] bus is latched at the start of the first WRITE cycle. A second WRITE cycle is generated by the HT321 to transfer the next 8 bits of data to the Backplane device.

For CPU initiated READ cycles from the ISA Backplane, data is applied to the SD[15:0] Backplane Bus by the responding device and routed through the ISA chip to the HD[15:0] bus so that the '486 CPU can aquire the data. The HBEN*[1:0] Shasta Local Bus signals, generated by the CPU in this case, are used to determine which way to route the backplane data through the HT321. Again, MEMCS16* and IOCS16* are monitored to see what data size will be transferred by the Backplane device. For CPU requests of 16-bits of data from an 8-bit Backplane device, the incoming SD[7:0] bus is latched at the end of the first cycle, and then another cycle is generated by the HT321 to acquire the next 8 bits of data from the Backplane device. During the second cycle of this transfer, both sets of 8-bit data are applied to the HD[15:0] pins to complete the request.

For DMA WRITE and Backplane MASTER mode READ Transfers to/from the Shasta Local Bus, the HT321 uses the SA0, SA1 and LBHEN* signals to determine the Shasta HBEN*[3:0] lines. These signals now indicate to the Local Memory device where to expect Valid Data on the HD[15:0] bus. When DMA transfers of data to the upper half of the Shasta data bus (HD[31:16]) occur, the HT321 will issue HBEN*[3:2] correctly; Local Memory Devices must accept this data on HD[15:0] and bridge the Data to the correct location.

For DMA READ and Backplane MASTER mode WRITE Transfer cycles to/from the Shasta Local Bus, the HT321 again asserts the HBEN*[3:0] signals but requires a responding Local Memory Device to provide Valid Data only to the HD[15:0] lines.The Memory Device must bridge the data on the HD[15:0] bus as required. No more than two bytes of data will be transferred by the HT321 during a DMA cycle.

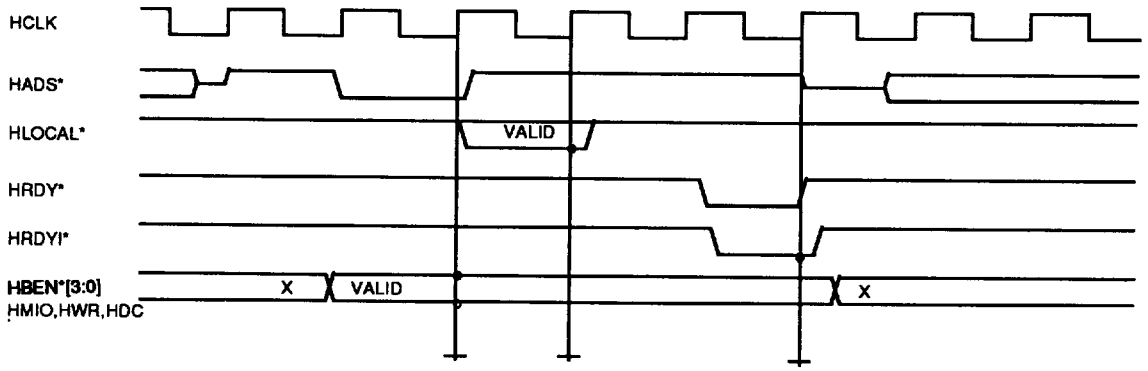


Figure 2.11 - HT321 Local Bus Signal Interface

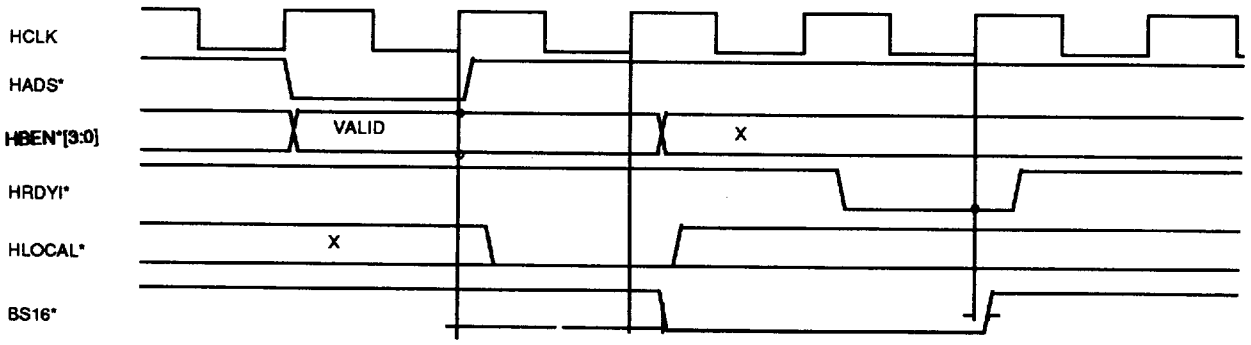


Figure 2.12 - BS16* Assertion

5. ISA BACKPLANE CONTROLLER

This module is responsible for producing ISA Compatible timing for the Backplane control signals. These signals include IOW*, IOR*, (S)MEMW*, (S)MEMR*, BALE and are synchronized to BCLK edges. In order to accomplish this, the ISA BACKPLANE CONTROLLER module monitors backplane signals MEMCS16*, IOCS16*, IOCHRDY, and 0WS to determine the timing required by the current cycle. INDEX 02H may be programmed to set the Default Timing of any backplane access. The AT Compatible setting is of 6 BCLK cycle duration. The options exist to set default as low as 3 BCLK cycles duration for a Backplane cycle. The duration of a Backplane cycle is measured from 1/2 BCLK before the assertion of BALE to the end of the Command asserted for the cycle.

Backplane cycles begin within the HT321 once it is determined that the current Local Bus cycle is for the ISA Controller. This happens one HCLK2 after HADS* is sampled, indicating the start of cycle. At this point, the ISA BACKPLANE CONTROLLER module will synchronize to the BCLK signal and begin the sequence by asserting a BALE pulse at the correct phase of BCLK. Depending on the type of cycle requested and the state of the incoming backplane cycle Moderator Signals, the proper Command(s) will be determined. At the completion of the Command, HRDY* will be issued by the HT321 to the Shasta Local Bus indicating the cycle is complete. When HRDYI* is returned to the HT321 the cycle actually completes. For more detail see Figures 5.11 and 5.12 in the AC Timing Section of this Data Sheet. A number of typical ISA Backplane cycles are shown in the following figures, 2.13, 2.14, 2.15, 2.16, 2.17, 2.18, 2.19, 2.20, 2.21, 2.22.

For DMA/MASTER MODE operation, the BACKPLANE CONTROLLER section of the ISA Chip is disabled, since the Commands will be asserted by the MASTER device. BALE is normally set true(high) for the duration of a DMA cycle, allowing address flow-thru to/from the backplane.

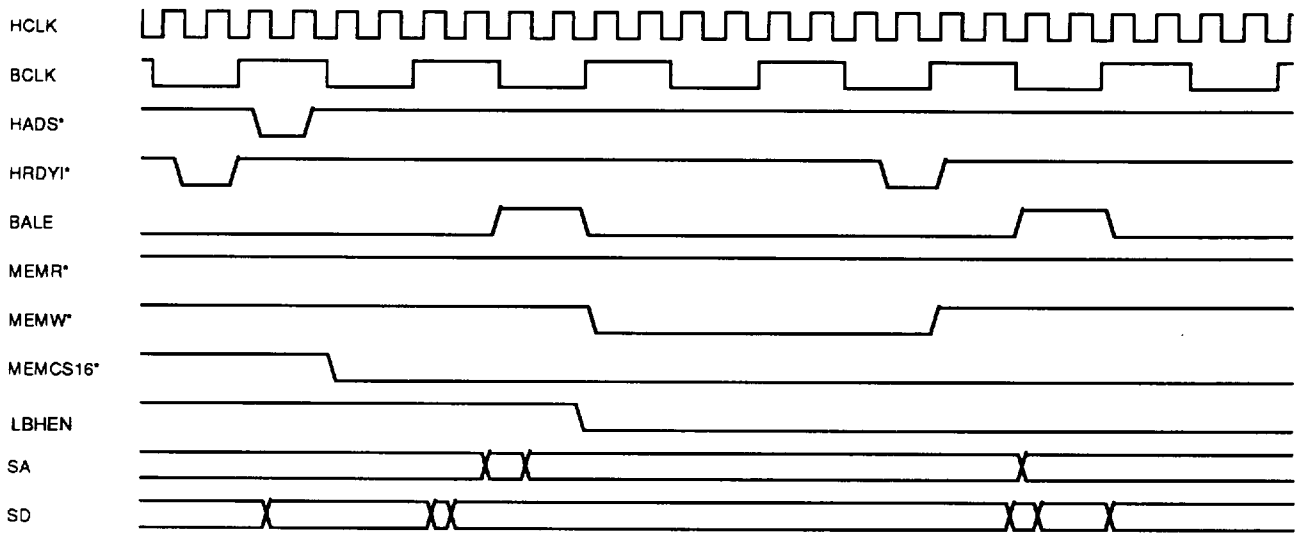


Figure 2.13 - 16-Bit MEMW* Cycle

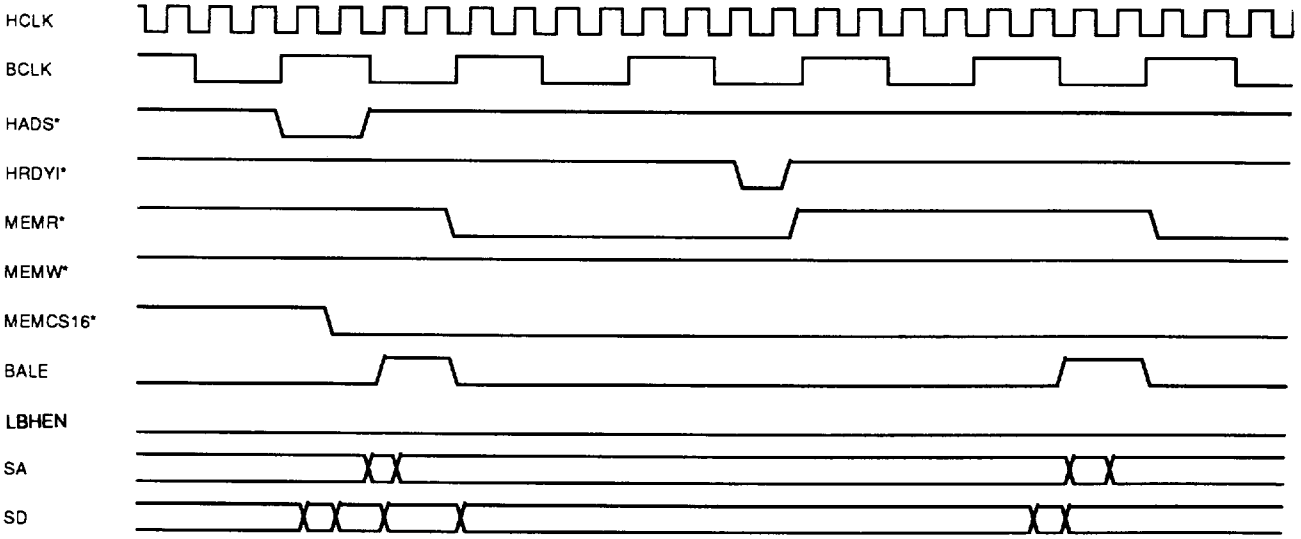


Figure 2.14 - 16-Bit MEMR* Cycle

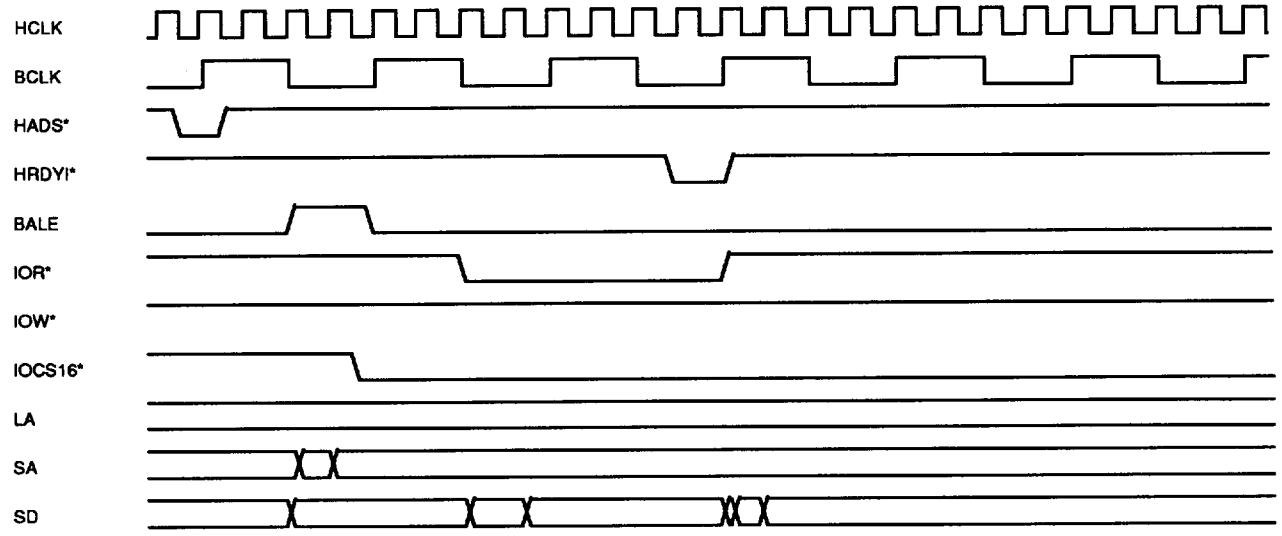


Figure 2.15 - 16-Bit I/O Read Cycle

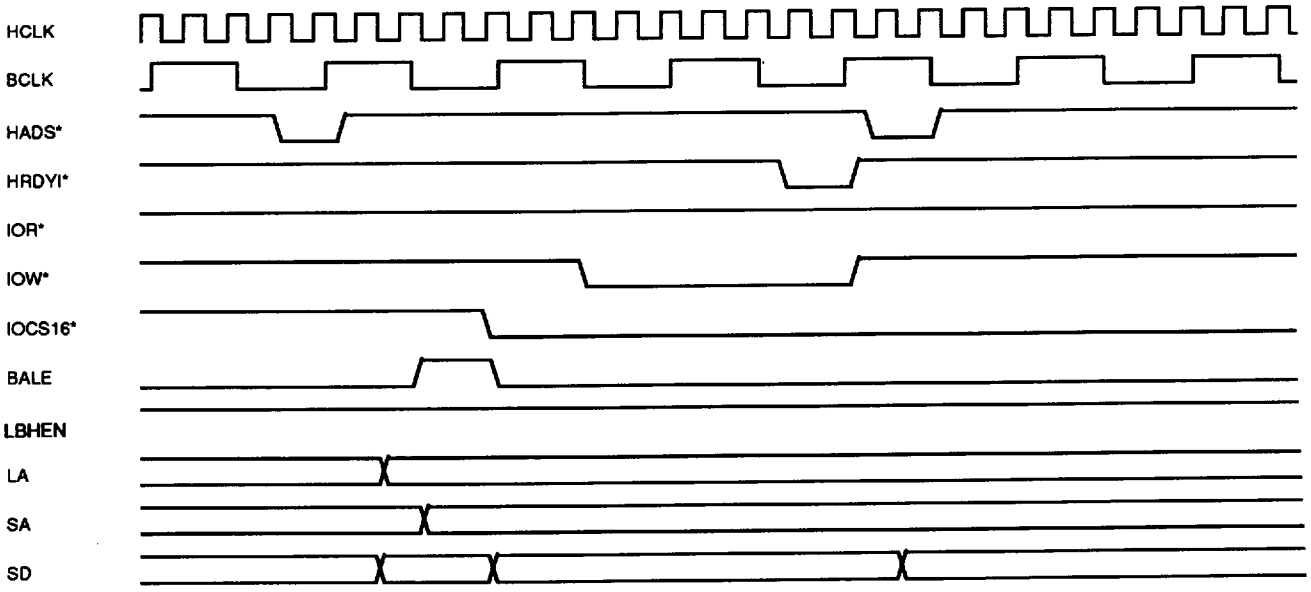


Figure 2.16 - 16-Bit I/O Write Cycle

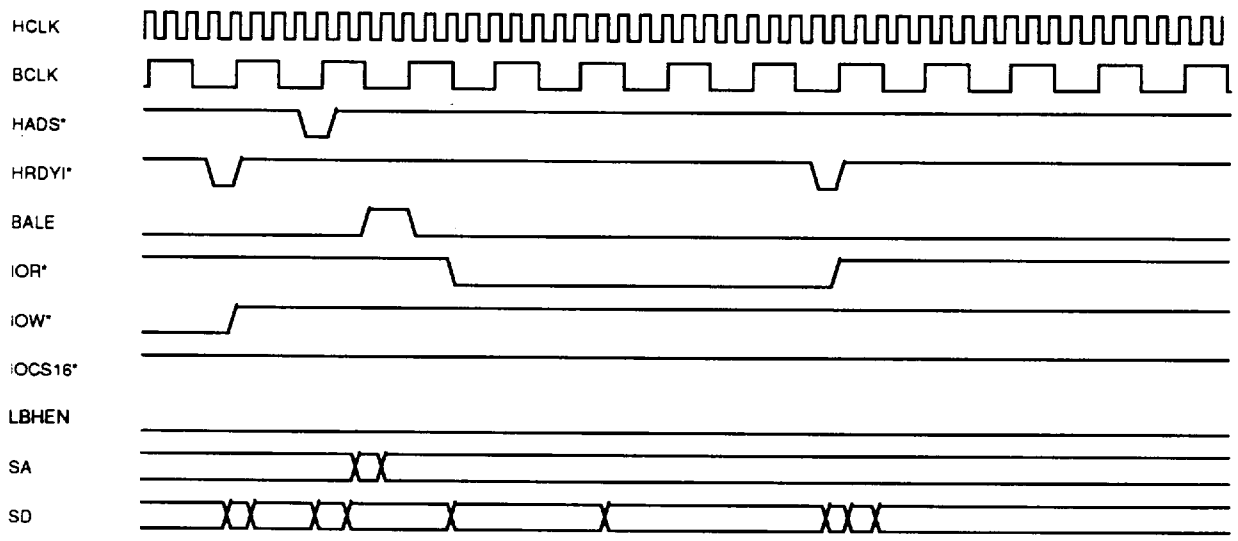


Figure 2.17 8-Bit I/O Read Cycle

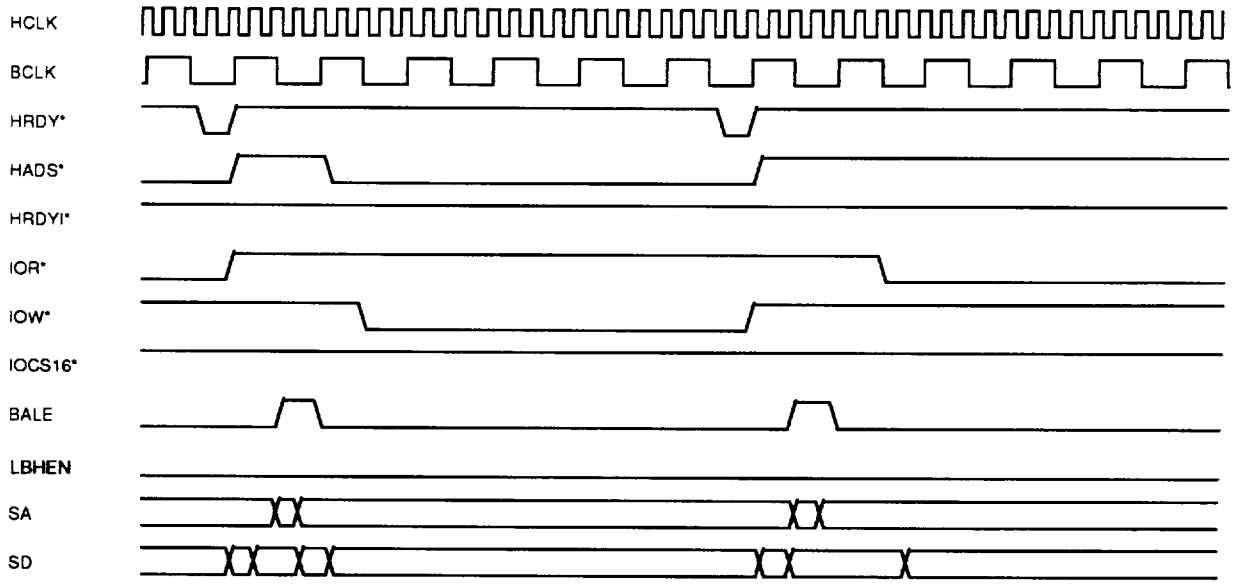


Figure 2.18 8-Bit I/O Write Cycle

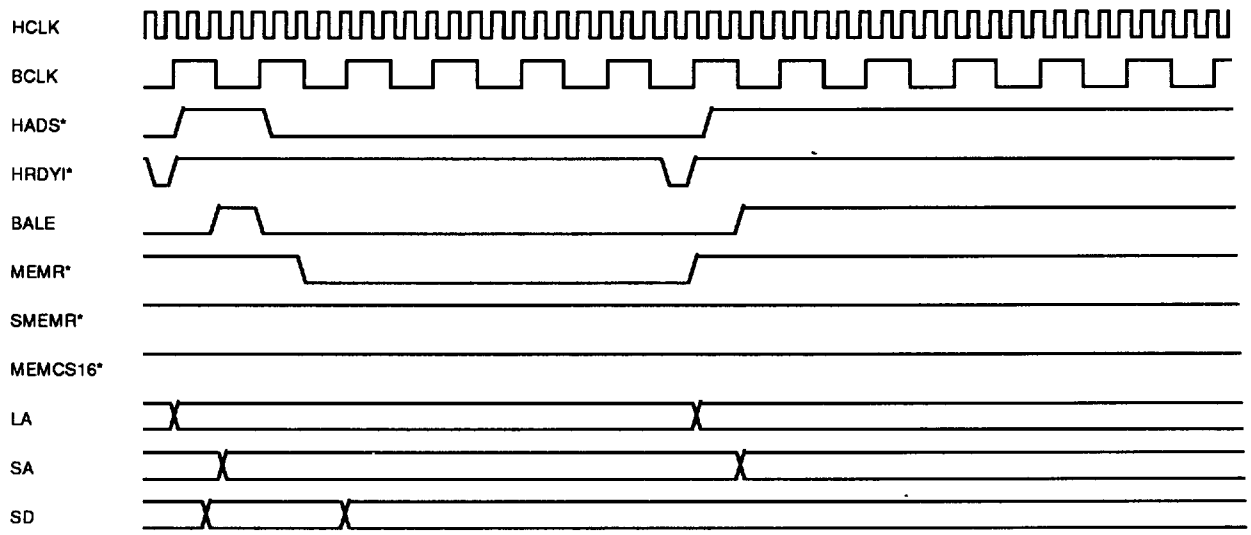


Figure 2.19 - 8-Bit MEMR* Cycle

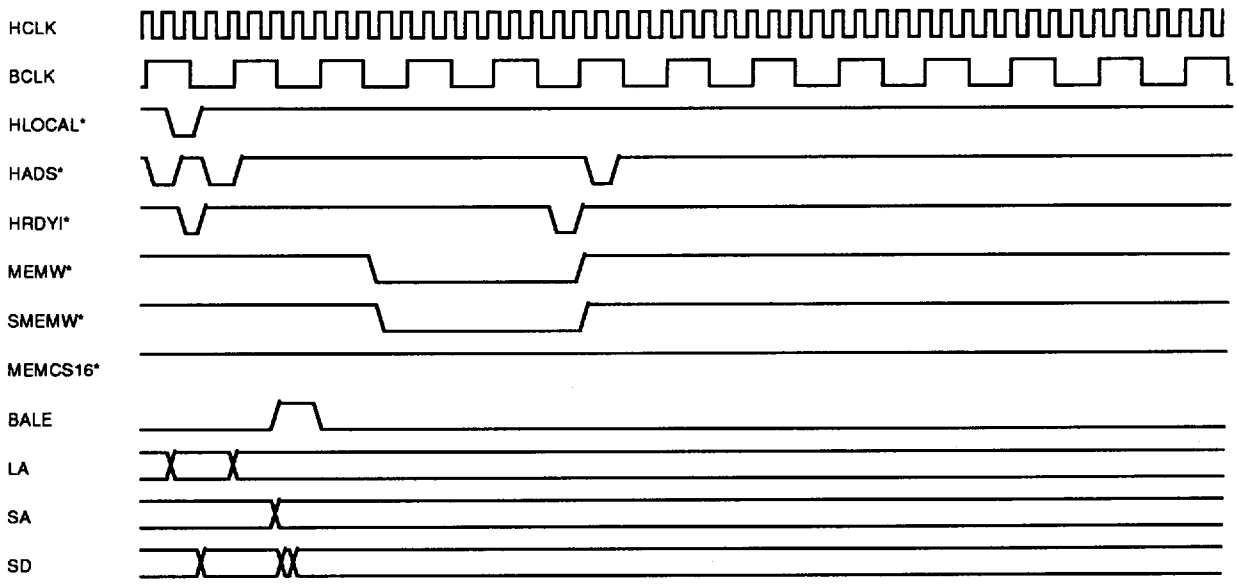


Figure 2.20 - 8-Bit MEMW* Cycle

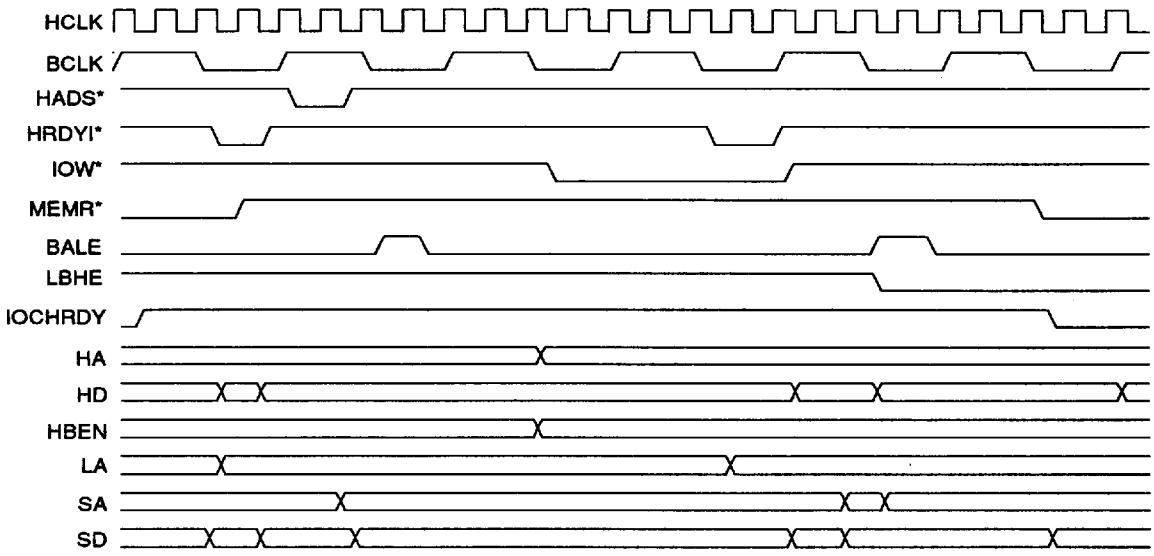


Figure 2.21 - IOCHRDY Wait States

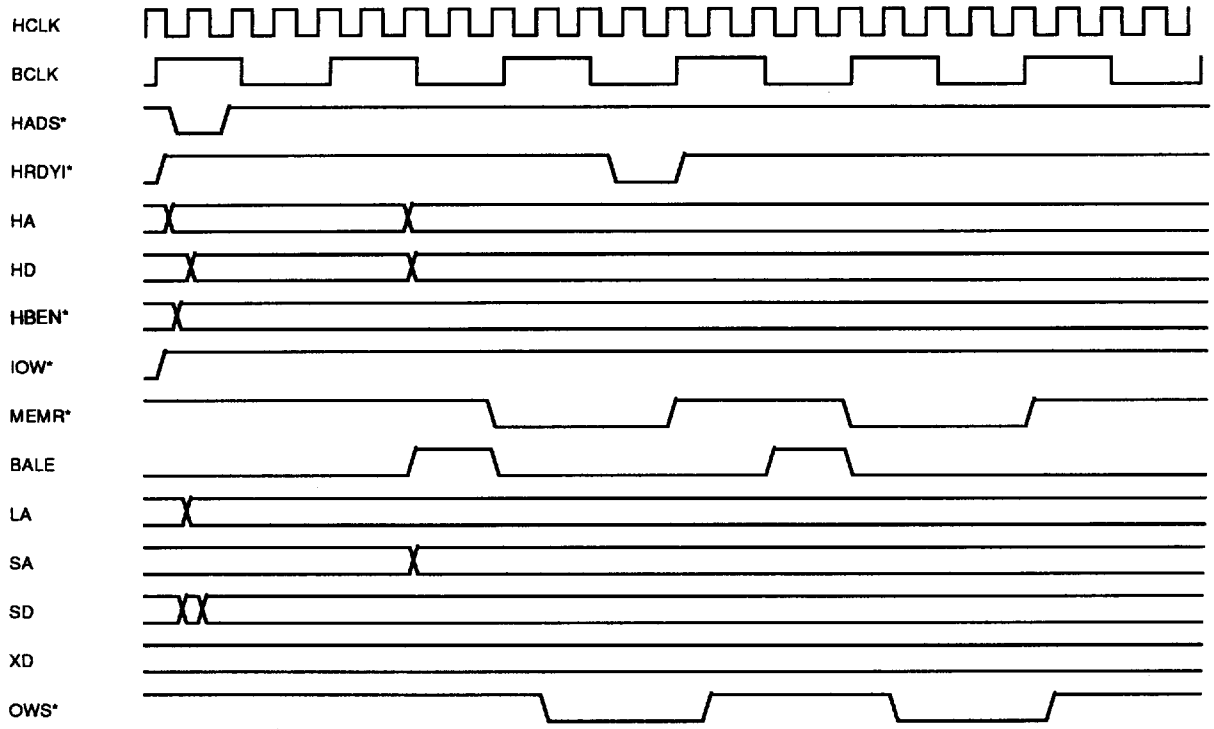


Figure 2.22 - 0WS Cycles

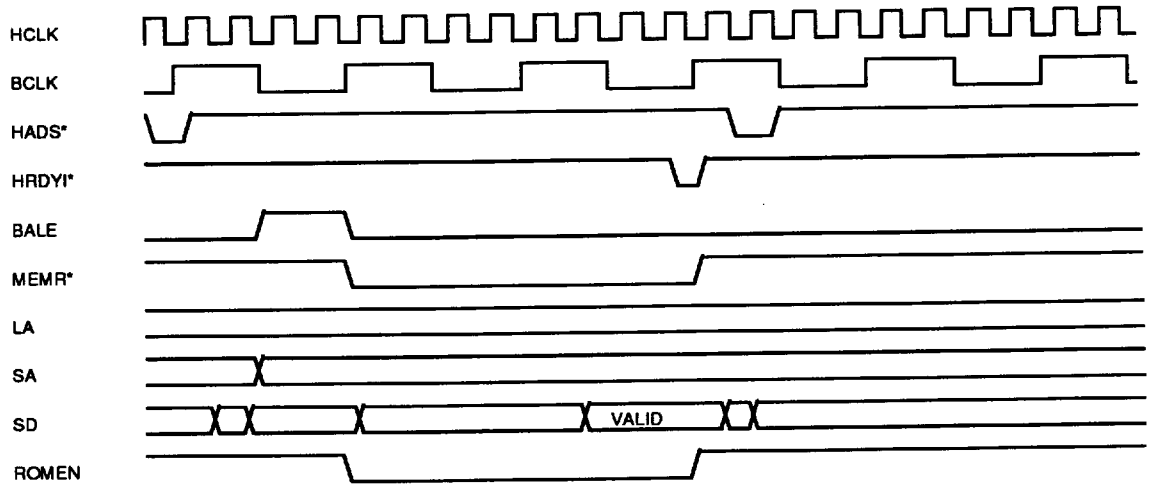


Figure 2.23 - PROM Read Cycles

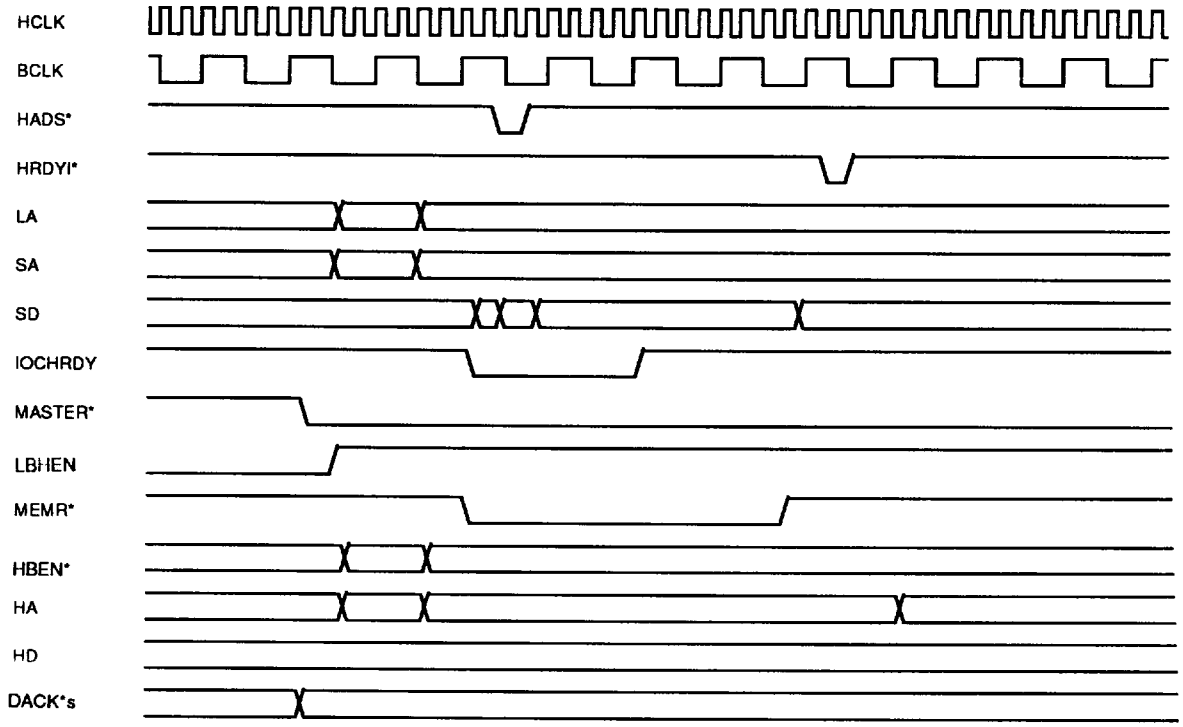


Figure 2.24 - MASTER Mode Backplane Read Cycle

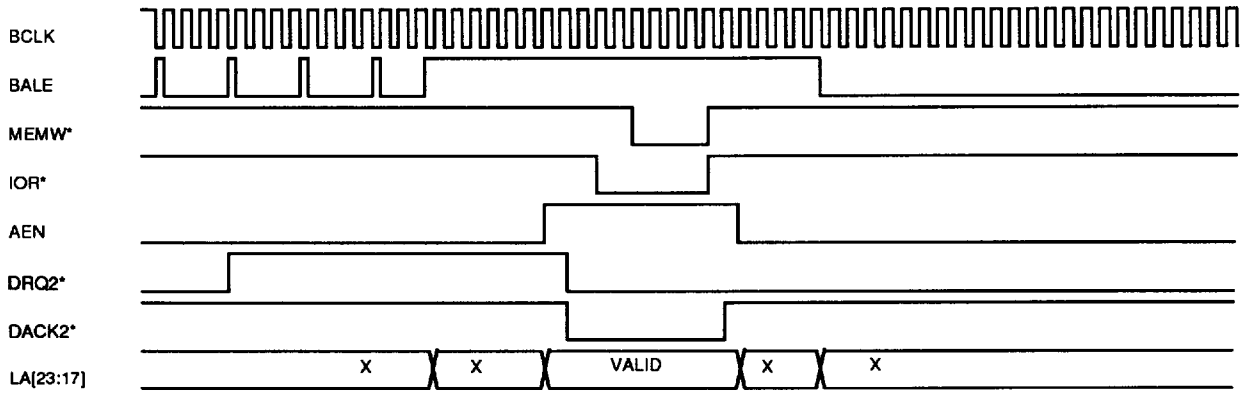


Figure 2.25 - DMA Cycle on the ISA Bus DRQ2/DACK

DMACLK = 4MHz
DMA Wait State = 1 (AT Standard)

6. I/O DECODE & CONFIGURATION

This module contains all the Internal Registers of the HT321 as well as Decodes for Internal and some External Devices. The HT321 provides "Chip Select" signals for two External Devices commonly used in AT Compatible Motherboard systems: Real Time Clock Chip Select (RTCCS* P81) and Keyboard Chips Select (KBCS* P80). The tables below chart the internal I/O decode information of the HT321.

The Configuration Module contains all the INDEX Registers which provide the HT321 Programmable Configuration Controls. The HT321 has a total of 32 mapped Index locations but only those containing programmable bits are implemented and accessible. These ISA Configuration Registers are mapped into INDEX 00 - 1Fh. Most of these registers are Read/Write, but only the bits indicated should be altered. All Unused or Reserved Registers and Bits must be left at Default or Masked off during Configuration to maintain future compatibility.

The ISA Chip is also responsible for maintaining the current Configuration INDEX Pointer Value. Therefore, access to I/O location 028H will be terminated by the HT321. Data Read from I/O location 028H is made available to the CPU via HD[15:0].

The Configuration INDEX Register Bits of the HT321 are described in detail in the Register Description Section of this Data Sheet. Please refer to this section for detail of the Registers, Control Functions and program access to the Registers.

I/O Decode

The following table shows the I/O Decode range for Internal Ports of the HT321.

A15-A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Range(Hex)	Selected Device
0	0	0	0	0	0	0	0	X	X	X	X	X	000 -01F	DMA1
0	0	0	0	0	0	0	1	0	0	0	0	X	020 - 021	PIC1
0	0	0	0	0	0	0	1	0	0	1	0	0	024	Config Data
0	0	0	0	0	0	0	1	0	1	0	0	0	028	Config Address
0	0	0	0	0	0	1	0	X	X	X	X	X	040 - 05F	PTC
0	0	0	0	0	0	1	1	0	X	X	X	0	060 - 06E(even)	KBC, Port B
0	0	0	0	0	0	1	1	1	X	X	X	X	070 - 071	RTC, NMI
0	0	0	0	0	1	0	0	0	X	X	X	X	080 - 08F	DMA Page
0	0	0	0	0	1	0	0	1	0	0	1	0	092	Sys Ctrl Port
0	0	0	0	0	1	0	1	X	X	X	X	X	0A0 - 0BF	PIC2
0	0	0	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	0	0	0	0	1	1	1	1	X	X	X	1	0F1	RESETNPU
0	0	1	0	0	1	0	0	0	X	X	X	X	480 - 48F	Ext. DMA Page

60-64 is KBC if A0=0, and Port B if A0=1, 070-071 is RTC if A0=1 and RTC and NMI if A0=0

All other address ranges are available to devices on the ISA bus.

I/O Address Map

The following table describes the I/O ports supported by the HT321. The table is numerically ordered by HEX Address from zero.

I/O TYPE

Addr Port	Read/ Write	Description
DMA Controller #1		
0000H	R/W	Channel 0 current address
0001H	R/W	Channel 0 current word count
0002H	R/W	Channel 1 current address
0003H	R/W	Channel 1 current word count
0004H	R/W	Channel 2 current address
0005H	R/W	Channel 2 current word count
0006H	R/W	Channel 3 current address
0007H	R/W	Channel 3 current word count
0008H	R/W	Command/Status Register
0009H	R/W	Request Register
000AH	R/W	Single Bit Mask Register
000BH	R/W	Mode Register
000CH	R/W	Clear Byte Pointer
000DH	R/W	Master Clear
000EH	R/W	Clear Mask Register
000FH	R/W	Write All Mask Register Bit
Programmable Interrupt Controller #1		
0020H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte

Addr Port	Read/ Write	Description
0021H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)
0023H		Reserved
0024H	R/W	Configuration Data Port
0028H	R/W	Configuration Address Port
0029H - 003FH		Reserved
Timer/Counter		
0040H	R/W	Timer 0 Count Load/Read
0041H	R/W	Timer 1 Count Load/Read
0042H	R/W	Timer 2 Count Load/Read
0043H	W	Timer Control Word
0044H - 005FH		Reserved
Write Keyboard Controller		
0060H	R/W	Keyboard Data
0062H - 0063H		Reserved
0064H	R/W	Keyboard Control/Status
Port B		
0061H	R/W	Port B Status Port
Real Time Clock		
0070H	W	Real-Time Clock Index and NMI Mask
0071H	R/W	Real-Time Clock Data Port
DMA Page Registers		
0080H	R/W	Not Used
0081H	R/W	Channel 2 Page Register
0082H	R/W	Channel 3 Page Register
0083H	R/W	Channel 1 Page Register
0087H	R/W	Channel 0 Page Register
0089H	R/W	Channel 6 Page Register

Addr Port	Read/ Write	Description
008AH	R/W	Channel 7 Page Register
008BH	R/W	Channel 5 Page Register
System Control Port		
0090H - 0091H		Reserved
0092H	R/W	System Control Port
0093H - 009FH		Reserved
Programmable Interrupt Controller #2		
00A0H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte
00A1H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)
DMA Controller #2		
00C0H	R/W	Channel 0 current address
00C2H	R/W	Channel 0 current word count
00C4H	R/W	Channel 1 current address
00C6H	R/W	Channel 1 current word count
00C8H	R/W	Channel 2 current address
00CAH	R/W	Channel 2 current word count
00CCH	R/W	Channel 3 current address
00CEH	R/W	Channel 3 current word count
00D0H	R/W	Command/Status
00D2H	R/W	Request Register
00D4H	R/W	Single Bit Mask Register
00D6H	R/W	Mode Register

Addr Port	Read/ Write	Description
00D8H	R/W	Clear Byte Pointer
00DAH	R/W	Master Clear
00DCH	R/W	Clear Mask Register
00DEH	R/W	Write All Mask Register Bit
00DFH - 00EFH		Reserved
Extended DMA Page Registers		
0480H	R/W	Not Used
0481H	R/W	Channel 2 Extended Page Register
0482H	R/W	Channel 3 Extended Page Register
0483H	R/W	Channel 1 Extended Page Register
0487H	R/W	Channel 0 Extended Page Register
0489H	R/W	Channel 6 Extended Page Register
048AH	R/W	Channel 7 Extended Page Register
048BH	R/W	Channel 5 Extended Page Register

7. MEGAFUNCTIONS

This block of the HT321 contains the standard AT Compatible Megafunctions necessary for the implementation of an AT-Compatible system and ISA bus. Within this module are the equivalents of two Intel 8237 DMA Controllers, two 8259 Intel Interrupt Controllers and one Intel 8254 Programmable Interval Timer. All the support logic necessary to implement and clock these devices is also included. Below is a brief description of each of the Megafunctions in this block. This information, together with the detailed Register Description for these devices located in the REGISTER DESCRIPTION section of this data sheet, should provide the user with enough information to properly program and use these devices. If further information is required, please examine the IBM AT Technical Reference manual or the Intel Data Sheet for the particular device in question.

DMA Controller

The HT321 contains two DMA controllers that are compatible with an Intel 8237. Each controller is a four-channel DMA device that can generate the Control Signals and Memory Addresses necessary to transfer information between a Peripheral Device and Memory. The DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection for the two DMA devices.

This arrangement is used to maintain IBM PC AT bus compatibility as documented by the IEEE P996 specification. The DMA functions are arbitrated by internal logic and will gain control of the Local Bus as a Temporary Bus master. To facilitate this operation, the HT321 utilizes the HOLD/HLDA protocol of the microprocessor.

The DMA Controller is clocked via one of two sources:

i) for AT-Compatibility, the DMA Controllers can be clocked with BCLK/2 (4 MHz),

or

ii) for systems requiring greater DMA performance, the DMA Controller can be clocked by BCLK (8 MHz).

The clock for the DMA Controllers is selected via INDEX 06 of the HT321. INDEX 06 also controls the DMA Wait States. The option ranges from 0 to 3 additional Wait States inserted into any DMA cycle generated. For AT-Compatibility, the setting should be at 1 Wait State.

Interrupt Controller

The HT321 incorporates two programmable Interrupt Controllers that are functionally compatible to an Intel 8259A. The controllers accept Interrupt Requests from Peripherals, resolve Priority between pending interrupts and interrupts in service, issue an interrupt request to the CPU and supply a vector which is used as an index by the CPU to select the service routine to execute.

A variety of Priority Assignment Modes is provided, which may be changed at any time during system operation to allow the complete interrupt subsystem to be restructured based on the Operating System requirements. The controllers are cascaded in a fashion compatible with the IBM PC AT and the IEEE AT Bus P996 Specification .

The table below shows typical interrupt levels assigned for an AT-compatible I/O bus.

The two devices are coupled in chain fashion by connecting the interrupt output of Programmable Interrupt Controller 2

(PIC2) to the interrupt request input 2 of PIC1. To ensure that all 16 interrupt channels operate correctly in this arrangement, all channels must be programmed to operate in Cascade Mode. PIC1 is located at addresses 020H - 021H and is configured for Master operation in Cascade Mode. PIC2 is a Slave device and is located at addresses 0A0H - 0A1H(see definitions below). The address location and Cascade interconnection provides compatibility with the IEEE AT Bus P996 Specification.

Two additional connections are made to the interrupt request inputs of PICs 1 and 2. The output of Timer 0 in the Counter/Timer Megafunction is connected directly to the input of Channel 0 (IRQ) of PIC1 and does not have an external connection. In a standard AT system implementation, IRQ1 is reserved exclusively for the Keyboard Output Buffer Full Flag. Therefore, the input pin for this interrupt has been named OPTBUFUL, or Output Buffer Full, and should only be used as an input from a Keyboard Controller. IRQ8 differs from the other IRQ's in that it has an inverter between the input pin and PIC2.

Interrupt	System Functions	I/O Bus
NMI	Parity Check	I/OCHCK
IRQ0	Timer	Not Available
IRQ1	Keyboard	Not Available
IRQ3	Serial Port 2	Available
IRQ4	Serial Port 1	Available
IRQ5	Parallel Port 2	Available
IRQ6	Floppy Disk	Available
IRQ7	Parallel Port 1	Available
IRQ8	Real Time Clk	Not Available
IRQ9	Not Used	Available
IRQ10	Not Used	Available
IRQ11	Not Used	Available

Typical System Interrupts and AT-compatible I/O Channel

Programmable Interval Timer

The HT321 integrates a Programmable Interval Timer (PIT), which is functionally equivalent to an Intel 8254 Programmable Interval Timer/Counter. The PIT is programmable through internal I/O ports located at 0040H through 0043H.

The Clock inputs of the three channels are driven by a 1.19 MHz clock, which is internally generated by dividing the oscillator input (OSC P160 14.31818 MHz) by 12. The outputs of the three channels are as follows:

- Channel 0 is a general purpose and software interrupt timer. The output of this channel is connected directly to the IRQ0 pin of the integral Programmable Interrupt Controller (PIC1). (see

the Interrupt Controller Functional Description)

- The output of Channel 1 is used internally by the HT321 to generate refresh requests.
- The output of Channel 2 provides for tone generation for a speaker. The HT321 presents this signal as SPeaKeR (SPKR P78).

Programmable Timer Control

The Programmable Interval Timer (PIT) in the HT321 is general purpose and can be used to generate accurate time delays under software control. The PIT contains three 16-bit counters (Counter[0:2]) which may be programmed as Binary or Binary Code Decimal (BCD) counters. Each counter operates independently of the other two and each can operate as a Timer or Counter.

The counters have common control logic that decodes control information written to the PIT and has the necessary controls to load, read, configure and direct each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the lack of an external hardware trigger signal. Counter 2 can be operated in any of six modes listed below.

Mode 0 - Interrupt on terminal count

Mode 1 - Hardware re-triggerable one-shot

Mode 2 - Rate generator

Mode 3 - Square wave generator

Mode 4 - Software triggered strobe

Mode 5 - Hardware re-triggerable strobe

Introduction

The HT342 is a high performance, pipelined DRAM controller and Write Buffer. The Controller interfaces to '486 Systems with minimum support logic. The Controller conforms to the Local Bus Specification.

The primary purpose of the HT342 Memory Control Unit (MCU) is to provide the interface to DRAM for the Shasta system. Two other non-memory related functions have also been assigned to the chip: the AT-compatible numerical error reporting and 16-bit cycle data bridging.

A 4-level write buffer facilitates 0 wait state write cycles as long as the write buffers are not full. A superior set of DRAM control algorithms have been defined that effectively utilize pipelined techniques and optimize zero wait state performance, even during write cycles on a page hit at maximum operating frequencies. This, combined with write buffering, effectively make all write cycles 0 wait state.

At lower operating frequencies the DRAM control section of the HT342 allows a 3-1-1-1 486 burst read cycle sequence during DRAM page hits in a CAS interleaved paging configuration. When the clock rate is higher, and the DRAM access times do not meet the 3-1-1-1 burst cycle timing requirements, a special data pipe can be activated relaxing the DRAM access time constraints. In this case 4-1-1-1 burst cycle can be achieved and save 3 wait states over 4-2-2-2 burst cycle timing.

Because of the 486 CPU bus specification, 16-bit cycles on the Local Bus require data bridging. The HT342 MCU controller provides the necessary circuitry. No extra logic is necessary for 16-bit device support. This is especially important because the HT321 ISA controller and some local bus VGA controllers (like the HT216) are 16-bit devices. The HT342 MCU allows these devices to be connnected to the Local Bus with no external bridging buffers.

Outlined below are the major features of the controller:

- One 184 pin PQFP package.
- 1 micron HCMOS Technology.
- Fully static operation: 0-33MHz CPU speeds.
- Shasta architecture compatible.
- LIM EMS 4.0 support.
- Separate Data Bus for DRAMs and Local Bus.
- Parity generation, detection and reporting.
- 256K, 1MB, 4MB, 16MB DRAM type support.
- Up to 256MB total addressability (4 banks of 16Mb DRAMs).
- Shadowing in 16KB increments between 640KB and 1MB.
- Up to 384KB of memory, from 640KB to 1MB, may be remapped above the main memory limit. Re-mapping coexists with Shadowing, meaning any remaining unshadowed DRAM may be re-mapped above the main memory limits.
- 1, 2, 4-way CAS interleave with fast paging.
- Middle BIOS support enable/disable.
- Programmable 26 Non-Cacheable regions.
- Refresh hidden from the system.
- CAS before RAS or RAS only Refresh.
- RAS staggering during Refresh.
- Programmable Timing Parameters for DRAM access.
- Read and Write Cycle Timing independently programmable.

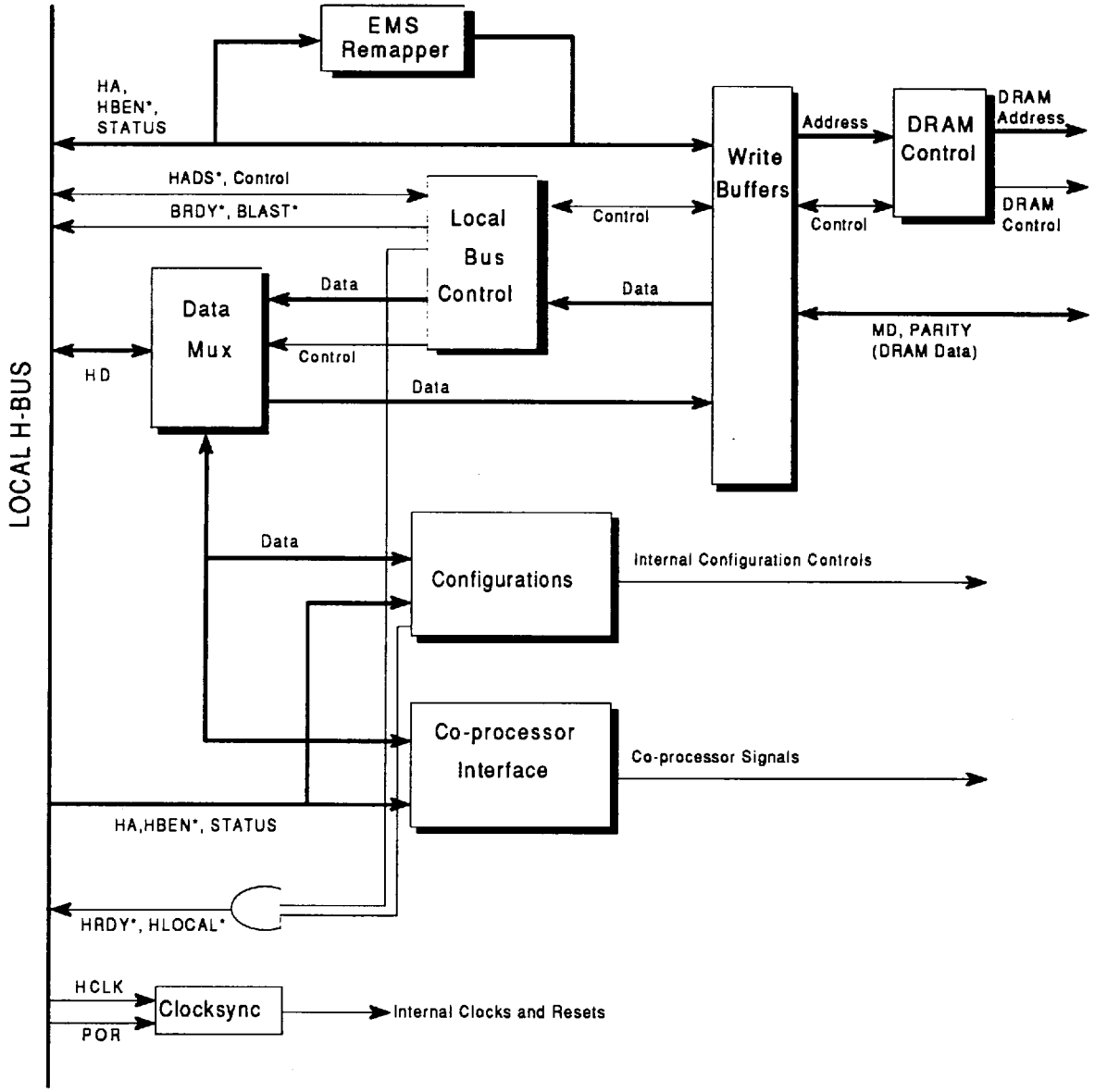


Figure 2.26 - HT342 MCU Internal Block Diagram

- 3-1-1-1 486 burst rate during DRAM page hits while interleaving.
- Data pipe relaxing DRAM timing constraints at higher clock rates, potential saving of 3 wait states with a 4-1-1-1 burst cycle.
- 4 deep double-word write buffering.
- Byte gathering support.
- Out of order operation (reads propagate ahead of writes if there is no hit in the write buffers).
- Ability to respond from within the write buffer for a Write Buffer Read Hit.
- AT-compatible floating point error reporting.

Architecture

The HT342 has three major operational sections: Local Bus Controller, Write Buffers and a DRAM Controller implementing complete DRAM Control functions. These three major modules, which are shown in the Block Diagram on Page 34, are called LOCAL_BUS_CONTROLLER, WRITE_BUFFERS and DRAM_CONTROLLER respectively. The LOCAL_BUS_CONTROLLER provides DRAM cycle recognition, EMS and Remap cycle handling, 16-bit data bridging and burst read data pipe.

The WRITE_BUFFERS and DRAM_CONTROLLER are organized in a pipelined fashion. The WRITE_BUFFERS module generates cycles for the DRAM_CONTROLLER module as a stage of the pipeline. These mega-modules are distinct and independent entities. Their functions are described below.

Local Bus Controller

The first task of this module is to qualify cycles. The module samples decodes from the DRAM_DECODER module, and the HLOCALI* input. The following cycles are qualified by the module as the HT342 MCU cycles:

- regular memory DRAM cycles. These cycles are passed immediately by the LOCAL_BUS_CONTROLLER to the WRITE_BUFFERS module.
- two of the 486 special cycles : flush and write back. These cycles are terminated by the LOCAL_BUS_CONTROLLER.

The following cycles require special attention and are described in detail:

- non-DRAM and non-special CPU read cycles for which HLOCALI* is sampled de-asserted and HBEN1* and HBEN0* are BOTH negated;
- non-DRAM and non-special CPU write cycles, for which HLOCALI* is sampled de-asserted, and HBEN1* and HBEN0* are BOTH negated.

These cycles are assumed by the HT342 to be directed toward 16-bit devices. The read cycles are not terminated by the HT342 MCU controller, but the read bridging is performed. The bridging during the read cycles is necessary, because the 486 processor expects the read data on the data bus lines (HD[31:0] bus) associated with the byte enables (HBEN*[3:0]) activated during the cycle. This occurs regardless of the bus sizing information supplied with the BS16 signal. Although the CPU knows that a 16-bit device does not have the upper 16 bit data bus connected, it still expects to see the data there. Therefore the bridging is necessary for all memory and I/O read cycles directed to 16-bit devices, when the HBEN1* and HBEN0* signals are negated. When any one of the signals is asserted, and the cycle is directed to a 16-bit device, the CPU reads the data associated with the HBEN1* and/or HBEN0* first, and then repeats the cycle (if necessary) with the HBEN1* and HBEN0* negated. This second, repeated cycle requires bridging of

the data returned by the 16-bit device. The HT342 MCU controller reads the data on the lower part of the data bus (HD[15:0]), and mirrors it on the upper one (HD31:16).

An even more complicated process takes place during write cycles to 16-bit devices. The 486 CPU does not mirror the upper 16 bits of the data bus on the lower 16 bits, when performing a write cycle with both HBEN*1 and HBEN*0 signals negated. Therefore a 16-bit device cannot read the data, since it does not have access to the upper 16 bits of the data bus. What makes things even worse, the 486 CPU still drives the lower 16 bits of the data bus with some invalid data. A complex set of data buffers would be needed to bridge the data during these cycles. The HT342 MCU controller takes care of the problem in an unusual way. The controller samples the write bridging condition and determines if the cycle is directed to a 16-bit device by sampling the HLOCALI* one clock after the HADS*. If the HLOCALI* is asserted, the cycle is assumed to be directed to a 32-bit local device and no action is taken. Otherwise the cycle is taken over by the MCU controller by asserting the HLOCAL* signal, and a BOFF* cycle is requested. At the same time the address and the write data from the CPU is stored internally and the cycle is terminated. One clock after the BOFF* is asserted, the CPU releases the entire Local Bus. The HT342 starts driving the bus one clock later and it repeats the stored cycle with the HD[31:16] lines mirrored on HD[15:0] lines. In this way the HT342 acts as a local bus master and emulates the behavior of the 386 CPU for the write cycles directed toward 16-bit devices. The overhead involved is minimum. There is a 6 clock penalty for these cycles. These cycles are usually much slower anyway (most of them are backplane cycles). The LOCAL_BUS_CONTROLLER is the module controlling BOFF cycles. Fig. 2.27 illustrates a BOFF* cycle. The AHOLD and BOFF* signals are used to take control of the Shasta Local Bus. The second cycle is generated by the HT342 MCU controller and the HD[31:16] part of the data bus is duplicated on the HD[15:0]. Fig. 2.28 shows an aborted BOFF* cycle. The HT342 does not initiate a BOFF* cycle after HLOCALI* is asserted.

Another function of the LOCAL_BUS_CONTROLLER is the control of burst DRAM cycles. The HT342 MCU controller always bursts cacheable DRAM read cycles. BRDY* is generated while bursting and HRDY* terminates the last cycle in the burst sequence. Fig. 2.29a shows a fastest possible sequence of a read burst cycle. This sequence occurs on a DRAM page hit, with the CAS active time during read set to 1 HCLK, and interleave option turned on, no CAS delays, no bus recoveries, etc.. The data pipe is not enabled. A 3-1-1-1 burst is performed. Fig. 2.29b shows the same cycle with 1 wait state added to every CAS cycle. The CAS active time has been set to 2 HCLK. This happens usually at higher operating frequencies, when the CAS access time of 1 HCLK is too short. In this case a 4-2-2-2 burst is performed. Possible advantages of the data pipe are shown by Figure 2.30 . When the pipe is disabled, the data coming back from the DRAM has to go through the HT342 MCU controller, heavily loaded Local Bus, and then meet the CPU setup requirements. By enabling the pipe, the only requirement the DRAM data has to meet is setup on the MD bus of the HT342. This relaxes the timing significantly, especially at higher operating frequencies. The 4-2-2-2 burst sequence shown in Fig. 2.29b can be shrunk down to 4-1-1-1, when the data pipe is enabled as shown by Fig. 2.30.

The last function of the LOCAL_BUS_CONTROLLER is to control the DRAM cycles in the EMS and Remap cases. Whenever an EMS or Remap translation is required, a wait state is added to the cycle in order to allow time for MA lines calculation.

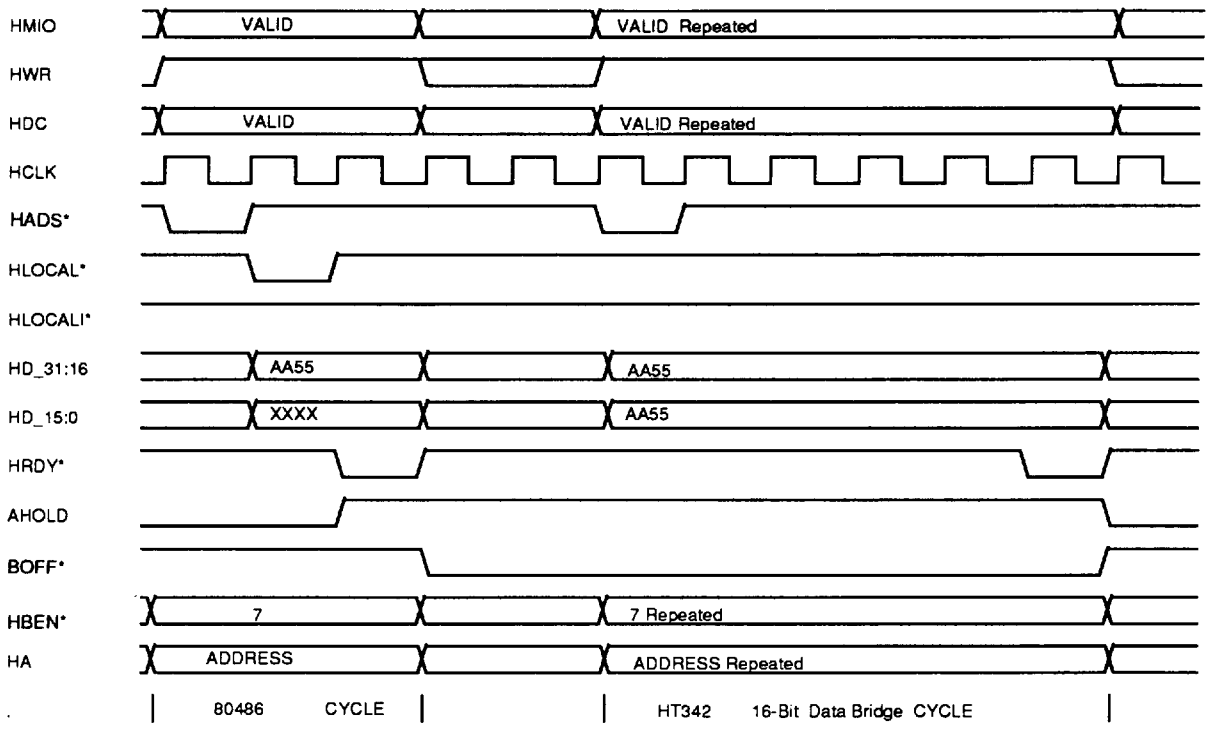


Figure 2.27 - BOFF Data Bridge Cycle

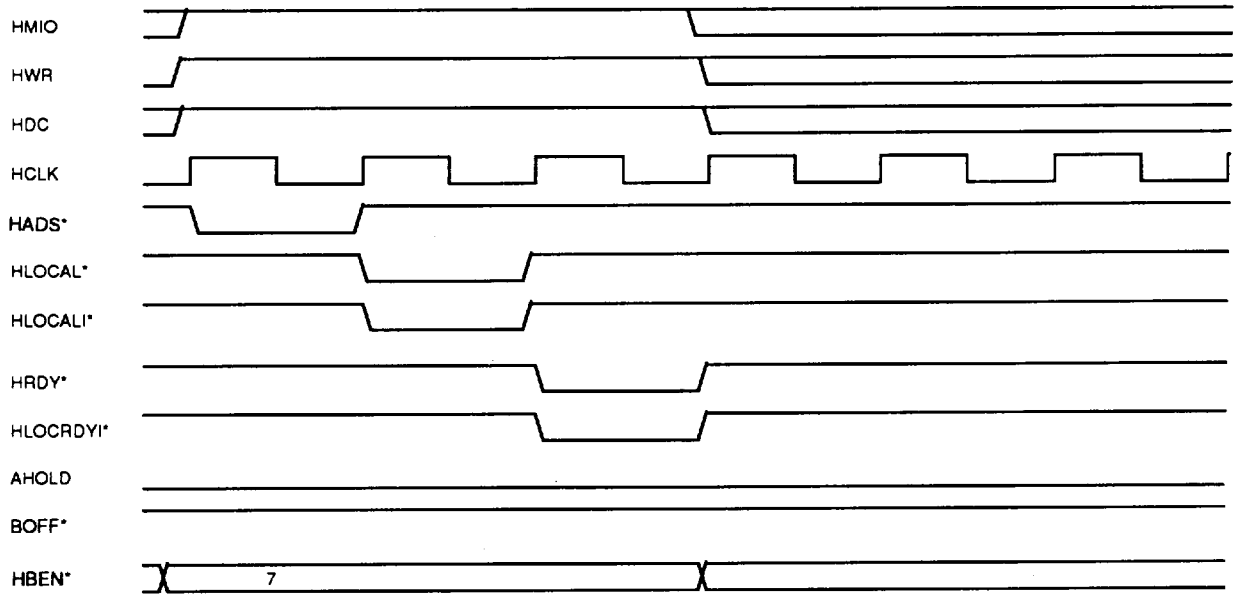


Figure 2.28 - Aborted BOFF Cycle

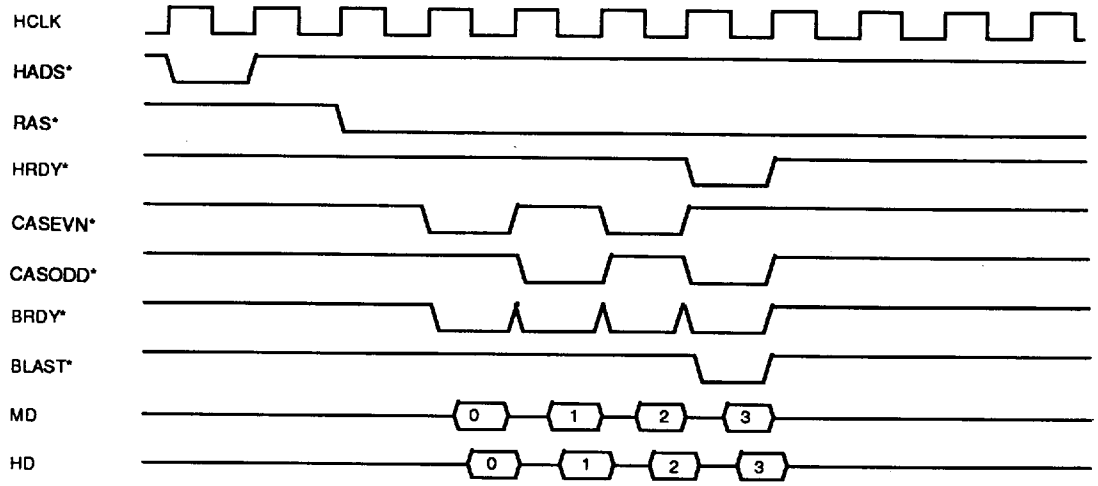


Figure 2.29a - Burst Cycle - Data Pipe Off - 0 Wait State

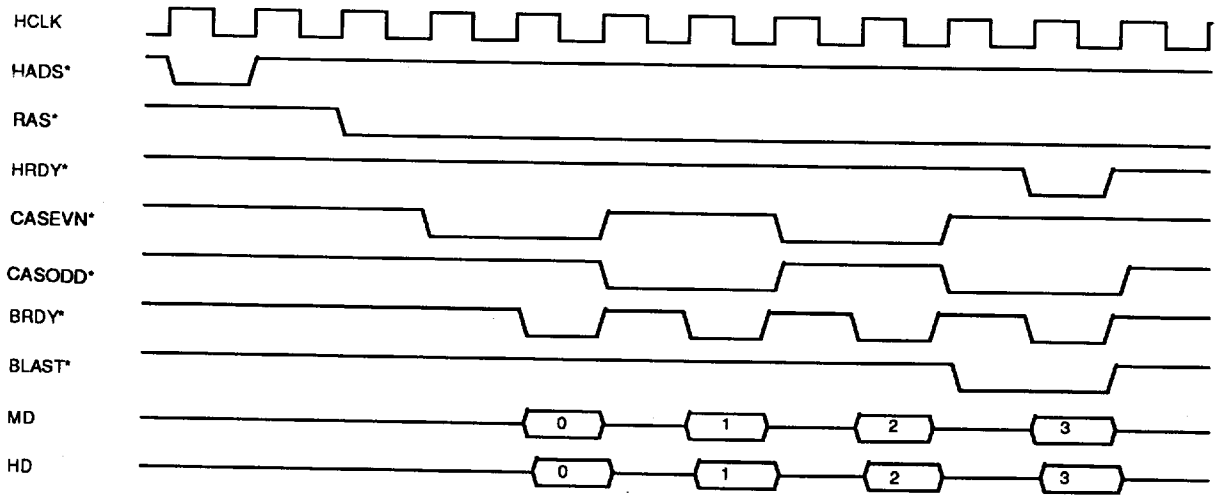


Figure 2.29b - Burst Cycle - Data Pipe Off - 1 Wait State

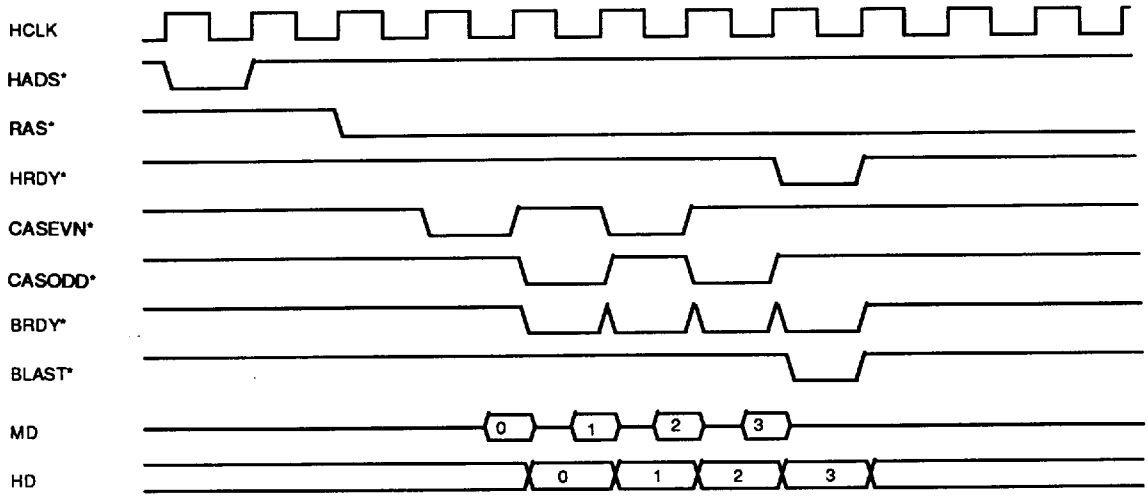


Figure 2.30 - Burst Cycle - Data Pipe On - 0 Wait State

Write Buffers

One of the major functions of the HT342 is buffering of write data. The module WRITE_BUFFERS controls cycles on the DRAM_CONTROLLER local bus.

Whenever one of the write buffers fills, the WRITE_BUFFERS module starts its unload sequence by generating cycles on the DRAM_CONTROLLER local bus. Write cycles from the module are always FIFO.

An important feature of the WRITE_BUFFERS module is byte gathering. This feature checks if data being written to the WRITE_BUFFERS happens to be a 'Write Buffer Write Hit' (an address match for the data of the cycle occurs for data already in the WRITE_BUFFERS, queued for unload) then the data will be directed to the write buffer where the match occurred. Multiple hits are impossible. This aligns with the 16-bit nature of current software written for '286 machines to be run on Shasta '486 Systems.

Another feature of the WRITE_BUFFERS module is out of order operation. Any read cycle will be processed before any write unload cycle, eliminating slow down by the collision of cache read miss cycles with latency of the write buffer unloads. This feature is tightly coupled with another feature of the WRITE_BUFFERS, which is an ability to respond from its buffers to a Write Buffer Read Hit. Typically, for Write Buffer Read Hits only a part of the data requested is present in the write buffer; the remainder is fetched from the DRAM.

DRAM_CONTROLLER

The third major unit of the HT342 is the DRAM_CONTROLLER. This unit provides all DRAM control algorithms.

The DRAM_CONTROLLER supports up to 4 banks of DRAM memory of 256KB, 1MB, 4MB and 16MB types. Any combination of these types of DRAM memory may be used, meaning it is possible to install any type of DRAM in any bank. From one to four banks may be used. This provides for unlimited flexibility of system upgrade. The DRAM_CONTROLLER supports programmable 2-way or 4-way CAS interleave. It is possible to select 2-way interleaving between two lower banks and between two upper banks, or between lower and upper banks. For 4-way interleave, all 4 banks must be installed. The interleaved banks must be populated by the same type of DRAMs. The HA2 address line determines 2-way CAS interleave. HA2 and HA3 are used for 4-way interleave.

Fast paging is also supported by the DRAM_CONTROLLER. Internal Pipelined Local Buses between the WRITE_BUFFERS and DRAM_CONTROLLER have bursting capability.This technique along, with the CAS interleaved scheme of DRAM control, provides faster burst cycles.

The tables below describe mapping of the HA to MA lines :

A. No Interleave

MA	0	1	2	3	4	5	6	7	8	9	10	11
CAS Address	HA2	HA3	HA4	HA5	HA6	HA7	HA8	HA9	HA10	HA11	HA12	HA13
RAS Address	X	Y	Z	HA14	HA15	HA16	HA17	HA18	HA19	HA20	HA21	HA22

where:	X	Y	Z	
	HA11	HA12	HA13	for 256K DRAMs
	HA12	HA13	HA21	for 1M DRAMs
	HA13	HA22	HA23	for 4M DRAMs
	HA23	HA24	HA25	for 16M DRAMs

B. 2-way Interleave

MA	0	1	2	3	4	5	6	7	8	9	10	11
CAS Address	HA3	HA4	HA5	HA6	HA7	HA8	HA9	HA10	HA11	HA12	HA13	HA14
RAS Address	X	Y	Z	HA15	HA16	HA17	HA18	HA19	HA20	HA21	HA22	HA23

where:	X	Y	Z	
	HA12	HA13	HA14	for 256K DRAMs
	HA13	HA14	HA22	for 1M DRAMs
	HA14	HA23	HA24	for 4M DRAMs
	HA24	HA25	HA26	for 16M DRAMs

C. 4-way Interleave

MA	0	1	2	3	4	5	6	7	8	9	10	11
CAS Address	HA4	HA5	HA6	HA7	HA8	HA9	HA10	HA11	HA12	HA13	HA14	HA15
RAS Address	X	Y	Z	HA16	HA17	HA18	HA19	HA20	HA21	HA22	HA23	HA24

where:	X	Y	Z	
	HA13	HA14	HA15	for 256K DRAMs
	HA14	HA15	HA23	for 1M DRAMs
	HA15	HA24	HA25	for 4M DRAMs
	HA25	HA26	HA27	for 16M DRAMs

RAS only or CAS before RAS Refresh methods are supported. Internal refresh counters generate refresh addresses during RAS only refresh. The RAS signals during refresh can be staggered.

A powerful set of Timing Options has been implemented, allowing the user to adjust timing to suit specific system and DRAM speeds:

a) RAS delay - 0 or 1 HCLK (Index 27H, Bit 7)

Selects MA setup time on RAS. For zero RAS delay setup time becomes 1 HCLK +/-system and internal delays. For 1 RAS delay the setup time is 1 HCLK longer.

b) CAS delay - 1 or 2 HCLK (Index 26H, Writes Bit 4, Reads Bit 3)

This parameter defines RAS to CAS delay. Switching MA lines from RAS to CAS Address always occurs in the middle of the delay. This parameter controls MA setup time to CAS, and MA hold time for RAS.

Separate CAS delay for read and write may be defined. This is possible because while paging write cycles are pipelined, the setup time for MA to CAS during a page hit is improved significantly compared to read cycles.

c) RAS Active time on Reads 2 to 9 HCLK in one clock increments. (Index 27H, Bits 4-2)

This parameter is determined by DRAM Specification of Read access time from RAS.

d) RAS Active time for Writes 2, 3, 4 or 5 HCLK. (Index27H, Bits 6-5)

This parameter is determined by DRAM minimum RAS width specification.

e) RAS precharge time - 1 to 4 HCLK (Index 27H, Bits 1-0)

f) CAS active time on reads-1 to 4 HCLK (Index 26H, Bits 1-0)

Determined by DRAM specification of read access time from CAS.

g) CAS active time on writes-1 to 2 HCLK (Index 26H, Bit 2)

Determined by DRAM specification of minimum CAS width and CAS data hold time on CAS.

h) CAS precharge - 0.5 or 1 HCLK (Index 26H, Bit 6)

i) Bus Recovery time - 0 , 0.5 or 1 HCLK (Index 2DH, Bits 1-0)

This parameter affects back to back CAS signals switched to alternate banks when interleaving is enabled. If there is no Recovery time specified the CAS signals will happen back to back while bursting. Specifying a Recovery time creates the inactive delay required for all CAS signals between consecutive Dword fetches.

j) First CAS burst read delay - 0 or 1 HCLK (Index 26H, Bit 5)

One more wait state will be inserted during the first cycle of a burst during a page hit on a read miss cycle. This parameter is determined by the DRAM specification of address access time during a page hit.

k) CAS Hold on RAS - 1 or 2 HCLK (Index 26H, Bit 7)

Applies to CAS before RAS Refresh timing. Sets the delay between the RAS being activated and CAS deactivated during the cycle.

Figures 2.34 and 2.35 illustrate basic RAS/CAS Read and Write Cycles with paging disabled. The differences are: WEN is not activated during a Read Cycle and the

timing control parameters are from separate configuration registers. tRAR/tRAW parameters refer to RAS active time on Reads/Writes (respectively), tCDR/tCDW to CAS delay on Reads/Writes, tCAR/tCAW to CAS active time on Reads/Writes, and TRP to RAS precharge.

Figure 2.31 illustrates the basic RAS/CAS Cycle with paging and no interleave. The TCP parameter refers to CAS precharge. BANKSELEVN (BANKSELODD) signals are stable throughout the cycle.

Figure 2.32 illustrates the basic RAS/CAS Cycle with Paging and 2-way Interleave. BANKSELEVN and BANKSELODD are stable throughout the cycle. The figure shows consecutive dwords accessed in an interleaved fashion with the HA2 Address line as the Interleave control. TBR refers to the Bus Recovery parameter described above.

Figure 2.33 illustrates the basic CAS/RAS cycle with Paging and 4-way Interleave. BANKSELEVN and BANKSELODD are controlling CAS activation. There is always at least a half HCLK Setup and Hold time provided when switching CASEVN* and CASODD* between banks. The figure shows consecutive Dwords accessed in an interleaved fashion with HA2/HA3 as the interleave controls.

Figure 2.36 illustrates the CAS before RAS Refresh Cycle. tCHR refers to the minimum timing parameter of CAS Hold on RAS described above, while figure 2.37 illustrates the RAS-only Refresh Cycle. The width of the RAS signal during refresh cycles is determined by tRAW. The width of the CAS signals during CAS before RAS refresh is determined by tCHR and tCAW.

Co-processor Interface

This module implements the AT compatible numerical error reporting. Fig. 2.38 illustrates the timing. Upon sampling the FERR* line asserted, the IRQ13 interrupt is generated. An I/O write to F0h clears the IRQ13 request. At the same time IGNERR* signal is asserted and remains active until FERR* line is negated.

Clock Sync

This module generates internal clocks and resets for the HT342.

DRAM Decoder

The purpose of this module is to generate an internal signal called DRAM_SPACE. This signal determines whether a cycle is targeted at the DRAM subsystem controlled by the HT342. It is exclusively resolved when HADS* is sampled as asserted.

Data Mux

This module provides multiplexing of the output data. The multiplexing occurs between data being read from configuration registers and data from the DRAM memory. The module also bridges data bytes during DMA cycles, if the necessity arises. (This occurs because the HT321 is a 16-bit device and it is the only source of DMA cycles). The bridging appears between lower (HD[0:15]) and upper (HD[16:31]) data bits.The bridging occurs also during cycles targeted to a 16-bit device. The bridging is controlled by the LOCAL_BUS_CONTROLLER.

Ems Remapper

EMS_REMAPPER is an address translator which changes the current host's Local Bus addresses (HA lines) into physical DRAM subsystem addresses. These addresses reflect the remapping and EMS support schemes. Essentially, the DRAM subsystem is viewed as a contiguous memory. During remapping (if the remap function is enabled) the EMS_REMAPPER changes the host request at some high address above DRAM space to one of the EMS pages (16K memory chunks between 640KB and 1MB address space). For the EMS support, an EMS page address is changed to a high memory (but existing in the DRAM subsystem) address according to an offset loaded by the user in the configuration registers.

Configurations

This module combines all configuration registers which provide the programmability of the HT342. These registers are defined in the HT342 Register descriptions in this data book.

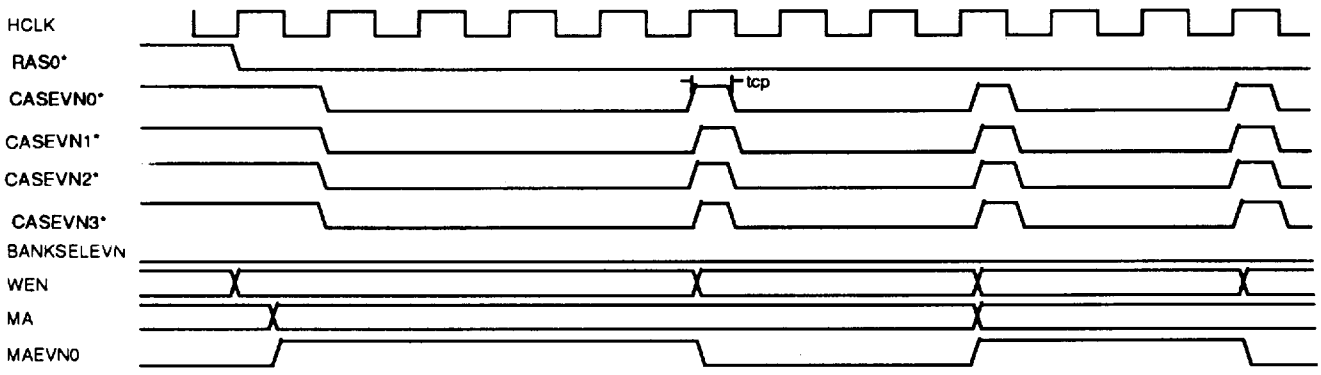


Figure 2.31 - RAS/CAS Cycle Page Mode On; Interleave Off

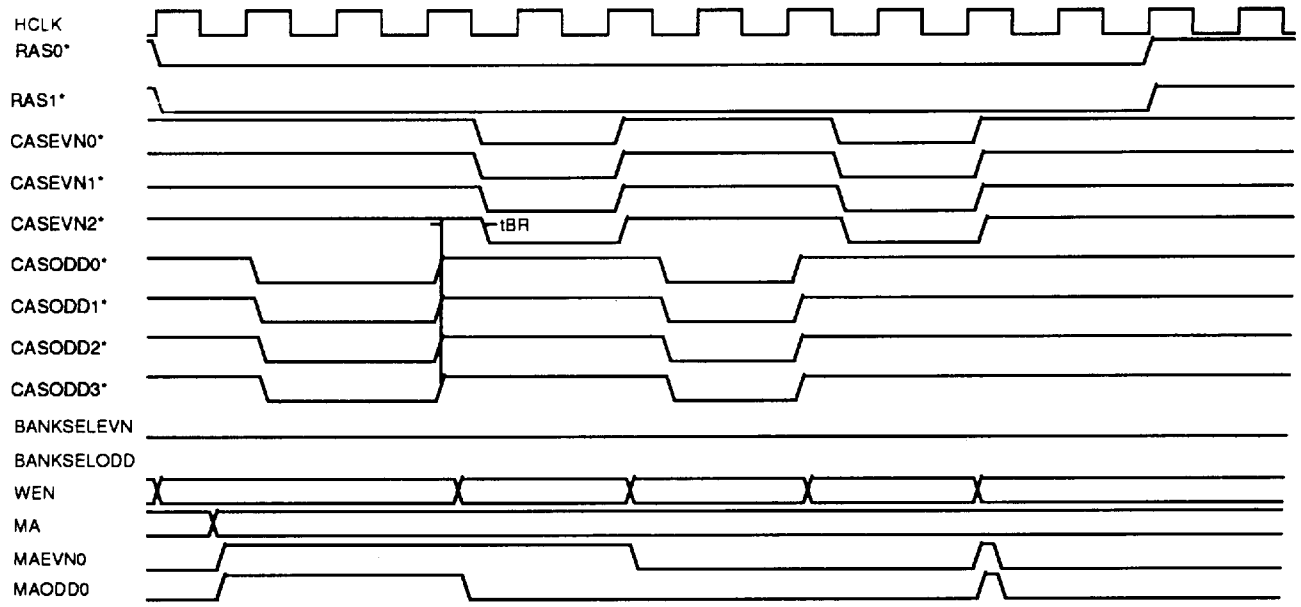


Figure 2.32 - RAS/CAS Cycle Page Mode On; Two-Way Interleave

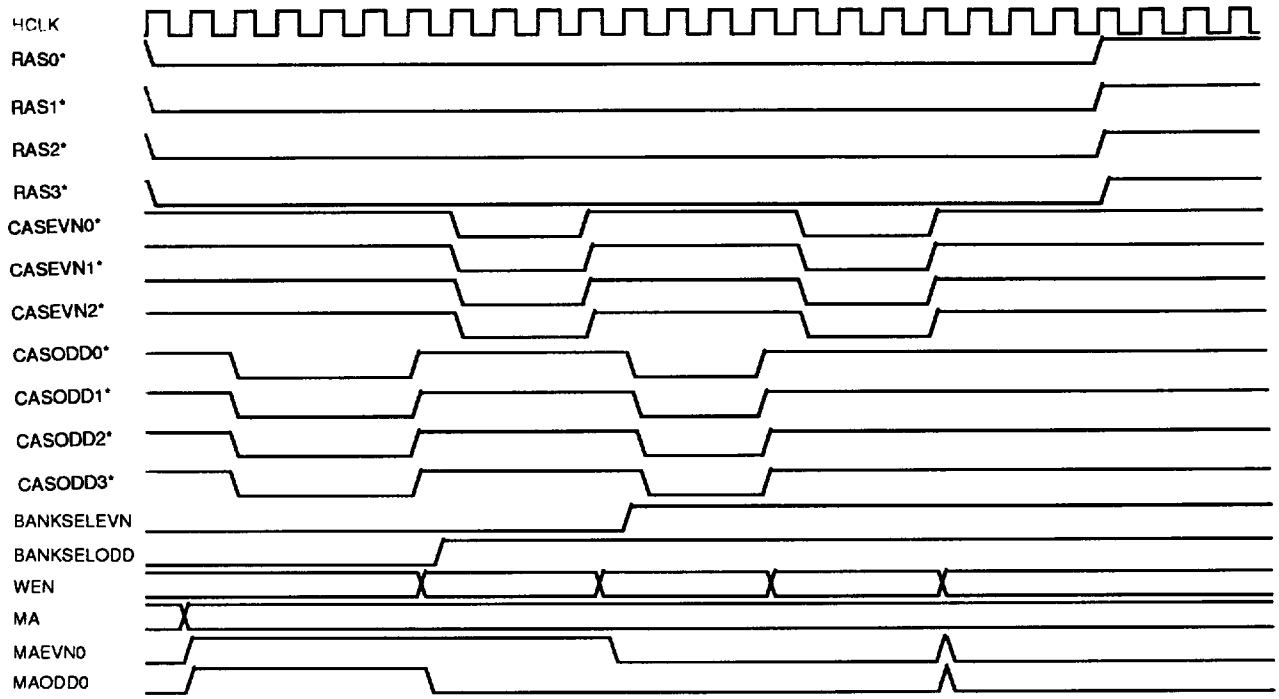


Figure 2.33 - RAS/CAS Cycle Page Mode On; Four-Way Interleave

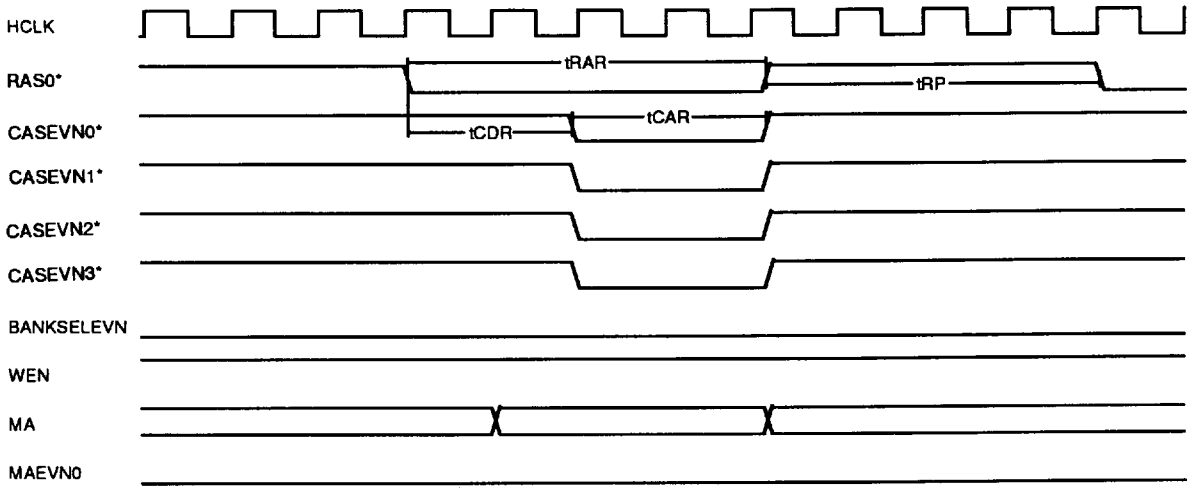


Figure 2.34 - RAS/CAS Read Cycle Page Mode Off

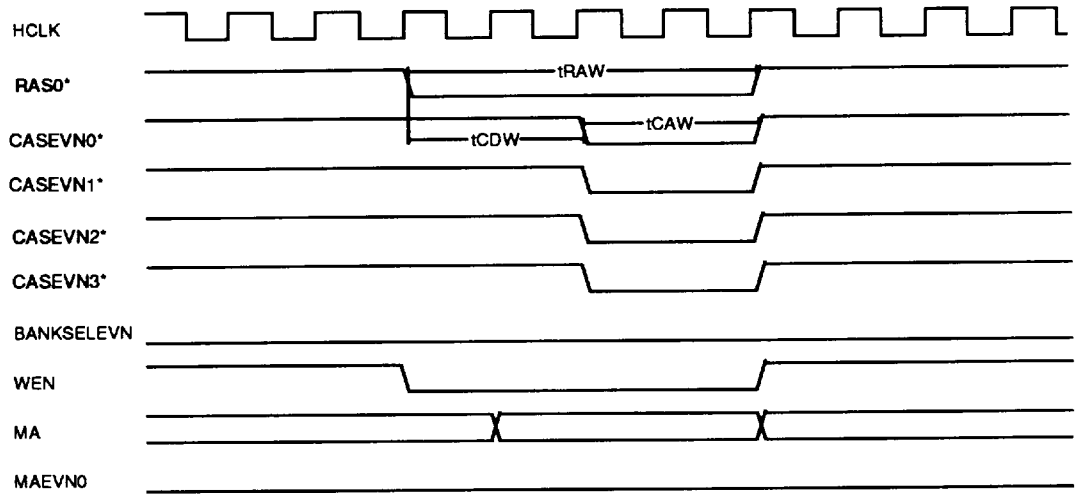


Figure 2.35 - RAS/CAS Write Cycle Page Mode Off

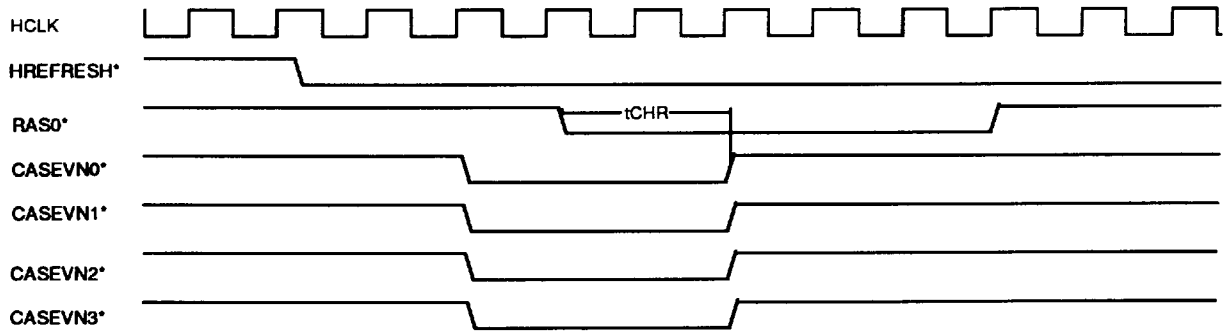


Figure 2.36 - CAS before RAS Refresh Cycle

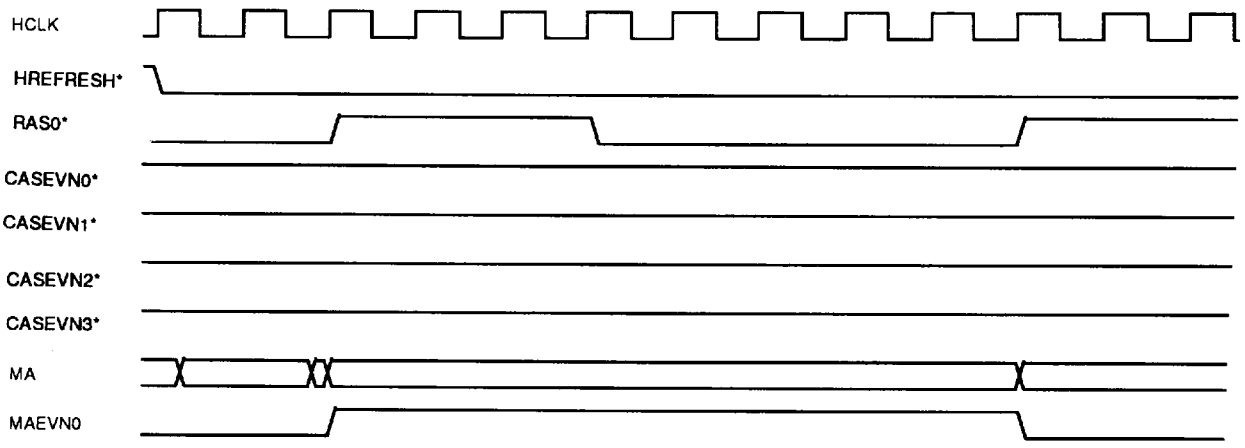


Figure 2.37 - RAS-only Refresh Cycle

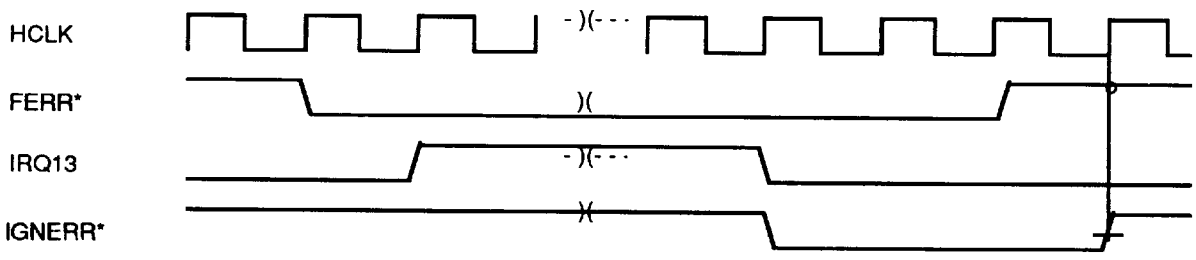


Figure 2.38 - AT Error Reporting

HT321 Register Descriptions

The HT321 chip has a total of 32 INDEX locations mapped into INDEX 00 - 1FH. Only the bits mentioned in this text should be programmed. All unused register bits should be left at default to maintain future compatibility.

The HT321 chip is also responsible for holding the current INDEX Pointer Value even when the Target Value is external to the HT321. Any access to I/O location 28H (CNFGASLO) is therefore terminated by the HT321. The data read at this location is made available to the CPU.

To program the INDEX registers, one must execute the following procedure:

i) Write I/O Location 28H with Value = INDEX (00 - 1FH for HT321)

ii) Write to I/O Location 24H with Control Value for the selected INDEX

To Read INDEX registers, execute the following procedure:

i) I/O Write Location 28H with Value = INDEX (00 - 1FH for HT321)

ii) I/O READ Location 24H - Control Value of selected INDEX is presented

To read the INDEX pointer value , one must execute the following procedure:

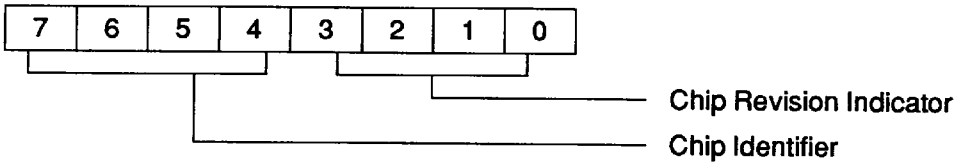
i) I/O READ Location 28H - INDEX ADDRESS (lower byte) presented

When an INDEX pointer is written to I/O location 28H, the pointer remains until another I/O write to 28H. This allows multiple DATA accesses at the INDEXed register .

At POR the INDEX pointer will default to INDEX 00H.

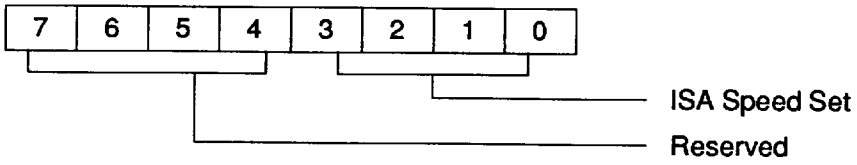
The remaining Indices are organized in the following fashion:

INDEX 00H: Chip/Revision Identifier, Read Only



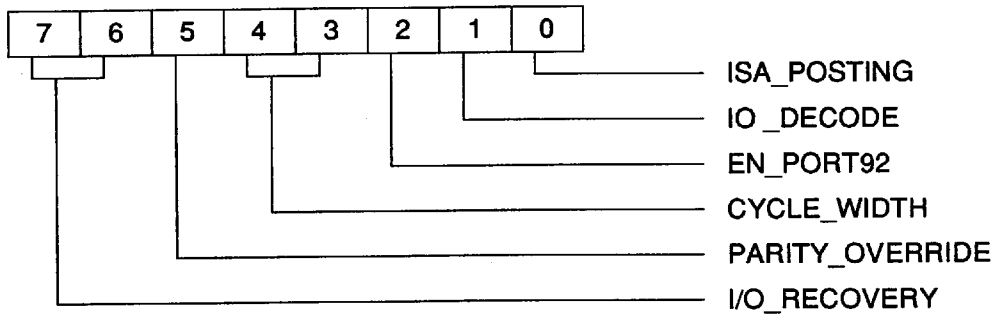
Bit(s)	Value	Meaning
3:0	0 - F	Chip Revision Indicator - (0 = Rev. A, 3= Rev. D)
7:4	0	Chip Identifier - (0 = HT321)

INDEX 01H: System Clocking (Reset State = 00H) R/W



Bit(s)	Value	Meaning
3:0	0000	
	0001	
	0010	Reserved
	0011	
	0100	
	0101	
	0110	HCLK frequency = 33MHz
	0111	HCLK frequency = 25MHz
	1000	HCLK frequency = 20MHz
	1001	HCLK frequency = 16MHz
	1010	
	1011	
	1100	Reserved. Do Not Program
	1101	
	1110	
	1111	
7:4	0	Reserved. Always program to 0

INDEX 02H: System Parameters (Reset State = 00H) **R/W**



	Bit(s)	Value	Meaning	
	0	0	POSTED Backplane MEMWN cycles disabled	
		1	POSTED Backplane MEMWN cycles enabled	
	1	0	10-Bit I/O decoding enabled	
		1	16-Bit I/O decoding enabled	
	2	0	PORT 92 Functionality disabled	
		1	PORT 92 Functionality enabled	
	4:3	0 0	Backplane Cycle Time = 6 BCLK's	
		0 1	Backplane Cycle Time = 5 BCLK's	
		1 0	Backplane Cycle Time = 4 BCLK's	
		1 1	Backplane Cycle Time = 3 BCLK's	
	5	0	Parity Error Override OFF	
		1	Parity Error Override ON	
*	7:6	00	I/O Recovery =	0 additional BCLK's
		01		1 additional BCLK's
		10		3 additional BCLK's
		11		7 additional BCLK's

* Note: Available only in Rev. D or later

Posted Backplane Memory Writes:

The HT321 is capable of posting Memory Writes to the Backplane. The Feature is enabled by a configuration bit called ISA_POSTING (active high). When Enabled, any memory write access to the backplane will be terminated using the HRDY* signal as early as possible. At this point the CPU may continue while the Backplane Memory Write Cycle is executed by the HT321. Any number of non-ISA cycles can be performed while the backplane sequencer completes the Posted Cycle.

IO_DECODE:

The HT321, by default, decodes Address [9:0] for internal I/O regions. The user has the option of enabling 16-bits of I/O decode, meaning that the HT321 will use Address [15:0] to decode internal I/O regions.

PORT_92:

PORT_92 functions of the HT321 may be enabled by setting bit 2 of this register.

CYCLE_TIME:

The AT standard time for ISA Backplane Cycles is 6 BCLK's duration. The user has the option of changing this default setting via this register. For non-standard applications, ISA Backplane Cycle Times can be reduced to a minimum of 3 BCLK's duration. For all of these settings, IOCHRDY, 0WS, MEMCS16* and IOCS16* operate normally.

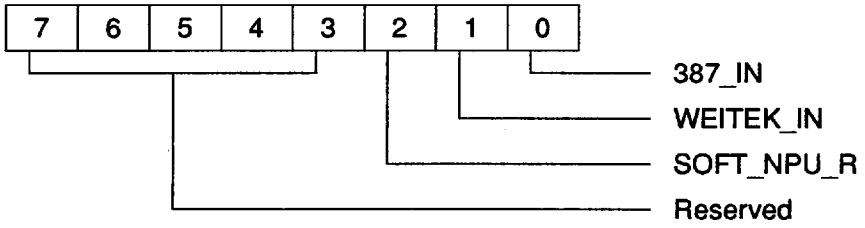
PARITY_OVERRIDE:

This bit provides a method of shutting off the Parity Detection Circuit of the HT321. With this bit set, Parity Errors flagged by the PARITY* signal asserted low are not passed to the NMI circuitry.(See I/O PORT B Function Bit 2)

I/O_RECOVERY

These bits provide a programmable I/O cycle recovery time. The "00" state provides a basic 1 1/2 BCLK minimum precharge time between back-to-back I/O cycles. The controller can be set to provide 1, 3, or 7 additional BCLK's of recovery, for a total of 2 1/2, 4 1/2, or 8 1/2 respectively. This option is available only in Rev. D or later.

INDEX 04H: Co-Processor (Reset State - 00H) **R/W*****



Bit(s)	Value	Meaning
0	0	80387 Co-Processor not installed
	1	80387 Co-Processor installed
1	0	Weitek Co-Processor not installed
	1	Weitek Co-Processor installed
2	0	Software Co-Processor RESET not blocked (1)
	1	Software Co-Processor RESET blocked (1)
7:3	0	Reserved. Always program to 0

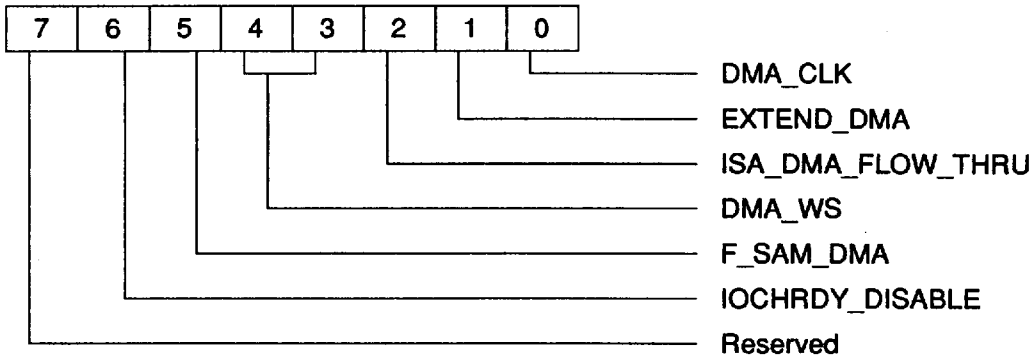
(1) Software Co-Processor RESET is defined as:

IOW* Command to I/O location 0F1H, DATA = xx(No Valid Data)

- if blocked, this Command will not result in a RESET387 from the HT321
- if not blocked, this Command will produce a pulse of the RESET387(P51).

***NOTE: This INDEX is made available for 386 implementations and does not require programming for 486 systems.

INDEX 06H: DMA (Reset State = 00H) **R/W**



	Bit(s)	Value	Meaning
	0	0	DMA Clock = BCLK divided by 2
		1	DMA Clock = BCLK inverted
	1	0	Extended DMA Page Registers Disabled
		1	Extended DMA Page Registers Enabled
	2	0	DMA FLOW_THRU Mode Disabled
		1	DMA FLOW_THRU Mode Enabled ****
	4:3	0 0	DMA Wait states = 3
		0 1	DMA Wait states = 2
		1 0	DMA Wait states = 1
		1 1	DMA Wait states = 0
	5	0	Fast Sample DMA Disable
		1	Fast Sample DMA Enable
*	6	0	IOCHRDY enabled during Master Cycles
		1	IOCHRDY disabled during Master Cycles
*	7	0	Reserved. Always program to 0

* Note: Available only in Rev. C or later

**** Note: Program the HT342 INDEX 2BH for this Option before use.

DMA_CLK:

This bit selects the clock frequency presented to the internal 8237 equivalents. The selection is either BCLK inverted or BCLK divided by two.

EXTEND_DMA:

For systems requiring use of the extended DMA page registers (I/O 480 - 48FH), this bit is used to enable use of these registers.

ISA_DMA_FLOW_THRU:

This feature should be enabled for systems that have a "WRITE BUFFER" as part of their memory controller circuitry. The HT342 is one such device. With this bit enabled, a hand-shake mechanism is used to determine when the WRITE BUFFER is empty and DMA cycles can proceed. Once HLDA is issued by the CPU, the HT321 will hold off issuing HLDA to its internal circuits until HRDY* is sampled true. This HRDY* is a signal from the Shasta Local Bus (HT342) that indicates the WRITE BUFFER is empty and its presence in the system pipeline has been by-passed.

DMA_WS:

This bit controls the number of DMA_CLK's inserted into the standard DMA cycle controlled by the integral DMA Controller of the HT321.

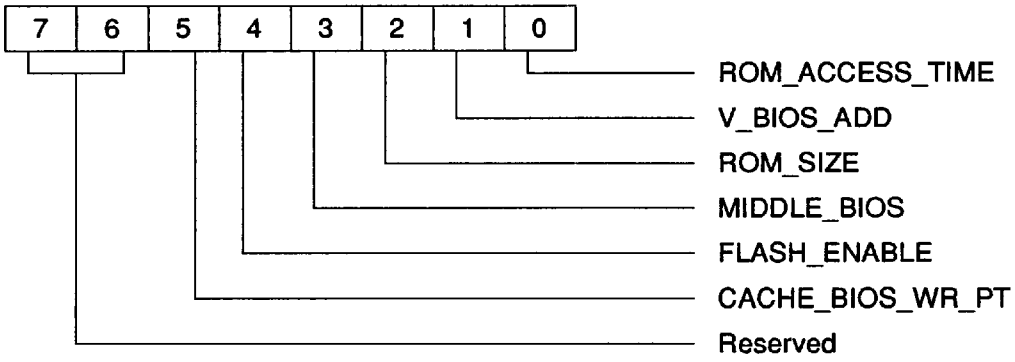
FAST_SAMPLE_DMA:

For slower (20 & 16MHz) 486 systems, this bit should be enabled in order to reduce latency for backplane derived memory read cycles on the HTK340 local bus.

IOCHRDY_ENABLE

This bit is used to enable/disable IOCHRDY generation from the HT321 during backplane MASTER mode DMA cycles. IOCHRDY can be used, if desired, to extend the command in MASTER mode by programming this bit to "0". This option is only available in Rev. C or later.

INDEX 07H: EPROM (Reset State = 00H) R/W***



	Bit(s)	Value	Meaning
	0	0	250nsec ROM Output Enable pulse duration
		1	125nsec ROM Output Enable pulse duration
	1	0	Video BIOS separate from System BIOS
		1	Video BIOS with System BIOS in same physical device
	2	0	ROM size = 64K
		1	ROM size = 128K
	3	0	Middle BIOS region of 64K space (below 16 Mb) Disabled
		1	Middle BIOS region of 64K space (below 16 Mb) Enabled
*	4	0	ROMEN disabled for EPROM writes
		1	ROMEN enabled for EPROM writes
**	5	0	EADS CACHE Invalidation disabled for EPROM writes
		1	EADS CACHE Invalidation enabled for EPROM writes
	7:6	0	Reserved. Always program to 0

* Note: Available only in Rev. C or later.

** Note Available only in Rev. D or later.

*** Note: The data width of the ROM is selected externally via the CLAMPA20* pin. During POR, this pin is read by the HT321. To configure the system for an 8-bit wide BIOS ROM, this pin should be pulled high via an external resistor. To configure the system for a 16-bit wide BIOS ROM, the CLAMPA20* pin should be pulled low via an external resistor.

FLASH_ENABLE:

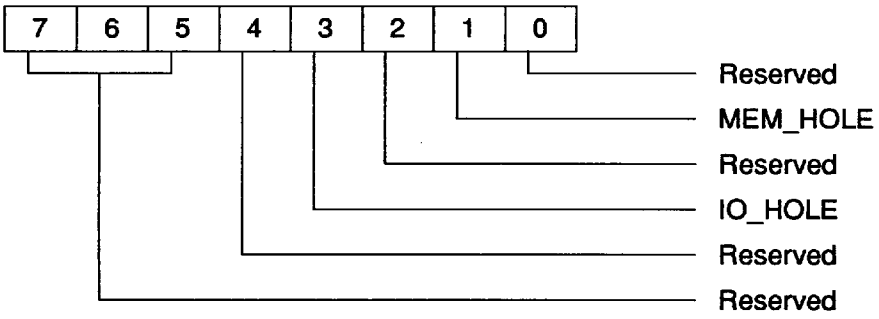
This bit selects the timing of the ROMEN pin on the HT321 device. With this bit programmed to "0", the ROMEN signal is qualified internally with the MEMR* command before being presented by the HT321. In this mode it can be used as an Output Enable for the BIOS ROM. With this bit set to "1", ROMEN is a straight address decode of the selected ROM space. In this mode, ROMEN can be used as the Chip Select to the EPROM and the MEMR* can be used as the Output Enable for the device. MEMW* can now be used; as the Write Enable to a FLASH EPROM device, if desired. This option is available in Rev. C or later.

CACHE_BIOS_WRITE_PROTECT

This bit enables/disables the Cached BIOS Space Write Protect feature. If a write cycle to BIOS space is detected when this bit is set, and EADS* pulse is produced 2 HCLKs after HADS* to cause this cache line to be invalidated. This feature allows the BIOS space to be set cacheable for a performance gain. This feature is only available in Rev. D or later.

Note: This bit cannot be set while Posted Backplane Memory writes (Index 02H, bit 0) is enabled. Write protect EADS* cycle timing is not compatible with posted ISA memory write cycles.

INDEX 08h: I/O and MEMORY MAP HOLES (Reset State = 00H) R/W



Bit(s)	Value	Meaning
0	0	Reserved. Always program to 0
1	0	Memory Map Hole Disabled
	1	Memory Map Hole Enabled
2	0	Reserved. Always program to 0
3	0	I/O Map Hole Disabled
	1	I/O Map Hole Enabled
4:7	0	Reserved. Always program to 0

"HOLES" in HT321 Map

In the HTK340 architecture, the HT321 is usually the default device. There may be some local devices, however, that do not conform to the HLOCAL* type of handshaking mechanism but still can operate on the Shasta bus. For these devices, the HT321 must not start or terminate a cycle or else contention is sure to occur. For these devices, the HT321 has pre-programmed I/O and MEMORY "regions" for which the HT321 will not respond to the cycle. One I/O and one MEMORY region are available.

The I/O region is a minimum of 16 bytes in size and must be multiples of 16 bytes. To program the I/O "holes", first set the range of addresses to be exempted via the "I/O HOLE LOW ADDRESS" and "I/O HOLE HIGH ADDRESS" registers. The "LOW ADDRESS" will contain the starting address of the I/O hole, whereas the "HIGH ADDRESS" should be programmed to the top of hole desired +1. For example, to set an I/O hole between location 320h- 32Fh, program the "LOW ADDRESS" register with "32h" and the "HIGH ADDRESS" register with "33h". To enable this newly programmed hole, set the corresponding bit in INDEX 08 of the HT321 configuration register.

The memory hole regions are multiples of 16K chunks with 16K being the smallest chunk available. MEM_HOLE has no size restriction and is programmed similar to the I/O hole programming described earlier. Again, the "END ADDRESS" should be the top of the desired hole range +1.

INDEX 10H: I/O HOLE LOW ADDRESS (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Start Address of I/O HOLE (Address 11 DOWN to 4)

INDEX 11H: I/O HOLE HIGH ADDRESS (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	End Address of I/O HOLE (Address 11 DOWN to 4)

INDEX 19H: MEM HOLE START ADDRESS, LOWER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Address of MEM HOLE Start (Address 21 DOWN to 14)

INDEX 1AH: MEM HOLE START ADDRESS, UPPER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
5:0	00-3F	Address of MEM HOLE Start (Address 27 DOWN to 22)
7:6	0	Reserved. Always program to 0

INDEX 1CH: MEM HOLE END ADDRESS, LOWER (Reset State = 00h), R/W

Bit(s)	Value	Meaning
7:0	00-FF	Address of MEM HOLE End (Address 21 DOWN to 14)

INDEX 1DH: MEM HOLE END ADDRESS, UPPER (Reset State = 00H), R/W

Bit(s)	Value	Meaning
5:0	00-3F	Address of MEM HOLE End (Address 27 DOWN to 22)
7:6	0	Reserved. Always program to 0

PC AT-Compatible Registers

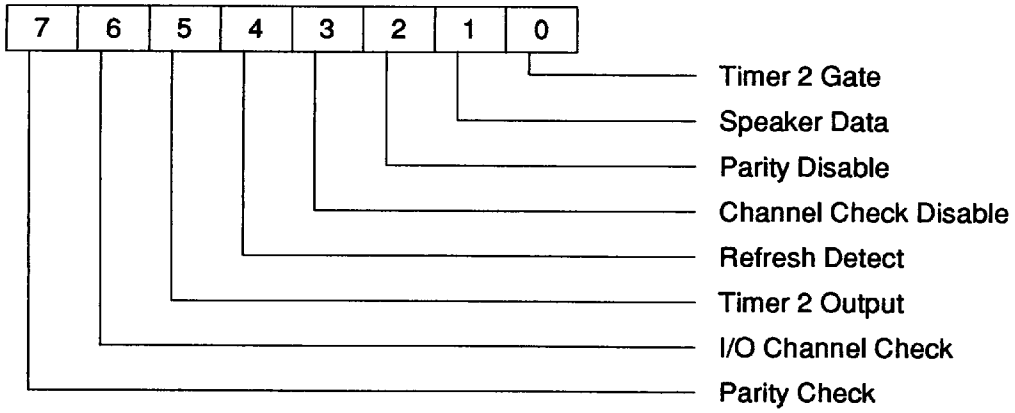
The HT321 has a number of AT-compatible internal registers in order to minimize external circuitry. These include PORT_B, NMI Mask Register, PORT_92 and all the internal Megafunction registers within the 8237, 8259 and 8254 functions. These registers and their bit definitions are shown below.

Keyboard Controller Interface 0060H, 0062H, 0064H R/W

The HT321 requires an external 8042 equivalent to process keyboard operations. The clock for the 8042 may be derived from BCLK or separate OSC circuit and should have a frequency that is between 6 MHz and 10 MHz when used with standard keyboard controllers.

The 8042 interfaces with the HT321 through OPTBUFUL (IRQ1) and a chip select line KBCS*. The 8042 also provides two output signals: KB_CLAMPA20*(P166) and RC(P77 Reset CPU). These signals are brought into the HT321 and combined internally with Alternate Port 92 FAST GATEA20 and FAST CPU RESET (FAST_RC) functions respectively.

I/0 Port 61H Port B 0061H R/W



This port controls several system level functions.

Bit(s)	Meaning
0	Timer 2 Gate (read/write). This bit controls operation of timer channel 2. 0 = channel 2 timer operation is disabled (default). 1 = channel 2 timer operation is enabled.

1 Speaker Data (read/write). This bit gates the output of channel 2 of the timer/counter.

0 = output is disabled (default).
1 = output is enabled.

2 Parity Disable (read/write). This bit is used to disable parity error initiation of NMI. This bit is logically ORed with Parity OVERRIDE Option Bit 5 of INDEX 02. By this method, System Parity Detect is disabled if Bit 5 (PARITY OVERRIDE) of INDEX 02 is set to a logical 1.

0 = PARITY* sampling is enabled (default).
1 = PARITY* sampling is disabled.

3 Channel Check Disable (read/write). This bit disables NMI generation for Channel Check Errors.

0 = enables IOCHK* sampling (default).
1 = disables IOCHK* sampling.

4 Refresh Detect (read only). This bit toggles for each refresh cycle.

5 Timer 2 Out (read only). This bit returns the state of the Timer 2 output.

6 IOPCHK I/O Channel Check (read only). This bit indicates an I/O Channel Check has occurred (usually a parity error) on the System I/O Channel.

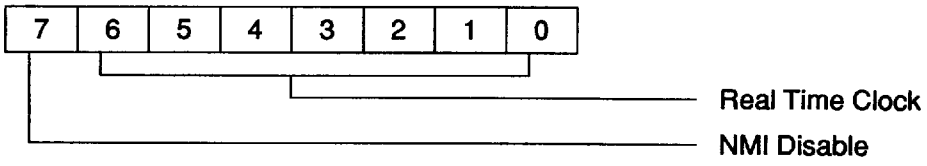
0 = no error occurred.
1 = an error occurred.

7 PCHK Parity Check (read only). This bit indicates a Parity Error has occurred on the local memory.

0 = no error occurred.
1 = an error occurred.

IOPCHK and PCHK are derived in the following manner. If IOCHK* is active (low) and IOCHK* sampling is enabled (PORT_B, bit 3 = 0), then IOPCHK is driven high and remains there until IOCHK* sampling is disabled (PORT_B, bit 3 =1) or RESET occurs. The PCHK signal (active high) is used to indicate that a DRAM parity error has occurred on the motherboard. The PARITY* signal, from another device (normally HT342) on the local bus, is sampled on every clock edge. If detected low on a rising HCLK2 edge and if RAM parity checking is enabled (PORT_B, bit 2 = 0), then PCHK is driven high. PCHK remains high until the RAM parity checking bit is disabled (PORT_B, bit 2 = 1) or RESET occurs.

I/O Port 70H RTC Index and NMI Mask 0070H W



This register is used to access the RTC and its CMOS RAM.

Bit 7 is an NMI Mask bit used to mask NMIs from accessing the CPU. Bits[6:0] would be used by an external RTC chip. The NMI output is active high and must be enabled before it can become active. NMI defaults on power-up to disabled. Once enabled, NMI equals the OR of the PCHK and IOPCHK signals.

Bit(s)	Meaning
6:0	RTC Index[6:0]. These bits are used as index pointers for an external real-time clock.
7	NMI Disable (write only). This bit controls the generation of NMIs. 0 = enables generation of NMIs (default). 1 = disables the generation of NMIs.

PORT_92:

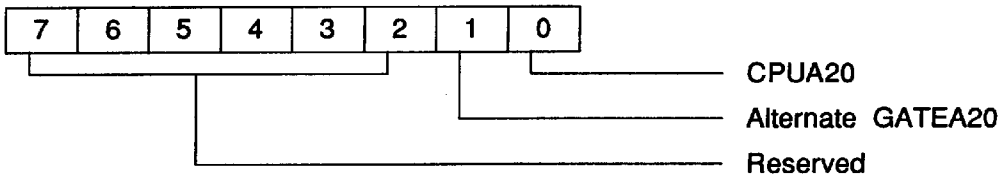
Access to PORT_92 is only enabled when the EN_P92 bit (INDEX 02H, bit 2) is set.

This PORT is located at I/O location 92H in the system address map and defaults on power-up to 00h. Two features of the PORT_92 functionality are implemented in the HT321. These are FAST_RC and Alternate GATEA20*. Bit 0 of this register enables the FAST_RC circuitry, whereas Bit 1 of this register holds the value of Alternate GATEA20*.

The Alternate GATEA20* output is directly connected to Bit 1 of the PORT_92 register. If a "1" is written to Bit 1 of PORT_92, then the CLAMPA20* output will go high. It will remain high until Bit 1 is changed by an IOW* to PORT_92 again.

FAST_RC provides a faster RESET of the CPU compared to the RC signal from the Keyboard Controller. To activate this Reset pulse, a "1" should be written into Bit 0 of PORT_92. When this is done, a pulse of 125 - 150 nS duration will be generated 6.72 uS after the trailing edge of the IOW* Command that programmed Bit 0 of this port. Only one pulse will be generated. To generate another FAST_RC pulse, Bit 0 of PORT_92 must first be reset to 0, then reprogrammed to 1.

I/O Port 92H System Control Port 0092H R/W Reset State = 00H



This register is used as a faster alternate to Gating A20 and/or Resetting the CPU rather than using the 8042 Keyboard Controller. This register is compatible with IBM PS/2 architecture.

Bit(s)	Meaning
0	Alternate CPU RESET (FAST_RC). 0 to 1 transition = a reset pulse is provided on the RESETCPU pin to reset the CPU 6.72usec later. After activation of a CPU reset, the status is maintained so the BIOS may determine that the reset was caused by a programmed CPU RESET condition.
1	Alternate GATEA20. 0 = CLAMPA20* is forced low (real mode). 1 = Address bit HA20 (on the Shasta local bus) should be treated as normal.
7:2	Reserved.

Internal DMA Controller Registers

This section describes the registers used during DMA functions.

Current Address Register **0000, 02, 04, 06 00C0, C6, CA, 00CEH** **R/W**

Each DMA channel has a 16-bit current address register that holds the address used during transfers. Each channel can be programmed to increment or decrement this register for each transfer completed. This register can be read or written by the CPU as consecutive 8-bit bytes. If Auto-Initialization is selected, this register is reloaded from the Base Address Register upon reaching Terminal Count in the Current Word Count Register. Channel 0 increment or decrement may be disabled by setting the Address Hold Bit in the Command Register.

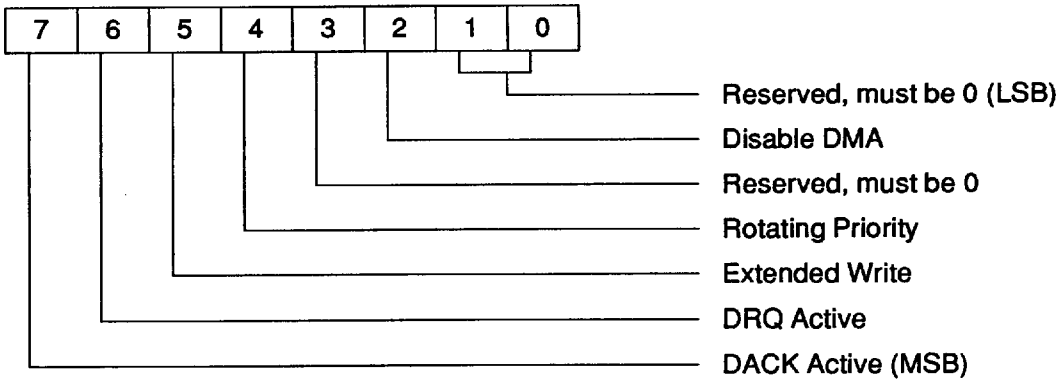
Current Word Count Register **0001,03,05,07,00C4,C8,CC,CE,00CFH** **R/W**

Each channel has a Current Word Count Register the value of which determines the number of transfers to execute. The actual number of transfers performed is one greater than the value programmed into the register. A register is decremented after each transfer until it transitions from 0000H to FFFFh. When this roll-over occurs, the HT321 generates T/C(P85), suspends operation for that Channel, sets the appropriate Request Mask Bit or re-loads during Auto-Initialize and continues.

Base Word Count Register

This register preserves the initial value of the Current Word Count Register. It is also a write-only register that is loaded by writing to the Current Word Count Register. This register's value is loaded into the Current Word Count Register during Auto-Initialization.

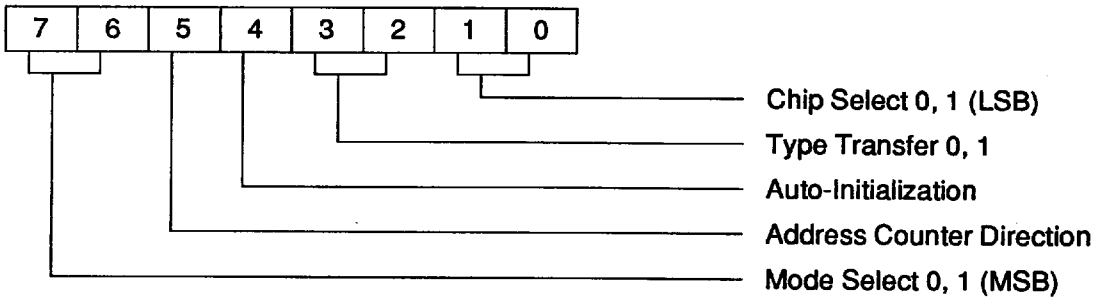
Command Status Register 0008, 00D0H R/W



This register controls the overall operation of a DMA subsystem. The register can be Read or Written by the CPU and is cleared by either a POR or a Master Clear command.

Bit(s)	Meaning
1:0	Reserved, must be 0.
2	Disable DMA: Bit 2 is the master disable of the DMA controller. Writing a "1" to this location disables the DMA subsystem (DMA1 or DMA2). This is used to prevent DMA cycles from occurring when the CPU needs to reprogram one of the Channels.
3	Reserved, must be 0.
4	Rotating Priority: Writing a "1" to bit 4 causes the HT321 to utilize a Rotating Priority scheme for honoring DMA requests. The default mode is Fixed Priority.
5	Extended Write is enabled by writing a "1" to bit 5, causing the write commands to be asserted one DMA Clock early during a transfer. The Read and Write commands both begin in state S2 when enabled.
6	DRQ active level is determined by bit 6. Writing a "1" in this bit position causes DRQ to become active low. Default is active high.
7	DACK active level is determined by bit 7. Programming a "1" in this bit position makes DACK an active high signal. Default is active low.

Mode Register **000BH, 00D6H** **R/W**



Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits 0 and 1 of a Write Command to the Mode Register determine which Channel's Mode Register is accessed. The remaining six bits control the Mode of the Selected Channel. Each Channel Mode Register may be read by sequential Reads to the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point.

During mode read operation, bits 0 and 1 are "1".

Bit(s)	Meaning
1:0	Channel Select 1, 0: Bits 1 and 0 determine which channel's Mode Register is written to. Read back of a mode register results in bits 1 and 0 both being "1"s.

CS1	CS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

Bit(s)	Meaning
3:2	Transfer Type 1, 0: Bits 3 and 2 control the type of transfer that is to be performed.

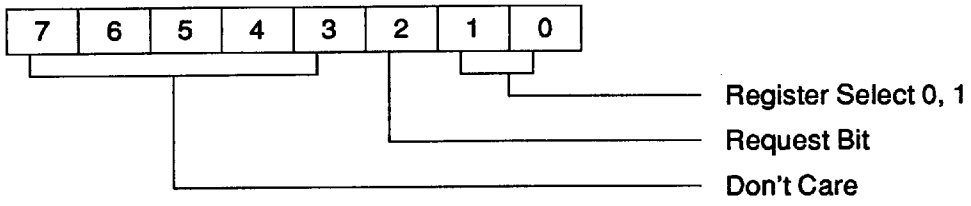
T1	T0	
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Don't use

Bit(s)	Meaning
4	Auto-Initialization function is enabled by writing a "1" in bit 4 of the Mode Register.
5	Address Counter Direction: Determines progression of Address count. A "1" in bit 5 decrements the address after each transfer.

7:6 Mode Select 1, 0 for each channel is accomplished by bits 7 and 6.

M1	M0	
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

Request Register **0009H, 00D2H** **W**



This is a 4-bit Read,3-bit Write Register used to initiate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or reset independently by the CPU. The Request Mask has no effect on software generated requests. All request bits are cleared to "0" by a RESET.

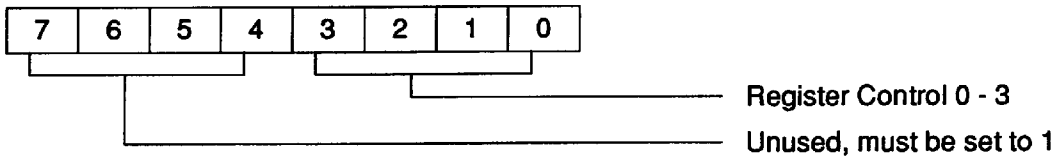
Bit(s) Meaning

1:0 Register Select 0, 1: Bits 1 and 0 determine which channel's Request Register is written to.

RS1	RS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

2 A Channel's Request Bit is set by writing a "1" to bit 2.

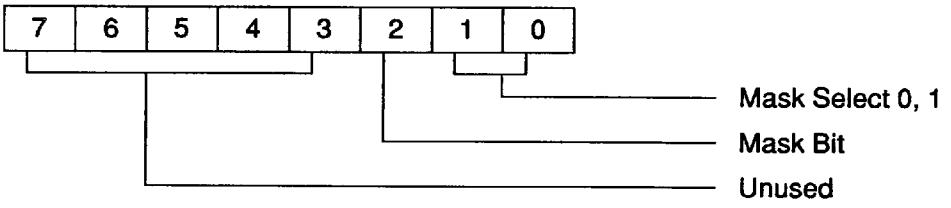
Request Register **0009H, 00D2H** **R**



Bit(s) Meaning

3:0 During a Request Register Read, the state of the request bit associated with each Channel is returned in bits 3 through 0 of the byte. The bit position corresponds to the Channel Number.

Single Bit Mask Register **000AH, 00D4H**



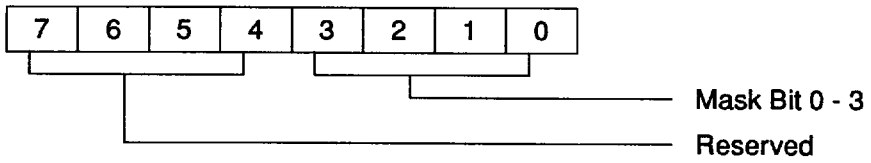
Each channel may be independently masked by Writing to the Single Mask Bit location. The operation of this register is explained below.

Bit(s)	Meaning
1:0	Mask Select 1, 0 - These two bits select the specific Channel Mask Bit to be set or reset.

MS1	MS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

2	Mask Bit sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a "1" to this bit position sets the mask, inhibiting external requests.

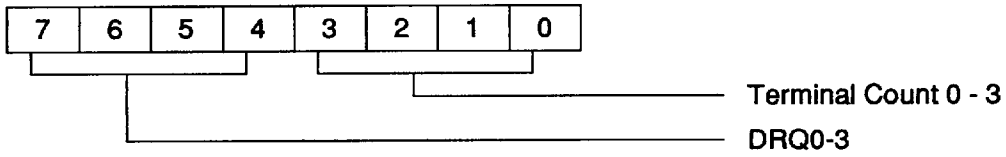
Write All Mask Register Bit **000FH, 00DEH** **R/W**



The Write All Mask Register has four active bits that are used to inhibit transfer cycles occuring from external DMA requests. All four mask bits may be programmed in one operation by Writing to the Write All Mask Bit I/O Address. The data format for this function is shown below.

Mask Bits 3 - 0: Each bit position in the field represents the mask bit of the Corresponding Channel. All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits are set , if Auto-Initialize is disabled, when Terminal Count is reached. The entire register can be cleared, enabling all four channels, by executing a Clear Mask Register Operation.

Status Register **0008H, 00D0H** **R**



The status of all four channels can be determined by Reading the Status Register. Information available indicates if a Channel has reached Terminal Count and whether an external service request is pending(DRQx). Bits 3 - 0 of this Register are cleared by a POR Reset, a Master Clear, or each time a Status Read takes place. Bits 7 - 4 are cleared by a POR Reset, a Master Clear, or the removal of the request pending. Bits 7 - 4 are not affected by the state of the Mask Register Bits. The Channel Number correlates to the bit position (Bit7:4=C3:C0 and Bit3:0=C3:C0).

Special Commands

Five Special Commands are provided to make programming the device easier. These commands are activated by access to a Specific I/O Address by assertion of either an IOR* or IOW*. Information on the data lines is ignored by the HT321 whenever an IOW* activated Special Command is issued. Data returned by IOR* activated Special Command is invalid. Descriptions of the five Special Commands follow:

Clear Byte Pointer Flip-Flop - This Command is normally executed prior to reading or writing of the Address or Word Count Register. It initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.

Set Byte Pointer Flip-Flop - Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an Address or Word Count Register.

Master Clear - This Command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter and Byte Pointer Flip-Flops are cleared and the Request Mask Register is Set. Immediately following Master Clear or RESET, the DMA Controller is in the Idle Mode.

Clear Request Mask Register - This command enables all four DMA Channels to accept Requests(DRQx's) by clearing the Mask bits in the Register.

Clear Mode Register Counter - In order to allow access to four Mode Registers using one I/O Address, an additional counter is used. After clearing the counter, all four Mode Registers may be read (Channel 0 first and Channel 3 last) by executing successive Reads at the Read Mode Register Address.

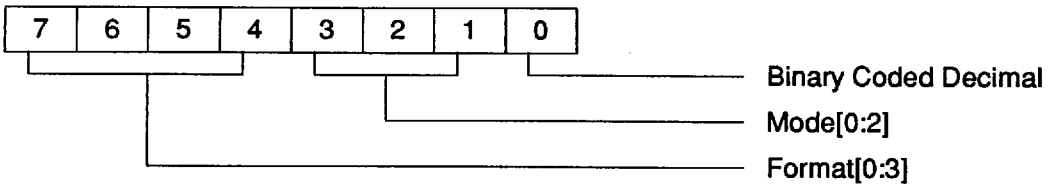
Programmable Interval Timer Registers

After power-up, the condition of PIT Control Registers, counter registers, CE and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word and then an initial count. The Control Register of a counter is written to by writing to the Control Word address (see the following table). The Control Word is a write-only location.

I/O ADDR	Function
040h	Counter 0 (Read/Write)
041h	Counter 1 (Read/Write)
042h	Counter 2 (Read/Write)
043h	Counter Control (Write)

Counter Control Register **(043H Write Only)**



Format[3:0] Bits[7:4] determine the command to be performed as shown in the PIT Command Table.

Mode[2:0] Bits[3:1] determine the counter's mode during Read/Write Counter Commands (see Read/Write Counter Command Table) or select the counter during a Read-Back Command (see ReadBack Command). Bits[3:1] become "don't care" during Latch Counter Commands.

Binary Coded Decimal - Bit 0 selects Count Format during Read/Write Counter Commands. Where bit 0 is set to "0", the count is binary, when bit 0 is set to "1", the count is Binary Coded Decimal.

Note that during Read-Back Command this bit must be "0".

Read/Write Counter Command

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (Counter Latch Command)
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (Counter Latch Command)
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (Counter Latch Command)
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSG
1	1	x	x	Read-Back Command (Counter RB Command)

When writing to a counter, two conventions must be observed:

Each counter's Control Word must be written before the initial count is written.

Writing the initial count must follow the format specified in the Control Word (Least Significant Byte only Most Significant Byte only, or Least Significant Byte, then Most Significant Byte).

MSB = Most Significant Byte
LSB = Least Significant Byte

A new initial count can be Written to a Counter any time after programming without rewriting the Control Word, as long as the Programmed Format is observed.

During Read/Write Counter Commands M[2:0] are defined as follows:

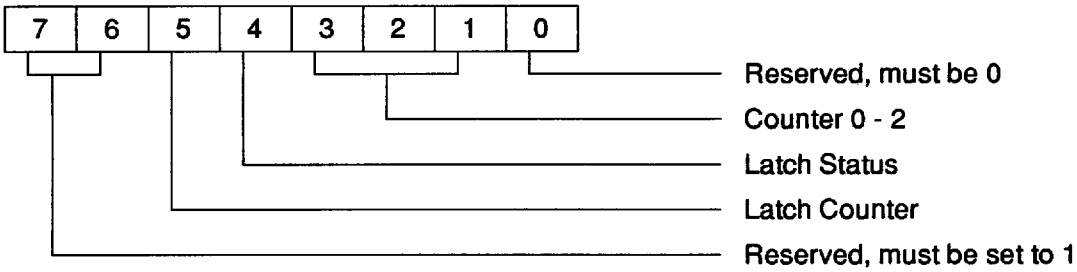
M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
x	1	0	Select Mode 2
x	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Latch Counter Command

When a Latch Counter Command is issued, the counter's output latches (COL and COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition, the latches are enabled and the contents of the CE may be read directly.

Latch Counter Commands may be issued to more than one counter before reading the first Counter to which the Command was issued. Also, multiple Latch Counter Commands issued to the same counter are ignored. The Count Read will be the Count at the time the first Latch Counter Command was issued.

Read-Back Command



The Read-Back Command allows the user to check the Count Value, Mode and State of the OUT signal and Null Count Flag of the selected counter(s).

The format of the Read-Back Command is:

Latch Counter[LC] - Writing a "0" in bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

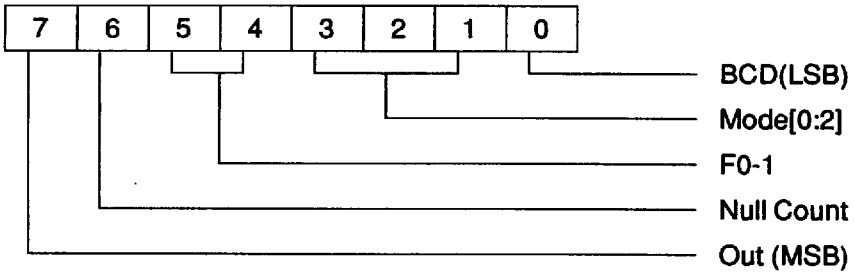
Latch Status[LS] - Writing a "0" in bit 4 causes the selected counter(s) to latch the current condition of its Control Register, Null Count and Output into the Status Register. The next read of the Counter results in the contents of the Status Register being read (see Status Byte read).

Counter[2:0] - Writing a "1" in bit 3 causes Counter 2 to latch one or both of the registers specified by Latch Counter and Latch Status. The same is true for bits 2 and 1, except that they latch Counters 1 and 0 respectively.

Each counter's latches remain latched until either the latch is Read or the Counter is reprogrammed.

If LS = LC = 0, Status is returned on the next Read from the Counter. The next one or two Reads (depending on whether the Counter is programmed to transfer one or two bytes) from the Counter result in the Count being returned.

Status Byte



OUT - Bit 7 contains the State of the OUT signal of the Counter.

Null Count - Bit 6 contains the Null Count Flag. This Flag is used to indicate that the contents of the CE are valid. Null Count is set to a "1" during a Write to the Control Register or the Counter. It is cleared to a "0" whenever the Counter is loaded from the counter input registers.

F[1:0] Bits[5:4] contain the F1 and F0 Command bits, which were written to the Command Register of the counter during initialization. This information is useful when determining whether the high byte, the low byte, or both must be transferred during counter read/write operations.

Mode[2:0] - These bits reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

BCD - Bit 0=1 Indicates the CE is operating in BCD format.

Interrupt Controller Registers

Initialization Command Words

The initialization process consists of writing a sequence of four bytes to each Interrupt Controller(PIC1, PIC2). The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H/0A0H with a "1" in bit 4 of the Data Byte. The Interrupt Controller interprets this as the start of the initialization sequence and does the following:

1. The Initialization Command Word Counter is reset to "0".
2. ICW1 is latched into the device.
3. Fixed Priority Mode is selected.
4. IR7 is assigned the highest priority.
5. The Interrupt Mask Register is cleared.
6. The Slave Mode Address is set to seven.
7. Special Mask Mode is disabled.
8. The IRR is selected for Status Read operations.

The next three I/O Writes to address 021H/0A1H will load ICW2-ICW4. See below for a flow chart of the initialization sequence. The initialization sequence can be terminated at

any point (all four bytes must be written for the controller to be properly initialized) by writing to address 020h/0A0h with a "0" in data bit 4. Note, this causes OCW2 or OCW3 to be written dependant upon how many Writes have occurred.

Initialization Sequence

START

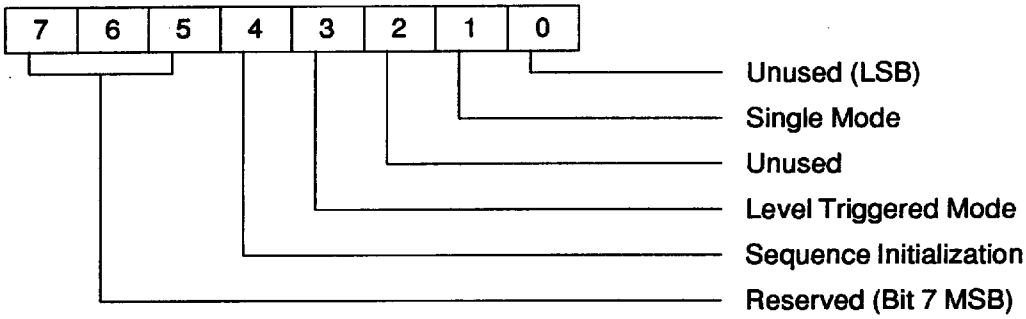
Write ICW1 A0 = 0 D4 = 1
Write ICW2 A0 = 1

Check CASCADE Mode?

YES - Write ICW3 A0 = 1
NO - Optionally Write ICW4

END OF INITIALIZATION Controller Ready

ICW1 (Address 020h / 0A0h) Write Only

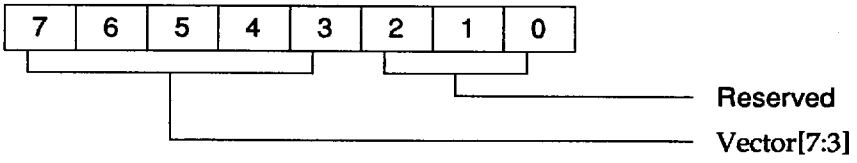


Sequence Initialization - Bit 4 indicates to the Interrupt Controller that an Initialization Sequence is starting and must be a "1" to Write ICW1.

Level Triggered Mode[LTM] - Bit 3 selects level or edge triggered inputs to the IRR. If a "1" is Written to LTM, a high level on the IRR input generates an interrupt request. The IRQ must be active until the first INTA cycle is started to generate the proper interrupt vector (an IR7 vector is generated if the IRR input is de-asserted too early), and the IRQ must be removed prior to EOI to prevent a second interrupt from occurring.

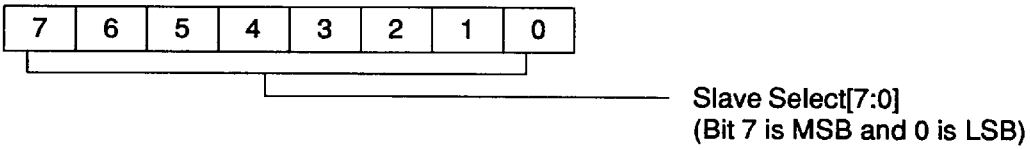
Single Mode - Bit 1 - 0 = 1 8259 and 1 = Cascaded 8259 (for AT Spec = 2x8259's)

ICW2 **(Address 021H / 0A1H Write Only)**



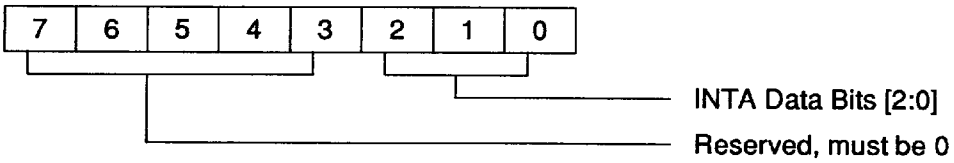
Vector[7:3]: These bits are the upper five bits of the Interrupt Vector and are programmable by the CPU. The lower three bits of the Vector are generated by the Priority Resolver during INTA. PIC1 and PIC2 need not be programmed with the same value of ICW2.

ICW3 Format for PIC1 **(Address 021H Write Only)**



Slave Select[7:0]: Select which IR inputs have Slave Mode controllers connected. ICW3 in PIC1 must be written with 04H for PIC2 to function.

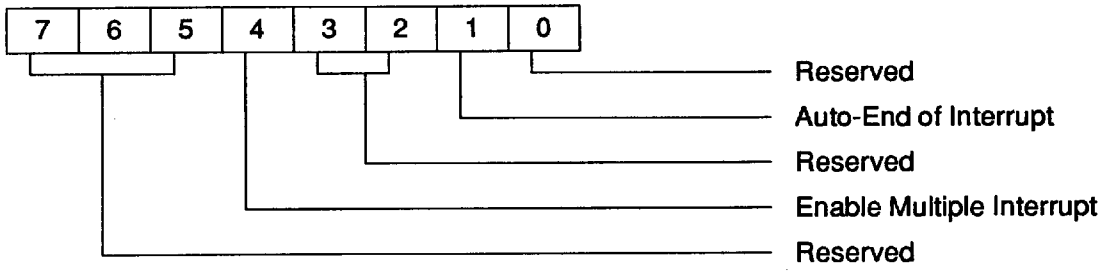
ICW3 Format for PIC2 **(Address 0A1H Write Only)**



INTA Data[2:0]: Determine the Slave Mode address the controllers will respond to during the cascaded INTA sequence. ICW3 in PIC2 should be written with 02H for Cascade Mode operation.

Note that bit [7:3] must be "0".

ICW4 (Address 021H / 0A1H Write Only)



Enable Multiple Interrupts - Bit 4 enables Multiple Interrupts from the same channel in Fixed Priority Mode. This allows PIC2 to fully nest interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by PIC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to PIC2 and to check its In Service Register for "0" when exiting an interrupt service routine. If "0", a non-specific EOI command should be sent to PIC1. If non-zero, no command is issued.

AEOI - Auto End-of-Interrupt - Bit 1 is enabled when ICW4[4:1] is written with a "0" in both. The interrupt controller performs a non-specific EOI on the trailing edge of the second INTA cycle. Note that this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.

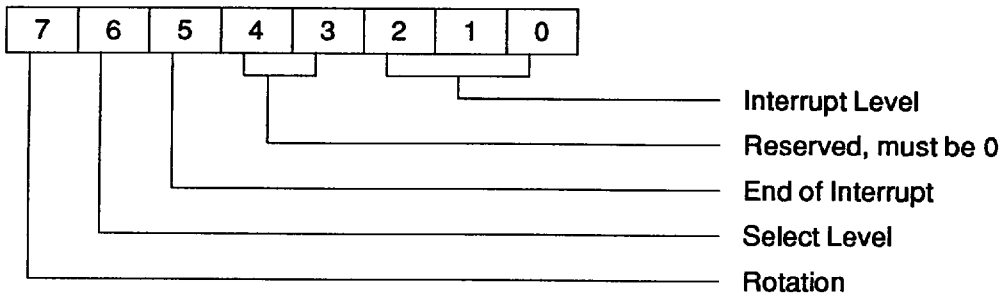
Operational Command Words

Operational Command Word One (OCW1) is located at address 021h/0A1h and may be Written any time the Controller is in Initialization Mode. Operational Command Words Two and Three (OCW2 and OCW3) are located at address 020h/0A0h. Writing to address 020h/0A0h with a "0" in bit 4 places the Controller in Operational Mode and loads OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1 **(Address 021H / 0A1H Read/Write Register)**

Mask Bits[7:0]: These bits control the state of the interrupt Mask Register. Each interrupt request can be masked by writing a "

1" in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no effect on lower priority requests. All IMR bits are cleared by writing ICW1.



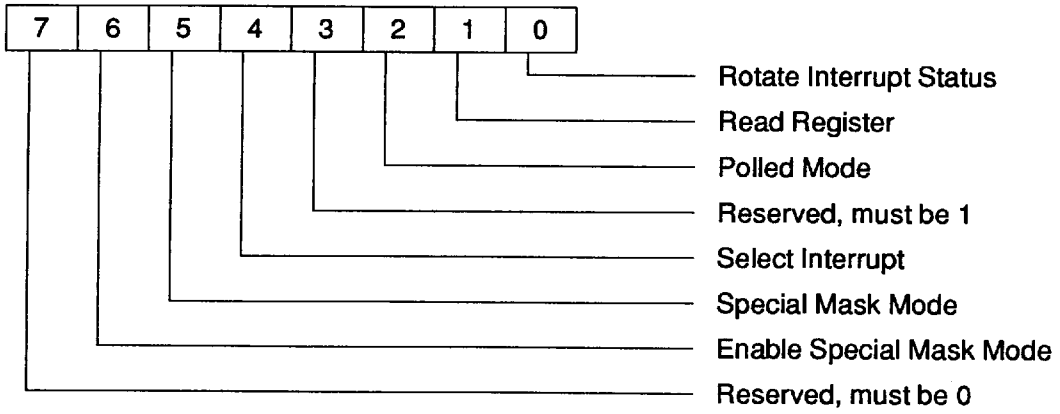
OCW2 **(Address 020H / 0A0H Write Only)**

Bit(s)	Value	Meaning
2:0		L2, L1, L0 - These bits determine the interrupt level acted upon when the SL bit is active.
4:3	0 0	Reserved, must be 0.
7:5		EOI, SL, R - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is shown below.

	IR Level to be acted upon							
	0	1	2	3	4	5	6	7
L	0	1	0	1	0	1	0	1
L	0	0	1	1	0	0	1	1
L	0	0	0	0	1	1	1	1

R	S	E		
0	0	1	Non-specific EOI Command	End of Interrupt
0	1	1	Specific EOI Command	
1	0	1	Rotate on Non-specific EOI Command	Automatic Rotation
1	0	0	Rotate in Automatic EOI Mode (Set)	
0	0	0	Rotate in Automatic EOI Mode (Clear)	
1	1	1	*Rotate on Specific EOI Command	Specific Rotation
1	1	0	*Set Priority Command	
0	1	0	No Operation	
			*L0-L2 are used	

OCW3 (Address 020H / 0A0H Write Only)



Bit	Meaning
0	Rotate Interrupt Status - This bit selects between the IRR and the ISR during Status Read operations if Read Register = 1 is selected. ISR is selected if this bit is set to "0".
1	Read Register - When the bit is a "1", reading the Status Port at address 020H/0A0H causes the contents of IRR or ISR (determined by Rotate Interrupt Status Bit) to be placed on D[7:0]. Asserting Polled Mode forces Read Register reset.
2	Polled Mode is enabled by writing a "1" to bit 2 of OCW3, causing the HT321 to perform the equivalent of an INTA cycle during the next I/O Read Operation to the Controller. The byte read during this cycle sets bit 7 if an Interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request is encoded in bits[2:0]. The IRR remains frozen until the read cycle is completed, at which time the Polled Mode bit is reset.
4	Select Interrupt - Writing a "0" in this bit position takes the Interrupt Controller out of initialize mode and writes OCW2 or OCW3.
5	Special Mask Mode - If Enable Special Mask Mode and Special Mask Mode are written with a "1", the Special Mask Mode is enabled. Writing a "1" to Enable Special Mask Mode and a "0" to Special Mask Mode disables Special Mask Mode. During Special Mask Mode, Writing a "1" to a Bit position inhibits interrupts and Writing a "0" enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition for the ISR.
6	Enable Special Mask Mode - Writing a "1" in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5. Enable Special Mask Mode allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

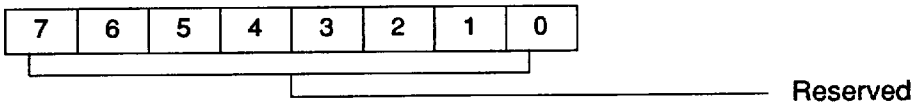
Identifier Port

INDEX 0020H **Read Only** **Write Ignored**

Bit(s)	Value	Meaning
3:0	0000	Revision number (0 = Rev. A)
7:4	0010	DRAM controller identifier

Feature Port

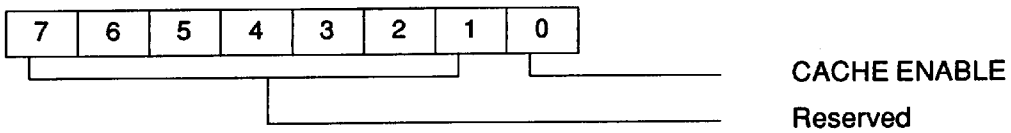
INDEX 0021H : (Reset State = 00H) Read Only Write Ignored



Bit(s)	Value	Meaning
7:0		Reserved

CACHE Options Port #1

INDEX 0022H: (Reset State = 00H) R/W

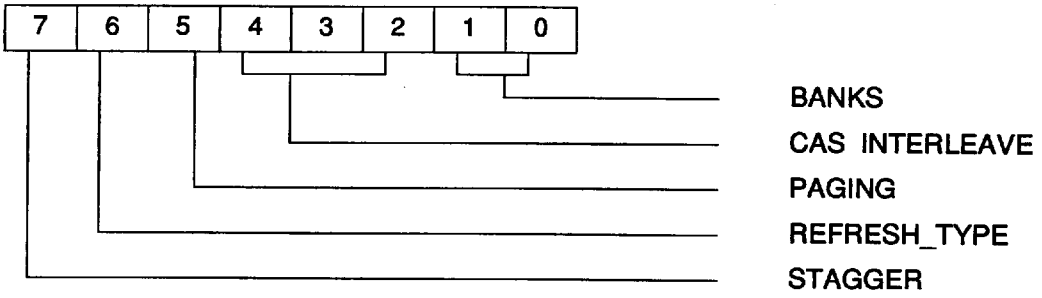


Bit	Value	Meaning
0	1	Cache enabled***
	0	Cache disabled
7:1		Reserved, Do not change contents

*** This bit provides a general enable for caching DRAM cycles in the 486 primary cache.

DRAM Options Port #1

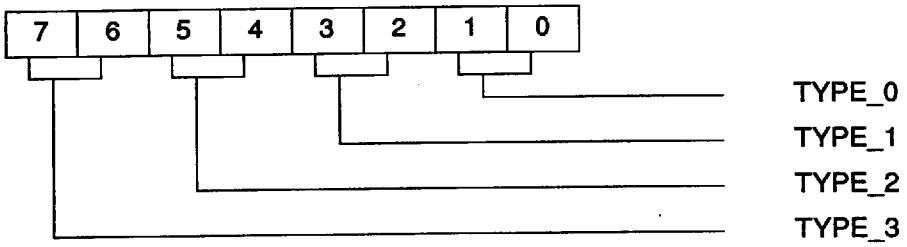
INDEX 0024H: (Reset State= 00H) R/W



Bit(s)	Value	Meaning
1:0		Number of banks installed:
	0 0	1 bank
	0 1	2 banks
	1 0	3 banks
	1 1	4 banks
4:2		CAS interleave type:
	0 0 0	No interleave
	0 0 1	2-way interleave on LOW Banks
	0 1 0	2-way interleave on HIGH Banks
	0 1 1	2-way interleave on Both LOW and HIGH Banks
	1 0 0	4-way interleave
	1 0 1	Reserved. Do not program.
	1 1 0	Reserved. Do not program.
	1 1 1	Reserved. Do not program.
5	0	DRAM Paging Disabled
	1	DRAM Paging Enabled
6	0	RAS Only Refresh
	1	CAS Before RAS Refresh
7	0	Staggered Refresh Disabled
	1	Staggered Refresh Enabled

DRAM Options Port #2

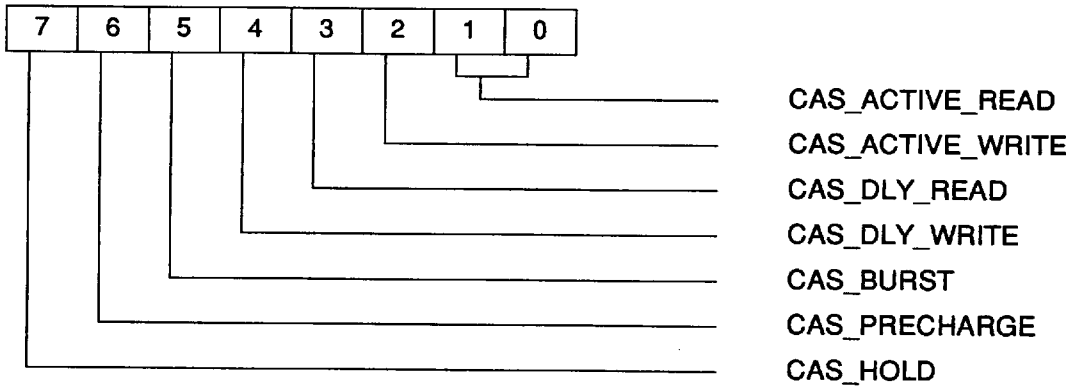
INDEX 0025H: (Reset State = 00H) R/W



Bit(s)	Value	Meaning
1:0		Type of DRAMs in bank 0
3:2		Type of DRAMs in bank 1
5:4		Type of DRAMs in bank 2
7:6		Type of DRAMs in bank 3
	0 0	256K DRAM type
	0 1	1Mb DRAM type
	1 0	4Mb DRAM type
	1 1	16Mb DRAM type

DRAM Options Port # 3

INDEX 0026H: (Reset State= FFH) R/W

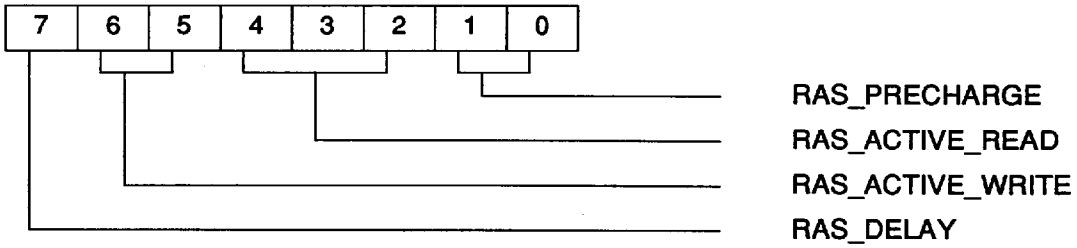


Bit(s)	Value	Meaning
1:0		CAS ACTIVE TIME (READS)
	0 0	1 HCLK
	0 1	2 HCLKs
	1 0	3 HCLKs
	1 1	4 HCLKs
2		CAS ACTIVE TIME (WRITES)
	0	1 HCLK
	1	2 HCLKs
3		CAS DELAY (READS)
	0	1 HCLK
	1	2 HCLKs
4		CAS DELAY (WRITES)
	0	1 HCLK
	1	2 HCLKs
5		First CAS BURST DELAY
	0	NONE
	1	1 HCLK
6		CAS PRECHARGE
	0	0.5 HCLK
	1	1 HCLK

7		CAS HOLD on RAS (CAS before RAS REFRESH)
	0	1 HCLK
	1	2 HCLKs

DRAM Options Port # 4

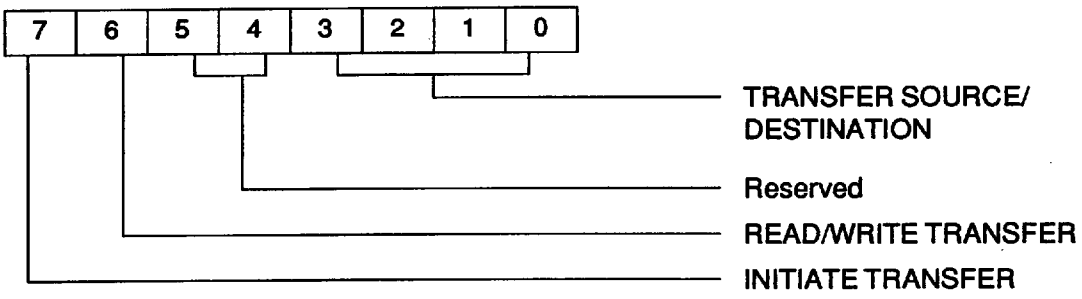
INDEX 0027H: (Reset State = FFH) R/W



Bit(s)	Value	Meaning
1:0		RAS PRECHARGE
	00	1 HCLK
	01	2 HCLKs
	10	3 HCLKs
	11	4 HCLKs
4:2		RAS ACTIVE (READS)
	000	2 HCLKs
	001	3 HCLKs
	010	4 HCLKs
	011	5 HCLKs
	100	6 HCLKs
	101	7 HCLKs
	110	8 HCLKs
	111	9 HCLKs
6:5		RAS ACTIVE (WRITES)
	00	2 HCLKs
	01	3 HCLKs
	10	4 HCLKs
	11	5 HCLKs
7		RAS Delay
	0	No RAS Delay (0 HCLK)
	1	1 HCLK Delay

Data Transfer Control Port (See section Accessing HT342 Registers)

INDEX 28H: (Reset State = 00H) R/W



Bit(s)	Value	Meaning
3:0		Transfer source/destination
	0000	EMS translation RAM location (MSB)
	0001	EMS translation RAM location (LSB)
	0010	REMAP RAM translation location
	0011	EMS Page Descriptor RAM location
	0100	Reserved. Do not program.
	0101	Reserved. Do not program.
	0110	Reserved. Do not program.
	0111	Reserved. Do not program.
	1000	NON_CACHEHIMEM register (MSB)
	1001	NON_CACHEHIMEM register (LSB)
	1010	NON_CACHE1MLO register
	1011	NON_CACHE1MHI register
	1100	TOP_OF_REMAP_MEMORY register (MSB)
	1101	TOP_OF_REMAP_MEMORY register (LSB)
	1110	TOP_OF_MEMORY register (MSB)
	1111	TOP_OF_MEMORY register (LSB)
4:5		Reserved. Do not change contents.
6	0	Read transfer.
	1	Write transfer.
7	0	No action.
	1	Initiate transfer.

Writing to this port can initiate a transfer of data to/from the Data Transfer Register. The source/destination of the transfer is specified by the data value written to the port. The direction of the transfer is specified by bit 6. If bit 6 is reset, the transfer will be (if initiated) a read transfer (from a RAM location/register to the Data Transfer Register); otherwise it will be a write transfer (from the Data Transfer Register to a RAM location/register). Setting bit 7 while writing to the port initiates the transfer.

The source/destination of the transfer specified by bits 3:0 could be :

- one of the RAMs (the location address is specified by the RAM Address Register), or
- one of the Cacheability Registers, or
- one of the Memory Boundary Registers.

Reading from this port brings back the source/destination value on bits 3:0 and the direction of the transfer on bit 6. Bit 7 is not readable since it only controls the transfer operation.

Before initiating a write transfer, data has to be written to the Data Transfer Register. If the write transfer is intended for a RAM location, the RAM Address Register should also be set properly prior to the transfer.

Before initiating a read transfer from a RAM location, the RAM Address Register should be set properly with the address of the RAM location.

After completing the read transfer, data can be read from the Data Transfer Register.

RAM Address Register (See section Accessing HT342 Registers)

INDEX 29H: (Reset State = 00H) R/W

Reading this index port reads the data stored in the address register. Writing to the index port writes the value from the HD data bus to the address register.

Bit(s)	Value	Meaning
4:0		RAM address register contents
7:5		Reserved. Do not change contents.

Data Transfer Port (See section Accessing HT342 Registers)

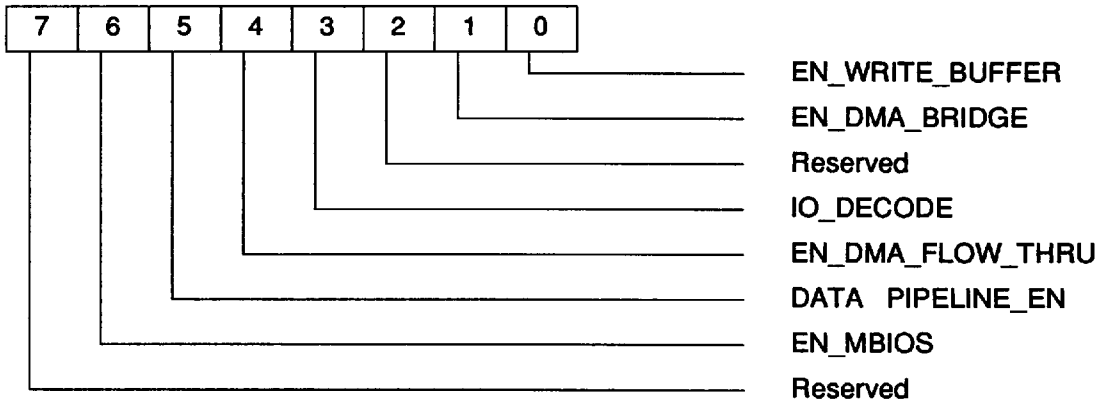
INDEX 2AH: (Reset State = 00H) R/W

Reading this index port reads the data stored in the data register. Writing to the index port writes the value from the HD data bus to the register.

Bit(s)	Value	Meaning
7:0		Data register contents

Other options

INDEX 002BH: (Reset State = 00H) R/W



Bit(s)	Value	Meaning
0	0	Write buffering disabled
	1	Write buffering enabled
1	0	16-bit DMA bridge enabled
	1	16-bit DMA bridge disabled
2	0	Reserved. Do not program
	1	Reserved. Do not program
3	0	10-bit I/O Decode
	1	16-bit I/O Decode
4	0	DMA Flow-thru Mode is disabled
	1	DMA Flow-thru Mode is enabled
5	0	Data Pipeline disabled
	1	Data Pipeline enabled
6	0	Middle BIOS disabled
	1	Middle BIOS enabled
7	0	Reserved
	1	Reserved

WRITE Buffering

When enabled provides for early write cycle termination. When disabled will cause extended cycles.

16-bit DMA Bridge

This option disables 16-bit DMA internal data bridging. It should only be used with 32-bit DMA devices on the HTK320 Local Bus (if there are any installed).

DMA Flow-thru Mode Override

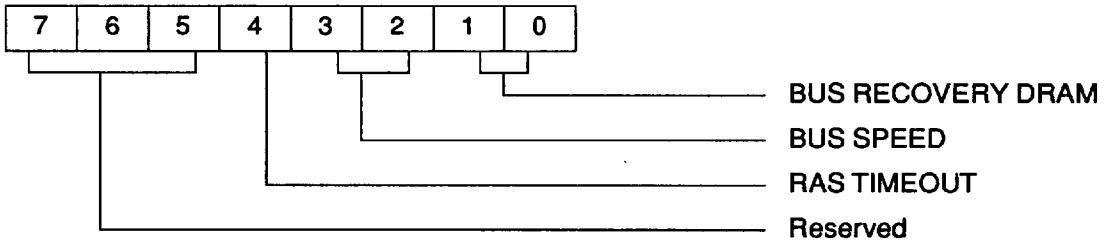
This mode of operation affects DMA cycles only. It disables write buffering by shutting the entire stage of the pipeline off. The mode minimizes the latency of the DMA cycles and speeds the read cycles up during DMA. The bit enables special handshake mechanisms between the HT342 and HT321 controllers. Every time the CPU grants the bus to the HT321 controller, the grant is not passed to the ISA backplane until the HT342 signals its readiness with asserting HRDYN signal. The HT342 does that after offloading the write buffers and shutting the write buffering pipeline off. That is why both the HT342 and HT321 controllers should have the DMA flow-thru bits set for this mode to be operational.

Data Pipeline Enable

See LOCAL_BUS_CONTROLLER description on page 36 for details.

DRAM Options Port #5

INDEX 002DH: (Reset State = 03H) R/W



Bit(s)	Value	Meaning
1:0		BUS Recovery for DRAM cycles
	0 0	No recovery
	0 1	1 HCLK
	1 0	0.5 HCLK
	1 1	1 HCLK
3:2		BUS Speed
	0 0	33MHz
	0 1	25MHz
	1 0	20MHz
	1 1	16MHz
4		RAS Timeout
	0	10uS RAS Timeout disabled
	1	10uS RAS Timeout enabled
7:5		Reserved. Do not change contents.

Cacheability Registers (See section Accessing HT342 Registers)

These registers are accessed via the standard Data Transfer Control Port (Index 28H) mechanism. They are read/write registers.

NON_CACHEHIMEM Register

14 bit register. Reset State = 040H (points at 1MB boundary)

Bit(s)	Value	Meaning
13:0		Address bits 27:14 specifying the highest DRAM address +1 for which the cache controller should cache a memory cycle. Any DRAM cycle above the address should be considered non-cacheable.

NON_CACHE1MLO = 0H (points at the beginning of the memory)

Bit(s)
5:6

NON_CACHE1MHI = 28H (points at segment A000)

Bit(s)	Value	Meaning
5:0		Address bits 19:14 specifying boundaries for a window below 1MB of memory. Any DRAM cycle within the memory area should be considered non-cacheable. NON_CACHE1MLO specifies the low boundary, NON_CACHE1MHI the high one.

Memory Boundary Registers (See section Accessing HT342 Registers)

Remap RAM Translation Location

5 bit register. Reset State = 040H. Used to assign Virtual Pages above Top of Memory to physical EMS pages.

Bit(s)	Value	Meaning
4:0	0:18H	Values represent translated virtual page numbers above Top of Memory Register for current translation and store corresponding physical EMS page numbers used in the remapping physical DRAM in the 640K TO 1MB memory space.

TOP_OF_REMAP_MEMORY Register

14 bit register. Reset State = 040H (points at 1MB boundary).

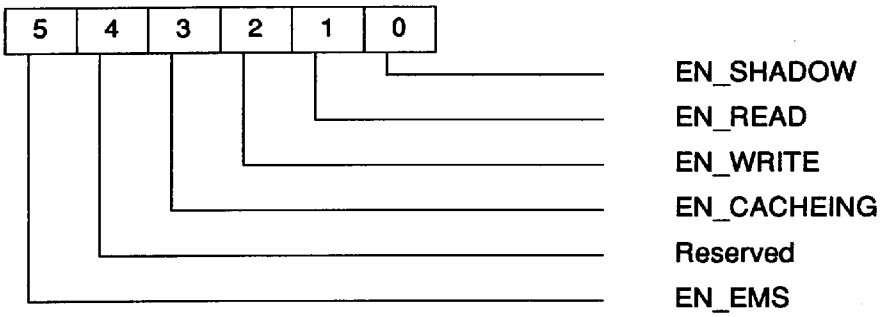
Bit(s)	Value	Meaning
13:0		Specifies the highest (+ 1) memory address (bits 27:14) which will be directed to the DRAM subsytem. The REMAP translation RAM contains the mapping scheme. This register value should be equal to TOP_OF_MEMORY + number of remapped EMS 16KB Blocks.

TOP_OF_MEMORY Register

14 bit register. Reset State = 040H (points at 1MB boundary).

Bit(s)	Value	Meaning
13:0		Specifies the highest (+ 1) memory address (bits 27:14) which will be directed to the DRAM subsytem if there is no REMAPPING in the system (effectively, it specifies the total amount of contiguous memory installed).

EMS Page Descriptor Registers (See section Accessing HT342 Registers)



An EMS page is a 16KB Block of memory between 640K and 1MB address space. Therefore, there are 24 EMS pages in an IBM PC address space.

Every one of the pages has a 6-bit register associated with it called EMS Page Descriptor Register. These registers are stored in a RAM called EMS Page Descriptor RAM. Pages are numbered 0 - 23 and page 0 corresponds to the 16K chunk right above the 640K boundary. The page numbers address the Page Descriptors RAM when the writing to the RAM process occurs.

NOTE: PAGE 0 corresponds to RAM Address = 8

Outlined below is the content of an EMS Page Descriptor Register. **(Reset State = 00H)**

Bit(s)	Value	Meaning
0	0	Shadowing is disabled
	1	Shadowing is enabled
1	0	Reading is disabled
	1	Reading is enabled
2	0	Writing is disabled
	1	Writing is enabled
3	0	Cacheing is disabled
	1	Cacheing is enabled
4	0	Reserved. Always program to "0"
5	0	EMS translation is disabled
	1	EMS translation is enabled

A read cycle directed to the EMS page will be treated as a DRAM cycle if:

- EMS is enabled, or
- Shadowing is enabled and Reading is enabled.

A write cycle directed to the EMS page will be treated as a DRAM cycle if:

- EMS is enabled, or
- Shadowing is enabled and Writing is enabled.

EMS Translation RAM (ETR) Location

14 bit register. Reset State = 040H. The ETR Address will set the translated physical address starting point for each 16K EMS window using a LIM EMS 4.0 compatible driver anywhere in physical memory. This EMS architecture defines 24 EMS pages sharing 4 ETR entries on translated EMS address.

Bit(s)	Value	Meaning
13:0		Address bits 27:14 of the target address for the current EMS Address Translation.

Accessing HT342 Registers

Straight Indexing Scheme

The straight indexing scheme applies to all so-called static registers. They contain the static bits configuring the HT342 by enabling, disabling and setting chip set features.

The general scheme to access these registers is simple:

- IOW to address 28H sets an index of the register to be accessed.

- IOW/IOR to/from address 24H writes/reads the value to/from the indexed register.

Double Indexing Scheme

The HT342 contains many table-based Remapping, EMS and Cacheability Translations.

These translation tables are all accessed through the configuration registers. If there were an INDEX per table entry, there would be too many INDICES. Instead, there is a double indexing scheme. The normal Indices address the Data Transfer Port, RAM Address Register and Data Transfer Control Port. These registers are used to access the tables, thus only three indices are required for all of them.

The Data Transfer Port resides at index 2AH, RAM Address Register at index 29H and Data Transfer Port at index 28H. The bits are all defined in the HT342 Register Description Section of the Data Sheet.

Two categories of data storage are accessed via the Double Indexing Scheme:

- RAM locations containing Translation table Entries, and EMS Page Description Registers.

- Static Registers called RAM-like Registers. These are Cacheability Registers and Memory Boundary Registers.

The only difference between the two categories is that RAM locations require a RAM Address Register to be filled in while transferring data to/from the location, and the RAM-like registers do not. Except for that, the access method is the same.

The sequence below describes how to write to a RAM location. For a RAM-like register, omit the step when the RAM Address Register is being set.

1. Set RAM Address Register

    - IOW to address 28H with value 29H

    - IOW to address 24H with RAM address value

2. Set Data Transfer Port

- IOW to address 28H with value 2AH

- IOW to address 24H with data of value to be transferred

3. Initiate the write transfer

- IOW to address 28H with value 28H

- IOW to address 24H with value:

a) bits 3:0 specify the destination of the transfer
b) bit 6 set
c) bit 7 set

The sequence below describes how to read a RAM location. For a RAM-like register, omit the step when the RAM Address Register is being set.

1. Set RAM Address Register

- IOW to address 28H with value 29H

- IOW to address 24H with RAM address value

2. Initiate the read transfer

- IOW to address 28H with value 28H

- IOW to address 24H with value:

a) bits 3:0 specify the source of the transfer
b) bit 6 reset
c) bit 7 set

3. Read data from Data Transfer Port

- IOW to address 28H with value 2AH

- IOR from address 24H gives the data transferred value

Setting DRAM Memory Size and Remapping

Memory Address Range and Decoding

The range of memory to which this chip responds is directly related to the type and number of DRAM banks installed. It is up to the user to determine the upper boundary of memory to which the chip is to respond. The memory address decode section is affected by 2 operations: EMS, Remapping. There are two key registers which determine if the HT342 will respond to a processor memory cycle: TOP_OF_REMAP_MEMORY (TRM) and TOP_OF_MEMORY (TM). Register TM describes the total amount of DRAM in the system. If there were 4 banks of 1M DRAMs, totalling 16 Megabytes, then the TM register would contain the necessary bits to describe 16 Megabytes. Register TRM describes the Upper Address Limit to which the HT342 is to respond. This will be the same as the TM register except when Remap is enabled. Remap is enabled if TRM > TM. Selected blocks of the 384K of Memory between 640K and 1M will be remapped beyond the Total Physical Memory. The difference between TRM and TM is the amount of memory to be remapped. The Maximum, TRM - TM = 384K. The HT342 will respond to all addresses below the value set by TRM.

Note that it is possible to program TRM to be greater than TM + 384K. It is also possible to program TRM < TM. These errors will result in Aliasing of Memory Blocks. **THIS MUST BE AVOIDED.**

Representation

The basic memory block or page size has been set to 16K. Remapping, EMS and cacheability are all identified in this basic unit. The TRM and TM Registers are programmed for Address Comparison with those on the HA bus. The TM/TRM Bits are compared with HA[27:14]. Thus, both TRM and TM registers are 14 bits wide and hold values representing Address Bits [27:14]. For instance, values of 16, 17 and 18 Megabytes would be represented by 00010000000000 Binary or 0400 Hex; 00010001000000B or 0440H; 00010010000000B or 0480H respectively.

The EMS Translation Table Register, Cacheability and EMS Page Descriptor Registers also use this structure. These other registers are described later.

Remap

In order to enable Remap of the Physical DRAM Memory between the 640K and 1MB space the TRM Register Value must exceed that of the TM Register. The REMAP RAM which contains the translation table setting the remapping scheme must also be programmed. The scheme implemented in the HT342 provides unlimited flexibility in remapping any of the 16K pages of DRAM between 640K to 1M above the Top of Physical Memory, at the same time allowing other pages to be shadowed or used as a standard EMS page as defined in the LIM EMS 4.0 Specification. For example, 8 physical pages could be shadowed (System and Video BIOS), 1 paged used for an EMS page (by LIM EMS driver) and the remaining 15 pages remapped above top of memory, available for system use. Additional flexability allow these 24 pages to be defined as cachable pages.

The following table shows the 24, 16K EMS pages defined for the memory space between 640 and 1024K.

HT342 Register Access

		Page	RAM Address Register	Virtual RAM Address
1024K	100000H	23	18H	1FH
	0FC000	22	17H	1EH
	0F8000	21	16H	1DH
	0F4000	20	15H	1CH
960K	0F0000	19	14H	1BH
	0EC000	18	13H	1AH
	0E8000	17	12H	19H
	0E4000	16	11H	18H
896K	0E0000	15	10H	17H
	0DC000	14	0FH	16H
	0D8000	13	0EH	15H
	0D4000	12	0DH	14H
832K	0D0000	11	0CH	13H
	0CC000	10	0BH	12H
	0C8000	9	0AH	11H
	0C4000	8	09H	10H
768K	0C0000	7	08H	0FH
	0BC000	6	07H	0EH
	0B8000	5	06H	0DH
	0B4000	4	05H	0CH
704K	0B0000	3	04H	0BH
	0AC000	2	03H	0AH
	0A8000	1	02H	09H
	0A4000	0	01H	08H
640K	0A000H			Data Transfer Register

If the REMAP RAM was loaded as the Table above describes, all 24 EMS pages (384KB) of Memory would be Remapped above the Top of Memory.

The order of Physical Page numbers placed in the Data Transfer Register does not matter, they can be set in any order. The same applies to the number of pages remapped.

Shadowing

Shadowing INCREASES performance by duplication of code contained in "slower EPROM" into "faster DRAM". The HT342 supports shadowing for any of the 24 EMS pages. EMS Page Descriptor Registers have been defined for each of the 24 pages. Each Register has 3 programmable Shadowing Attributes :

- Shadowing Enabled/Disabled (if this Bit is reset, the following two do not matter)
- Reading Enabled/Disabled (if the global shadowing Bit is set, this Bit determines whether a Read Cycle will Access the DRAM.
- Writing Enabled/Disabled (if the global shadowing Bit is set, this Bit determines whether a Write Cycle access the DRAM.

The sample source code below illustrates how Shadowing of the main 64KB BIOS might be achieved using the methods described above.

SHDWBIOS 1.00 Copyright LSI Logic Corporation of Canada Inc.
SHDWBIOS.ASM

```
COFFSET equ     0f000h          ; We want to shadow the system BIOS
PAGES   equ     4               ; We Want to shadow only four pages, ie 64k
code    segment public
        assume cs:code,ds:code
initialize proc near
phinst:
; Setup DRAMS so that we read from EPROMs and write into DRAMS
    mov     ax,COFFSET          ; Get the code offset
    sub     ax,0a000h           ; Subtract 640k
    mov     dx,0                ; Setup for 16-bit divide
    mov     bx,400h             ; Divide this resultant by 16K
```

```
        idiv    bx          ; Page offset is now in ax
        add     al,8        ; This is the 8 offset assigning page 0 to RAM location 8
        mov     dl,al       ; Save resultant
        mov     dh,dl       ; and keep one more copy
        mov     cx,PAGES    ; This is the number of pages to convert
wxfer_set:
        mov     al,29h      ; Get the Transfer address loaded
        out     28h,al
        mov     al,dl       ; Get the address for this page
        out     24h,al
        inc     dl          ; Bump Page address for next time
        mov     al,2ah      ; Get the Transfer data loaded
        out     28h,al
        mov     al,5        ; Turn on shadowing with writing to DRAMS
        out     24h,al
        mov     al,28h      ; Initiate a write transfer
        out     28h,al
        mov     al,0c3h
        out     24h,al
        loop    wxfer_set   ; Continue definition of 16k pages
; Now block load the EPROM into the underlying DRAM
        mov     ax,COFFSET  ; Set pointer to the BIOS
        mov     ds,ax
        mov     dl,PAGES
xfer0:
        mov     bx,0        ; Start at the beginning of the BIOS
        mov     cx,2000h    ; Do a 16k data sweep
```

```
xfer1:
    mov   ax,[bx]       ; Read from EPROM
    mov   [bx],ax       ; Give to dynamic RAM
    inc   bx
    inc   bx            ; Bump pointer
    loop  xfer1         ; Loop until 64k is done
    dec   dl            ; Reduce number of pages to do
    jz    xfer2         ; Jump if all pages done
    mov   ax,ds         ; Bump Data Segment by 16K
    add   ax,400h
    mov   ds,ax         ; Save new segment
    jmp   xfer0
; Setup DRAMS so that we read from DRAMS and write into EPROMs
xfer2:
    mov   dl,dh         ; Get back the page offset
    mov   cx,PAGES      ; This is the number of pages to convert
rxfer_set:
    mov   al,29h        ; Get the Transfer address loaded
    out   28h,al
    mov   al,dl         ; Get the address for this page
    out   24h,al
    inc   dl            ; Bump the page pointer
    mov   al,2ah        ; Get the Transfer data loaded
    out   28h,al
    mov   al,0bh        ; Turn on shadowing with reading from DRAMS
    out   24h,al        ; and turn on the cache controller
    mov   al,28h        ; Initiate a write transfer
    out   28h,al
    mov   al,0c3h
```

```
        out     24h,al
        loop    rxfer_set
    ; Now get back to DOS
        mov     ah,0
        int     21h
    initialize endp
    code        ends
        end     phinst
```

EMS 4.0 Support

Any one of the 24 EMS pages can be used as an EMS page in the sense of the LIM™ EMS 4.0 Specification.

The HT342 provides a limited flexibility for translation any of the 24 EMS Page Addresses Anywhere in Memory. This is achieved by means of enabling EMS Bit of the EMS Page Descriptor Register(this overrides shadowing) and loading the EMS Translation RAM (ETR) to point to the Translated Address. There is a limitation of the process : only 4 ETR locations are provided for all 24 EMS pages. In this way page 0 shares its ETR entry with pages: 4,8,12,16,20; page 1 with 5,9,13,17,21, etc..

The ETR is a 14-bit register representing Bits 27 to 14 of the target address for the current EMS Address Translation. In this way a Window that will point anywhere in Memory from EMS space may be set . Any one of the 24 EMS pages may be programmed, but only 4 ETR entries are available.

In order to enable a 16KB EMS window using Page 0 (at Physical Address A000:0000) as an EMS page and access a 16KB Memory Block immediately above the 1MB boundary, do the following:

1. Set EMS Page Descriptor Register for page 0 (RAM address 8) to 20H - EMS bit on.

2. Set EMS Translation location MSB to 0 (RAM address 8).

3. Set EMS Translation location LSB to 40H (RAM address always set to page number + 8, which in this case is 8).

There will now be a 16K EMS window at A000:0000. Access to this Address+offset will result in access to the physical address 10000:0000+offset.

Notes :

EMS vs. remapped memory:

Remapped Memory cannot be accessed by means of an EMS window.

However, a DRAM memory within EMS space can be remapped.

EMS and shadow:

EMS takes precedence over Shadowing. That means if both EMS and Shadowing are enabled the Page will default to an EMS Page and Address Translation will be activated.

Cacheability

The Cacheability Registers referenced in previous paragraphs define Non-Cacheable regions of memory. 26 different regions may be described. A window below 1MB may be set by means of the NON_CACHE1MLO (NC1MLO) and NON_CACHE1MHI (NC1MHI) registers.

These registers will not effect cacheability if they contain equal values. NC1MLO sets the low boundary of a non-cacheable region below 1MB and NC1MHI sets the high boundary of the region. A further register affecting cacheability is NON_CACHEHIMEM (NCHM). It sets a limit above which everything is non-cacheable. Normally this register's content equals that of the TRM register. It is possible to disable caching totally by loading MSB and LSB of this register with 0.

Each of the 24 EMS pages has an associated cache-ability bit. This defines a further 24 regions of Cache Control.

Notes :

Caching and Remap:

Remapped space can be cached. Flush the cache, though, each time the REMAP Table is changed (usually this table is set only once; during the boot phase).

Caching and shadowing:

Shadowed space can be cached. No restrictions apply.

Caching and EMS:

EMS space can also be cached. Flush the cache, though, each time a context switch occurs.

Pin Name	Pin Number	Pin Type	Description
Local Bus Interface			
EADS*	172	O	When in 486 mode, this pin is used as the EADS* connection, indicating that the HT321 has applied a valid address onto the Shasta local bus, when snooping may be required.
HA[31,27:2]	38-25, 22-10	I/O	Host Address Bus. Normally these lines are Inputs and they define the address of the device being accessed on the backplane. During DMA or Backplane MASTER cycles, these Address lines will be Outputs driven to the HA bus.
HADS*	44	I/O	Host Address Strobe, active low. This indicates that the address and status lines from the processor are stable and valid. They are valid from the Clock edge near the end of HADS*, or from the rising edge of HADS*. During DMA or Backplane MASTER cycles this signal will be an Output and will be strobed when the HA, HBEN and status lines are stable.
HBEN*[3:0]	40-43	I/O	Host Byte Enables, active low. These signals define onto which byte the data will be transfered. During DMA or Backplane MASTER cycles, these lines will be driven by the HT321.
HCLK	163	I	Host Clock. This is a single phase clock that drives the entire system. This clock drives the entire HT321.
HD[15:0]	176-183, 2-9	I/O	Host Data Bus. When configuration registers are Read/Written, data will pass over the data bus. All backplane accesses are also passed via the ISA controller to/from the Local Host Data Bus.
HHLDA	168	I	Host Hold Acknowledge, active high. This signal from the CPU, indicates the Host Bus has been released and is free for use.

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
HLOCAL*	167	I	Host Local Cycle, active low. This is asserted as result of a LOCAL Bus Device decoding a Valid Address for it's operation (normally the HT342 Controller). It will be active one clock after HADS* and will remain low for 1 HCLK. It will then be driven high, then tri-stated. If this signal is not detected 1 HCLK cycles after HADS*, then the HT321 will operate as the CPU Default Access, and initiate the sequence for the Backplane
HMIO HDC HWR	175-173	I/O	Host Status Lines: HMIO, HDC and HWR.(Host Memory I/O, Host Data Code and Host Write Read) These signals, validated at HADS*, define the type of CPU access. During DMA or Backplane MASTER accesses these lines will be driven by the HT321.
HRDYI*	165	I	Host Ready In, active low. During all cycles this signal going active signifies termination of the cycle.
HRDY*	39	I/O	Host Ready, active low. This signal goes active to indicate the readyness to end the cycle. The Signal duration will be one HCLK, then will be driven high and tristated.
HREFRESH*	171	I/O	Host Refresh, active low. This signal indicates a Refresh Cycle to the DRAM Controller and Backplane. This signal is initiated from Internal Timer Channel 1.During MASTER mode this signal is an Input and a Refresh cycle can be initiated by asserting it low.
HRESCPU	170	O	Host reset, active high. When this signal is active, the processor is being reset. This signal will be asserted by the ISA Controller when a System Reset occurs, or a Shutdown is detected, or RC occurs, or when Port 92 FAST_RC occurs.

Pin Name	Pin Number	Pin Type	Description
KB_CLAMPA20*	166	I	KeyBoard Clamp A20, active low. When active, HA20 should be treated as low regardless of what the real level of the line is. When high, HA20 should be treated normally.
PARITY*	169	I	Parity Check, active low. This is activated by a Memory Device on the Shasta Local Bus when it detects a Parity Error. It remains active for 1 HCLK, then is de-asserted and tri-stated. Once active, if the internal Parity Mask is open, an NMI will occur.
CPU Interface			
BS16*	45	O	Bus Size 16, active low.The HT321 indicates to the CPU that it can only accept data on HD[0:15]. If more than two bytes of data are required for the cycle, the CPU must perform a second cycle to acquire/present all the Data.
HOLDREQ	48	O	Host Hold Request, active high. This signal is asserted when a DMA (or MASTER DMA)request occurs. It will remain high until the Temporary Bus master completes it's Cycle(s).
INT	50	O	Host Interrupt, active high. When asserted, the HT321 is requesting the CPU execute an Interrupt cycle. The signal source is the Internal 8259 Interrupt Controller.
NMI	49	O	Non-Maskable Interrupt, active high. When active, the HT321 is requesting that the CPU execute a Non Maskable Interrupt sequence. This is usually the result of a PARITY* check or IOCHCK asserted during a Backplane cycle.
RESETNPU	51	O	RESET Co-Processor. This line, active high, Resets a Co-processor device on the Local Bus.Connect it to the RESETI* line of the Co-Processor.

Pin Name	Pin Number	Pin Type	Description
Backplane Interface			
AEN	164	O	Address Enable, active high. When high during a DMA cycle, either 8 or 16 bit, I/O devices other than the Active DACK should not activate decode. Used in conjunction with HHLDA it can determine which type of access is currently in progress. AEN HHLDA Cycle 0 0 CPU 0 1 MASTER 1 0 Refresh 1 1 DMA
BALE	75	O	Bus Address Latch Enable. When high, the Address on the SA values may be changing. At the falling edge, all Address lines will be guaranteed stable. This signal is normally low for all non-backplane accesses. During MASTER, Refresh or DMA, Cycles this signal will remain high.
BCLK	68	O	Backplane System Clock. This Clock to the backplane is synchronized with the Commands of the HT321 and has a Frequency of 8.00 - 8.33 MHz.
DACK*[7:5],[3:0]	65-59	O	DMA Acknowledge. Active low. These signals are the respective Bus Grant Signals to DRQ requests.
DRQ[7:5],[3:0]	58-52	I	DMA Requests. These signals are used by Backplane DMA or Master DMA devices. Priorities decrease from 0 to 7. DMA Channels 0 to 3, perform 8-bit cycles, Channels 5 to 7, 16-bit cycles.
IOCHK*	159	I	I/O Channel Check, active low. When asserted, it indicates that a fatal system failure at a Backplane device. If enabled, the result is an NMI

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
IOCHRDY	144	I/O	I/O Channel Ready, active high. This signal indicates that no wait state insertion is necessary for the current backplane cycle. Slow I/O devices can Negate this Signal to Suspend the Cycle until Ready for completion.
IOCS16*	142	I	I/O Chip Select is 16-bits, active low.Asserted by the respondant Backplane Device, it indicates Acceptance of a 16-bit transfer for the Current I/O Cycle .
IOR*	66	I/O	I/O Read, active low. This signal indicates an I/O read operation is in progress on the backplane. For CPU and DMA cycles, this signal is an Output; for MASTER Mode cycles it is an input.
IOW*	67	I/O	I/O Write, active low. This signal indicates when an I/O Write operation is in progress. During Local Host Bus I/O Memory access, this signal will not be active. Normally an Output, during Master mode accesses this signal will be in input.
IRQ1	158	I	Interrupt Request 1. Interrupt from the 8042 Keyboard Controller, called by pseudonym "OPTBUFULL".
IRQ15,14,[12:9], [7:3]	145-146, 148-151, 153-157	I	Interrupt Requests. Interrupts from the I/O Channel indicate that an Peripheral on the Backplane is requesting service by the CPU. Inputs to the 8259 Interrupt Controller of the HT321. Priorities decrease from IRQ[9:15] and then from IRQ3 down to IRQ 7. An interrupt request is generated on the rising edge of an IRQ which must be maintained high until acknowledged by the INTA cycle.
IRQ8*	152	I	Interrupt Request 8. Active low. Real Time Clock interrupt.

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
IRQ13	147	I	Interrupt Request 13. When high, the Numerical Co-Processor has detected an Exception and requests Interrupt Service.
LA[23:17]	112-106	I/O	Backplane Address Bits 23 to 17. These signals are flow- thru Addresses to the Backplane. These signals are Outputs during all cycles except MASTER cycles when they are Inputs.
LBHEN*	137	I/O	Latched Bus High Enable. Active low. This signal will be an Output during Backplane cycles initiated by the HT321 (both CPU and DMA).This signal will be an input during MASTER Mode accesses.
MASTER*	140	I	The ISA Backplane Master cycle indicator, active low. When active at the DRQ/DACK exchange, it indicates that a Backplane Master device owns the Shasta local bus using the HT321 as a Synchronizer/Interface chip between the ISA and Shasta Local Bus.
MEMCS16*	141	I	Memory Chip Select is 16 bits, active low. Asserted by the respondant Backplane Device, it indicates Acceptance of a 16-bit transfer for the Current Cycle.
MEMR*	71	I/O	Memory Read, active low. When active, this signal indicates that a Memory Read Cycle is in progress on the backplane. This signal will be active for all backplane accesses below 16 Mbytes. Normally an Output,during a MASTER Mode Cycle, this signal will be an Input.
MEMW*	72	I/O	Memory Write, active low.When active, this signal indicates that a Memory Write Cycle is in progress on the backplane. This signal will be active for all memory backplane accesses below 16 Mbytes. Normally an Output,during a MASTER Mode Cycle, this signal will be an Input.

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
OSC	160	I	Oscillator (14.31818 MHz),to the backplane. The HT321 divides this by twelve to produce 1.19MHz for the Internal 8254 equivalent. (equal to T.V. Colour-burst Frequency)
RESETDRV	76	O	Backplane Reset, active high. When active, all devices on the backplane should initialise. This signal is activated by a power on reset.
SA[19:0]	136-129, 126-117, 114,113	I/O	System Address 0 to 19. These signals are the latched addresses to the backplane. SA0 and SA1 are calculated from the HBENs during non-refresh cycles. During Refresh Cycles, these lines contain the Refresh Address. During all cycles except MASTER these lines are Outputs.
SD[15:0]	103-94,91-86	I/O	System Data Bus 0 to 15. This data bus connects directly to the ISA backplane and is used to transfer information to/from the HT321 and the ISA Backplane peripherals. The direction of data flow depends on the type of cycle and the originator. (i.e. ISA Bus MASTER, CPU or HT321).
SMEMR*	73	O	System Memory Read, active low. This backplane signal is similar in timing to the MEMR signal except that it is only active for accesses to the backplane below 1 Mbyte and is always an Output.
SMEMW*	74	O	System Memory Write, active low. This backplane signal indicates that a Memory Write is in progress to an Address below 1 Mbyte. This signal is derived from MEMW so has the same timing, but is always an Output.
TC	85	O	Terminal Count, active high. When active, it indicates the DMA controller has reached the end of its Address Increment/Decrement Count.

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
0WS*	143	I	Zero Wait State, active low.Asserted by the respondant Backplane Device, this signal indicates that the slave device requests early Termination of the Backplane Cycle or is capable of a Zero Wait State Cycle.
Peripheral Interface			
KBCS*	80	O	Chip select for the system Keyboard Controller. Active low.
RC	77	I	Keyboard reset, active low. When asserted, the 8042 keyboard controller is requesting a "warm Shasta Local Bus Reset".
ROMEN	79	O	Output Enable/Chip Select for the System BIOS ROM.If Index 07, bit 4 =0, this signal is ROM Address Space qualified with MEMR*. If Index 07, bit 4 = 1, this signal is simply ROM Address Space selected.
RTCCS*/MODE	81	O	Chip select for the system RTC. Active low. During POR this line is read to determine which CPU is connected in the system. If this line is pulled high, 386 mode is selected, if low, 486 mode.
SPKR	78	O	Speaker output signal to drive an external speaker. It is generated by Counter 2 of the 8254 Timer and gated by Bit 1 of Port_B register.

HT321 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
Other signals			
CLAMPA20*/ ROMWIDTH	84	I/O	CLAMP A20, active low. When active, HA20 should be treated as ZERO regardless of what the real Value is. When high, HA20's Value passed as normal. During POR this line is READ to determine whether an 8 or 16-bit EPROM is installed in the system. Low during POR, then ROM accesses are 16-Bit, high ROM is 8-Bit.
POR	82	I	Power On Reset, active high. This is the Power-on Reset that indicates Reset the entire System.
TESTIN	83	I	Input for test patterns or other tests activation. When it is asserted high, all outputs are tri-stated. This may be used by In Circuit Testers. Low for Normal Operation.
VCC	34,46,69,931 05,116,12713 9,161,184		Power
GND	1,24,47,70, 92,104,115,1 28,138,162		Ground

HT342 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
Local Bus Interface			
AHOLD	158	O	Address Hold. This signal is activated during BOFF cycles in order to get hold of the Shasta Local Bus.
BLAST*	25	I/O	Last Burst, active low. This signal is driven by the i486/487SX host and indicates the last bursted cycle in the burst sequence. During BOFF cycles it is driven low (active) by the HT342 MCU controller, since these cycles are not burstable.
BOFF*	62	I/O	Back Off, active low. This signal activated during BOFF cycles in order to get hold of the Local Bus.
BRDY*	37	I/O	Burst Ready, active low. This signal goes active to indicate the burst cycle is ready to end. It is used for all cacheable cycles (including the last one). The signal is always tristated after the last burst is finished.
HA31,HA[27:2]	171,172-183,2-15	I/O	Host Address Bus. These lines are inputs for all non-BOFF cycles and are used to determine if the address of a device currently addressed is a DRAM "hit" meaning if the cycle belongs to the MCU controller. Usually these lines are driven by the CPU, except for the DMA, when they are driven by the ISA controller. During BOFF cycles the lines are driven by the MCU.
HADS*	36	I/O	Host Address Strobe, active low. Defines the beginning of the cycle. During BOFF cycles the line is driven by the MCU.
HBEN*[3:0]	167-170	I/O	Host Byte Enables, active low. These signals define which bytes contain valid transfer data.During DMA cycles they will be driven by the HT321.During DRAM read cycles the state of these signals has no meaning. All four(4) bytes are presented to the Host Data Bus. During BOFF cycles the lines are driven by the MCU.

Pin Name	Pin Number	Pin Type	Description
HCLK	164	I	Host Clock. This clock drives the entire chip.
HD[31:0]	67-63, 59-50,48, 45-38,35, 32-30,21-18	I/O	Host data bus. Data from the MCU controller is driven to the bus during reads and accepted from the bus during writes.
HHLDA	23	I	Hold acknowledge. This signal is used to determine the DMA bridge path. Certain special considerations for write buffering and DRAM algorithms are taken when the signal is active. Active high signal.
HLOCALIN*	26	I	Host Local In, active level. This signal is passed to the HLOCAL* output in the first T2 state clock. In this way, a device on the Shasta Local Bus, which does not support the HLOCAL* protocol, can still be supported. The signal is also sampled, when determining if a BOFF cycle should be performed. If sampled asserted, no BOFF cycle is started. Therefore only 32-bit devices should activate this signal.
HLOCAL*	165	I/O	Host Local, active level. Asserted when the MCU controller decodes a valid address for a DRAM Operation (memory cycles) or configuration operation (I/O cycles). Asserted one clock after HADS* and will remain low for one clock. It will then be driven high and tristated. Asserting HLOCALIN* will also activate this output.
HLOCRDY*	68	I	Local Ready active low. Provides for a Direct Local Ready Path.Allows for connection of less flexible Local Bus Devices.

HT342 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
HMIO, HDC, HWR	159,163,160	I/O	Host Status Line bus: HMIO, HDC, HWR. Host Memory I/O, Host Data Code, Host Write Read. These signals, qualified at HADS*, define the type of CPU access. During DMA or Backplane MASTER accesses,these lines will be driven by the HT321. During BOFF cycles they are driven by the MCU.
HRDY*	157	I/O	Host Ready, active low. This signal is active to indicate readiness to terminate the cycle. This signal will last 1 HCLK, then will be driven high and tristated.
HRDYI*	24	I	Host Ready active low. This is the signal that terminates any cycle on the Shasta Local Bus. It comes from external combinatorial logic and connects to the 486 host READY input.
HREFRESH*	22	I	Host Refresh, active low. This signal indicates to the MCU and backplane that a refresh should occur.
HRESCPU	49	I	Host Reset, active high. The signal resetting the CPU, used for the MCU only to end a possible bursted cycle interrupted by a cycle asynchronous reset.
KEN*	61	I/O	Cache Enable, active low. The signal is asserted by the MCU controller when a cycle is decoded to be a DRAM cycle and it is defined cacheable by its internal cacheability registers. After the cycle is completed the signal is negated and tristated.
PARITY*	60	I/O	Parity Check, active low. This signal goes active when a memory device on the Summit Local Bus detects a parity error. It remains active for 1 HCLK then is driven high and tristated. The DRAM controller will generate the signal when it detects a parity error during a DRAM cycle.

Pin Name	Pin Number	Pin Type	Description
POR	166	I	Power On Reset, active high. This is the Power on Reset that indicates the entire system is being reset.
DRAM Interface			
BANKSELEVN	83	O	This line selects the Bank Accessed in the even group of Banks. It is used to multiplex CASEVN*[0:3] directing them to the appropriate bank.
BANKSELODD	84	O	This line selects the Bank currently Accessed in the Odd group of Banks. It is used to multiplex CASODD*[0:3] directing them to the appropriate bank.
CASEVN*[3:0]	110-107	O	Four CAS signals for each Even Bank of the DRAM memory. There is one CAS line per byte. These signals should be multiplexed using BANKSELEVN signals to access the selected bank. Active low signals.
CASODD*[3:0]	106-104,101	O	Four CAS signals for each Odd Bank of the DRAM Memory. There is one CAS line per byte. These signals should be multiplexed using BANKSELODD signal in order to access the selected bank.Active low signals.
MA[11:1]	99-94, 91-87	O	These are address lines connecting to the memory address lines of the DRAMs.
MAEVN0	86	O	This is the Lower Address line connected to the Least Significant Memory Address line of the Even Banks of DRAM.
MAODD0	100	O	This is the Lower Address line connected to the Least Significant Memory Address line of the Odd Banks of DRAM.
MD[31:0]	156-140, 137-129, 126-121	I/O	This is the dedicated 32-bit Data Bus for the DRAM.

HT342 Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
PARD[3:0]	120-117	I/O	These are Parity Data lines of the DRAM. One Bit per Byte of DRAMs.
RAS*[3:0]	114-111	O	RAS signals to each of the four banks of DRAM Memory. RAS0 corresponds to the first bank, RAS1 to the second, etc. Active low signals.
WEN	85	O	Write Enable. The signal to drive all WE pins of the Banks of DRAM.
Co-processor Interface			
FERR*	29	I	Floating point Error, active low. This line signals a co-processor error has occurred. It connects to the FERR output of the i486/487SX CPU.
IGNERR*	28	O	Ignore Error, active low. This line is a part of the AT compatible floating point error reporting scheme. It connects to the i486/487SX CPU.
IRQ13	27	O	Interrupt line 13. Connects to the HT321 ISA controller.
VCC	17,33,46,708 0,93,102, 115,127,1381 61,184		Power
GND	1,16,34,47, 69,81,92, 103,116,1281 39,162		Ground
NC	79-71,82		Ground

Pin Names in Alphabetical Order

AEN	164
BALE	75
BCLK	68
BS16*	45
CLAMPA20*/ROMWIDTH	84
DRQ*[3:0]	55-52
DRQ*[7:5]	58-56
DACK*[3:0]	62-59
DACK*[7:5]	65-63
EADS*	172
GND	1,24,47,70,92,104, 115,128,138,162,
HA[31:2]	38-25,22-10
HADS*	44
HBEN*[3:0]	43-40
HCLK	163
HD[15:0]	183-176,9-2
HDC	174
HHLDA	168
HLOCAL*	167
HMIO	175
HOLDREQ	48
HRDY*	39
HRDYI*	165
HREFRESH*	171
HRESCPU	170
HWR	173
INT	50
IOCHK*	159
IOCHRDY	144
IOCS16*	142
IOR*	66
IOW*	67
IRQ1	158
IRQ[15:3]	145-157
KBCS*	80
KB_CLMPA20*	166
LA[23:17]	112-106
LBHEN*	137
MASTER*	140
MEMCS16*	141
MEMR*	71
MEMW*	72
NMI	49
OSC	160
PARITY*	169
POR	82
RC	77
RESETDRV	76
RESETNPU	51
ROMEN	79
RTCCS*	81
SA[19:0]	136-129,126-117, 114-113
SD[15:0]	103-94,91-86
SMEMR*	73
SMEMW*	74
SPKR	78
TC	85
TESTIN	83
0WS*	143
VCC	23,46,69,93,105,116 127,139,161,184

Pin Names and Numbers in Numerical Order

001 GND	047 GND	093 VCC	139 VCC
002 HD7	048 HOLDREQ	094 SD6	140 MASTER*
003 HD6	049 NMI	095 SD7	141 MEMCS16*
004 HD5	050 INT	096 SD8	142 IOCS16*
005 HD4	051 RESETNPU	097 SD9	143 0WS*
006 HD3	052 DRQ0	098 SD10	144 IOCHRDY
007 HD2	053 DRQ1	099 SD11	145 IRQ15
008 HD1	054 DRQ2	100 SD12	146 IRQ14
009 HD0	055 DRQ3	101 SD13	147 IRQ13
010 HA2	056 DRQ5	102 SD14	148 IRQ12
011 HA3	057 DRQ6	103 SD15	149 IRQ11
012 HA4	058 DRQ7	104 GND	150 IRQ10
013 HA5	059 DACK0*	105 VCC	151 IRQ9
014 HA6	060 DACK1*	106 LA17	152 IRQ8*
015 HA7	061 DACK2*	107 LA18	153 IRQ7
016 HA8	062 DACK3*	108 LA19	154 IRQ6
017 HA9	063 DACK5*	109 LA20	155 IRQ5
018 HA10	064 DACK6*	110 LA21	156 IRQ4
019 HA11	065 DACK7*	111 LA22	157 IRQ3
020 HA12	066 IOR*	112 LA23	158 IRQ1
021 HA13	067 IOW*	113 SA0	159 IOCHK*
022 HA14	068 BCLK	114 SA1	160 OSC
023 VCC	069 VCC	115 GND	161 VCC
024 GND	070 GND	116 VCC	162 GND
025 HA15	071 MEMR*	117 SA2	163 HCLK
026 HA16	072 MEMW*	118 SA3	164 AEN
027 HA17	073 SMEMR*	119 SA4	165 HRDYI*
028 HA18	074 SMEMW*	120 SA5	166 KB_CLMPA20*
029 HA19	075 BALE	121 SA6	167 HLOCAL*
030 HA20	076 RESETDRV	122 SA7	168 HHLDA
031 HA21	077 RC	123 SA8	169 PARITY*
032 HA22	078 SPKR	124 SA9	170 HRESCPU
033 HA23	079 ROMEN	125 SA10	171 HREFRESH*
034 HA24	080 KBCS*	126 SA11	172 EADS*
035 HA25	081 RTCCS*	127 VCC	173 HWR
036 HA26	082 POR	128 GND	174 HDC
037 HA27	083 TESTIN	129 SA12	175 HMIO
038 HA31	084 CLAMPA20*	130 SA13	176 HD15
039 HRDY*	085 TC	131 SA14	177 HD14
040 HBEN3*	086 SD0	132 SA15	178 HD13
041 HBEN2*	087 SD1	133 SA16	179 HD12
042 HBEN1*	088 SD2	134 SA17	180 HD11
043 HBEN0*	089 SD3	135 SA18	181 HD10
044 HADS*	090 SD4	136 SA19	182 HD9
045 BS16*	091 SD5	137 LBHEN*	183 HD8
046 VCC	092 GND	138 GND	184 VCC

Pin Names in Alphabetical Order

AHOLD	158	HMIO	159
BANKSELEVN	83	HRDY*	157
BANKSELODD	84	HRDYI*	24
BLAST*	25	HREFRESH*	22
BOFF*	62	HRESCPU	49
BRDY*	37	HWR	160
CASEVN*[3:0]	110-107	IGNERR*	28
CASODD*[3:0]	106-104,101	IRQ13	27
FERR*	29	KEN*	61
GND	1,16,34,47,69,81,92 103,116,128,139,162	MA[11:1]	99-94,91-87
		MAEVN0	86
HA31,[27:2]	171,172-183,2-15	MAODD0	100
HADS*	36	MD[31:0]	156-140,137-129,126-121
HBEN*[3:0]	167-170	NC	79-71,82
HCLK	164	PARD[3:0]	120-117
HD[31:0]	67-63,59-50,48, 45-38,35,32-30,21-18	PARITY*	60
		POR	166
HDC	163	RAS*[3:0]	114-111
HHLDA	23	VCC	17,33,46,70,80,93, 102,115,127,138,161,184
HLOCALI*	26		
HLOCAL*	165	WEN	85
HLOCRDY*	68		

Pin Names in Numerical Order

001 GND	047 GND	093 VCC	139 GND
002 HA15	048 HD16	094 MA6	140 MD15
003 HA14	049 HRESCPU	095 MA7	141 MD16
004 HA13	050 HD17	096 MA8	142 MD17
005 HA12	051 HD18	097 MA9	143 MD18
006 HA11	052 HD19	098 MA10	144 MD19
007 HA10	053 HD20	099 MA11	145 MD20
008 HA9	054 HD21	100 MAODD0	146 MD21
009 HA8	055 HD22	101 CASODD0*	147 MD22
010 HA7	056 HD23	102 VCC	148 MD23
011 HA6	057 HD24	103 GND	149 MD24
012 HA5	058 HD25	104 CASODD1*	150 MD25
013 HA4	059 HD26	105 CASODD2*	151 MD26
014 HA3	060 PARITY*	106 CASODD3*	152 MD27
015 HA2	061 KEN*	107 CASEVN0*	153 MD28
016 GND	062 BOFF*	108 CASEVN1*	154 MD29
017 VCC	063 HD27	109 CASEVN2*	155 MD30
018 HD0	064 HD28	110 CASEVN3*	156 MD31
019 HD1	065 HD29	111 RAS0*	157 HRDY*
020 HD2	066 HD30	112 RAS1*	158 AHOLD
021 HD3	067 HD31	113 RAS2*	159 HMIO
022 HREFRESH*	068 HLOCRDY*	114 RAS3*	160 HWR
023 HHLDA	069 GND	115 VCC	161 VCC
024 HRDYI*	070 VCC	116 GND	162 GND
025 BLAST*	071 NC	117 PARD0	163 HDC
026 HLOCALIN*	072 NC	118 PARD1	164 HCLK
027 IRQ13	073 NC	119 PARD2	165 HLOCAL*
028 IGNERR*	074 NC	120 PARD3	166 POR
029 FERR*	075 NC	121 MD0	167 HBEN3*
030 HD4	076 NC	122 MD1	168 HBEN2*
031 HD5	077 NC	123 MD2	169 HBEN1*
032 HD6	078 NC	124 MD3	170 HBEN0*
033 VCC	079 NC	125 MD4	171 HA31
034 GND	080 VCC	126 MD5	172 HA27
035 HD7	081 GND	127 VCC	173 HA26
036 HADS*	082 NC	126 GND	174 HA25
037 BRDY*	083 BANKSELEVN	129 MD6	175 HA24
038 HD8	084 BANKSELODD	130 MD7	176 HA23
039 HD9	085 WEN	131 MD8	177 HA22
040 HD10	086 MAEVN0	132 MD9	178 HA21
041 HD11	087 MA1	133 MD10	179 HA20
042 HD12	088 MA2	134 MD11	180 HA19
043 HD13	089 MA3	135 MD12	181 HA18
044 HD14	090 MA4	136 MD13	182 HA17
045 HD15	091 MA5	137 MD14	183 HA16
046 VCC	092 GND	138 VCC	184 VCC

HTK340
Shasta 486 Chip Set

HT321 DC Specifications

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 TO +7	V
Input Voltage	VIN	-0.3 TO VDD + 0.3	V
DC Input Current	IIN	10	mA
Storage Temperature Range	TSTG	-40 to + 125	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Case Temperature Range	T_{CASE}	0 to + 85	°C

DC Characteristics: VDD = 5V ± 5%, T_{CASE} = 0°C to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL				0.8	V
Voltage Input High	VIH		2			V
Input Current	IIH		-10	1	10	uA
Voltage Output High	VOH					
HADS*,HD[15:0],HREFRESH*,LBHEN*,LA[23:17], SA[19:0],SD[15:0],BCLK,BALE,RESETDRV,MEMR*, MEMW*,SMEMR*,SMEMW*,IOW*,IOR*,AEN, DACK*[7:5, 3:0],TC,IOCHRDY		IOH = -8mA	2.4	4.5		V
HA[31,27:2],HBEN*[3:0],HRDY*,HMIO,HDC,HWR, EADS*,HRESCPU,BS16*,HOLDREQ,NMI,INT, RESET387,SPKR,ROMEN,KBCS*,RTCCS*, CLAMPA20*		IOH = -4mA	2.4	4.5		V
Voltage Output Low	VOL					
HADS*,HREFRESH*,LBHEN*,LA[23:17],SA[19:0], SD[15:0],BCLK,BALE,RESETDRV,MEMR*,MEMW*, SMEMR*,SMEMW*,IOW*,IOR,AEN,DACK*[7:5,], TC,IOCHRDY,HD[15:0]		IOL = 16mA		0.4	0.8	V
HA[31,27:2],HBEN*[3:0],HRDY*,HMIO,HDC,HWR, EADS*,HRESCPU,BS16*,HOLDREQ,NMI,INT, RESET387,SPKR,ROMEN,KBCS*,RTCCS*, CLAMPA20*		IOL = 8mA		0.4	0.8	V
Tri-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	1	10	uA
Output Short Circuit Current	IOS	VDD=Max, Vout=0V	20 -10	110 -90	220 -190	mA mA
Supply Current	IDD	CLK=33MHz CL=50pF VCC = 5.0V			85	mA

Note: Not more than one Output may be shorted at a time, for a maximum duration of ONE SECOND.

Figure 5.1 - HT321 DC Specifications

HT342 DC Specifications

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 TO +7	V
Input Voltage	VIN	-0.3 TO VDD +0.3	V
DC Input Current	IIN	10	mA
Storage Temperature Range (plastic)	TSTG	-40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Case Terperature Range	T_{CASE}	0 to +85	°C

DC Characteristics: VDD = 5V± 5%, T_{CASE} = 0°C to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL				0.8	V
Voltage Input High	VIH		2			V
Input Current	IIH		-10	1	10	uA
Voltage Output High	VOH					
RAS*[1:0],MA[1:11]		IOH = -8mA	2.4	4.5		V
HD[31:0], HRDY*		IOH = -6mA	2.4	4.5		V
HLOCAL*,PARITY*,RAS*[3:2],CASEVEN*[3:0], CASODD*[3:0],MAEVEN0,MAODD0,BANKSELEVN, BANKSELODD,WEN,PARD[3:0],MD[31:0], CHIPSEL*[3:0],IRQ13,HMIO,HDC,HWR,HADS,HA31, HA[27:2],HBEN*[3:0],IGNERR*,BRDY*,KEN,BOFF*, AHOLD		IOH = -4mA	2.4	4.5		V
Voltage Output Low	VOL					
RAS*[1:0],MA[1:11]		IOL = 8mA		0.4	0.8	V
HD[31:0], HRDY*		IOL = 6mA		0.4	0.8	V
HLOCAL*,PARITY*,RAS*[3:2],CASEVEN*[3:0], CASODD*[3:0],MAEVEN0,MAODD0,BANKSELEVN, BANKSELODD,WEN,PARD[3:0],MD[31:0], CHIPSEL*[3:0],IRQ13,HMIO,HDC,HWR,HADS,HA31, HA[27:2],HBEN*[3:0],IGNERR*,BRDY*,KEN,BOFF*, AHOLD		IOL = 4mA		0.4	0.8	V
Tri-State Output Leakage Current	IOZ	VOH=VSS or VDD	-19	1	10	uA
Output Short Circuit Current	IOS	VDD=Max, VO=VDD VDD=Max, VO=0V	20 -10	110 -90	220 -190	mA mA
Supply Current	IDD	CLK=33MHz CL=50pF VCC = 5.0V			210	mA

Note: Not more than one Output may be shorted at a time, for a maximum duration of ONE SECOND.

Figure 5.2 - HT342 DC Specifications

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Shasta 486 Chip Set

HT321 AC Characteristics

VCC= 5V ± 5%; T_{CASE} = 0°C to 85°C; C_L = 50pF unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Fig Ref	Notes
t1	BCLK to BALE Valid	1	5	nS	5.4	
t2	BCLK to BALE Invalid	1	5	nS	5.4	
t3	BCLK to COMMAND Active (16 Bit Memory)		10	nS	5.4	
t4	BCLK to COMMAND In-Active		10	nS	5.4	
t5	BCLK to COMMAND Active (8 Bit Memory)		10	nS	5.4	
t6	Write DATA to COMMAND Active 8 Bit Memory and I/O	24		nS	5.4	
t7	COMMAND negated to Write DATA Invalid	25/10*		nS	5.4	*For 8-Bit Memory Cycles
t8	SA[0:19],LBHEN Valid to BALE	28		nS	5.4	
t9	LA[17:23] Valid to BALE Invalid	116		nS	5.4	
t10	IOCHRDY Hold	5		nS	5.4	
t11	IOCHRDY Setup	5		nS	5.4	
t12	0WS* Setup	5		nS	5.4	
t13	0WS* Hold	5		nS	5.4	
t14	MEMCS16*,IOCS16*, Setup	5		nS	5.4	
t15	MEMCS16*,IOCS16*,	5		nS	5.4	
t16	IOCHK* to NMI Delay		15	nS		
t17	IRQ[2:15] to INT Delay		15	nS		
t18	AEN Active/Inactive Delay (from CPUHLDA)		15	nS	5.5	
t19	BALE Active/Inactive Delay (from CPUHLDA & HCLK2)		12	nS	5.5	
t20	CPUHLDA Setup	7		nS	5.5	
t21	CPUHLDA Hold	5		nS	5.5	
t22	CPUHRQ Active/Inactive Delay		15	nS	5.5	
t23	DACKx Active/Inactive Delay		15	nS	5.5	
t24	DRQx Setup	10		nS	5.5	
t25	DRQx Hold	5		nS	5.5	
t26	AEN Delay from MASTER*		12	nS	5.5	
t27	IOR* Active/Inactive Delay		10	nS	5.5	
t28	IOW* Active/Inactive Delay		10	nS	5.5	
t29	MEMR* Active/Inactive Delay		10	nS	5.5	
t30	MEMW* Active/Inactive Delay		10	nS	5.5	
t31	MA[1:11], SA[0:19] Address Valid Delay in MASTER* Mode			nS	5.5	
t32	SBHE* Active/Inactive Delay		12	nS	5.5	
t33	TC Active/Inactive Delay		12	nS	5.5	
t34	TC Active Pulse Width	700		nS	5.5	

Figure 5.3 - ISA Interface

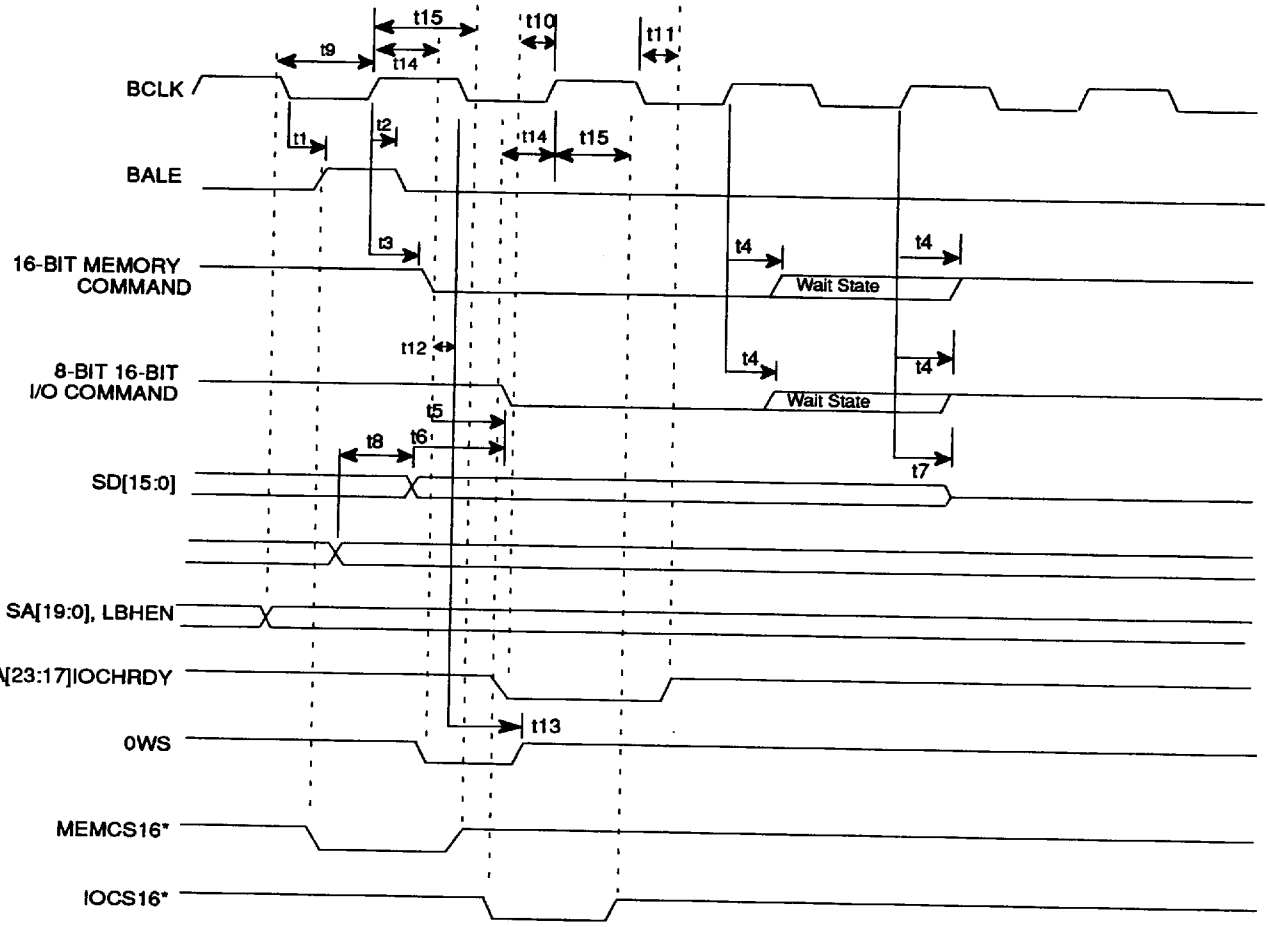


Figure 5.4 ISA Backplane Interface

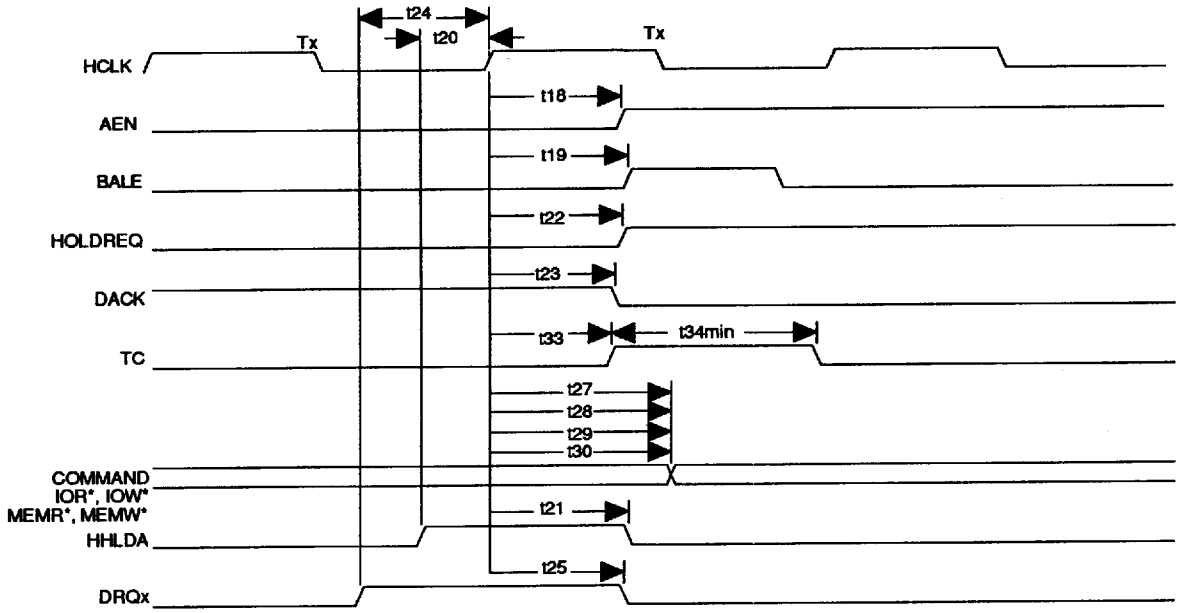
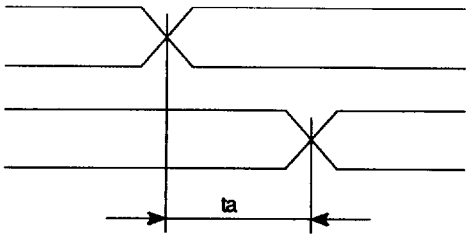


Figure 5.5 - SETUP and HOLD Timings I/O Interface, DMA Signals

HT321 AC Characteristics

Symbol	Parameter	Min	Max	Unit	Fig Ref	Notes
t100	HCLK Fequency	0	33	MHz	5.8	Duty Cycle 50% ± 5%
t101	HCLK Period	30		ns	5.8	
t102	HCLK Period Stability		0.1%	Δ		Adjacent Clocks
t103	HA[31,27:2],HADS*,HRDY*,BS16*,HBEN[3:0], REFRESH*,EADS*,HMIO,HDC,HWR Valid Delay		13	ns	5.9	
t104	HRESCPU Valid Delay		7	ns	5.9	
t105	HOLDREQ,BCLK Valid Delay		10	ns	5.9	
t106	HADS*,HRDYI*,HBEN[3:0],HMIO,HDC,HWR HHLDA,MASTER*,HLOCAL*,POR,HA[31,27:2] HD[15:0], (for Writes) Setup	6		ns	5.10	
t107	HADS*,HRDYI*,HBEN[3:0],HMIO,HDC,HWR HHLDA,MASTER*,HLOCAL*,POR,HA[31,27:2] HD[15:0], (for Writes) Hold	4		ns	5.10	
t108	SD to HD for CPU Reads Delay		13	ns	5.7	
t109	PARITY* to NMI Delay		15	ns	5.7	NMI Mask is OFF
t110	KB_CLAMPA20* to CLAMPA20* Delay		14	ns	5.7	

Figure 5.6 SHASTA Interface



ta = t108, t109, t110, t223, t226, t237

Note 5: The parameters applied only when BOFF is activated.

Note 6: The parameter is non-critical. Preserving the setup and hold time specifications assures the signal recognition within the specified HCLK period.

Figure 5.7 - Asynchronous Delays

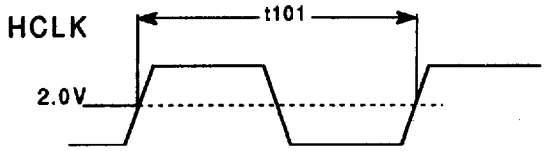


Figure 5.8 - HCLK

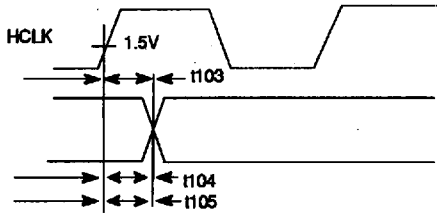


Figure 5.9 - Output Waveforms

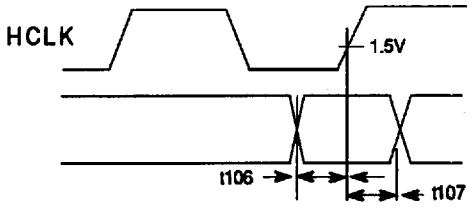


Figure 5.10 - Input Waveforms

HT342 AC Characteristics

VCC = 5V ± 5%; T_{CASE} = 0°C to 85°C; C_L = 50 pF unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Fig. Ref.	Notes
t200	HCLK Frequency		33.33	MHz	5.8	Duty Cycle 50% ± 5%
t201	HCLK Period	30		ns	5.8	
t202	HCLK Period Stability		0.1%	Δ		Adjacent Clocks
t203	HRESCPU Setup	16		ns	5.13	
t204	HRESCPU Hold	2		ns	5.13	
t205	HADS Setup	6		ns	5.13	
t206	HADS Hold	3		ns	5.13	
t207	HA[27:2], HA31 Setup	13		ns	5.13	
t208	HA[27:2], HA31 Hold	3		ns	5.13	
t209	HMIO, HDC, HWR Setup	12		ns	5.13	
t210	HMIO, HDC, HWR Hold	3		ns	5.13	
t211	HBEN*[3:0] Setup	11		ns	5.13	
t212	HBEN*[3:0] Hold	3		ns	5.13	
t213	FERR* Setup	6		ns	5.13	
t214	FERR* Hold	3		ns	5.13	
t215	HHLDA Setup	13		ns	5.13	
t216	HHLDA Hold	3		ns	5.13	
t217	BLAST* Setup	10		ns	5.13	
t218	BLAST* Hold	2		ns	5.13	
t219	HRDYI* Setup	12		ns	5.13	
t220	HRDYI* Hold	3		ns	5.13	
t221	HLOCALIN* Setup	3		ns	5.13	
t222	HLOCALIN* Hold	3		ns	5.13	
t223	HLOCALIN* -> HLOCAL* Asynchronous Delay	3	9	ns	5.7	
t224	HLOCRDY* Setup	3		ns	5.13	
t225	HLOCRDY* Hold	3		ns	5.13	
t226	HLOCRDY* -> HRDY* Asynchronous Delay	3	10	ns	5.7	
t227	POR Setup	4		ns	5.13	
t228	POR Hold	3		ns	5.13	
t229	HREFRESH* Setup	4		ns	5.13	
t230	HREFRESH* Hold	3		ns	5.13	
t231	HD[31:0] Write Setup	11		ns	5.13	
t232	HD[31:0] Write Hold	3		ns	5.13	
t233	HD[31:0] Read Delay	3	14	ns	5.12	Pipeline on
t234	HD[31:0] Read Float Delay	3	15	ns	5.12	Pipeline on
t235	MD[31:0], PARD[3:0] Read Setup	0		ns	5.13	Pipeline on
t236	MD[31:0], PARD[3:0] Read Hold	4		ns	5.13	Pipeline on
t237	MD[31:0], HD[31:0] Asynchronous Delay	4	16	ns	5.7	Pipeline off
t238	MD[31:0], PARD[3:0] Write Valid Delay	3	20	ns	5.12	
t239	MD[31:0], PARD[3:0] Write Float Delay	3	15	ns	5.12	

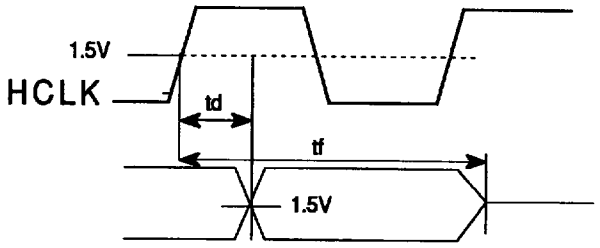
Figure 5.11 - HT342 AC Characteristics

HT342 AC Characteristics

VCC = 5V ± 5%; T_{CASE} = 0°C to 85°C; C_L = 50 pF unless otherwise specified

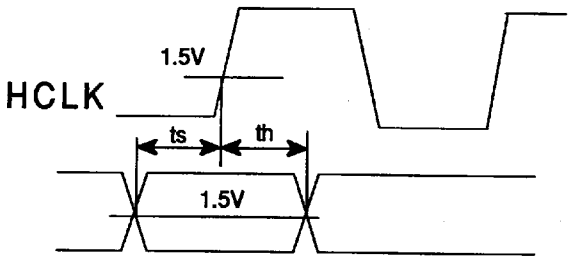
Symbol	Parameter	Min	Max	Unit	Fig. Ref.	Notes
t240	HRDY* Valid Delay	3	17	ns	5.12	
t241	BRDY* Valid Delay	3	14	ns	5.12	
t242	HLOCAL* Valid Delay	3	14	ns	5.12	
t243	PARITY* Valid Delay	3	12	ns	5.12	
t244	HRDY*, BRDY*, HLOCAL*, PARITY Float Delay	3	15	ns	5.12	
t245	KEN Valid Delay	3	14	ns	5.12	
t246	KEN Float Delay	3	15	ns	5.12	
t247	RAS*[3:0] Delay	3	12	ns	5.12	20 pF Load
t248	RAS*[3:0] Delay	3	14	ns	5.12	85 pF Load
t249	CASEVN*[3:0], CASODD*[3:0] Delay from rising edge	3	14	ns	5.12	20 pF Load
t250	CASEVN*[3:0], CASODD*[3:0] Delay from rising edge	3	21	ns	5.12	85 pF Load
t251	CASEVN*[3:0], CASODD*[3:0] Delay from falling edge	3	14	ns	5.12	20 pF Load
t252	CASEVN*[3:0], CASODD*[3:0] Delay from falling edge	3	21	ns	5.12	85 pF Load
t253	WEN* Delay	3	12	ns	5.12	20 pF Load
t254	WEN* Delay	3	17	ns	5.12	85 pF Load
t255	BANKSELEVN, BANKSELODD Valid Delay	3	15	ns	5.12	
t256	MA[11:1], MAEVN0, MAODD0 Row Address Valid Delay	3	20	ns	5.12	20 pF Load
t257	MA[11:1], MAEVN0, MAODD0 Row Address Valid Delay	3	26	ns	5.12	85 pF Load
t258	MA[11:1], MAEVN0, MAODD0 Column Address Valid Delay	3	15	ns	5.12	20 pF Load
t259	MA[11:1], MAEVN0, MAODD0 Column Address Valid Delay	3	20	ns	5.12	85 pF Load
t260	IRQ13 Delay	3	13	ns	5.12	
t261	IGNNE Delay	3	14	ns	5.12	
t262	AHOLD Delay	3	10	ns	5.12	BOFF Cycles
t263	BOFF Delay	3	15	ns	5.12	BOFF Cycles
t264	HA[27:2], HA31, HMIO, HWR, HDC, HBEN[3:0], HHLDA, BLAST* Valid Delay	3	16	ns	5.12	BOFF Cycles
t265	BOFF, HA[27:2], HA31, HMIO, HWR, HDC, HBEN[3:0], HHLDA, BLAST* Float Delay	3	16	ns	5.12	BOFF Cycles
t266	HADS* Delay	3	16	ns	5.12	BOFF Cycles
t267	HD[31:0] Write Data Valid Delay	3	18	ns	5.12	BOFF Cycles
t268	HD[31:0] Write Data Float Delay	3	19	ns	5.12	BOFF Cycles

Figure 5.11 - HT342 AC Characteristics (Continued)



td = t233, t238, t240, t241, t242, t243, t245, t247, t248-t263, t264, t266, t267
tf = t234, t239, t244, t246, t265, t268
Note 1: The parameters are relative to the rising edge of the HCLK signal.

Figure 5.12

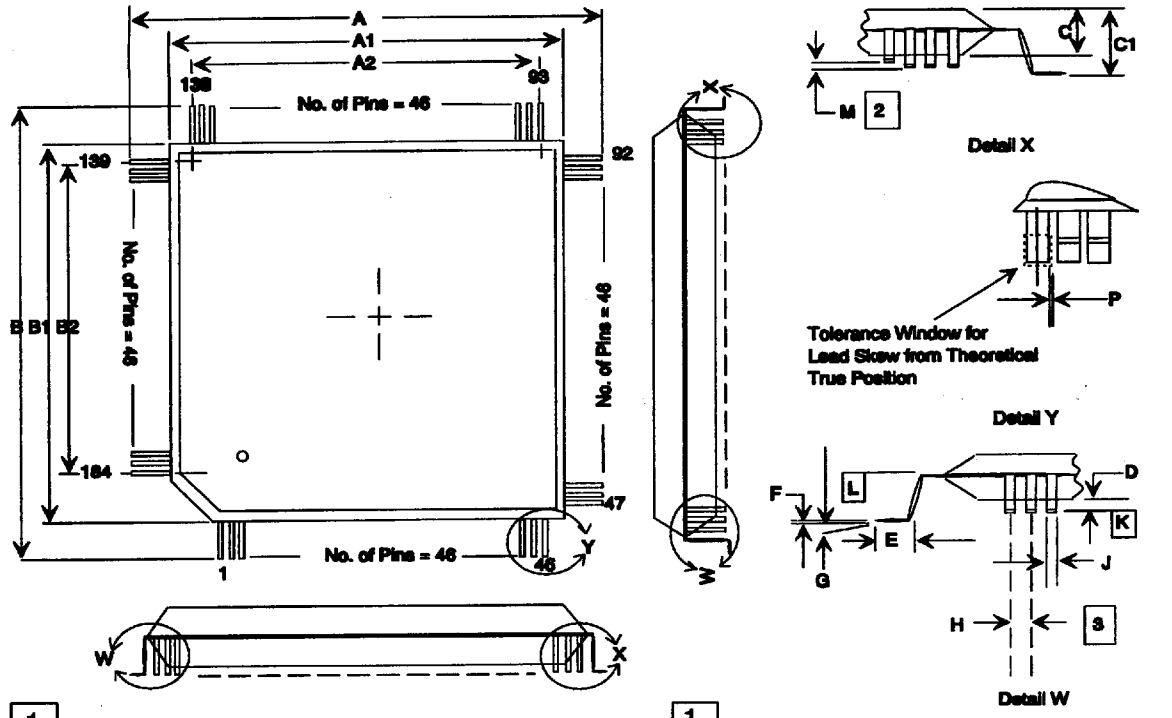


ts = t203, t205, t207, t209, t211, t213, t215, t217, t221, t224, t227, t235
th = t204, t206, t208, t210, t212, t214, t216, t218, t222, t225, t228, t230, t236
Note 2: HD[31:0] Read Delay is an asynchronous delay from the MD[31:0] bus.
Note 3: The parameters are relative to the falling edge of the HCLK signal.
Note 4: The parameters are relative to the rising or falling edge of the HCLK signal dependant upon the timing shown.

Figure 5.13

HTK340
Shasta 486 Chip Set

Package Outline



1

Dimensions in mm		
Sym	Minimum	Maximum
A	30.30	30.90
A1	27.90	28.10
A2	22.50 Ref.	
B	30.30	30.90
B1	27.90	28.10
B2	22.50 Ref.	
C	3.68	4.01
C1	3.43	3.66
D	0.25	0.36
E	0.30	0.70
F	0.10	0.25
G	0°	10°
H	0.40	0.60
J	0.15	0.25
M	0.10 Max	
P	0.05 Max	
No. of Pins	184	

1

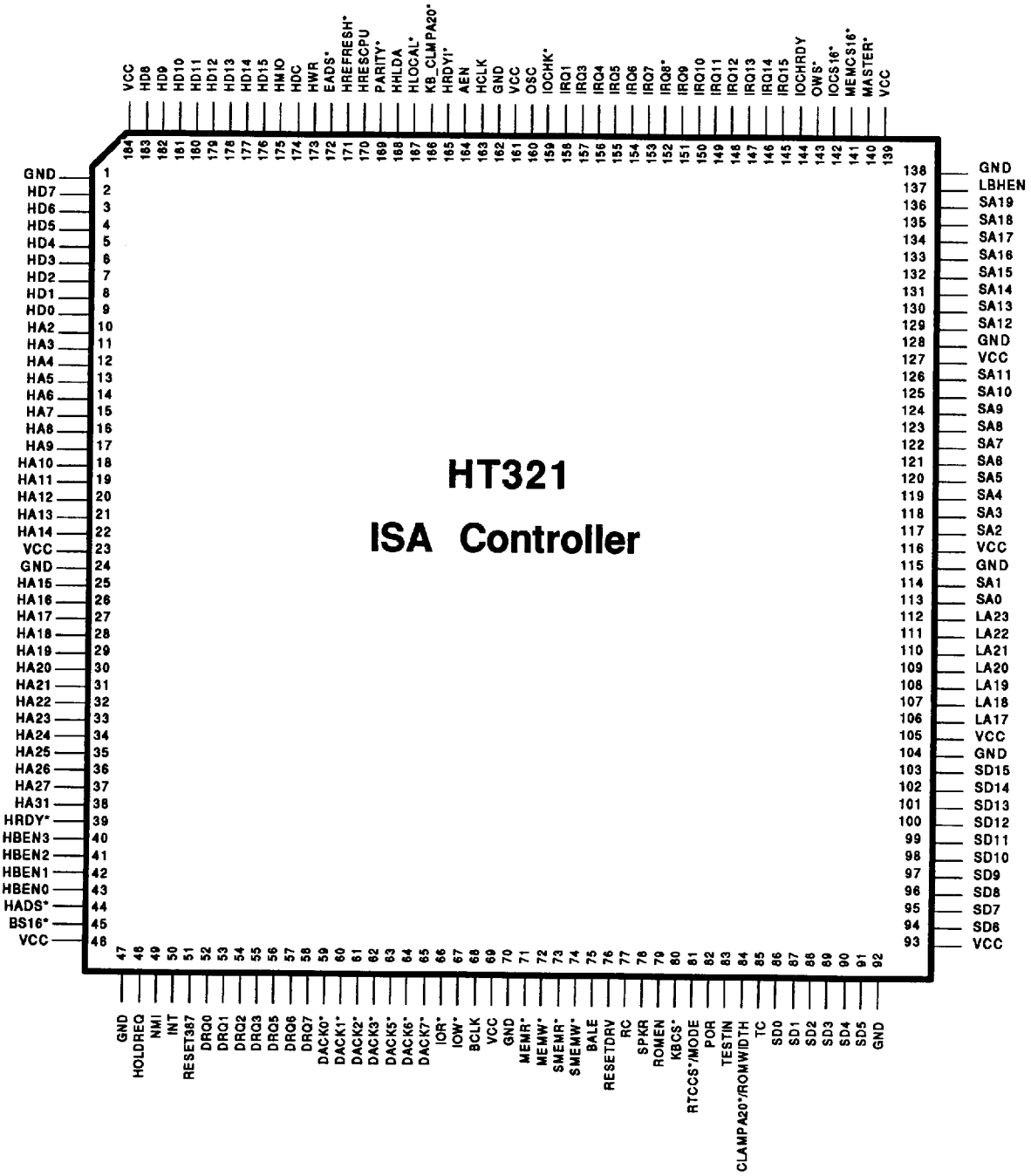
Dimensions in Inches		
Sym	Minimum	Maximum
A	1.193	1.216
A1	1.098	1.106
A2	0.886 Ref	
B	1.193	1.216
B1	1.098	1.106
B2	0.886 Ref	
C	0.145	0.158
C1	0.135	0.144
D	0.010	0.014
E	.012	.028
F	0.004	0.010
G	0°	10°
H	0.016	0.024
J	0.006	0.010
M	0.004 Max.	
P	0.002 Max.	
No. of Pins	184	

NOTES: Unless otherwise specified

2 Nominal dimensions in millimeters. Inches rounded to the nearest .001 inch. Controlling dimension in mmillmeters.

3 Coplanarity of all leads shall be within 0.1 MM (0.004") (Difference between highest and lowest lead with seating plane K as reference)

HT321 Pin Package



HTK340
Shasta 486 Chip Set