HT44
486 Cache Controller

T-52-33-21

General Features

- Support for 486SX/DX/DX2 CPUs
- System implementation with Headland's HTK340 chip set and future 486 chip sets
- 16, 20, 25 and 33 MHz CPU speeds

Memory Configurations

- 32KB, 64KB, 128KB, 256KB, 512KB & 1MB cache sizes
- 25ns SRAMs required at 33 MHz
- Asynchronous and synchronous SRAMs are supported
- Programmable write-protected and non-cacheable regions are supported through the chip set

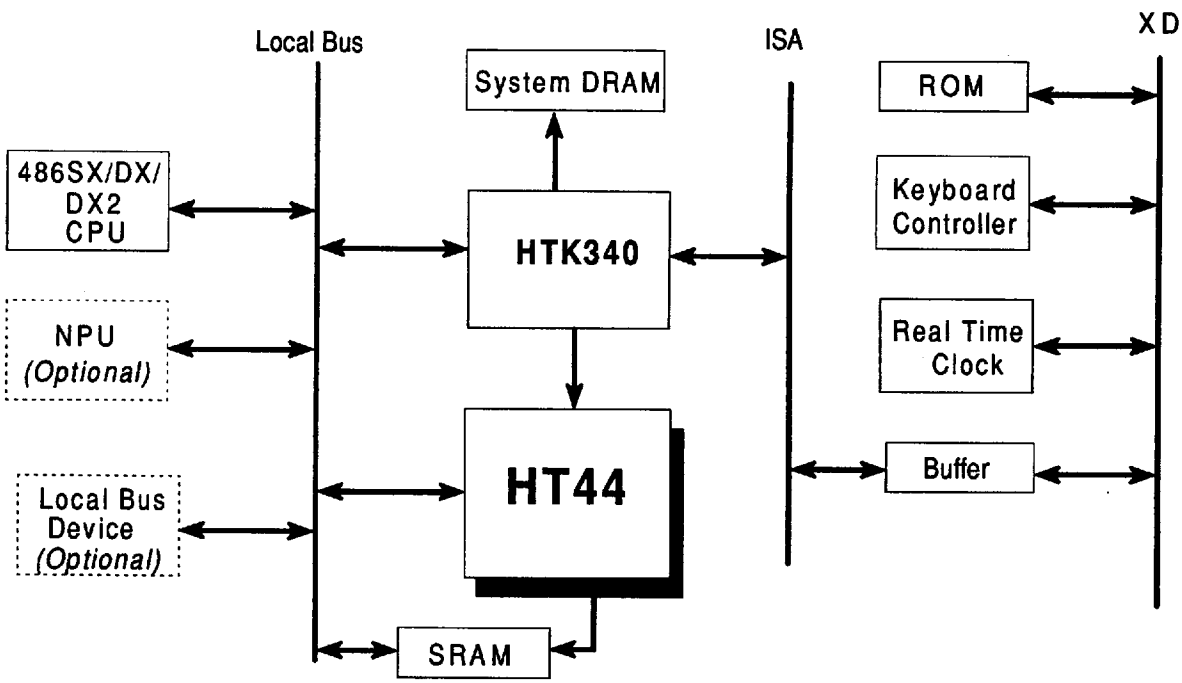
Architecture

- Look-Aside
- Write through
- Direct mapped
- Integrated tag comparator
- Zero wait state cache hits
- Simultaneous 486 and secondary cache update on read miss
- 486 line burst cycle support

Package & Die

- 84-pin PLCC
- LSI Logic's 0.7 micron HCMOS process

HT44 System Block Diagram



HT44
486 Cache Controller

Description

The HT44 is a look-aside write-through, 80486SX™, 486DX™ or 486DX2™ secondary cache controller. It is packaged in an inexpensive 84-pin plastic-leaded chip carrier (PLCC).

Architecture

With its look-aside architecture, the HT44 fits beside the CPU-to-Memory bus and not in the data path. Therefore, once the HT44 has been designed into a 486 system, it can be populated for secondary cache systems or left vacant for non-secondary cache systems. The HT44 is direct- mapped to the available address space.

Performance

The HT44 has a number of performance enhancing features. These include zero-wait-state burst line fills to the 486 on secondary cache hits, and simultaneous 486 and secondary cache updates on read misses.

Memory Configurations

The HT44 supports cache sizes from 32KBytes to 1MB. Both synchronous and asynchronous SRAMs are supported. 25ns SRAMs are sufficient for zero-wait-state operation at 33MHz.

Chip Set Support

The HT44 can be implemented with minimal glue logic in a 486 system with the HTK340 (code name Shasta) chip set. The registers in the HTK340 allow for programming of non-cacheable and write-protected areas of memory. The HTK340 will support the HT44 with *synchronous* SRAMs only. Future Headland chip sets will support both synchronous and asynchronous SRAM designs.

The HT44 can also be used with some third-party chip sets, however, additional glue logic may be required.

Functional Description

1.0 Overview

The HT44 is a write-through, direct-mapped, look-aside, secondary cache controller designed for use in 486 systems using the Headland family of 486 chips. The cache controller's organization matches that of the 486 internal cache. The cache update policy is read miss and write hit only. The controller updates the cache during 486 line fill cycles and is almost transparent to the system. No write cycles are altered because of the presence of the cache, however in certain modes, secondary cache read miss cycles have a wait state added. Read hit cycles are always 2-1-1-1 which means zero-wait-state bursts. Write miss cycles do not have any penalty, while write hit cycles could have a 0 or 1 wait state secondary cache write rate.

The HT44 uses an external TAG RAM architecture, suppling a TAG RAM interface with on-chip comparators. Industry standard asynchronous RAMs can be used to build the TAG RAM array. The comparator is 13 bits wide, including a VALID bit used for handling read miss cycles, flushing the cache, and power-up.

The cache controller is a perfect solution for upgradeable systems. The upgradeable cache subsystem can be built as a part of the main board with sockets provided for the HT44, TAG and data SRAMs or as a daughter card to be plugged into the motherboard.

The chip has four configuration pins dedicated to selecting the mode of operation. These are: CLK2X1, SYNC*, SHASTA and CSMODE. These pins affect the timing and behavior of the chip and are described in detail in the Internal Architecture and Theory of Operation sections of this document.

2.0 Internal Architecture

Figure 1 illustrates the internal block diagram of the HT44 cache controller. The major blocks are CLOCK SYNC & GEN, CHIP ENABLER, KEN* HANDLER, HADS*/-SADS* HANDLER, COMPARATORS & TAG GENERATION and CACHE CONTROL.

The CLOCK SYNC & GEN module supplies clocks and resets to the rest of the internal circuits. The input controlling this module is CLK2X1. If high, the module assumes the input clock to be twice that of the system frequency and uses the HRESCPU input to determine the phase information. Figure 2 illustrates the phase determination timing.

The CHIP ENABLER module enables the entire operation of the chip. The TAG RAM used for the cache implementation can be built of widely available asynchronous RAMs. These RAMs do not have an asynchronous reset. In order to flush the TAG (invalidate all VALID bits) one has to activate the FLUSH* input of the HT44 and go through a software procedure of sweeping all line addresses with read cycles.

During the power up and boot sequence, there is always a possibility of having an address match between the TAG RAM and the boot vector or some BIOS code. The CHIP ENABLER module takes care of this problem by making sure the HT44 controller powers up disabled (in a flushed mode). This is done

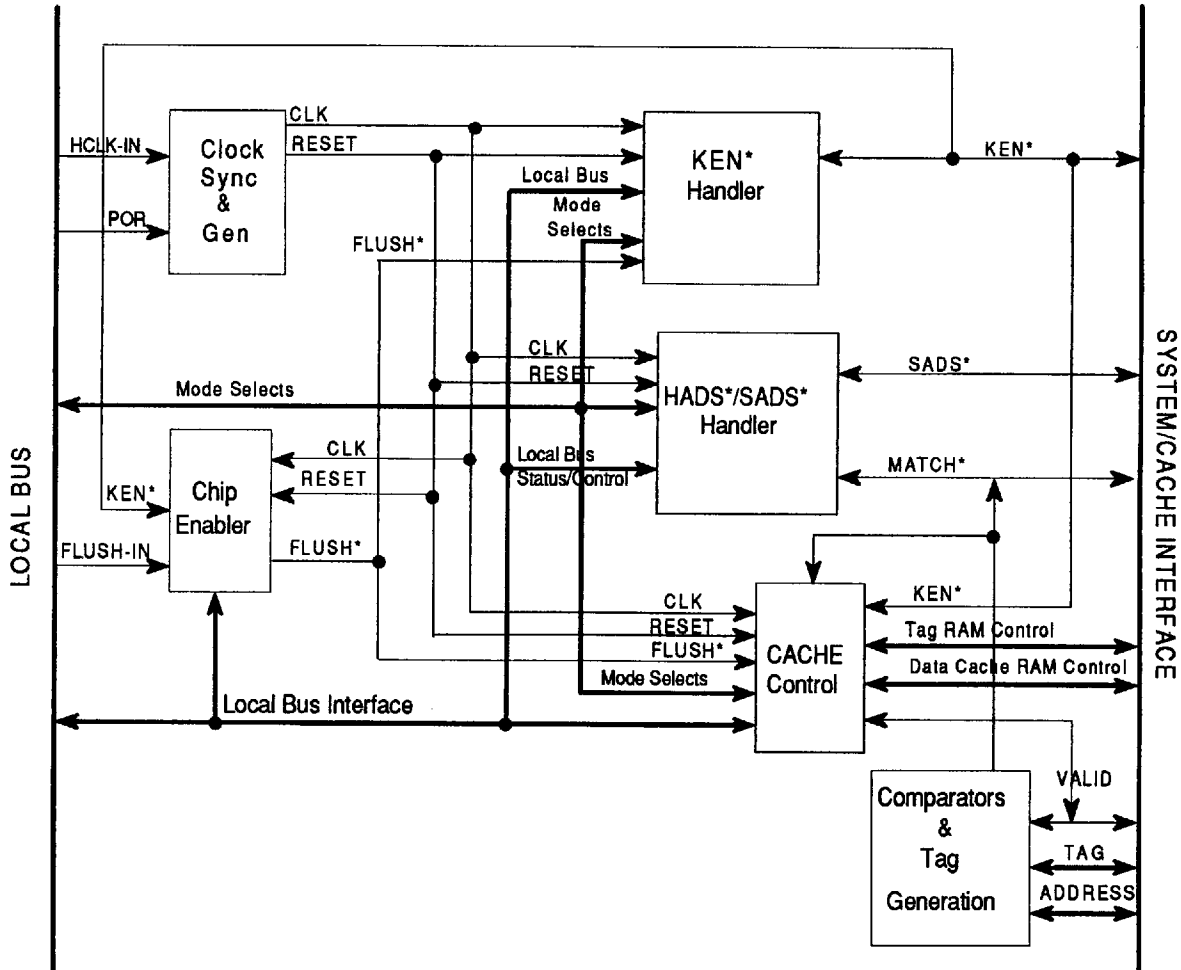


Figure 1 - HT44 Internal Block Diagram

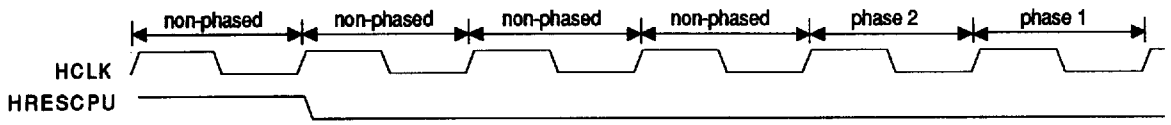


Figure 2 - Phase Determination (CLK2X1 =1)

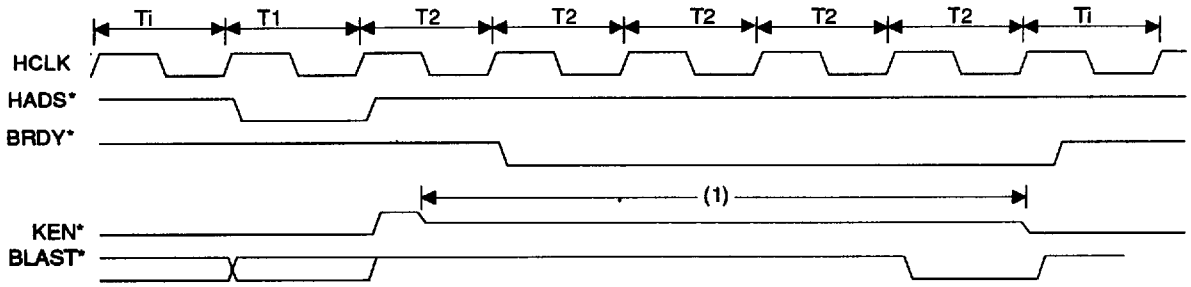


Figure 3a - KEN* timing for cacheable read miss cycle.

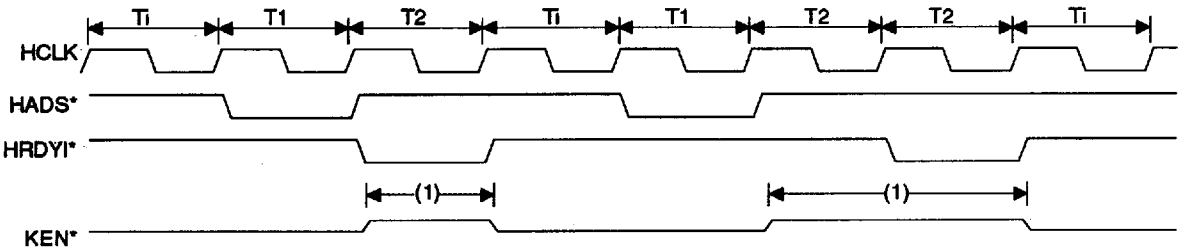


Figure 3b - KEN* timing for memory write cycles.

by the CHIP ENABLER module which forces an internal FLUSH line active on power-up. While in this state, any non-cacheable read cycle flushes the TAG entry associated with the address being read by invalidating the VALID bit. The first cacheable read cycle gets the HT44 out of the flush mode and enables its operation. Having seen the first cacheable read cycle, the CHIP ENABLER module deactivates the previously forced active internal FLUSH line. From then on, the internal FLUSH line is affected by the FLUSH* input pin only.

The KEN* handler module takes care of the KEN* generation. The module is activated only when the SHASTA pin is strapped high. In the SHASTA mode, the KEN* pin becomes an I/O pin. It is driven active at all times except for T2 states during memory write cycles, read miss cycles and DMA memory cycles. During these states, the signal is tri-stated. The purpose of activating the signal is to make sure that the read hit cycles (hits in the secondary cache) will be bursted by the CPU. Figures 3a, 3b and 3c show the timing for the KEN* signal in the SHASTA mode in all three cases when it is not driven.

The COMPARATORS & TAG GENERATION module compares the TAG[11:0] with the ADDRESS[11:0] bus and qualifies the comparison result with the VALID bit. The result of this operation is a signal called MATCH*, which is used internally for hit/miss determination and is also sent out on the MATCH* output. During cacheable read miss cycles, when the cache is updated, the TAG[11:0] bus is driven by the HT44 with ADDRESS[11:0] values.

The HADS*/SADS* HANDLER module is the main CPU/Local Bus control module. Its operation is affected primarily by the SHASTA strap.

In the SHASTA mode HADS* is connected to the CPU ADS* signal and synchronous cache data SRAMs (if they need the signal). The SADS* signal connects to the rest of the system. During CPU memory write cycles (Figure 4a), HADS* is an input that is passed asynchronously to the SADS* output. During cache read hits in the secondary cache, the

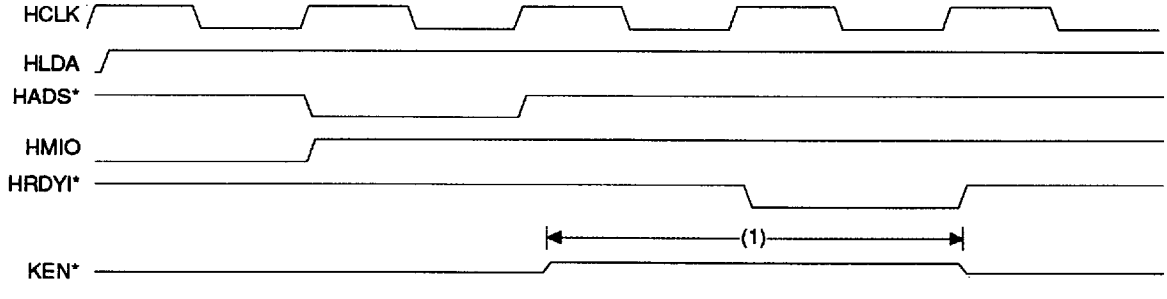


Figure 3c - KEN* timing for DMA cycle

Note (1): Not Driven by HT44

SADS* does not get generated; in other words, the cycle does not propagate to the Local Bus. All other CPU cycles have a wait state added such that SADS* follows HADS* by one state (1 or 2 HCLKs depending on the CLK2X1 option) - see Figure 4b. During DMA cycles (HLDA pin active), HADS* becomes an output and SADS* is an input. The HADS* follows SADS* asynchronously (Figure 4c).

In the non-SHASTA mode, SADS* is always an output. During CPU cycles this signal is generated one wait state after HADS* if the KEN* signal is deasserted (see Figure 5a). Otherwise, if KEN* is asserted, no SADS* appears. Figure 5b illustrates DMA cycles where SADS* always follows HADS*, asynchronously.

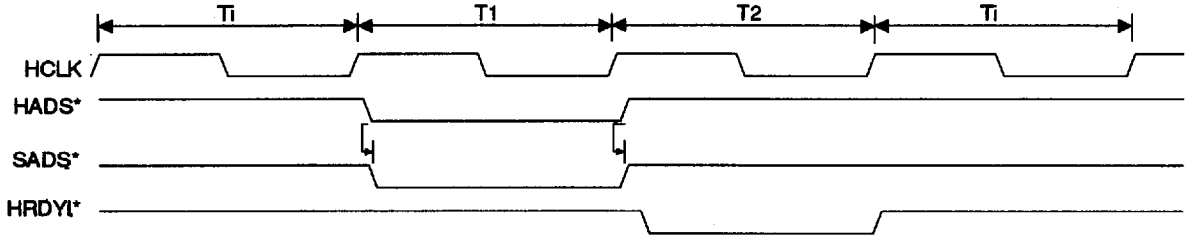


Figure 4a - HADS*/SADS* during CPU memory write (Shasta mode)

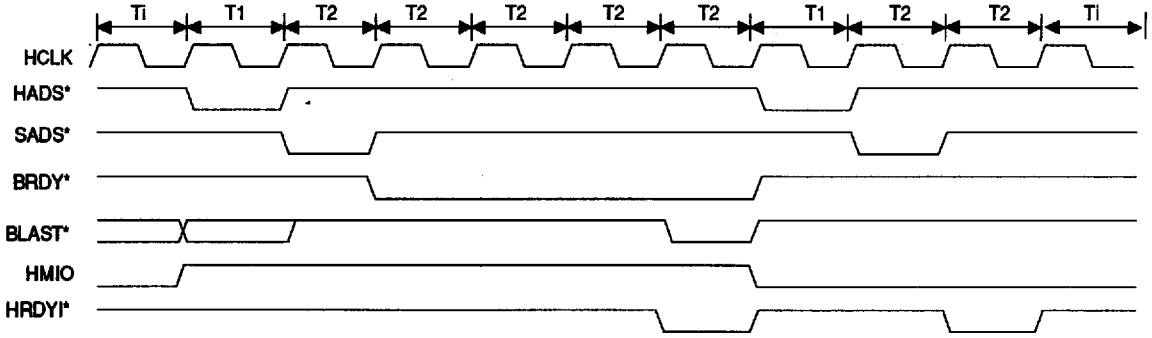


Figure 4b - HADS*/SADS* during cacheable read miss and I/O cycles (Shasta mode)

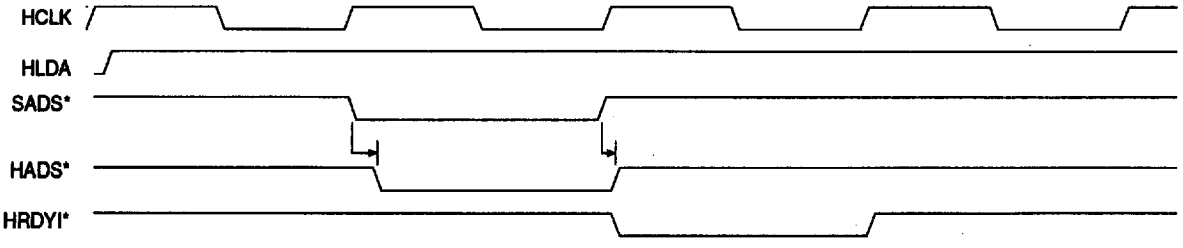


Figure 4c - HADS*/SADS* during DMA cycle (Shasta mode)

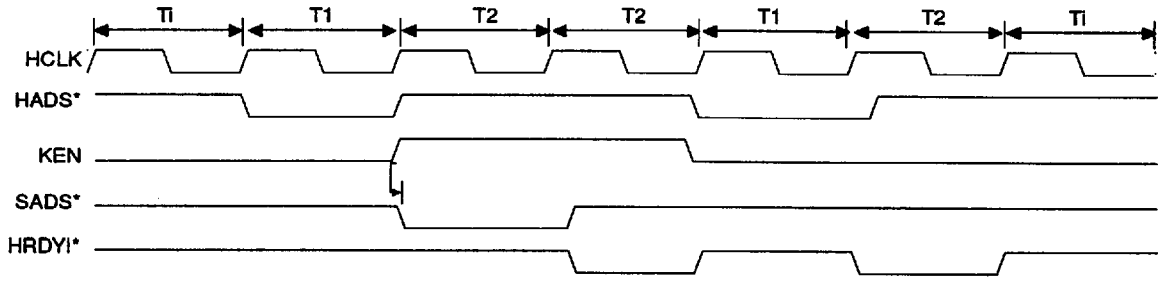


Figure 5a - SADS* generation during CPU cycles (Non-Shasta mode)

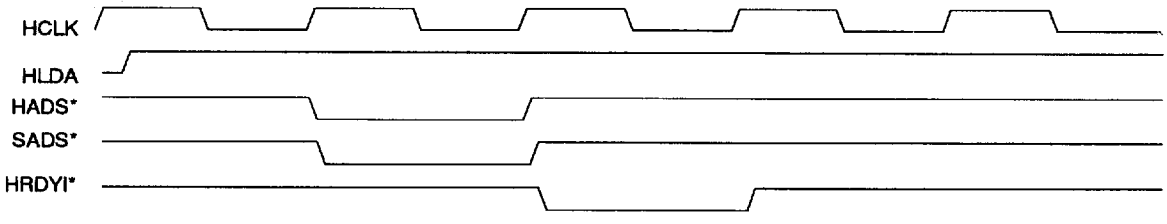


Figure 5b - SADS* generation during DMA cycle (Non-Shasta mode)

The CACHE CONTROL module shown in Figure 1 is the main state machine controlling DATA RAM and TAG RAM operation. This module generates all data and TAG RAM interface signals as well as terminating cycles during cache read hits by sending BRDY* and HRDY* signals.

3.0 Theory of operation

The HT44 is a secondary level cache controller. Its main purpose is to provide a cache and a system interface such that cache read hit cycles can occur in a bursted zero-wait-state fashion. The cache operation can be defined as write-through. In this respect, one of the major goals is to limit the cache's effect on write cycles; in other words, write cycles should not be slowed down by the presence of the cache. The cache updates its contents during cacheable read miss cycles. This operation occurs simultaneously with the 486 CPU's cache line fill cycle. Only complete burst line fills can be cached by the HT44. If the burst cycle filling the line in the primary and secondary cache is interrupted (by means of asserting an HRDY* or a BLAST* with BRDY* signal before the last dword of the line is fetched), the line fill cycle will not be completed, and the cache entry will not be validated.

The HT44 does not have cacheability mapping registers. The controller relies entirely on the KEN* input to determine whether a cycle should be cached or not.

The major option affecting the cache theory of operation is the SHASTA option. This is detailed below.

3.1 Cacheability in non-SHASTA Mode

When the SHASTA option is disabled (strapped low), the KEN* signal is used to qualify all cache cycles: cache hits and misses. In this case, the KEN* signal is not only the indication of the cacheability mode information, but is also a chip select for the cache during hit cycles. In the non-SHASTA mode MATCH* indicates the comparison result and KEN* is used to derive the hit/miss information. If KEN* is not active during the first T2 state following assertion of the HADS* starting a cycle, the cycle is assumed to be non-cacheable; both the MATCH* signal and cycle are ignored. If KEN* is asserted during the first T2 state, the cycle is assumed to be cacheable and the MATCH* signal determines if it is a hit or a miss. In this option, the KEN* signal is not sampled after the first KEN* sample. The only factor determining whether a miss cycle will complete is the ability of the system to burst the cycle and complete it. If the CPU, for any reason, interrupts the burst cycle before filling out the line completely, the cache will not be updated.

3.2 Cacheability in SHASTA Mode

When the SHASTA pin is strapped high, the theory of operation is quite different. The MATCH* signal is the only qualifier for the cycle to be qualified as a cache hit. The KEN* signal is driven during idle, T1 and the first T2 state. The KEN* signal is examined by the HT44 only during cache read misses in order to fill out a cache line. KEN* has to be present during the entire T2 state, starting from its second clock, so that the cache will be filled properly.

3.3 TAG RAM in SHASTA vs. non-SHASTA Mode

A very important implication of the difference between SHASTA and non-SHASTA mode of operation is the TAG entry size. In the non-SHASTA mode, the TAG has to contain all address bits that are not part of the data SRAM addresses up to the top of the DRAM memory. Since KEN* acts as a chip select for the HT44 controller, the cycles for which KEN* is negated will not be responded to by the HT44. In the SHASTA mode, having a MATCH* between the TAG entry and ADDRESS[11:0] is enough to qualify a hit cycle in the secondary cache. Therefore, the TAG RAM has to contain all address bits for which the system can generate cycles, including the non-DRAM high addresses. A good example is the Weitek coprocessor addresses (C000000H), which has HA31 and HA30 set. HA31 must become a part of the TAG entry, otherwise there will be an alias between the Weitek space and the DRAM space. It is assumed that in the non-SHASTA mode the KEN* signal will not be asserted during Weitek cycles, so that caching cannot occur for this space.

3.4 Cache line fills

An important feature of the HT44 cache operation is the ability to fill/update its contents simultaneously with the 486 CPU. This occurs during cacheable read miss cycles. Figure 6 shows how TAG entries are updated during these cycles. The TAG entry is invalidated during the first burst cycle by clearing the VALID bit for the entry, and then when the cycle finishes, the TAG entry is validated by setting the VALID bit. A cacheable read miss cycle is one of two cases in which the TAG is written. The other case is the flush operation. In SHASTA mode, KEN* qualifies the TAG_WE* signal during read miss cycles. In this way, non-cacheable cycles will not corrupt the valid cache entries. This implies restrictions on the KEN* signal supplied by the system such that KEN* should be valid throughout the entire miss cycle.

3.5 DMA operation

In SHASTA mode, the system is connected to SADS* and the CPU and the synchronous data RAM (if installed) to HADS*. During DMA, SADS* gets tri-stated, becomes an input, and is passed to HADS* asynchronously. In the non-SHASTA mode, SADS* is always driven and HADS* is always passed to SADS* regardless of the CPU/DMA mode of operation. In DMA mode, HADS* is always passed to SADS* asynchronously.

DMA cycles are never cacheable. The HT44 doesn't respond to read hit cycles and does not update the cache during DMA read miss cycles. During DMA cache write hit cycles, the cache is updated in order to maintain memory coherency. In both SHASTA and non-SHASTA modes, the data is expected in the proper byte locations during write hit cycles as detailed by the HBEN[3:0] signals.

3.6 Cycle termination

The only cycles terminated by the HT44 cache controller are secondary cache read hit cycles. The BRDY* signal is used to terminate these cycles. HRDY* is also generated by the HT44 during the last burst cycle.

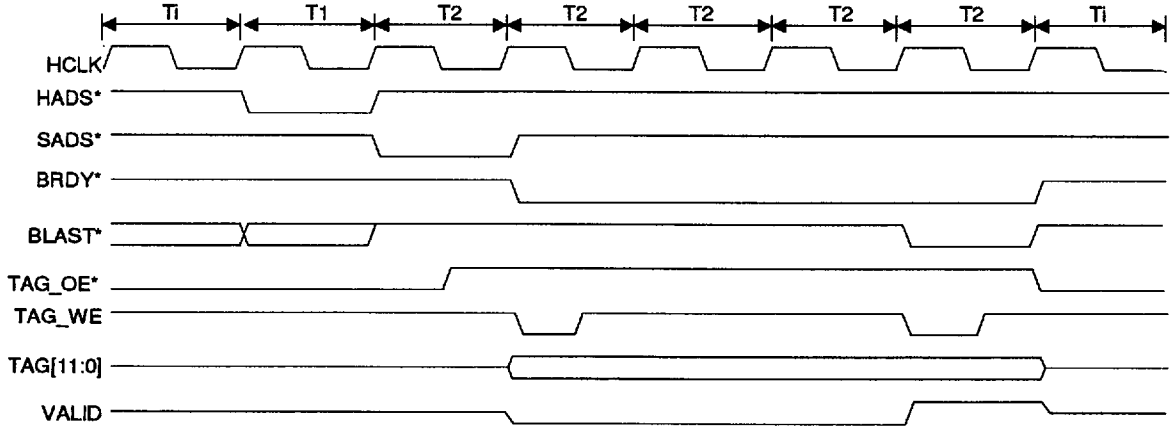


Figure 6 - TAG RAM Update during cacheable read miss cycle

4.0 Timing options

Three straps define timing options of the HT44. These are: CLK2X1, SYNC* and CSMODE.

4.1 CLK2X1 options

This option defines the input clock coming into the HT44 cache controller. If high, the input clock is considered to be double that of the system frequency. There are two implications to be considered when strapping the CLK2X1 pin high: phasing and write hit operations.

i) Phasing

HRESPCU defines the phase relation ship between the double frequency clock and single frequency source driving the CPU. Figure 2 illustrates when the phase information becomes internally available.

ii) Write hit operations

Write cycles are always terminated bythe system and not by the HT44.

In the asynchronous data SRAM option (SYNC* = high), there is an issue when writing data into the cache in a write hit situation. Since the 486 bus is synchronous, and data is invalidated on the clock edge where the HRDYI* signal terminating the cycle is sampled asserted, one cannot terminate a write hit cycle at a zero-wait-state rate if the single clock option is used (CLK2X1 = 0). When CLK2X1 = 1 and a double frequency clock is available, the HT44 uses the falling edge of the input clock to bring WEA*/WEB* up (back edge of the cycle). In this case the write hit cycle can be terminated at a zero-wait-state rate. Figure 7 illustrates this cycle.

4.2 SYNC* options

The SYNC* option defines the type of SRAM used to build the cache data array. Two major options are available: asynchronous SRAM, defined by SYNC* strap pin tied high, and synchronous SRAM with SYNC* tied low.

4.2.1 Asynchronous SRAM option (SYNC* =1)

This option requires two banks of asynchronous SRAM. WEA*/OEA* selects the first bank, WEB*/OEB* the second one. CHIPSEL*[3:0] are common for both banks. The two banks are needed because of the interleaving necessary to achieve a zero-wait-state burst rate during secondary cache read hit cycles. Interleaving occurs on address HA2.

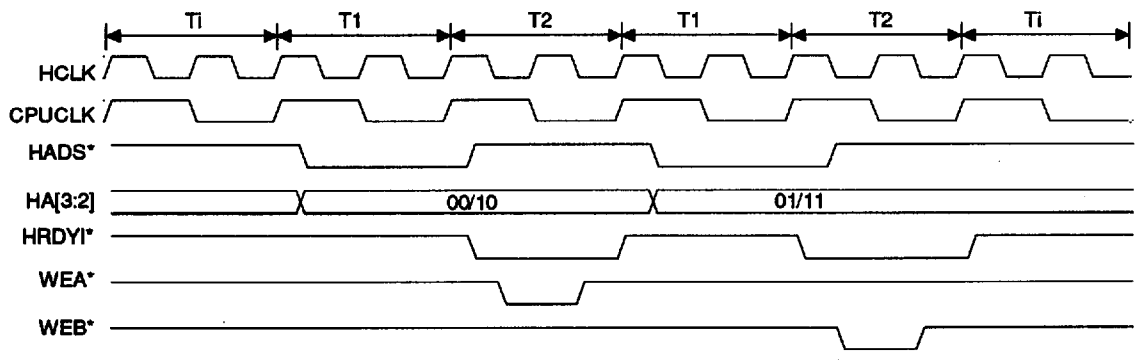


Figure 7 - Cacheable write hit cycles with double frequency clock option (CLK2X1=1)

The table below describes the interleaving scheme:

HA3	HA2	CAA0	CAB0	OEA*/WEA*	OEB*/WEB*
0	0	0	X	on	off
0	1	X	0	off	on
1	0	1	X	on	off
1	1	X	0	off	on

Figure 8 illustrates a secondary cache read hit cycle. The cycle starts from address 0, and the 486 burst sequence in this case is 0-4-8-C. According to the table above, the first bank accessed is bank A with CAA0 = 0 , then B with CAB0 = 0, then A with CAA0 = 1 and finally B with CAB0 = 1. Note that the CAA0/CAB0 lines always have at least a 2 HCLK access time (not including CPU and HT44 delays). This is due to the prediction done by the HT44 on these lines (burst address is known in advance). The other addresses for the data cache SRAMs are taken from the CPU and are stable during the cycle. BRDY* and HRDY* are supplied from the HT44 during the cycle. The cycle is not passed to the system side, so SADS* is not generated.

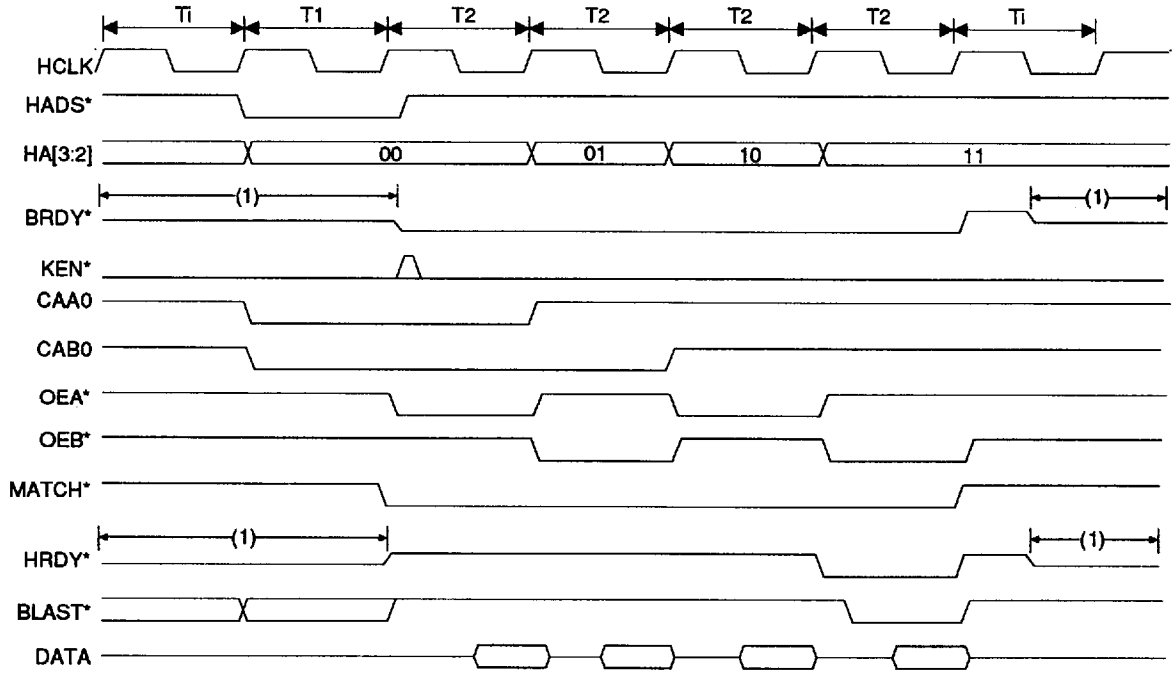


Figure 8 - Secondary cache read hit cycle with Asynchronous SRAM option (0-4-8-C Burst Sequence)

Note (1): Not Driven by HT44

Figure 9 illustrates a secondary cache read miss cycle. In this case, the burst sequence starts from address C, and the sequence is C-8-4-0. As the above table illustrates, the first bank accessed is bank B with CAB0 = 1, then A with CAA0 = 1, then B with CAB0 = 0 and finally A with CAA0 = 0. The HRDY* and BRDY* signals are supplied by the system since it is a miss cycle.

NOTE: The system has to be capable of supplying a data hold time on any of the burst miss cycles. If the system is not capable of supplying the necessary data hold time on cacheable read miss cycles, the asynchronous SRAM option (SYNC = 1) cannot be used.*

A write hit in a CLK2X1 = 0 option (single frequency clock) is shown in Figure 10. A wait state has to be added due to the inherent race condition mentioned in section 4.1.ii).

If the system is not aware of the HT44's presence and is capable of terminating the write

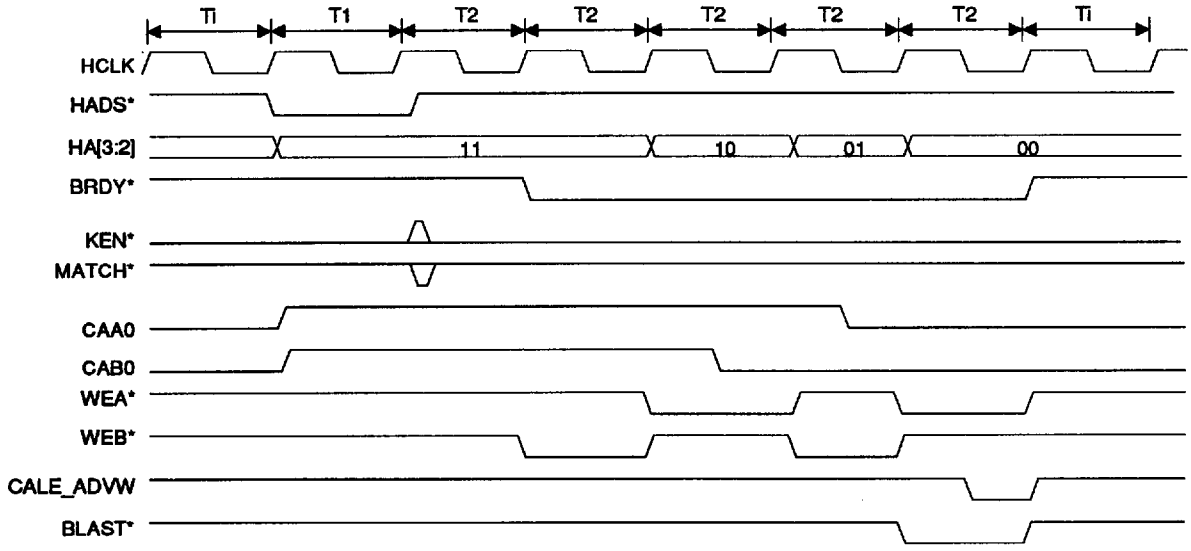


Figure 9 - Secondary cache read miss cycle with Asynchronous SRAM option

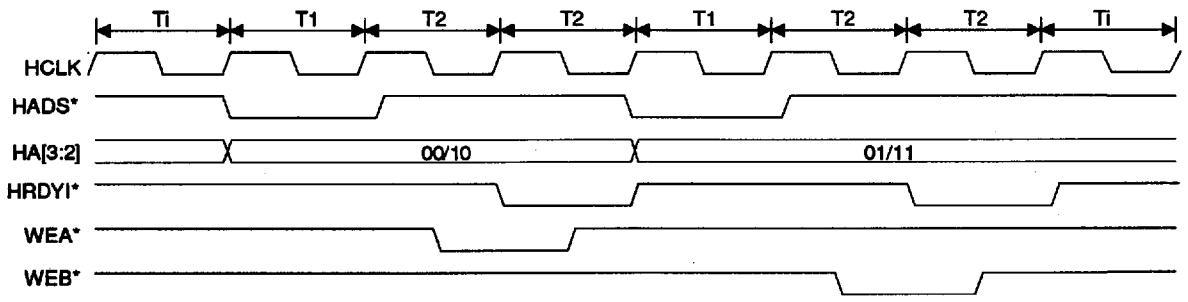


Figure 10 - Cacheable write hit cycles with Asynchronous SRAM option (CLK2X1 = 0)

cycle at a zero-wait-state rate, the asynchronous SRAM option with CLK2X1 = 0 option cannot be used. This is due to the write hit timing which requires at least a one-wait-state write cycle.

Another important signal for the asynchronous SRAM option is CALE_ADVW. It can be used to correct the problem during writing to the cache when addresses are invalidated on the same clock edge that WEA*/WEB* is negated. This applies specifically to the last burst cycle. The CALE_ADVW signal should be used as a latch enable for the data cache addresses, and the timing of this signal always makes sure that its rising edge follows the rising edge of WEA*/WEB*. See Figure 9 for the CALE_ADVW timing.

4.2.2 Synchronous SRAM option (SYNC* = 0)

The synchronous data SRAM option assumes the presence of a synchronous cache data SRAM subsystem. The major difference is that interleaving is not necessary, and therefore, one bank can be used to build the data cache array. All signals are synchronous to the single frequency clock. The synchronous SRAM option cannot be used with the double frequency option (ie. the combination of SYNC* = 0 and CLK2X1 = 1 is invalid).

In the synchronous data SRAM option, the OEA* and OEB* signals are equivalent and can be used interchangeably (for example, to spread the load). The same applies to WEA* and WEB*. Figure 11 illustrates the secondary cache read hit cycle in the synchronous SRAM option.

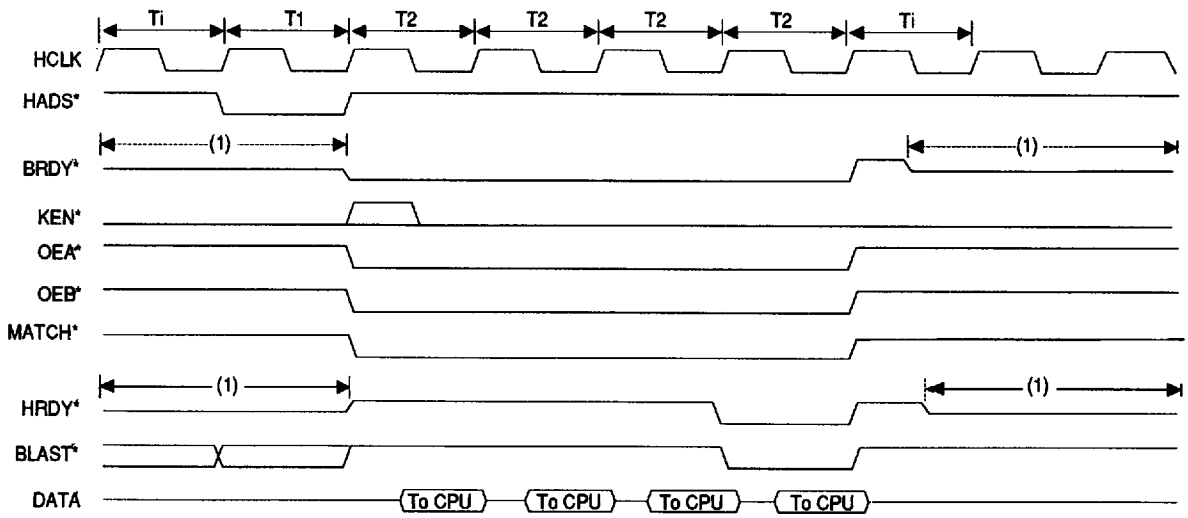


Figure 11 - Secondary cache read hit cycle with Synchronous SRAM option

Note (1): Not Driven by HT44

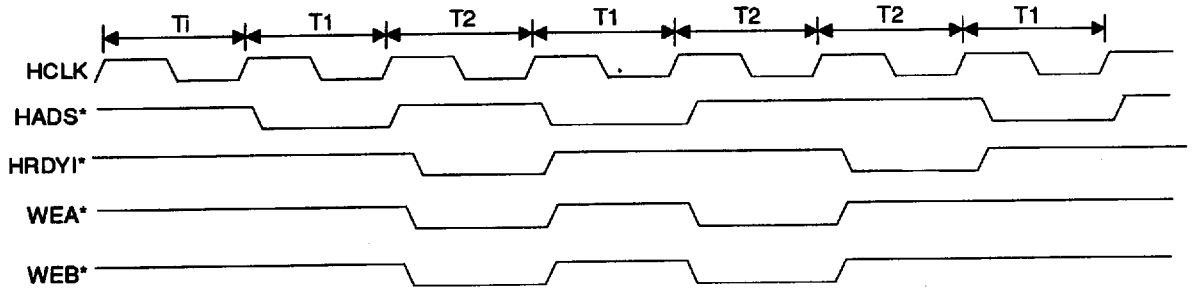


Figure 12 - Cacheable write hit cycles with synchronous SRAM option

Secondary cache write hit cycles in the synchronous SRAM option always implement a zero-wait-state write hit cycle. Obviously, it is up to the system to terminate the cycles, but there are no constraints from the HT44 cache controller as far as the rate of the cycles is concerned. The timing is shown on Figure 12.

Secondary cache read miss cycles in the synchronous cache data SRAM mode have two additional modes of operation. The modes of operation relate to the behavior of the CHIPSEL*[3:0] signals in the synchronous data SRAM option. Figure 13 shows cacheable read miss cycles in the synchronous data cache SRAM option. These additional modes are described in Section 4.3.

4.3 CSMODE options

The HT44 cache controller implements two different timing options on the CHIPSEL*[3:0] lines during cacheable read miss cycles in the synchronous data cache SRAM option. The CSMODE =1 option matters only when SYNC*=0 (synchronous data SRAM option).

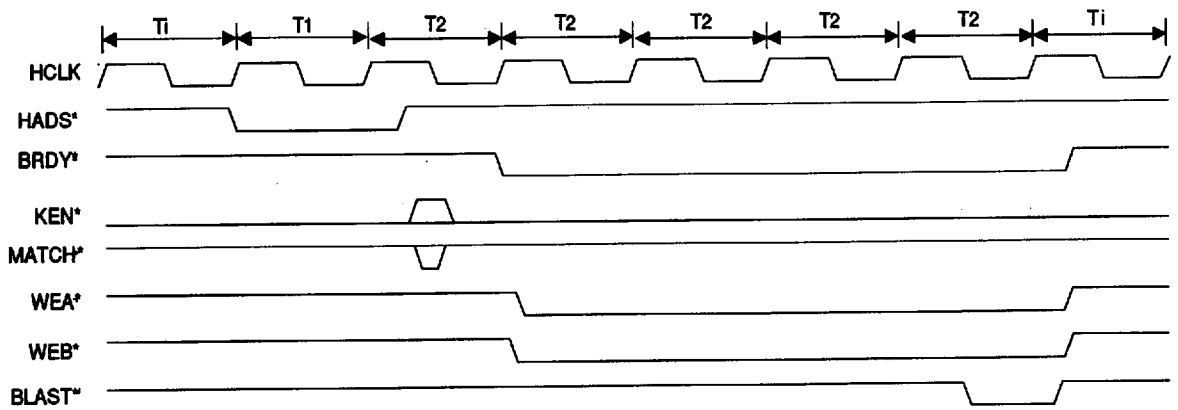


Figure 13 - Secondary cache read miss cycle with Synchronous SRAM option

When CSMODE=0, the CHIPSEL*[3:0] lines follow either HWR line (if low indicating a read cycle, then all CHIPSEL*[3:0] are activated) or HBE*[3:0] lines (if HWR = 1 indicating a write cycle, then CHIPSEL*[3:0] follow HBE*[3:0], respectively). With CSMODE = 1 and SYNC* = 0, the CHIPSEL*[3:0] lines, during cacheable read miss cycles, follow the BRDY* line asynchronously. In this way, the lines are activated only for the clock edge when data becomes available. For all other types of cycles, the CHIPSEL*[3:0] lines behave the same way regardless of the CSMODE option setting.

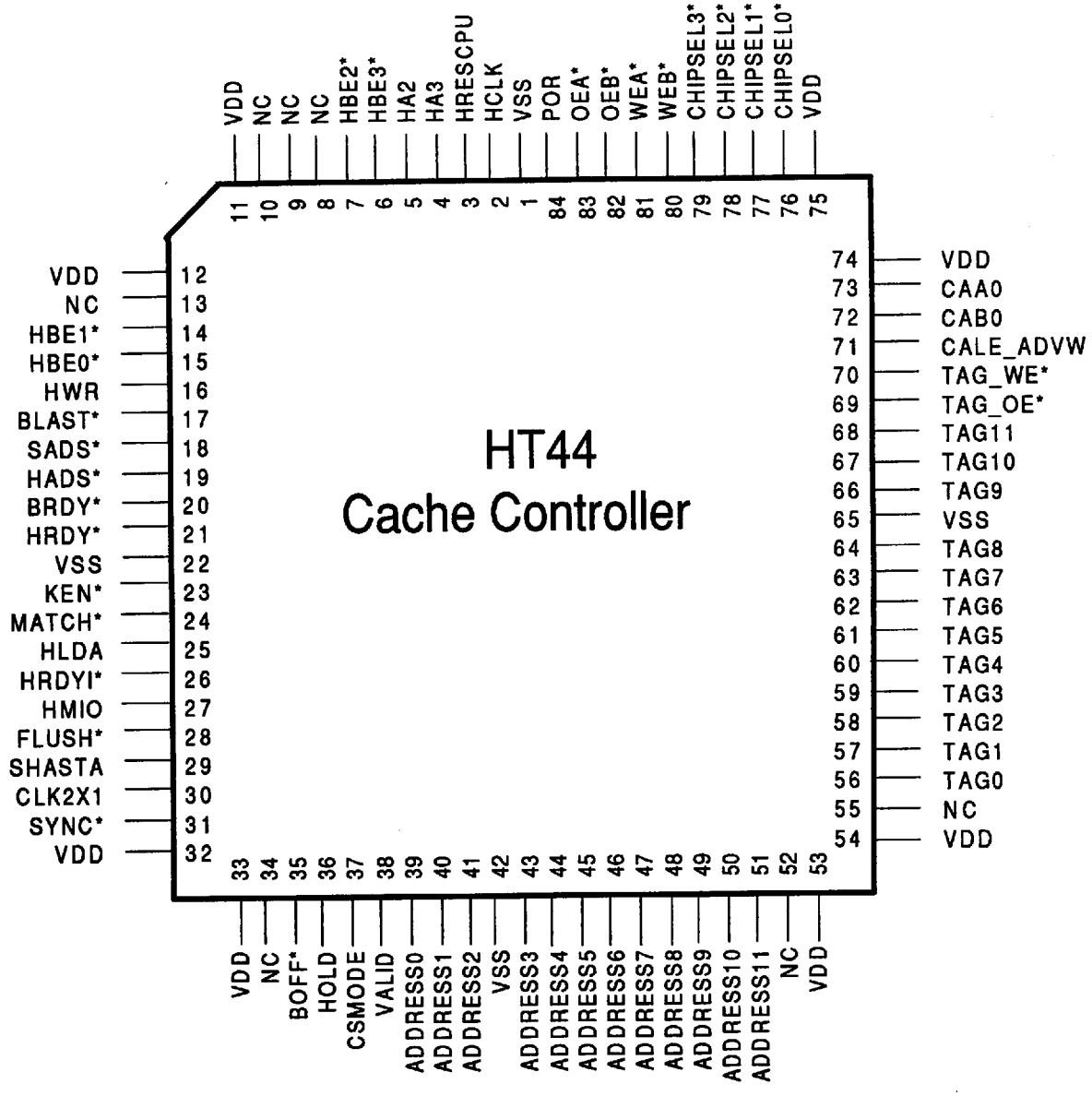
4.4 Summary of options

The table below summarizes all options of the HT44 chip.

CLK2X1	SHASTA	SYNC*	CSMODE	Description
0	0	0	0	Non-SHASTA mode with synchronous data SRAMs
0	0	0	1	As above
0	0	1	X	Non-SHASTA mode with asynchronous data SRAMS and single frequency clock
0	1	0	0	SHASTA mode with synchronous data SRAMs
0	1	0	1	As above
0	1	1	X	Should not be used
1	0	0	X	Should not be used
1	0	1	X	Non-SHASTA mode with asynchronous data SRAMs and double frequency clock

HT44
486 Cache Controller

Pin Diagram



Pin Names in Alphabetical Order

ADDRESS[11:0]	51-43,41-39	HRDY*	21
BLAST*	17	HRESCPU	3
BOFF*	35	HWR	16
BRDY*	20	KEN*	23
CAA0	73	MATCH*	24
CAB0	72	NC	8,9,10,13,34,52,55
CALE_ADVW	71	OEA*,OEB*	83-82
CHIPSEL*[3:0]	79-76	POR	84
CLK2X1	30	SADS*	18
CSMODE	37	SHASTA	29
FLUSH*	28	SYNC*	31
HA[3:2]	4-5	TAG[11:0]	68-66, 64-56
HADS*	19	TAG_OE*	69
HBE*[3:0]	6-7, 14-15	TAG_WE*	70
HCLK	2	VALID	38
HLDA	25	WEA*,WEB*	81-80
HMIO	27	VDD	11,12,32,33,53,54,74,75
HOLD	36	VSS	1,22,42,65
HRDYI*	26		

Pin Names and Numbers in Numerical Order

1	VSS	30	CLK2X1	59	TAG3
2	HCLK	31	SYNC*	60	TAG4
3	HRESCPU	32	VDD	61	TAG5
4	HA3	33	VDD	62	TAG6
5	HA2	34	NC	63	TAG7
6	HBE*3	35	BOFF*	64	TAG8
7	HBE*2	36	HOLD	65	VSS
8	NC	37	CSMODE	66	TAG9
9	NC	38	VALID	67	TAG10
10	NC	39	ADDRESS0	68	TAG11
11	VDD	40	ADDRESS1	69	TAG_OE*
12	VDD	41	ADDRESS2	70	TAG_WE*
13	NC	42	VSS	71	CALE_ADVW
14	HBE*1	43	ADDRESS3	72	CAB0
15	HBE*0	44	ADDRESS4	73	CAA0
16	HWR	45	ADDRESS5	74	VDD
17	BLAST*	46	ADDRESS6	75	VDD
18	SADS*	47	ADDRESS7	76	CHIPSEL*0
19	HADS*	48	ADDRESS8	77	CHIPSEL*1
20	BRDY*	49	ADDRESS9	78	CHIPSEL*2
21	HRDY*	50	ADDRESS10	79	CHIPSEL*3
22	VSS	51	ADDRESS11	80	WEB*
23	KEN*	52	NC	81	WEA*
24	MATCH*	53	VDD	82	OEB*
25	HLDA	54	VDD	83	OEA*
26	HRDYI*	55	NC	84	POR
27	HMIO	56	TAG0		
28	FLUSH*	57	TAG1		
29	SHASTA	58	TAG2		

Pin Name	Pin Number	Pin Type	Description
Local Bus Interface			
BLAST*	17	I	Burst LAST (Active Low). This signal comes from the Local Bus Host indicating the last cycle in the burst sequence. The signal is ignored during the fourth burst cycle.
BOFF*	35	I	Back OFF (Active Low). This signal comes from Local Bus devices requesting control of the CPU bus. In a 486 system, the CPU will grant its bus one HCLK after receiving the BOFF* signal.
BRDY*	20	I/O	Burst ReaDY (Active Low). This signal goes active to indicate the readiness to end a burst cycle. It is activated during read hits only and terminates every one of the burst cycles in the burst sequence. This signal will last one HCLK, then will be driven high and tri-stated.
HA[3:2]	4,5	I	Host Address line bus. These lines are inputs and are used to determine the burst sequence. Usually these lines are driven by the CPU, except during DMA.
HADS*	19	I	Host ADdress Strobe (Active Low). Defines the beginning of the cycle.
HBE*[3:0]	6-7, 14-15	I	Host Byte Enables (Active Low). These signals define onto which byte the data will be transferred. During read cacheable cycles, the state of these lines is irrelevant and all 4 bytes have to be provided to the Local Bus.
HCLK	2	I	Host CLocK. HT44 clock input. A 1X or 2X clock can be connected to the HT44 depending on the operating mode required.
HLDA	25	I	HoLD Acknowledge. This signal signifies that the CPU has relinquished its bus in response to a HOLDRQ. The device issuing the HOLDRQ now has control of the local bus.

Pin Symbol	Pin Number	Pin Type	Description
HMIO	27	I	Host Memory or I/O. This signal with HADS* defines the type of the host access.
HOLD	36	I	HOLD request. This signal signifies that another device is requesting control of the local bus. This signal is used in conjunction with HLDA to fully define the DMA/MASTER cycles.
HRDY*	21	I/O	Host ReaDY (Active Low). This signal goes active to indicate the readiness to end the cycle. It is activated during read hits only and terminates the last cycle in the burst sequence. This signal will last one HCLK, and then will be driven high and tri-stated.
HRDYI*	26	I	Host ReaDY In (Active Low). This signal goes active to indicate final termination of the current cycle. This signal will be activated for one HCLK, and then will be driven back to its inactive state.
HRESCPU	3	I	Host RESet CPU. This signal is an indication to the HT44 that the CPU is being reset. This signal is used for phase synchronization of the internal clocks within the HT44 when the 2X HCLK option is used. This signal is also used to qualify the strap input pins and, hence, must be connected for both 1XHCLK and 2XHCLK modes.
HWR	16	I	Host Write Read. This signal with HADS defines the type of host access.
KEN*	23	I/O	Cache ENable (Active Low). This signal comes from the external chip set and indicates whether the cycle is cacheable. The only cycles that can be defined as cacheable by this chip are memory addresses, for which the HT44 cache controller is capable of storing the address tags. This signal qualifies hit cycles during the CPU T2 state. During T1 and Idle states the signal is always asserted. In Shasta Mode, KEN* is driven by the HT44 during Idle and T1 CPU states and then tri-stated.
POR	84	I	Power On Reset. This is the signal that indicates the entire system is being reset.

Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
SADS*	18	O	System ADdress Strobe (Active Low). This signal indicates the beginning of the cycle for all Local Bus devices except for the HT41 chip. The signal is asserted one clock after HADS* has been asserted if the KEN* input during this clock is deasserted. In Shasta mode, SADS* drives the entire local bus including the Shasta Chip set. Cycles for the Local Bus devices connected to the SADS* output cannot be cached by the HT44 cache controller.
Configuration			
CLK2X1	30	I	CLocK2X1. This input is used to select the type of Clocking connected to the HT44. Pulling the pin down indicates a single phase 1X clock is connected to the HCLK input, pulling it up indicates that a 2X clock is connected to the HCLK input. The 2X clock should only be used in conjunction with the asynchronous SRAM option.
CSMODE	37	I	Chip Select MODE. This input is used to select the type of timing generated on the CHIPSEL[3:0] outputs. See Functional Description for more detail.
SHASTA	29	I	SHASTA. This input is used to select the interface for the HT44. Pulling this pin up selects the HTK340 interface option.
SYNC*	31	I	SYNC (Active Low). This input is used to select the type of SRAM connected to the HT44. Pulling the pin down indicates that the synchronous SRAM interface has been enabled, pulling it up indicates the asynchronous SRAM interface has been enabled.

Pin Name	Pin Number	Pin Type	Description
Data Cache Control Signals			
CAA0	73	O	Cache Address bank A, bit 0 . This is the lower-data-cache-RAMs address lines for bank A. This is needed for address prediction and interleaving during bursting.
CAB0	72	O	Cache Address bank B, bit 0. This is the lower-data-cache-RAMs address lines for bank B. This is needed for address prediction and interleaving during bursting.
CALE_ADVW	71	O	CALE_ADVanced Write. This signal is used to latch addresses on the asynchronous cache RAMs. When SYNC* is active, this pin becomes an advanced write strobe. See Functional Description for more details.
CHIPSEL*[3:0]	79-76	O	Data Cache CHIP SELects (Active Low). These are byte selects connected to CS lines enabling individual bytes during write hit/read miss updates.
FLUSH*	28	I	FLUSH (Active Low). This signal flushes a tag entry on the first clock after a read cycle has been found, regardless of the hit information.
OEA*,OEB*	83-82	O	Data Cache Output Enables (Active Low). These are output enables for two banks of cache data RAMs. For the asynchronous data SRAM option, the existence of two banks of data SRAM is mandatory. The data is always interleaved between the banks. For the synchronous data SRAM option, these two outputs are equivalent.
WEA*,WEB*	81-80	O	Data Cache Write Enables (Active Low). These are write enables for two banks of the cache data RAMs. For the asynchronous data SRAM option, the existence of two banks of the data SRAM is mandatory. The data is always interleaved between the banks. For the synchronous data SRAM option, these two outputs are equivalent.

Pin Symbol	Pin Number	Pin Type	Description
Tag Ram Interface			
ADDRESS[11:0]	51-43, 41-39	I	ADDRESS inputs. This is the address stored in the TAG RAM during miss cycles. The address is compared against the TAG[11:0] lines in order to find the hit/miss information. The lines come from the HA lines directly and depend on the cache and DRAM memory size. Not all lines have to be used for some cache and memory sizes. Unused lines should be pulled high through a weak resistor.
MATCH*	24	O	MATCH (Active Low). This output supplies the comparison result of TAG[11:0] inputs and ADDRESS[11:0] inputs. If these inputs are equal, then MATCH will go active. This signal remains valid for the duration of the cycle.
TAG_OE*	69	O	TAG RAM Output Enable (Active Low). This signal enables the read operation from the TAG RAM. It is deactivated during read miss cycles and flush operations. The clock edge deactivating the signal is used to latch the TAG information coming from the TAG RAM. Both TAG and VALID information use this signal.
TAG_WE*	70	O	TAG RAM Write Enable (Active Low). This signal controls the write operation to the TAG RAM. It is activated during read miss cycles and flush operations. Both TAG and VALID information use this signal.
TAG[11:0]	68-66, 64-56	I/O	Address TAG. The address portion of the TAG is written to the TAG RAM and read from the TAG RAM on these lines. The ADDRESS[11:0] lines appear on the TAG[11:0] lines, while writing to the TAG RAM. Note that not all lines have to be used for some cache and memory sizes. Unused lines should be pulled high through a weak resistor.
VALID	38	I/O	Line VALID. This is the signal stored in the TAG RAM indicating that the entire line is present and valid in the cache. The bit qualifies the comparison result between the ADDRESS[11:0] and TAG[11:0] lines.

Pin Symbol	Pin Number	Pin Type	Description
Power, Ground and No Connects			
VSS	1,22,42,65		Ground
VDD	11,12,32,33,53, 54,74,75		5V Power
NC	8,9,10,13,34, 52,55		No Connects

DC Specifications

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD + 0.3	V
DC Input Current	IIN	10	mA
Storage Temperature Range	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Case Temperature Range (Commercial)	TC	0 to +85	C

DC Characteristics: VDD = 5V +/- 5%, TC = 0°C to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL				0.8	V
Voltage Input High	VIH		2			V
Input Current	IIH		-10	1	10	uA
Voltage Output High OEA*, OEB*, WEA*, WEB*	VOH	IOH = 12mA	2.4	4.5		V
CAA0, CAB0, CHISEL*[3:0]		IOH = 8mA	2.4	4.5		V
TAG_OE*, HRDY*, KEN*, HADS*, SADS*, BRDY*		IOH = 6mA	2.4	4.5		V
MATCH*, CALE_ADVW, TAG[11:0], VALID		IOH = 4mA	2.4	4.5		V
OEA*, OEB*,WEA*, WEB*		IOH = 24mA	0.4	0.8		V
CAA0, CAB0, CHIPSEL*[3:0]		IOL = 16mA	0.4	0.8		V
TAG_OE*, HRDY*, KEN*, HADS*, SADS*, BRDY*		IOL = 12mA	0.4	0.8		V
MATCH*, CALE_ADVW, TAG[11:0], VALID		IOL = 8 mA	0.4	0.8		V
Tri-State Output Leakage Current	IOZ	VOH=VSS OR VDD	-10	1	10	uA
Output Short Circuit Current (See Note)	IOS	VDD=Max, VO=VDD, VO=OV, VDD=Max	20 -10	110 -90	220 -190	mA mA
Supply Current	IDD	CLK = 25MHz CL=50pF		18	28	mA

Note: Not more than One Output may be shorted at a time, for a maximum duration of ONE SECOND.

Symbol	Parameter	Min	Max	Unit	Fig. Ref	Notes
t1	HCLK		33	MHz		Duty Cycle 50% +/- 5%
t2	HRESCPU, HA[3:2] Setup	2		ns	14b	Note 1
t3	HRESCPU, HA[3:2] HOLD	2		ns	14b	Note 1
t4	HRDYI* Setup	3		ns	14b	Note 1
t5	HRDYI* Hold	3		ns	14b	Note 1
t6	KEN*, POR setup	4		ns	14b	Note 1
t7	KEN*, POR Hold	3		ns	14b	Note 1
t8	HADS*, HMIO, HWR, HHLDA, HOLD, BLAST*, BRDY*, BOFF Setup	5		ns	14b	Note 1
t9	HADS*, HMIO, HWR, HHLDA, HOLD, BLAST*, BRDY*, BOFF hold	3		ns	14b	Note 1
t10	ADDRESS[11:0] Setup	7		ns	14b	Note 1
t11	ADDRESS[11:0] Hold	3		ns	14b	Note 1
t12	TAG[11:0], VALID Read Setup	9		ns	14b	Note 1
t13	TAG[11:0], VALID Read Hold	3		ns	14b	Note 1
t14	TAG[11:0], VALID Write Delay	3	10	ns	14a	Note 1
t15	TAG[11:0], VALID Write Float Delay	3	11	ns	14a	Note 1
t16	HRDY* Valid Delay	3	12	ns	14a	Note 1
t17	HRDY* Float Delay	3	10	ns	14a	Note 3
t18	BRDY* Valid Delay	3	11	ns	14a	Note 1
t19	BRDY* Float Delay	3	10	ns	14a	Note 3
t20	HADS* Valid Delay (Asynchronous delay from SADS*)	3	8	ns	14c	Note 2
t21	HADS* Float Delay (Asynchronous delay from HLDA, HOLD and BOFF)	3	8	ns	14c	Note 2
t22	KEN* Valid Delay	3	10	ns	14a	Note 1
t23	KEN* Valid Delay (Asynchronous delay from TAG [11:0] and VALID)	3	10	ns	14c	Note 2

VDD = 5 V +/- 5%, TC = O°C - 85°C, CL = 50pF

AC Characteristics

Symbol	Parameter	Min	Max	Unit	Fig. Ref	Notes
t24	KEN* Float Delay	3	10	ns	14a	Note 3
t25	SADS* Valid Delay (Asynchronous delay from HADS*, HWR and HMIO)	3	8	ns	14c	Note 2
t26	SADS* Float Delay (Asynchronous delay from HLDA, HOLD and BOFF)	3	8	ns	14c	Note 2
t27	OEA*, OEB* Delay	3	10	ns	14a	Note 1
t28	WEA*, WEB* Delay	3	10	ns	14a	Note 1
t29	WEA*, WEB*, Delay (Asynchronous delay from TAG[11:0] and VALID)	3	13	ns	14c	Note 2
t29a	WEA*, WEB* Delay (Asynchronous delay from BRDY*)	3	8	ns	14c	Note 2
t30	CALE Delay	3	17	ns	14a	Note 1
t31	CALE Delay (Asynchronous delay from TAG[11:0] and VALID)	3	14	ns	14c	Note 2
t32	CAA0, CAB0 Delay	3	13	ns	14a	Note 1
t33	CAA0, CAB0 Delay (Asynchronous delay from HA[3:2])	3	8	ns	14c	Note 2
t34	CHIPSEL* [3:0] Delay (Asynchronous delay from BRDY*)	3	8	ns	14c	Note 2
t35	CHIPSEL* [3:0] Delay (Asynchronous delay from HBEN[3:0])	3	8	ns	14c	Note 2
t36	CHIPSEL* [3:0] Delay (Asynchronous delay from TAG [11:0] and VALID)	3	11	ns	14c	Note 2
t37	MATCH* Delay (Asynchronous delay from TAG [11:0] and VALID)	3	11	ns	14c	Note 2
t38	TAG_WE* Delay	3	15	ns	14a	Note 1
t39	TAG_OE* Delay	3	10	ns	14a	Note 4

VDD = 5 V +/- 5%, TC = $O^{o}C$ - $85^{o}C$, CL = 50pF

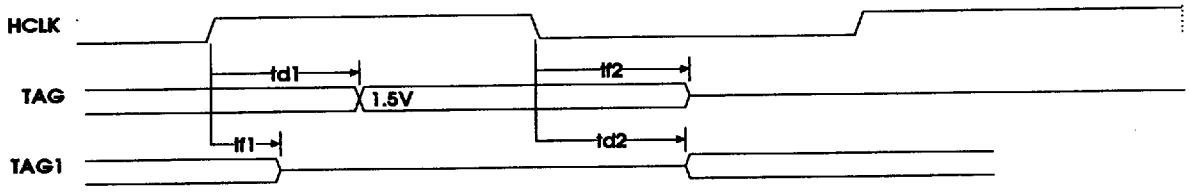


Figure 14a

td1 = t14, t16, t18, t22, t27, t28, t30, t30, t32, t38, t39

tf1 = t15

td2 = t39

tf2 = t17, t19, t24

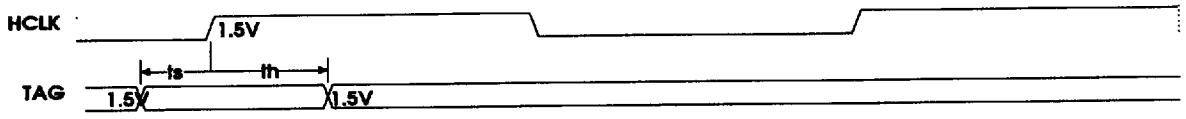


Figure 14b

ts = t2, 54, t6, t8, t10, t12

th = t3, t5, t7, t11, t13

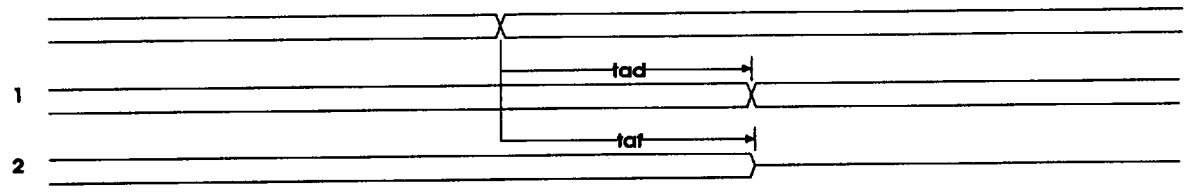


Figure 14c

tad = t20, t23, t25, t29, t31, t33, t34, t35, t36, t37

taf = t21, t26

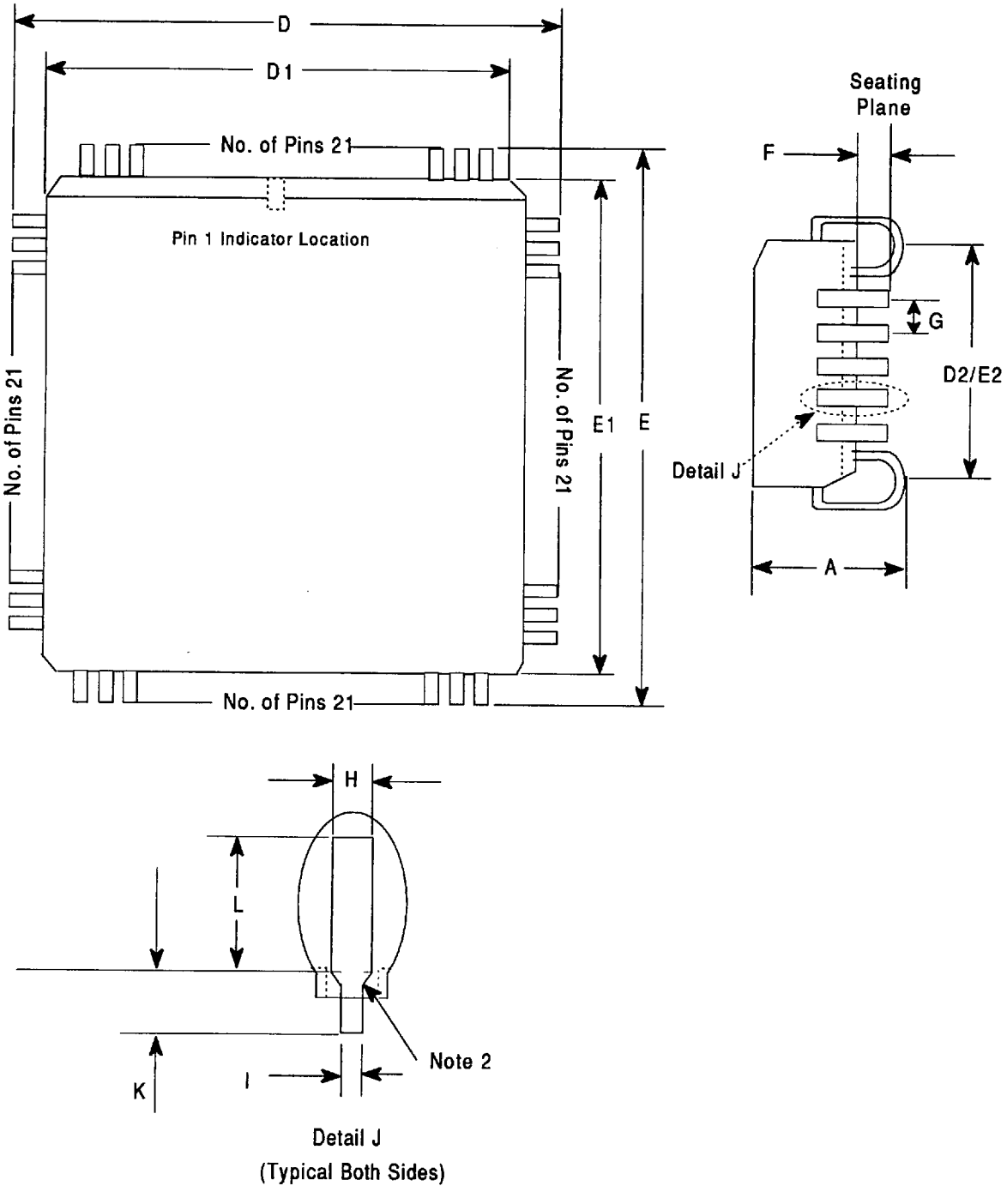
Note 1: The parameters are relative to the rising edge of the HCLK signal.

Note 2: The parameters are asynchronous delays from input signals.

Note 3: The parameters are relative to the falling edge of the HCLK signal.

Note 4: The parameters are relative to the rising or falling edge of the HCLK signal dependent upon the timing shown.

Package Outline



Detail J
(Typical Both Sides)

See Notes on next page.

Plastic Leaded Chip Carrier Dimensions

84-Pin PLCC (J-Bend) (MD)

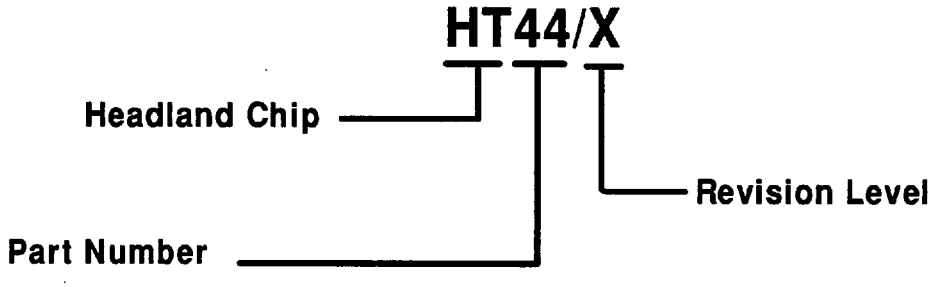
Dimensions in inches		
Symbol	Min	Max
A	0.165	0.200
D	1.185	1.195
D1	1.150	1.158
D2	1.090	1.130
E	1.185	1.195
E1	1.150	1.158
E2	1.090	1.130
F	0.020	
G Ref	0.050	
H	0.026	0.032
I	0.013	0.021
K	0.025	
L	0.060	

Dimensions in mm		
Symbol	Min	Max
A	4.191	5.080
D	30.10	30.35
D1	29.21	29.41
D2	27.69	28.70
E	30.10	30.35
E1	29.21	29.41
E2	27.69	28.70
F	0.508	
G Ref	1.270	
H	0.660	0.813
I	0.330	0.533
K	0.635	
L	1.524	

Notes:

1. *All dimensions and tolerances conform to ANSI Y14.5M-1982.*
2. *Transition is optional.*
3. *Plastic body details between leads are optional.*
4. *Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.010 inch/0.254 mm.*
5. *Controlling dimension - inch.*
6. *Lead and pockets are optional.*

Product Order Information



IMPORTANT: Contact your local sales office for the current Order Code/Part Number

Appendix A: Schematic Diagram of the HT44 Evaluation Module

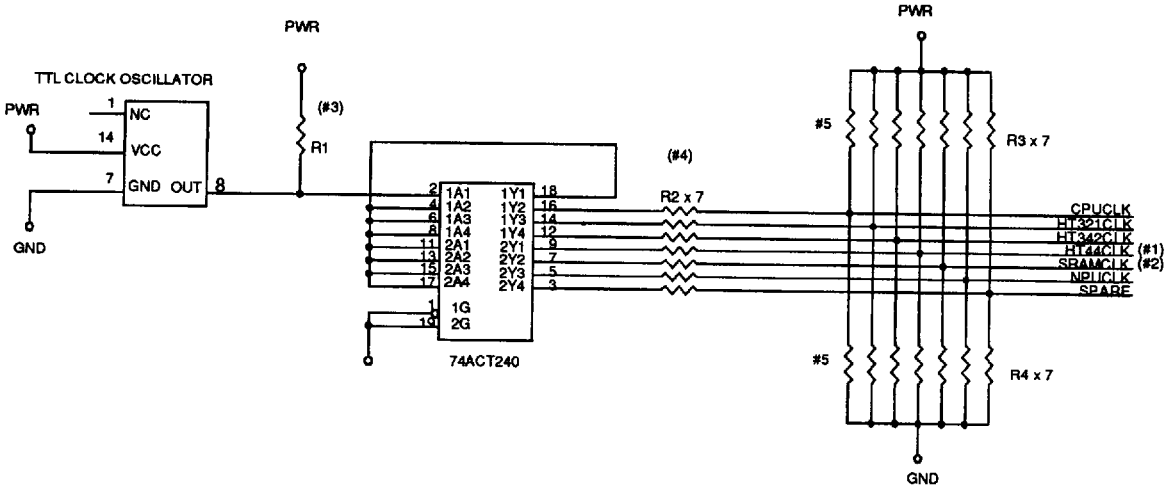
Description: The HT44 evaluation module is designed to plug into the CPU socket of the HTK340 evaluation motherboard for the purpose of demonstrating the performance and compatibility of the HT44 secondary cache controller. This module is not intended to be a production design. Rather, the HT44 is intended to be designed onto the motherboard of 486 systems via an 84-pin PLCC socket.

Motherboard Implementation Notes:

In a motherboard implementation the following changes and/or additions to this schematic are required:

CLOCKING:

It is highly recommended that individual clocking sources be used for the HT44 and the synchronous SRAM. These clock sources should come directly from the main clock driver chip that supplies the CPUCLK signal. An example diagram is shown below:



NOTES:

(1) This signal line should be connected to the HT44, pin 2 (HCLK).

(2) This signal line should be connected to the "CLK" input of the synchronous SRAM array.

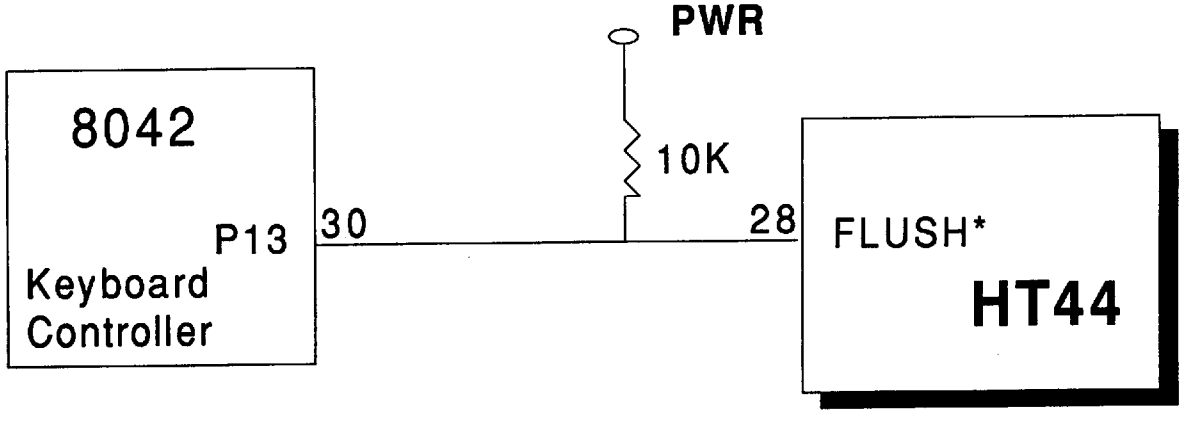
(3) The values of R1, R2, R3, and R4 vary from layout to layout. It is up to the designer to choose the correct values for their design.

(4) Place these series dampening resistors close to the 74ACT240 buffer.

(5) Place these terminating resistors close to the destination device.

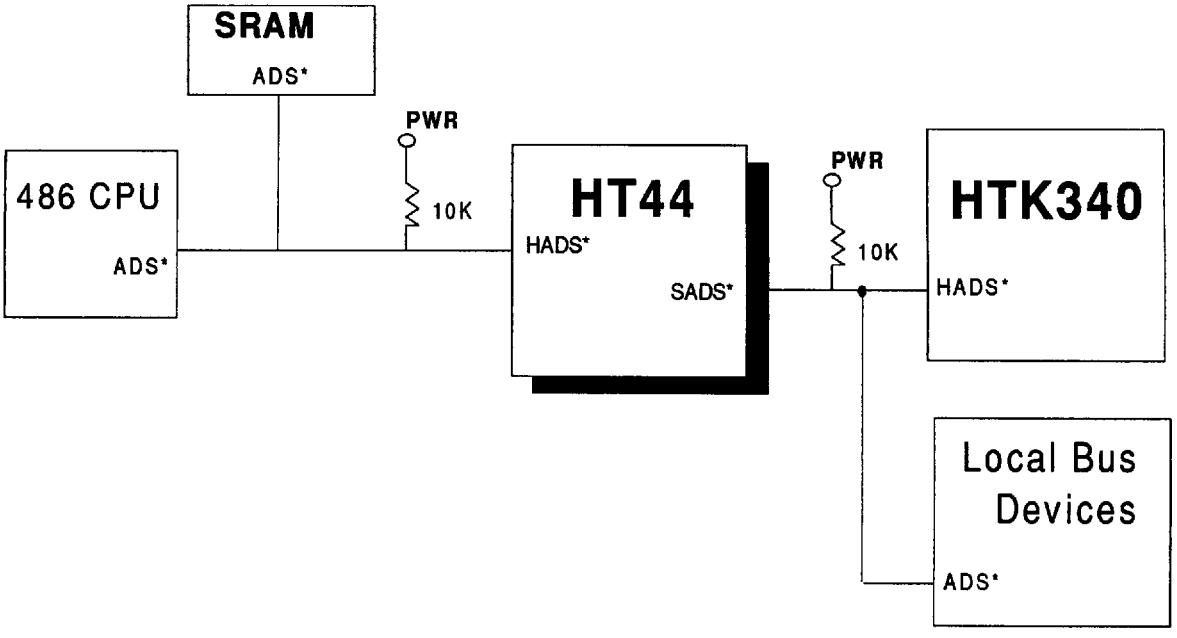
FLUSH*

BIOS developed for the HT44 has the option of disabling the caching operation of the HT44 separately from the 486 internal cache. In order to achieve this, a separate connection is required from the 8042 keyboard controller device to the HT44 FLUSH* pin. BIOS has been designed to use P13, (pin 30 of a 40 pin DIP device) on the 8042 for this function. The connection required on the board is shown below.



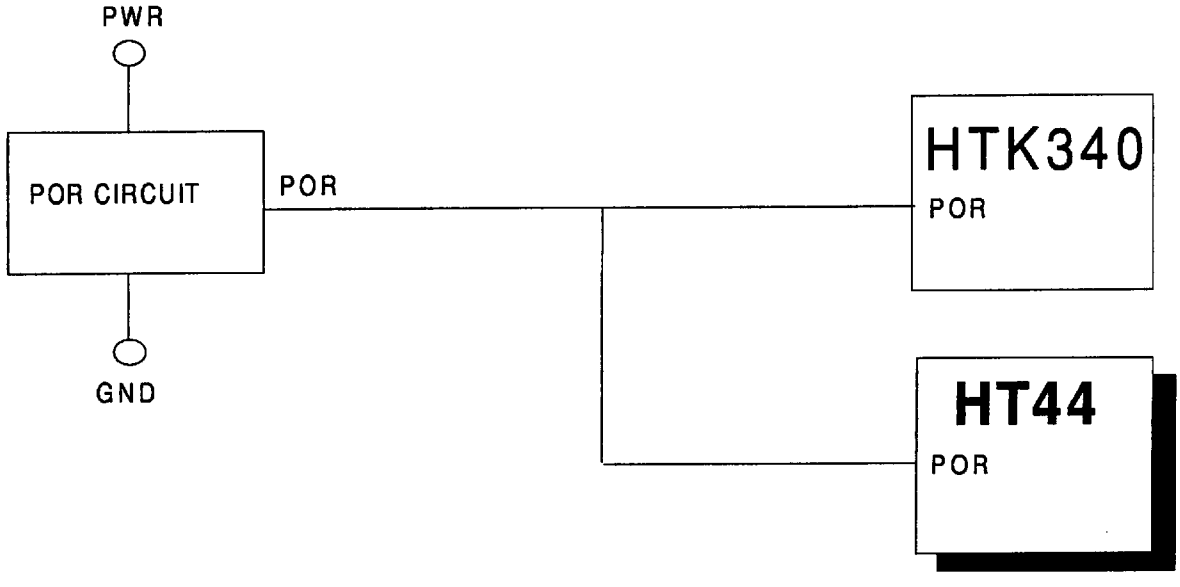
SADS*

The exact connection required for the HADS* and SADS* signals may not be clear from the schematic. The block diagram below is meant to clarify this situation. Although the HT44 is a look-aside cache controller, it is necessary to intercept the ADS* signal coming from the CPU when used in conjunction with the HTK340 chip set. The HTK340, as well as all other local bus devices should connect their ADS* pins to the SADS* signal on the HT44. A typical connection is shown below.



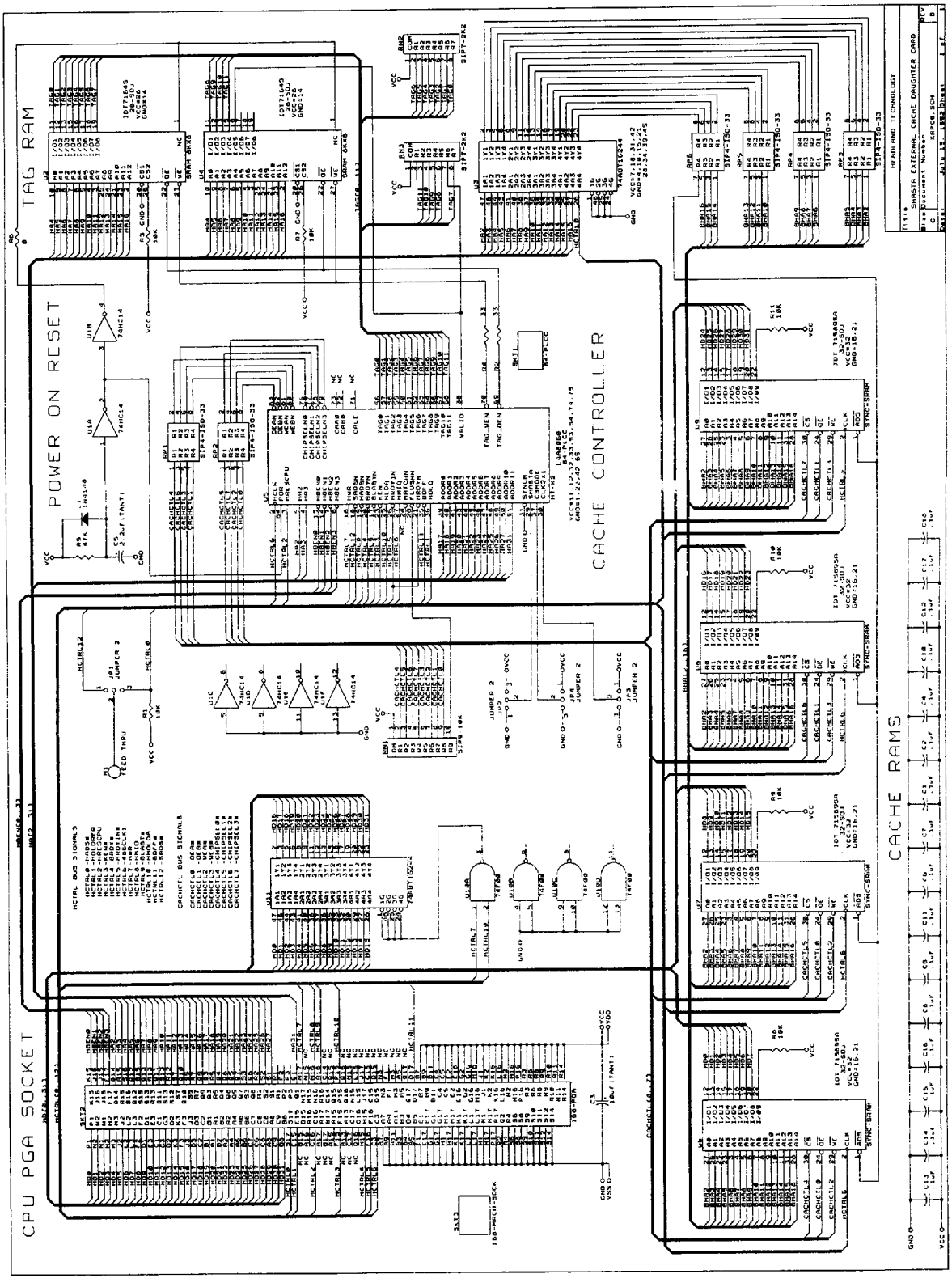
POR

The POR circuit detailed in the HT44 Daughter Card Schematic may not be required for motherboard implementation. Typically, a similar circuit already exists on the motherboard design to provide reset to the system. The POR signal applied to the HTK340 chip set is all that is required for the HT44 POR input. A diagram showing this connection is given below.



Appendix A

Warning:The schematic on the following page is intended as a design example only. Changes to this design can occur. Contact your local Headland Field Applications Engineer to ensure that you have the latest revision. Headland assumes no responsibility for designs based on this schematic.


TAG RAM
POWER ON RESET
CACHE CONTROLLER
CACHE RAMS
CPU PGA SOCKET

Appendix B: Bill of Material

HT44 Module Revision B

Headland does not endorse or support any of the manufacturers listed below. However, these parts have been proven to work and any substitutions should have equivalent or better specifications.

Item	Qty	Reference	Part	Description	Maker	Part #
1	1	C3	10uF(TANT)	CAPACITOR 16V,TANTALUM, SMT	MATSUO	267M1602106
2	1	C5	2.2uF(TANT)	CAPACITOR,16V, TANTALUM, SMT	MATSUO	267M1602336
3	16	C1,C2,C4,C6, C7,C8,C9,C10, C11,C12,C13, C14,C15,C16, C17,C18	1uF	CAPACITOR, CERAMIC, 1206 SMT	NOVACAP	1206Z105M500N
4	7	R1,R3,R7,R8, R9, R10,R11	10K	RESISTOR,5%,1206 SMT	DALE	10000 OHM CRCW1206
5	6	RP1,RP2,RP3, RP4,RP5,RP6	SIP4-ISO-33	4 RESISTOR SIP, ISOLATED, 33 OHM	DALE	CSC08A-03-330K
6	1	RN1	SIP9-10K	9 RESISTOR SIP, BUSSED,10000 OHM	DALE	CSC10A-01-103K
7	2	RN2,RN3	SIP7-2K2	7 RESISTOR SIP,BUSSED,2200 OHM	DALE	CSC08A-01-222K
8	1	R6	0	RESISTOR,5%,1206,SMT	DALE	0 OHM CRCW 1206
9	2	R4,R2	33	RESISTOR,5%,1206,SMT	DALE	33 OHM CRCW1206
10	1	R5	47K	RESISTOR,5%,1206,SMT	DALE	47000 OHM CRCW1206
11	1	D1	1N4148	DIODE,SMT SOT23	MOTOROLA	FDS0914.SO
12	4	JP1,JP2,JP3, JP4	JUMPER 2	3 PIN HEADER,SINGLE ROW	SAMTEC	TSW-103-07-TS
13	1	SKT1	84-PLCC	PLCC SOCKET,84 POSITION WITH POSTS, SMT	AMP	822152-1
14	1	SKT2	168-PGA	PGA SOCKET,168 POSITION,17x17	PCI	UXP17168TLA70
15	1	SKT3	168-MACH-SOCK	MACHINED SOCKETS,168 PIECES PER BOARD	SAMTEC	SC-1P1-GG

Item	Qty	Reference	Part	Description	Maker	Part #
16	1	H1	FEED THRU	NO PART REQUIRED, HOLE IN PCB TO CONNECT A WIRE		
17	2	U3,U11	74ABT16244	16 BIT BUFFER,48 PIN SSOP	TI	74ABT16244DL
18	1	U10	74F00	FAST IC,QUAD 2 INPUT NAND, 14 PIN SOIC	SIGNETICS	74F00D
19	1	U1	74HC14	HS CMOS IC,HEX INV SCHMITT, 14 PIN SOIC	SIGNETICS	74HC14D
20	1	U5	HT44	EXTERNAL CACHE CTRL,84 PLCC	HEADLAND	L4A8060
21	2	U4,U2	SRAM 8KX8	CMOS SRAM,8Kx8,28 PIN SOJ,15nS	IDT	IDT7164S15Y
22	4	U6,U7,U8, U9	SYNC-SRAM	SRAM,32Kx9,BURST CNTR,20nS 32 PIN	SOJIDT	IDT71589S20Y

Appendix C - BIOS Vendors

BIOS for the HT44 cache controller and the HTK340 486 chip set can be obtained from the following sources:

- American Megatrends Inc.
  6145-F Northbelt Parkway
  Norcross, GA 30071
  (PH) 404-263-8181
  (FX) 404-263-9381

- Mr. BIOS™
  Microid Research
  P.O. Box 33211
  Los Gatos, CA 95031-3211
  (PH) 408-395-4096
  (FX) 408-395-8192

- Phoenix Technologies Ltd.
  40 Airport Parkway
  San Jose, CA 95110
  (PH) 408-452-6500
  (FX) 408-452-1985

There is one reason why asynchronous data SRAM's cannot be used with the HT44 and HTK340 chip set. Read miss cycle data hold time.

The HTK340 chip set does not provide the necessary data hold time on Cache read miss cycles when the HT44 needs to update the cache line with new data coming from the DRAM's. The HTK340 operates synchronously on Read Miss Cycles and removes the valid data at the same time the WE* signal is trying to latch data into the SRAM's. The race condition with asynchronous SRAM's violates the required hold time for these devices.

SYNCHRONOUS SRAM VENDORS

As of the printing date for this data book, the following SRAM manufacturers offer synchronous SRAM's compatible with the HT44.

1) IDT (Integrated Device Technology Inc.)
   Part No. IDT 71589 [32Kx9]
   2975 Stender Way
   Santa Clara, CA 95054
   Tel: 408-727-6116

2) Cypress Semiconductor
   Part No. CY7B173 [32Kx9]
   3901 North First St.
   San Jose, CA 95134
   Tel: 408-943-2600

3) Micron Technology, Inc.
   Part No. MT58C1616 [16Kx16]
   2805 East Columbia Rd.
   Boise, Idaho 83706
   Tel: 208-368-3900

4) Motorola Semiconductor
   Part No. MCM62486A [32kx9]
   3501 Ed Bluestein Blvd.
   Austin, Texas 7821
   Tel:914-473-8170