Chapter 5
Specifications

This chapter provides specifications for Headland's HT35 Mixed 3.3V/5V Single-Chip Peripheral Controller. It has three sections:

- Section 5.1, "AC Timing"
- Section 5.2, "Electrical Requirements"
- Section 5.3, "Packaging"

5.1 AC Timing

This section specifies the AC timing for the HT35. The relationship between various signals is depicted in Figures 5.1 through 5.11. The figures depict:

- Figure 5.1, "Write Cycle"
- Figure 5.2, "Read Cycle"
- Figure 5.3, "XDATA Control Timing"
- Figure 5.4, "IDE Interface Timing"
- Figure 5.5, "Serial Port Interface Timings"
- Figure 5.6, "EPP Write Cycle"
- Figure 5.7, "EPP Read Cycle"
- Figure 5.8, "RTC, Keyboard, and Mouse Interface"
- Figure 5.9, "SRAM Read Operation"
- Figure 5.10, "SRAM Write Operation"
- Figure 5.11, "ROM Read"

The numbers in Figures 5.1 through 5.11 refer to the AC timing parameters listed in Column 1 of Table 5.1.

Table 5.1
AC Timing

Parameter	*Description*	*Min (ns)*	*Typical (ns)*	*Max (ns)*
Write and Read				
1	AEN Setup Time	40		
2	AEN Hold Time	10		
3	Address Setup Time to $\overline{IOW}$, $\overline{IOR}$	40		
4	Command Pulse Width	150		
5	Write Data Setup	40		
6	Write Data Hold	10		
7	Address Hold Time	10		
8	Read Data Delay			100
9	Read Data Hold	10		60
XDATA Control				
10a	XDIRS/XDIRX Delay from XDIR Low			30
10b	XDIRS/XDIRX Delay from XDIR High			30
10c	XDIRX Delay from $\overline{IOR}$ Low			30
10d	XDIRX Delay from $\overline{IOR}$ High			30
IDE Interface				
11	Delay from Address to Enable Strobe			25
12	Delay from Address to Disable Strobe			25
13	$\overline{IDEN}$[1:0] Delay from Address			40
Serial Port Interface				
30	Delay from $\overline{IOW}$			200
31	Delay to Set Interrupt from Modem Input			250
32	Delay to Reset Interrupt from $\overline{IOR}$			250
EPP Write				
60	Command Setup Time to Data Valid			250
61	Command Hold Time to Write Inactive	0		
62	Data Hold Time to Command Inactive	50		
63	Data Setup Time to Command Inactive	100		
64	Wait Inactive to Command Inactive	0		600
65	Command Active to Wait Inactive			10
66	Command Inactive to Wait Active	0		
67	Command Active to Wait Active[1]			50

(Sheet 1 of 2)

Table 5.1 (Cont.)
AC Timing

Parameter	*Description*	*Min (ns)*	*Typical (ns)*	*Max (ns)*
EPP Read				
70	Write Inactive to Command Active	10		
71	Command Active to Data 3-state			0
72	Wait Inactive to Command Inactive			600
73	Command Inactive to Data 3-state			100
74	Command Active to Data Valid (normally Ready System)			50
75	Data Valid to Wait Inactive	0		
76	Command Active to Wait Active[1]			50
77	Command Inactive to Wait Active	0		
78	Command Active to Data Invalid	0		
79	Command Active to Wait Inactive			10
RTC, Keyboard and Mouse Interface				
80	$\overline{RC}$ Active from SX1			50
81	A20GATE Delay from SX1			60
82	MCLK, MDATA, KCLK, KDATA Active from SX1			25
SRAM Read				
85	Address Valid from $\overline{OE}$ Active			3
86	Address Delay from $\overline{OE}$ Inactive	-3.4		
87	Data Setup Time	43		0
88	Data Hold Time	-6		
89	Command Width (8 MHz)		250	
	Command Width (12 MHz)		167	
SRAM Write				
90	Address Valid to $\overline{WE}$ Active	65		5
91	Address Delay from $\overline{WE}$ Inactive	19		10
92	Data Valid to $\overline{WE}$ Active	62		
93	Data Delay from $\overline{WE}$ Inactive	19		500
94	Command Width (8 MHz)		125	
	Command Width (12 MHz)		83	
ROM Read				
95 t_{ACC}	Address to Output Delay			250
96 t_{OE}	Output Enable to Output Delay			150
97 t_{OH}	Output Hold from Addresses or $\overline{OE}$, Whichever Comes First	0		
98 t_{DF}	$\overline{OE}$ HIGH to Output Float			30

(Sheet 2 of 2)

1. This parameter is only applicable in a "Normally Ready" system in which WAIT is normally inactive and must be asserted to extend a cycle.

Figure 5.1
Write Cycle

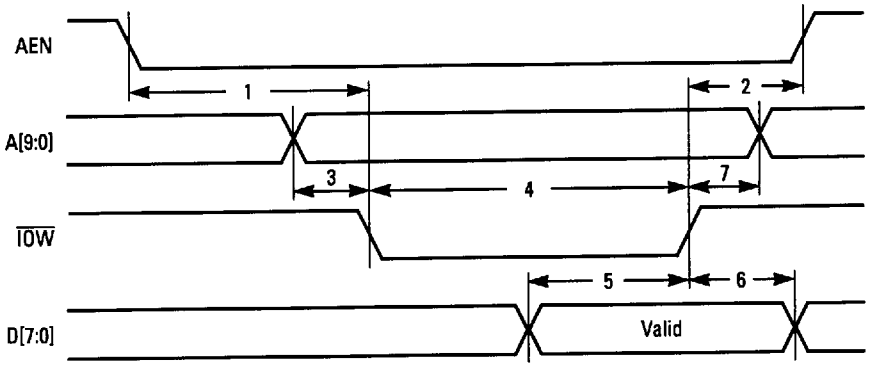


Figure 5.2
Read Cycle

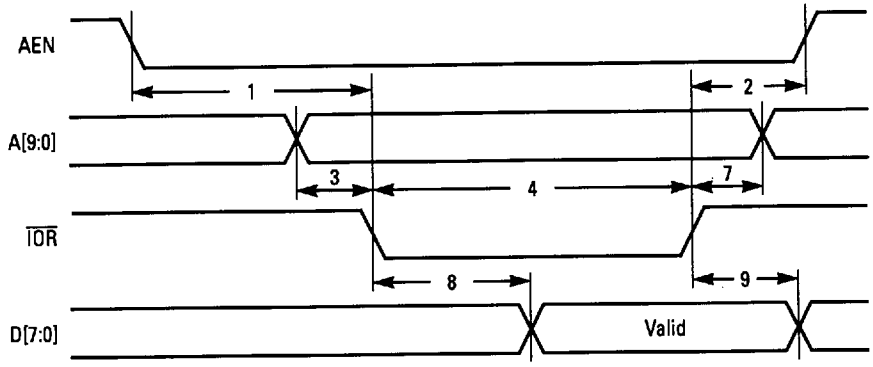


Figure 5.3
XDATA Control
Timing

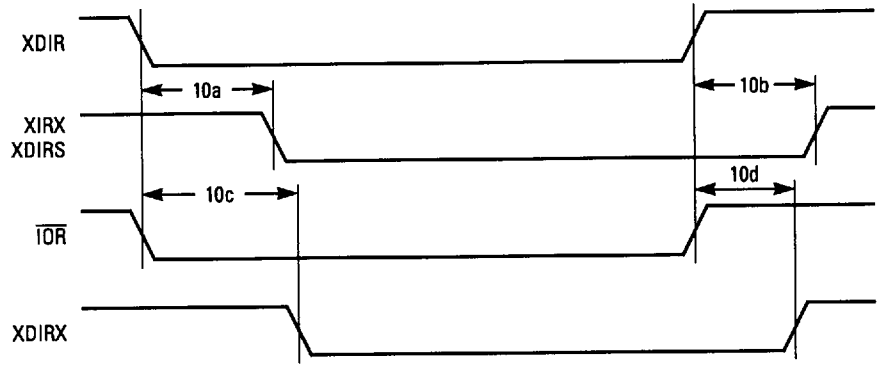


Figure 5.4
IDE Interface Timing

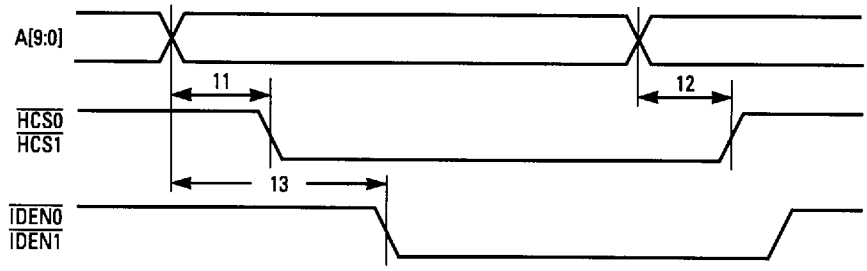


Figure 5.5
Serial Port Interface Timing

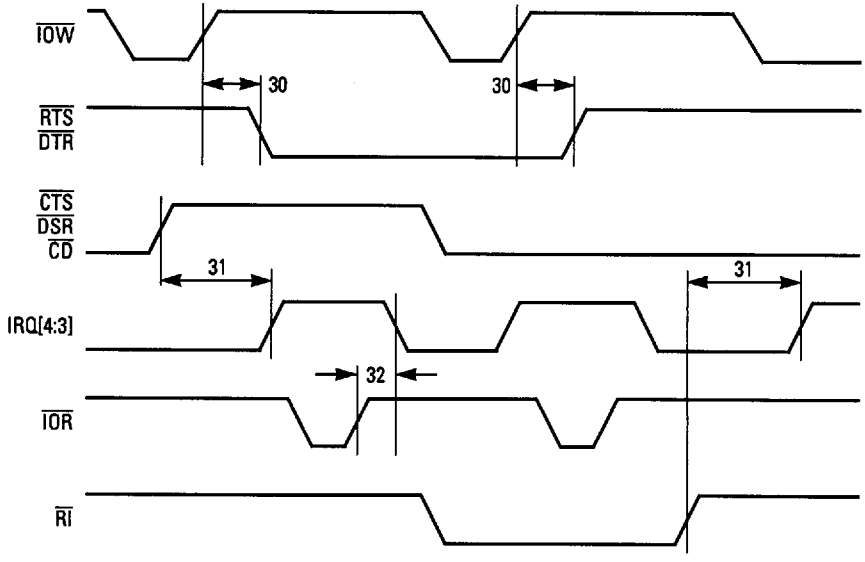


Figure 5.6
EPP Write Cycle

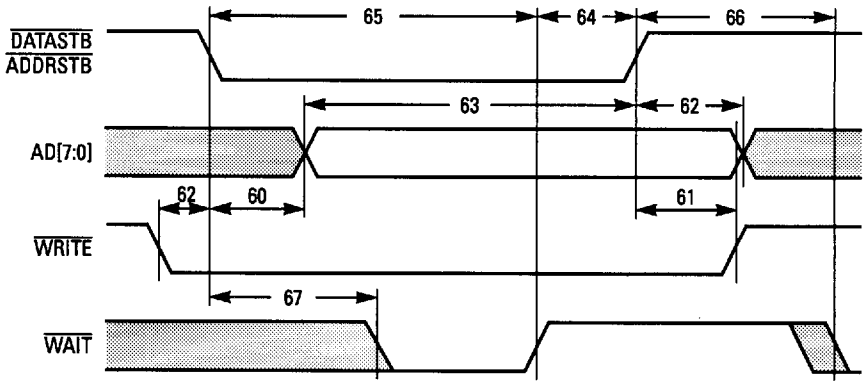


Figure 5.7
EPP Read Cycle

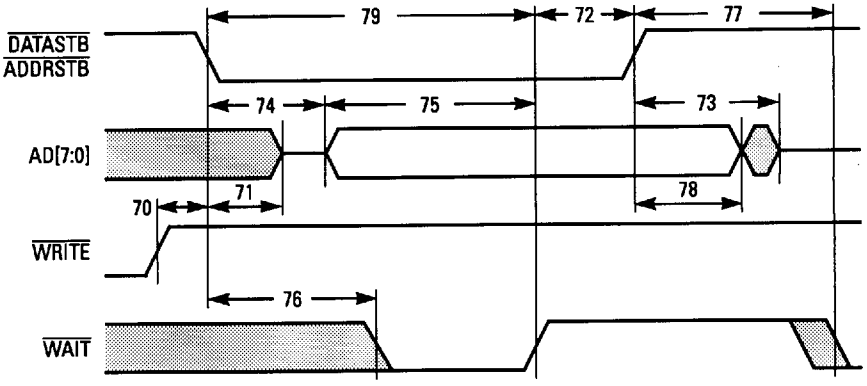


Figure 5.8
RTC, Keyboard, and
Mouse Interface

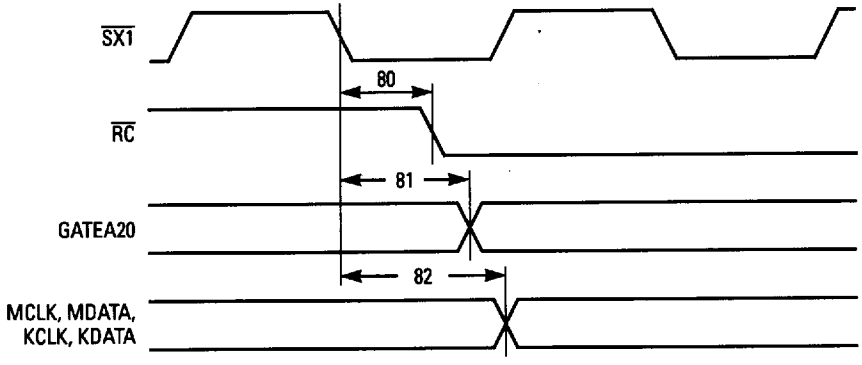


Figure 5.9
SRAM Read
Operation

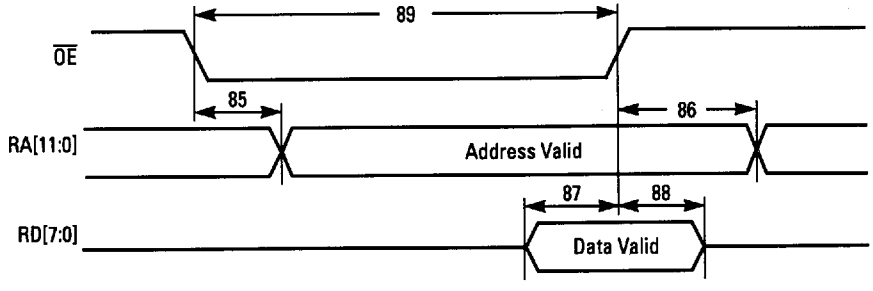


Figure 5.10 SRAM Write Operation

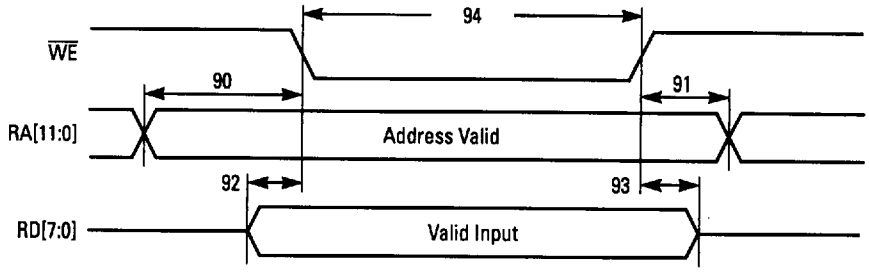
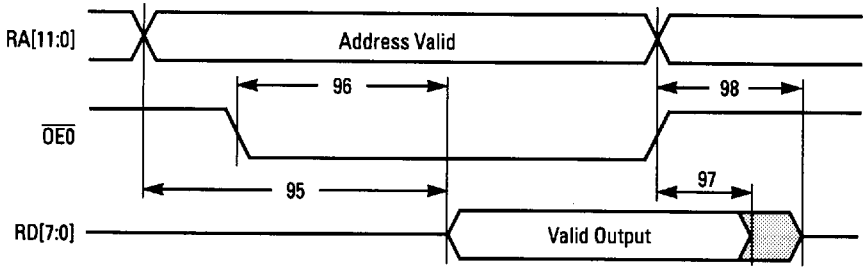


Figure 5.11 ROM Read



5.2 Electrical Requirements

This subsection specifies the electrical requirements for the HT35. Three tables list electrical data as follows:

- Table 5.2, "Absolute Maximum Ratings"
- Table 5.3, "Recommended Operating Conditions"
- Table 5.4, "DC Characteristics"

Table 5.2 Absolute Maximum Ratings

Parameter	*Symbol*	*Limits*	*Units*
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC Input Current	IIN	10	mA
Storage Temperature Range (Plastic)	TSTG	-40 to +125	°C

Table 5.3 Recommended Operating Conditions

Parameter	*Symbol*	*Limits*	*Units*
DC Supply Voltage	VDD	3 to 5.25	V
Operating Case Temperature	TC	0 to +85	°C

Table 5.4
DC Characteristics

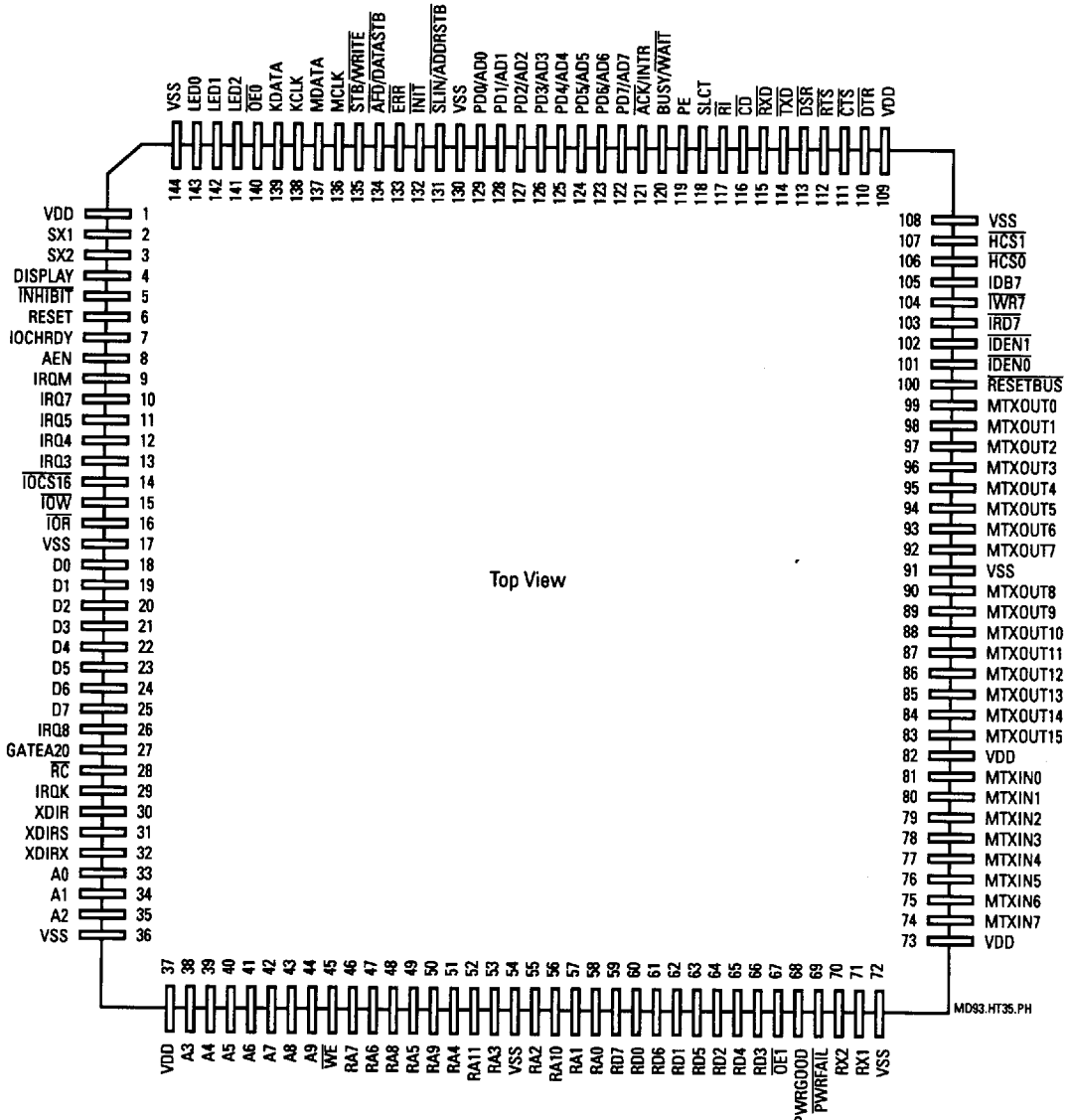
Symbol	*Parameter*	*Condition*	*Min*	*Typical*	*Max*	*Units*
VIL	Voltage Input Low				0.8	V
VIH	Voltage Input High		2			V
IIH	Input Current			1	10	uA
VOH	Voltage Output High			4.5		V
	XDIRX, XDIRS, $\overline{DTR}$, $\overline{RTS}$, $\overline{TXD}$, IRQ[4:3], IRQ8, $\overline{IDEN}$[1:0], $\overline{IWR7}$, $\overline{IRD7}$, RA0, RA[11:1], RD[7:0], $\overline{RC}$, GATEA20, IRQK, IRQM,$\overline{WE}$, $\overline{OE}$[1:0]	IOH = 2 mA				
	IOCHRDY, IRQ[5,7]	IOH = 2 mA 3-State				
	D[7:0], $\overline{HCS}$[1:0], $\overline{RESETBUS}$, IDB7	IOH = 4 mA				
	OUT[15:0]	IOH = 4 mA Open Drain				
	LED[2:0]	IOH = 6 mA				
	$\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$	IOH = 10 mA[1]				
	KDATA, KCLK, MDATA, MCLK	IOH = 12 mA				
	PD[7:0]	IOH = 12 mA[1]				
VOL	Voltage Output Low			0.4	0.8	V
	XDIRS, XDIRS, $\overline{DTR}$, $\overline{RTS}$, $\overline{TXD}$, IRQ[4:3], IRQ8, $\overline{IDEN}$[1:0], $\overline{IWR7}$, $\overline{IRD7}$, RA0, RA[11:1], RD[7:0], $\overline{RC}$, GATEA20, IRQK, IRQM, $\overline{WE}$, $\overline{OE}$[1:0]	IOL = 2 mA				
	IOCHRDY, IRQ[5,7]	IOL = 2 mA 3-State				
	D[7:0], $\overline{HCS}$[1:0], $\overline{RESETBUS}$	IOL = 4 mA				
	IDB7	IOL = 4 mA[1]				
	OUT[15:0]	IOL = 4 mA Open Drain				
	LED[2:0]	IOL = 6 mA				
	$\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, SLIN	IOL = 10 mA[1]				
	KDATA, KCLK, MDATA, MCLK	IOL = 12 mA[1]				
	PD[0:7]	IOL = 12 mA[1]				
	PWRGOOD, $\overline{PWRFAIL}$	Schmitt				
	$\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$, $\overline{CD}$, $\overline{RXD}$, $\overline{ERR}$, SLCT, BUSY, PE, $\overline{ACK}$, $\overline{IOCS16}$	–[1]				

1. When VDD = 3 volts, these inputs operate at a logic HIGH level of 5 volts and are not damaged by input of 7 volts. The HT35 operates in a system where its VDD is 3 to 3.6 volts and the rest of the system is operating at 5 volts. All inputs and outputs are CMOS logic levels. Since CMOS levels are essentially VSS to VDD, these outputs are TTL compatible at a VDD of 5 or 3.3 volts. The inputs indicated may be driven with TTL inputs when the VDD is 3.3 volts.

5.3 Packaging

Headland supplies the HT35 in a 144-pin Plastic Quad Flat Pack (PQFP) package. Figure 5.12 shows the HT35 pinout. Table 5.5 shows the HT35 pin list. Figure 5.13 shows the HT35 mechanical drawing.

Figure 5.12
HT35 Pinout



Note:
1. *NC* pins are not connected.

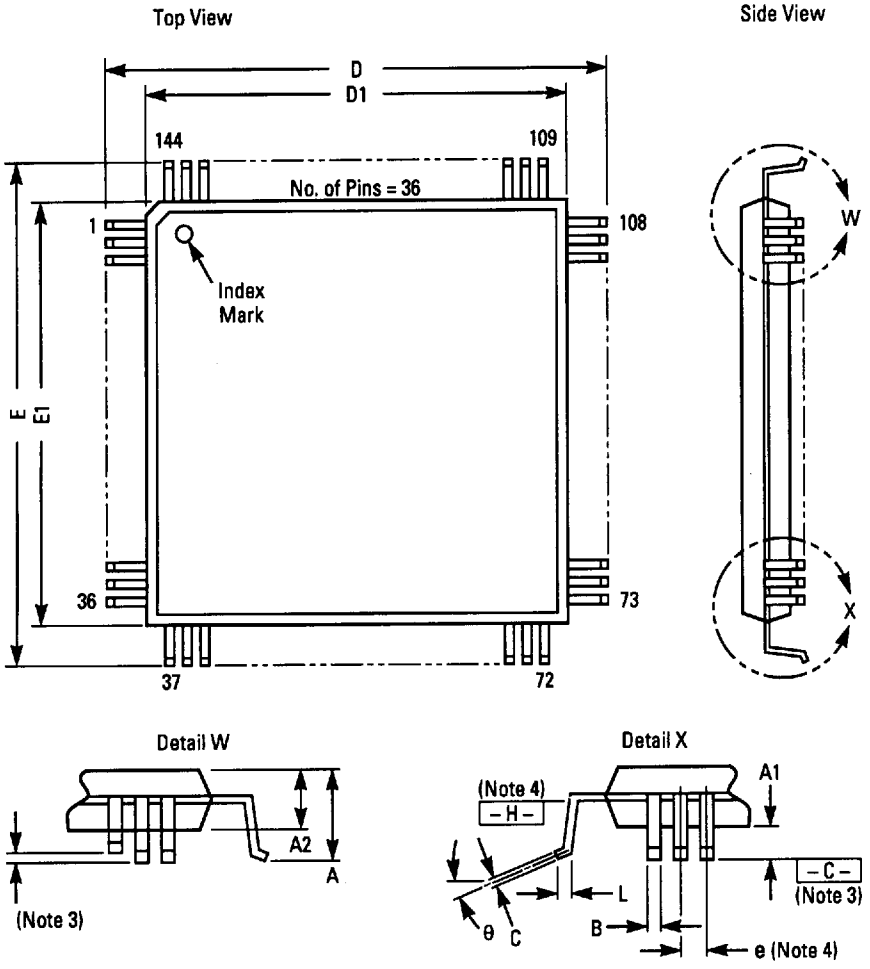
Table 5.5
HT35 Alphabetical Pin List

Signal	*Pin*	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*	*Pin*
A0	33	IOCHRDY	7	MTXOUT8	90	RD2	64
A1	34	$\overline{\text{IOCS16}}$	14	MTXOUT9	89	RD3	66
A2	35	$\overline{\text{IOR}}$	16	MTXOUT10	88	RD4	65
A3	38	$\overline{\text{IOW}}$	15	MTXOUT11	87	RD5	63
A4	39	$\overline{\text{IRD7}}$	103	MTXOUT12	86	RD6	61
A5	40	IRQ3	13	MTXOUT13	85	RD7	59
A6	41	IRQ4	12	MTXOUT14	84	RESET	6
A7	42	IRQ5	11	MTXOUT15	83	$\overline{\text{RESETBUS}}$	100
A8	43	IRQ7	10	$\overline{\text{OE0}}$	140	$\overline{\text{RI}}$	117
A9	44	IRQ8	26	$\overline{\text{OE1}}$	67	$\overline{\text{RTS}}$	112
$\overline{\text{ACK}}$/INTR	121	IRQK	29	PD0/AD0	129	RX1	71
AEN	8	IRQM	9	PD1/AD1	128	RX2	70
$\overline{\text{AFD}}$/$\overline{\text{DATASTB}}$	134	$\overline{\text{IWR7}}$	104	PD2/AD2	127	$\overline{\text{RXD}}$	115
BUSY/$\overline{\text{WAIT}}$	120	KCLK	138	PD3/AD3	126	SLCT	118
$\overline{\text{CD}}$	116	KDATA	139	PD4/AD4	125	$\overline{\text{SLIN}}$/$\overline{\text{ADDRSTB}}$	131
$\overline{\text{CTS}}$	111	LED0	143	PD5/AD5	124	$\overline{\text{STB}}$/$\overline{\text{WRITE}}$	135
D0	18	LED1	142	PD6/AD6	123	SX1	2
D1	19	LED2	141	PD7/AD7	122	SX2	3
D2	20	MCLK	136	PE	119	$\overline{\text{TXD}}$	114
D3	21	MDATA	137	$\overline{\text{PWRFAIL}}$	69	VDD	1
D4	22	MTXIN0	81	PWRGOOD	68	VDD	37
D5	23	MTXIN1	80	RA0	58	VDD	73
D6	24	MTXIN2	79	RA1	57	VDD	82
D7	25	MTXIN3	78	RA2	55	VDD	109
DISPLAY	4	MTXIN4	77	RA3	53	VSS	17
$\overline{\text{DSR}}$	113	MTXIN5	76	RA4	51	VSS	36
$\overline{\text{DTR}}$	110	MTXIN6	75	RA5	49	VSS	54
$\overline{\text{ERR}}$	133	MTXIN7	74	RA6	47	VSS	72
GATEA20	27	MTXOUT0	99	RA7	46	VSS	91
$\overline{\text{HCS0}}$	106	MTXOUT1	98	RA8	48	VSS	108
$\overline{\text{HCS1}}$	107	MTXOUT2	97	RA9	50	VSS	130
IDB7	105	MTXOUT3	96	RA10	56	VSS	144
$\overline{\text{IDEN0}}$	101	MTXOUT4	95	RA11	52	$\overline{\text{WE}}$	45
$\overline{\text{IDEN1}}$	102	MTXOUT5	94	$\overline{\text{RC}}$	28	XDIR	30
$\overline{\text{INHIBIT}}$	5	MTXOUT6	93	RD0	60	XDIRS	31
$\overline{\text{INIT}}$	132	MTXOUT7	92	RD1	62	XDIRX	32

Table 5.6
HT35 Numerical Pin List

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD	37	VDD	73	VDD	109	VDD
2	SX1	38	A3	74	MTXIN7	110	$\overline{\text{DTR}}$
3	SX2	39	A4	75	MTXIN6	111	$\overline{\text{CTS}}$
4	DISPLAY	40	A5	76	MTXIN5	112	$\overline{\text{RTS}}$
5	$\overline{\text{INHIBIT}}$	41	A6	77	MTXIN4	113	$\overline{\text{DSR}}$
6	RESET	42	A7	78	MTXIN3	114	$\overline{\text{TXD}}$
7	IOCHRDY	43	A8	79	MTXIN2	115	$\overline{\text{RXD}}$
8	AEN	44	A9	80	MTXIN1	116	$\overline{\text{CD}}$
9	IRQM	45	$\overline{\text{WE}}$	81	MTXIN0	117	$\overline{\text{RI}}$
10	IRQ7	46	RA7	82	VDD	118	SLCT
11	IRQ5	47	RA6	83	MXTOUT15	119	PE
12	IRQ4	48	RA8	84	MXTOUT14	120	BUSY/$\overline{\text{WAIT}}$
13	IRQ3	49	RA5	85	MXTOUT13	121	$\overline{\text{ACK}}$/INTR
14	$\overline{\text{IOCS16}}$	50	RA9	86	MXTOUT12	122	PD7/AD7
15	$\overline{\text{IOW}}$	51	RA4	87	MXTOUT11	123	PD6/AD6
16	$\overline{\text{IOR}}$	52	RA11	88	MXTOUT10	124	PD5/AD5
17	VSS	53	RA3	89	MXTOUT9	125	PD4/AD4
18	D0	54	VSS	90	MXTOUT8	126	PD3/AD3
19	D1	55	RA2	91	VSS	127	PD2/AD2
20	D2	56	RA10	92	MXTOUT7	128	PD1/AD1
21	D3	57	RA1	93	MXTOUT6	129	PD0/AD0
22	D4	58	RA0	94	MXTOUT5	130	VSS
23	D5	59	RD7	95	MXTOUT4	131	$\overline{\text{SLIN}}$/$\overline{\text{ADDRSTB}}$
24	D6	60	RD0	96	MXTOUT3	132	$\overline{\text{INIT}}$
25	D7	61	RD6	97	MXTOUT2	133	$\overline{\text{ERR}}$
26	IRQ8	62	RD1	98	MXTOUT1	134	$\overline{\text{AFD}}$/$\overline{\text{DATASTB}}$
27	GATEA20	63	RD5	99	MXTOUT0	135	$\overline{\text{STB}}$/$\overline{\text{WRITE}}$
28	$\overline{\text{RC}}$	64	RD2	100	$\overline{\text{RESETBUS}}$	136	MCLK
29	IRQK	65	RD4	101	$\overline{\text{IDEN0}}$	137	MDATA
30	XDIR	66	RD3	102	$\overline{\text{IDEN1}}$	138	KCLK
31	XDIRS	67	$\overline{\text{OE1}}$	103	$\overline{\text{IRD7}}$	139	KDATA
32	XDIRX	68	PWRGOOD	104	$\overline{\text{IWR7}}$	140	$\overline{\text{OE0}}$
33	A0	69	$\overline{\text{PWRFAIL}}$	105	IDB7	141	LED2
34	A1	70	RX2	106	$\overline{\text{HCS0}}$	142	LED1
35	A2	71	RX1	107	$\overline{\text{HCS1}}$	143	LED0
36	VSS	72	VSS	108	VSS	144	VSS

Figure 5.13
HT35 144-Pin PQFP
Mechanical Drawing



Dimension		mm
A	Max	4.01
A1	Min	0.25
A2	Min	3.20
	Nom	3.40
	Max	3.60
B	Min	0.22
	Max	0.38
C	Min	0.13
	Max	0.23
D	Min	30.80
	Nom	31.20
	Max	31.60
D1	Min	27.90
	Max	28.10
e	BSC	0.65
E	Min	30.80
	Nom	31.20
	Max	31.60
E1	Min	27.90
	Max	28.10
L	Min	0.73
	Nom	0.88
	Max	1.23
θ	Min	0°
	Max	7°

Note:
1. Total number of pins is 144.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code PH.

MD93.PH