LSI LOGIC

HT216-32 Local Bus VGA Controller

Features

- HT216 Local Bus VGA with 32 bit CPU data and address interface
- Fully hardware register compatible with the IBM VGA standard; BIOS compatible with EGA; hardware emulation of CGA, MDA, and Hercules graphics standards
- Direct local bus CPU interface for 80386DX™ 80486SX™, 80486DX™, and 80486DX2™
- Up to 40 MHz local bus clock rate supported
- Separate memory and dot clocks
- Hardware implementation of raster operations, destination alignment, color expansion, and cursor provide high performance in GUI environments such as Windows 3.0™
- Up to 80 MHz dot clock support
- FastWrite™ cache, CPU write FIFO, CRTC FIFO, and a prefetch queue support efficient concurrent processing at high CPU clock rates
- Resolutions up to 1024x768x256 colors non-interlaced and 1280x1024x16 interlaced supported with 1 megabyte display memory
- 72 Hz ergonomic refresh rate supported at 1024x768x256 color, non-interlaced
- Flexible memory support for 64Kx16, 256Kx4 and 256Kx16 DRAMS
- Fast page mode display memory support
- Programmable 16/32 bit memory interface
- Pin compatible with future Headland HT21X graphics products; compatible with HT216 BIOS and drivers
- Requires only 5 I.C.s for local bus design (HT216-32, 256Kx16 DRAM (2), clock generator, and RAMDAC w/comparator)
- 208 pin PQFP

General Description

The HT216-32 sets a new standard for VGA performance, once thought possible only with coprocessor/accelerator solutions. Based on the HT216, the HT216-32 offers this performance at SVGA prices by means of its local bus CPU interface and judicious use of hardware assist functions.

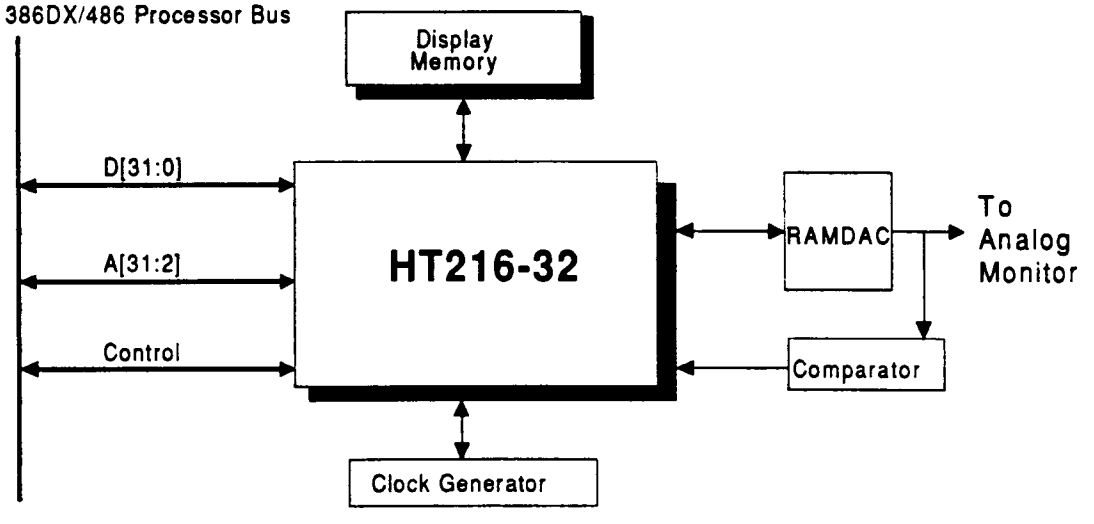

Figure 1 - Local Bus System Block Diagram

A significant performance advantage is made possible by avoiding the 8 MHz I/O bus bottleneck which constrains standard I/O bus based VGA designs. The HT216-32 is able to directly interface with 80386DX™, 80486SX™, 80486DX™ and 80486DX2™ CPUs and run at up to 40 MHz CPU clock rates. Without the I/O bus bottleneck, 386 and 486 CPUs have plenty of computing horsepower to support high performance super VGA graphics. For most PC applications, including those run under Windows 3.x, adding the additional processing power and associated cost of a coprocessor or accelerator is therefore redundant. The cost of coprocessor/accelerator based graphics solutions is significantly higher than that of standard VGA due to the higher cost of the graphics chip and the VRAM that is often required. However, cost of implementation of local bus VGA is comparable to that of I/O based SVGA.

Some local bus VGA solutions simply add a local bus interface to a design originally intended for I/O (ISA/MCA) interface. In contrast, the HT216-32 was designed from its inception to operate efficiently on the local bus. To fully realize the benefits of local bus operation requires more than just operating at the higher clock rates of the CPU local bus. Through the use of separate memory and dot clocks, the HT216-32's architecture is very different from many VGA controllers. Rather than viewing VGA merely as an integrated system with a singular task (i.e. to access display memory when necessary and provide display memory refresh), the HT216-32 VGA controller is a system with distinct distributed processing capabilities. With this approach, the HT216-32 is implemented to handle several independent tasks simultaneously, thereby increasing overall system performance.

To optimize the concurrent processing of the various internal modules, the HT216-32 has a FastWrite™ cache, an 8 deep CPU write FIFO, a sixteen deep CRTC FIFO, and a CPU read prefetch queue. These features allow each of the internal modules to operate at peak throughput and prevent the creation of any bottlenecks during asynchronous operation.

In addition to its local bus capabilities, the HT216-32 has a number of hardware assist features which also enhance its performance. These features include the hardware implementation of all Windows 3.x™ defined 256 color raster operations, fast page mode memory support, a hardware cursor, fat pixel color expansion (monochrome to color expansion), automatic source alignment to destination on CPU reads, page look ahead on all CPU operations, and a single operation read-modify-write. The performance benefits of these features are especially apparent in GUI environments such as Windows 3.x.

The HT216-32 provides a cost effective means of implementing VGA on a motherboard through its high level of integration and flexible memory architecture. An implementation of the HT216-32 may be designed with as few as five active components (HT216-32, clock generator, 256Kx16 DRAM (2), and RAMDAC w/comparator).

The memory interface supports the use of 64Kx16, 256Kx4 and 256Kx16 DRAMS, allowing flexibility in price/availability of memory used. Also, the HT216-32 is programmable to get maximum performance from 45 ns, 53 ns, 60 ns, and 70 ns fast page mode DRAM.

Architecture:

The intent of the HT216-32's architecture is to enhance the processing of asynchronous events (e.g. CPU memory reads/writes, CRTC FIFO accesses, Display Memory (DM) refresh, etc.). This requires that the VGA controller not be viewed as an integrated system with a singular task (i.e. to access DM when necessary and provide color palettes), but rather as a system which has distinct distributed processing requirements.

A block diagram of the HT216-32 is shown in figure 2. There are 5 main modules: CRT controller (CRTC), Bus Interface and I/O proces-

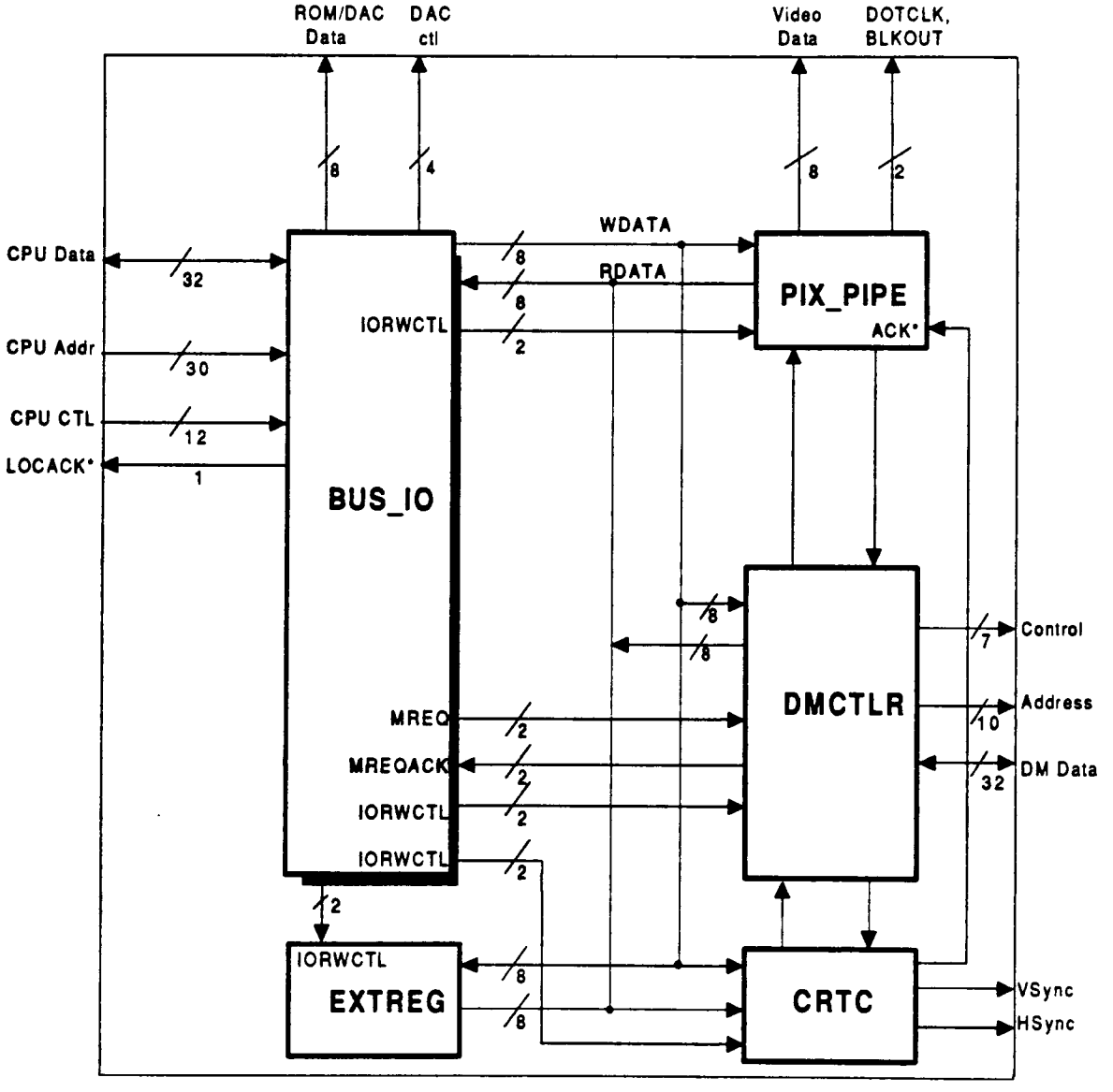

Figure 2 - HT216-32 Internal Block Diagram

sor (BUS_IO), Display Memory Controller (DMCTLR), Pixel Pipeline Controller (PIX_PIPE) and Extension Registers (EXTREG). With the exception of the EXTREG module, which has no active function, all modules operate independently. Apart from inter-communicative functions and responsibilities, all of the modules will perform their respective tasks concurrently. A further discussion of each of the modules of the HT216-32 follows.

Bus I/O Module

The BUS_IO module is responsible for interfacing with the host environment, staging all requests to, and receiving all responses from the internal modules. It also provides storage for the Miscellaneous Registers. It is designed to operate in local bus mode.

On valid accesses, the HT216-32 will assert an acknowledge (LOCACK*) to the motherboard control logic. This logic is used to indicate that the current access is to remain on the local bus rather than being sent to the I/O bus. For all requests, BUS_IO will perform the necessary address decode to determine if the currently requested operation is to be recognized by the HT216-32.

For Memory Write requests, the HT216-32 has a one deep FastWrite cache which stores the CPU address and data. This allows the processor to immediately continue and does not involve a wait condition while the current request is processed. This cached request is then synchronized and sent to the DMCTLR module for processing. When the DMCTLR module has finished processing, it will acknowledge the request, which signifies that the FastWrite cache is empty. If a second request is received from the processor before the DMCTLR has completed processing the first request, BUS_IO will place the processor in a wait state until the acknowledge for the first request has been received. When the acknowledge is received from DMCTLR, the FastWrite cache will be updated with CPU address and data for the second request and the wait condition for the CPU will be released. Then another request will be asserted to the DMCTLR. In this circumstance, the second request is pre-synchronized to minimize the length of the processor wait condition.

For Memory Read requests, the HT216-32 has a 2x32 pre-fetch queue that is used to cache a read "look-ahead". When BUS_IO receives a read request from the host, it will first check the address to determine if the currently requested data is already in the pre-fetch queue. If the data is found it will immediately be made available to the host. If the data is not found, then BUS_IO will WAIT the host, synchronize the request, and then transmit the request to the DMCTLR. The DMCTLR will read the requested data, as well as data from adjacent locations in Display Memory (with respect to the same word of the Display Memory address).

There are 4 bytes (i.e. one from each plane) from each 16-bit Display Memory address. For example: If the HT216-32 is programmed in planar graphics mode and the host requests a read from address 0xA0002, this corresponds to physical Display Memory address 0x0002. The DMCTLR will read 0x0002 first and 0x0003 second. If the host requests a read from address 0xA00F7, this corresponds to Display Memory address 0x00F7. The DMCTLR will read 0x00F7 first and then 0x00F6. At the completion of the first read, the DMCTLR will send an acknowledge to BUS_IO. Therefore the host will only be held in a WAIT condition until the completion of the read that was actually requested: The pre-fetch will be "hidden". This sequence holds true for all program models in VGA.

In planar modes, each read and pre-fetch accesses two adjacent bytes with respect to the host request; in odd/even modes it accesses 4 adjacent bytes and in chain4 modes it accesses 8. The read data from the pre-fetch queue output to the CPU is formatted as required by the plane read logic according to the standard VGA Graphics Controller register settings.

For I/O read and write requests, BUS_IO will decode the address to determine a specific decode (i.e. 0x3C2), or an index-data pair (i.e. 0x3C4,5). Apart from miscellaneous storage in the BUS_IO module, all other storage is contained in the other modules. So the BUS_IO module decodes the address and generates the specific read and write strobes and an I/O address A0 (IOA0) to be sent to the other modules. A write strobe will either write the I/O data into the index (for IOA0=0), or into the indexed data register (for IOA0=1). A read strobe will enable the tri-state data output drivers (of each of the other modules) to drive the data from the requested addresses onto a common 8-bit bus. During the read strobe where IOA0=0, the index data will be present on the bus. For I/O word operations, two back-to-back strobes are generated, the first with IOA0=0 and the second with IOA0=1.

CRTC Module

The CRTC is responsible for the generation of all signals to drive the CRT display. It is also responsible for generating addresses to the Display Memory for accessing displayed information. All horizontal timing is based on the period of the character clock. All horizontal timing registers are programmed in units of Character clocks. character clocks are an integral number of dot or pixel clocks. In the VGA standard, character clocks can be either 8 or 9 dots wide. The HT216-32 extends this to 6, 7, 8, or 9 dots.The vertical timing is based on the horizontal timing so vertical timing registers are programmed in terms of horizontal lines.

The address counter is driven by the memory clock MCLK. This ensures that the addresses to the DM are generated synchronously with the Display Memory control strobes (i.e. RAS*, CAS*, etc.) which are also generated using MCLK. In general the CRTC in the HT216-32 is similar to the standard VGA CRTC and will not be discussed in further detail here.

DMCTLR Module

The DMCTLR module is responsible for coordinating and controlling all interfacing between Display Memory and any module which requires access to Display Memory. It generates all the timing necessary to control the Display Memory itself. Since the Display Memory is the limiting resource in the system,the DMCTLR optimizes accesses to the Display Memory, while maintaining the prioritization necessary to ensure that no essential accesses are late or overlooked entirely. Here is the prioritization scheme:

> The operation in progress is the highest priority task, followed by CRTC display requests/Display Memory refresh requests, CPU memory read requests and finally CPU memory write requests.

CRTC display requests and CPU memory requests are asynchronous in nature; therefore two possible methods exist for processing these events.

First, synchronous interleaving between CPU "slots" and CRTC accesses may be forced. The average number of CRTC accesses is set at one per character. When a CPU slot becomes available and it is determined that a memory access request had been previously received, the slot will be used to process the request. The drawback to this approach is that on any given memory access request the CPU must wait for an available slot before the request can be processed. Therefore the CPU experiences an inherent average latency equal to one half of the total time between CPU slots.

The second method is to use a FIFO buffer for CRTC accesses. Once the FIFO is full, the DMCTLR is released to process other requests. When the FIFO reaches a "low water mark", it asserts a CRTC FIFO request to the DMCTLR. As rapidly as possible the DMCTLR will process this request and fill the FIFO again.

Since it is possible that a certain amount of latency will exist between the assertion of the

CRTC FIFO requests and the processing of that request, the value of the "low water mark" must take into account the maximum possible latency that can occur (i.e. in a "worst case" situation). The HT216-32 provides for that eventuality by implementing a FIFO buffer in the DMCTLR with a capacity of 16 logical DM locations. Each logical DM location is 32 bits wide and encompasses 4 planes. The FIFO is initially filled after DM refresh for every horizontal line during active vertical display, and at the end of the last line in the frame (or field in interlaced modes). During the active horizontal display period it is filled on an "as-needed" basis.

A drawback to the FIFO approach detailed above is the possibility that the CPU could experience a large latency period if a memory access request were received while the FIFO is being filled. The HT216-32 minimizes this latency in two distinct ways. For memory read requests it employs a 2-deep pre-fetch queue (See the BUS_IO section for details), and for memory write requests it employs another FIFO called the WRITE FIFO.

The function of the WRITE FIFO is to off load the processing of CPU memory write requests from immediate processing into Display Memory so the DMCTLR can wait until "dead time" to actually write data into memory. The write FIFO has 8 locations and is organized exactly as Display Memory is organized, with 4 "planes" of memory (e.g. 32 bits) and an address tag for each location.

When the BUS_IO module asserts a memory write request to the DMCTLR, the request is processed and written into the write FIFO exactly as it would be written into Display Memory (Note that this requires the VGA ALU on the input side of the write FIFO). When the memory write request has been processed, the appropriate ACKnowledge is sent to the BUS_IO module.

At any given instant, if the DMCTLR is not busy processing another task, and if the write FIFO is not empty, the DMCTLR will fill up this "dead" time by writing the contents of the write FIFO into Display Memory. Since the contents of the write FIFO are organized exactly as Display Memory is, this tends to be a very efficient operation. The inclusion of the write FIFO is the reason for the higher priority of memory reads over memory writes. The write FIFO off loads the overhead of the actual write to the Display Memory and allows the memory write request to be processed immediately without inserting CPU wait states, but a memory read request requires the CPU to be held in wait condition until the requested data has actually been read from Display Memory and is available to the CPU.

All of the storage for the Graphic Controller Register (0x3CE, F) and Timing Sequencer register (0x3C4, 5) is resident in the DMCTLR module.

EXTREG Module

The EXTREG module is responsible for the storage of the extended feature control information in the HT216-32. It is implemented as an extension to the Timing Sequencer (0x3C4, 5) at indices 0x80-0xFF. Access to these extension registers is controlled through an access enable/disable sequence written to 0x3C5 with the index set to 0x06. When a value of 0xEA is written with this index, extension access is enabled. While access is enabled a read to 0x3C5 with an index set to 0x06 will return a value of 0x01. To disable access a value of 0xAE is written to this index. A read with access disabled will return a value of 0x00.

PIX_PIPE Module

The PIX_PIPE module is responsible for reading information from the CRTC FIFO in the DMCTLR and processing and sequencing this information for display on the CRT. It combines the functions of the Attribute Controller as well as Graphic Controller pixel formatting and parallel to serial conversion as described in the standard VGA documentation. The Attribute Controller registers reside in the PIX_PIPE module. Since, under this im-

plementation the functionality of the standard VGA components is maintained, no further discussion of PIX_PIPE is necessary.

Host Interface

The host environment for the HT216-32 can vary depending upon the microprocessor. The HT216-32 has been designed to work with the Intel™ microprocessor bus. The 386DX, 486SX, 486DX and 486DX2 are supported directly. The Local Bus Application Note (part number 756-0108-02) details some of the issues concerning the use of the HT216-32 with the 486 family of microprocessors. The HT216-32 uses a 2X clock whereas the 486 uses a 1X clock.

Local Bus

The Local Bus is defined as the Address lines, Data lines and Control signals of the microprocessor. Table 1 lists the interface signals used on the local bus. As shown in table 1, there are two differences between interfacing to the 386DX and 486 microprocessors. BRDY* must be connected to the corresponding 486 pin. BRDY* and READY* are internally connected inside the HT216-32. This allows the HT216-32 to sense activity on the BRDY* pin although 486 burst mode is not supported. BOFF* is connected to the 486 BOFF* pin to allow the HT216-32 to detect a busbridged transfer initiated by the HTK340 core logic during external palette writes in cases where there is a multimedia card in the ISA slot.

386DX	486
	CPU_HLDRQ/BOFF*
A[2:31]	A[2:31]
D[0:31]	D[0:31]
ADS*	ADS*
D/C*	D/C*
M/IO*	M/IO*
W/R*	W/R*
READY*	READY*
	BRDY*
BE[0:3]*	BE[0:3]*

Table 1

A microprocessor interface block diagram for the HT216-32 is shown in Figure 3. Figure 4 details some of the functional timing relationships discussed here. The HT216-32 samples the addresses and states provided by the microprocessor during ADS*. If the address decode indicates that the address is within the VGA space then the HT216-32 generates a local bus acknowledge signal. This is an active high or low signal depending upon the local bus mode. The local bus acknowledge output signal from the HT216-32 (e.g. LOCACK*) is tied to the corresponding local bus acknowledge (e.g. LBA) input of the system logic circuitry. The system logic circuitry is the core logic chip or chip set for a PC/AT implementation. Having received the LOCACK* from the HT216-32, the system logic circuitry should ignore the present cycle and not produce a ready signal to the CPU. It must also tri-state™ the READY* to the CPU and allow the HT216-32 to control the cycle.

After sending LOCACK*, the HT216-32 takes the responsibility for sending the READY* and BRDY* signals to the microprocessor when the cycle is completed. The ready signal line has to be a shared line amongst the CPU, HT216-32 and the system logic. The HT216-32 senses activity on the READY* and BRDY* line to decipher whether the current cycle is a

pipelined or a non-pipelined cycle and to stay in synchronization with the CPU. The HT216-32 cannot sense the cycle type unless the ready line is shared. This is highlighted in the block diagram in figure 3.

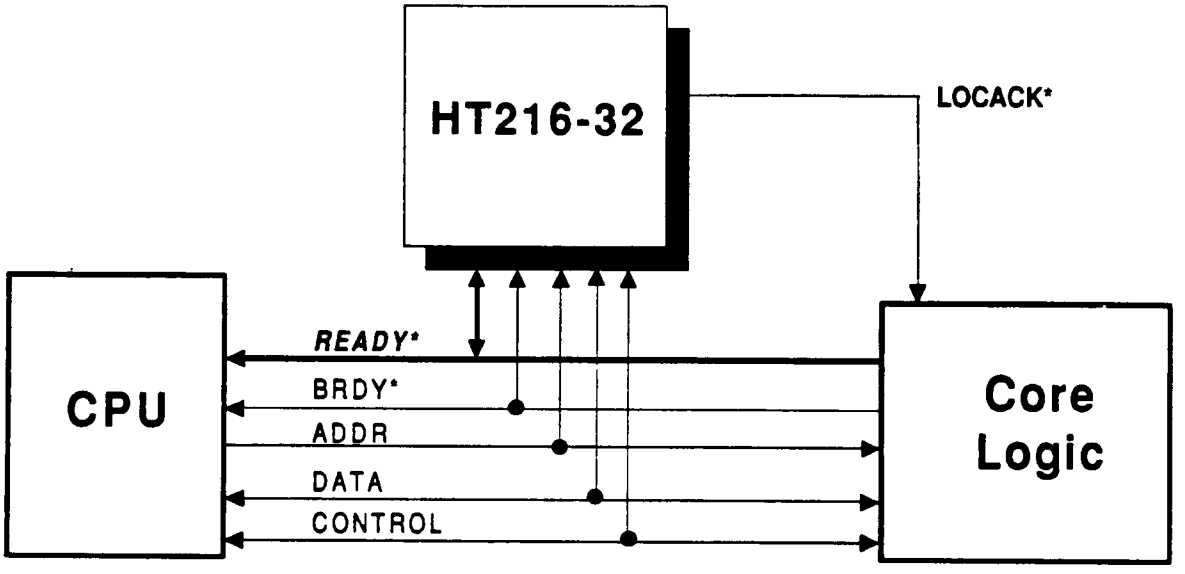

Figure 3 - Microprocessor Interface for HT216-32

The Register Description section details the MPORCTL register (port 106), which contains two bits that define three local bus acknowledge modes.

LACKMD[1:0]

00 = Synchronous Local Bus Acknowledge Mode (mode 0)

01 = Reserved (mode 1)

10 = Address Decode, active low Mode (mode 2)

11 = Address Decode, active high Mode (mode 3)

In mode 0, the LOCACK* pin is normally in high impedance state until asserted by the HT216-32. Mode 0 is thus designed to accommodate more than one device on the local bus. For example, mode 2 works with Headland Technology's HTK320 chip set and the 82C496™ chip set from Opti and the 82C486™ from VLSI Technology. The modes are shown in figure 4. Mode 3 is useful in designs that use parts such as the Austek Microcache™. This cache controller has an active high Local Bus Acknowledge (LBA) input. In mode 0, LOCACK* needs external pull-up. In mode 2 and 3, LOCACK* (or LOCACK) is always driven.

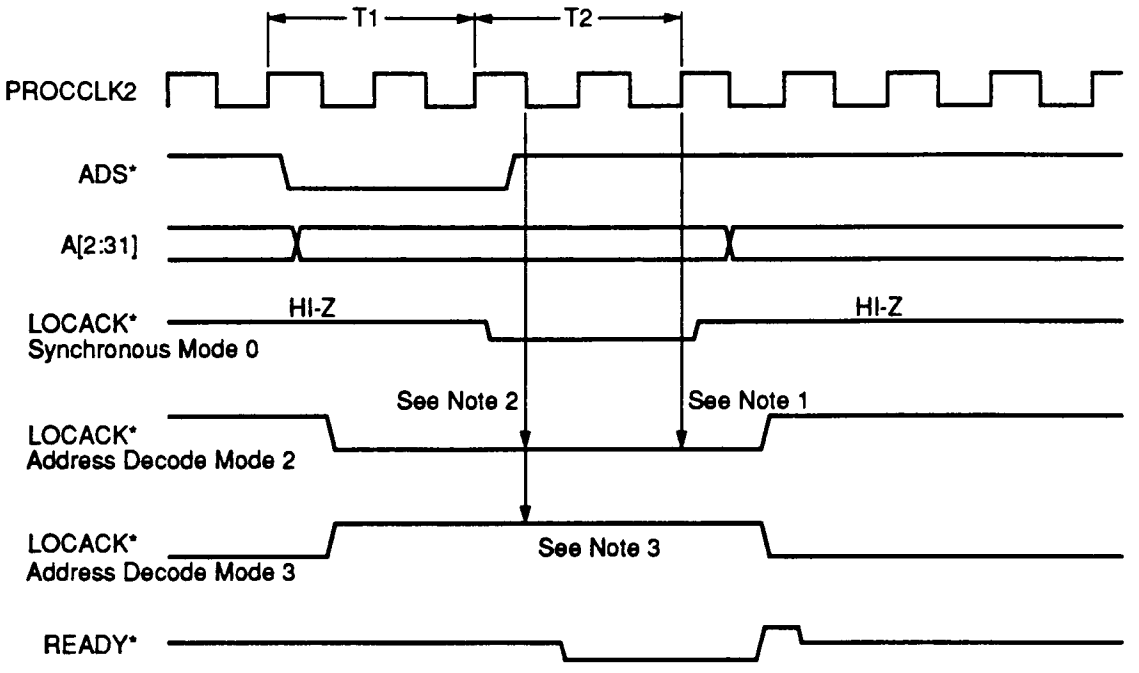

Figure 4a - HT216-32 Local Bus Acknowledge Modes

Notes 1) The HTK340 and HTK320 chips sample LOCACK here, in mode 2*
2) Elite chip set samples LOCACK here, in mode 2*
3) Austek Microcache samples LOCACK here, in mode 3

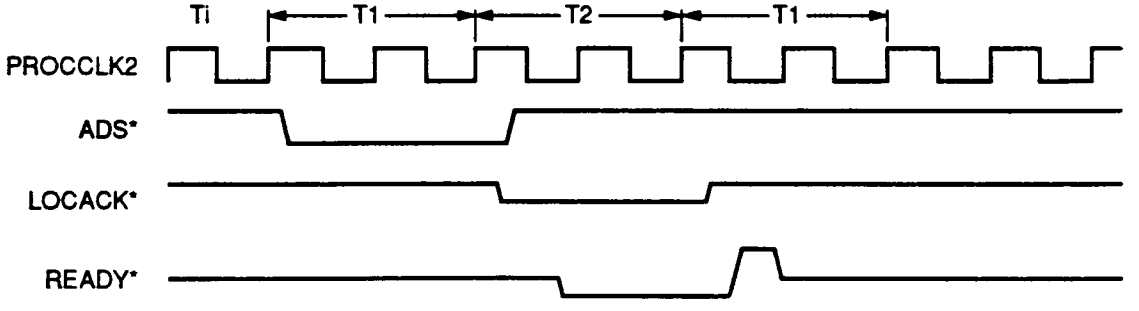

Figure 4b - HT216 -32 Zero Wait State, Non Pipelined Cycle in Mode 0

Figure 4 - Local Bus Acknowledge Modes

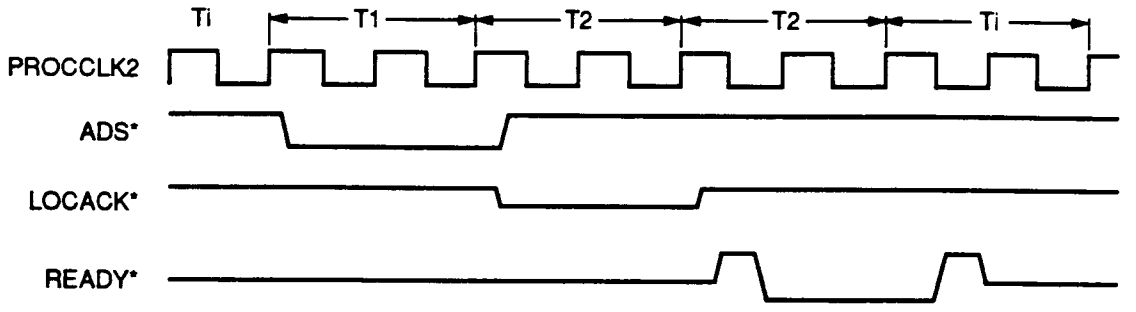

Figure 4c - HT216-32 One Wait State, Non-Pipelined Cycle in Mode 0

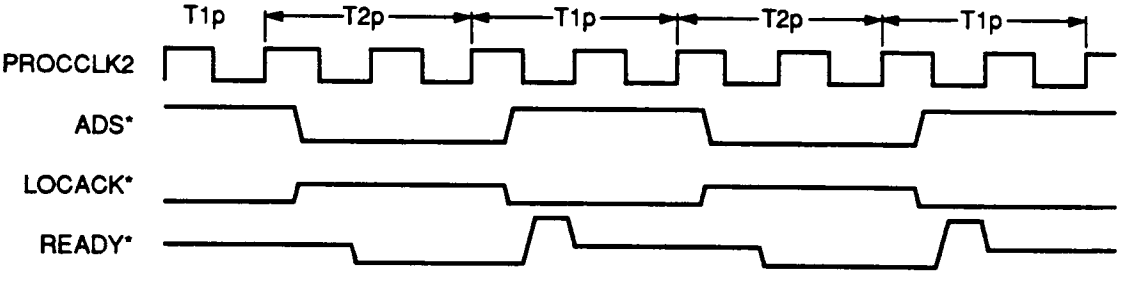

Figure 4d - HT216 -32 Zero Wait State, Pipelined Cycle in Mode 0

Figure 4 - Local Bus Acknowledge Modes (Continued)

A wide variety of system core logic chips and cache controllers exist in the market for PC/AT implementations. Three predominant considerations determine the selection of a CPU and chip set for use with HT216-32 local bus VGA:

1 - The PROCCLK2 to the HT216-32 can't exceed 80MHz.

2 - The time at which the LOCACK* (or LOCACK) signal from the HT216-32 is sampled by the core logic or the cache controller.

3 - CPU READY* and BRDY* must be shared between the HT216-32 and system core logic.

The first consideration is constrained by internal propagation delays and design. The second is dictated by the maximum time it takes for the HT216-32 to decode the address. The worst case is 14ns for mode 2 and 3. It is only after this decoding that the HT216-32 produces the LOCACK* signal. Suffice it to say that the later in the cycle the system logic samples the LOCACK*, the faster the PROCCLK2 can be for the HT216-32. Some specific cases are described here.

The Austek Microcache samples LOCACK, and the Eagle chip set from Elite™ Microelectronics, Inc. samples LOCACK*, in the middle of Phase 1 of state T2 (See figure 4a). This allows reliable operation at a PROCCLK2 of up to 80MHz.

The HT216-32 READY* signal must have access to the CPU READY* and BRDY* signals in order to remain in sync with the CPU. The preferred method is to OR-tie the READY* signals from the core logic and HT216-32 to generate the CPU READY*. The HT216-32 does not assert BRDY* but it needs to sense activity on this signal to the CPU. Therefore, BRDY* must also be connected to form a wired-OR configuration. In order for this to work properly, the core logic must relinquish control (tri-state) of the READY* signal.

The cycle definition signals D/C*, M/IO*, W/R*, BE[0:3]* and ADS* from the microprocessor are connected directly to the corresponding inputs on the HT216-32. The PROC_RST (processor reset) input on the HT216-32 is normally connected to the CPURESET signal produced by the system logic in 386DX based implementations. In 486 based implementations, the PROC_RST input pin on the HT216-32 should be connected to the 486CLK1. The RESET (system reset) input to the HT216-32 is also produced by the system logic and carries out a comprehensive reset of the internal blocks of the HT216-32. The data lines D[0:31] are connected to the corresponding inputs on the HT216-32. The address lines A[2:31] are also connected directly to the SA[2:31] inputs on the HT216-32.

HT216-32 has provision for interrupting the host during vertical retrace (non-display time). Power On Reset register 106, bit 1 in the HT216-32 allows the user a choice of edge-triggered (PC/AT type) or level sensitive interrupt. The interrupt pin can be connected directly to the IRQ9 on the system bus.

VGA Initialization

The Power On Reset (POR) registers in the HT216-32 are used to initialize functionally critical aspects of the HT216-32. There are 4 POR registers located at I/O locations 0x104, 0x105, 0x106 and 0x107. (Refer to the Register Description section for a discussion of these registers.) The POR state of the bits in these registers is determined by the logical state found on the 32 Display Memory data lines during system reset. All 32 data lines are internally pulled low. This means that in the absence of any external influence, they will be determined to have been logical 0 during POR. A pull-up resistor with a value of between 4.7K Ohms and 10K Ohms must be used to initialize any of these register bits to a logical one. POR registers correspond to the Display Memory data lines as shown below.

PORT	POR REGISTER NAME	DM LINES
0x104	DMBIMD, DM & Bus Interface Mode	B0MD[0:7]
0x105	ROMMDCTL, ROM Mode Control	B0MD[8:15]
0x106	MPORCTL, Misc. POR Control	B0MD[16:23]
0x107	VIODMRG, Variable I/O Decode Match	B0MD[24:31]

Table 3 - Power On Reset Register Listing

BIOS Interface

A VGA 'Performance' BIOS for the HT216-32 is available from Headland Technology, Inc. Most motherboard designs feature a combined system (PC/AT system) and VGA BIOS. Headland Technology offers the HTK320 chip set for the 386DX and the HTK340 chip set for the 486. These do not require any special effort to have a combined system and VGA BIOS. The top half of the EPROM contains the system BIOS and the lower half contains the VGA BIOS. No changes are required in either BIOS to achieve this.

The HTK340 or the HTK320 can be programmed to access both the System (F0000-FFFFF or E0000-FFFFF) and VGA (C0000-CFFFF) BIOS spaces in the same EPROM. See the HTK340 or HTK320 Data Sheet for further details.

Display Memory Interface

The HT216-32 can interface with 64Kx16, 256Kx4 and 256Kx16 Fast Page mode DRAMs. The 256Kx16 DRAMs must have two WE* inputs. The HT216-32 can be configured to have a 16 or 32 bit wide Display Memory data bus. In general, higher performance is achieved with a wider data bus, and a larger memory is required to support higher resolution modes. Faster memory is required to support the ergonomic modes at higher resolutions. Ergonomic modes require display refresh rates of 70 or 72 Hz. A VGA system design engineer needs to consider these issues to decide the optimum Display Memory configuration for a cost-effective implementation.

Video Mode	Memory Map		
	A0000-AFFFF	B0000-B7FFF	B8000-BFFFF
Color Text Modes 3CE:06[1:0] = 11			X
Mono Text Modes 3CE:06[1:0] = 10		X	
VGA Graphics 3CE:06[1:0] = 01	X		
Extended VGA Graphics 3CE:06[1:0] = 00	X	X	X
Hercules Emulation Enabled*		X	X

Table 4 - Display Memory Address Map

Display memory is accessible if:
Enable RAM 3C2.1=1

Note: Extended VGA graphics can be displayed when 3CE:06 [1:0] = either 01 or 00

The following sections discuss several aspects of the interface between the HT216-32 and the Display Memory.

Configurations

The following table shows allowable Display Memory configurations for the two types of DRAMs:

Option	Memory Type	# of RAS lines available	# of chips/Total memory size in bytes	
1	256K x 4	2	4/512K	8 /1M
2	256K x 16	2	1/512K	2/1M
3	64K x 16	3	2/256K	4/512K

Table 5 - Display Memory Configurations

Memory configurations are specified by the type of memory.

Bits 1 and 0 of Power On Reset Register 104 select 256Kx4, 256Kx16 or 64Kx16 DRAMs.

Note: 256Kx16 DRAMs with two WEs are supported

Connections

The HT216-32 has several pins that are designed to provide an efficient interface to the display memory. Table 6 shows these pins.

Pin Name	# of Pins
MA[9:0]	10
RAS[1:0]*	2
CAS*	1
WE[3:0]*	4
Total	17

Table 6 - Display Memory Interface Pins

These display memory signals are described in detail below:

1. RAS Connections: RAS0 from HT216-32 always drives bank 0 planes 0 and 2, while RAS 1 always drives bank 0 planes 1 and 3, This allows font data in plane 2 (IBM compatible) to be duplicated in plane 3 and interleaved for improved font access in text modes. MA9_RAS2* is used in option 3 to drive all four planes for bank 1.
2. CAS Connection: There is one CAS line from the HT216-32 that is connected to each DRAM chip.
3. WE* Connections: The four WE signals are to be connected to the numerically corresponding memory plane.
4. MA9_RAS2*: Some 256Kx16 Fast Page Mode memories require this signal to operate as the tenth memory address line. Only nine address lines are required for 256Kx4 DRAMs. Only 8 address lines are required for 64Kx16 DRAMs.
5. Minimum Memory Size: The minimum memory size required by the original IBM PC is 256K. All IBM standard modes can operate with 256K of memory. Extended modes except 1024x768x256 require 512K and 1024x768x256 requires 1 Meg.

Note: Refer to the application note (part #756-0108-02) "HT216-32 Local Bus VGA Solution" for details about the HT216-32 interface to the 256Kx4 and 256Kx16 DRAMs.

Display Memory Timing

The HT216-32 has an efficient interface to the display memory by virtue of separate pixel and memory clocks. The HT216-32 provides maximum flexibility for optimizing the interface to the DRAM chips. This is accomplished via two mechanisms. First, the HT216-32 provides a Memory Controller Timing Register, which allows for BIOS programmability of parameters t_{RAS}, t_{RP}, t_{CAS} and t_{CP} as shown in figure 5. Secondly, the HT216-32 allows for system oriented selection of the MCLK frequency which proportionally expands or contracts all memory timings.

The process of selecting values for the Display Memory Timing Register requires three steps:

(1) Select DRAM based on price/performance requirements. One has to consider the modes to be supported including ergonomic modes. The faster the DRAM the better the performance, but also the higher the price.

(2) Select MCLK frequency in conjunction with Memory Controller Timings for t_{CAS} and t_{CP}, based on the memory device's fast page mode cycle time. (t_{PC}).

(3) Select Memory Controller Timings for t_{RAS} and t_{RP} to fit minimum requirements of DRAM and MCLK selection.

The memory interface timing parameters are programmed in the Display Memory Controller Timing Control Register. Refer to the Extended Register section, index FD. Headland Technology will provide an application note detailing steps 1-3 above for determining memory clock frequencies for a given DRAM.

	Default	Range
^tRAS	5 MCLKs	4-5 MCLKs
^tRP	4 MCLKs	3-4 MCLKs
^tCAS	2 MCLKs	1-3 MCLKs
^tCP	2 MCLKs	1-2 MCLKs
MCLK Frequency	None	40-70MHZ

Table 7 - Programmable Timing Parameters (HT216-32 Reg 3C4:FD)

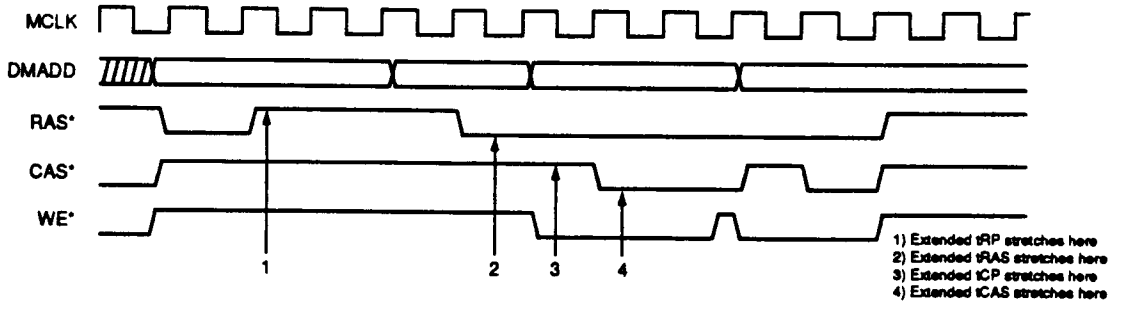

Figure 5 - Programmability of Display Memory Parameters

	53ns	60ns	70ns
^{t}RAS	53	60	70
^{t}RP	30	40	50
^{t}CAS	15	20	20
^{t}CP	10	10	10
^{t}PC	30	40	45
^{t}RC	100	110	130

Table 8 - Typical Memory Timing Parameters used to calculate MCLK

Programmable Alternative Address Decodes

Extended Linear Address Mode (XLAM): XLAM is enabled if 3C4:C8.6 = 1. When enabled the DM address space will be relocated by replacing A23 through A20 with the contents of 3C4:C9[3:0] and A31 through A24 will be replaced with the contents of 3C4:CF[7:0].

Variable I/O Decode (VIODCD): VIODCD is enabled if 107[7:0] = 00H. When enabled, all VGA Registers (normally located at 3XX) will be relocated by replacing A15 through A8 with the contents of 107[7:0] upon detection of any valid I/O access to the 3XX range.

Note: Any address that responds to only Read or Write should provide a non-responsive alternative (a "don't-care" response) to prevent hang ups.

RAMDAC Interface

Designed to work at dot clock rates of up to 80MHz, the HT216-32 supports both monochrome and color high resolution graphics and text display modes on displays such as IBM's PS/2 analog monitors and the NEC Multisync™ and Sony MultiScan™ monitors. The HT216-32 works with an external palette such as the IMSG176-80Z and IMSG176-66Z from Inmos™, which provides blanking and look-up of the 8 bits per pixel generated by the HT216-32 into a larger color set.

Clock Interface

The HT216-32 has 4 clock signal control outputs that select the external clock. ICD2047SC-20™ has been used on the HTK340/HT216-32 demonstration board as shown in the example design schematics. The 14.318 MHz clock input may be connected to the X1 input of the ICD2047SC-20 device through a 0.047 µF capacitor. This signal is generally available on all PC/AT motherboards and thus avoids the need for a separate crystal for the clock chip. Integrated Circuit Systems ICS1394-20™ and IC Designs ICD2047SC-020 are both recommended for use with a separate MCLK oscillator. ICS2474-273™ and AV9116-17™ are dual clock chips that provide the dot clock as well as the memory clock (MCLK) for the HT216-32.

Comparator Interface

The comparator is used during power up to detect the monitor type connected to the RAMDAC output. There are some RAMDACs that have the comparator integrated inside the RAMDAC chip itself. If this type of RAMDAC is used, an external comparator chip is not needed.

Port Address	VGA Port	Description
102	Setup	STUP
104	Display Memory and Bus Interface Mode	DMBIMD
105	ROM Mode Control	ROMMDCTL
106	Miscellaneous Power on Reset Control	MPORCTL
107	Variable IO Decode Match	CIODMRG
46E8h	Video Subsystem Enable	VIDSYS
3B0		
3B1		
3B2		
3B3		
3B4	CRTC Index (RW)	CRX
3B5	CRTC Data (RW)	CR0-CR3X
3B6		
3B7		
3B8		
3B9		
3BA	Feature Control (W), Display Status (R)	FC(W), STAT (R)
3BB		
3BC		
3BD		
3BE		
3BF		
3C0	Attribute Controller Index/Data (W), Index (R)	ARX, AR0-AR14
3C1	Attribute Controller Data (R)	ARX, AR0-AR14
3C2	Miscellaneous Output (W), Feature Read (R)	MISC, FEAT
3C3	Alternate Video Subsystem Enable (RW)	ALTVSE
3C4	Sequencer Index (RW)	SRX
3C5	Sequencer Data (RW) Extension Registers (RW)	SR0-SR7, ER83-ERFF
3C6	Color Palette Pixel Mask (RW)	DACMASK
3C7	Palette State (R), Color Palette Address Register Read Mode (W)	DACSTATE, DACRX
3C8	Color Palette Address Register Write Mode (RW)	DACWX
3C9	Color Palette Data (RW)	DACDATA
3CA	Feature Control (R)	FC
3CB		
3CC	Miscellaneous Output (R)	MISC
3CD		
3CE	Graphics Controller Index (RW)	GRX
3CF	Graphics Controller Data (RW)	GR0-GR7
3D0		
3D1		
3D2		
3D3		
3D4	CRTC Index (RW)	CRX
3D5	CRTC Data (RW)	CR0-CR3X
3D6		
3D7		
3D8		
3D9		
3DA	Feature Control (W), Display Status (R)	FC, STAT
3DB		
3DC		
3DD		
3DE		
3DF		

Setup Registers

Desc.	Register Name	Bits	R/W	Port (Hex)
STUP	Set Up	1	R	102
DMBIMD	DM and Bus Interface Mode	8	R/W	104
ROMMDCTL	ROM Mode Control Register	8	R/W	105
MPORCTL	Misc. POR Control Register	8	R/W	106
VIODMRG	Variable IO Decode Match	8	R/W	107
VIDSYS	Video Subsystem Enable	2	W	46E8, 56E8, 66E8, 76E8

General Registers

Desc.	Register Name	Bits	R/W	Port (Hex)	
				Mono	Color
MISC	Miscellaneous Output	7	R/W	3C2(W),3CC(R)	3C2(W),3CC(R)
FC	Feature Control	3	R/W	3BA(W),3CA(R)	3DA(W),3CA(R)
FEAT	Feature Read (Input Status 0)	4	R	3C2	3C2
STAT	Display Status (Input Status 1)	6	R	3BA	3DA(R)
DACMASK	Palette Pixel Mask	8	R/W	3C6	3C6
DACSTATE	Palette State	2	R	3C7	3C7
DACRX	Color Palette Read Mode Index	8	W	3C7	3C7
DACWX	Color Palette Write Mode Index	8	R/W	3C8	3C8
DACDATA	Color Palette Data Mode Index	8	R/W	3C9	3C9
ALTVSE	Alt. Video Subsystem Enable	1	R/W	3C3	3C3

Sequencer Index Registers

Desc.	Register Name	Bits	R/W	Index	Port (Hex)
SRX	Sequencer/Extensions Index	8	R/W	–	3C4
SR0	Reset	2	R/W	00	3C5
SR1	Clocking Mode	5	R/W	01	3C5
SR2	Plane Mask	4	R/W	02	3C5
SR3	Character Map Select	6	R/W	03	3C5
SR4	Memory Mode	3	R/W	04	3C5
SR6	Control Register	1	R/W	06	3C5
SR7	Reset Horizontal Character Counter	0	W	07	3C5

Graphics Control Registers

Desc.	Register Name	Bits	R/W	Index	Port (Hex)
GRX	Graphics Controller Index	4	R/W	–	3CE
GR0	Set/Reset	4	R/W	00	3CF
GR1	Enable Set/Reset	4	R/W	01	3CF
GR2	Color Compare	4	R/W	02	3CF
GR3	Data Rotate	5	R/W	03	3CF
GR4	Read Map Select	2	R/W	04	3CF
GR5	Graphics Mode	6	R/W	05	3CF
GR6	Miscellaneous	4	R/W	06	3CF
GR7	Color Don't Care	4	R/W	07	3CF
GR8	Bit Mask	8	R/W	08	3CF

Attribute Controller Registers

Desc.	Register Name	Bits	R/W	Index	Port (Hex)	
ARX	Attribute Controller Index	6	R/W	--/85	3C0(W)	3C1(R)
AR0-F	Palette Regs 0-15	8	R/W	00-0F	3C0(W)	3C1(R)
AR10	Mode Control	7	R/W	10	3C0(W)	3C1(R)
AR11	Overscan Color	8	R/W	11	3C0(W)	3C1(R)
AR12	Color Plane Enable	6	R/W	12	3C0(W)	3C1(R)
AR13	Horizontal Pixel Panning	4	R/W	13	3C0(W)	3C1(R)
AR14	Color Select	4	R/W	14	3C0(W)	3C1(R)

CRT Controller Registers

Desc.	Register Name	Bits	R/W	Index	Port (Hex)	
CRX	CRT Controller Index	6	R/W	--	3B4	3D4
CR0	Horizontal Total	8	R/W	00	3B5	3D5
CR1	Horizontal Display Enable End	8	R/W	01	3B5	3D5
CR2	Horizontal Blanking Start	8	R/W	02	3B5	3D5
CR3	Horizontal Blanking End	8	R/W	03	3B5	3D5
CR4	Horizontal Retrace Start	8	R/W	04	3B5	3D5
CR5	Horizontal Retrace End	8	R/W	05	3B5	3D5
CR6	Vertical Total	8	R/W	06	3B5	3D5
CR7	Overflow	8	R/W	07	3B5	3D5
CR8	Preset Row Scan	7	R/W	08	3B5	3D5
CR9	Character Cell Height	8	R/W	09	3B5	3D5
CRA	Cursor Start	6	R/W	0A	3B5	3D5
CRB	Cursor End	7	R/W	0B	3B5	3D5
CRC	Start Address High	8	R/W	0C	3B5	3D5
CRD	Start Address Low	8	R/W	0D	3B5	3D5

CRT Controller Registers(cont.)

Desc.	Register Name	Bits	R/W	Index	Port (Hex)	
CRE	Cursor Location High	8	R/W	0E	3B5	3D5
CRF	Cursor Location Low	8	R/W	0F	3B5	3D5
CR10	Vertical Retrace Start	8	W/RW	10	3B5	3D5
CR11	Vertical Retrace End	8	W/RW	11	3B5	3D5
CR12	Vertical Display Enable End	8	R/W	12	3B5	3D5
CR13	Offset	8	R/W	13	3B5	3D5
CR14	Underline Row Scan	7	R/W	14	3B5	3D5
CR15	Vertical Blanking Start	8	R/W	15	3B5	3D5
CR16	Vertical Blanking End	8	R/W	16	3B5	3D5
CR17	CRT Mode Control	7	R/W	17	3B5	3D5
CR18	Line Compare	8	R/W	18	3B5	3D5
CR1F	VGA Identification	8	R	1F	3B5	3D5
CR22	Graphics Controller Data Latch	8	R	22	3B5	3D5
CR24	Attribute Controller Index Data Latch	7	R	24	3B5	3D5
CR3x	Clear Vertical Display Enable FF	1	W	3x	3B5	3D5

Extensions must be enabled to write to extended registers, otherwise unexpected results may occur.

Extension Register Summary

Desc.	Register Name	Bits	R/W	Index	Port (Hex)
XAAI	Extended Alternate Attribute Index	7	R/W	83	3C4
PIR	Product Revision	8	R	8E	3C4
PID	Product Identification	8	R	8F	3C4
PPA	Pointer Pattern Address	8	R/W	94	3C4
PXH	Pointer Horizontal Position High	3	R/W	9C	3C4
PXL	Pointer Horizontal Position Low	8	R/W	9D	3C4
PYH	Pointer Vertical Position High	2	R/W	9E	3C4
PYL	Pointer Vertical Position Low	8	R/W	9F	3C4
GRL0	Plane 0 Background Latch	8	R/W	A0	3C4
GRL1	Plane 1 Background Latch	8	R/W	A1	3C4
GRL2	Plane 2 Background Latch	8	R/W	A2	3C4
GRL3	Plane 3 Background Latch	8	R/W	A3	3C4
CLKSEL	Extended Clock Select	4	R/W	A4	3C4
CAR	Cursor Attribute Register	3	R/W	A5	3C4
SCRAM	Scratch RAM Register	8	R/W	B3	3C4
POR0	Power On Reset 0	8	R	B4	3C4
POR1	Power On Reset 1	8	R	B5	3C4
POR2	Power On Reset 2	8	R	B6	3C4
POR3	Power On Reset 3	8	R	B7	3C4
MNLCK	Monochrome Lock	8	R/W	C0	3C4
MISCTL2	Miscellaneous Control II	8	R/W	C8	3C4

** Duplicated VGA registers also accessible as extension registers for state save/restore.*

Extension Register Summary (Cont.)

Desc.	Register Name	Bits	R/W	Index	Port (Hex)
XLAOL	Extended Linear Address Offset Low	4	R/W	C9	3C4
HOVR	Horizontal Overflow	5	R/W	CA	3C4
LWMRK	Low Water Mark Register	4	R/W	CB	3C4
DMFNCTL	DM Function Control Register	4	R/W	CC	3C4
XALUCTL	Extended ALU Function Control Register	8	R/W	CD	3C4
XALUSLT	Extended ALU Function Select Register	8	R/W	CE	3C4
XLADOH	Extended Linear Address Offset High	8	R/W	CF	3C4
MISCTL1	Miscellaneous Control I	7	R/W	E0	3C4
INTRLC	Interlace Value Register	8	R/W	E1	3C4
XCHRWD	Extended Character Width Register	5	R/W	E2	3C4
HWMRK	High Water Mark Register	4	R/W	E3	3C4
LSBA	Lower Split Bank Address Register	8	R/W	E8	3C4
USBA	Upper Split Bank Address Register	8	R/W	E9	3C4
SWSTB	Switch Strobe Register**	–	W	EA	3C4
OVSL	Overstrike Row Scan Match Value	5	R/W	EB	3C4
FGLAT0	Foreground Latch Plane 0 Register	8	R/W	EC	3C4
FGLAT1	Foreground Latch Plane 1 Register	8	R/W	ED	3C4
FGLAT2	Foreground Latch Plane 2 Register	8	R/W	EE	3C4
FGLAT3	Foreground Latch 3	8	R/W	EF	3C4
	Reserved	–	R/W	F3	3C4
	Reserved	–	R/W	F4	3C4
FBPAT	Foreground/Background Pattern Register	8	R/W	F5	3C4

Desc.	Register Name	Bits	R/W	Index	Port (Hex)
RAMBKSL	1 MByte RAM Bank Select Register	8	R/W	F6	3C4
SWRB	Switch Readback Register	8	R	F7	3C4
XCLKCTL	Extended Clock Control Register	8	R/W	F8	3C4
XPSEL	Extended Page Select Register	1	R/W	F9	3C4
XFCOLR	Extended Foreground Color Register	8	R/W	FA	3C4
XBCOLR	Extended Background Color Register	8	R/W	FB	3C4
COMCTL	Compatibility Control Register	8	R/W	FC	3C4
DMCTRL	Display Memory Controller Timing	5	R/W	FD	3C4
FBCTRL	Foreground/Background Control Register	5	R/W	FE	3C4
16INTR	16-Bit Interface Control Register	6	R/W	FF	3C4

Note: Register 8E will have different configurations depending on the Chip and the revision of that chip.

** *A byte-sized I/O write decode only; no bits of this register exist. Byte writes to this register cause the switch settings on CPU data bus bits 15-8 to strobe into the Switch Readback register (ERF7).*

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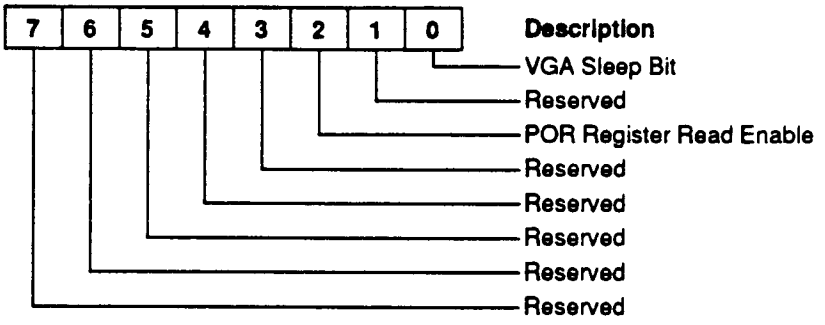
PORT	DESCRIPTION	ACCESS	NOTES
102	Setup/Adapter Enable Reg	R/W	1
104	POR Register 0 (DMBIMD)	R/W	2
105	POR Register 1(ROMMDCTL)	R/W	2
106	POR Register 2 (MPORCTL)	R/W	2
107	POR Register 3 (VIODMRG)	R/W	2
46E8	Video Subsystem Enable	W	1

Notes: *1. 102 is accessible if the HT216-32 is in setup mode (46E8.4=1).*
2. 104-7 are accessible if a value of 0x05h is written to register 102.

The HT216-32 Power On Reset (POR) registers are used to initialize functionally critical aspects of the HT216-32. There are 4 POR registers at I/O locations 0x104 - 0x107 inclusive. These registers must follow the same protocol as the standard 0x102 setup register; i.e., they can only be accessed while the HT216-32 is in set-up mode. To avoid any conflict with the standard IBM specification, a value of 0x05H must be written to the VGA setup port (0x102) before ports 104 to 107 can be accessed (either read or write), and bit 2 of port 102 is write only. Setup mode is initiated by setting bit 4 of I/O port 0x46E8 to a logical 1. POR registers 0x104, 0x105, 0x106, and 0x107 correspond to the presence or absence of external pullup resistors on the Display Memory data lines for planes 0, 1, 2, and 3 respectively, with bits 0 through 7 matching.

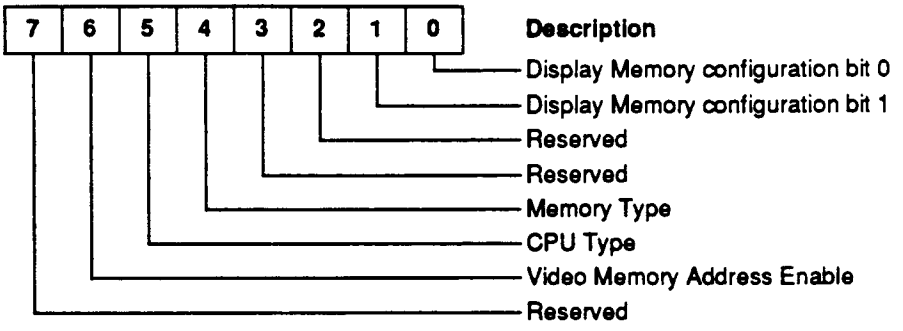
STUP Setup/Adapter Enable Register 102 R/W



This register enables memory and I/O addressing. The HT216-32 must be in setup mode (46E8.4=1) to access this register. See page 36 for a description of 46E8.

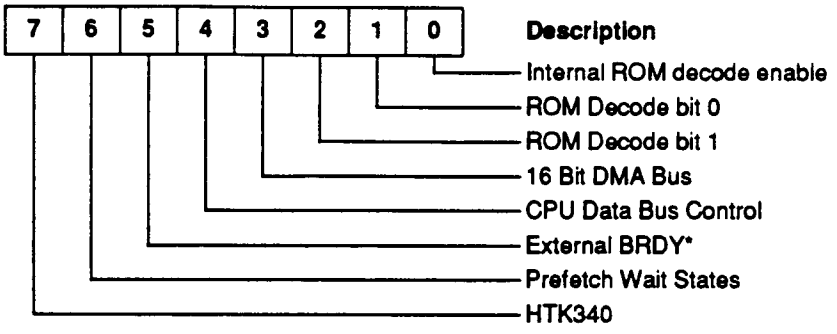
Bit	Bit Name	Description
[7:3],1		Reserved
2	PORRDE	POR Register read Enable This is a write only bit. Writing 0x05 to register 102 allows access to the Power On Reset registers 104, 105, 106 and 107.
0	VGASLP	VGA Sleep Bit 0 = Disables memory and I/O addressing (except for ports 102 and 3c3 to allow the HT216-32 to be re-enabled). 1 = Enable memory and I/O addressing.

DMBIMD — DM and Bus Interface Mode Register — 104 R



Bit	Bit Name	Pin #	Pin Name	Description
7		114	B0MD7	Reserved
6	VMASE	113	B0MD6	Video Memory Address Enable (Applicable only to HT217) 0 = VMAS_HIGH* and VMAS_LOW* not used to qualify RAM or ROM access. 1 = Use VMAS_HIGH* and VMAS_LOW* to qualify RAM and ROM access
5	CPUTYP	112	B0MD5	CPU Type 0 = 386DX 1 = 486
4	MEMTYP	111	B0MD4	Memory Type 0 = DRAM 1 = Reserved
[3:2]		110 109	B0MD3 B0MD2	Reserved Reserved
[1:0]	MEMCFG.1 MEMCFG.0	108 107	B0MD1 B0MD0	Display Memory Configuration 00 = Memories with 9 row, 9 column address ie. 256Kx4 DRAMs or 256Kx16 01 = Memories with 10 row, 8 column address ie. 256Kx16 DRAMs 10 = Reserved 11 = Memories with 8 row, 8 column address 64Kx16 DRAMs

ROMMDCTL ROM Mode Control Register 105 R/W



Bit	Bit Name	Pin #	Pin Name	Description
7	HTK340	122	B0MD15	HTK340 0 = HTK340 core logic present 1 = HTK340 core logic not present.
6	PREFETCH	121	B0MD14	Prefetch Wait States 0 = Default. Prefetch memory reads require one wait state. Used to meet CPU setup requirements at higher CPU clocks. In this mode the data bus is guaranteed not to drive the CPU data bus until the second T2 state. 1 = Zero wait states memory read cycles if the requested data is in the prefetch queue. In this mode the CPU data bus can be driven during the first T2 state.
5	XBRDY	120	B0MD13	Wait for external BRDY* 0 = (Default) Normal operation of READY* pin. HT216-32 will internally terminate its own cycles. The READY* pin will be driven low across the T2/T1 boundary, driven high for a short time then returned to tri-state (as a tri-state it will monitor ready activity on the local bus). READY* is guaranteed to be tri-stated before the end of T1. 1 = With the exception of read cycles the READY* pin timing will remain as described in bit 5 = 0. CPU read cycles will however, not be terminated until a

ready is received from the BRDY* pin. Until then the DATA bus will be driven.

BRDY* is sampled at the beginning of every T state. If the HT216-32 asserts LOCACK* BRDY* must wait until READY* becomes active before being asserted. (BRDY* can become active in the same T state as READY*, but never before).

BRDY* input is not needed for CPU write cycles. The HT216-32 will latch write data at the T state boundary on which ready is low and internally terminate the cycle. External logic must support zero wait state write cycles.

This feature can be used to increase setup times on ready to the CPU or add wait states to the HT216-32 cycles.

Note: This power up option should only be used in non-pipelined environments. This bit is Read Only.

4	CPUDTA	119	B0MD12	Tristate CPU data bus control 0 = The HT216-32 drives the entire data bus during valid reads regardless of the status of byte enable pins. For example BE = 3 (16 bit read of upper word) The HT216-32 will drive data bits 31-16 with valid data and will drive data bits 15-0 with unknown data. 1 = The HT216-32 treats the data bus as an upper and lower word. During reads only the word requested through the BE pins is driven, the other word is tristated. For example BE = 7 (8 bit read of upper word) The HT216-32 will drive data bits 31-24 with valid data, data bits 23-16 with unknown data and data bits 15-0 are tristated.

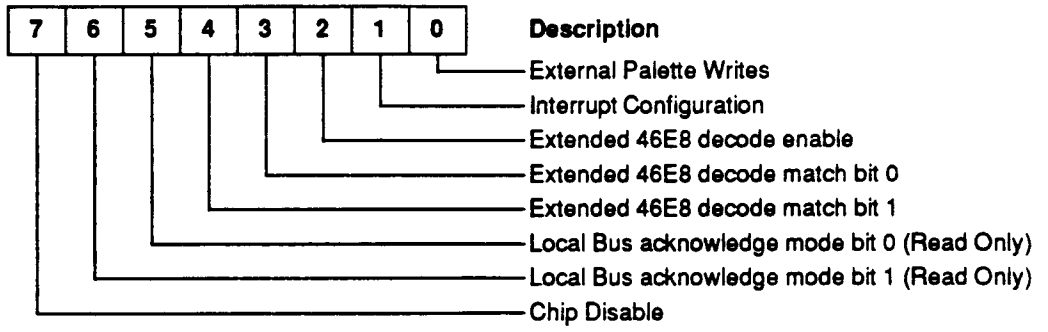
Note: If this bit is active, 105.3 must be 0. This bit is Read Only.

3	16DMA	118	B0MD11	16 bit DMA read bus bridging support 0 = External bus bridging must be used to support 16 bit DMA transfers. 1 = When this bit is set and pin 155 (CPUHLDA) is active, the HT216-32 will only allow 16 bit read transfers. The data will always be presented on the lower word of the CPU data bus (D[15:0]). The HT216-32 will internally bridge read cycles with either BE2* or BE3* active to the lower word D[15:0]. Data bus bits [31:16] will be driven with invalid data. For example: Read with BE[3:0]* = 1100. The HT216-32 will operate normally. Read with BE[3:0]* = 1011. The HT216-32 will drive data bus bits D[15:0] with data normally meant for D[31:16]. Read with BE[3:0]* = 1100. The HT216-32 will drive data bus bits D[15:8] with data normally meant for D[31:24].

Note: If this pin is active 105.4 must be 0.
While this bit is set BE1 and BE2* must never both be set to 0.*

2:1	ROMDCD.1 ROMDCD.0	117 116	B0MD10 B0MD9	ROM Decode 00 = decode at 0xC0000 to 0xC5FFF 01 = decode at 0xC0000 to 0xC5FFF and 0xC6800 to 0xC7FFF 10 = decode at 0xC0000 to 0xC7FFF 11 = Reserved
0	IROMDCDE	115	B0MD8	Internal ROM LOCACK Enable 0 = ROM LOCACK disabled. (default) 1 = ROM LOCACK enabled

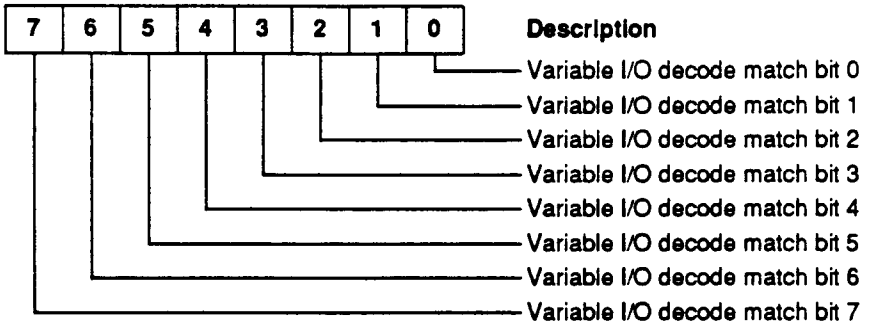
MPORCTL Misc. POR Control Register 106 R/W



Bit	Bit Name	Pin #	Pin Name	Description
7	CHIPDIS	131	B0MD23	Chip Disable 0 = HT216-32 enabled. 1 = HT216-32 disabled.
[6:5]	LACKMD.1 LACKMD.0	129 128	B0MD22 B0MD21	Local Bus acknowledge (Read Only) 00 = Synchronous Local Bus acknowledge 01 = Reserved 10 = Address Decode Active low 11 = Address Decode Active high
Note: These bits are read only.				
[4:3]	E46E8DM.1 E46E8DM.0	127 126	B0MD20 B0MD19	Extended 46E8 Decode Match 00 = decode 46E8 register at 0x46E8 01 = decode 46E8 register at 0x56E8 10 = decode 46E8 register at 0x66E8 11 = decode 46E8 register at 0x76E8

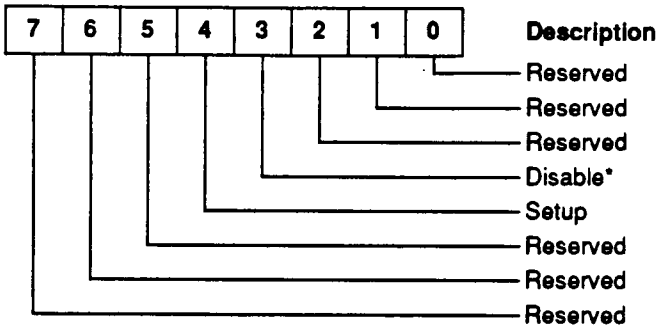
Bit	Bit Name	Pin #	Pin Name	Description
2	E46E8E	125	B0MD18	Extended 46E8 Decode Enable 0 = use normal VGA decode for 46E8 1 = use bits [4:3] to determine specific I/O decode address for register 46E8.
1	INTCONFG	124	B0MD17	Interrupt Configuration 0 = Edge triggered (AT bus type) interrupt 1 = Level triggered interrupt
0	XPALWR	123	B0MD16	External Palette Writes 0 = Disabled 1 = Enabled

VIODMRG Variable I/O Decode Match Register 107 R/W



Bit	Bit Name	Pin #	Pin Name	Description
[7:0]	VIODCDM.7	139	B0MD31	Variable I/O Decode
	VIODCDM.6	138	B0MD30	When Register value is 0 (default) I/O responds at
	VIODCDM.5	137	B0MD29	normal VGA addresses of 03xx. If any other value
	VIODCDM.4	136	B0MD28	is programmed then this value will be substituted
	VIODCDM.3	135	B0MD27	for address bits [15:8] for I/O decodes. This allows
	VIODCDM.2	134	B0MD26	relocation of I/O decode space.
	VIODCDM.1	133	B0MD25	If VIODCM [7:0] = 03 then VGA decode = 0x03y
	VIODCDM.0	132	B0MD24	If VIODCM [7:0] = 02 then VGA decode = 0x02y
				If VIODCM [7:0] = 87 then VGA decode = 0x87y
				where y = Programmable VGA specific decodes,
				0x03C4, 0x3B5, etc.

VIDSYS — Video Subsystem Enable — 46E8 (W)



This register is used to control access to the memory and I/O addresses of the HT216-32.

Bit	Bit Name	Description
4	SETUP	Setup Mode This bit is used to put the HT216-32 into set up mode. 0 = Accesses to port 102 are ignored. 1 = Puts HT216-32 in setup mode and enables access to port 102. Setting port 102 bit 0 = 0 disables memory and I/O addressing (except for ports 102 and 3C3, which allow the HT216-32 to be re-enabled.)
3	DISABLE*	Disable The complement of this bit is used to internally drive the HT216-32 DISABLE pin. 0 = All video memory and I/O port accesses with the exception of port 46E8 will be disabled. Video data continues to be driven to the RAMDAC and monitor. 1 = Enable all video memory

I/O Port 46E8

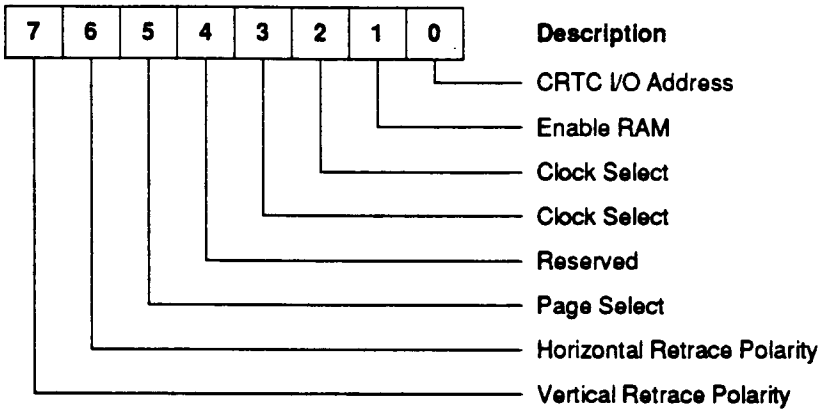
Port Address	106.2	106.4	106.3
[4:7]6E8	0	-	-
46E8	1	0	0
56E8	1	0	1
66E8	1	1	0
76E8	1	1	1

HT216-32 is designed to accommodate up to 4 co-resident VGA implementations. These implementations can exist at port addresses 46E8, 56E8, 66E8 and 76E8. Power On Reset register 106 bits 2, 3 and 4 determine the port address that controls access to the I/O and memory addresses of the HT216-32.

Each General Register contains a separate port address to allow direct programming access.

Desc.	Register Name	Bit	R/W	Index	Ports	
					Mono	Color
MISC	Miscellaneous Output	7	R/W	–	3C2(W),3CC(R	3C2(W),3CC(R)
FC	Feature Control	3	R/W	–	3BA(W),3CA(R	3DA(W),3CA(R)
FEAT	Feature Read (Input Status 0)	4	R	–	3C2	3C2
STAT	Display Status (Input Status 1)	7	R	–	3BA	3DA
DACMASK	Palette Pixel Mask	8	R/W	–	3C6	3C6
DACSTATE	Palette State	2	R	–	3C7	3C7
DACRX	Color Palette Read Mode Index	8	W	–	3C7	3C7
DACWX	Color Palette Write Mode Index	8	R/W	–	3C8	3C8
DACDATA	Color Palette Data Register	6	R/W	–	3C9	3C9
ALTVSE	Alt.Video Subsystem Enable	1	R/W	–	3C3	3C3

MISC Miscellaneous Output Register 3CC(R) 3C2(W)



The functions in this register include setting the polarity of horizontal and vertical retrace signals and the video clock source. This register is written to 3C2 and can be read back at 3CC.

Bit	Description
7	Vertical Retrace Polarity 0 = Selects active high 1 = Selects active low
6	Horizontal Retrace Polarity 0 = Selects active high 1 = Selects active low
5	Page Select 0 = Selects odd memory locations 1 = Selects even memory locations This bit is the LSB of the display memory address when in 'Odd/Even' modes (Sequencer Reg4 bit 2 = 1). It is set for modes 0, 1, 2, 3 and 7 (text modes). This bit has no effect if Chain (Graphics Reg 6 bit 1) Mode is enabled.
4	Reserved (reads back 0)

[3:2] Clock Select

If Extension Register F8 bit 1 = 0 , then use table 7 - Clock Select Source Settings.

Bit-3	Bit-2	Extension Reg. A4 bit 4 = 0	Extension Reg. A4 bit 4 = 1
0	0	25.175MHz	50.350MHz
0	1	28.322MHz	65.000MHz
1	0	Feature Connector	Feature Connector
1	1	0MHz	40.000 MHz

Table 7 - Clock Select Source Settings

If Extension Register F8 bit 1 = 1, then CLKCTRL[0:3] are outputs that drive selects on a programmable clock chip. The CLKCTRL pins are driven by port 3C2 bit 2, 3C2 bit 3 and Extension register A4 bit 4 and 5 respectively. The clock chip must drive the input with a 25.175MHz clock during power-up for the HT216-32 to be properly initialized.

Note: All Clock Select bits (3C2 bit[3:2], Extension Register A4 bit 4, 5 and Extension Register F8 bit 1) should only be changed during synchronous reset (SR0 bit 1 = 0) or display memory contents may be corrupted.

1 Enable RAM

0 = Disables processor access to Display RAM

1 = Display RAM responds at addresses set by the value programmed to the Control Data Select of the Graphics Controller.

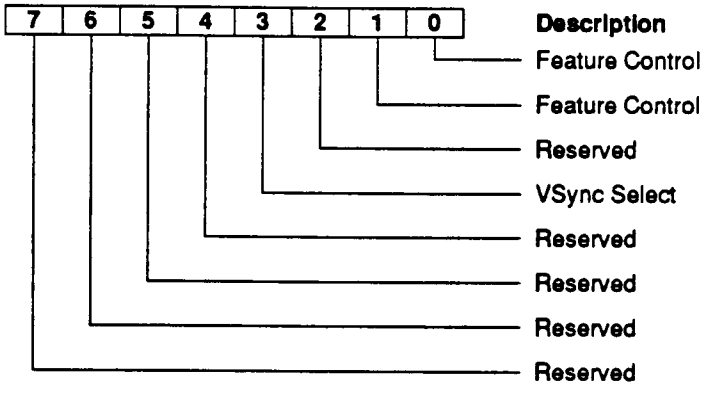
0 CRTC I/O Address

0 = Sets the CRTC to 3Bx and the Input Status Register 1 to 3BA for monochrome mode.

1 = Sets the CRTC to 3Dx and the Input Status Register 1 to 3DA for color mode.

This bit selects I/O addresses for monochrome (3Bx) or color mode (3Dx). The following registers are affected by this bit: the Display Status Register, the Feature Control Register, the CRT Controller Index Register and the CRT Controller Data Register.

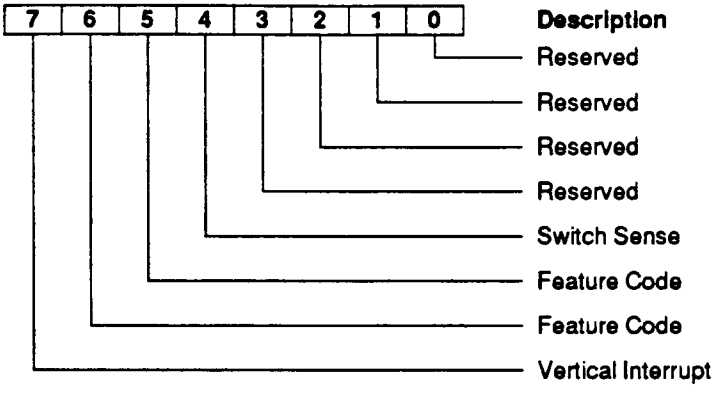
FC Feature Control Register 3BA/3DA(W) 3CA(R)



This register is write only. Reading I/O port 3BA/3DA returns the contents of the Display Status Register. For state save/restore and VGA compatibility, this register can be read at I/O port 3CA.

Bit	Description
3	Vertical Sync Select 0 = Enables normal vertical sync output to the monitor. This bit should always be set to 0. 1 = Output is the logical OR of vertical sync and vertical display enable.
[1:0]	Feature Control These bits drive the Feature Control 1 and Feature Control 0 pins of the Feature connector.

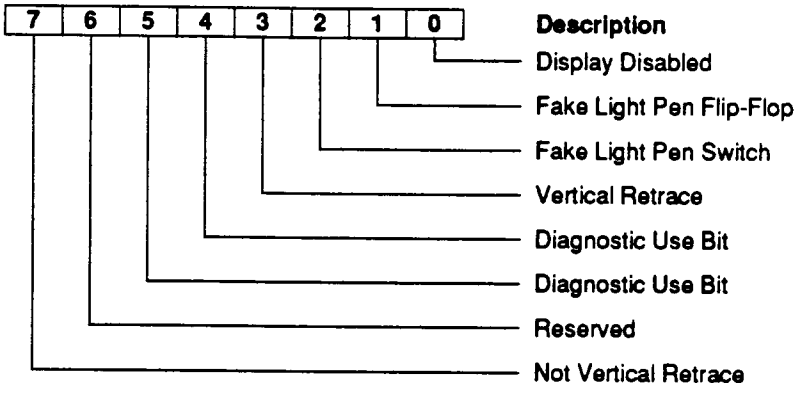
FEAT Feature Read Register(Input Status 0) 3C2(R)



This register is read only. It reads two pin locations on the Feature Connector plus Switch Sense and Vertical Interrupt.

Bit	Description
7	Vertical Interrupt 0 = No interrupt is pending 1 = An interrupt is pending
Note:	*When set to 0, Controller Register 11 bit 5 enables CRT Interrupts to occur at the leading edge of vertical sync. The interrupt is normally connected to IRQ2 in a PC/AT.*
[6:5]	Feature Code These bits are input from the feature connector as feature code. These bits read back as 1 if nothing is connected to the feature connector.
4	Switch Sense This bit returns the state of the SWITCH pin. The SWITCH pin is connected to the output of the monitor ID comparator.

STAT Display Status Register(Input Status 1) 3BA/3DA (R)



This register is read only at 3BA/3DA and sets the Attribute Controller index/data toggle to index state.

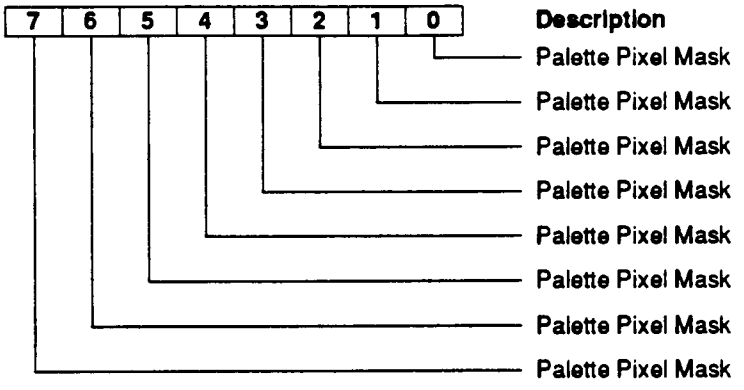
Bit	Description
7	Not Vertical Retrace 0 = Vertical Retrace is active 1 = Vertical Retrace is inactive
[5:4]	Diagnostic These bits are connected to 2 of the 8 outputs of the Attribute Controller (Video[0:7] output data during display periods and overscan color during non-display periods). Selection of one of the four pairs of bits is controlled by bits[5:4] of Color Plane register Attribute Reg12.

Color Plane Register		Display Status (HT216-32)	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Input Status Diagnostic Use Settings

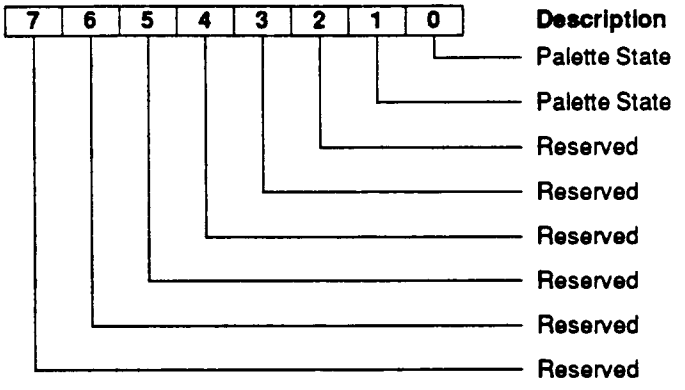
3	Vertical Retrace 1 = Vertical retrace in progress
2	'Fake' Light Pen Switch This bit always reads as 1 since the light pen is not implemented in the HT216-32.
1	'Fake' Light Pen Flip-Flop This bit always reads as 0 since the light pen is not implemented in the HT216-32.
0	Display Disabled 0 = Display of video data is enabled 1 = Vertical or horizontal retrace interval is in progress

DACMASK Palette Pixel Mask Register 3C6 R/W



This register is located in the Color Palette chip. The contents of this register are ANDed with the 8 bits of video data coming into the Color Palette to allow displayed colors to be altered without changing display memory or the contents of the Color Palette. Rapid animation, overlays and flashing objects can be produced by partitioning color information by one or more bits in the color palette.

DACSTATE Palette State Register 3C7 (R)



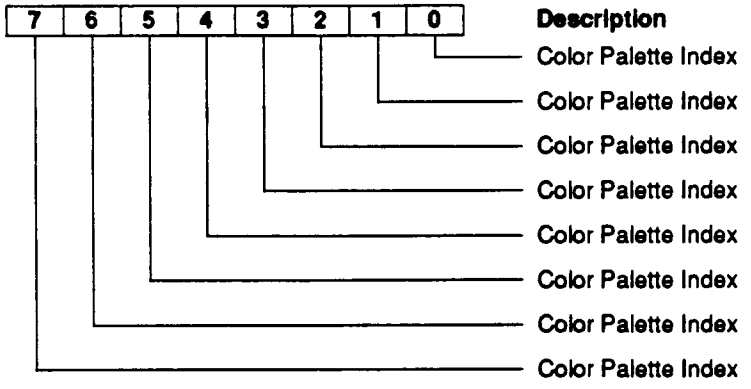
Registers 3C6-3C9 are generally implemented in the color palette chip. However, in the HT216-32 Register 3C7 is internal to the chip. The Color Palette chip automatically increments the index register when the index is written at 3C7 or 3C8.

Automatic incrementing is used to save and restore the color values and eliminates the need to reload the index every three bytes. The index value is written to this register and saved in an internal register where it is automatically incremented. The save register is used to point at the current data register until the 3-byte read sequence is completed. When the blue value is read, the save register is updated and incremented again. The entire palette (or any subset) is read by writing the index of the first color in the set, then reading the values for each color.

This register is used to write index to read color data values. Port 3C8 is used to index the write color data values. The index is read back at 3C8 only. Read accesses to this register are intercepted and substituted by the DACSTATE register contents. Certain information, such as whether the chip is being read or written to, is required for saving and restoring the state of the video system during interrupt service. Data values must therefore be accessed in 3-byte sequences. When a color palette register is written, any 3-byte read or write sequence in progress is aborted and a new one is started.

Bit	Bit Name
[1:0]	Palette State These bits are the low-order bits of the last I/O write to ports 3C6-3C9. 00 - The last I/O write was to 3C8, the color palette 'write-mode' index register 11 - The last I/O write was to 3C7, the color palette 'read-mode' index register

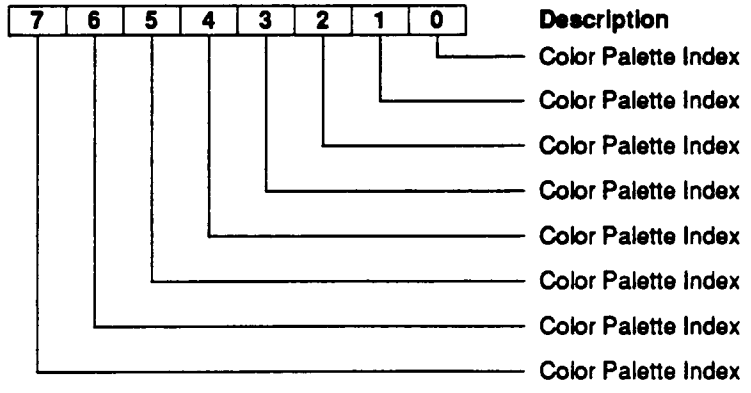
DACRX Color Palette "Read Mode" Index 3C7(W)



Contains the index value for read access to the 256 registers in the Color Palette. These registers are 18 bits in length (6 bits each for red, green and blue). Each register is accessed as a sequence of 3 bytes located in color palette (RAMDAC).

Note: See DACSTATE 3C7 (R) for a description of how this register functions.

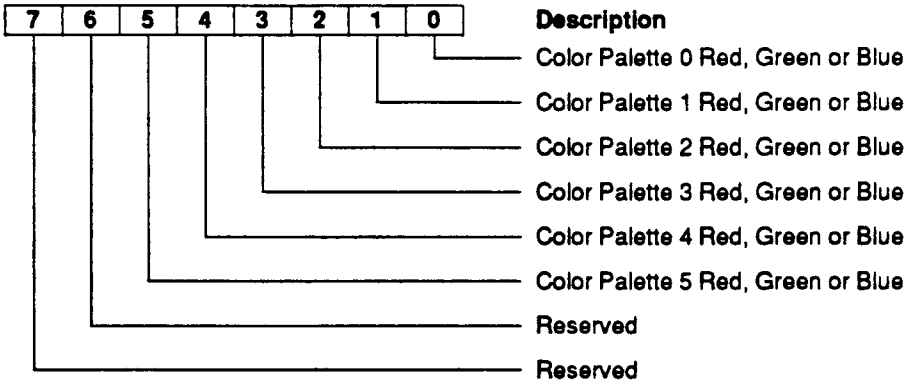
DACWX Color Palette "Write Mode" Index 3C8 R/W



This register contains the index value for write access to the 256 registers in the Color Palette. These registers are 18 bits in length (6 bits each for red, green and blue). Each register is accessed as a sequence of 3 bytes located in color palette (RAMDAC).

Note: See DACSTATE 3C7 (R) for a description of how this register functions.

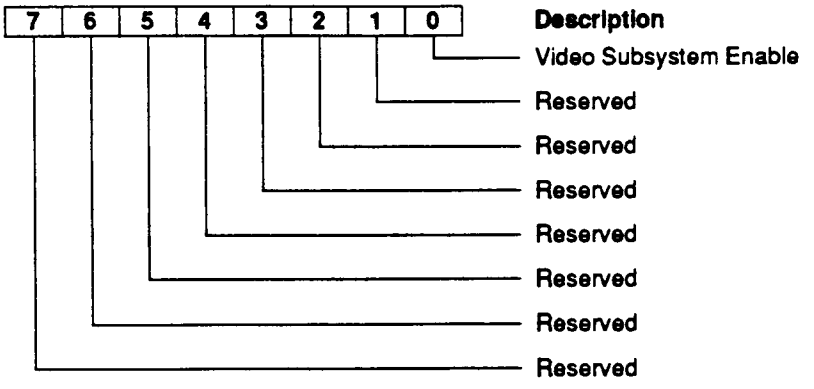
DACDATA Color Palette Data Registers 3C9 R/W



The Color Palette registers are 18 bits in length (6 bits each for red, green and blue). Each register is accessed as a sequence of 3 bytes. After writing the index to the DACRX, or DACWX register (port 3C7 or 3C8), data values are read from or written to port 3C9 in sequence: 1) red, 2) green, 3) blue. The index register is automatically incremented for each 3 byte set, allowing multiple color registers to be read from or written to and eliminating the need to reload the index every three bytes located in color palette (RAMDAC).

Note: See DACSTATE 3C7 (R) for a description of how this register functions.

ALTVSE — Alternate Video Subsystem Enable — 3C3 R/W



This register enables memory and I/O addressing. The HT216-32 must be in setup mode (46E8.4=1) to access this register.

Bit	Description
Bit 0	VGA Subsystem Enable 0 = Disables memory and I/O addressing (Ports 102 & 3C3 are not disabled to allow the HT216-32 to be re-enabled.) 1 = Enables memory and I/O addressing

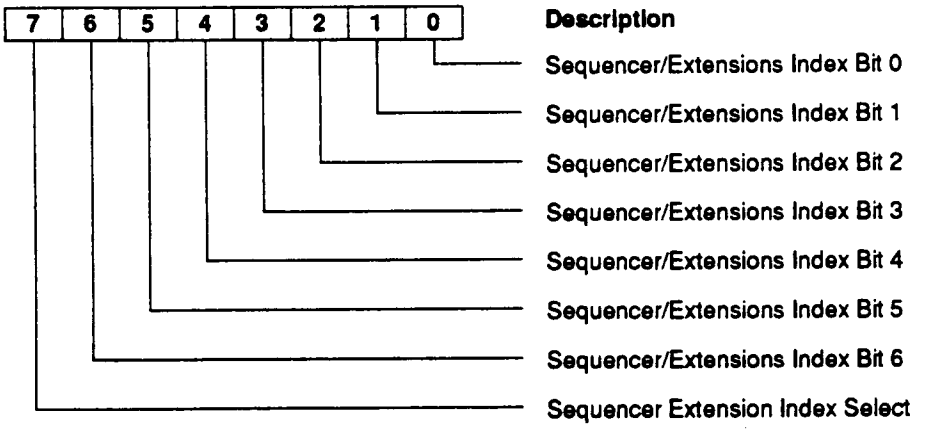
Note: In PC/AT systems where the VGA is implemented as an optional board (for installation in a slot on the bus), the HT216-32 is put into setup mode by 46E8 bit 4. In PS/2 Systems where the VGA is implemented as a standard feature (as part of the motherboard logic), the HT216-32 is put into setup mode by I/O port 94 bit 5.

The Sequencer Registers generate all memory timing for the display RAMs and the character clock for controlling display memory refresh reads. Timings controlled by the Sequencer registers include horizontal count resolution, dot clock, and video load control. There are nine read/write Sequencer Registers including one index register and eight data registers. Two addresses are used: the index address (3C4) selects a data register, and the data address (3C5) reads or writes data to the selected data register.

Sequencer Index Registers

Desc.	Register Name	Bits	Access	Index	Port
SRX	Sequencer/Extensions Register Index	8	R/W	--	3C4
SR0	Reset Register	8	R/W	00	3C5
SR1	Clocking Mode	5	R/W	01	3C5
SR2	Plane Mask	4	R/W	02	3C5
SR3	Character Map Select	6	R/W	03	3C5
SR4	Memory Mode	3	R/W	04	3C5
SR6	Control Register	1	R/W	06	3C5
SR7	Reset Horizontal Character Counter	0	W	07	3C5

SRX Sequencer /Extensions Register Index 3C4 R/W



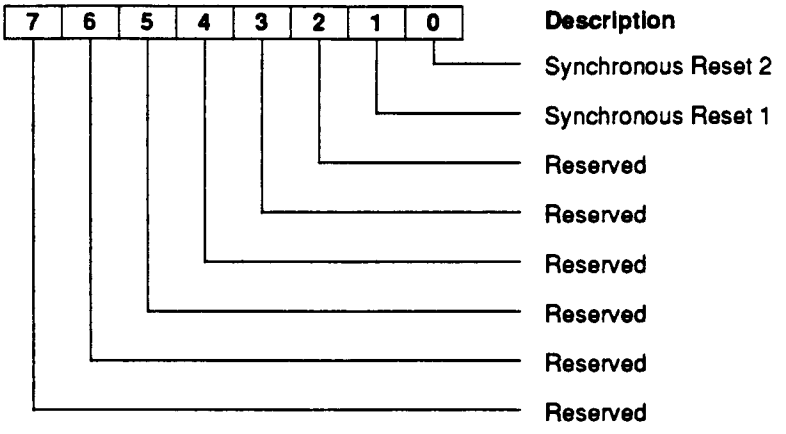
Bit	Description
7	Sequencer/Extensions Index Select 0 = Disables Extensions Index Enables access to Sequencer Registers through three least significant bits of this register. 1 = Enables write access to Extension Registers.

This register points to the Sequencer and the HT216-32 Extension registers. If bit 7= 0, the three low-order bits determine which Sequencer register will be pointed to in the next register read/write operation. If bit 7 = 1 then the seven low-order bits determine which Extension Register will be pointed to in the next register read/write operation.

Note: *If a value is written to the index register that points to SR[0:7] (0-FF with Extensions disabled or 0-7F with Extensions enabled), then read back of the index register will return a value from [0:7] (forcing bits[3:7] to 0). If a value is written to the index register that points to the Extension Registers (80-FF with Extensions enabled), readback of the index register will return the value written.*

SR0 Reset Register 3C5 R/W

Index 00

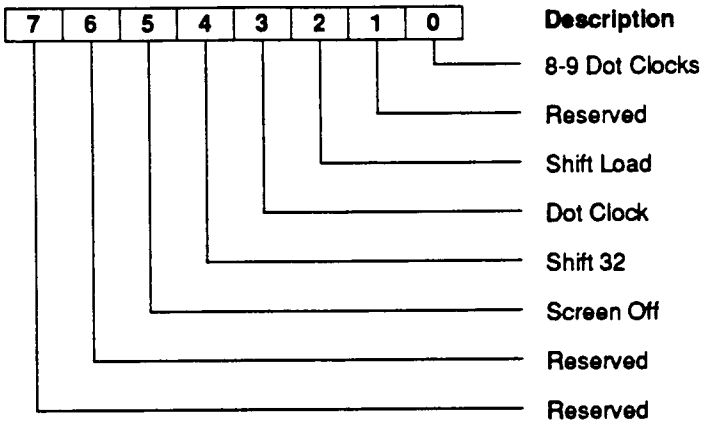


This register halts all timing including CRT timing. Both Reset Register bits must be set to 1 to allow the Sequencer to operate.

Bit	Description
1	Synchronous Reset 1 0 = The Sequencer initiates a synchronous clear and halt. Display memory, refresh and H/V sync signals to the display are disabled. 1 = The Sequencer operates as usual.
Note:	*This bit may be set to 0 for short periods of time (a few tens of microseconds at most). The following registers and associated bits can be changed only when this bit is 0:* *Clocking Mode Register (Sequence Reg1) bits 0 and 3* *Misc Output register bits[2:3]* *Extensions CLKSEL Register bit 4* *Extensions 'Extended Timing Select' Register bits[0:7]DMCTRL*
0	Synchronous Reset 2 This bit performs identically to bit 1, however, when it transitions from 1 to 0, it also resets the Character Map Register (Sequence Reg3) to 0.

SR1 Clocking Mode 3C5 R/W

Index 01



This register configures the timing circuits of the Sequencer. Before this register can be modified, the Sequencer must be placed in a synchronous Reset state.

Bit	Description
5	Screen Off 0 = Normal operation. 1 = Blanks the screen and disables the picture generating logic. This bit can be used for rapid scan update; disabling allows the video process uninterrupted access to memory.
Note:	*The blanking mechanism does not stop Horizontal and Vertical sync, blanking, or Display Enable signals. For example, the DE bit in the Display Status Register still toggles during screen blanking.*
4	Shift 32 0 = Loads the display data serializers every 1 or 2 cycles of the character clock as determined by bit 2 of this register. 1 = Loads the display data serializers every 4 cycles of the character clock.
Note:	*This bit is typically set for high resolution monochrome graphics modes (32 pixels per CRTC memory access). It is not used in any currently defined standard or extended VGA mode.*
3	Dot Clock 0 = Selects the Sequencer Master Clock to be output on the Dot Clock output pin of the HT216-32 chip. 1 = Divides the Sequencer master clock by 2 to generate the Dot Clock. The Dot Clock divided by 2 is used for 320 x 200 modes with the exception of 256 color mode.
Note:	*The Dot Clock is the primary clock used by the system. When the Dot Clock is modified, all*

other timings based on the Dot Clock will change accordingly.

2 Shift Load

The value of this bit is significant only when bit 4 is set to 0. If so:

0 = Loads the display serializers every character clock.
1 = Loads the display serializers every other character clock.

This bit is typically only set for monochrome graphics modes.

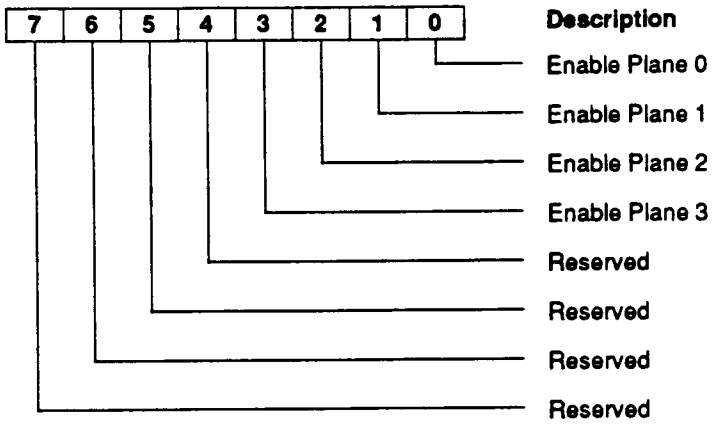
0 8/9 Dot Clocks

0 = The Sequencer generates 9-dot wide Character Clocks.
1 = The Sequencer generates 8-dot wide Character Clocks.

Note: Monochrome text modes (720 x 350 resolution) and VGA 400-line text modes (9 x 16 font, 40 x 25 and 80 x 25 text modes) use 9-dot character clocks; other standard modes use 8-dot character clocks.

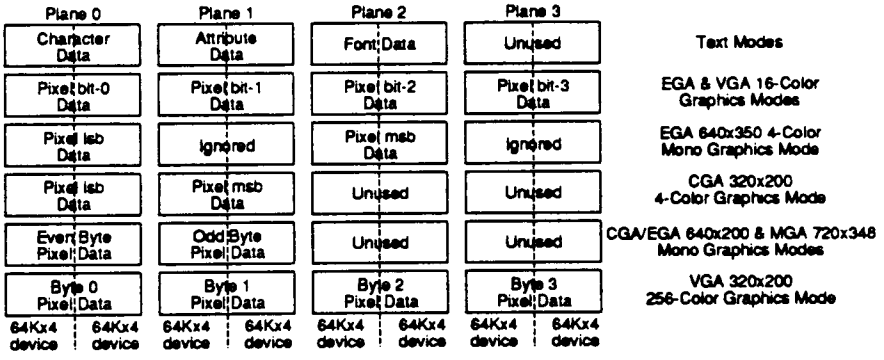
SR2 Plane Mask 3C5 R/W

Index 02



This register controls CPU write access to the four display memory planes. Any combination of planes may be enabled for writing at any time. It is important for graphics drawing operations.

Bit	Description
[3:0]	Enable Plane [3:0] 0 = Disable write access 1 = Enable write access



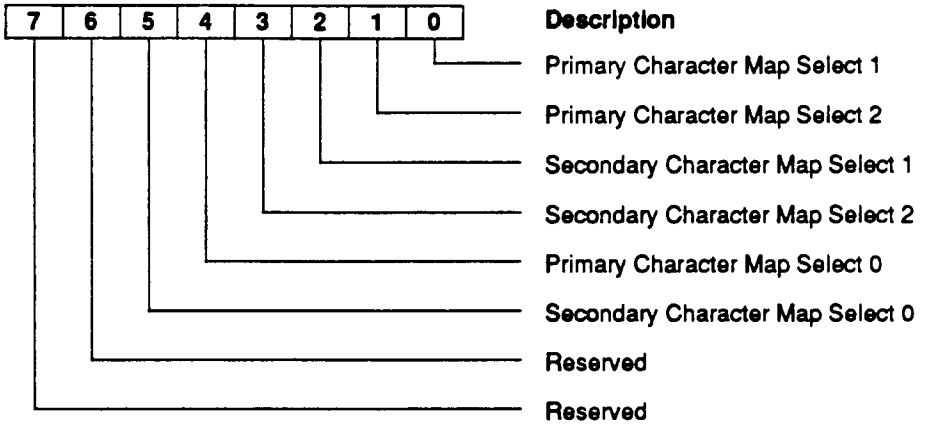
In 4-bit per pixel graphics modes, set this register to 0F (planes [0:3] each contain 1 bit of the pixel value). In text modes, set this register to 3 (the CPU needs to access planes 0 and 1; the font information is retrieved directly by hardware, independent of the contents of this register).

Note: *When odd/even modes are selected by clearing bits 2 and 3 of Memory Mode Register (SR4), planes 0/1 and planes 2/3 should have the same plane mask value.*

In Odd/Even and Chain 4 modes, this register is still in effect, and is ANDed with the plane select generated by the Odd/Even circuitry. For example, in Odd/Even mode the circuitry causes planes 0 and 2 to be enabled on CPU writes to even addresses and planes 1 and 3 to be enabled on CPU writes to odd addresses. However, if the plane mask setting is 3, only plane 0 (even addresses) and plane 1 (odd addresses) can actually be written to.

SR3 Character Map Select 3C5 R/W

Index 03



This register is used with software that requires multiple character sets. It selects which RAM character sets will be displayed. In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit may be redefined to be a switch between character sets. This function is enabled when the Primary and Secondary Character Map Select bits are set to different values. Whenever the two values are the same, the character select function is disabled.

Any change made to the contents of this register takes effect at the start of the next character line on the display.

Bit	Description
5,3,2	Secondary Character Map Select These bits select the bank used to generate text characters when the character attribute bit-3 is '1' according to the following table:

SR3[5]	SR3[3]	SR3[2]	FONT #	Table Location
0	0	0	0	1st 8k of Plane 2
0	0	1	1	2nd 8k of Plane 2
0	1	0	2	3rd 8k of Plane 2
0	1	1	3	4th 8k of Plane 2
1	0	0	4	5th 8k of Plane 2
1	0	1	5	6th 8k of Plane 2
1	1	0	6	7th 8k of Plane 2
1	1	1	7	8th 8k of Plane 2

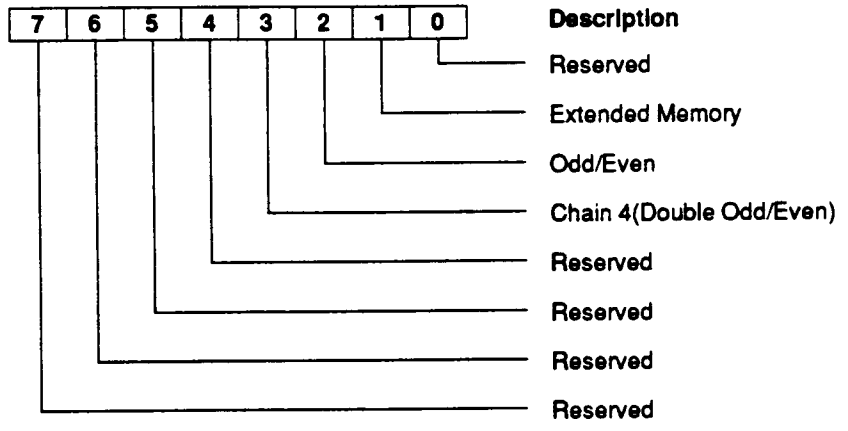
1,0,4 Primary Character Map Select

These bits select the bank used to generate text characters when the character attribute bit-3 is '0'.

SR3[1]	SR3[0]	SR3[4]	FONT #	Table Location
0	0	0	0	1st 8k of Plane 2
0	0	1	1	2nd 8k of Plane 2
0	1	0	2	3rd 8k of Plane 2
0	1	1	3	4th 8k of Plane 2
1	0	0	4	5th 8k of Plane 2
1	0	1	5	6th 8k of Plane 2
1	1	0	6	7th 8k of Plane 2
1	1	1	7	8th 8k of Plane 2

SR4 Memory Mode Register 3C5 R/W

Index 04



This register is initialized by the BIOS during a mode select operation and is used by the Sequencer to determine how the memory is structured for that mode. Before this register can be modified, the Sequencer must be placed in a Synchronous Reset state using either Synchronous Reset 1 or Synchronous Reset 2.

Bit	Description
Bit 3	Chain 4 (double odd/even) This bit is used to generate display memory addresses in the implementation of 256-color modes. It affects display memory accesses from the CPU, not CRTC accesses. 0 = Enables the processor to access data sequentially in the bit map identified by the Map Mask register (Sequence Reg 3). 1 = A0 provides plane select bit-0 and A1 provides plane select bit-1. This bit takes priority over the Graphics Controller Read Map Register, Graphics Reg 5 bit 4 and bit 2 of this register (these bits are ignored).

Note: In order for writes to be accessed, the Plane Mask Register (Sequencer Reg 2) bit for planes selected by Chain 4 must be set. The plane select generated by Chain 4 is logically ANDed with the Plane Mask Register to generate another plane select.

Chain 4 Memory Modes

A1	A2	Map
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Odd/Even

0 = The Sequencer is placed in the Odd/Even mode. Even CPU addresses access planes 0 and 2 and odd CPU addresses access planes 1 and 3.

1 = The CPU addresses data within a bit plane sequentially. The planes are accessed according to the value in the Plane Mask Register (SR2).

Note: Set this bit to 0 for text modes and when emulating CGA graphics modes. This bit tracks the function of the Graphics Controller Mode register (GR5) bit 4.

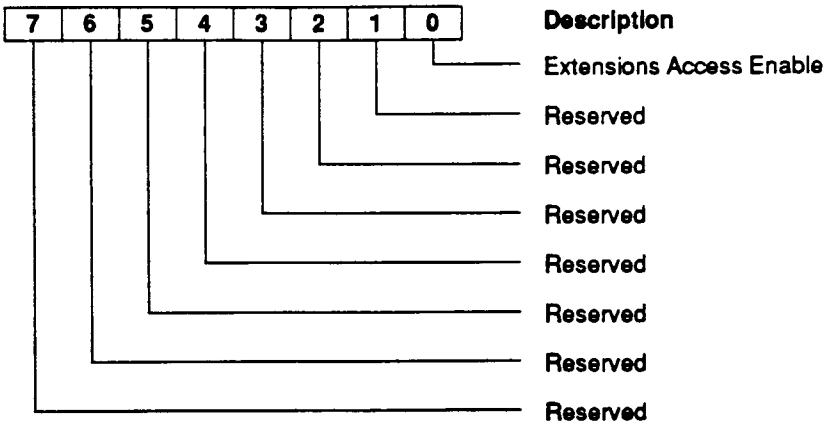
Bit 1 Extended Memory

0 = Allows emulation of EGA modes that assume a display memory size of 64k.

1 = Setting for standard VGA.

SR6 Extensions Control Register 3C5 R/W

Index 06

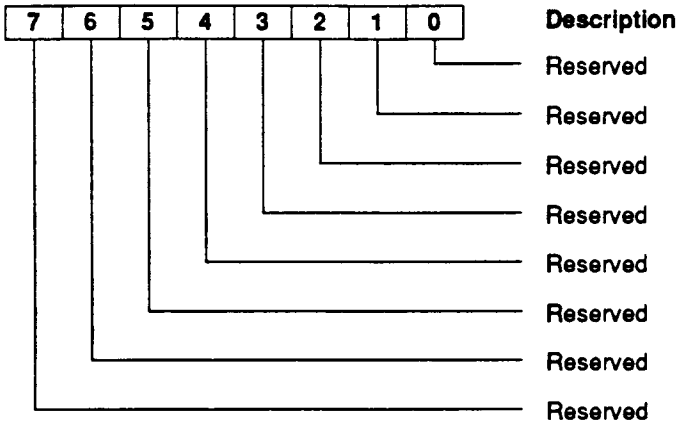


This register provides access to the HT216-32 Extended Registers (registers pointed to by Sequencer indices 80-FF). Access is enabled by writing 0xEA and disabled by writing 0xAE. Reading this register returns the state of the access enable flag in bit 0 (0 = disabled, 1 = enabled).

Note: *Access to the Extension Registers is enabled on reset. This allows the on-board BIOS to initialize the HT216-32 chip to a particular mode of operation.*

SR7 Reset Horizontal Character Counter 3C5(W)

Index 07



Writing to this register with any data will cause the horizontal character counter to be held in a reset condition (character counter output = 0). A write of any value to the Extensions Control Register (Sequence Reg 6) clears the latch that is holding the reset condition of the character counter.

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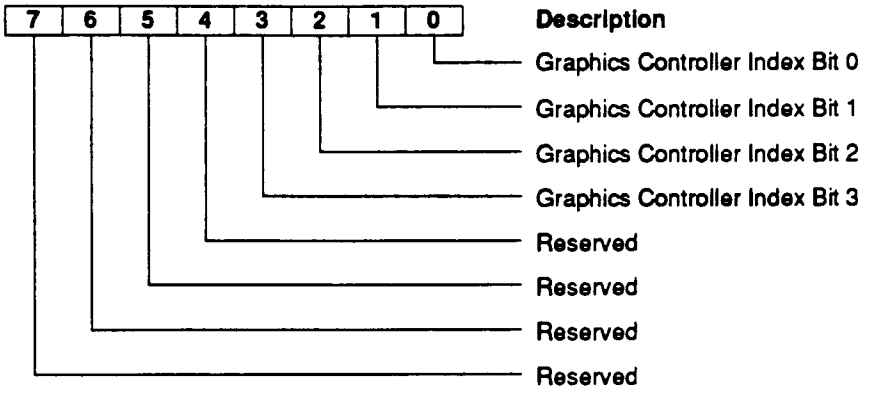
The Graphics Controller directs data from the display memory to the Attribute Controller and the CPU. There are ten read/write Graphics Controller Registers including one index register and nine data registers. Two port addresses are used; the index address (3CE) selects a data register, and the data address (3CF) reads or writes data to the selected data register.

Graphics Control Registers

Desc.	Register Name	Bits	Access	Index	Port
GRX	Graphics Controller Index	4	R/W	--	3CE
GR0	Set/Reset	4	R/W	00	3CF
GR1	Enable Set/Reset	4	R/W	01	3CF
GR2	Color Compare	4	R/W	02	3CF
GR3	Data Rotate	5	R/W	03	3CF
GR4	Read Map Select	2	R/W	04	3CF
GR5	Graphics Mode	6	R/W	05	3CF
GR6	Miscellaneous	4	R/W	06	3CF
GR7	Color Don't Care	4	R/W	07	3CF
GR8	Bit Mask	8	R/W	08	3CF

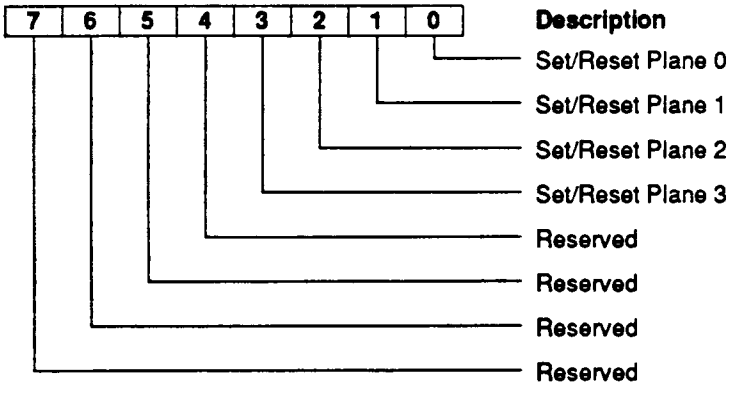
GRX Graphics Controller Index 3CE R/W



The Graphics Controller Index Register points to the internal data registers of the Graphics Controller. The four low-order bits determine which data register will be accessed when a read/write is performed using port address 3CF.

GR0 Set/Reset 3CF R/W

Index 00



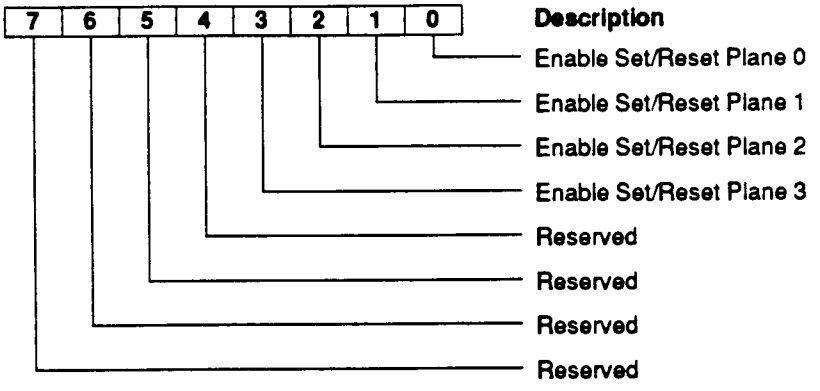
This register is used to define a fill color written to display memory during any display memory write operation. The four low-order bits in this register enable the Set/Reset function in Write Mode 0. When Set/Reset is enabled for a bit plane, the Set/Reset Register writes to the plane. When disabled, processor data is written to the plane. For example, if the Set/Reset Register contents are 1101, then a write to display memory will result in the following:

	7	6	5	4	3	2	1	0
Plane 3	1	1	1	1	1	1	1	1
Plane 2	1	1	1	1	1	1	1	1
Plane 1	0	0	0	0	0	0	0	0
Plane 0	1	1	1	1	1	1	1	1

Note: This assumes the Enable Set/Reset register (Graphics Reg 1) contents are 1111, all planes are enabled (Sequencer Reg 2 = 1111) and all bits are unmasked (Graphics Reg 8 = FF).

GR1 Enable Set/Reset 3CF R/W

Index 01



This register defines which memory planes will receive fill data from the Set/Reset Register. The bits in this register function in conjunction with the Set/Reset Register (Graphics Reg 0) and the Mode Register (Graphics Reg 5). If the Mode Register is programmed to Write Mode 0, the contents of the Set/Reset register are written to the respective display memory planes. If the Write Mode is 0 and Set/Reset are not enabled on a plane, the plane is written with the data from the CPU data bus.

For example, if the Set/Reset Register (Graphics Reg 0) contents are 0100, the contents of the Enable Set/Reset Register are 0101 and a write of 11001101 is performed on display memory, the following settings will result:

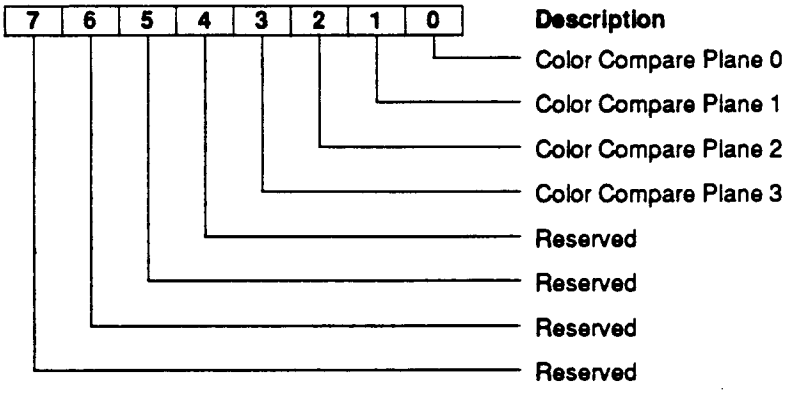
	7	6	5	4	3	2	1	0
Plane 3	1	1	0	0	1	1	0	1
Plane 2	1	1	1	1	1	1	1	1
Plane 1	1	1	0	0	1	1	0	1
Plane 0	0	0	0	0	0	0	0	0

Note: 1. *The settings above assume Write Mode = 0, all planes enabled (Sequencer Reg2 = 1111) and all bits unmasked (Graphics Reg8 = FF).*

2. *Refer to the Mode Register, Port 3CF Bit[1:0] for additional information on Write Mode.*

GR2 Color Compare Register 3CF R/W

Index 02



This register is used to implement graphics drawing algorithms that must find and identify objects by their colors. The 4 low-order bits of this register contain the value that video data is compared with during processor reads. The data returned from the comparison will be a logical 1 in each bit position where the 4 bit planes equal the compare value.

The Color Compare Register uses Read Mode 1 (Graphics Reg5 bit 3) to match pixels with a specific color. If GR5 bit 3 = 1, the data read from display memory planes [0:3] is compared to the bits [0:3] in the Color Compare Register. A bit value of 1 is returned to the CPU when a match occurs for each pixel and a 0 is returned for each pixel that does not match the Color Compare Register.

For example, if the contents of the Color Compare Register are 0011 (to compare planes 0 and 1) and the contents of the plane are as follows:

	7	6	5	4	3	2	1	0
Plane 3	0	0	0	0	0	0	0	0
Plane 2	1	1	1	1	1	1	1	0
Plane 1	0	0	0	0	0	0	0	1
Plane 0	1	1	1	1	1	1	1	1

The data bus will contain the following (assuming Graphics Reg7 = 1111):

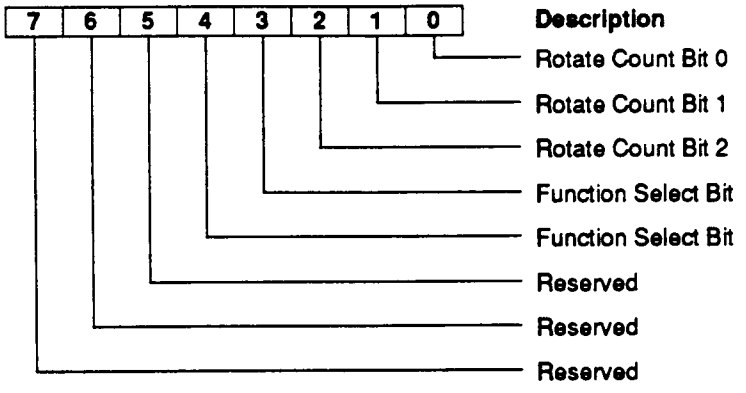
	7	6	5	4	3	2	1	0
Bus	0	0	0	0	0	0	0	1

Notes:

1. *Bit planes with the Color Don't Care (Graphics Reg7) bit set return a logical 1 to a Color Compare.*
2. *Color Compare data has no meaning in mode 13h (320 x 200 x 256 colors).*

GR3 Data Rotate 3CF R/W

Index 03



This register controls two independent functions: logical functions performed on write data and right data rotation.

Bit	Description
[4:3]	Function Select These bits determine how the data latches in the processor affect video data that is being written into memory. The logical operation that results is shown below:

Bit-4	Bit-3	Operation
0	0	No change
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

Note: *Data is defined as any option available with the Write Mode Register. Data cannot be the CPU latched data. For example, if the contents of the Data Rotate Register bits[2:0] are 011 and a program writes CA to display memory:*

C Data =	1	1	0	0	1	0	1	0 = CA
the Result Stored is =	0	1	0	1	1	0	0	1 = 59
(the result is shifted 3 bits to the right, circularly)								

If the contents of Data Rotate Register bits 3 and 4 are binary 11 (XOR function) and the Graphics CPU latches have been loaded (by a read of display memory) data will appear as follows:

	7	6	5	4	3	2	1	0
Plane 3 Latch	1	0	0	1	0	1	1	1
Plane 2 Latch	0	1	1	1	1	0	0	1
Plane 1 Latch	1	1	0	1	0	1	0	1
Plane 0 Latch	1	0	1	1	0	0	0	0

A write with data 00111100 will cause an XOR function to be performed on the PC data and the CPU latch, resulting in display memory being the following:

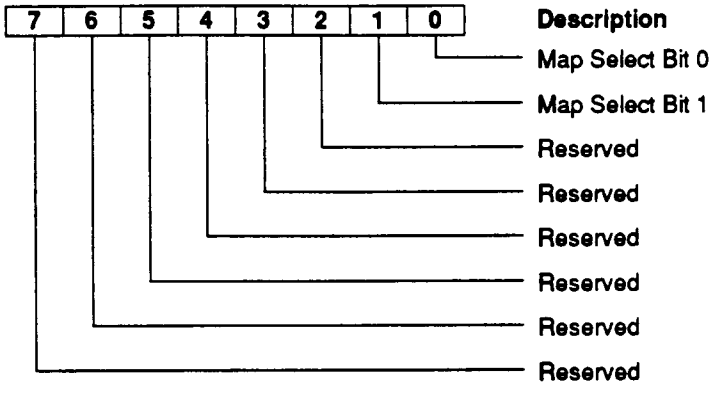
	7	6	5	4	3	2	1	0
Plane 3	1	0	1	0	1	0	1	1
Plane 2	0	1	0	0	0	1	0	1
Plane 1	1	1	1	0	1	0	0	1
Plane 0	1	0	0	0	1	1	0	0

The above condition assumes write mode = 1, all planes enabled (Sequencer Reg 2 = 1111) and all bits unmasked (Graphics Reg 8 = FF)

Bit	Bit Name
[2:0]	Rotate Count These bits perform a right rotate function on the data written by the CPU. If the Mode register (Graphics Reg 5) is programmed for Write Mode 0, the value in this field represents the number of bits the CPU data will be right rotated during CPU write cycles.

GR4 Read Map Select 3CF R/W

Index 04



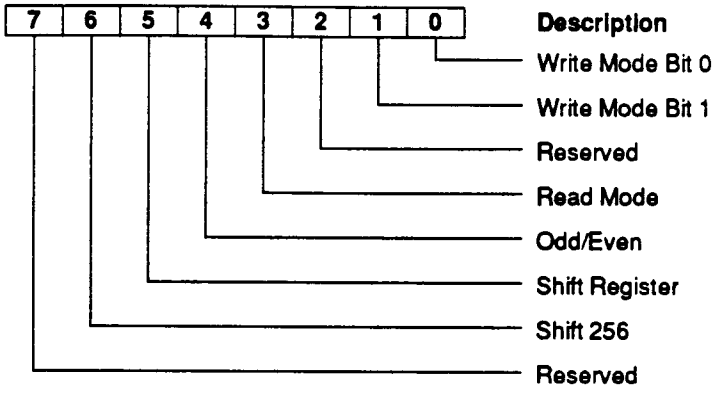
The two low-order bits of this register designate the memory plane [0:3] from which the CPU reads data. The four memory planes are selected as follows:

Bit-1	Bit-2	Plane Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

Note: *If the double odd/even bit (SR4 bit-3, also called 'Chain 4') is set, the contents of this register are ignored.*

GR5 Mode 3CF R/W

Index 05



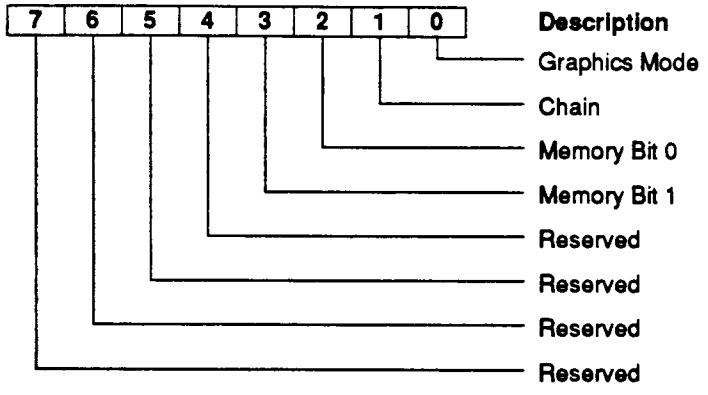
Bit	Description
6	Shift 256 0 = Bit 5 of this register is ignored. 1 = The video shift register is set up for 256-color mode.
5	Shift Register The data bits in the memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7 and M3D0-M3D7. 0 = M0D7-M0D0, M1D7-M1D0, M2D7-M2D0 and M3D7-M3D0 are shifted out; bit 7 always shifts out first. The outputs for the M0-M3 planes are ATR0-ATR3. 1 = The data in the four serial shift registers will be formatted as follows (the LSB is shifted out first):

MSB							LSB	Output to:
M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	ATR0
M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	ATR1
M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	ATR2
M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	ATR3

4	Odd/Even This bit is used to put the graphics controller in the Odd/Even addressing mode to emulate the CGA. This bit will track the function of Sequencer Memory Mode register bit 2, however the binary values will be inverted. The effect of this is even planes of memory are read when A0=0; if A0=1 then odd planes are read. Map select bit 1 in GR4 selects plane 0, 1 pair or the 2, 3 pair. 0 = Normal addressing mode. 1 = Odd/Even addressing mode.
3	Read Mode 0 = The CPU reads data from the display memory planes. The Read Map Select register (Graphics Register 4) selects the plane. 1 = The CPU reads the result of the logical comparison between the data from the four display memory planes and the contents of the Color Compare register (Graphics Reg 2).
[1:0]	Write Mode 0 = Each of the four display memory planes is written with the CPU data rotated right by the number of counts in the Rotate register, unless Set/Reset is enabled for any of the four planes. When Set/Reset is enabled, planes that are affected are written with 8 bits of the value contained in the Set/Reset register for that plane. 1 = Each display memory plane is written with the contents of the CPU latches. These latches are loaded by a CPU read operation. This operation overrides bit mask values. 2 = Memory planes [0:3] are filled with the value of data bits[0:3]. For example, memory plane 0 is filled with the value of Data Bus bit 0, memory plane 1 is filled with the value of Data Bus bit 1, etc. 3 = The CPU data is rotated, ANDed with the Bit Mask register, and written to the bit mask in place of the Bit Mask register. Set/Reset is enabled for all planes in this mode.

GR6 Miscellaneous 3CF R/W

Index 06

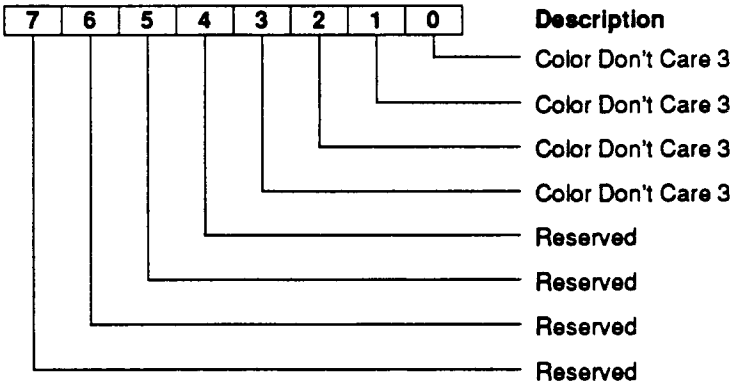


This register is used to select the memory address range where display memory is mapped to the host and enables latches for the character generator.

Bit	Description
[3:2]	Memory Map This field controls the mapping of the address memory buffer into the CPU address space. Memory Map 0: A0000 for 128k Memory Map 1: A0000 for 64k Memory Map 2: B0000 for 32k Memory Map 3: B8000 for 32k
1	Chain Odd Maps to Even 0 = Planes 0 and 2 are selected. 1 = Planes 1 and 3 are selected. CPU address bit A0 is replaced by a higher order address bit and odd/even maps are selected with odd/even values of the address bit. The value of A0 determines which memory plane is selected.
0	Graphics Mode 0 = Selects text mode. 1 = Selects graphics mode and disables the character generator latches. In this mode, color data is serialized in the shift registers before it is passed to the Attribute Controller.

GR7 Color Don't Care 3CF R/W

Index 07



This register masks particular planes from being tested during color compare cycles. It is used in conjunction with the Color Compare Register (Graphics Reg 2).

Bit	Description
[3:0]	Color Don't Care The four low-order bits of this register control if a specific bit plane is examined in a color compare operation. 0 = Disables color comparison 1 = Enables color comparison

For example, if the contents of the Color Compare Register (Graphics Reg 2) are 0011 (to compare planes 0 and 1) and the contents of the Color Don't Care register are 1011 (ignore plane 2) and the planes hold the following values:

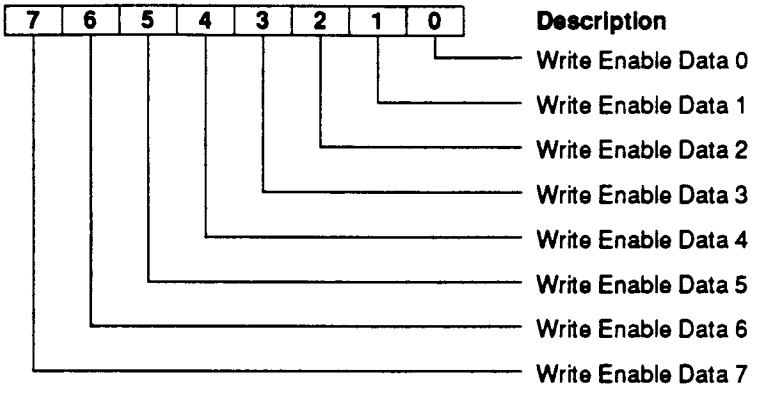
	7	6	5	4	3	2	1	0
Plane 0	1	1	1	1	1	1	1	1
Plane 1	0	1	0	0	1	1	0	1
Plane 2	1	1	0	1	0	1	1	0
Plane 3	0	0	0	1	1	1	0	0

then the data bus will contain the following:

	7	6	5	4	3	2	1	0
Bus	0	1	0	0	0	0	0	1

GR8 Bit Mask 3CF R/W

Index 08



This register is used to mask certain bit positions from being modified during read-modify-write cycles. However, it does not implement a true bit mask and must be used with care.

Bit	Description
[7:0]	Write Enable Data 0 = Preserves the values of the corresponding bit in each of the four memory planes. The data read in the previous cycle will be written into memory and stored in an internal latch within the Graphics Controller. 1 = Allows unrestricted manipulation of the data in the corresponding bit in each of the four memory planes.

The Bit Mask is applicable to any data written by the CPU, including rotate, logical functions (AND, OR, XOR), Set/Reset and No Change. The data must be latched internally by reading the location. The Bit Mask applies to all four planes simultaneously.

For example, if the contents of the Bit Mask register are 01101001 and the data latches have been loaded as in the following table:

	7	6	5	4	3	2	1	0
Plane 0 Latch	1	0	1	0	1	0	1	0
Plane 1 Latch	1	1	0	0	1	1	0	1
Plane 2 Latch	0	0	1	0	1	0	1	1
Plane 3 Latch	0	1	0	1	0	0	1	0

then a CPU write of 0100110 will result in display memory as follows:

	7	6	5	4	3	2	1	0
Plane 3	0	1	1	1	0	0	1	0
Plane 2	0	1	1	0	0	0	1	0
Plane 1	1	1	1	0		1	0	0
Plane 0	1	1	1	0	0	0	1	0
Effect	L	B	B	L	B	L	L	B

(L = Latched data, B = Bus Data)

Note: *The above example assumes all planes are enabled (Sequencer Reg 2 = 1111).*

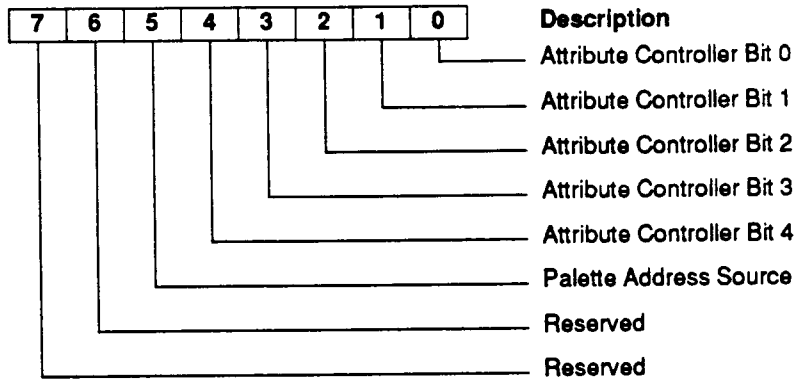
Attribute Controller Registers

This section describes the seven Attribute Controller Registers. The Attribute Controller provides a palette of 16 colors selectable from a possible 64. It also controls blinking and underline operations.

The Attribute Controller Index Register (ARX) is read at Extension Index 83 for state save and restore. An extra bit is available (the data/index pointer) when reads are performed at the extension port. Writes to ARX at the 3C0 port toggle the data/index pointer. The Attribute Controller Index Register can also be read at CRTC index 24.

Desc.	Register Name	Bits	Access	Index	Ports	
ARX	Attribute Controller Index	6	R/W	--/83	3C0(R/W)	3C5(R/W)
AR0-F	Palette Regs 0-15	8	R/W	00-0F	3C0(W)	3C1(R)
AR10	Mode Control	7	R/W	10	3C0(W)	3C1(R)
AR11	Overscan Color	8	R/W	11	3C0(W)	3C1(R)
AR12	Color Plane Enable	6	R/W	12	3C0(W)	3C1(R)
AR13	Horizontal Pixel Panning	4	R/W	13	3C0(W)	3C1(R)
AR14	Color Select	4	R/W	14	3C0(W)	3C1(R)

ARX Index Register 3C0/3C5 R/W

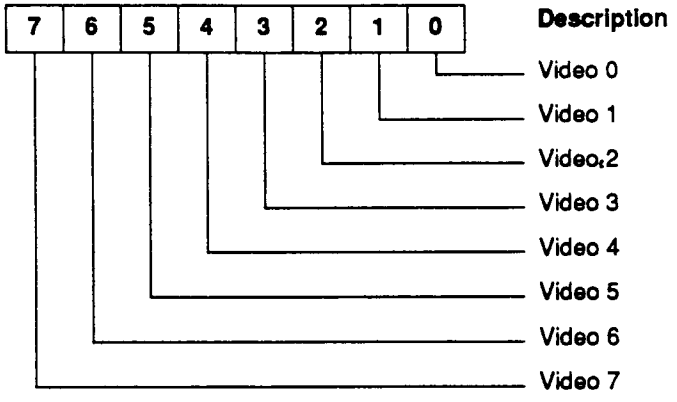


The five low-order bits of this register are used as an index to the data registers in the Attribute Controller. Accesses to 3C0 are directed to index and data on alternate accesses. The 3C0 I/O port index/data pointer is initialized for access of the index register by reading the Display Status Register (also called Status Register 1) at I/O port 3BA/3DA.

Bit	Description
5	Palette Address Source This bit selects the address source for the palette registers (0 = CPU, 1 = video data stream), which requires that CPU writes to the palette registers only take place when this bit is 0. 0 = Address source is CPU. The screen displays the color indicated by the Overscan Color register (Attribute Reg11), normally black. 1 = Normal video display.
[4:0]	Attribute Controller Index These bits form a 5 bit field for storing an index to the data registers in the Attribute Controller.

AR0-F Palette Registers 3C0(W), 3C1(R)

Index 00-0F



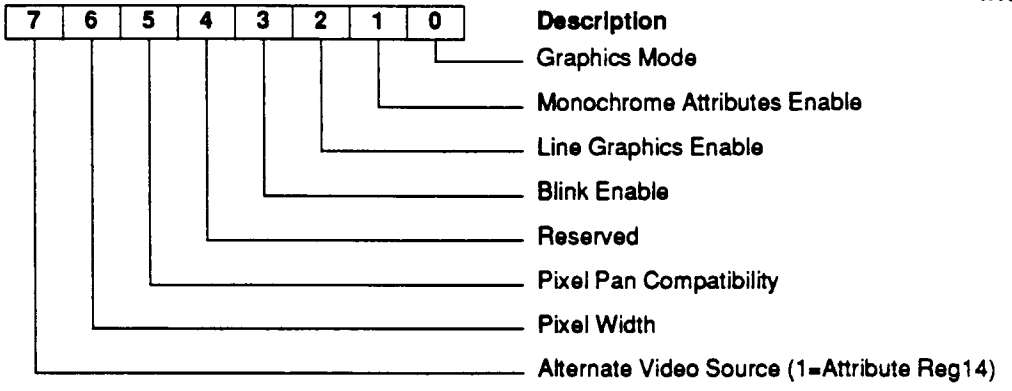
These registers dynamically map the text attribute or graphic color input value to the display color.

The Palette registers enable the user to access 64 addresses in the DAC color table. This palette allows 16 colors to be displayed simultaneously. In 256k color modes, these registers remain in use to index the DAC color table and should not be modified from the default settings.

To support analog monitors, 8 bits of color value output from the Attribute Controller are remapped by the external color palette (DAC). The DAC uses the 8 bits from the Attribute Controller as an index into a group of 256 registers. When using color analog monitors, each register contains three six-bit color values (one each for Red, Green and Blue) that display 256k colors. Analog monochrome monitors connect to the Green output (Red and Blue are ignored) and display a maximum of 64 shades of grey.

AR10 Mode Control 3C0(W), 3C1(R)

Index 10



This Register selects the graphics mode and monochrome attributes.

Bit	Description
7	Alternate Video Source This bit controls the source of video output bits 4 and 5. In 256-color mode, this bit is ignored and video outputs 4 and 5 are driven from bits 4 and 5 of the Palette registers (AR0-F). 0 = Video output bits 4 and 5 are driven from bits 4 and 5 of the Palette Registers (AR0-F). 1 = Video output bits 4 and 5 are driven by AR14 bits 0 and 1.
6	Pixel Width 0 = The video shift register is clocked at full speed. 1 = The video shift register is clocked at half speed for 256 color mode; the internal Attribute Controller Color Palette is by passed and the 8 video-bits are passed directly to the external palette.
5	Pixel Panning Compatibility 0 = Both Screen A and Screen B in split-screen mode will pan together. 1 = Only Screen A (upper screen) will pan.

Note: IBM VGA forces AR13 bits to be 0 even in 9-dot mode. A 1-bit left shift results.

3 Blink Enable

This bit functions in both text and graphics modes.

0 = Character blink is disabled.

1 = Character blink is enabled at a rate determined by the current vertical retrace frequency divided by 32 (16 frames in one state and 16 frames in the other state). This is the same rate as the cursor 'slow' blink (approximately 1/4 second each at 60Hz and about 1/3 second at 50Hz).

2 Line Graphics Enable

0 = Special line graphics character are disabled.

1 = Enables special line graphics characters by forcing the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0h through DFh.

Note: This bit is ignored in graphics modes.

1 Monochrome Attributes Enable

This bit works in graphics modes only.

0 = Selects color character attributes.

1 = Controls blinking in monochrome 4-color modes. Pixel patterns in graphics 4-color mode (mode 'F') are black (00), white (01), blinking (10) and intensified white (11). These patterns map to palette entries 0, 1, 4 and 5 if plane 3 is off and 8, 9, C and D if plane 3 is on (2 bits per pixel get mapped to planes 0 and 2 with planes 1 and 3 = 0).

0 Graphics Mode

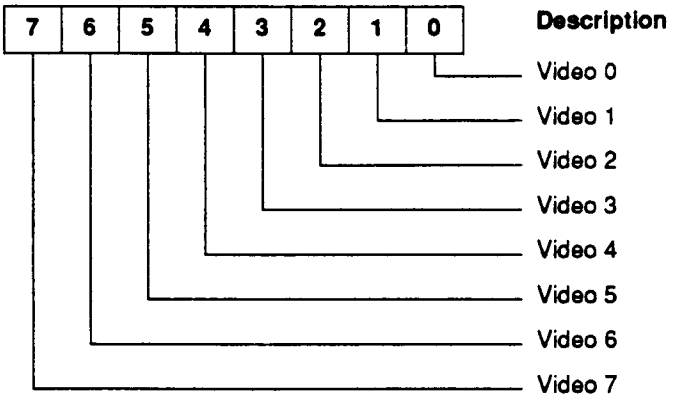
0 = Selects text mode.

1 = Selects graphics mode.

Summary of Operation of AR10					
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Mode**	**Description**
0	x	x	1	Graphics	Plane 3 selects palette A3
1	x	0	1	Graphics	If plane 3 data = 0 then palette input A[3:1] If plane 3 data = 1 then palette input A3 is blinked
1	x	1	1	Graphics	Palette input A3 is blinked (toggled on/off at the blink rate)
BL	BG	x	0	Text	If BL = 0 characters don't blink (attribute bit-7 controls BG intensity) If BL = 1 characters blink if attribute bit 7 = 1 (BG is non-intensified) Character blink toggles the character between foreground color (AR10 bits[0:3]) and normal background color (AR10 bits[4:6])

AR11 Overscan Color 3C0(W), 3C1(R)

Index 11

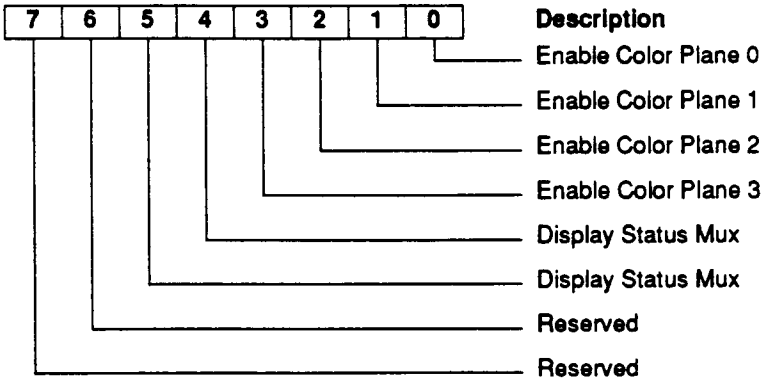


This register defines the overscan or border color displayed on the CRT screen. The overscan color is displayed when both the Blank and Display Enable signals are inactive.

Note: Refer to AR0-F for information on how the video output bits are connected, especially bit[7:4], and how they interact with Attribute Reg 14.

AR12 Color Plane Enable 3C0(W), 3C1(R)

Index 12



This Register enables color planes and runs diagnostics.

Bit	Description
[5:4]	Display Status Mux These bits are used to run diagnostics on the color subsystem card. These bits select video output data during display periods and overscan color during non-display periods as shown below:

Display Status Mux Summary

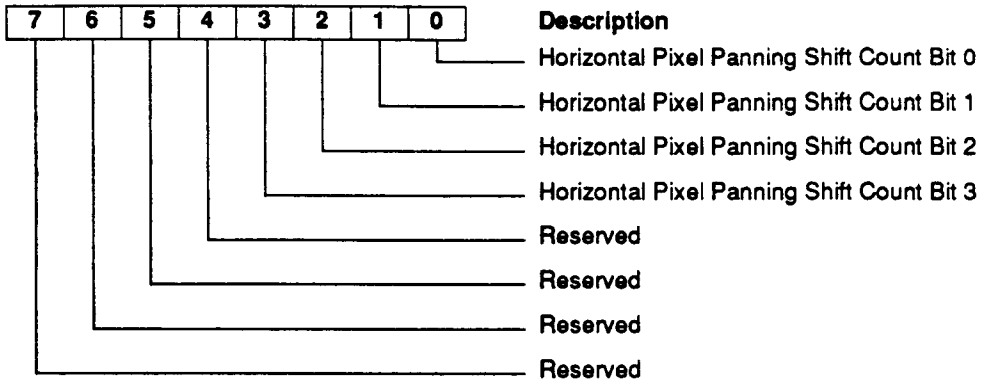
Color Plane Register		Display Status Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Setting bit 4 disables the cursor blink counter.

[3:0]	Color Plane Enable These bits control whether the data read from a specific bit plane is used for video output. 0 = Disables the bit plane output 1 = Enables the bit plane output.

AR13 Horizontal Panning 3C0(W), 3C1(R)

Index 13



This register is used to select how many pixels of display data are to be shifted left or right horizontally. Pixel panning is available in both text and graphics modes.

Bit	Description
[3:0]	Horizontal Pixel Panning Shift Count The amount of shift varies with the character width according to the following table:

Count	9-bit Characters	8-bit Characters	256-color Mode
0	1 pixel left	no shift	no shift
1	2 pixels left	1 pixel left	no shift
2	3 pixels left	2 pixels left	1 pixel left
3	4 pixels left	3 pixels left	2 pixels left
4	5 pixels left	4 pixels left	2 pixels left
5	6 pixels left	5 pixels left	3 pixels left
6	7 pixels left	6 pixels left	3 pixels left
7	8 pixels left	7 pixels left	3 pixels left
8-F	no shift	1 pixel right	1 pixel right

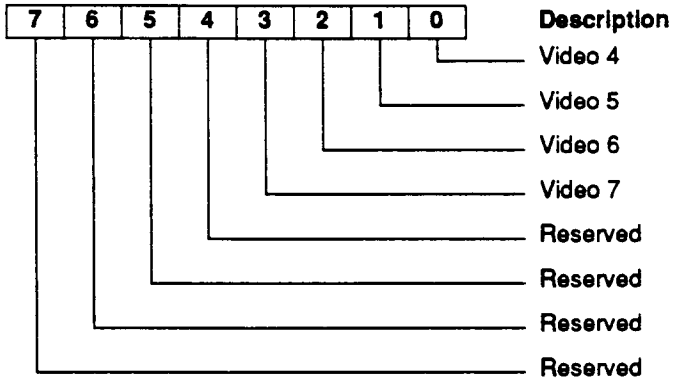
Notes: 1. *To prevent distortion of displayed images this register should only be changed during Vertical Retrace.*

2. *Set the Offset register (Controller Reg13) to at least one more than normal, when characters are not aligned with the character cell.*

3. *When AR10 bit 7 = 1, the output of this register is forced to 0 (no shift) by a successful line compare and remains in that state until the end of Vertical Retrace.*

AR14 Color Select 3C0(W), 3C1(R)

Index 14



This register is used to provide video output information.

Bit	Description
[3:2]	Video [7:6] These bits drive video output bits [7:6].
[1:0]	Video [5:4] When AR10 bit 7 = 1, these bits drive Video Output bits [5:4] instead of AR0-F (Color Palette Register) bits [5:4]. When AR10 bit 7 = 0, bits [5:4] of the internal palette are used for color bits C5 and C4.

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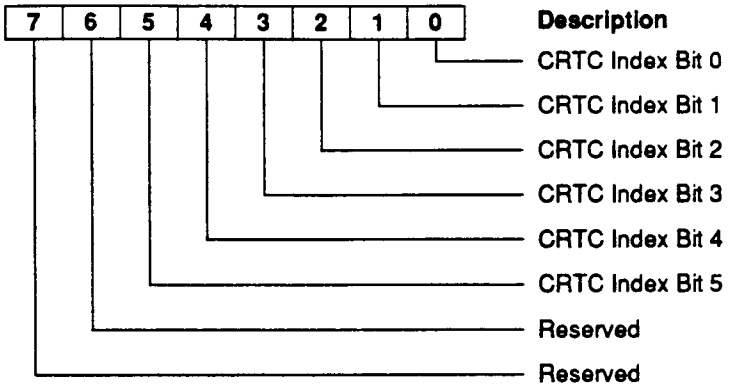
The CRT Controller registers generate the synchronizing and blanking signals that define the display raster. These registers consist of one index register and 29 internal data registers. Two port addresses are used; the index address selects a data register, and the data address reads or writes data to the selected data register. In monochrome modes, the index register is mapped at port address 3B4 and the data register is mapped at port address 3B5. In color modes, the index register is mapped at port address 3D4 and the data register is mapped at port address 3D5.

The CRT Controller Registers are listed in the following table:

Desc.	Register Name	Bits	Access	Index	Ports Mono/Color
CRX	Index Register	6	R/W	–	3B4/3D4
CR0	Horizontal Total Register	8	R/W	00	3B5/3D5
CR1	Horizontal Display Enable End	8	R/W	01	3B5/3D5
CR2	Horizontal Blanking Start	8	R/W	02	3B5/3D5
CR3	Horizontal Blanking End	8	R/W	03	3B5/3D5
CR4	Horizontal Retrace Start	8	R/W	04	3B5/3D5
CR5	Horizontal Retrace End	8	R/W	05	3B5/3D5
CR6	Vertical Total	8	R/W	06	3B5/3D5
CR7	Overflow	8	R/W	07	3B5/3D5
CR8	Preset Row Scan	7	R/W	08	3B5/3D5
CR9	Character Cell Height	8	R/W	09	3B5/3D5
CRA	Cursor Start	6	R/W	0A	3B5/3D5
CRB	Cursor End	7	R/W	0B	3B5/3D5
CRC	Start Address High	8	R/W	0C	3B5/3D5
CRD	Start Address Low	8	R/W	0D	3B5/3D5
CRE	Cursor Location High	8	R/W	0E	3B5/3D5
CRF	Cursor Location Low	8	R/W	0F	3B5/3D5
CR10	Vertical Retrace Start	8	(W, R/W)	10	3B5/3D5
CR11	Vertical Retrace End	8	(W, R/W)	11	3B5/3D5

Desc.	Register Name	Bits	Access	Index	Ports Mono/Color
CR12	Vertical Display End	8	R/W	12	3B5/3D5
CR13	Offset	8	R/W	13	3B5/3D5
CR14	Underline Row Scan	7	R/W	14	3B5/3D5
CR15	Vertical Blanking Start	8	R/W	15	3B5/3D5
CR16	Vertical Blanking End	8	R/W	16	3B5/3D5
CR17	CRT Mode Control	7	R/W	17	3B5/3D5
CR18	Line Compare	8	R/W	18	3B5/3D5
CR1F	VGA Identification	8	R	1F	3B5/3D5
CR22	Graphics Control Data Latches	8	R	22	3B5/3D5
CR24	Attribute Controller Index/Data Latch	7	R	24	3B5/3D5
CR3x	Clear Vertical Display Enable Flip-Flop	1	W	3x	3B5/3D5

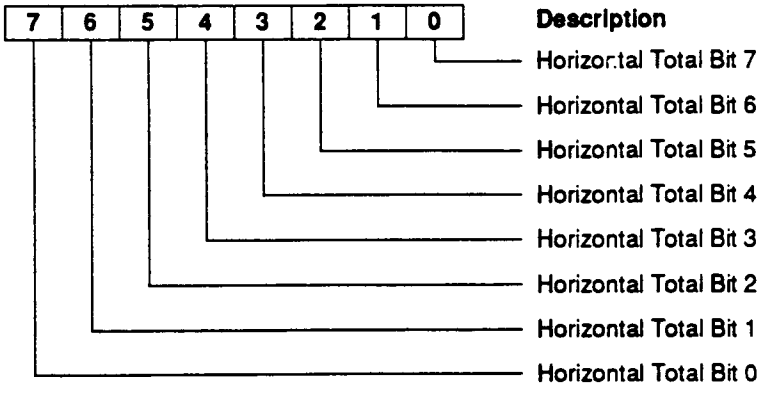
CRX CRT Controller Index Register 3B4/3D4 R/W



This register selects which of the 29 internal CRTC data registers will be accessed during the next read/write operation at port address 3B5 (mono) or 3D5 (color).

CR0 Horizontal Total Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)
Index 00

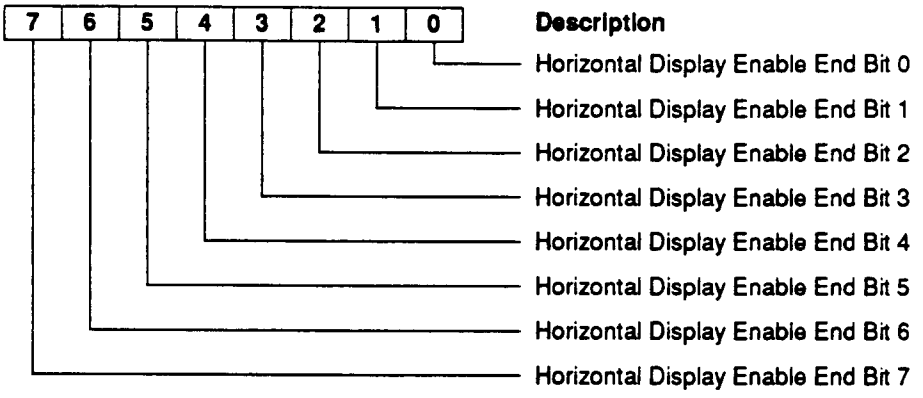


This register defines the total number of character clocks in a horizontal scan line, including blanking and retrace. All horizontal and vertical timing is based upon the contents of this register.

Note: *Value of bits in Horizontal Total Register = (Total number of character clocks in one scan line) - 5*

CR1 Horizontal Display Enable End Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)
Index 01

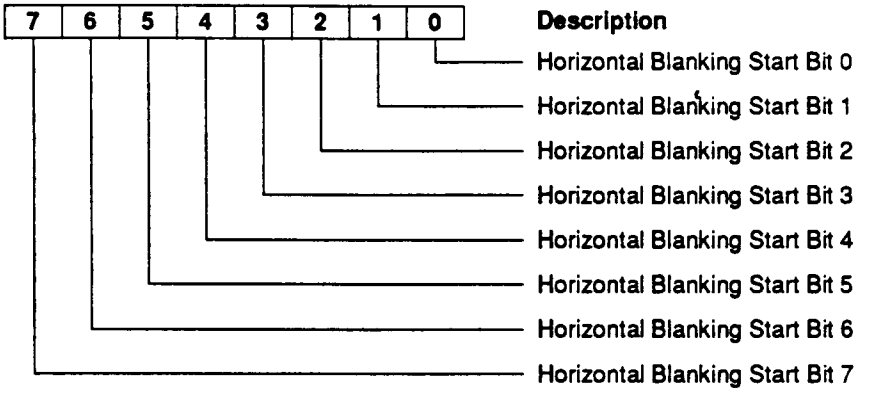


This register controls the duration of the Horizontal Display Enable pulse. The contents of this register define the total number of displayed characters in one horizontal scan line.

Note: *Value of bits in Horizontal Display Enable End Register = (Total number of characters per scan line) - 1*

CR2 Horizontal Blanking Start Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)
Index 02

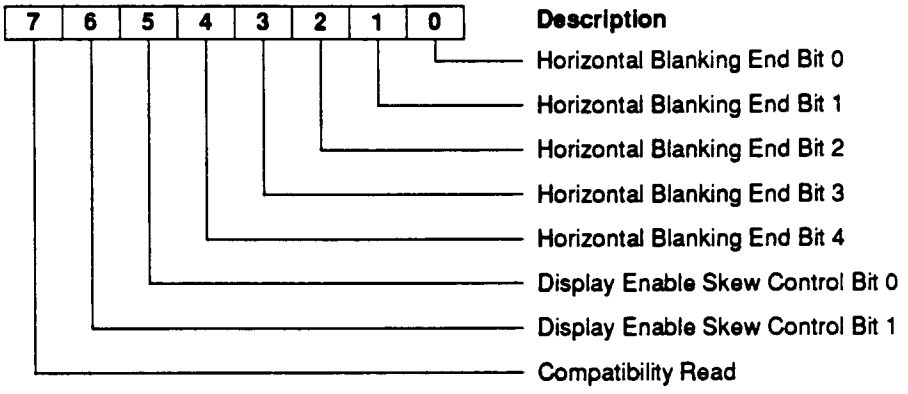


The contents of this register trigger the start of the Horizontal Blanking pulse. The Horizontal Blanking signal becomes active when the internal horizontal character counter is equal to the contents of this register.

Note: *Horizontal Blanking Start = Horizontal Display End (CR1) + 1*

CR3 Horizontal Blanking End Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)
Index 03



This register determines the duration of the Horizontal Blanking pulse and provides a mechanism for display enable skewing in text modes.

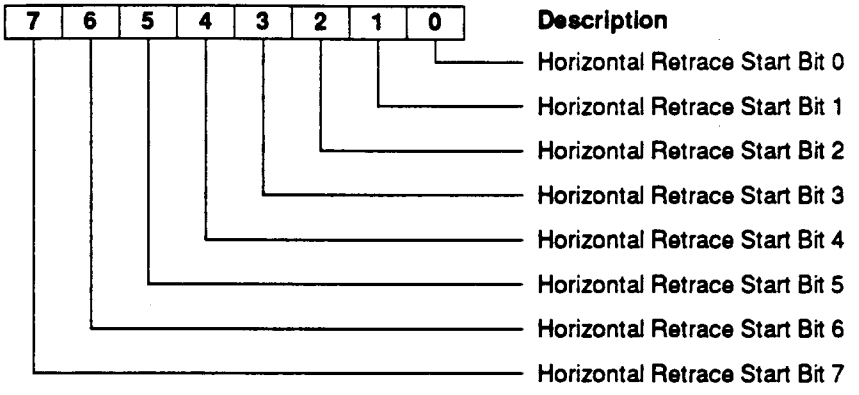
Bit	Description
7	Compatibility Read 1 = Enables read access to CRTC registers CR10 and CR11. This bit must be set for all standard and extended VGA modes.
[6:5]	Display Enable Skew The CRT Controller must access the display buffer, the attribute code, and the character generator font information prior to displaying data on the screen. These bits allow the Display Enable signal to be skewed up to 3 character clocks. Typically this field is set to 0. In 1024 x 768 extended modes, the Display Enable signal is skewed by one character clock to allow for synchronization with Horizontal and Vertical Retrace.
[4:0]	Horizontal Blanking End These bits and CR5 bit 7 comprise a 6-bit register that determines the duration of the Horizontal Blanking pulse in character clocks. The Horizontal Blanking pulse becomes inactive when the contents of the internal character counter match these bits.

Note: *Horizontal Blanking End = Horizontal Blanking Start (CR2) + width of Horizontal Blanking pulse in character clocks .*

CR4 Horizontal Retrace Start Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)

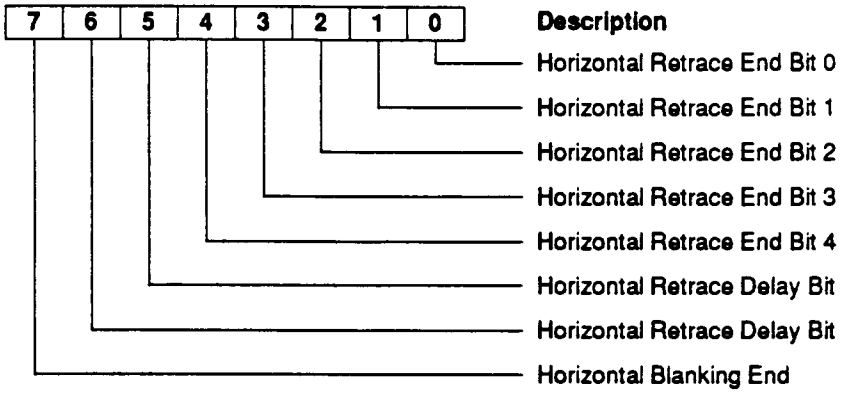
Index 04



This register triggers the horizontal character position at which the Horizontal Retrace pulse starts. When the contents of this register match the internal Horizontal Character Counter, the Horizontal Retrace pulse becomes inactive. It is used to center the image on the monitor screen.

CR5 Horizontal Retrace End Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)
Index 05



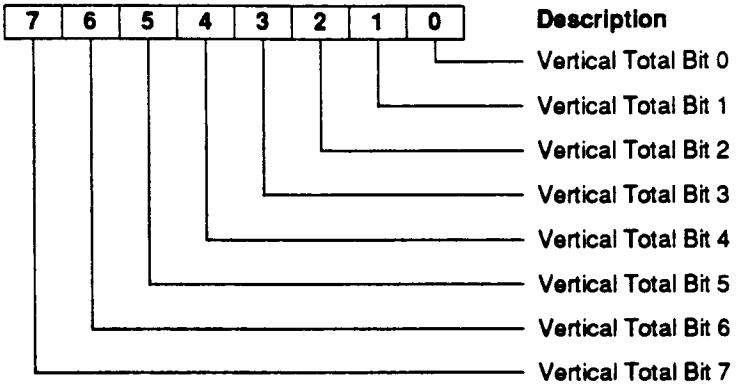
This register is used to skew Horizontal Retrace with respect to Display Enable to end Horizontal Retrace, and contains the msb of the Horizontal Blanking End register.

Bit	Description
7	Horizontal Blanking End Bit This bit in conjunction with CR3 bits [4:0] determines the duration of the Horizontal Blanking pulse in character clocks.
[6:5]	Horizontal Retrace Delay These bits allow the Horizontal Retrace pulse to be skewed (delayed) by up to 3 character clocks. This field is set to 0 in most cases.
[4:0]	Horizontal Retrace End The Horizontal Retrace pulse becomes inactive when the internal character counter equals the value of this field.

Note: *Horizontal Retrace End = Horizontal Retrace End (CR3) + width of Horizontal Retrace pulse in character clocks.*

CR6 Vertical Total Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)
Index 06



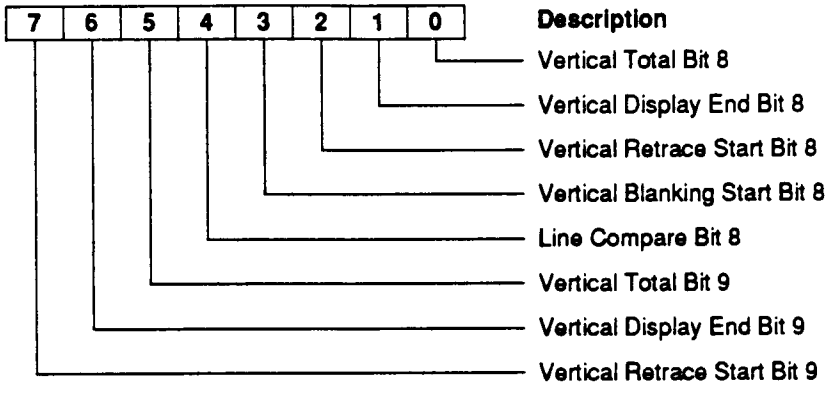
The Vertical Total register defines the total number of horizontal scan lines on the CRT, including the period during Vertical Retrace. This register contains the low-order 8 bits of a 10-bit register. The ninth and tenth bits are located in the Overflow register (CR7).

Note: *Vertical Total = number of horizontal scan lines + Vertical Retrace in Horizontal Scan Lines - 2*

CR7 Overflow Register 3B5/3D5

Write Protected by Extension Register C8(5) and CR11(7)

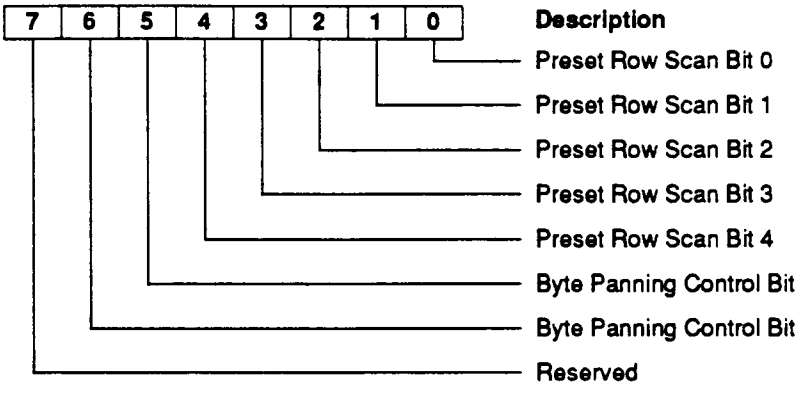
Index 07



The Overflow register contains the high-order overflow bits for CRTC registers that require more than eight bits.

CR8 Preset Row Scan Register 3B5/3D5 R/W

Write Protected by Extension Register C8(5) and CR11(7)
Index 08



This register is used to customize the display format. It provides a mechanism for smooth scrolling and byte panning control.

Note: This register should be changed only during Vertical Retrace.

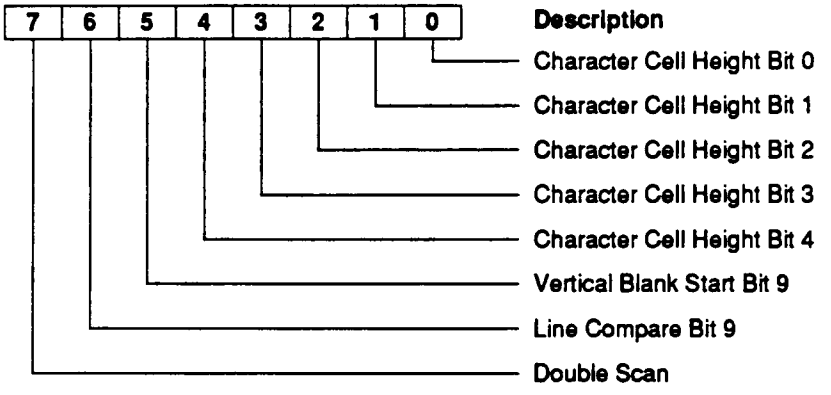
Bits	Description
[6:5]	Byte Panning Control These bits extend the capability of the Horizontal Panning register (Attribute Reg13). Up to 8 pixels can be panned horizontally by AR13. This field increases horizontal panning capability by up to 24 pixels, resulting in a total panning capability of 1-32 pixels. The table below shows the display shift that results from setting Byte Panning Bit 6 and Bit 5.

Bit-6	Bit-5	Byte Panning	
0	0	0 bytes	(display shifts 0 pixels left)
0	, 1	1 byte	(display shifts 8 pixels left)
1	0	2 bytes	(display shifts 16 pixels left)
1	1	3 bytes	(display shifts 24 pixels left)

[4:0]	Preset Row Scan These bits are used for smooth scrolling in text modes and certain graphics modes. For example, by setting the Preset Row Scan to 1 the next frame will start at scan line 1 of the character cell, giving an appearance of shifting the screen up one scan line.

CR9 Character Cell Height Register 3B5/3D5 R/W

Index 09



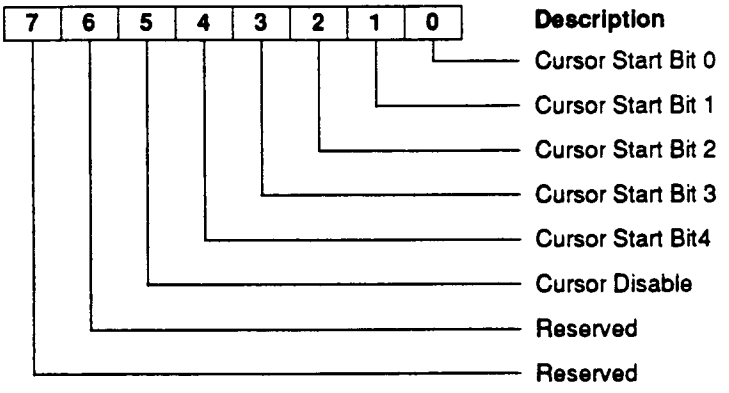
This register improves the quality of CGA text modes by allowing the VGA to double scan CGA 200 line modes. It also specifies the number of scan lines per character row and contains bit 9 from the Line Compare and Vertical Blank Start registers.

Bit	Description
7	Double Scan 0 = Normal scan line generation. 1 = Double Scan enabled. Each scan line is displayed twice in succession, enhancing CGA 200-line modes by double scanning to 400 lines. Character height, cursor and underline locations double.
6	Line Compare Bit-9 This is bit 9 of the Line Compare register; CR18 contains bits 7-0 and CR7 bit 4 contains bit 8.
5	Vertical Blanking Start Bit 9 This is bit 9 of the Vertical Blanking Start register; CR15 contains bits [7:0] and CR7 bit 3 contains bit 8.
[4:0]	Character Cell Height These bits specify the number of scan lines per character row.

Note: Character Cell Height = Number of scan lines per character cell - 1

CRA Cursor Start Register 3B5/3D5 R/W

Index 0A

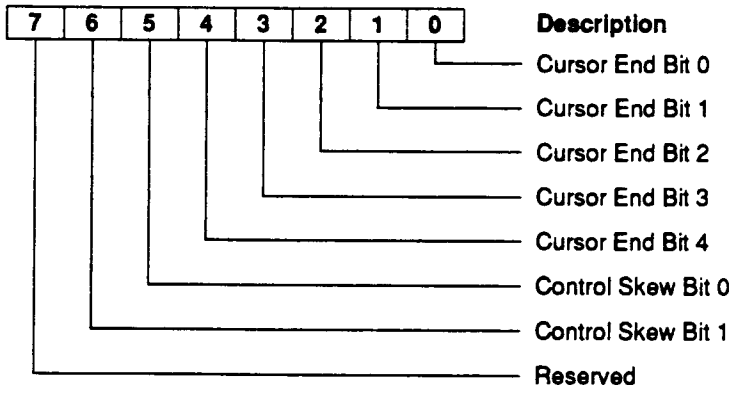


This register determines the scan line within a character cell at which the cursor will begin. When used with the Cursor End register this register defines the size of the cursor with respect to a character cell.

Bit	Description
5	Cursor Disable 0 = Cursor enabled. 1 = Cursor disabled.
[4:0]	Cursor Start These bits determine the scan line where the cursor will start within a character cell. When used with the Cursor End register these bits define the size of the cursor. For example: Cursor Start (CRA) = 0 Cursor End (CRB) = 7 The cursor will occupy scan lines 0 - 7 within a character cell, appearing as a block. Cursor Start (CRA) = 11 Cursor End (CRB) = 12 The cursor will occupy scan lines 11 & 12 within a character cell, appearing as an underline. Cursor Start (CRA) = 9 Cursor End (CRB) = 6 The cursor will not be visible.

CRB Cursor End Register 3B5/3D5 R/W

Index 0B



This register specifies the scan line within a character cell at which the cursor will end. When used with the Cursor Start register, this register defines the size of the cursor with respect to a character cell.

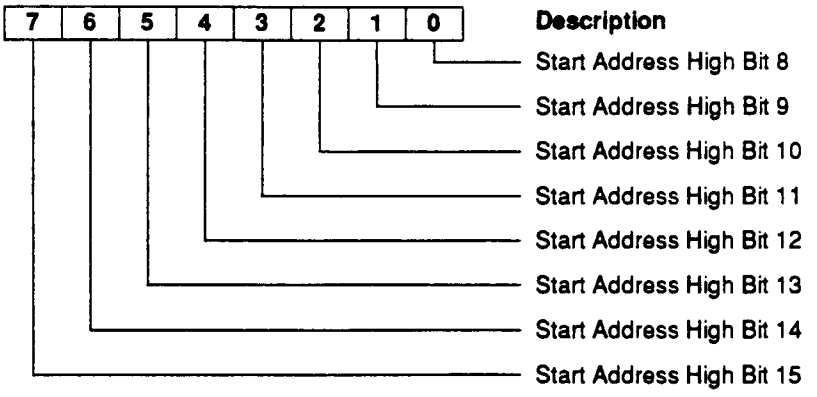
Bit	Description
[6:5]	Cursor Skew Control These bits control the cursor skew. Set this field to 0 for all VGA and extended modes. Typical bit settings and skews are shown below:

Bit 6	Bit 5	Skew
0	0	Zero character skew
0	1	Zero character skew
1	0	One character skew
1	1	Two character skew

[4:0]	Cursor End This field determines the scan line within a character cell where the cursor will end. Refer to the Cursor Start register (CRA) for programming examples.

CRC Start Address High Register 3B5/3D5 R/W

Index 0C



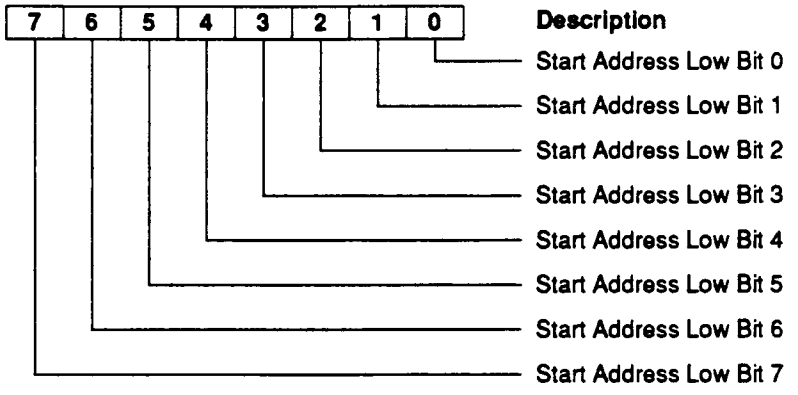
The Start Address High Register is used to pan an image on the screen, or move between display pages in memory. In conjunction with the Start Address Low Register (CRD) it defines the address in display memory of the data that will be displayed in the upper left corner of the screen (starting position).

If the VGA is using split screen mode, the Start Address registers specify the start address of Screen A (upper portion). The start address of Screen B (lower portion) is always 0. The Start Scan Line of Screen B is determined by the Line Compare Register (CR18).

Note: *This register is also used to identify the HTVGA chip. Any value written to this register can be read back exclusive-OR'd with EAh (binary 11101010) at the VGA Identification register (CR1F).*

CRD Start Address Low Register 3B5/3D5 R/W

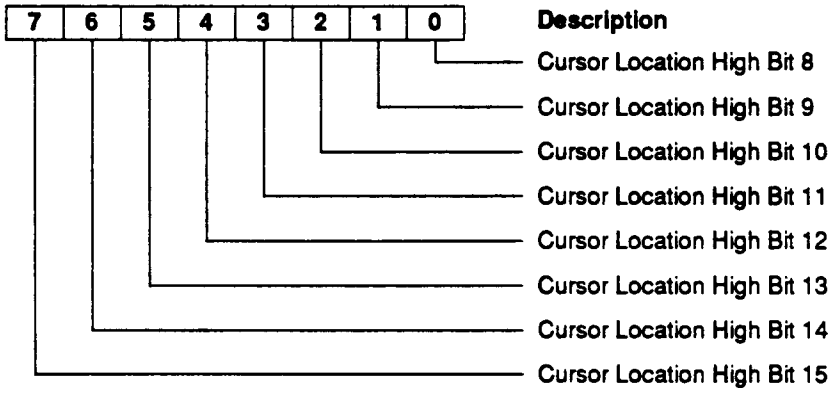
Index 0D



This register contains the 8 low-order bits of the Start Address register. See the Start Address High register (CRC) for a full description.

CRE Cursor Location High Register 3B5/3D5 R/W

Index 0E



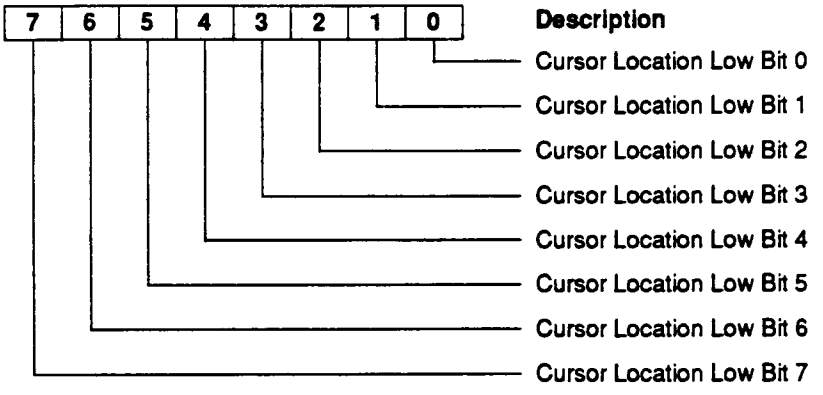
The Cursor Location High Register together with the Cursor Location Low Register (CRF), comprises a 16-bit field that specifies the offset of the cursor location from the start of physical display memory in character positions.

The value of the Cursor Location Registers is relative to the start of physical display memory, not to the start of the screen. When the Screen Start Address Registers (CRC & CRD) and the Cursor Location Registers are set to 0, the cursor is positioned over the upper left character on the screen (row 1, column 1). If the screen start registers are set to 1, the cursor will remain pointed to the same character.

Note: *Since text information is stored in display memory as character/attribute pairs, the address of the character under the cursor will be exactly two times the value in the Cursor Location Registers plus the base address of the screen.*

CRF Cursor Location Low Register 3B5/3D5 R/W

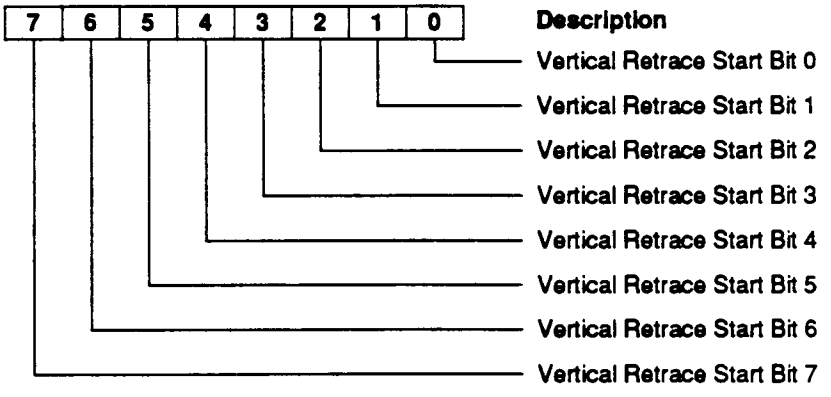
Index 0F



This register contains the 8 low-order bits of the 16-bit Cursor Location Register used to specify the offset of the cursor location from the start of physical display memory in character positions. See the Cursor Location High Register (CRE) for additional information.

CR10 Vertical Retrace Start 3B5/3D5 (W, R/W)

Index 10

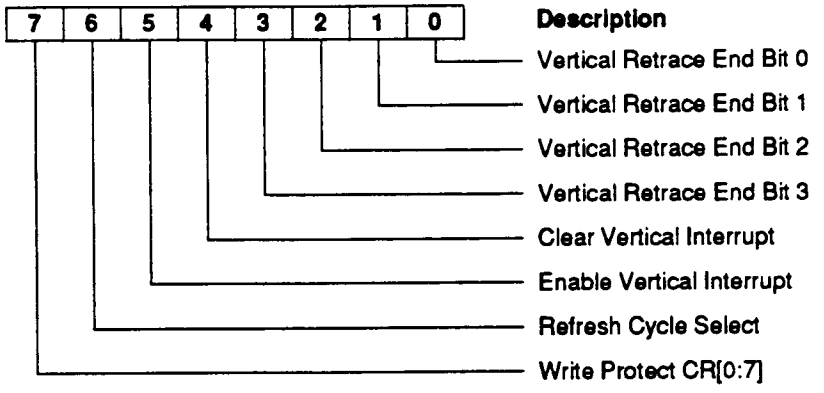


This register contains the 8 low-order bits of a 10-bit scan line count that triggers the start of the Vertical Retrace pulse. The two high-order bits are accessed through the Overflow Register (CR7).

Note: This register is read only when CR3 bit 7 = 1

CR11 Vertical Retrace End Register 3B5/3D5 (W, R/W)

Index 11



This register determines the vertical refresh rate.

Note: This register can be read only when CR3 bit 7 = 1

Bit	Description
7	Write Protect CR0-CR7 0 = No write protection of CRTC registers CR0-CR7. 1 = Write protect CR0-CR7.
6	Refresh Cycle Select 0 = Selects three DRAM refresh cycles per horizontal retrace. 1 = Five DRAM refresh cycles.
5	Vertical Interrupt Enable This bit controls whether interrupts are generated on the INT pin of the HT216-32 chip. This pin is typically connected to IRQ2 of the system bus. IRQ2 is used to identify the start of a vertical retrace. Once a Vertical Interrupt occurs; it can be cleared when a 0 is written to bit 4 of this register. 0 = Enables vertical interrupts. 1 = Disables vertical interrupts. The interrupt status can still be read at the Input Status Register 0 (port 3C2 bit 7).
4	Clear Vertical Interrupt 0 = Clears the vertical interrupt flip-flop and reasserts the interrupt signal. 1 = Allows the vertical interrupt flip-flop to be set at the start of the next Vertical Retrace interval.

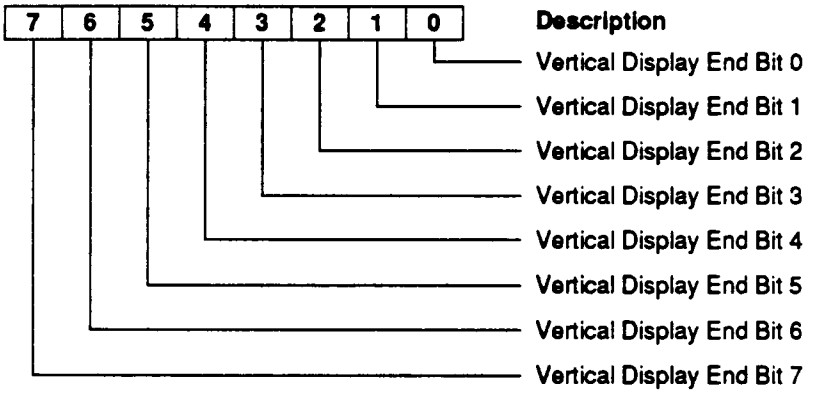
[3:0] Vertical Retrace End

The Vertical Retrace pulse becomes inactive when these bits match the lower four bits of the internal scan line counter. The width of the Vertical Retrace pulse is determined as follows:

Note: *Vertical Retrace End = Vertical Retrace Start (CR10) + the width of the Vertical Retrace pulse in horizontal scan units.*

CR12 Vertical Display Enable End Register 3B5/3D5 R/W

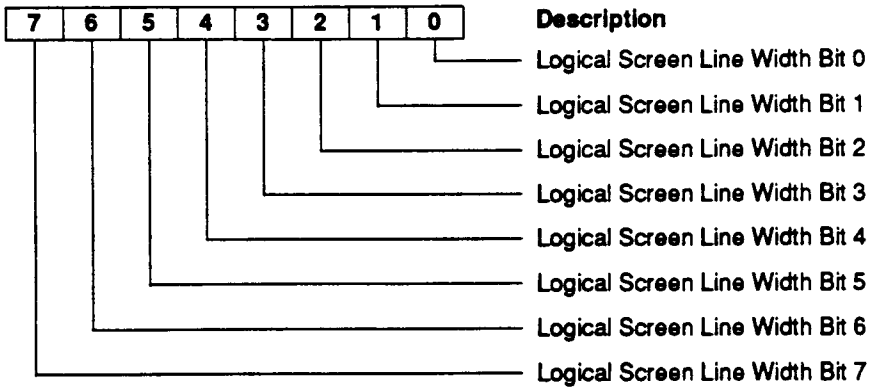
Index 12



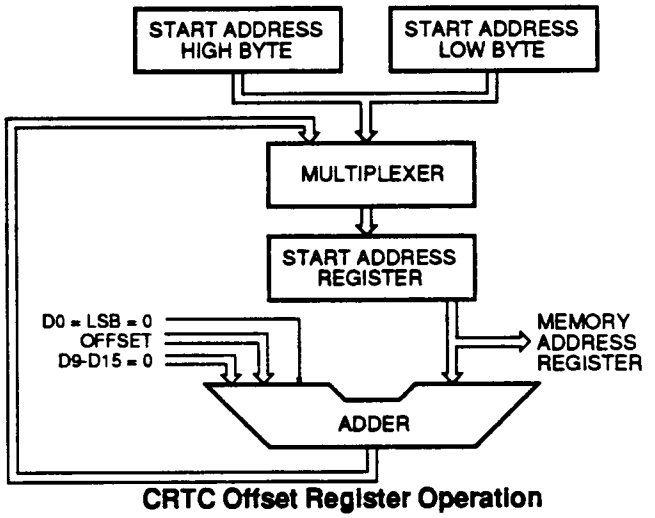
This register contains the 8 low-order bits of the 10-bit Vertical Display Enable End Register. The value in this register defines the point in a vertical scan at which vertical display enable ends and blanking begins. The ninth and tenth bits are located in the Overflow register (CR7).

CR13 Offset Register 3B5/3D5 R/W

Index 13



The Offset Register contents define the logical line width of the screen. The starting address of the next character row is determined by the value in this register.

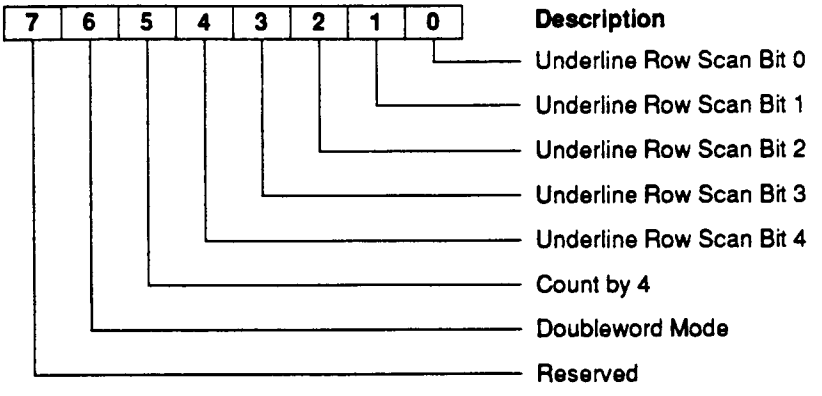


CRTC Offset Register Operation

The figure above is a functional diagram of how the Offset register is used. The register start address is sent to the memory address counter. When the memory address counter is counting bytes, the next line address is the current line start address + two times the Offset register contents. This is shown in the figure because the adder has one of the input port's least significant bits forced to 0. When the memory address counter is counting words, the next line address is the current line start address + four times the Offset register contents. The byte or word mode for the memory address counter is selected by the Mode Control Register (CR17), bit 6. The Start Address High and Low bytes correspond to the first address after a Vertical Retrace starts.

CR14 Underline Row Scan Register 3B5/3D5 R/W

Index 14

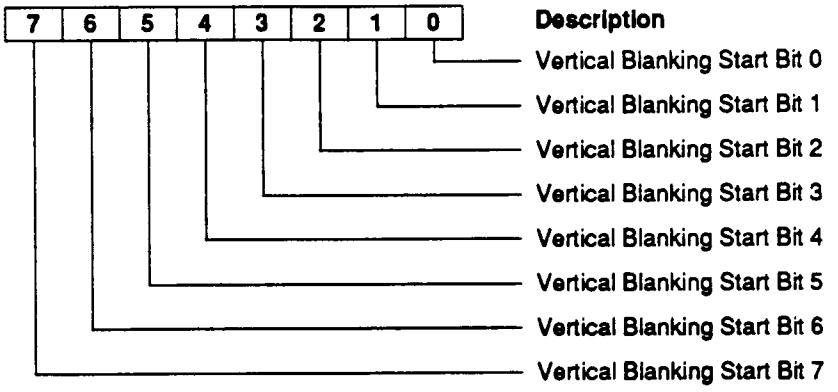


This register defines which line of a character cell will be illuminated when the underline attribute is set. It is used in text modes only.

Bit	Description
6	Doubleword Mode 0 = Allows Mode register (CR17) bit-6 to control the addressing mode. 1 = Forces Doubleword mode. The CRTC memory address counter is shifted up two bits to provide the linear address to display memory. The display memory address bit-0 is driven from CRTC memory address counter bit-12 and display memory address bit-1 is driven from CRTC memory address counter bit-13. The Byte Mode bit (CR17 bit-6) is ignored.
5	Count By 4 0 = Character clock not divided by 4. 1 = Divides the character clock input to the memory address counter by 4 when double addresses are used.
Note:	*If CR17 bit 3 'Count by 2' is 0, the memory address counter is clocked by the character clock /4. If 'Count by 1' is 1, the memory address counter is clocked by the character clock/2 and 'Count by 4' is ignored. When 'Count by 2' and 'Count by 4' are both 0, the memory address counter is clocked by the unmodified character clock.*
[4:0]	Underline Row Scan These bits specify the horizontal row scan in a character cell at which underlining will occur. The scan lines of the character cell are assumed to be numbered from the top of the cell starting at 0.
Note:	*Underlining is enabled while in monochrome modes (EGA/VGA mode 7 and Hercules/MGA text modes) by setting this field to 13 (the last scan line of the 8x14 character cell). For color modes, this field is normally programmed to a value larger than the size of the character cell to effectively disable underlining.*

CR15 Vertical Blanking Start Register 3B5/3D5 R/W

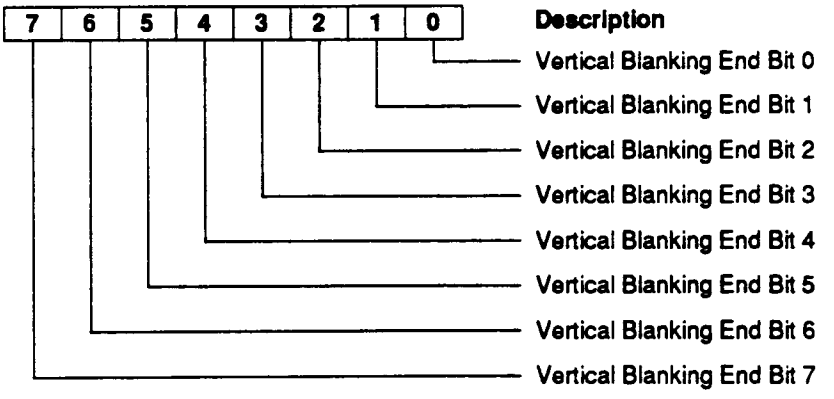
Index 15



This register contains the low-order 8 bits of the horizontal scan line count of the 10-bit Vertical Blanking Start Register. The ninth bit is located in the Overflow register (CR7 bit-3) and the tenth bit is located in the Character Cell Height Register (CR9 bit-5).

CR16 Vertical Blanking End Register 3B5/3D5 R/W

Index 16

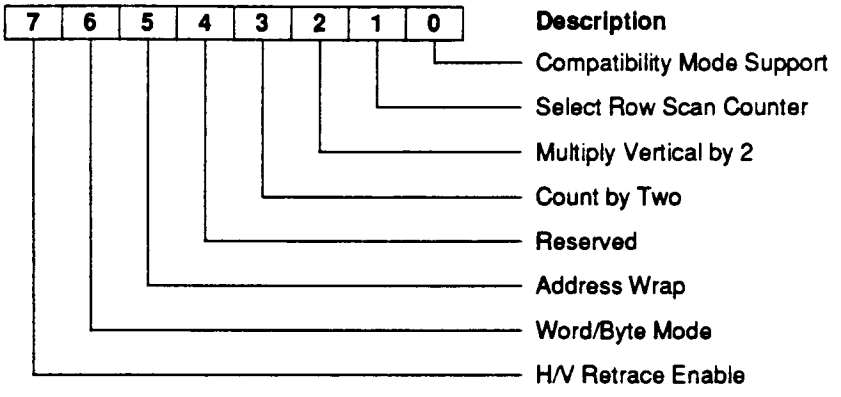


These bits specify the horizontal scan line count at which the Vertical Blanking pulse becomes inactive. The vertical blanking width (w) is determined from the following algorithm:

Note: *Value programmed into the Vertical Blanking End = The value of the Vertical Blanking Start (CR15) + width of blanking pulse in character clocks.*

CR17 CRT Mode Register 3B5/3D5 R/W

Index 17



The Mode control register is a multifunction register. Each bit defines a different option.

Bit	Description
7	Horizontal/Vertical Retrace Enable 0 = Disables Horizontal and Vertical Retrace. 1 = Enables Horizontal and Vertical Retrace.
6	Word/Byte Mode 0 = Selects Byte mode. 1 = Selects Word mode. Word mode causes the address counter bits to shift down one bit, and the MSB of the counter appears on the LSB of the memory address output.

Note: If Doubleword Mode (CR14 bit-6) is set, this bit is ignored.

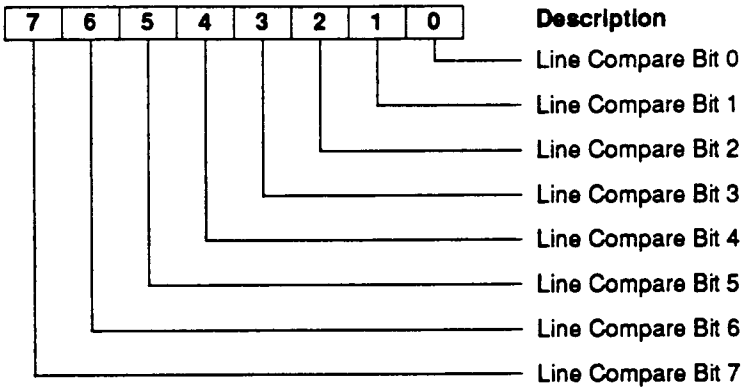
	CRTC Output Pin	Byte Address Mode	Word Address Mode	Doubleword Address Mode
RAM Row Address	xA15 xA15 xA15	MA15 MA14 MA8	MA14 MA13 MA8	MA13 MA12 MA8
RAM Column Address	xA3 xA2 xA1 xA0	MA3 MA2 MA1 MA0	MA2 MA1 MA0 MA13/MA15	MA1 MA0 MA13 MA12

Internal Memory Address Counter/Output Multiplexer Relationship

5	Address Wrap The Address Wrap bit selects the correct memory address counter bit to be output on xA0 in word mode. This bit must always be set to 1. In word mode, this bit controls the output from the memory address counter to the address bus and enables the full 256k of memory on the adapter.
3	Count By 2 0 = The memory address counter is clocked by the character clock. 1 = The memory address counter is clocked by the character clock divided by 2. This bit also creates either a byte or word refresh address for display memory.
2	Multiply Vertical By 2 0 = Selects the horizontal retrace clock 1 = Selects the horizontal retrace clock divided by 2. The following vertical registers must be programmed to half their normal value to result in the same number of scan lines: CR6 Vertical Total CR10 Vertical Retrace Start CR12 Vertical Display End CR15 Vertical Blanking Start CR18 Line Compare
Note:	*These registers have overflow bits in the Overflow Register (CR7)*
1	Select Row Scan Counter This bit allows compatibility with the Hercules graphics card and other 400 line graphics systems. 0 = No substitution takes place. 1 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time.
0	Compatibility Mode This bit allows compatibility with the IBM Color Graphics Adapter. 0 = No substitution takes place. 1 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time.

CR18 Line Compare Register 3B5/3D5 R/W

Index 18

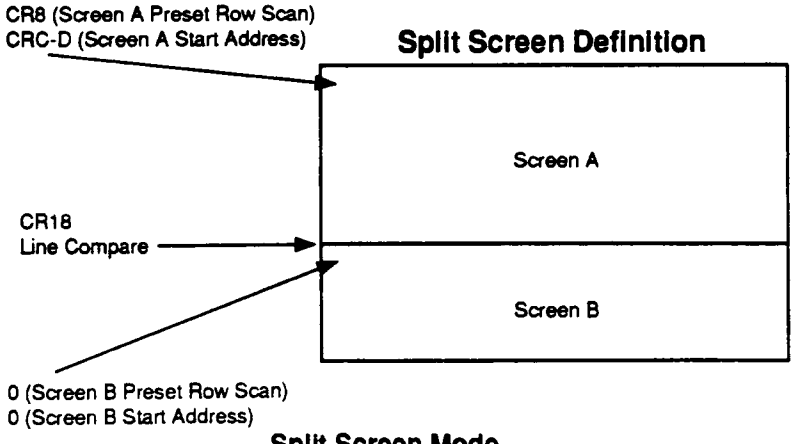


This register contains the 8 low-order bits (bits 0 through 7) of the 10 bit Line Compare register. CR7 bit 4 contains bit 8 of this register and CR9 bit 6 contains bit 9. When the horizontal scan line counter value is equal to the contents of the Line Compare register, the memory address generator and the character row scan count are cleared.

Split Screen Definition

The screen area where the Line Compare register points is called Screen A and the screen area below that point is called Screen B (see figure below). In the standard EGA and VGA, Screen A may be smooth scrolled vertically and panned horizontally, but Screen B cannot. The VGA provides a control over whether screen B pans with screen A or is stationary when screen A is panned (AR10 bit-5).

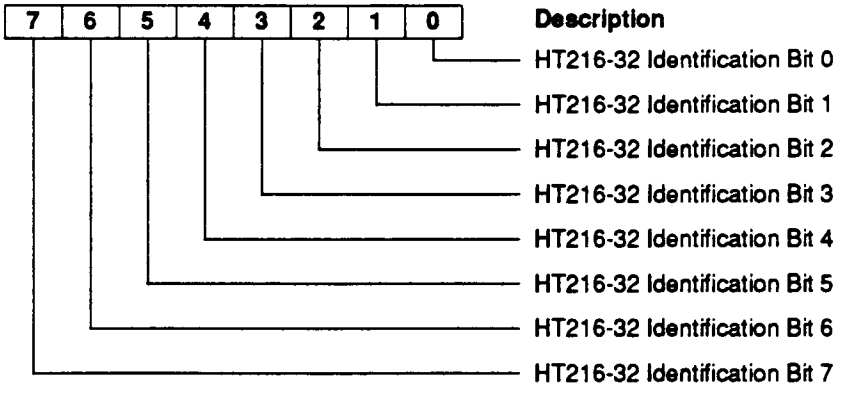
The Line Compare register determines the point where Screen A ends and Screen B begins. It is typically set to a value of FF (along with a One in CR7 bit-4 and CR9 bit-6) to disable the split-screen feature (no comparison ever occurs so Screen B never starts).



Split Screen Mode

CR1F Identification Register 3B5/3D5 (R)

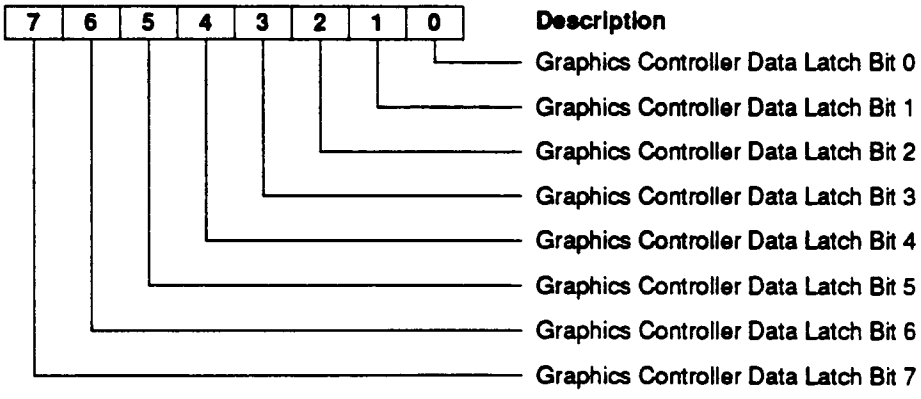
Index 1F



This read-only register is used to determine if a graphics adapter supports the HT extension registers. The exact nature and capabilities of the chip installed can be determined by reading the chip revision registers (Extension Reg 8E and Extension Reg 8F). The value read back from this register is the current value in the Start Address High Register (CRC) exclusive OR'd with EA. For example, if CRC contains 0, this register will read back as EA; if CRC contains FF, this register will read back as 15; etc.

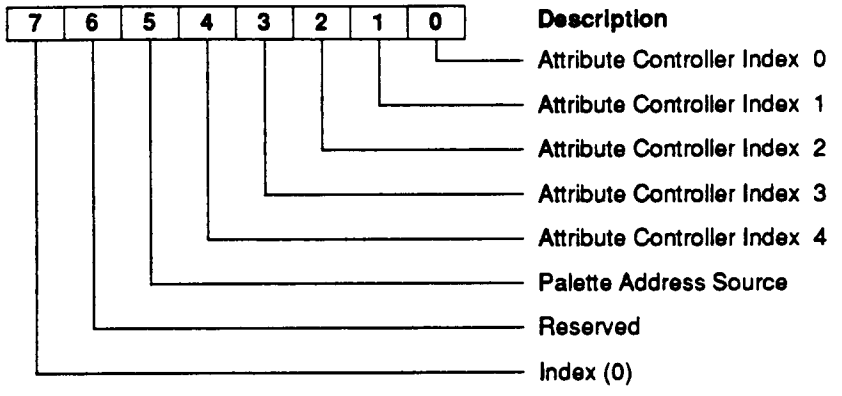
CR22 Graphics Controller Data Latches 3B5/3D5 (R)

Index 22



This register is used to read the state of the Graphics Controller Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (Graphics Reg4 bits [1:0]) and is in the range 0-3.

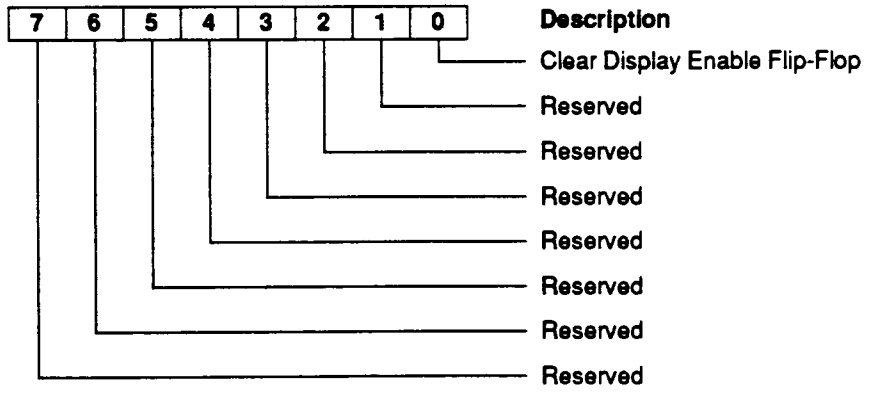
CR24 Attribute Controller Index/Data Latch 3B5/3D5 (R)
Index 24



This register is used to read back the state of the attribute controller index/data latch.

Note: *A read from this register returns the same information as a read returned by Extension Register 83.*

CR3x Clear Vertical Display Enable Flip-Flop 3B5/3D5 (W)
Index 30-3F



This register clears the display. Writing odd values to this register causes the Vertical Display Enable Flip-Flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer retrace period. When the vertical display is terminated early, the screen blanks early for one frame, causing a minor visual disturbance, and the Sequencer directs more display memory cycles to the CPU.

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Extension Registers

The extension registers in the HT216 are used to provide for the wide variety of extended features beyond those provided by IBM's standard VGA. All extension registers are implemented as an extension to the Timing Sequencer I/O port locations, 0x3C4 for index and 0x3C5 for data. To access the extensions a value of EA must be written to the data port 3C5 with the index port 3C4 set at 0x06. To disable access to the extension registers, a value of AE must be written.

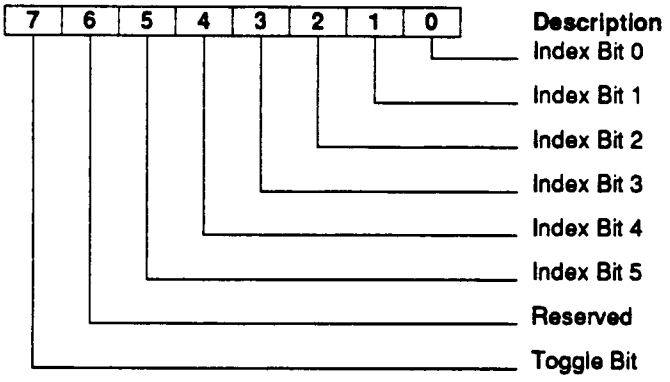
Desc.	Register Name	Bits	Access	Index	Port
XAAI	Extended Alternate Attribute Index	7	R/W	83	3C4
PIR	Product Revision	8	R	8E	3C4
PID	Product Identification	8	R	8F	3C4
PPA	Pointer Pattern Address	8	R/W	94	3C4
PXH	Pointer Horizontal Position High	3	R/W	9C	3C4
PXL	Pointer Horizontal Position Low	8	R/W	9D	3C4
PYH	Pointer Vertical Position High	2	R/W	9E	3C4
PYL	Pointer Vertical Position Low	8	R/W	9F	3C4
GRL0	Plane 0 Background Latch	8	R/W	A0	3C4
GRL1	Plane 1 Background Latch	8	R/W	A1	3C4
GRL2	Plane 2 Background Latch	8	R/W	A2	3C4
GRL3	Plane 3 Background Latch	8	R/W	A3	3C4
CLKSEL	Extended Clock Select	4	R/W	A4	3C4
CAR	Cursor Attribute Register	3	R/W	A5	3C4
SCRAM	Scratch RAM Register	8	R/W	B3	3C4
POR0	Power On Reset 0	8	R/W	B4	3C4
POR1	Power On Reset 1	8	R	B5	3C4
POR2	Power On Reset 2	8	R	B6	3C4
POR3	Power On Reset 3	8	R	B7	3C4
MNLCK	Monochrome Lock	8	R/W	C0	3C4
MISCTL2	Miscellaneous Control 2	8	R/W	C8	3C4

Desc.	Register Name	Bits	Access	Index	Port
XLAOL	Extended Linear Address Offset Low	4	R/W	C9	3C4
HOVR	Horizontal Overflow Register	5	R/W	CA	3C4
LWMRK	Low Water Mark Register	4	R/W	CB	3C4
DMFNCTL	DM Function Control Register	4	R/W	CC	3C4
XALUCTL	Extended ALU Function Control Register	8	R/W	CD	3C4
XALUSLT	Extended ALU Function Select Register	8	R/W	CE	3C4
XLADOH	Extended Linear Address Offset High	8	R/W	CF	3C4
MISCTL1	Miscellaneous Control 1 Register	7	R/W	E0	3C4
INTRLC	Interlace Value Register	8	R/W	E1	3C4
XCHRWD	Extended Character Width Register	5	R/W	E2	3C4
HWMRK	High Water Mark Register	4	R/W	E3	3C4
LSBA	Lower Split Bank Address Value	8	R/W	E8	3C4
USBA	Upper Split Bank Address Value	8	R/W	E9	3C4
SWSTB	Switch Strobe Register	--	W	EA	3C4
OVSL	Overstrike Row Scan Match Value	5	R/W	EB	3C4
FGLAT0	Foreground Latch Plane 0	8	R/W	EC	3C4
FGLAT1	Foreground Latch Plane 1	8	R/W	ED	3C4
FGLAT2	Foreground Latch Plane 2	8	R/W	EE	3C4
FGLAT3	Foreground Latch Plane 3	8	R/W	EF	3C4
	Reserved	--	R/W	F3	3C4
	Reserved	--	R/W	F4	3C4

Desc.	Register Name	Bits	Access	Index	Port
FBPAT	Foreground/Background Pattern Register	8	R/W	F5	3C4
RAMBKSL	1 MByte RAM Bank Select Register	8	R/W	F6	3C4
SWRB	Switch Readback Register	8	R	F7	3C4
XCLKCTL	Extended Clock Control Register	8	R/W	F8	3C4
XPSEL	Extended Page Select Register	1	R/W	F9	3C4
XFCOLR	Extended Foreground Color Register	8	R/W	FA	3C4
XBCOLR	Extended Background Color Register	8	R/W	FB	3C4
COMCTL	Compatibility Control Register	8	R/W	FC	3C4
DMCTRL	Display Memory Controller Timing	5	R/W	FD	3C4
FBCTRL	Foreground/Background Control Register	5	R/W	FE	3C4
16INTR	16 Bit Interface Control Register	6	R/W	FF	3C4

XAAI — Extended Alternate Attribute Index — 3C4 R/W

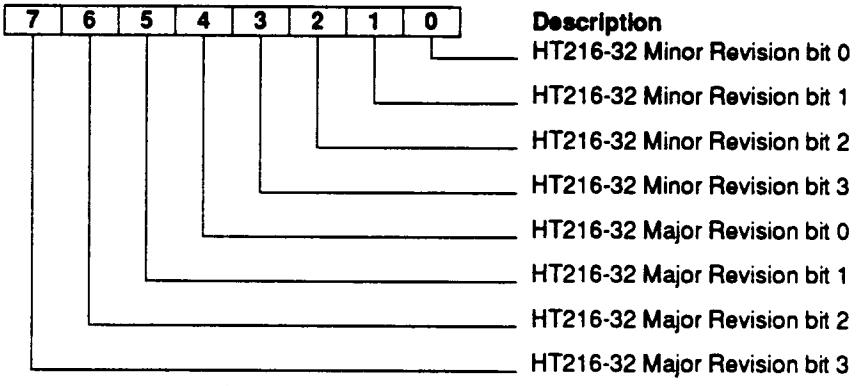
Index 83



Bits [5:0] of this register represent the Attribute Controller Index. Bit 7 toggles between Index and Data mode (0 = Index, 1 = Data).

PIR — Product Revision Register — 3C4(R)

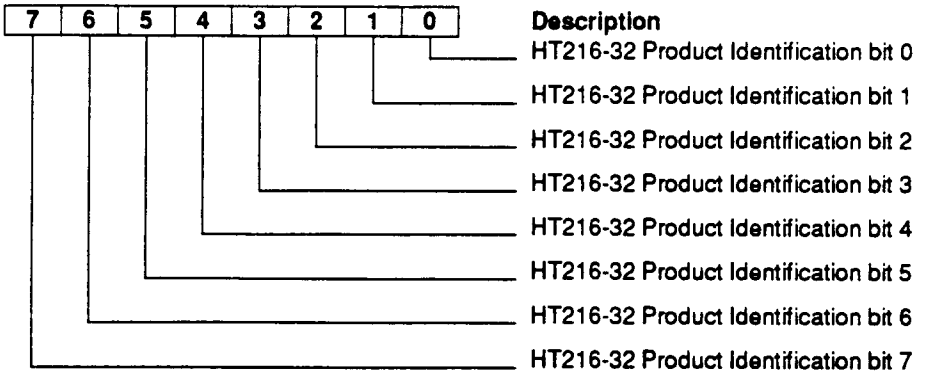
Index 8E



Bit	Bit Name	POR	Description
7	MAJREV.3	0	
6	MAJREV.2	1	
5	MAJREV.1	1	
4	MAJREV.0	0	
3	MINREV.3	0	
2	MINREV.2	0	
1	MINREV.1	0	
0	MINREV.0	0	

PID Product Identification Register 3C4(R)

Index 8F

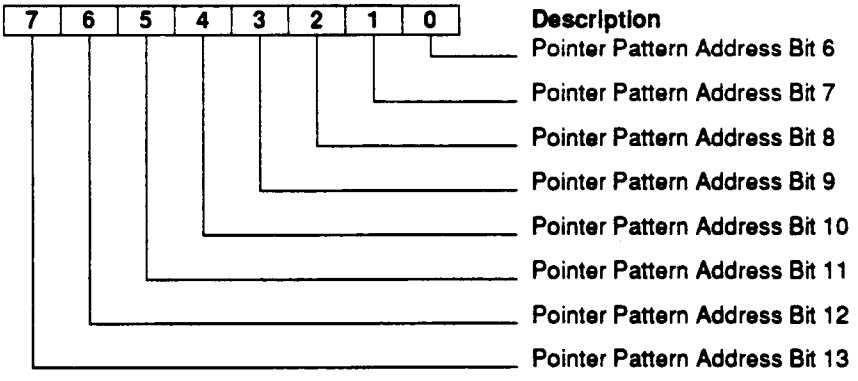


Bit	Bit Name	POR	Description
7	HT216-32PID.7	0	
6	HT216-32PID.6	1	
5	HT216-32PID.5	1	
4	HT216-32PID.4	1	
3	HT216-32PID.3	0	
2	HT216-32PID.2	1	
1	HT216-32PID.1	1	
0	HT216-32PID.0	1	

Indices 0x8E and 0x8F are used to properly identify the HT216-32 and its current revision. The HT216-32 product identification code is 78H. The major revision is used typically to indicate product revisions which incorporate new features or performance enhancements, while the minor revision indicates product revisions for fixing design and/or functional bugs. Please note that the major revision level for the initial release of the HT216-32 is 61H. Both registers are read only.

PPA — Pointer Pattern Address Register — 3C4 R/W

Index 94



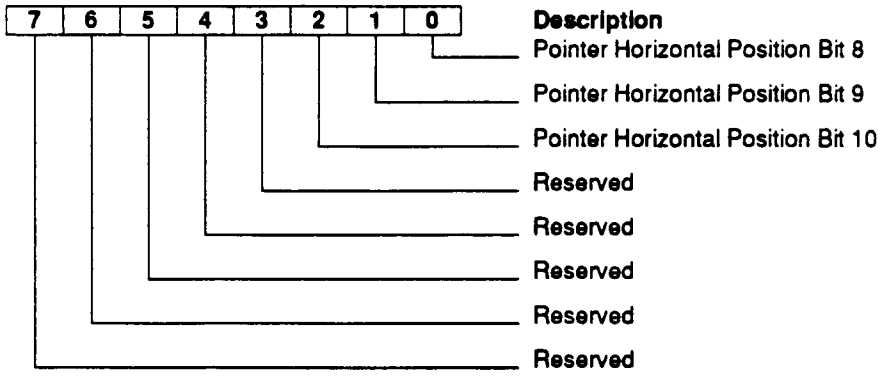
Bit	Bit Name	POR	Description
7	PPA.7	1	
6	PPA.6	1	
5	PPA.5	1	
4	PPA.4	1	
3	PPA.3	1	
2	PPA.2	1	
1	PPA.1	1	
0	PPA.0	1	

The pointer pattern address register, index 94, provides pointer pattern address bits 6 through 13. The entire pointer pattern address is constructed as follows:

Address	Source
PPadd.17	Index 0xFF bit 6 (PTBS.1)
PPadd.16	Index 0xFF bit 5 (PTBS.0)
PPadd.15	Always 1
PPadd.14	Always 1
PPadd.13	Index 0x94 bit 7 (PPA.7)
PPadd.12	Index 0x94 bit 6 (PPA.6)
PPadd.11	Index 0x94 bit 5 (PPA.5)
PPadd.10	Index 0x94 bit 4 (PPA.4)
PPadd.9	Index 0x94 bit 3 (PPA.3)
PPadd.8	Index 0x94 bit 2 (PPA.2)
PPadd.7	Index 0x94 bit 1 (PPA.1)
PPadd.6	Index 0x94 bit 0 (PPA.0)
PPadd.5	0 for AND mask, 1 for XOR mask
PPadd.4	Pointer row bit 4
PPadd.3	Pointer row bit 3
PPadd.2	Pointer row bit 2
PPadd.1	Pointer row bit 1
PPadd.0	Pointer row bit 0

PXH Pointer Horizontal Position High Register 3C4 R/W

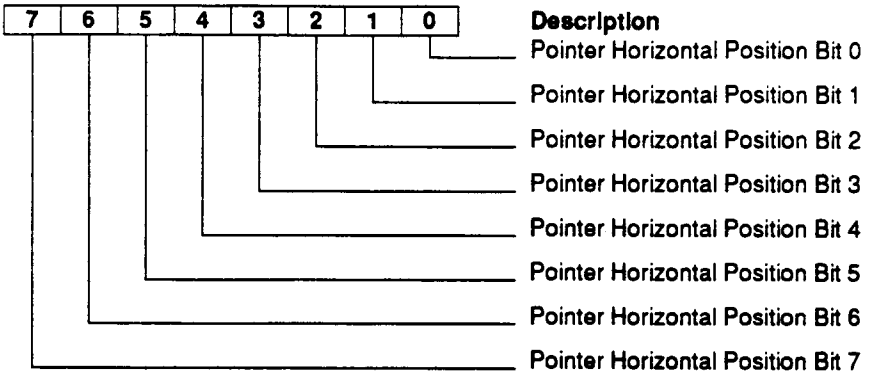
Index 9C



Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	-		
2	PXH.2	0	
1	PXH.1	0	
0	PXH.0	0	

PXL Pointer Horizontal Position Low Register 3C4 R/W

Index 9D

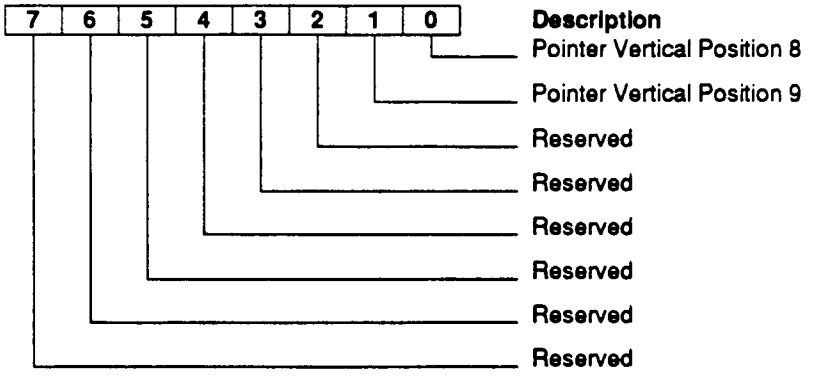


Bit	Bit Name	POR	Description
7	PXL.7	0	
6	PXL.6	0	
5	PXL.5	0	
4	PXL.4	0	
3	PXL.3	0	
2	PXL.2	0	
1	PXL.1	0	
0	PXL.0	0	

The pointer horizontal position low and high registers, indices 0x9C and 0x9D, define the pixel x-coordinate position on which the pointer begins to appear (i.e., when enabled by 0xA5.7). This necessarily implies that the maximum number of displayed pixels on a horizontal line is 2048.

PYH — Pointer Vertical Position High Register — 3C4 R/W

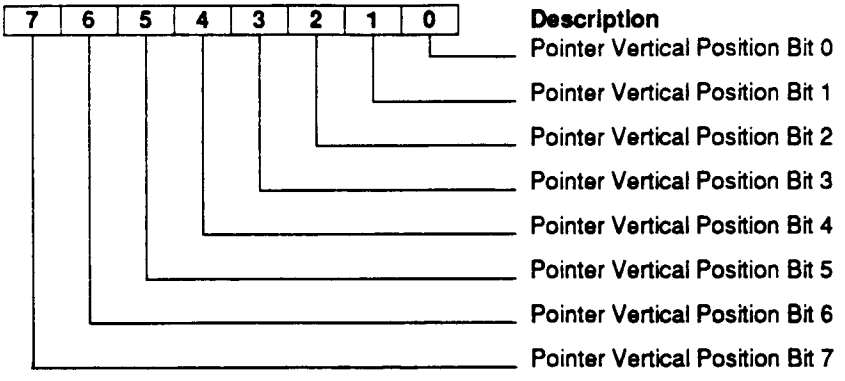
Index 9E



Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	-		
2	-		
1	PYH.1	0	
0	PYH.0	0	

PYL — Pointer Vertical Position Low Register — 3C4 R/W

Index 9F

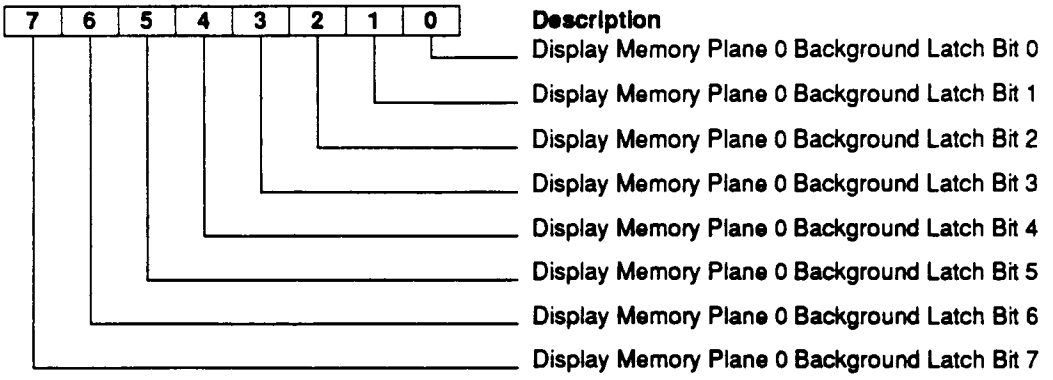


Bit	Bit Name	POR	Description
7	PYL.7	0	
6	PYL.6	0	
5	PYL.5	0	
4	PYL.4	0	
3	PYL.3	0	
2	PYL.2	0	
1	PYL.1	0	
0	PYL.0	0	

The pointer vertical position low and high registers, indices 0x9E and 0x9F, define the pixel y-coordinate position on which the pointer begins to appear (i.e., when enabled by 0xA5.7). This necessarily implies that the maximum number of vertically displayed lines in a frame (or in each field of a frame in interlace modes) is 1024.

GRL0 Plane 0 Background Latch Register 3C4 R/W

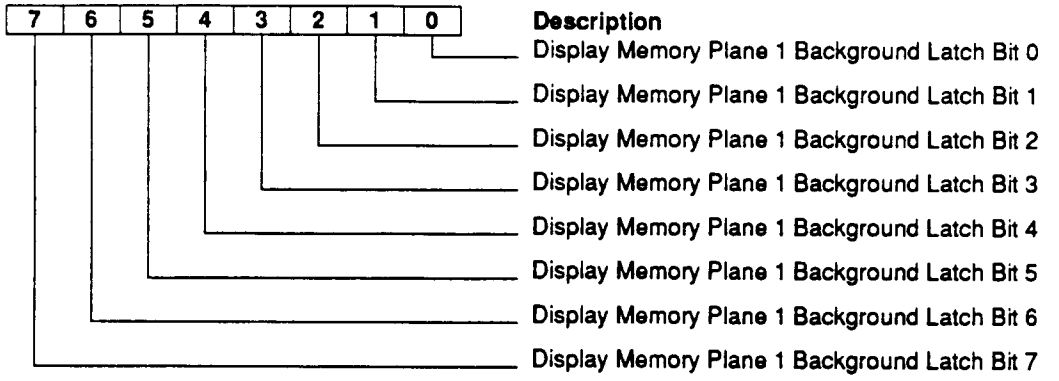
Index A0



Bit	Bit Name	POR	Description
7	GRL0.7	0	
6	GRL0.6	0	
5	GRL0.5	0	
4	GRL0.4	0	
3	GRL0.3	0	
2	GRL0.2	0	
1	GRL0.1	0	
0	GRL0.0	0	

GRL1 Plane 1 Background Latch Register 3C4 R/W

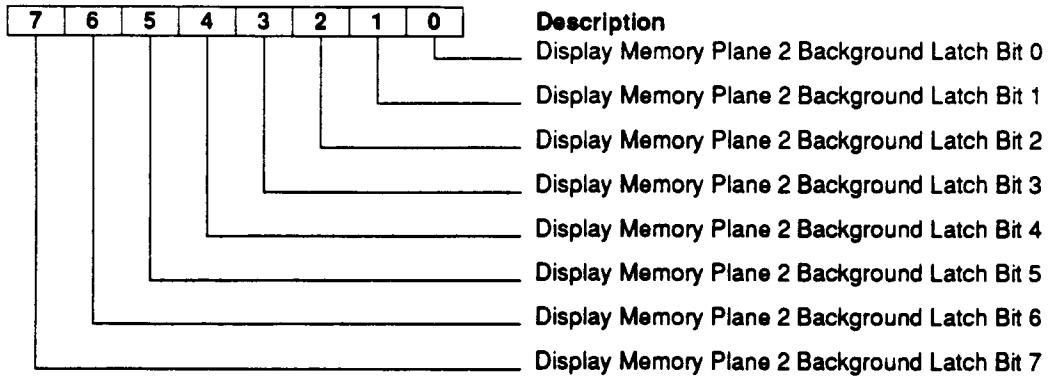
Index A1



Bit	Bit Name	POR	Description
7	GRL1.7	0	
6	GRL1.6	0	
5	GRL1.5	0	
4	GRL1.4	0	
3	GRL1.3	0	
2	GRL1.2	0	
1	GRL1.1	0	
0	GRL1.0	0	

GRL2 Plane 2 Background Latch Register 3C4 R/W

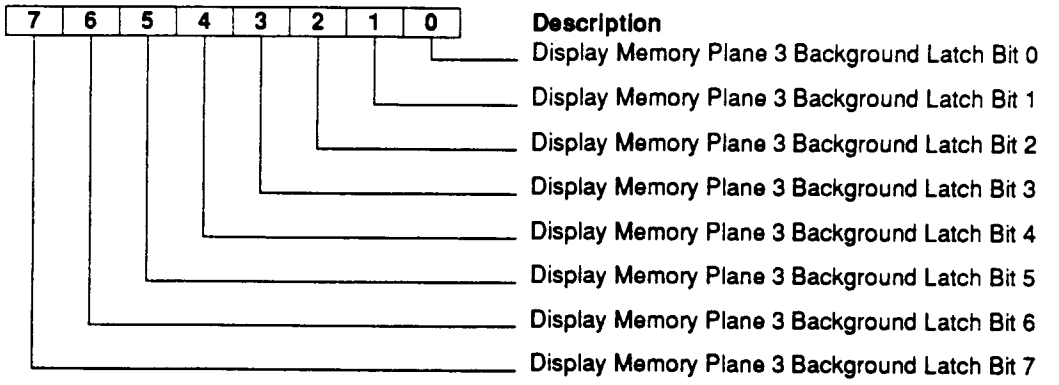
Index A2



Bit	Bit Name	POR	Description
7	GRL2.7	0	
6	GRL2.6	0	
5	GRL2.5	0	
4	GRL2.4	0	
3	GRL2.3	0	
2	GRL2.2	0	
1	GRL2.1	0	
0	GRL2.0	0	

GRL3 Plane 3 Background Latch Register 3C4 R/W

Index A3

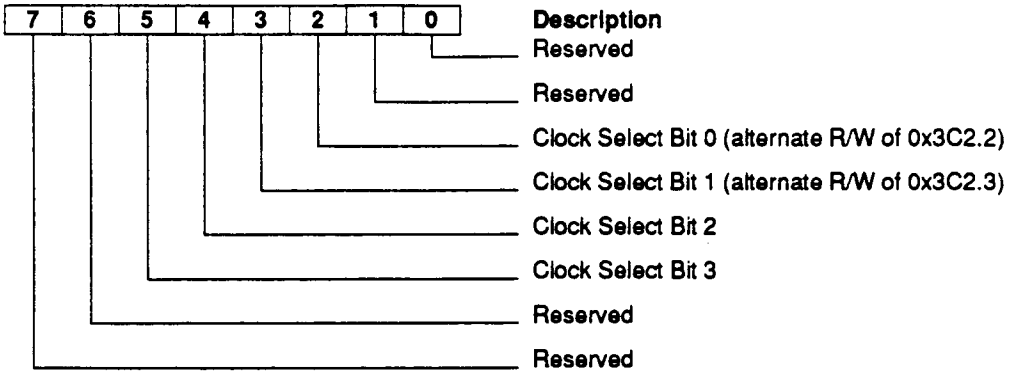


Bit	Bit Name	POR	Description
7	GRL3.7	0	
6	GRL3.6	0	
5	GRL3.5	0	
4	GRL3.4	0	
3	GRL3.3	0	
2	GRL3.2	0	
1	GRL3.1	0	
0	GRL3.0	0	

The four background latch registers, indices 0xA0, 0xA1, 0xA2 and 0xA3, provide for I/O access to all four planes of the Display Memory (DM) background latch. This is an alternative to the "standard" method of performing a CPU memory write operation to DM (which is destructive) followed by a memory operation to the same location, thereby loading the background latches with the desired information. Having I/O access to the background latches also facilitates save and restore operations in multi-tasking environments.

CLKSEL — Extended Clock Select Register — 3C4 R/W

Index A4

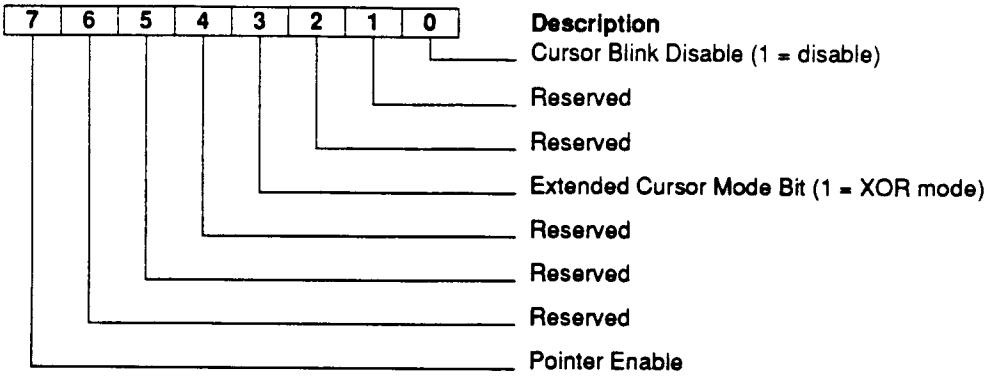


Bit	Bit Name	POR	Description
7	-		
6	-		
5	CLKSEL.3	0	
4	CLKSEL.2	0	
3	CLKSEL.1	0	
2	CLKSEL.0	0	
1	-		
0	-		

The extended clock select register, index 0xA4, defines the four clock select bits that are output to an external clock synthesizer chip. Only bits 4 and 5 of this register are unique; bits 2 and 3 are miscellaneous control register bits 2 and 3, the standard VGA clock select bits. This register provides an alternate I/O read/write location such that all four clock select bits may be read or written simultaneously.

CAR — Cursor Attribute Register — 3C4 R/W

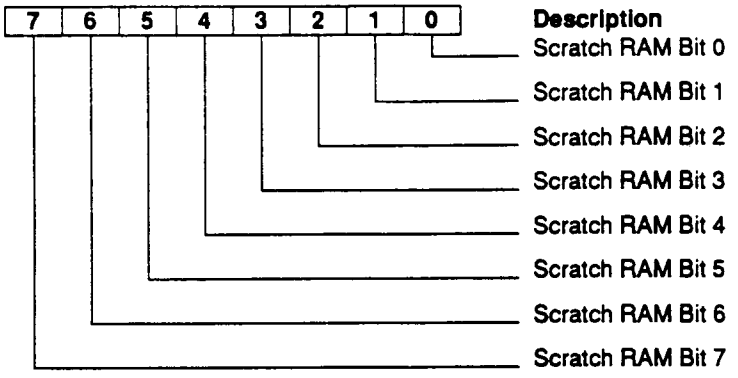
Index A5



Bit	Bit Name	POR	Description
7	HCURE	0	Pointer Enable 0 = Hardware cursor (i.e., pointer) disabled 1 = Hardware cursor enabled
3	XCMD	0	Extended Cursor Mode Bit 0 = Text mode cursor is opaque (IBM compatible) 1 = Text mode cursor is transparent
0	XCBK	0	Cursor Blink Disable 0 = Text mode cursor blinks normally (IBM compatible) 1 = Text mode cursor does not blink

SCRAM — Scratch RAM Register — 3C4 R/W

Index B3

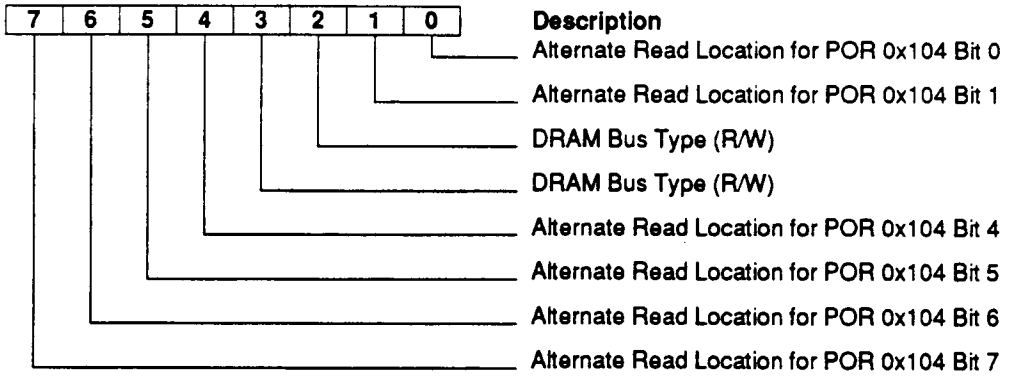


Bit	Bit Name	POR	Description
7	SCRAM.7	0	
6	SCRAM.6	0	
5	SCRAM.5	0	
4	SCRAM.4	0	
3	SCRAM.3	0	
2	SCRAM.2	0	
1	SCRAM.1	0	
0	SCRAM.0	0	

Index 0xB3 is an 8 bit read/write register available as temporary storage.

POR0 Power On Reset 0 Register 3C4(R)

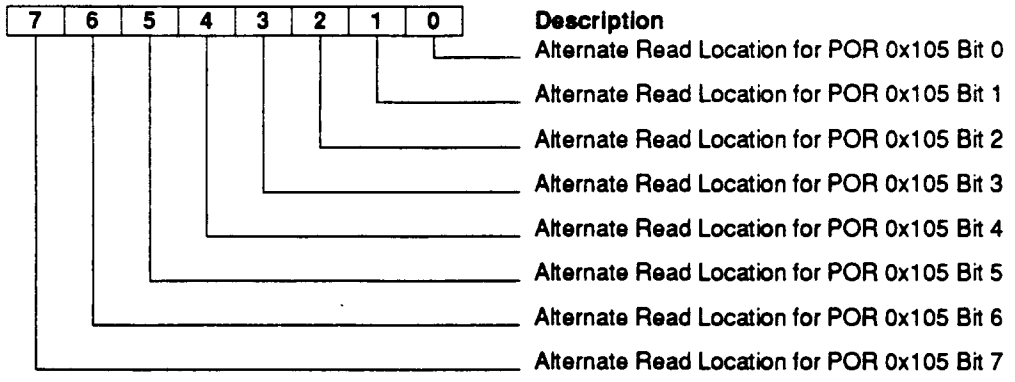
Index B4



Bit	Bit Name	Description
7	APOR0.7	
6	APOR0.6	
5	APOR0.5	
4	APOR0.4	
[3:2]	APOR0.3:2	DRAM Bus Type (These bits are R/W) 00 = Reserved 01 = 16 bit DRAM bus 10 = 32 bit DRAM bus (default) 11 = Reserved
1	APOR0.1	
0	APOR0.0	

POR1 Power On Reset 1 Register 3C4(R)

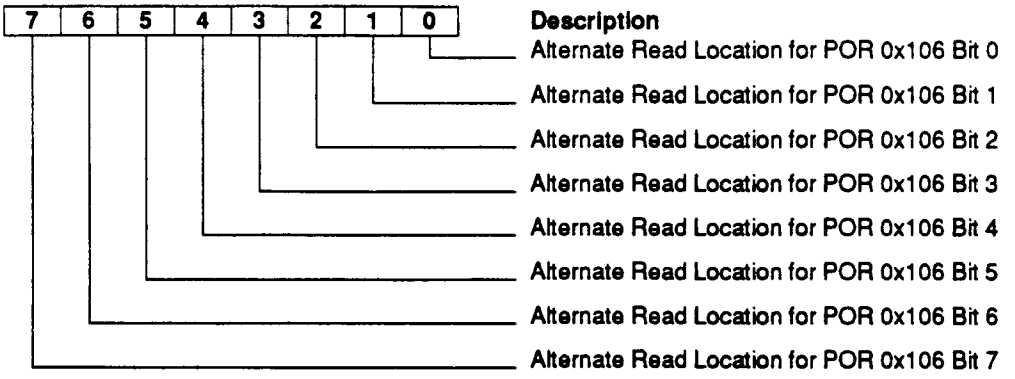
Index B5



Bit	Bit Name	Description
7	APOR1.7	
6	APOR1.6	
5	APOR1.5	
4	APOR1.4	
3	APOR1.3	
2	APOR1.2	
1	APOR1.1	
0	APOR1.0	

POR2 Power On Reset 2 Register 3C4(R)

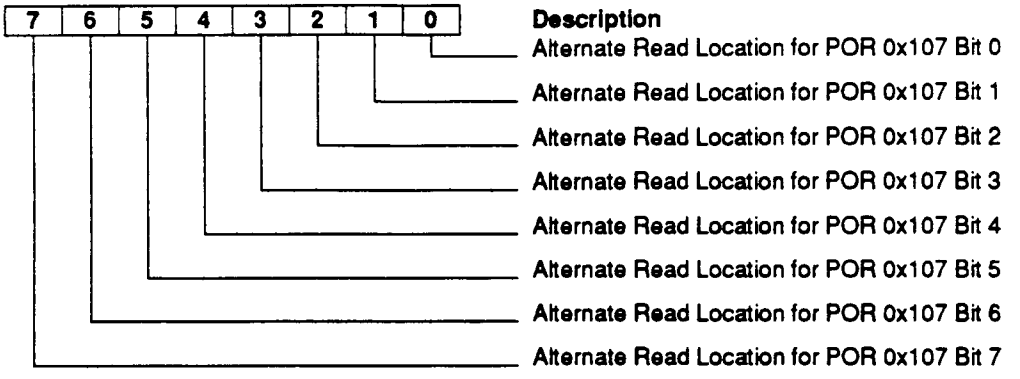
Index B6



Bit	Bit Name	Description
7	APOR2.7	
6	APOR2.6	
5	APOR2.5	
4	APOR2.4	
3	APOR2.3	
2	APOR2.2	
1	APOR2.1	
0	APOR2.0	

POR3 Power On Reset 3 Register 3C4(R)

Index B7

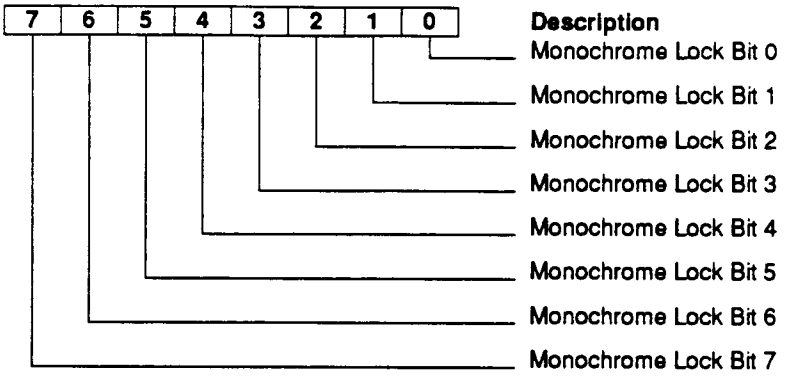


Bit	Bit Name	Description
7	APOR3.7	
6	APOR3.6	
5	APOR3.5	
4	APOR3.4	
3	APOR3.3	
2	APOR3.2	
1	APOR3.1	
0	APOR3.0	

These registers, indices 0xB4, 0xB5, 0xB6 and 0xB7, provide for an alternate read source of the POR registers 0x104, 0x105, 0x106 and 0x107 allowing software to inspect the POR values without having to put the HT216-32 in Setup mode.

MNLCK — Monochrome Lock Register — 3C4 R/W

(write 0x09 to arm, 0x18 to lock) — Index C0



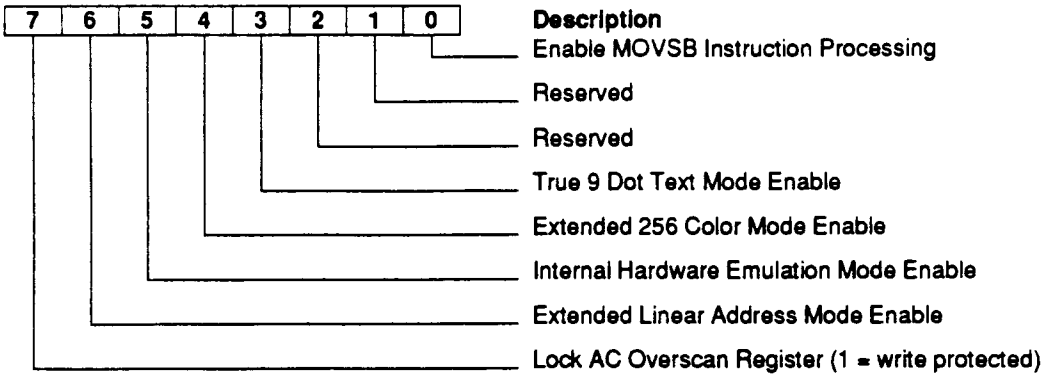
Bit	Bit Name	POR	Description
7	MNLCK.7	0	
6	MNLCK.6	0	
5	MNLCK.5	0	
4	MNLCK.4	0	
3	MNLCK.3	0	
2	MNLCK.2	0	
1	MNLCK.1	0	
0	MNLCK.0	0	

This register, index 0xC0, can lock the HT216-32 in monochrome emulation mode. This is useful if there is another VGA in the system and the HT216-32 is programmed to emulate a co-resident MDA or Hercules adapter. Once locked, I/O decodes 0x3Cy are removed from the HT216-32's I/O decode space (where 'y' implies any single digit hex value). In order to trip the lock, it must first be armed. This is accomplished by writing a value of 0x09 to this register. Once armed, writing a value of 0x18 to this register will trip the lock. Writing any other value or performing an I/O read will disarm the lock. Once locked, there are two possible methods of unlocking it. The first is a power-on (or "hard") reset. The second is by "disabling" the VGA by setting the Disable pin to 1 in a Micro Channel system, or by setting bit 3 of port 0x46E8 to a zero (0) in all other configurations.

Note: *This latter method will only reset the "trip"; the locking mechanism will still be armed.*

MISCTL2 Miscellaneous Control 2 Register 3C4 R/W

Index C8

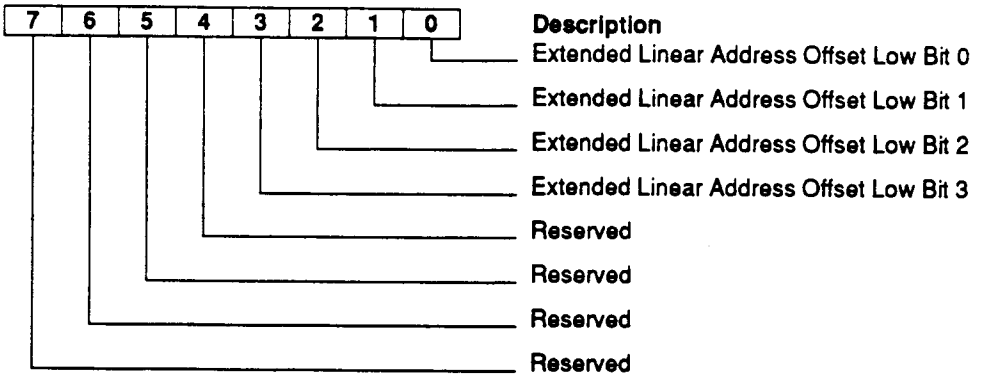


Bit	Bit Name	POR	Description
7	LOSR	0	Lock AC Overscan Register 0 = Write access to Attribute Controller overscan register (AC index 0x11) is allowed. 1 = Write access to AC overscan register is denied.
6	XLAM	0	Extended Linear Address Mode Enable 0 = Extended linear address mode disabled. 1 = Extended linear address mode enabled. In this mode, the 4 bit value in the Extended Linear Address Low Offset register (index 0xC9) is used as a match against upper address bits A[23:20] to point to a 1MByte address offset in upper system memory through which Display Memory can be accessed. (The 386DX also uses the 8 bit value in the Extended Linear Address High Offset register at index 0x3CF to match against A[31:24]. This eliminates the need for the paging required when the standard 64KByte window at 0x0A0000 is used.
5	IEME	0	Internal Hardware Emulation Mode Enable 0 = Internal Hardware Emulation mode disabled. 1 = Internal Hardware Emulation mode enabled. When activated, the HT216-32 will emulate either the CGA color, or MDA/Hercules monochrome adapters.

4	E256	0	Extended 256 Color Mode Enable 0 = IBM VGA compatible 256 color mode (i.e., each 8 bit pixel value is formed by collecting two nibbles over 2 PCLK's from the Attribute Controller output - the 8 bit output PEL is 1/2 the frequency of the PCLK). 1 = The whole 8 bits in the PEL is shifted out each PCLK.
3	T9DT	0	True 9 Dot Text Mode Enable 0 = Standard IBM compatible 9 dot text mode. 1 = In 9 dot text modes, the 9th dot of the font is accessed from plane 3 of Display Memory.
0	ENMOVSB	0	Enable MOVSB Instruction processing 0 = Not enabled 1 = Enabled (See discussion of ERCD.6) This allows the use of REPMOVSB instruction with modulo 8 offset of the CPU address. Modulo 8 offset implies that CPU address/8 gives no remainder on a double word boundary.

XLAOL — Extended Linear Address Offset Low — 3C4 R/W

Index C9

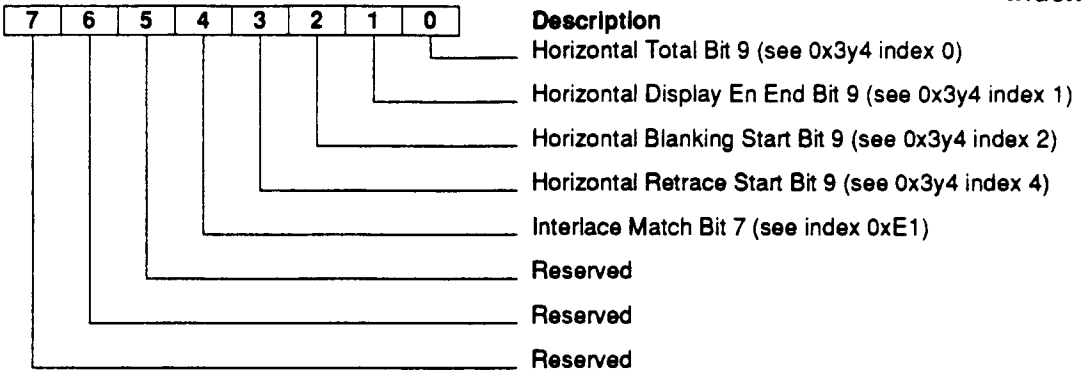


Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	XLAOL.3	0	
2	XLAOL.2	0	
1	XLAOL.1	0	
0	XLAOL.0	0	

If the extended linear address mode is enabled, this register, index 0xC9, provides the value against which SA[23:20] are compared to determine if the current Display Memory access is valid. In a 386DX configuration, the 8 bit value from index 0xCF is used to compare against SA[31:24].

HOVR — Horizontal Overflow Register — 3C4 R/W

Index CA

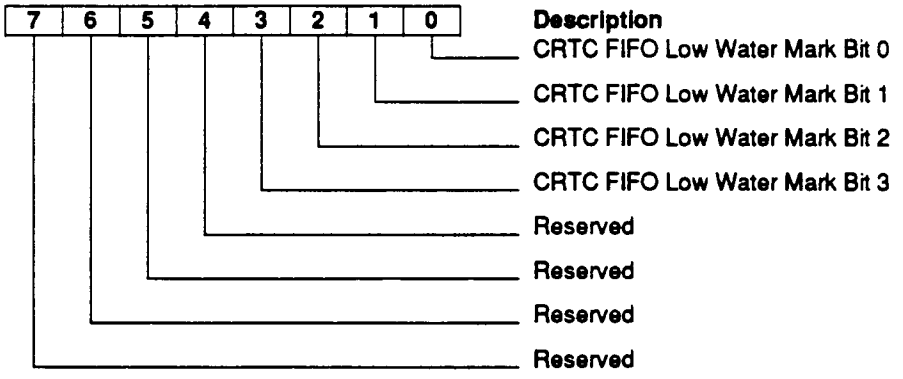


Bits	Bit Name	POR	Description
[7:5]	-		Reserved; must be set to 0.
4	INTRLC.7	0	Interlace Match Bit 7 0 = Interlace vertical sync match formed by index 0xE1 bits [0:6]. 1 = If interlace mode is enabled (0xE0.1 = 1), and if this register is enabled (0xE0.5 = 1) then this bit becomes the 8th bit of the interlace vertical sync match value. (For a more in-depth discussion of interlace mode, see description of 0xE0.1. For a more in-depth discussion of the usage of this register, see description of 0xE0.5).
3	HSS.7	0	Horizontal Retrace Start Bit 9 0 = Horizontal Retrace start match formed by 8 bits in 0x3y4 index 4. 1 = If enabled by 0xE0.5, this bit forms the 9th bit of the horizontal retrace start match.
2	HBS.7	0	Horizontal Blanking Start Bit 9 0 = Horizontal blanking start match formed by 8 bits in 0x3y4 index 2. 1 = If enabled by 0xE0.5, this bit forms the 9th bit of the horizontal blanking start match.
1	HDE.7	0	Horizontal Display Enable End Bit 9 0 = Horizontal display enable end match formed by 8 bits in 0x3y4 index 1. 1 = If enabled by 0xE0.5, this bit forms the 9th bit of the horizontal display enable end match.

0	HTOT.7	0	Horizontal Total Bit 9 0 = Horizontal total match formed by 8 bits in 0x3y4 index 0. 1 = If enabled by 0xE0.5, this bit forms the 9th bit of the horizontal total match.

LWMRK Low Water Mark Register 3C4 R/W

Index CB

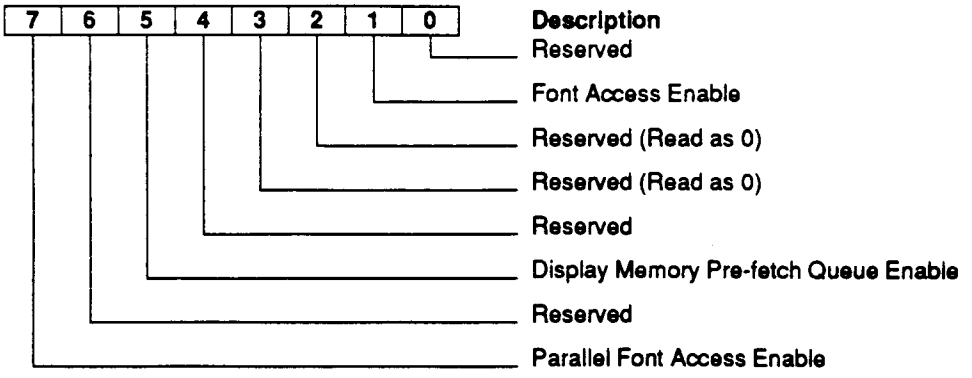


Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	LWMRK.3	0	
2	LWMRK.2	0	
1	LWMRK.1	0	
0	LWMRK.0	0	

This register, index 0xCB, forms a 4 bit value that is compared with the CRTC FIFO count. When a match occurs, the FIFO sends a fill request to the Display Memory Controller. This register is used to indicate the lowest possible count the CRTC FIFO is allowed to reach to ensure that when a character request is received there are some remaining characters in the FIFO, avoiding an under-run condition. This value must take into account the maximum possible latency for all conditions, such as another operation in progress.

DMFNCTL DM Function Control Register 3C4 R/W

Index CC



Bit	Bit Name	POR	Description
7	PFONTMDE	0	Parallel Font Access Enable 0 = Text mode fonts are only accessed from Display Memory (DM) plane 2. 1 = Fonts can be accessed from either plane 2 or plane 3. This requires that the font tables stored in plane 2 be imaged in plane 3. For example, if font accesses are currently from plane 2 AND the next font to be accessed is not in the same page as the last AND the character code of the font to be fetched is not that of a blank character, then the DM controller will begin accessing fonts from plane 3, thereby eliminating the wait for the plane 2 RAS to pre-charge. Similarly, when the proper set of conditions arise, the font source will revert to plane 2.
5	PFQE	0	Display Memory Pre-fetch Queue Enable 0 = Display Memory prefetch queue disabled. 1 = A two deep prefetch queue for DM reads will be enabled. In this mode, all valid DM reads will be matched against the address of the data stored in the 2 deep pre-fetch queue. If a match (i.e., a "hit") is found, then the data from the pre-fetch queue will be returned to the host. If there is no match (i.e., a "miss"), then the physical DM location which that address points to, as well as the next adjacent location in the same physical DM word, are loaded into the 2 pre-fetch queue locations. For example, if the HT216-32 is programmed to be in a planar mode (in which case physical DM addresses match CPU addresses), a DM

read to CPU address 0X0A000 will load physical DM address 0x0000 and 0x0001 into the pre-fetch queue; a read to CPU address 0x0A8001 will load physical Display Memory addresses 0x8001 and 0x8000 into the pre-fetch queue. In both cases the order of reads is preserved, with the CPU read completed when the first read is completed.

1 FPGMDE 0 Font Access Enable

0 = IBM VGA compatible font addressing. In this mode the font address is determined as follows:

DM Address bit	Source
[17:16]	ERF6[5:4] CRTC extended bank select bits[1:0]
[15:13]	Character Map Select[2:0] (from Sequencer Reg. 3)
[12:5]	Character Code.0 (from DM plane 0)
[4:0]	Character Row Scan Address[4:0] (from CRTC)

1 = Font address optimized for DRAM page mode accesses. In this mode, the font address is determined as follows. Note that this addressing scheme is not compatible with font load routines which store the font in DM plane 2 while the VGA is programmed in a "linear" address mode (i.e., they expect the font to be read according to the address map above). In order to avoid a font mismatch, the HT216-32 detects this "linear" font address mode and manipulates the CPU address so that the address of the CPU data (i.e., the font) read and write will match the font address as shown below. The read detection is separately controlled from the write detection:

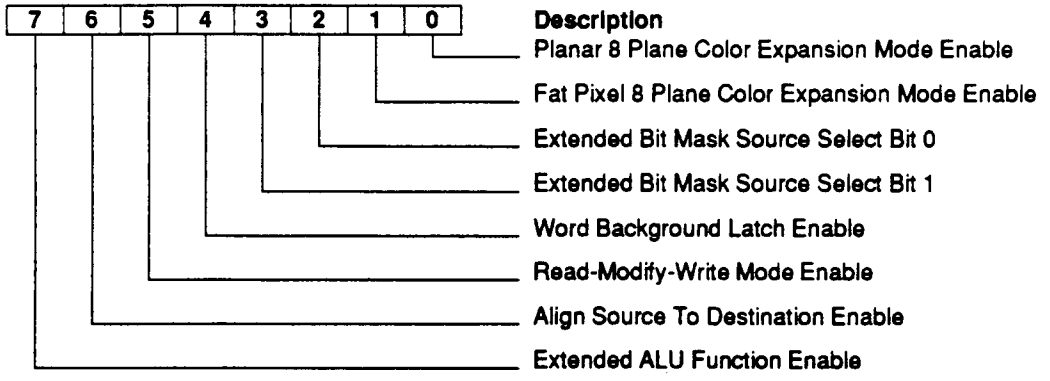
Note: *Read Detect = Chain4 AND Chain* AND GCOE* AND GCText AND Fontpgmode*
Write Detect = Chain4 AND Chain AND TSOE* AND GCText AND Fontpgmode*

DM Address bit	Source
[17:16]	0xF6[5:4] (CRTC extended bank select bits[1:0]
[15:13]	Character Map Select[2:0] (from Sequencer Reg. 3)
[12:8]	Character Row Scan Address [4:0] (from CRTC)
[7:0]	Character Code[7:0] (from DM plane 0)

Note: *This mode has priority over the pseudo-blank character access (bit 6).*

XALUCTL Extended ALU Function Control Register 3C4 R/W

Index CD



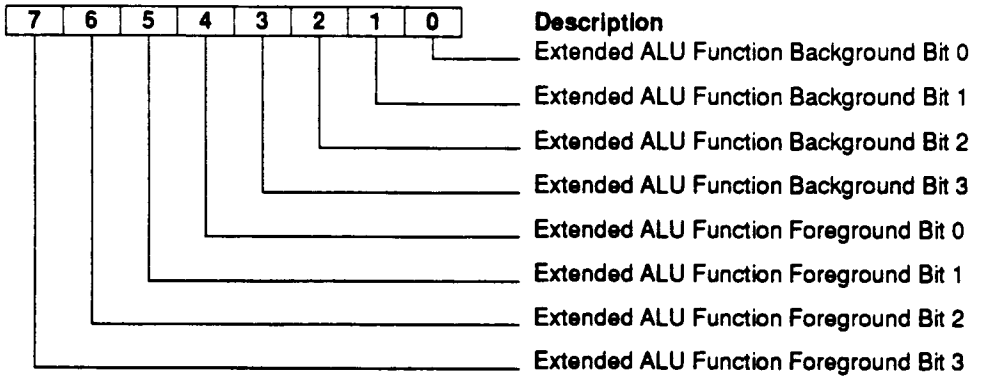
Bit	Bit Name	POR	Description
7	EXALU	0	Extended ALU Function Enable 0 = The HT216-32 ALU and bit mask function in an IBM compatible manner (this restriction does not apply to Extended Register 0xEF, the foreground/background control register). 1 = The ALU and bit mask functions are extended in the following fashion (recall that the ALU result is 8 bits wide). The ALU logical function is defined by the 8 bits in 0xCE. The lower four bits are for background operations, and the upper four bits are for foreground operations (see explanation under 0xFE[3:2],[5:4] for further detail). The 16 logical operations as defined by this register (and operating on inputs A and B) are as shown under 0xCE. The inputs A and B to the ALU and foreground/background (bits[7:4]/[3:0]) selection are determined as follows (see their respective explanations for more detail): Input B determined by bit 5 of this register Input A determined by 0xFE[3:2] F/B ROP Select determined by 0xFE[5:4] The source of the bit mask is derived from bits[3:2] of this reg. Each bit input to the ALU byte is operated on and masked independently (i.e., A7, B7 and Mask7 operate independent of bits 6 through 0, etc.)

6	ASTODE	0	Align Source To Destination Enable 0 = HT216-32 operates in VGA compatible manner. 1 = If the HT216-32 has been programmed into sequential chain 4 mode (0x3C4 index 4.4 = 1 AND 0xFC.4 = 1) AND bit 1 of this register is set to 1, then on Display Memory reads the Display Memory controller will perform the alignment necessary to ensure that the 8 adjacent 8 bit pixels to be read from Display Memory (i.e., the source), starting at the address specified during the CPU read, are stored sequentially in the extended 64 bit background latch such that they will align with the destination (i.e., when they are combined with information to be written to DM). See the explanation under bit 1 of this register for more information about this mode.
5	RMWMDE	0	Read-Modify-Write Mode Enable 0 = HT216-32 operates in VGA compatible manner. 1 = During CPU writes to DM, the HT216-32 will perform a Read-Modify-Write operation (RMW)to the address specified during CPU operation. All other functions of the HT216-32 data path, including any and all extensions to those provided by the standard VGA, will be concurrently in effect, with the exception that the contents of the background latch will not be affected during the operation (although it may participate in the determination of the information to be written to DM, as indicated above). This allows the source (e.g., the contents of the background latch, etc.) and the destination (the location in DM being read/written) to be combined in one CPU operation.
4	WBGLTE	0	Word Background Latch Enable 0 = IBM VGA compatible operation. 1 = For the upper byte of a CPU word write, use the upper location of the extended background latch (normally, the background latch stores only one physical DM location and therefore the same background latch is used for mix operations on all CPU writes). This allows the use of 16 bit patterns in planar modes. This bit has meaning only in planar modes.

[3:2]	BMSKSL.1 BMSKSL.0	0 0	Extended Bit Mask Source These bits allow the destination bit mask to be derived from various sources. The bit mask allows the individual bits within each plane of DM to be preserved during DM write operations. Bit 1 of this register (FP8PCEXP) affects how the resulting bit mask is used, as explained below. 00 = Use contents of Graphics Reg8 as bit mask source. 01 = Use CPU byte as bit mask source 1x = Use contents of 0xF5 as bit mask source.
1	FP8PCEXP	0	Fat Pixel 8 Plane Color Expansion Mode Enable 0 = HT216-32 operates in VGA compatible manner. 1 = Each byte in a CPU operation is regarded as 8 adjacent pixels. Therefore each bit in an 8 bit operation is expanded to an 8 bit field before being used in any given operation. For example, when the CPU writes a byte to DM, the HT216-32 will regard that byte as representing 8 adjacent pixels, with bit 7 of the byte as the left most displayed pixel, and bit 0 as the right most pixel. Each bit in the bit mask (as defined by bits 2 and 3 of this register) will be expanded to a byte and used to mask out the respective 8 bit pixel; bit 7 the left most pixel, bit 0 the right most pixel, etc. Both the A and B inputs to the ALU will be expanded out in a similar fashion. In this mode the 8 bytes in the extended background latch are treated as 8 adjacent pixels, but register CE operates on all 8 pixels concurrently.
0	P8PCEXP	0	Planar 8 Plane Color Expansion Mode 0 = HT216-32 operates in a VGA compatible manner. 1 = In planar modes only, the HT216-32 will operate on 16 adjacent pixels when the CPU writes a word to Display Memory. Normally, the VGA requires that in planar modes each group of 8 pixels be operated on independently. This mode in the HT216-32 allows this concept to be extended to a 16 pixel group, represented by a CPU word. In this mode, all ALU functions and registers with the exception of the extended background latch are used similarly with each byte in the word. Both the word from the CPU and the 2 bytes in the background latches are used such that bit 7 of the most significant byte represents the left most displayed pixel, and bit 0 in the least significant byte the right most displayed pixel.

XALUSLT Extended ALU Function Select Register 3C4 R/W

Index CE



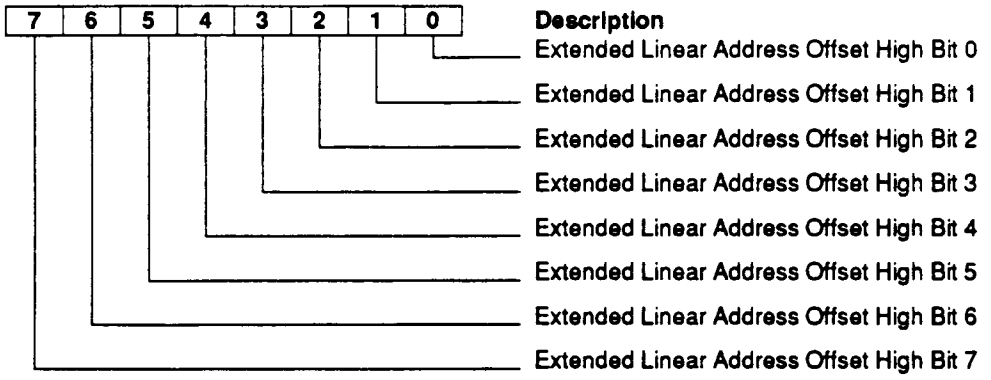
Bit	Bit Name	POR	Description
7	XFSEL.7	0	
6	XFSEL.6	0	
5	XFSEL.5	0	
4	XFSEL.4	0	
3	XFSEL.3	0	
2	XFSEL.2	0	
1	XFSEL.1	0	
0	XFSEL.0	0	

When index 0xCE is enabled by bit 7 of 0xCD (EXALU), this register defines the logical operation that the HT216-32 ALU will perform, with bits [7:4] used in foreground operations and bits [3:0] used in background operations. Bits [5:4] of 0xFE define the source of the Foreground/Background (FB) select; an FB value of 0 defines a background operation and a value of 1 a foreground operation. If the same operation is desired on both the foreground and background, both the upper and lower nibbles of this register must be programmed to the same value. The 16 possible logical operations (also referred to as Raster Operations, or ROPs) are shown in the following table.

4 bit value	Logical operation ("*" = logical NOT)
1111	Mask to 1
1110	(A OR B)
1101	(A* OR B)
1100	(B)
1011	(A OR B*)
1010	(A)
1001	(A Exclusive OR B)*
1000	(A AND B)
0111	(A AND B)*
0110	(A Exclusive OR B)
0101	(A)*
0100	(A* AND B)
0011	(B)*
0010	(B* AND A)
0001	(A OR B)*
0000	Mask to 0

XLADOH — Extended Linear Address Offset High — 3C4 R/W

Index CF

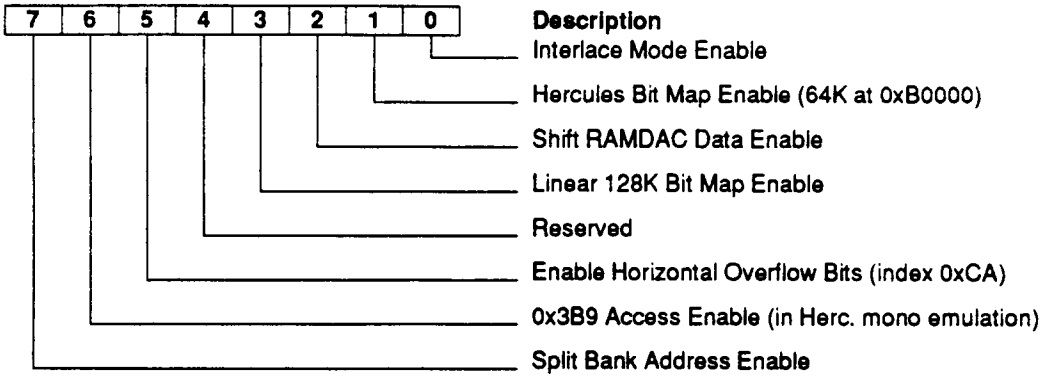


Bit	Bit Name	POR	Description
7	XLAOH.7	0	
6	XLAOH.6	0	
5	XLAOH.5	0	
4	XLAOH.4	0	
3	XLAOH.3	0	
2	XLAOH.2	0	
1	XLAOH.1	0	
0	XLAOH.0	0	

When index 0xCF is enabled by 0xC8.6 AND when in 386DX local bus mode, this register is used to match against CPU address bits[31:24] to determine if the current CPU memory read or write request is to valid HT216-32 Display Memory space.

MISCTL1 Miscellaneous Control 1 Register 3C4 R/W

Index E0



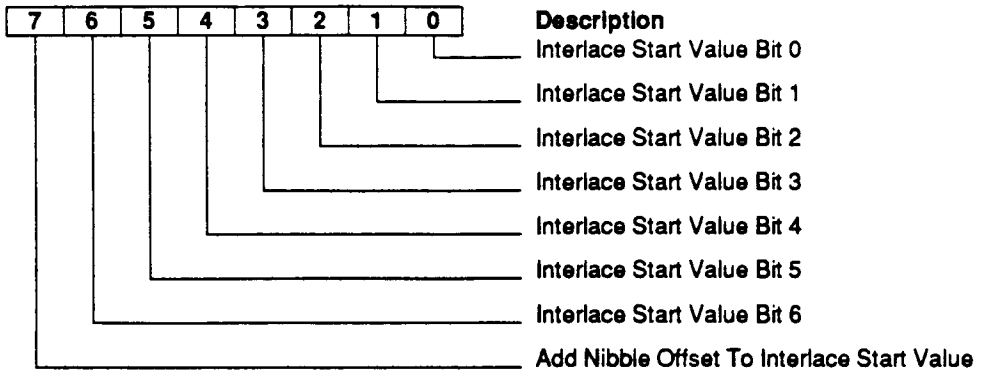
Bit	Bit Name	POR	Description
7	SBAE	0	Split Bank Address Enable 0 = If 0xC8.6 is 0, then register 0xE8 is used to define a 4KByte base page address for a 64KByte page into the HT216-32's DM (note that the HT216-32 can address up to 1MByte of Display Memory). This 64k window is addressed by the CPU through the standard 64K space at 0x0A0000. In chain4 modes (as defined by SR04.3), all 8 bits of 0xE8 are used, whereas in chain modes (as defined by GR06.1 bit 1) bit 4 is ignored and in linear modes bits 4 and 5 are ignored. 1 = If 0xC8.6 is 0, then register 0xE8 is used to define a 4KByte base page address for a 32KByte page into the HT216-32's DM. This 32K window is addressed by the CPU through a 32K window starting at 0x0A0000. Register 0xE9 is used to define a similar 32K window accessed by the CPU at 0xA8000.
6	E3B9A	0	0x3B9 Access Enable (in Herc. mono emulation) 0 = No access to 0x3B9 in Hercules emulation mode. 1 = If in Hercules emulation mode (determined by 0xC8.5 AND 0x3C2.0), then access is enabled to a 4 bit register at 0x3B9. This register is used to define the "color" displayed on the monitor and must be non-zero in this emulation mode.

5	HOVFE	0	Enable Horizontal Overflow Bits (Index 0xCA) 0 = HT216-32 operates in VGA compatible mode. 1 = Enable 9th bit of CRTC horizontal counter and start matches by enabling 9th bit overflows as defined in 0xCA. In this mode,The CRTC horizontal character counter is extended to 9 bits by enabling a 9th bit of horizontal total, display end, blank start and sync start.
3	L128	0	Linear 128K Bit Map Enable 0 = HT216-32 operates in VGA compatible manner. 1 = If in planar mode, then if a 128KByte bit map is enabled by Graphics Reg06[3:2], then access to DM is available through a linear 128K bit map at 0x0A0000. Normally, planar bit maps are limited to a 64K map at 0x0A0000.
2	SRDACDE	0	Shift RAMDAC Data Enable 0 = HT216-32 operates in VGA compatible manner 1 = On I/O reads and writes from the CPU, the HT216-32 will shift the RAMDAC data left 2 places. This is necessary to support VGA compatible modes in RAMDACs with 8 bit D/A conversion capability (as opposed to 176 compatible DACs that have only a 6 bit D/A conversion capability).
1	HCBME	0	Hercules Bit Map Enable (64K at 0xB0000) 0 = HT216-32 operates in VGA compatible manner 1 = If internal monochrome emulation mode is enabled (by 0xC8.5) AND 0x3C2.5), then setting this bit enables a linear 64KByte bit map at 0x0B0000.

0	INTLE	0	Interlace Mode Enable 0 = HT216-32 operates in VGA compatible manner 1 = Interlace mode is enabled. In this mode, each vertical frame is comprised of 2 fields, even and odd. During even fields, even scan lines are displayed; during odd fields, odd scan lines are displayed. Note that interlace mode is valid only for graphics modes (as determined by AR10.0). In order to prevent the even and odd field scan lines from displaying on top of one another, the display of the odd field is delayed by one half horizontal scan line. This is accomplished by delaying the vertical sync at the end of the even field by one half of a horizontal scan line. In order to accomplish this, 0xE1[6:0] (and 0xCA.5 if enabled AND if required) must be programmed with the integer truncation of the following value: Interlace start = [hsync_start - (htotal + 5)+2]. If [hsync_start - (htotal + 5)] is an odd value, then 0xE1.7 must be set to 1.

INTRLC Interlace Value Register 3C4 R/W

Index E1

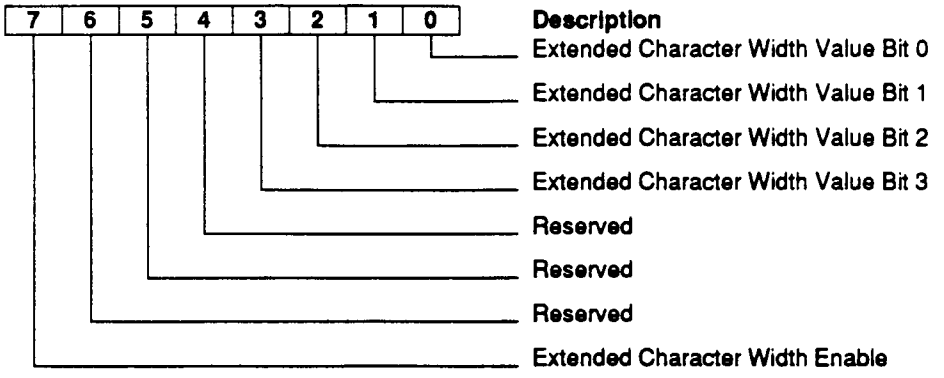


Bit	Bit Name	POR	Description
7	INTRLNO	0	
6	NTRLC.6	0	
5	NTRLC.5	0	
4	NTRLC.4	0	
3	NTRLC.3	0	
2	NTRLC.2	0	
1	NTRLC.1	0	
0	NTRLC.0	0	

This register, index 0xE1, defines a delay equal to half the total horizontal line width which is added to the start of the vertical sync at the end of the even field of an interlaced frame. This is explained in more detail under the description of 0xE0.0

XCHRWD Extended Character Width Register 3C4 R/W

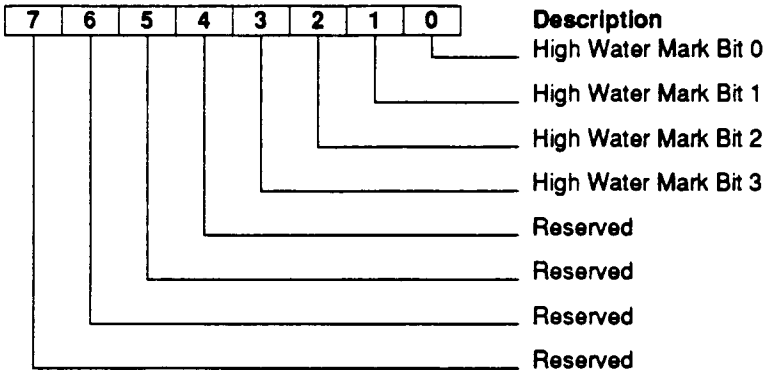
Index E2



Bit	Bit Name	POR	Description
7	XCHRWDTH	0	Extended Character Width Enable 0 = CRT characters are 8 or 9 dots wide, as determined by Sequence Reg01.0. This is the IBM VGA compatible mode of operation. 1 = Bits[3:0] of this register determine the width of the character.
[3:0]	HARDOTS.3 HARDOTS.2 HARDOTS.1 HARDOTS.0	0 0 0 0	Extended Character Width Value These bits, when enabled by bit 7 of this register, determine the width of the character displayed on the CRT. Only values less than or equal to 9 are allowed.

HWMRK High Water Mark Register 3C4 R/W

Index E3

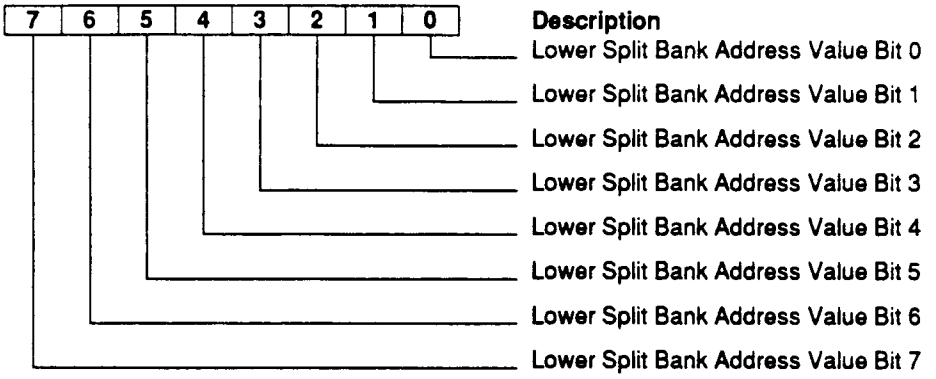


Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	HWMRK.3	0	
2	HWMRK.2	0	
1	HWMRK.1	0	
0	HWMRK.0	0	

Bits [3:0] of index 0xE3, define the CRT FIFO count which is the preset value when the FIFO will be determined to be "full". A value of 0 will cause the optimal value to be automatically calculated by the HT216-32. This register accepts user-defined values.

LSBA — Lower Split Bank Address Register — 3C4 R/W

Index E8

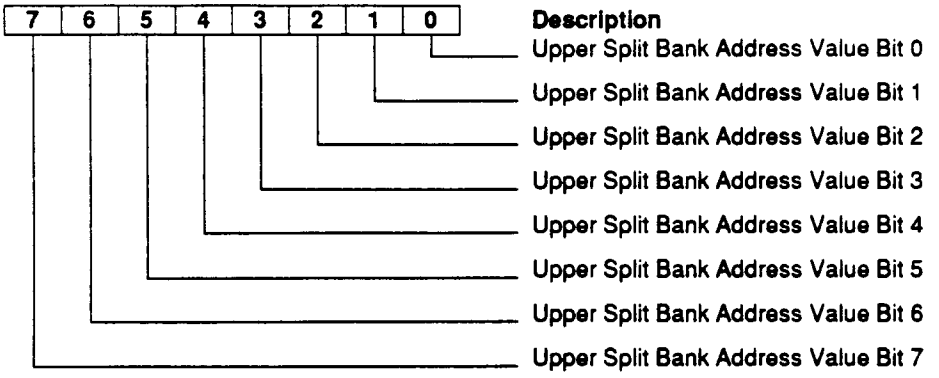


Bit	Bit Name	POR	Description
7	LSBA.7	0	
6	LSBA.6	0	
5	LSBA.5	0	
4	LSBA.4	0	
3	LSBA.3	0	
2	LSBA.2	0	
1	LSBA.1	0	
0	LSBA.0	0	

This register, index 0xE8, defines a 4 KByte base starting address for either a 64K (0xE0.7 = 0) or a 32K (0xE0.7 = 1) window starting at the DM address segment as defined by Graphic Reg 06[3:2] (usually 0x0A0000 in graphics modes). This allows the CPU to page through the HT216-32's 1 MByte total available DM. The contents of this register are added to CPU addresses [19:12], with ripple through to higher order address bits. See the explanation under Extension Reg E0.7 for more information.

USBA — Upper Split Bank Address Register — 3C4 R/W

Index E9

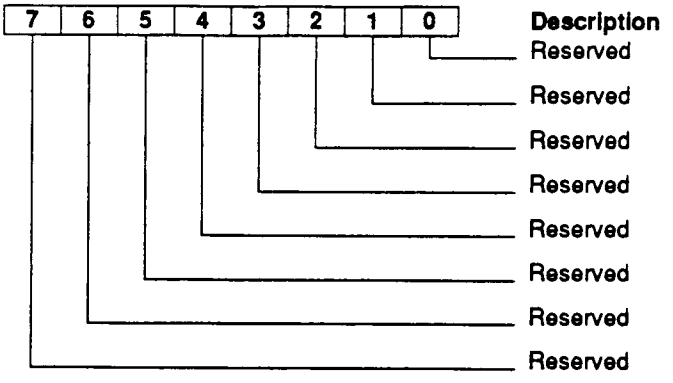


Bit	Bit Name	POR	Description
7	USBA.7	0	
6	USBA.6	0	
5	USBA.5	0	
4	USBA.4	0	
3	USBA.3	0	
2	USBA.2	0	
1	USBA.1	0	
0	USBA.0	0	

When index 0xE9 is enabled by 0xE0.7, it defines a 4 KByte base address for a 32K window starting at the DM address segment as defined by Graphics Reg. 06 [3:2] (usually 0x0A8000 in graphics modes). This allows the CPU to page through the HT216-32's 1 MByte total available DM. The contents of this register are added to CPU addresses [19:12] with ripple through to higher order address bits. See the explanation under 0xE0.7 for more information.

SWSTB Switch Strobe Register 3C4(W)

Index EA

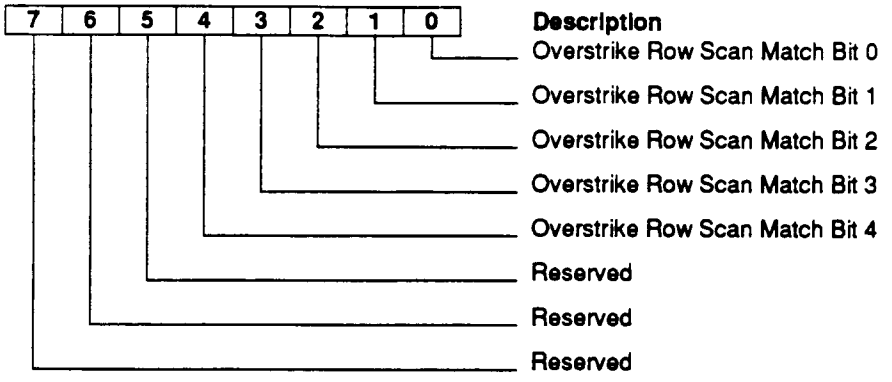


Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	-		
2	-		
1	-		
0	-		

This register, index 0xEA, is a write only register and is used to load the contents of the external switches into 0xF7. When a CPU I/O write to 0x3C5 occurs while this index is set at 0x3C4, then the external data transceiver on the upper data bus is forced off, and the external switches connected to the DAC/EPROM are dynamically loaded into 0xF7.

OVSL — Overstrike Row Scan Match Value — 3C4 R/W

Index EB

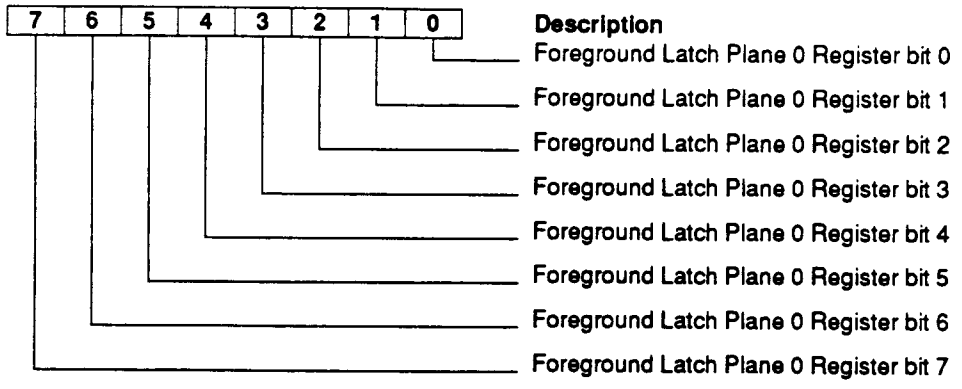


Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	OVSL.4	0	
3	OVSL.3	0	
2	OVSL.2	0	
1	OVSL.1	0	
0	OVSL.0	0	

When extended attribute mode is enabled (as determined by 0xFC.0), if the value of the extended attribute on any particular character is such that overstrike is enabled for that character, then the value stored in this register, index 0xEB, indicates the row scan line in which the overstrike line is to appear. Its function is analogous to text mode underline (as determined by CR14[4:0]). Refer to the description of 0xFC.0 for more information.

FGLAT0 Foreground Latch Plane 0 Register 3C4 R/W

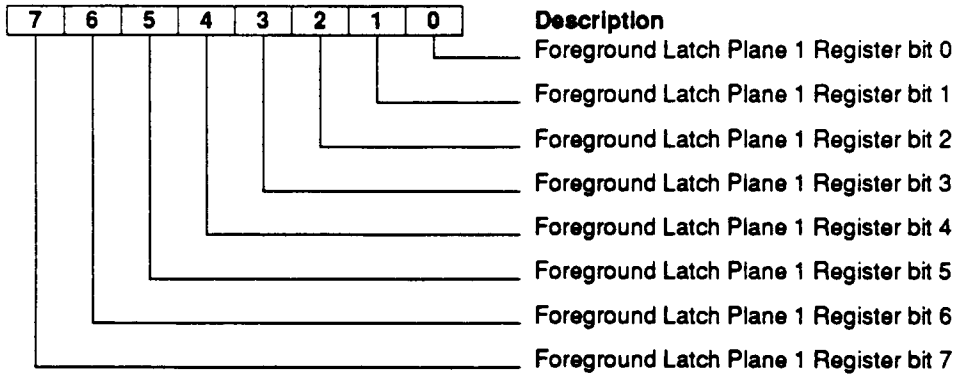
Index EC



Bit	Bit Name	POR	Description
7	FGLAT0.7	0	
6	FGLAT0.6	0	
5	FGLAT0.5	0	
4	FGLAT0.4	0	
3	FGLAT0.3	0	
2	FGLAT0.2	0	
1	FGLAT0.1	0	
0	FGLAT0.0	0	

FGLAT1 Foreground Latch Plane 1 Register 3C4 R/W

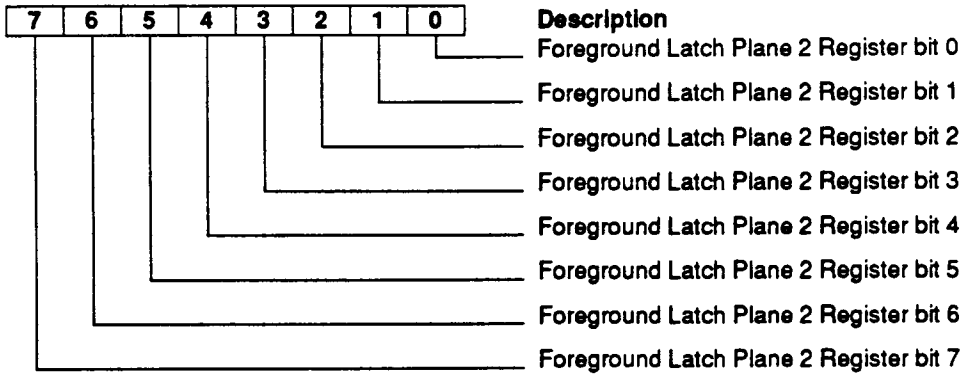
Index ED



Bit	Bit Name	POR	Description
7	FGLAT1.7	0	
6	FGLAT1.6	0	
5	FGLAT1.5	0	
4	FGLAT1.4	0	
3	FGLAT1.3	0	
2	FGLAT1.2	0	
1	FGLAT1.1	0	
0	FGLAT1.0	0	

FGLAT2 Foreground Latch Plane 2 Register 3C4 R/W

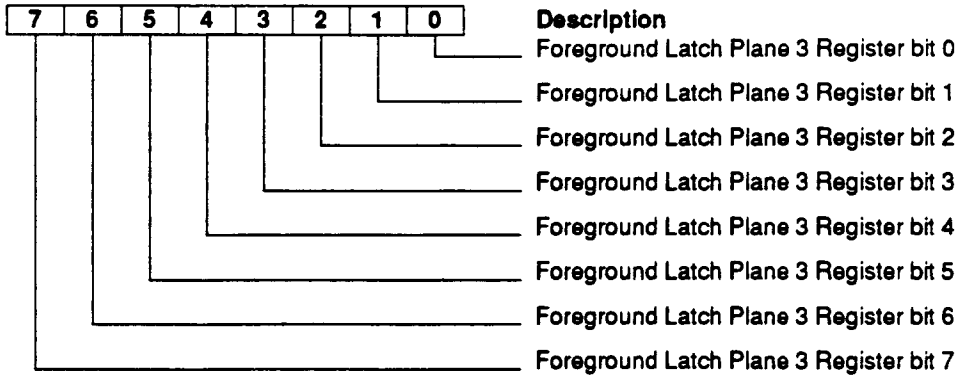
Index EE



Bit	Bit Name	POR	Description
7	FGLAT2.7	0	
6	FGLAT2.6	0	
5	FGLAT2.5	0	
4	FGLAT2.4	0	
3	FGLAT2.3	0	
2	FGLAT2.2	0	
1	FGLAT2.1	0	
0	FGLAT2.0	0	

FGLAT3 Foreground Latch Plane 3 Register 3C4 R/W

Index EF



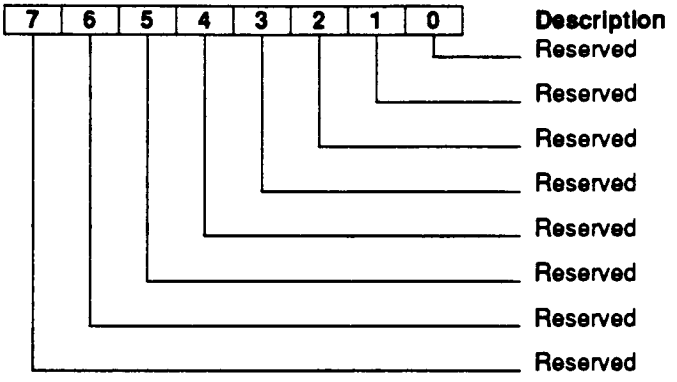
Bit	Bit Name	POR	Description
7	FGLAT3.7	0	
6	FGLAT3.6	0	
5	FGLAT3.5	0	
4	FGLAT3.4	0	
3	FGLAT3.3	0	
2	FGLAT3.2	0	
1	FGLAT3.1	0	
0	FGLAT3.0	0	

These registers, indices 0xEC, 0xED, 0xEE, 0xEF, perform two functions. When emulation mode is not enabled (as determined by 0xC8.5), then they provide the foreground latch data for planes 0, 1, 2 and 3 to be combined in the ALU, as defined throughout the documentation. When emulation mode is enabled, they define the alternate values for the htotal, hblank end, hsync (retrace) start and hsync (retrace) end registers (see application note on HT216-32 emulation mode for further details).

Note: Register 0xF5 is also used as an alternate value for vertical display end in emulation modes.

3C4 R/W

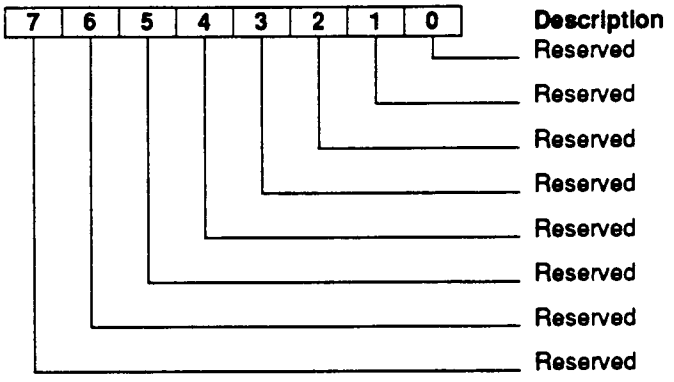
Index F3



Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	-		
2	-		
1	-		
0	-		

3C4 R/W

Index F4

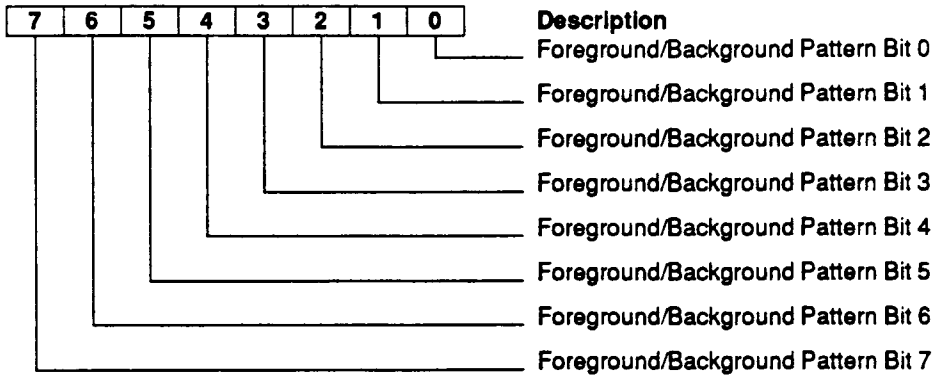


Bit	Bit Name	POR	Description
7	-		
6	-		
5	-		
4	-		
3	-		
2	-		
1	-		
0	-		

These registers, indices 0xF3 and 0xF4, are reserved and must be set to 0.

FBPAT Foreground/Background Pattern Register 3C4 R/W

Index F5

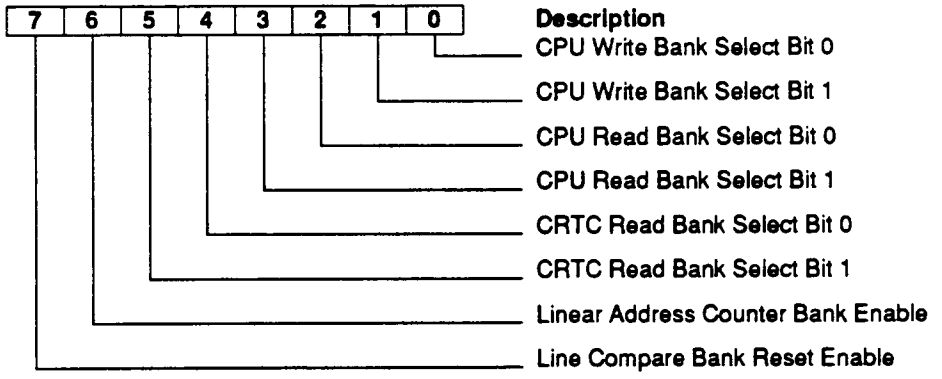


Bit	Bit Name	POR	Description
7	FBPAT.7	0	
6	FBPAT.6	0	
5	FBPAT.5	0	
4	FBPAT.4	0	
3	FBPAT.3	0	
2	FBPAT.2	0	
1	FBPAT.1	0	
0	FBPAT.0	0	

This register, index 0xF5, performs two functions. When emulation mode is not enabled (as defined by 0xC8.5), it defines the 8 bit foreground/background pattern value used in the HT216-32's extended ALU (see 0xFE[5:4]/[3:2] for more information). If emulation mode is enabled, it defines the alternate vertical display enable end value.

RAMBKSL 1 MByte RAM Bank Select Register 3C4 R/W

Index F6

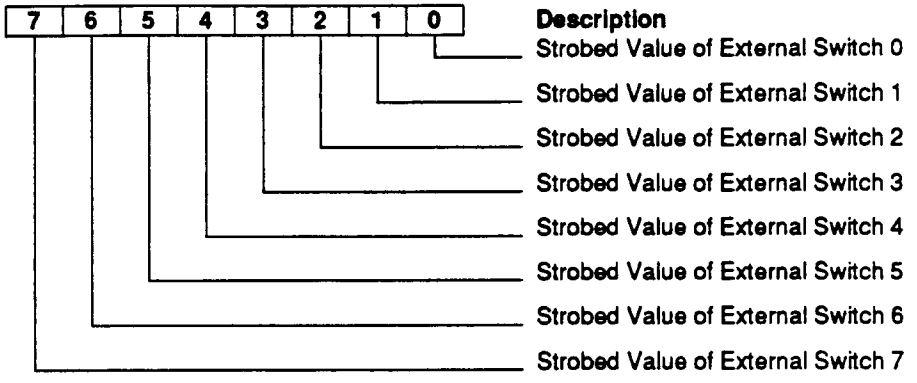


Bits	Bit Name	POR	Description
7	LCBR	0	Line Compare Bank Reset Enable 0 = When CRTC vertical line count matches line compare value (as determined by CR18), then bits 16 and 17 of the extended linear address count value are reset to 0 along with bits [15:0] (i.e., as normal). 1 = When CRTC vertical line count matches line compare value (as determined by CR18), then bits 16 and 17 of the extended linear address count value are reset to the value of bits 4 and 5 of this register, respectively.
6	LABE	0	Linear Address Counter Bank Enable 0 = The CRTC linear address counter is restricted to 16 bits. For applications requiring greater than the corresponding amount of memory, bits 4 and 5 of this register define the 256 KByte bank of memory from which CRTC information is fetched. 1 = The CRTC linear address counter is extended to 18 bits.
[5:4]	CTBS.1 CTBS.0	0 0	CRTC Read Bank Select When bit 6 of this register is set to 0, these 2 bits define from which of the four possible 256 KByte banks of Display Memory CRTC information is to be fetched.
[3:2]	RBSL.1 RBSL.0	0 0	CPU Read Bank Select These two bits determine which of the four possible 256 KByte banks of Display Memory will be accessed on CPU memory reads.

[1:0]	WBSL.1 WBSL.0	CPU Write Bank Select These two bits determine which of the four possible 256 KByte banks of Display Memory will be accessed on CPU memory writes.

SWRB Switch Readback Register 3C4(R)

Index F7

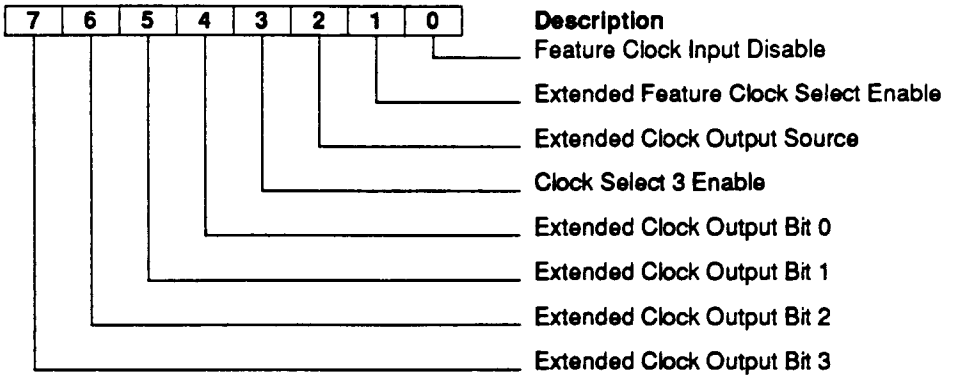


Bit	Bit Name	POR	Description
7	SWV.7	-	
6	SWV.6	-	
5	SWV.5	-	
4	SWV.4	-	
3	SWV.3	-	
2	SWV.2	-	
1	SWV.1	-	
0	SWV.0	-	

This register, index 0xF7 is used to receive the contents of the external switches from 0xEA. When a CPU I/O write to 0x3C5 occurs while index 0xEA is set at 0x3C4, then the external data transceiver on the upper data bus is forced off, and the external switches connected to the DAC/EPROM are dynamically loaded into 0xF7. This register is read only.

XCLKCTL Extended Clock Control Register 3C4 R/W

Index F8

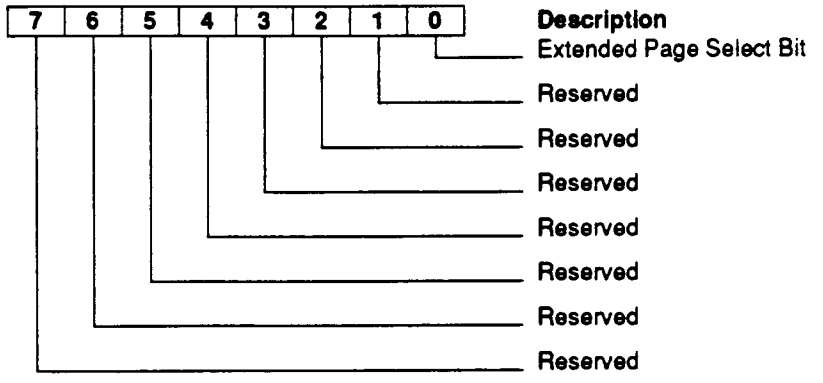


Bit	Bit Name	POR	Description
[7:4]	XCKO.3 XCKO.2 XCKO.1 XCKO.0	0 0 0 0	Extended Clock Output When bit 2 of this register = 1, these 4 bits are output as clock selects to an external frequency synthesizer, as determined by bits 1 and 0 of this register.
3	CKSL3E	0	Clock Select 3 Enable 0 = All four clock select pins are outputs. 1 = The external pin normally used to output clock select bit 3 is used as an external frequency source and is selected whenever clock select bit 3 is a one.
2	XCOS		Extended Clock Output Source 0 = Clock selects[3:0] to the external frequency synthesizer are determined by 0xA4[5:4] and 0x3C2[3:2], respectively. 1 = Clock selects [3:0] to the external frequency synthesizer are determined by bits [7:4] of this register.
1	EFCKSLE	0	Extended Feature Clock Select Enable 0 = If bit 0 of this register is 0 then if bits [1:0] of the clock select value are equal to 0x2, then the external feature clock input is selected as the dot-clock source. 1 = If bit 0 of this register is 0 then if bits [3:0] of the clock select value are equal to 0x2, then the external feature clock input is selected as the dot-clock source.

0	FCKIE	0	Feature Clock Input Disable 0 = The external feature clock input will be used as the dot-clock source as determined by the clock select value and bit 1 of this register. 1 = The clock select value selects one of 16 possible frequencies from the external frequency synthesizer (i.e., selection of the external feature clock input is overridden).

XPSEL — Extended Page Select Register — 3C4 R/W

Index F9



Bit	Bit Name	POR	Description
[7:1]	-		Reserved; must = 0.
0	XPSEL	0	Extended Page Select In chain4 modes (as determined by SR04.4) this bit is used to determine the DM address as follows:

DM Address bit	Source
[17:16]	0xF6[3:2] for reads; 0xF6[1:0] for writes
15	Page Select bit (0x3C2.5)
14	Extended Page Select bit
[13:0]	CPU Address[15:2]
Plane Select[1:0]	CPU Address[1:0] in 256 color modes

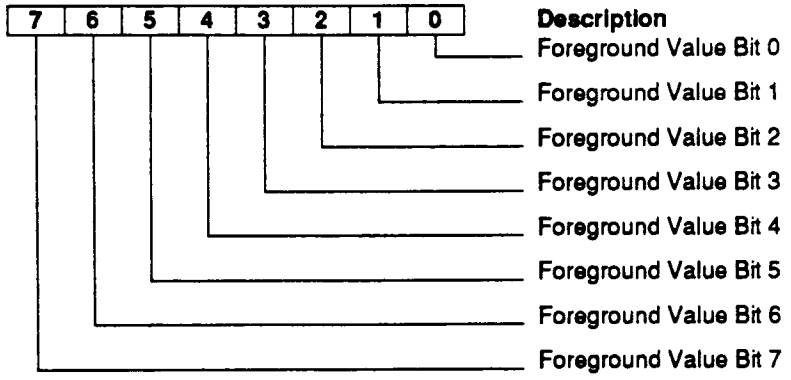
Note: *Linear Address Mode: Address bits 31:0 come from the CPU for byte/pixel modes. Address bits 31:2 come from the CPU for planar (16-color) modes. See Chain4 bit in Sequencer Register Index 04.*

Programming Note: Apparent Addressing from Software Perspective

Byte-Wide Display Memory Address Bits	Planar Modes	Packed Pixel Modes
[19:18]	RMBKSL [1:0] Writes [3:2]Reads or LSBA [7:6] or USBA [7:6]	Same as Planar Modes
17	CPU 15	MISC Bit 5 or LSBA Bit 5 or USBA Bit 5
16	CPU 14	XPSEL Bit 0 or LSBA Bit 4 or USBA Bit 4
15:2	CPU [13:0]	CPU [15:2]
[1:0]	Plane Select [1:0]	CPU [1:0]

XFCOLR Extended Foreground Color Register 3C4 R/W

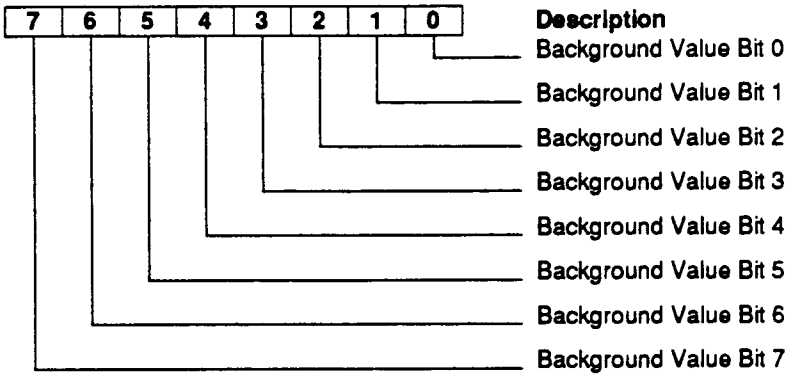
Index FA



Bit	Bit Name	POR	Description
7	FCOLR.7	0	
6	FCOLR.6	0	
5	FCOLR.5	0	
4	FCOLR.4	0	
3	FCOLR.3	0	
2	FCOLR.2	0	
1	FCOLR.1	0	
0	FCOLR.0	0	

XBCOLR Extended Background Color Register 3C4 R/W

Index FB

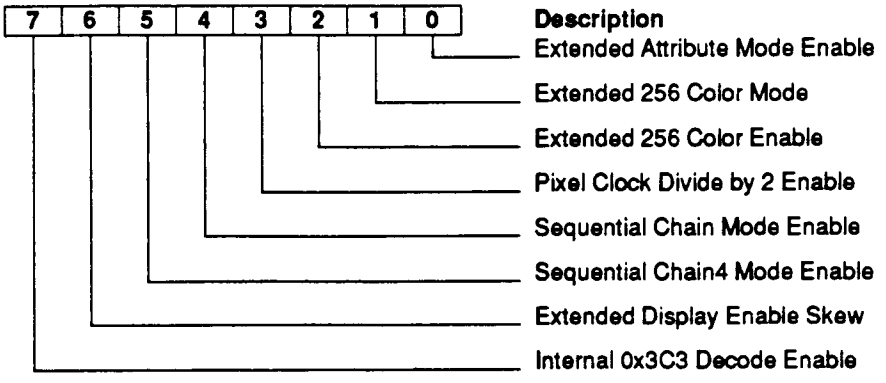


Bit	Bit Name	POR	Description
7	BCOLR.7	0	
6	BCOLR.6	0	
5	BCOLR.5	0	
4	BCOLR.4	0	
3	BCOLR.3	0	
2	BCOLR.2	0	
1	BCOLR.1	0	
0	BCOLR.0	0	

These two registers, indices 0xFA and 0xFB, are used as the foreground and background sources in the extended function mode of HT216-32's ALU. This is described in more detail under 0xFE[5:4] and 0xFE[3:2]. Note that in planar modes, only the lower 4 bits of these registers are used, whereas in fat pixel (i.e., chain4) modes, all 8 bits are used.

COMCTL Compatibility Control Register 3C4 R/W

Index FC



The Compatibility Control register enables selection and aspects of operation of enhanced 256-color graphics modes, enhanced attributes in text mode, refresh and extended display enable skews, and masked DRAM writes.

Bit	Bit Name	POR	Description
7	E3C3	0	Internal 3C3 Decode Enable When this bit is 1, the DISABLE bit is 1 and bit 0 of 3C3 is 1, the HT216-32 is mapped into the host's I/O and memory address space. When this bit is 1, the DISABLE bit is 1 and bit 0 of 3C3 is 0, 3C3 is the only I/O address at which the HT216-32 answers, and all memory addressing to the CPU is disabled. In both these cases the HT216-32 answers at I/O address 3C3.
Note:	*If this bit is 0 and the DISABLE bit is 1, then bit 0 of 3C3 has no effect and 3C3 is not decoded as a register. When the DISABLE bit is 0, all I/O and memory addressing is disabled.*		
6	XDESK	0	Extended Display Enable Skew 0 = Display enable skew is selected by bits 5 and 6 of CR03. 1 = Display enable skew is 1 greater than the skew selected with bits 5 and 6 of CR03.

5	SQCH4	0	Sequential Chain 4 0 = Chain 4 mode operates under bit 3 of SR4 and bit 1 of GR6. 1 = The nature of the Chain 4 mode (selected when bit 3 of SR4 is 1) changes. On CPU accesses, instead of routing CPU address bits A[15:2] to linear address bits LA[15:2] and substituting bits on LA[1:0], A[15:2] are routed to LA[13:0] and the same bits are substituted on LA[15:14] instead of LA[1:0]. The net effect of this is to cause chain 4 bit-maps to be stored at consecutive display memory addresses, where they can be scanned in byte mode.

Note: For a full description of substitution of bits in chain 4 and sequential chain modes, see GR6 bit 1.

4	SQCH	0	Sequential Chain 0 = Chain mode operates as described under bit 1 of GR6. 1 = The nature of the chain mode (selected when bit 3 of SR4 is 0 and bit 1 of GR6 is 1) changes. On CPU accesses, instead of routing CPU address bits A[15:1] to linear address bits LA[15:1] and substituting bits on LA0, A[15:1] are routed to LA[14:0] and the same bits are substituted on LA15 instead of LA0. The net effect of this causes chain bit-maps to be stored at consecutive display memory addresses, where they can be scanned in byte mode.

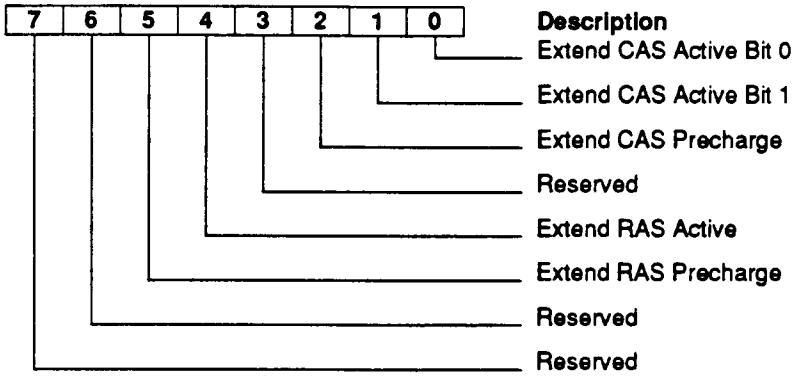
Note: For a full description of sequential chain see discussion under bit 1 of GR6.

3	PCD2	0	Pixel Clock Divide by 2 Enable 0 = Normal operation. 1 = Divides the dot clock output frequency by 2. This is useful when using a HiCOLOR™ RAMDAC which collects bytes of video data on the rising and falling edges of DTCLKOUT.
2	ECOLRE	0	Extended 256-Color Enable 0 = No enhanced 256-color mode. 1 = Enhanced 256-color mode selected by bit 1 of this register is in effect for CPU addressing whenever the Chain 4 bit is 1, and enhanced CRTC 256-color mode (whereby memory address counter bit 15 is placed on linear address bit 1 and memory address counter bit 14 is placed on linear address bit 0) is in effect for CRTC addressing whenever the Doubleword Mode bit is 1.

1	ECMD	0	Extended 256-Color Mode This bit selects the type of extended 256-color CPU addressing mode that is used when the extended 256-Color Enable bit (bit 2) is 1 and when the Chain 4 bit (Bit 3 for SR4) is 1. 0 = 64K extended 256-color mode. If the Chain 4 bit is 1, then during CPU reads and writes, CPU address bits [15:2] are placed on linear address bits [15:2], the non-inverted Page Select bit (bit 5 of the Miscellaneous Output register 3C2) is placed on linear address bit 1 and the Extended Page Select bit (bit 3) of this register is placed on linear address bit 0. When Chain 4, bit is 1, CPU address bits 0 and 1 select the plane. When the Chain 4 bit is 0, the selected extended 256-color mode has no effect on CPU addressing. The net effect of the extended 256-color modes is to substitute new CPU and CRTC address multiplexings. This bit has no effect if bit 2 = 0. 1 = 128K extended 256-color mode. In this mode, if the Chain 4 bit is 1, for CPU addressing, CPU address bits [15:2] are placed on linear address bits [15:2], the non-inverted Page Select bit is placed on linear address bit 1 and CPU address bit 16 is placed on linear address bit 0.
0	EATE	0	Extended Attribute Enable 0 = Extended text attributes disabled. 1 = Extended Attributes Enabled. The extended attribute byte for each character is fetched from plane 3 at the same time and from the same address as the character code and attribute byte. This byte is ORed with the font data on the underline scan line, in the same way the underline is inserted. This provides a means of underlining text with any and all normal attributes.

DMCTRL — Display Memory Controller Timing — 3C4 R/W

Index FD



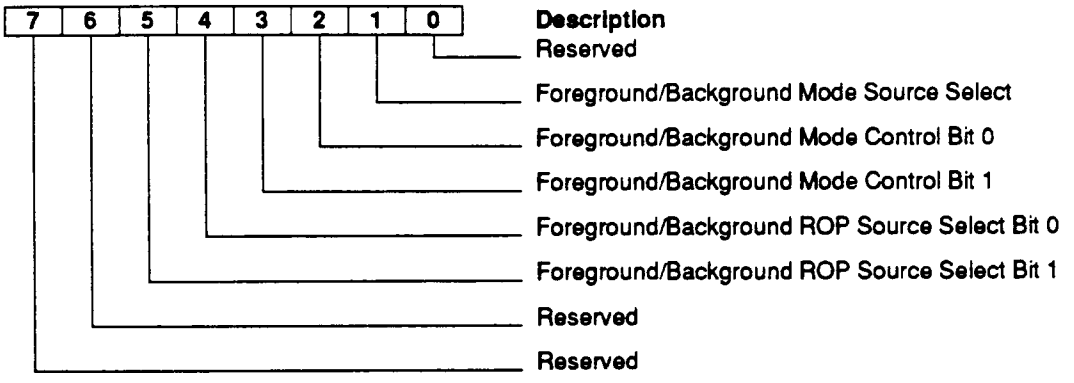
This register allows the programming of Display Memory interface parameters in terms of number of memory clocks (MCLKs).

Bit	Bit Name	POR	Description
5	XRASPRE	1	Extend RAS Precharge 1 = 4 MCLKs 0 = 3 MCLKs
4	XRASACT	1	Extend RAS Active 1 = 5 MCLKs 0 = 4 MCLKs
2	XCASPRE	1	Extend CAS Precharge 1 = 2 MCLKs 0 = 1 MCLKs
[1:0]	XCASACT.1 XCASACT.0	0 1	Extend CAS Active

Bit 1	Bit 0	^{t}CAS in number of MCLKs
0	0	1
0	1	2
1	0	3
1	1	Not Allowed

FBCTRL Foreground/Background Control Register 3C4 R/W

Index FE



Bit	Bit Name	POR	Description
[5:4]	FBRSL.1 FBRSL.0	0 0	Foreground/Background ROP Source Select These bits select the source of the Raster Operations. 00=CPU Byte 01=Bit Mask Register (3CF:08) 1x=Foreground Background Pattern Register (3C4:F5)
[3:2]	FBMC.1 FBMC.0		Foreground/Background Mode These bits select the source of the byte input to each of the four plane ALUs.

Bit 3	Bit 2	Mode of CPU-Side ALU Input Operations
0	0	Set/Reset Output Mode (VGA Mode)
0	1	Solid Foreground/Background Mode
1	0	Dithered Foreground Mode
1	1	Read-modify-write mode (set if CD.5=1)

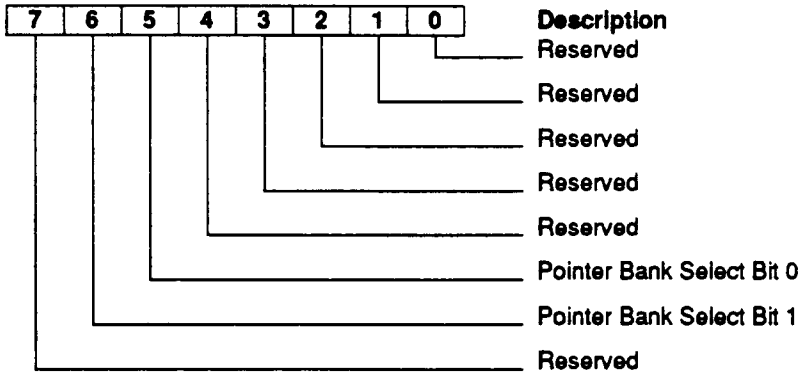
Set/reset output mode means that the output is the CPU-side ALU input.

Solid Foreground/Background Mode means that a byte is input into the foreground/background select circuitry, with each 1-bit of the byte selecting the foreground color stored in extension register FA and each 0-bit selecting the background

			color stored in extension register FB. The resultant byte for each plane becomes the CPU-side input to each plane's ALU. This provides the capability to generate a solid foreground against a solid background with a single write, basically expanding a binary (monochrome) pattern to a color pattern. The source of the selection byte in this mode is the Foreground/Background Pattern register (ERF5) if bit 1 of this register is 0 and is the rotated CPU byte if bit 1 of this register is 1. Dithered Foreground Mode means that the foreground latch byte for each plane (from ER EC-EF) is input directly to that plane's CPU-side ALU input. This provides the capability to support fully dithered foreground patterns, with dithered background patterns optionally stored in the normal latches and the two combined via the bit mask. In the Read-modify-write mode (CD.5=1) the destination data is fed into the B side of the ALU.
1	FBRC	0	Foreground/Background Source When the HT216-32 is in solid foreground/background mode (bits 3 and 2 are 0 and 1 respectively) then the 8-bit pattern that selects the foreground color in Extension Register FA and the background color in extension register FB can come either from the Foreground/Background Pattern register ER F5 or from the rotated CPU byte. 0 = Foreground/Background Pattern register is source. 1 = Rotated CPU byte is source

16INTR — 16 Bit Interface Control Register — 3C4 R/W

Index FF



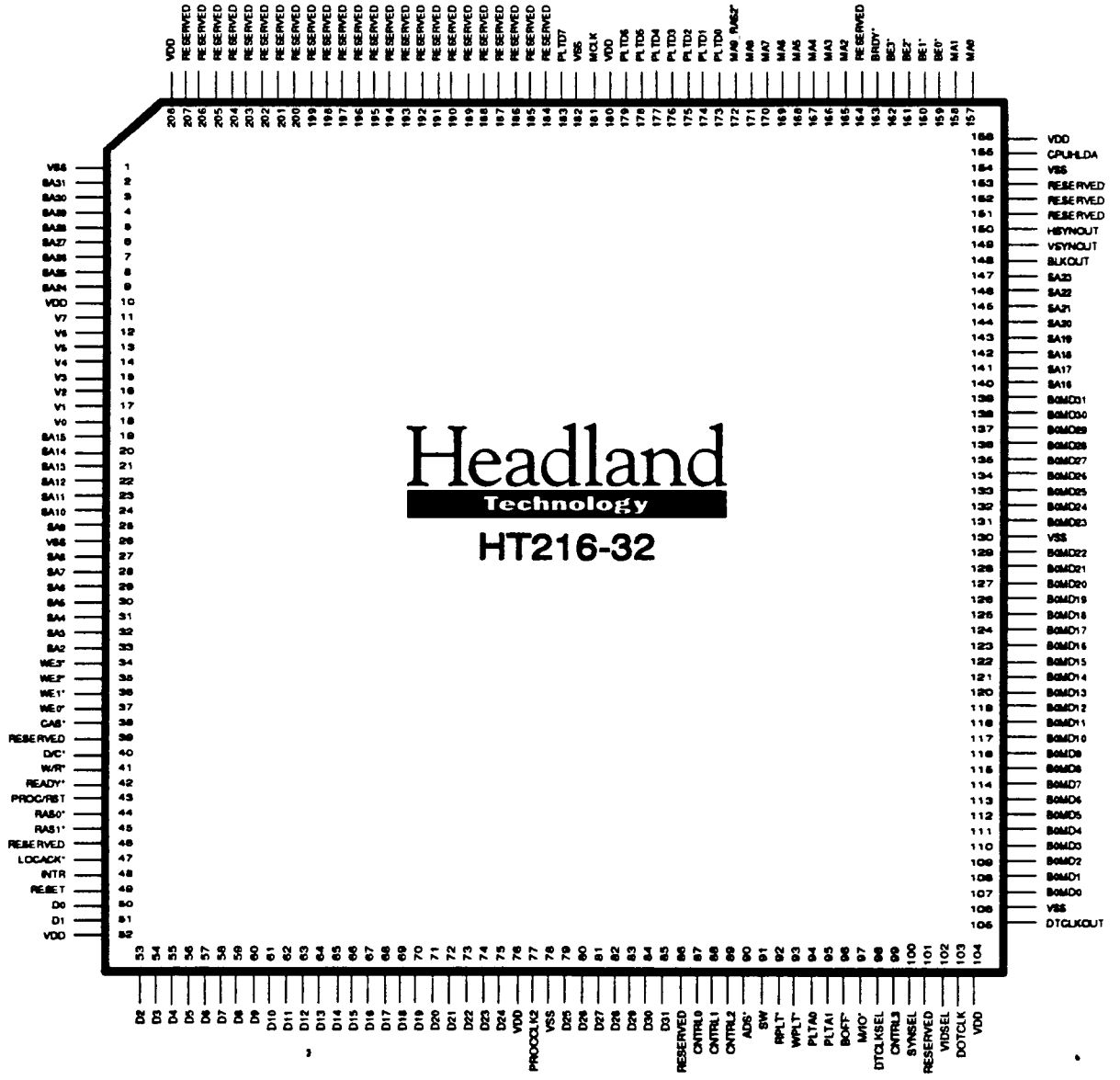
This register is used to control 16-bit options in the interface of the HT216-32 and associated components to the system bus. The HT216-32 presents a true 16-bit interface to the system, saving a significant number of wait states.

Bit	Bit Name	POR	Description
7		-	Reserved Read as 1.
[6:5]	PTBS.1	0	Pointer Bank Select
	PTBS.0	0	These bits provide linear address bits 17 and 16 respectively, when addressing the hardware cursor pattern during screen refresh. These bits select either 1M or one of up to 4 banks of 256K DRAMs.
[3:0]		-	Reserved Read as 1.

Pin Names

The HT216-32 is a local bus only part housed in a 208 pin PQFP.

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
90	ADS*	68	D17	32	SA3
107	B0MD00	69	D18	31	SA4
108	B0MD01	70	D19	30	SA5
109	B0MD02	71	D20	29	SA6
110	B0MD03	72	D21	28	SA7
111	B0MD04	73	D22	27	SA8
112	B0MD05	74	D23	25	SA9
113	B0MD06	75	D24	24	SA10
114	B0MD07	79	D25	23	SA11
115	B0MD08	80	D26	22	SA12
116	B0MD09	81	D27	21	SA13
117	B0MD10	82	D28	20	SA14
118	B0MD11	83	D29	19	SA15
119	B0MD12	84	D30	140	SA16
120	B0MD13	85	D31	141	SA17
121	B0MD14	40	D/C*	142	SA18
122	B0MD15	103	DOTCLK	143	SA19
123	B0MD16	105	DTCLKOUT	144	SA20
124	B0MD17	98	DTCLKSEL	145	SA21
125	B0MD18	150	HSYNOUT	146	SA22
126	B0MD19	48	INTR	147	SA23
127	B0MD20	47	LOCACK*	9	SA24
128	B0MD21	97	M/IO*	8	SA25
129	B0MD22	157	MA0	7	SA26
131	B0MD23	158	MA1	6	SA27
132	B0MD24	165	MA2	5	SA28
133	B0MD25	166	MA3	4	SA29
134	B0MD26	167	MA4	3	SA30
135	B0MD27	168	MA5	2	SA31
136	B0MD28	169	MA6	91	SW
137	B0MD29	170	MA7	100	SYNSEL
138	B0MD30	171	MA8	18	V0
139	B0MD31	172	MA9_RAS2*	17	V1
159	BE0*	181	MCLK	16	V2
160	BE1*	94	PLTA0	15	V3
161	BE2*	95	PLTA1	14	V4
162	BE3*	173	PLTD0	13	V5
148	BLKOUT*	174	PLTD1	12	V6
96	BOFF*	175	PLTD2	11	V7
163	BRDY*	176	PLTD3	10,52,76,104,	VCC
38	CAS*	177	PLTD4	156,180,208	VCC
87	CNTRL0	178	PLTD5	1,26,78,106,130	VSS
88	CNTRL1	179	PLTD6	154,182	VSS
89	CNTRL2	183	PLTD7	149	VSYNOUT
99	CNTRL3	43	PROC/RST	41	W/R*
155	CPUHLDA	77	PROCCLK2	37	WE0*
50	D0	44	RAS0*	36	WE1*
51	D1	45	RAS1*	35	WE2*
53	D2	42,	READY*	34	WE3*
54	D3	39,46,86,96,101,	RESERVED	93	WPLT*
55	D4	151,152,153,155,	RESERVED		
56	D5	164,184,185,186,	RESERVED		
57	D6	187,188,189,	RESERVED		
58	D7	190,191,192,	RESERVED		
59	D8	193,194,194,	RESERVED		
60	D9	196,197,198,	RESERVED		
61	D10	199,200,201,	RESERVED		
62	D11	202,203,204,	RESERVED		
64	D13	205,206,207	RESERVED		
65	D14	49	RESET		
66	D15	92	RPLT*		
67	D16	33	SA2		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HT216-32

Pin Name	Pin Number	Pin Type	Description
ADS*	90	I/O	This input from the CPU indicates that a new address and cycle definition has been applied on the local bus.
B0MD[0:31]	107-129, 131-139	I/O	Memory Data Bus: B0MD[0:7] is for Blue and plane 0 data (for configuration pullups refer to POR register 104). [8:15] is for Green and plane 1 data (for pullups refer to POR register 105). [16:23] is for Intensity and plane 3 data (for pullups refer to POR register 107). [24:31] is for Red and plane 2 data (for pullups refer to POR register 106).
BE[0:3]*	159-162	I/O	Unlatched byte enables.
BLKOUT*	148	O	This output indicates that the video data is blanked during horizontal and vertical retrace. It should be connected to the blanking input of the color palette.
BRDY*	163	I/O	For 486 based implementations, this pin is connected to the corresponding BRDY* pin. For 386DX implementations this pin is a no connect. Burst mode is not supported by HT216-32, but for proper operation, HT216-32 needs to sense activity on this pin.
BOFF*	96	I/O	Connected to the BOFF* input of the 486. This is used to accomplish palette updates to the local bus as well as the system I/O bus.
CAS*	38	O	This output is the only Column Address Strobe for display memory. It drives all display memory planes.
CNTRL[0:3]	87-89, 99	O, I/O	These outputs control an external clock synthesizer to select one of several alternative Dot Clock sources. See DOTCLK.
CPUHLDA	155	I/O	This is the Hold Acknowledge input from the CPU. Refer to Register 105 bit 3.
D[0:31]	50, 51, 53-75, 79-85	I/O	This is the 32 bit wide data interface to and from the host system. These pins are connected directly to the CPU data bus.
D/C*	40	I/O	Data/Code*. This input, in conjunction with W/R* and M/IO* defines cycle type.

Pin Name	Pin Number	Pin Type	Description
DOTCLK	103	I	Dot Clock. This input is the primary source for the Dot Clock. There are also several alternative clocks that may be selected via the following registers; the Miscellaneous Output Register (3CC/3C2), bits [3:2], the Extended Clock Select Register (3C4:A4), bits [5:2], and the Extended Clock Control Register (3C4:F8), bits [7:3].
DTCLKOUT	105	O	Dot Clock Out. This output is the shift clock for video data. It should be connected to the clock input of the external color palette, and the feature clock input from the feature connector.
DTCLKSEL	98	I	Dot Clock Select. This input may be used to select the FCLK input as the Dot Clock source. Thereby allowing the Feature Connector to drive the monitor.
HSYNOUT	150	O	Horizontal Sync Out. This output drives the horizontal sync on the monitor. The polarity of this signal may be inverted via the Miscellaneous Output Register (3C2), bit-6.
INTR	48	I/O	CPU Interrupt. This pin is active high. The interrupt will occur at the start of the vertical retrace interval if enabled by clearing Vertical Retrace End Register (CR11) bit 5 and setting bit 4. This signal will stay active until reset by clearing CR11 bit 4. (Bit 4 must then be set to enable the next vertical retrace interrupt.) This pin can be connected directly to IRQ9 on the system bus. Refer to Port 106 bit 1 for interrupt configuration.
LOCACK*	47	O	This output indicates that the current bus cycle is resident within the HT216-32.
M/IO*	97	I/O	Memory/IO. This pin is active low. It defines memory versus I/O cycle type. Together with D/C* and W/R* it defines the CPU cycle type.
MA[0:8]	157, 158, 165-171	O	Display Memory Address bits.
MA9_RAS2*	172	O	Display Memory Address bit. MA9 also works as RAS2* for 64Kx16 DRAMs.
MCLK	181	I	This clock input drives the display memory control circuitry. An appropriate frequency source should be selected in conjunction with DRAM selection to optimize system price/performance requirements.

Pin Name	Pin Number	Pin Type	Description
PLTA[0:1]	94, 95	O	Palette Address. This output should be connected to address input A0 and A1 on the color palette.
PLTD[0:7]	173-179, 183	I/O	Palette Data [0:7]. This is the I/O data interface to the external color palette.
PROC_RST	43	I	Processor Reset. This pin must be connected to the same source as the CPU reset in a 386DX system. In a 486 system connect this pin to 486CLK1 (1X clock).
PROCCLK2	77	I	This clock input drives the bus interface control circuitry. It should be connected to the CLK2 clock.
RAS[0:1]*	44, 45	O	These outputs are the primary Row Address Strobes used to control the display memory. Ras0 drives bank 0, planes 0 and 2, while RAS1 drives bank 0 planes 1 and 3.
READY*	42	I/O	As an output, READY* is driven low to the CPU to terminate the bus cycle. READY* is used in a WIRED-OR configuration to stay in sync with the CPU.
RESERVED	86	I	These are reserved input pins.
RESERVED	39, 101, 151-153	O	These are reserved output pins.
RESERVED	46,164, 184-207	I/O	These are reserved I/O pins.
RESET	49	I	This input performs a comprehensive hardware reset on the HT216-32.
RPLT*	92	O	Read Palette. This output is a read strobe for the external color palette.
SA[2:31]	33-27, 25-19, 140-147, 9-2	I/O	These are CPU address inputs A[2:31].
SW	91	I	Monitor Switch. This input may be used to determine monitor type and is driven by the board's monitor comparator circuit. The state of this pin may be read at Feature Read Register (3C2) bit 4.
SYNSEL	100	I	Sync Select. This input may be used to tri-state the HSYNOUT and VSYNOUT outputs, thereby allowing the monitor to be driven instead by the Feature Connector.

Pin Name	Pin Number	Pin Type	Description
V[0:7]	18-11	O	Video Data. These outputs should be connected to the video data input bus of the external color palette.
VIDSEL	102	I	Video Select. This input may be used to tri-state the V[7:0] output bus, thereby allowing the color palette to be driven instead by the Feature Connector.
VSYNOUT	149	O	Vertical Sync Out. This output drives the vertical sync on the monitor. The polarity of this signal may be inverted via the Miscellaneous Output Register (3C2) bit 7.
W/R*	41	I/O	Write/Read*. This input in conjunction with D/C* and M/IO* defines cycle type.
WE[3:0]*	37-34	O	Write Enables. These outputs drive one plane each of display memory to enable data writes to individual planes.
WPLT*	93	O	Write Palette. This output is a write strobe for the external color palette.

DC Characteristics

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC Input Current	IIN	10	mA
Storage Temperature Range (Plastic)	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Ambient Temperature Range (Commercial)	TA	0 to +70	C

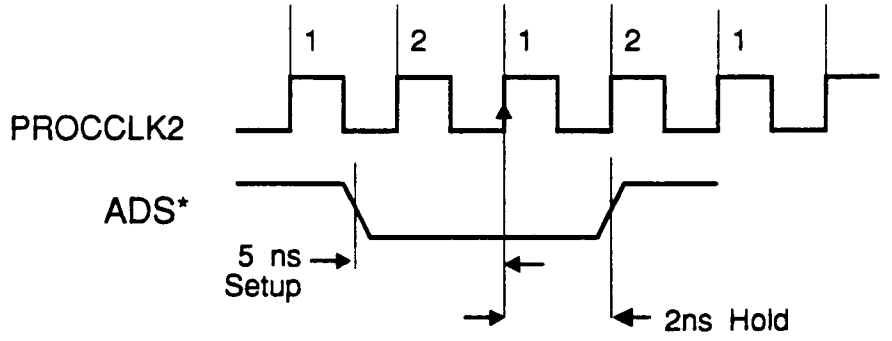
DC Characteristics: VDD = 5V +/- 5%, TA = 0C to 70C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL				0.8	V
Voltage Input High	VIH		2			V
Input Current	IIH		-10	1	10	µA
Voltage Output High	VOH					
LOCACK*, CAS*, INTR, MA[9:0], BRDY*, RAS[1:0]*, READY*, WE[3:0]*,V[7:0], DTCLKOUT, HSYNOUT, VSYNOUT, BLKOUT, WPLT*		IOH=24mA	2.4	4.5		V
ADS*, BE[3:0]*, D/C*, PROC_RST, SA[31:2], W/R*, CNTRL[3:0], SW, RPLT*		IOH=6mA	2.4	4.5		V
PLTA[1:0], PLTD[7:0], B0MD[31:0], D[31:0]		IOH=10mA	2.4	4.5		V
Voltage Output Low	VOL					
LOCACK*, CAS*, INTR, MA[9:0], BRDY*, RAS[1:0]*, READY*, WE[3:0]*,V[7:0], DTCLKOUT, HSYNOUT, VSYNOUT, BLKOUT, WPLT*		IOL=12mA		0.4	0.8	V
ADS*, BE[3:0]*, D/C*, PROC_RST, SA[31:2], W/R*, CNTRL[3:0], SW, RPLT*		IOL=3mA		0.4	0.8	V
PLTA[1:0], PLTD[7:0], B0MD[31:0], D[31:0]		IOL=4mA		0.4	0.8	V
3-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	1	10	µA
Output Short Circuit Current	IOS	VDD=Max, V0=VDD				mA
See Note		VDD=Max, V0=0V				mA
Supply Current	IDD	CLK=40MHz, CL=50pf			300	mA

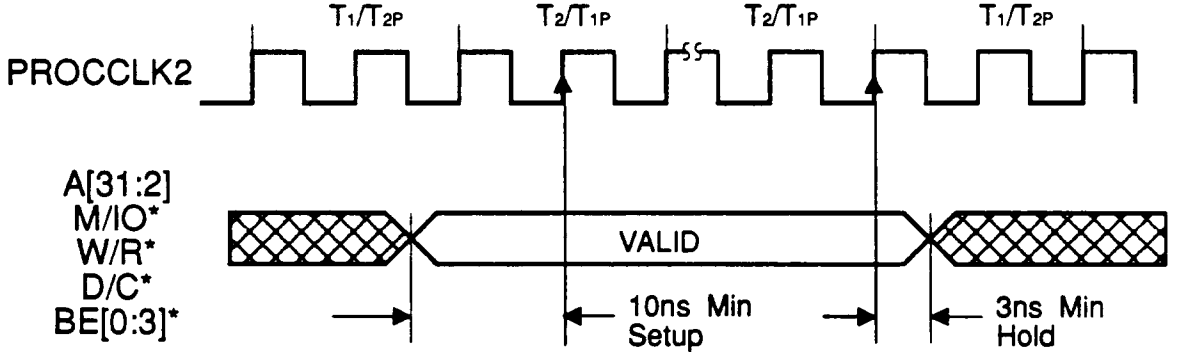
Note: Not more than one output may be shorted at any time for a maximum duration of one second. Short Circuit Current values are for 3mA IOL/6mA IOH outpputs, they will scale for other outputs.

Local Bus Interface Timing

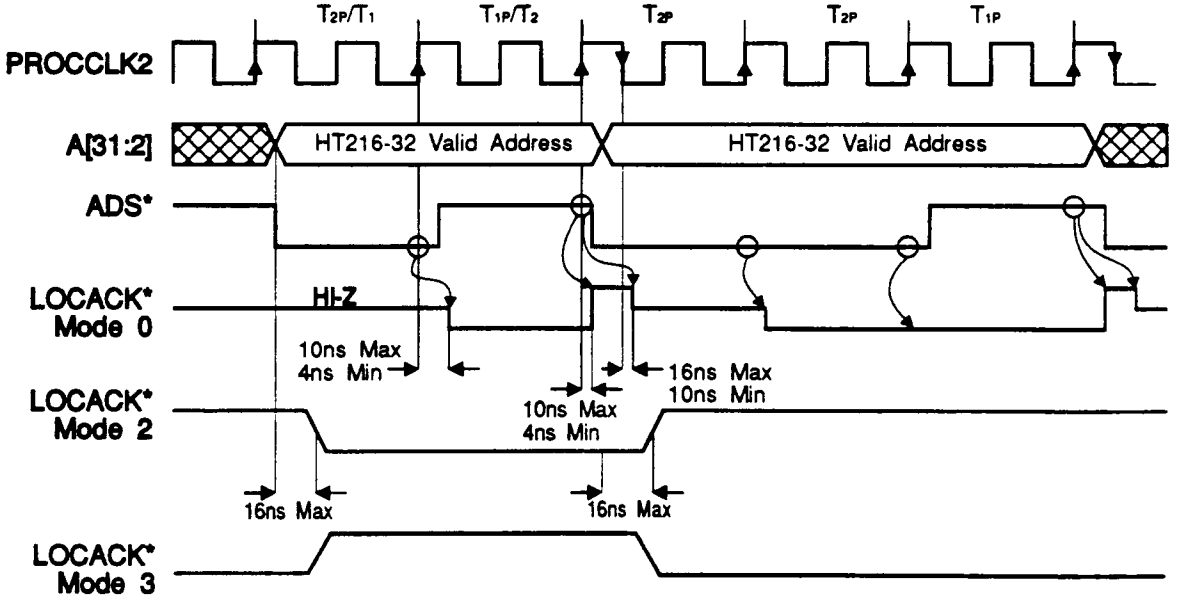
Parameter	Min	Typ	Max	Units
ADS* setup	5			ns
ADS* hold	2			ns
A[31:2], M/IO*, D/C*, W/R*, BHE*, BLE*, BE[0:3]* Setup	9			ns
A[31:2], M/IO*, D/C*, W/R*, BE[0:3]* hold	3			ns
LOCACK* valid delay from valid address in Mode 2,3			16	ns
LOCACK* invalid delay from address invalid			16	ns
LOCACK* valid delay from PROCCLK2 in T_{1P}/T_2 in Mode 0	4		10	ns
LOCACK* HI from PROCCLK2 in Mode 0	4		10	ns
LOCACK* float from PROCCLK2	10		16	ns
READY* valid delay from PROCCLK2 in T_{RS}			16	ns
READY* HI delay from PROCCLK2 in T_1/T_P	4		10	ns
READY* float delay from PROCCLK2 in T_1/T_P	7		12	ns
READY*, BRDY* input setup	4			ns
READY*, BRDY* input hold	3			ns
CPU Write data setup	$0.6(t_{CLK2})+.6$			ns
CPU Write data hold	2			ns
Read data valid after PROCCLK2 in T_1/T_P			19	ns
Read data float after PROCCLK2 in T_1/T_P	7		17	ns



ADS* Timing



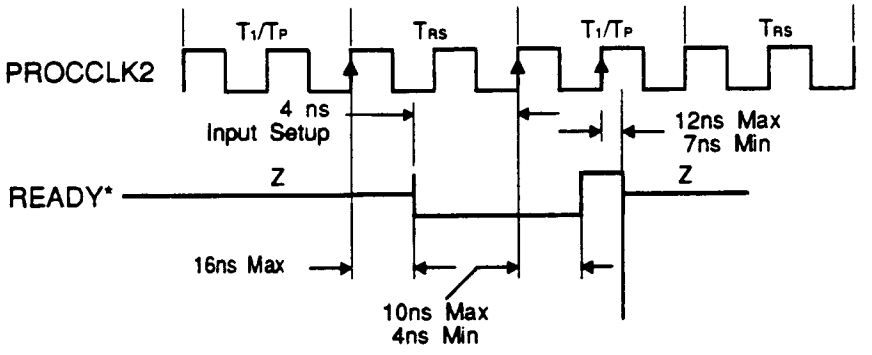
CPU Interface Timing



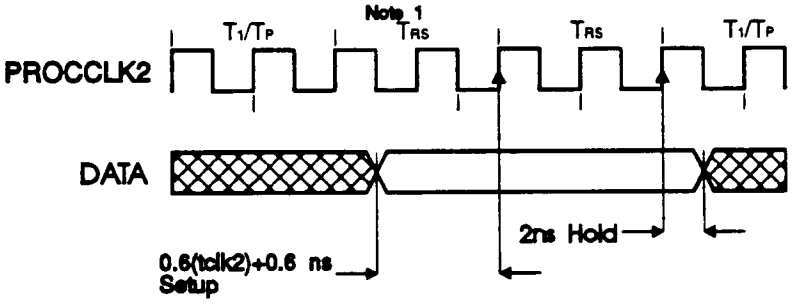
LOCACK* Timing

Note: Mode 3 has the same timing as Mode 2

Note: Timing Diagrams are not drawn to scale.

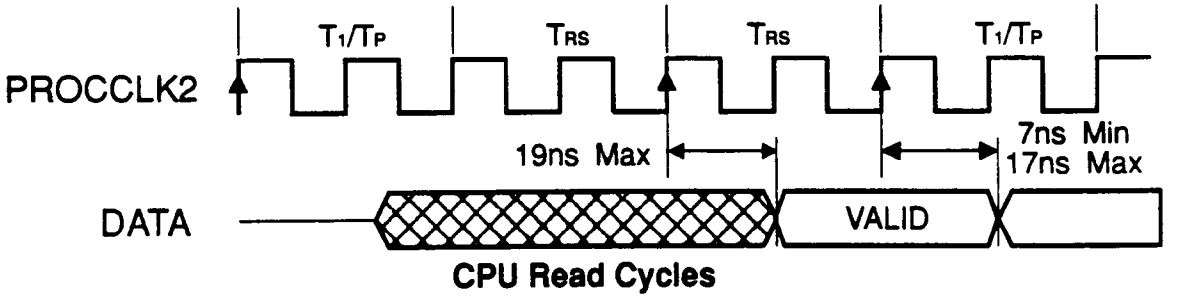


CPU READY Timing



CPU Write Cycles

Note 1: T_{RS} is the READY sensitive state. Refer to the 387™ DX databook for details about the T_1, T_P and T_{RS} states. tclk2 is the period of the PROCCLK2 to the HT216-32.



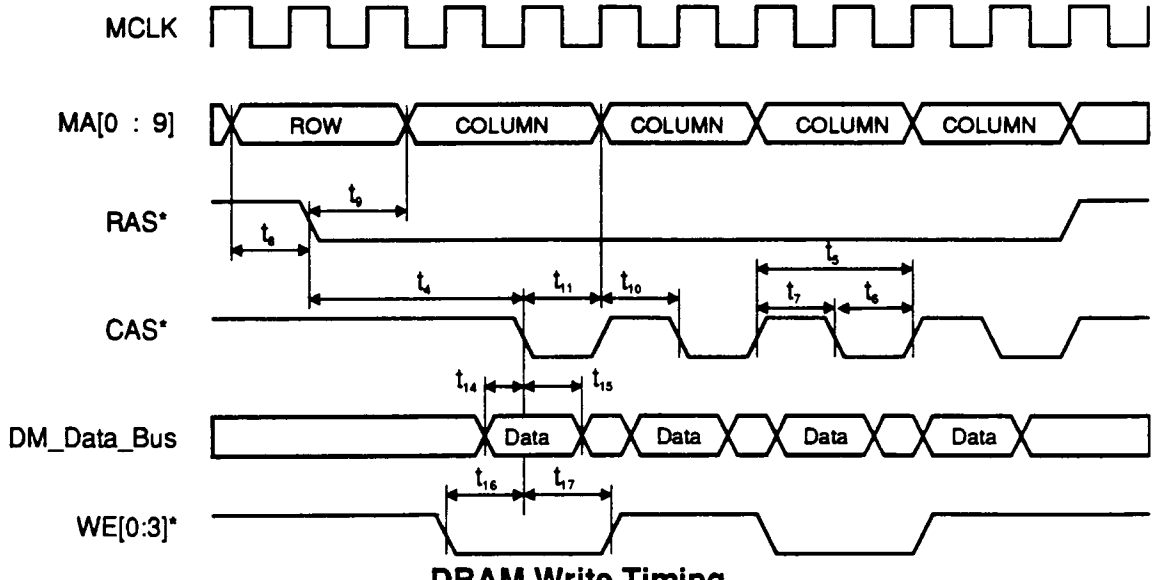
CPU Read Cycles

Note: Timing Diagrams are not drawn to scale.

DRAM Timing

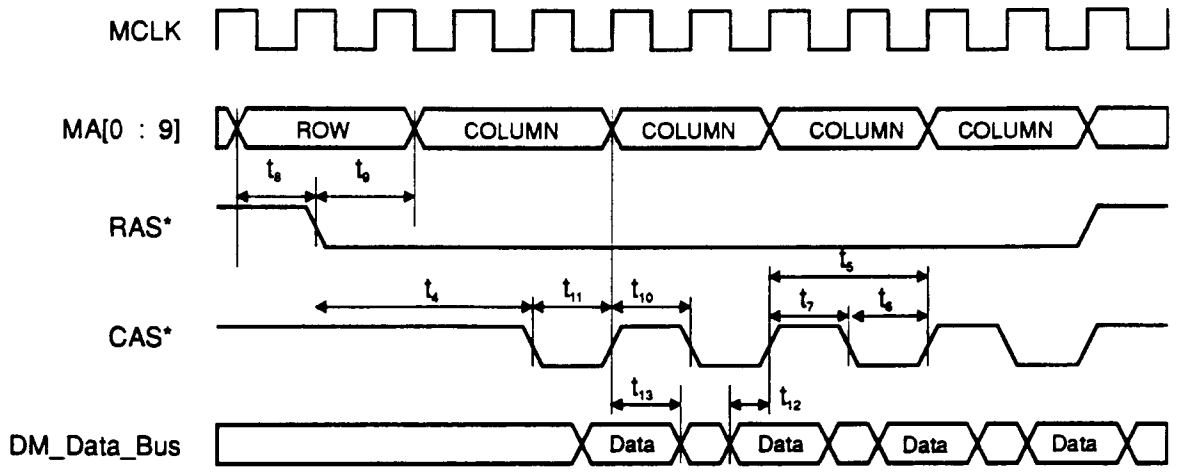
Symbol	Parameter	Min	Typ	Max
t1	RAS* cycle time	(7-9)t		
t2	RAS* pulse width low	(4-5)t+(0 → 1)		
t3	RAS* precharge	(3-4)t-(0 → 1)		
t4	RAS* low to CAS* low	2t + (0.5 → 1.5)		
t5	CAS* cycle time	(2 - 5)t		
t6	CAS* pulse width low	(1-3)t + (0 → 1)		
t7	CAS* precharge	(1-2)t - (0 → 1)		
t8	Row address setup to RAS* low	t - (1 → 3)		
t9	Row address hold from RAS* low	(1-3)t + (0.5 → 1.5)		
t10	Column address setup to CAS* low	1t		
t11	Column address hold from CAS* low	1t		
t12	Read data valid before CAS* high	0		
t13	Read data hold after CAS* high	0		
t14	Write data setup to CAS* low	t - 15		
t15	Write data hold after CAS* low	t - 5		
t16	WE[0:3] low setup to CAS* low	(t - 0.5) →(t + 1.5)		
t17	WE[0:3] low hold after CAS* low	t - 0.5 → +2		
t18	CAS* high for CAS before RAS refresh	2t - (0 - 1)		
t19	RAS* low from CAS* low for CAS before RAS refresh	(t - 0.5) →(t + 1.5)		

NOTE: t = 1/MCLK, 40 MHz ≤ MCLK ≤ 70 MHz
(7-9)t implies 7t, 8t or 9t.
(0→1) implies any value from 0 to 1 ns

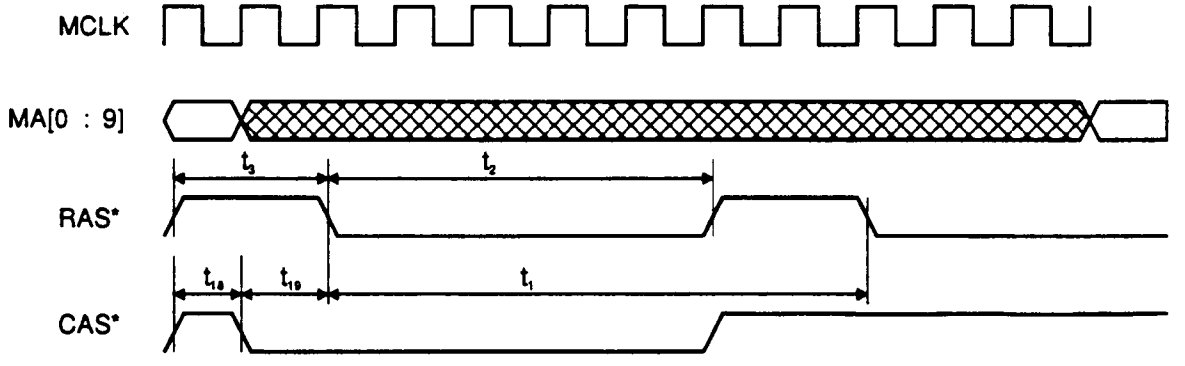


DRAM Write Timing

Note: Timing Diagrams are not drawn to scale.



DRAM Fast Page Mode Read Timing

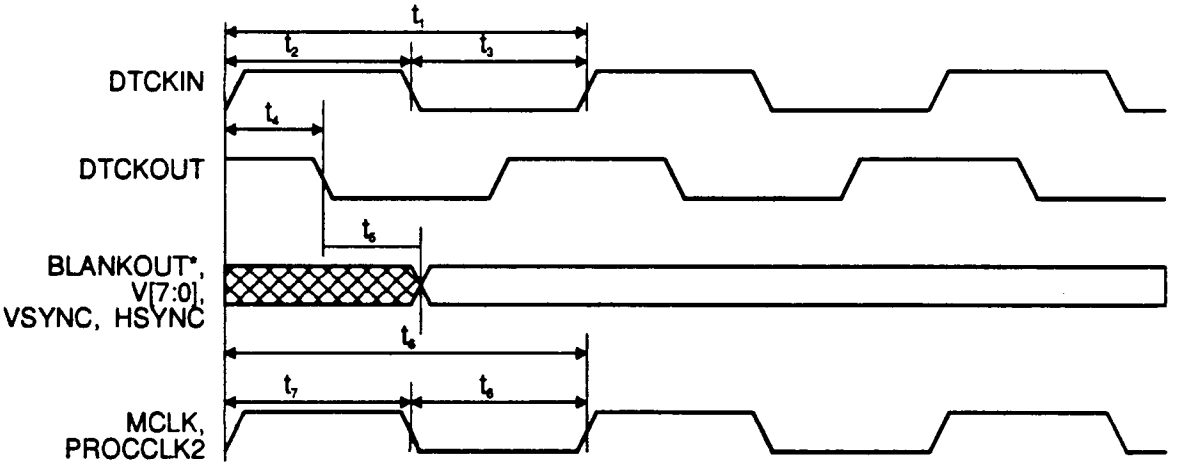


DRAM Refresh Timing

Note: Timing Diagrams are not drawn to scale.

Clock and Video

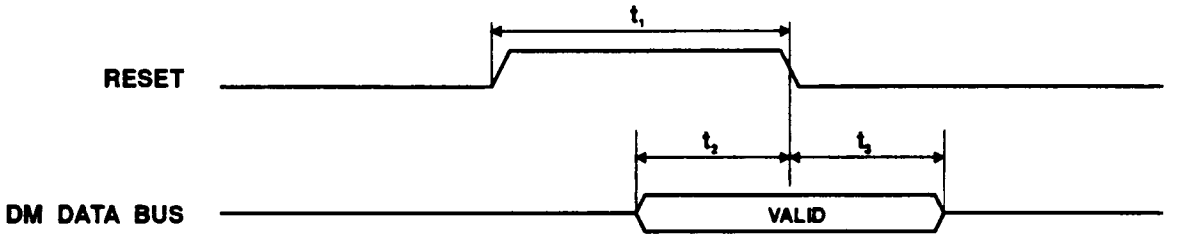
	Parameter	Min	Typ	Max	Units
t1	DOTCLK Clock cycle	12.5			ns (80MHz)
t2,t3	Clock (measured at 2.0V)high & low	[t1/2] - 5%		t1/2+5%	ns
t4	DOTCLK to DTCLKOUT		3	15	ns
t5	DTCLKOUT to BLKOUT*,V[7:0] Delay			3	ns
t5	DTCLKOUT to VSYNOUT, HSYNOUT Delay			5	ns
t6	MCLK period	14.28		25	ns
t7	MCLK High	5.7		5.7	ns
t8	MCLK Low	5.7		5.7	ns
t6	PROCCLK2 period	12.5		125	ns
t7	PROCCLK2 High	5		119.05	ns
t8	PROCCLK2 Low	5		119.05	ns



Note: Timing Diagrams are not drawn to scale.

Reset Timing

	Parameter	Min	Typ	Max	Units
t1	RESET Pulse Width	10t			t=1/MCLK
t2	DM Data Bus Setup to RESET low	50			ns
t3	DM Data Bus Hold from RESET low	30			ns

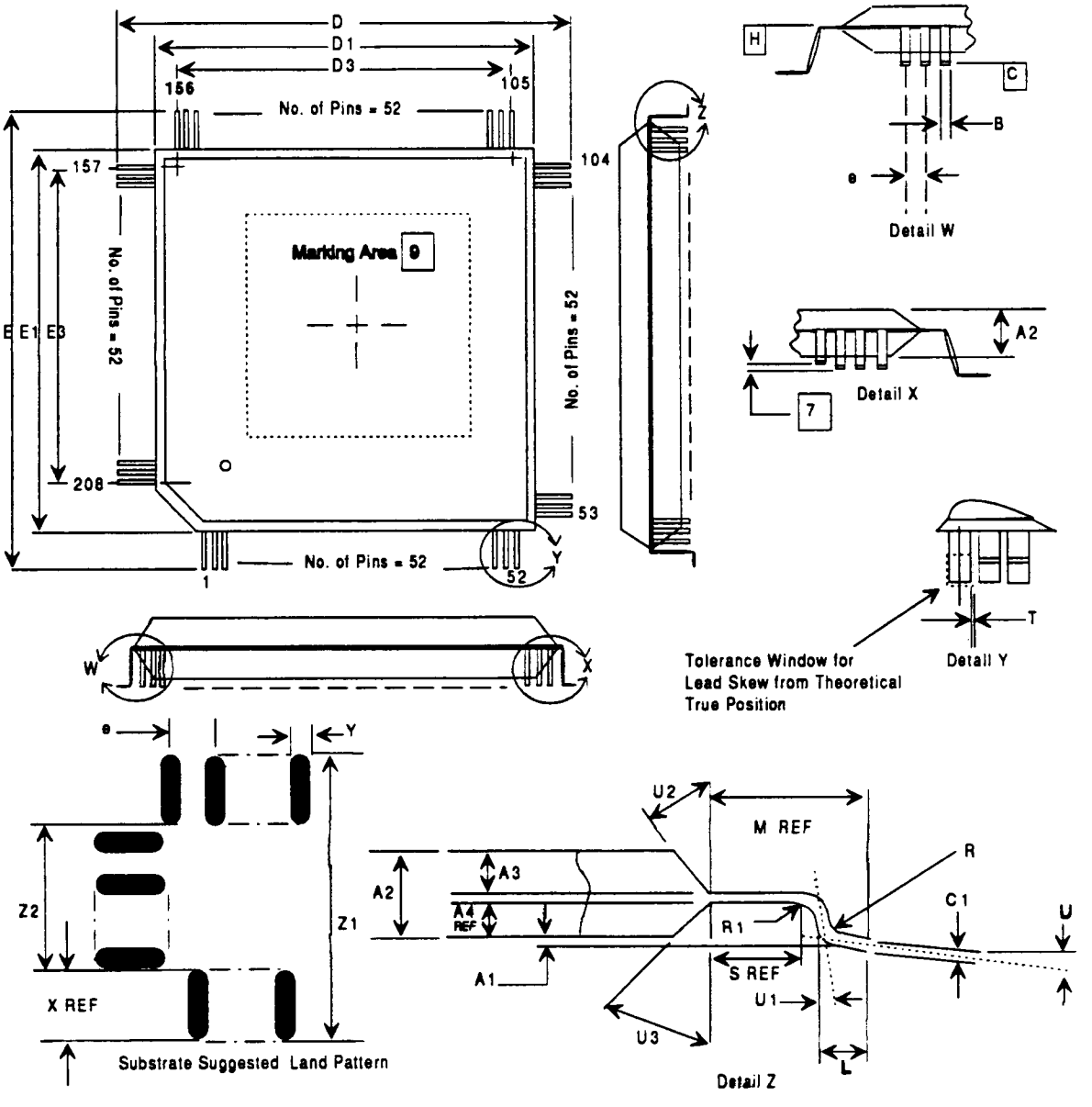


Note: Timing Diagrams are not drawn to scale.

Capacitive Loading for AC Characteristics

Pin	Load in pF
11-18,47,48,87-89,92,93, 99,105, 148,	25 pFCMOS
94,95	30 pF CMOS
173-179,183	31 pF CMOS
3[illegible]-37,107-129,131-139,	35 pF CMOS
44,45	43 pF CMOS
50-62,64-75,79-85	45 pF CMOS
42,149,150	50 pF CMOS
165-172,157,158	55 pF CMOS
38	71 pF CMOS
All Other Pins	85 pF CMOS

Input capacitance of each HT216-32 pin is approximately 10 pF.

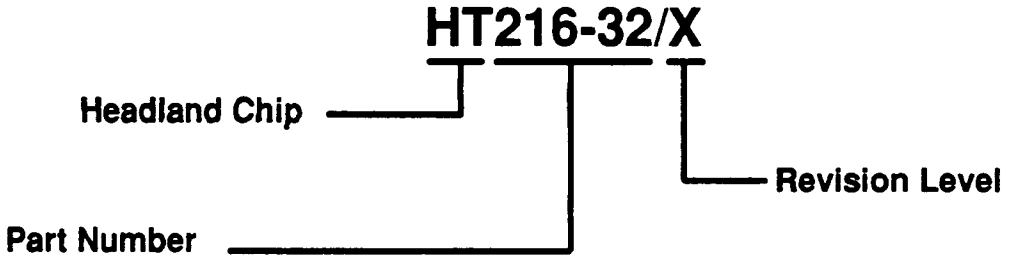

D
D1
D3
156
105
No. of Pins = 52
157
104
Marking Area
E E1 E3
No. of Pins = 52
No. of Pins = 52
208
53
No. of Pins = 52
1
52
Z
Y
H
C
B
e
Detail W
A2
Detail X
7
T
Detail Y
Tolerance Window for
Lead Skew from Theoretical
True Position
W
X
e
Y
Z2
Z1
X REF
Substrate Suggested Land Pattern
U2
M REF
R
A3
A2
A4
REF
R1
C1
U
A1
S REF
U1
U3
L
Detail Z

DIMENSIONS IN MM			
Symbol	Minimum	Maximum	Note
A1	0.25	0.36	
A2	3.40 +/- 0.10		
A3	1.60 +/- 0.05		
A4	1.60 REF.		
B	0.23 +/- 0.05		6, 10
C1	0.15 +/- 0.03		10
D	30.60 +/- 0.20		2
D1	28.00 +/- 0.10		3
D3	25.5 REF.		11
E	30.60 +/- 0.20		2
E1	28.00 +/- 0.10		3
E3	25.5 REF.		11
e	0.5 Basc.		8
L	0.50 +/- 0.10		
M	1.30 REV		
R	0.19 +/- 0.06		
R1	0.13	-	
S	0.40	-	
T	-	0.1	12
U	2.5 +/- 2.5°		
U1	4 +/- 4°		
U2	10 +/- 2°		
U3	10 +/- 2°		
208 PQFP Recommended Land Pattern			
X	2.0 REF.		
Y	0.3 +/- 0.1		
Z1	32.0 +/- 0.1		
Z2	28.0 +/- 0.1		
TOTAL # OF PINS	208		

NOTES: Unless otherwise specified

1. Datum Plane -H- located at mold parting line is coincident with the bottom of lead, where the lead exits the plastic body.
2. To be determined at seating plane -C-.
3. Dimension D1 and E1 do not include mold protursion. Allowable protrusion is .25mm per side.
4. These dimensions to be determined at datum plane -H-.
5. All dimensions in millimeters. Controlling dimension in millimeters. Inches should be rounded to nearest .001 inch.
6. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot minimum space between adjacent leads to be 0.07.
7. Coplanarity of all leads shall be within 0.076mm difference between highest and lowest lead with seating plane -C- as Reference.
8. Lead pitch determined at datum -h-.
9. Marking area free of protrusion and intrusion.
10. Plating thickness included. Plating thickness to be 0.005mm Minimum; 0.020mm Maximum.
11. Dimension D3 and E3 to be centered relative to dimension D1 and E1 within +/- 0.15mm respectively.
12. From the true lead location measured at seating plane -C-.

Product Order Information



IMPORTANT: Contact your local sales office for the current Order Code/Part Number