Features:

- Highly Integrated, Single Chip 80386SX AT Compatible Solution
- Special Multiple Context Hardware EMS Support (LIM 4.0 compatible) using 2 sets of 32 EMS Registers
- Single or Dual BIOS
- Shadow RAM support over entire C0000 to DFFFF Address range in 16K increments, E0000 to FFFFF in 64K increments
- Page Mode and 2-way Interleaving
- Supports up to 12MHz AT Bus Clock
- High Performance Muxed DRAM Interleave
- Programmable DRAM timing
- Asynchronous AT Bus Clock
- Three-State Test Mode
- 16-Bit ROM BIOS Support

HT 18A/B Special Features

- 16 and 20 MHz CPU Clock Speeds
- Supports up to 8M CPU Memory using combinations of 64K, 256K and 1M Devices
- 4 Bank, 4-way Interleave Mode

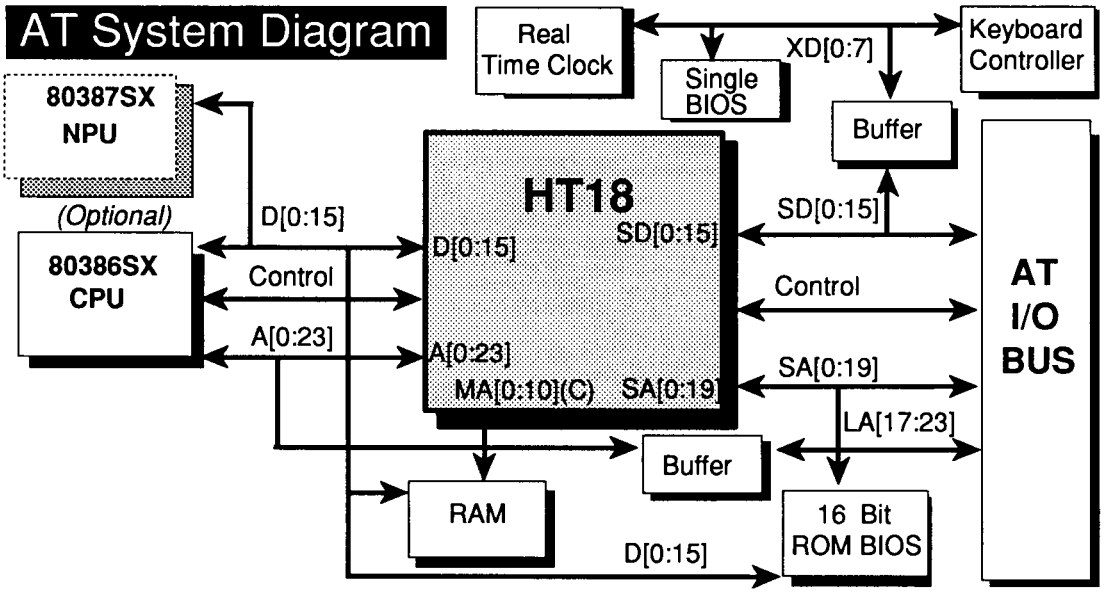
HT18C/25MHz Special Features

- 16, 20 and 25MHz CPU Clock Speeds
- Supports up to 20M with EMS CPU Memory using combinations of 256K, 1M and 4M Devices

Description

The HT18 is an advanced PC/AT compatible, single-chip 80386SX design solution. This highly integrated single chip allows simple, low cost system design options while featuring high performance, low power consumption, and minimum board space requirements. Advanced memory management features include support for page mode, with 2 or 4-way interleaving in both pipelined and non-pipelined modes(18A/B only). Extended Hardware EMS options include dual sets of 32 registers with multiple context operation. Revisions A/B support 256K and 1M DRAMs in 1 by 1, 1 by 4, and 1 by 9 device configurations. Rev C supports 4M devices, as well. A Shadow RAM option for System Video BIOS and dual or single system ROM BIOS support adds to overall design versatility.

A complete PC/AT compatible system with advanced features may be implemented with minimal external support logic. The HT18 performs all CPU and peripheral support functions in a single chip. Integrated device functions include DMA Controllers, a Memory Mapper, Timers, Counters, Interrupt Controllers, a Bus Controller and all supporting circuitry for PC core logic requirements. An asynchronous AT Bus clock allows for a constant 8MHz Bus clock rate for highest bus device compatibility as defined in IEEE Spec P996. This device is packaged in a 208-pin Plastic Quad Flat Pack combining several external buffers into this space saving solution.



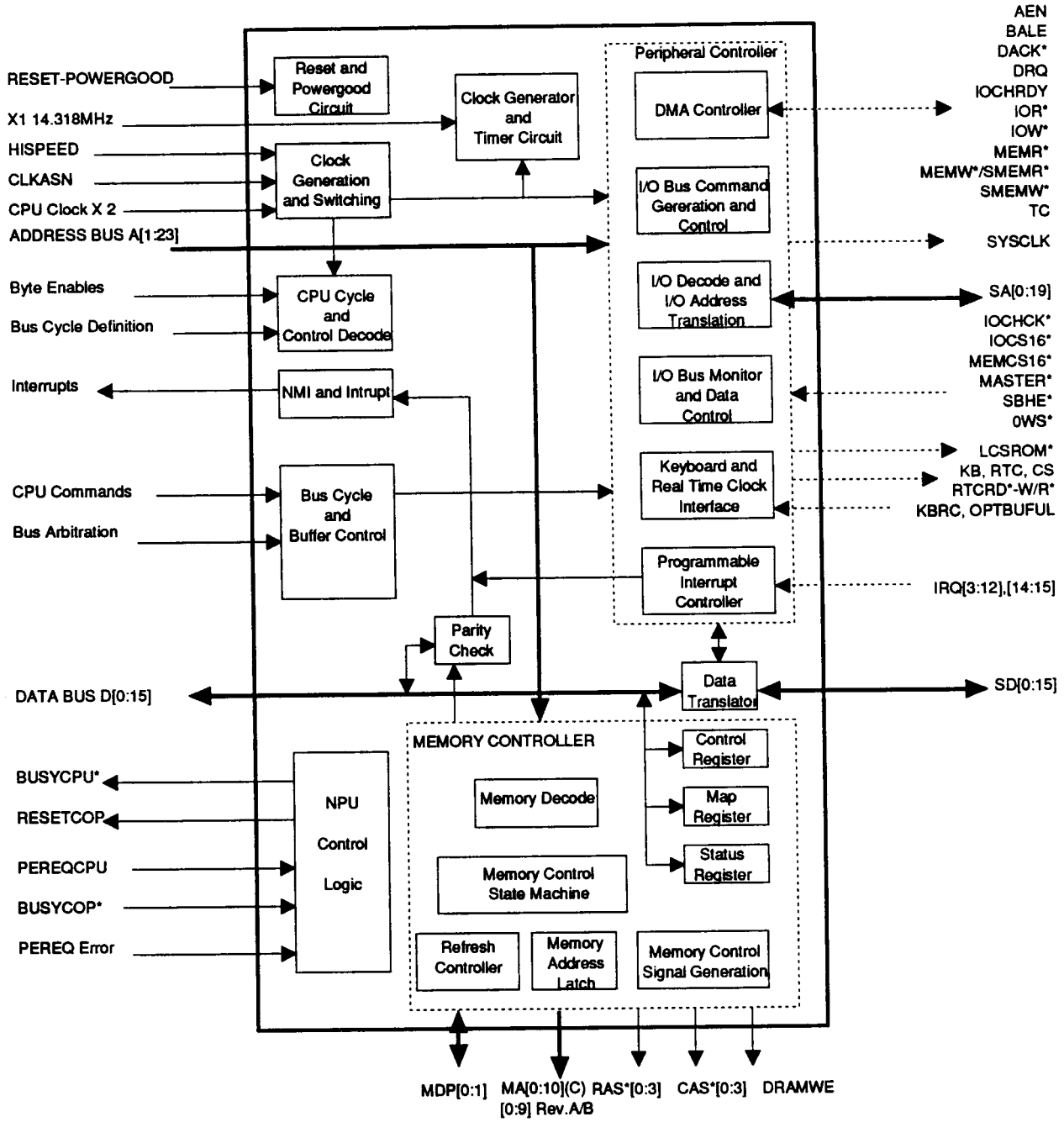
Overview:

The HT18 single chip, integrates the majority of the main board logic required for a cost effective, high performance PC AT-compatible computer based on a 80386SX microprocessor. It provides address control and buffering of the A, SA, and MA buses as well as providing necessary data path interface.

Peripheral circuit functions embedded in this device include: an 82284 compatible clock generation and READY interface, 82288 compatible bus controller, 74612 compatible memory mapper, 8254 compatible programmable interval timer, two 8237 compatible DMA controllers, and two 8259 compatible interrupt controllers.

Additional feature enhancements incorporated into the chip are a special multiple context, high performance hardware LIM EMS control, 8-bit or 16-bit wide BIOS options, flexible memory options, OS/2 Fast Alternate Gate A20 and Hot Reset. This section of the data sheet provides functional descriptions of the following logic sections of the HT18:

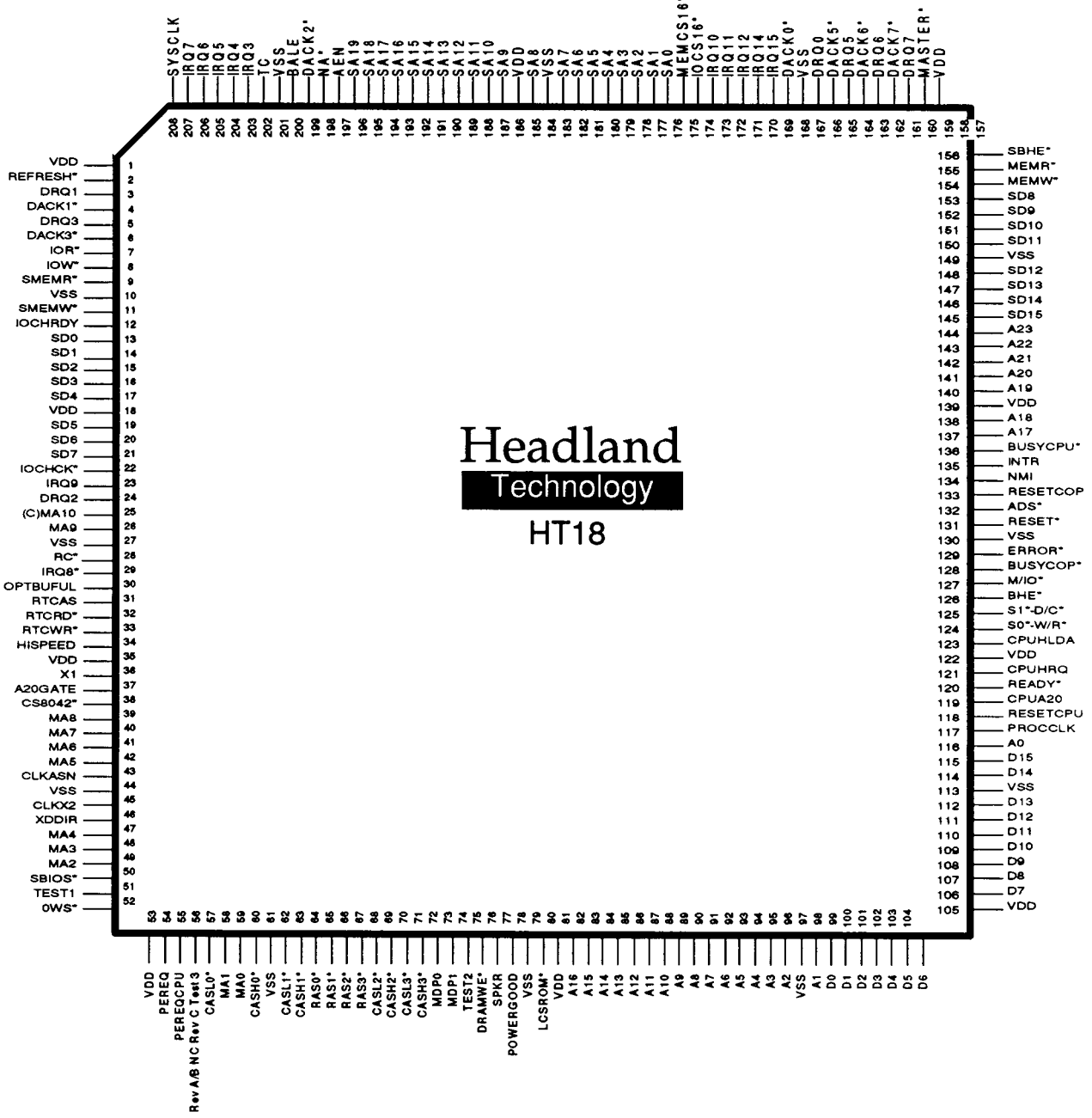
- **CPU Interface**
- **Clock Generation**
  - **Internal Clocks**
  - **Clock Switching Logic**
- **I/O Channel Interface**
  - **I/O Bus**
  - **I/O Decode**
  - **I/O Address Map**
  - **Keyboard Controller Interface**
  - **Real-Time Clock Interface**
  - **DMA Controller**
    - **Address Generation**
    - **Register Descriptions**
  - **Interrupt Controller**
  - **Programmable Interval Timer**
- **Bus Control**
- **NPU Interface**
- **System Control Port - Port 92H**
- **Memory Controller**
  - **DRAM Interface**
  - **Extended Memory**
  - **EMS**
  - **ROM/BIOS Interface**
  - **Pipeline Option**



Internal Block Diagram

Pin Names and Numbers in Alphabetical Order

A[0:23]	116, 97, 95-81, 137, 138, 140-144
A20GATE	37
AEN	197
BHE*	126
BALE	200
BUSYCOP*	128
BUSYCPU*	136
CASH*[0:3]	60, 63, 69, 71
CASL*[0:3]	57, 62, 68, 70
CLKASN	43
CLKX2	45
CPUA20	119
CPUHLDA	123
CPUHRQ	121
CS8042*	38
D[0:15]	98-104, 106-112, 114-115
DACK*[0:3], [5:7]	167,4,199,6,164,162,160
DRAMWE*	75
DRQ[0:3], [5:7]	165,3,24,5,163,161,159
ERROR*	129
HISPEED	34
INTR	135
IOCHCK*	22
IOCHRDY	12
IOCS16*	173
IOR*	7
IOW*	8
IRQ[3:7]	203-207
IRQ8*	29
IRQ[9:12]	23, 172-170
IRQ[14:15]	169, 168
LCSROM*	79
M/IO*	127
MA[0:10]	59, 58, 49-47, 42-39,26, 25
MASTER*	158
MDP[0:1]	72-73
MEMCS16*	174
MEMR*	155
MEMW*	154
NA*	198
NC	50,
NMI	134
NPCS*-ADS*	132
OPTBUFUL	30
PEREQ	54
PEREQCPU	55
POWERGOOD	77
PROCCLK	117
RAS*[0:3]	64-67
RC*	28
READY*	120
REFRESH*	2
RESET*	131
RESETCOP	133
RESETCPU	118
RTCAS	31
RTCRD*	32
RTCWR*	33
S0*-W/R*	124
S1*-D/C*	125
SA[0:19]	175-182,184,186-196
SBHE*	156
SBIOS	50
SD[0:15]	13-17,19-21,153-150, 148-145
SMEMR*	9
SMEMW*	11
SPKR	76
SYSCLK	208
TC	202
TEST[1:3]	51, 74, 56
X1	36
XDDIR	46
0WS*	52
GND	10,27,44,61,78,96,113, 130,149,166,183,201
VCC	1, 18,35,53,80,105,122 139,157,185



(c) = Rev. C option

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn*	Description
CPU Interface 386SX Mode				
A[0:16]	116,97,95-81	I	PU	Address bits [0:16]: Inputs from 80386SX CPU. The HT18 takes the address bus inputs and generates SA bus for I/O slots, and the MA bus for the system DRAM.
A[17:19], [21:23]	137-138,140, 142-144	I/O	PU	A[17:19], [21:23], bi-directional Address lines: Inputs from [21:23] the 80386SX CPU used for memory selection decoding. They output addresses from the memory mapper (internal) logic during DMA operations.
A20	141	I/O		Address 20 is output for CPU cycles and input during Bus Master cycles.
ADS*	132	I/O	PU	ADdress Status input from the 386SX. When low, the 386SX is providing valid address on A[23:1], and driving the R/W*, D/C*, M/IO*, BHE*, A0 control lines.
BHE*	126	I	PU	Byte High Enable: A low at this input enables the high byte [15:8] of the data bus. Driven by the CPU.
CPUA20	119	I	PU	CPU Address 20 from CPU: This input drives the A20 output pin, if CPUHLDA = 0 and A20GATE = 1.
CPUHLDA	123	I	PD	CPU Hold Acknowledge: The CPU drives this input high to indicate that it has released control of the buses.
CPUHRQ	121	O		CPU Hold ReQuest: When high, the HT18 needs to perform a DMA, Refresh, or bus Master operation.
D[0:15]	98-104, 106-112, 114-115	I/O	PU	Bi-directional Data Bus: Transfering data to/from the CPU. This is part of what is commonly referred to as the Local Bus.
D/C*	125	I	PU	Data or Control bus cycles. A high level indicates a 386SX Mode Memory or I/O Data cycle by the 386SX. Low indicates a control cycle; inclusively interrupt acknowledge, halt, or code fetches.
INTR	135	O		INTerrupt Request: A high on this output requests an interrupt from the CPU.
M/IO*	127	I	PU	Memory I/O: From CPU: if high during set up, memory cycle is in progress; if low, I/O cycle is occuring. Three-state when the CPU is in Hold Acknowledge. (See CPUHLDA)

*For Internal PU/PD Resistance Range see DC Specifications.

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
NMI	134	O		Non-Maskable Interrupt: A high level forces the CPU to unconditionally execute an interrupt routine.
PROCCLK	117	O		PROCessor CLocK: this output supplies the clock signal for the CPU and co-processor. It drives CLK on the CPU, and the clock lines on the co-processor. Rate determined by HISPEED.
READY*	120	O		READY: A low level tells the CPU that the current bus cycle is near completion.
RESETCPU	118	O		RESET CPU: A low-to-high transition resets the CPU during powerup, keyboard reset, and shutdown status. The rising edge resets the CPU, if the pin is held high for 16 clock cycles.
W/R*	124	I	PU	Write or Read bus cycles of the 386SX; high for 386SX Mode Writes, low for Reads.

Keyboard and RTC Interface

CS8042*	38	O		Chip Select 8042: A low level drives CS* of an external keyboard controller.
IRQ8*	29	I	PU	This input is driven by a Real Time Clock interrupt output to support standard RTC devices. (Note that Interrupt Request 8 is active low, unlike the other Interrupt Requests.)
OPTBUFUL	30	I	PD	OutPuT BUffer FULl: Input from P24 of the keyboard controller. Setting this pin high activates the internal IRQ. This causes an INTR to the CPU, indicating the keyboard buffer is full.
RC*	28	I	PU	Reset CPU: When driven low by the keyboard controller (P20), the CPU resets its internal registers.
RTCAS	31	O		Real Time Clock Address Strobe:A low to high signal transition latches the RAM address for read/write operations.
RTCRD*	32	O		Real Time Clock ReaD: When low, data is read from the RTC.
RTCWR*	33	O		Real Time Clock WRite: When low, data is written to the RTC.

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
I/O Interface				
AEN	197	O		Address ENable DMA: This signal is used to disconnect the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When AEN is high, the DMA controller drives the address bus, data bus, I/O read/write lines and memory read/write signals.
BALE	200	O		Buffered Address Latch Enable: This signal is provided by the 82288 bus controller and is used to latch valid addresses and memory decodes from the microprocessor. It is used by the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). A high level indicates the presence of valid address at the I/O slots. System Addresses (SA[0:19]) are latched on the falling edge of BALE.
DACK*[0:3], DACK*[5:7]	167,4, 199, 6, 164, 162, 160	O		DMA ACKnowledge: When low, these signals are used to DACK*[5:7] requests (DRQ[0:3],[5:7]) from peripherals on the I/O expansion slots.
DRQ[0:3], DRQ[5:7]	165, 3, 24, 5 163,161,159	I	PD	DMA ReQuests: These asynchronous channel requests DRQ[5:7] are used by peripheral devices and the I/O channel microprocessors, active high signals request DMA services or control of the system. They are prioritized with DRQ0 having the highest priority and DRQ7 having the lowest. Each signal should be held high until the corresponding DMA Request Acknowledge (DACK* signal) goes active (low). DRQ[0:3] govern 8-bit DMA transfers, DRQ[5:7] control 16-bit DMA transfers with devices on the I/O slots.
IOCHCK*	22	I	PU	I/O CHannel CheckK: A low on this input indicates there is an uncorrectable system error. Provides the system board with parity (error) information about memory or devices on the I/O channel. This causes the NMI (Non-Maskable Interrupt) output to become active (high), and interrupts the CPU. Needs external 4.7K Ohm pullup.
IOCHRDY	12	I	PU	I/O CHannel ReaDY: This signal is used by any slow I/O device driving this line low immediately upon detecting its valid address and a Read/Write command. The HT18 will add more wait states for a page miss by pulling this signal low. Needs external 1K Ohm pullup and should be driven low or active by any open collector device.

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
IOCS16*	173	I	PU	I/O Chip Select 16: A low indicates a 16-bit I/O data transfer on the SA bus. This signal should be driven by an open collector or three-state driver capable of sinking 20mA. Needs external 300 Ohm pullup.
IOR*	7	I/O	PU	I/O Read: When low, instructs an I/O device to drive or write its data onto the data bus. It is driven by the microporcessor or DMA controller, either resident in the system or on the I/O channel.
IOW*	8	I/O	PU	I/O Write: When low, instructs an I/O device to read or capture the data on the data bus. It may be driven by any microprocessor or DMA controller in the system.
IRQ[3:7], IRQ[9:12], IRQ[14:15]	203-207, 23, 172-170, 169-168	I	PU	Interrupt ReQuest: These pins signal the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine). IRQ3 has the highest priority interrupt, IRQ15 the lowest.
MASTER*	158	I	PU	MASTER*: This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel issues a DRQ to a DMA channel in cascade mode and receives a DACK*. Upon receiving the DACK*, an I/O microprocessor pulls MASTER* input low, which will allow it to control the system address, data, and control lines. After this signal is pulled low the I/O microprocessor must wait one system clock period before driving the address and data lines and two clock periods before issuing a Read/Write command. If this signal is held low for more than 15 microseconds, the system memory may be lost because of a lack of refresh.
MEMCS16*	174	I	PU	MEMory Chip Select 16 wide: External devices drive this input low for 16-bit data transfers. Connects to the system expansion bus. Needs external 300 Ohm pullup.
MEMR*	155	I/O	PU	MEMory Read signal: Output is low during a memory read cycle. This signal instructs the memory devices to drive data onto the data bus. It can be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel drives this signal it must have the address lines valid on the bus for 1 system clock period before driving MEMR* active. Three-stated when MASTER* is low and the CPU does not control the system. Not active during local memory cycles.

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
MEMW*	154	I/O	PU	MEMory Write signal:Output is low during a memory write. This signal instructs the memory devices to store the data present on the data bus. It is active during all memory write cycles and can be driven by any microprocessor or DMA controller in the system. When driven by a microprocessor on the I/O channel the address lines on the bus must be valid for one system clock period before driving the signal active. This is three-stated when MASTER is low. Not active in local memory cycles.
REFRESH*	2	I/O		REFRESH input is low when the current cycle is for memory refresh and can be driven by a microprocessor on the I/O channel. Needs external 470 Ohm pullup.
SA0	175	I/O	PU	System Address bit 0: Bi-directional address bit on the expansion slot. It supplies address bit 0 during refreshes.
SA[1:19]	176-182,184, 186-196	I/O	PU	System Address bus: Bi-directional bus used to address memory and I/O devices within the system. These lines alone allow access of up to 1MB of memory and up to 16MB when used with LA[18:23]. SA[0:19] are gated on the system bus when BALE is high and are latched on the falling edge of BALE. These signals are generated by the microprocessor or DMA controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.
SBHE*	156	I/O	PU	System Byte High Enable: Low when peripherals are performing a transfer on the upper byte. 16-bit devices use SBHE* to condition data bus buffers tied to SD[8:15].
SD[0:15]	13-17,19-21, 153-150, 148-145,	I/O	PU	I/O System Data Bus: These signals provide bus bits [0:15] for the microprocessor, memory, and I/O devices. SD0 is the least-significant bit and SD15 is the most significant bit. All 8-bit devices on the I/O channel use SD[0:7] for communications to the microprocessor. The 16-bit devices will use SD[0:15]. To support 8-bit devices, the data on SD[8:15] will be gated to SD[0:7] during 8-bit transfers to these devices; 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
SMEMR*	9	O		System MEMory Read: Low during memory reads. This signal instructs the memory devices to drive data onto the data bus. It is active only when the memory decode is within the low 1MB of memory space. This is a buffered version of MEMR*.
SMEMW*	11	O		System MEMory Write: Low during memory writes. This signal instructs the memory devices to store the data present on the data bus. It is active only when the memory decode is within the low 1 MB of memory space. This is a buffered version of MEMW*.
SYSCLK	208	O		SYStem CLocK: This provides a clock for devices on the expansion slot. SYSCLK is a quarter of CLKASN.
TC	202	O		Terminal Count: pulses high when the DMA channel terminal count is reached. This signal is available on the expansion slots.
XDDIR	46	O		EXternal Data BUS control for KBD and RTC: 1 = Write 0 = Read
0WS*	52	I	PU	Zero Wait State: This signal tells the microprocesser that it can complete the present bus cycle without inserting additional wait cycles. It comes from an address decode gated with a Read/Write command. In order to run a memory cycle to an 8-bit device with a minimum of 2 wait states, 0WS* must be driven low one system clock after Read/Write commands are gated with the address decode for the device. These Read/Write commands are active on the falling edge of the system clock. This signal should be driven by an open collector or three-state driver capable of sinking 20mA. External 300 Ohm pull up.

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
NPU Interface				
BUSYCOP*	128	I	PU	BUSYCOP* input to be connected to BUSY* output of the coprocessor. When the math co-processor is working, it drives this pin low, which in turn forces BUSYCPU* output low and halts the CPU.
BUSYCPU*	136	O		BUSYCPU* output connects to the BUSY* input of the CPU. A low level on this pin indicates the math co-processor is operating. Interrupts are honored by the CPU while this input is low. (See ERROR*)
ERROR*	129	I	PU	ERROR: Connect ERROR* from the co-processor to this input. A low level indicates the math co-processor has an unmasked error condition.
PEREQ	54	I		Processor Extension REQuest: Request from NPU for Processor Extension. If this logic is to remain dormant leave this pin floating. This signal uses a CMOS input buffer.
PEREQCPU	55	O		Processor Extension REQuest to CPU: Request passed on to CPU from NPU for extension. If this logic is to remain dormant leave this pin floating.
RESETCOP	133	O		Not Connected
Memory Interface				
CASH*[0:3]	60,63, 69,71	O		Column Address Strobe High order byte: Control up to four banks of DRAMs.These signals can be connected directly to DRAM CAS inputs through a 22 Ohm resistor. (Resistor value may vary with board layout and number of RAMs used.)
CASL*[0:3]	57,62, 68,70	O		Column Address Strobe Low order byte: Controls up to four banks of DRAMs. These signals can be connected directly to DRAM CAS inputs through a 22 Ohm resistor. (Resistor value may vary with board layout and number of RAMs used.)
DRAMWE*	75	O		DRAM Write Enable: Generates the write strobe to DRAMs. This is a gated signal derived from the MEMW* input.

Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
LCSROM*	79	O		Latch Chip Select ROM: Drives the chip enable pins of the EPROM, ie E0000-FFFFF and FE0000-FFFFFF for EPROMs.
MA[0:9] MA10(C)	59-58, 49-47, 42-39, 26, (25)	O		Multiplexed Address bus: to DRAMs, should connect to the memory address of the DRAM through 22 Ohm resistors. MA10 - Rev C only.
MDP[0:1]	72-73	I/O	PU	Memory Data Parity: Low (0) and high (1) bytes: When data is written to RAM or read from RAM its parity value is calculated.
RAS*[0:3]	64-67	O		Row Address Strobe: Controls up to four banks of DRAMs. These signals can be connected directly to DRAM RAS inputs through a 22 Ohm resistor. (Resistor value may vary with board layout and number of RAMs used.)
SBIOS*	50	I	PU	Switch for single BIOS: 1 = Two Chip BIOS 0=Single BIOS
Clock Inputs				
CLKX2	45	I	PU	CLocK X 2: Drive this clock input at twice the desired processor clock (PROCCLK) frequency. This signal is used when CPU is running at "High" speed. For 16MHz system operations CLKX2 and CLKASN can share the 32MHz OSC.
CLKASN	43	I	PU	CLocKASN: Drive this clock input at four times the desired SYSCLK frequency. This signal is used when CPU is running at "Low" speed. For 16MHz system operations CLKX2 and CLKASN can share the 32 MHz OSC.

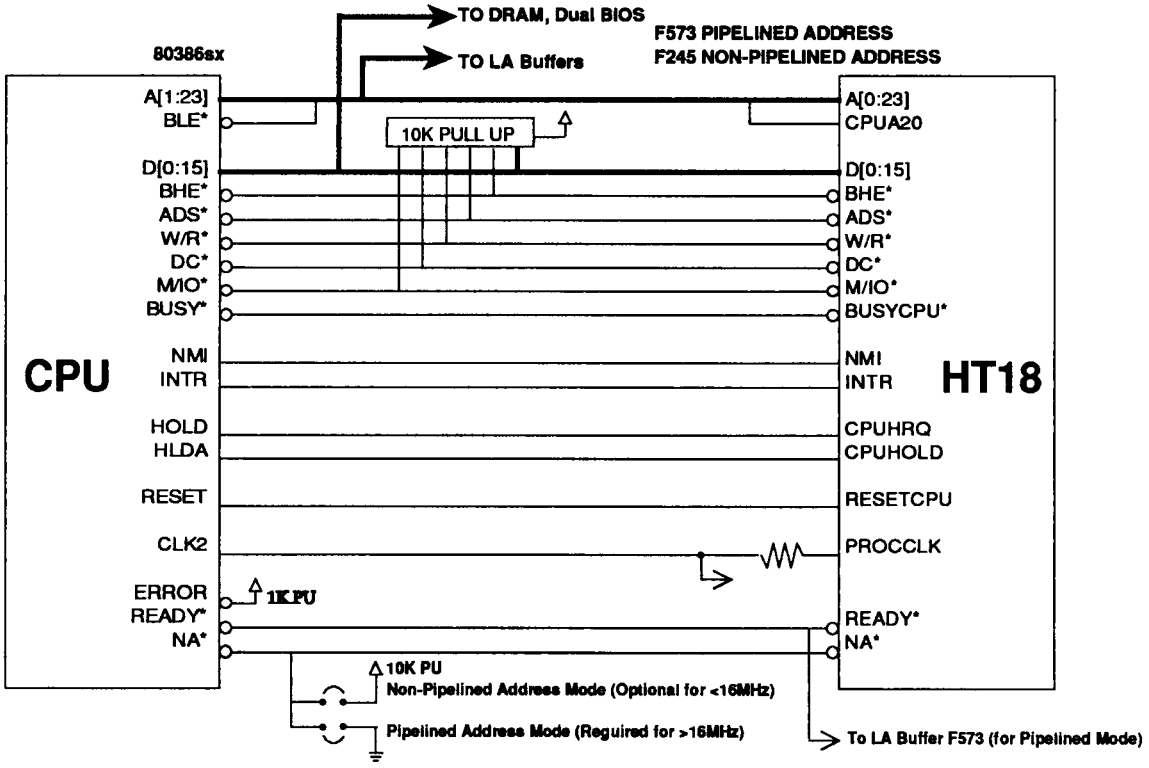
Pin Symbol	Pin Number	Pin Type	Internal Pull Up/Dn	Description
X1	36	I	PU	This input is tied to a 14.31818 MHz Oscillator, to generate OSC.

Miscellaneous and Reset

A20GATE	37	I		Gates address from CPU: If CPUHLDA=0 the CPU is driving the address bus. When A20GATE is high, the upper address bit (CPUA20 input) drives the A20 pin directly, when low the A20 output is forced low if Port 92 bit 1 = 0.
HISPEED	34	I	PU	HIgh SPEED: When high, PROCCLK (the processor clock) speed is equal to the CLKX2 rate for on-board memory accesses. When low, PROCCLK is one half of CLKASN.
NA*	198	I		Next Address: This is used to place the HT18 in pipeline mode. A low or 0 = Pipeline mode, 1 = non-pipeline mode (default)
NC	50			Not Connected
POWER-GOOD	77	I	PU	POWERGOOD: When low, it resets the HT18 controller. A Schmitt Trigger buffers the input pin.
RESET*	131	O		RESET: A low level used to reset the system logic at power-up or low-line voltage. (Open Drain Outputs)
SPKR	76	O		SPeaKeR: Output of the Timer 8254 Channel 2 (mega function). This connects to a speaker, through a buffer.
TEST [1:3]	51, 74, 56	I	PU	Tie TEST[1:3] ICT test functions can use these pins to float all output pins by pulling them low. For normal non-test operation these pins should not be used or connected.TEST 3 must be grounded for normal operation.

CPU Interface

The HT18 provide all the CPU main board interface signals for Numeric processor, memory, peripherals, and I/O interface required for a PC AT-compatible computer. The HT18 supports common CPU processor speeds of 12.5, 16 , 20 MHz. Rev C supports 12.5 to 25 MHz processor speeds. To obtain the highest system performance with lower cost DRAM technology at higher CPU speeds, the 80386SX address pipelining option is fully supported.

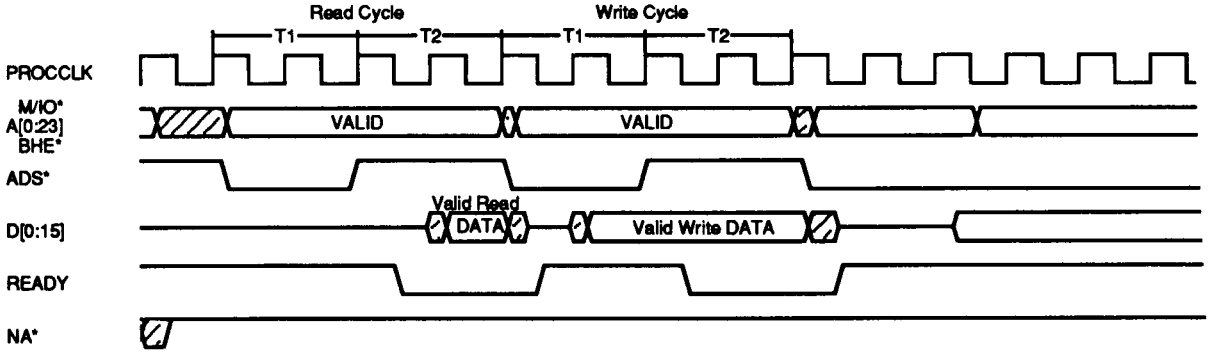


CPU Interface Diagram

Major signal timing relationships and sequences are shown 80386SX CPU interfaces. Both pipelined and non-pipelined address timings are shown for 80386SX CPU's with emphasis on the functional timing relationship between signals.

The fastest 386SX microporcessor bus cycles require only two bus states. The diagrams below show two read and write cycles with each cycle having two bus states. These bus states are named T1 and T2 or in the case of pipelined address mode, T1P and T2P.

Any memory or I/O address may be accessed by these two-state bus cycles if the responding device is fast enough. The HT18 can end these fast two-state cycles by acknowledging the end of the cycle by use of the READY* handshake. In the event the responding device is not fast enough to complete the cycle in two-states, the HT18 delays the READY* signal activation, causing insertion of extra bus cycles until READY* signal activation terminates the cycle. These extra bus cycles or wait-states are further illustrated in the sections on I/O Channel Interface including: Keyboard, RTC, DMA, PIT and Interrupt Controller associated with I/O devices. The Memory Controller Section also contains explanations on wait-states during local DRAM and ROM cycles.

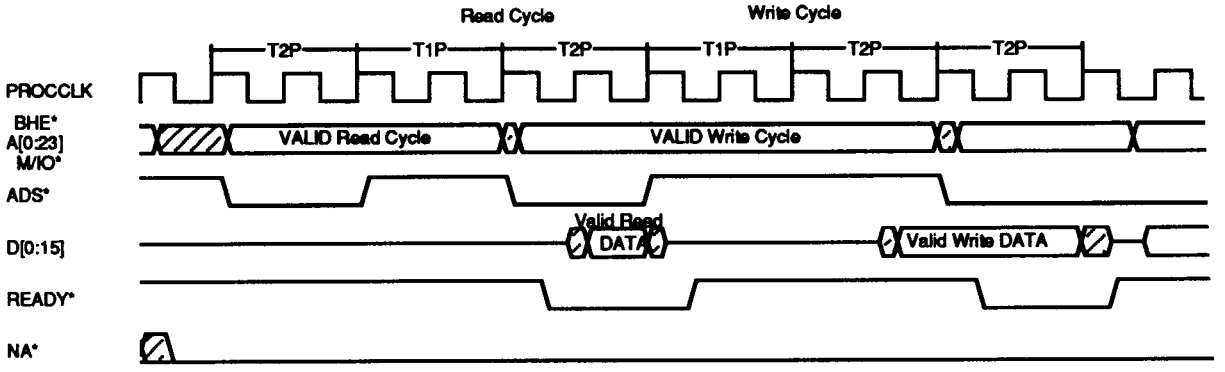


80386SX CPU FUNCTIONAL TIMING - Read and Write Cycles Non-pipelined Addressing

Pipelined address mode is required for 20/25MHz 386SX microprocessor operation. For this mode the NA* signal to the HT18 and the 386SX must be tied to ground. The BHE*, A[0:23], M/IO* and D/C* signals are driven low during the last T2P cycle for the next cycle. This provides the extra memory decode time needed to maintain zero wait state page operation in the upcoming cycle. The disadvantage of this mode is that in order to establish the address pipeline after an idle or hold acknowledge cycle the first cycle must be a non-pipelined T1 cycle and finish with an extra T2P cycle, as shown in the 386SX funtional CPU Pipeline Diagram.

In actual operation address pipelining is almost always maintained because in the absence of any other request, a code prefetch request is always internally pending until the instruction decoder and code prefetch queue are completely full. This insures that when operating in this mode the address pinpeline is maintained for long periods unless the bus in not available, as in Hold Acknowledge cycles or other unusual type operations.

Detailed AC timing specifications from indicated clock edges are found in the AC Specification Section.

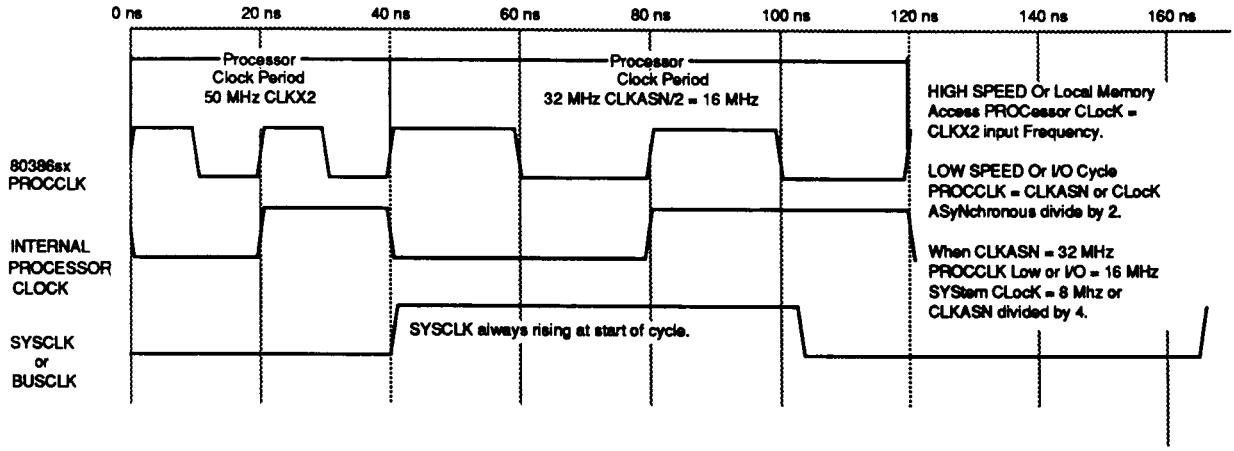


80386SX CPU FUNCTIONAL TIMING - Read and Write Cycles Pipelined Addressing

Clock Generation

The HT18 clock generator provides all the clock switching and control for the main processor clock (PROCCLK), internal clocks (DMACLK), and I/O bus clock (SYSCLK). All clock signals are described below:

PROCCLK is an output clock for the selected processor and should have a frequency twice the desired processor frequency. The source for PROCCLK can switch from three sources depending on cycle type and operation mode. These three sources are CLKX2 input pin, CLKASN input pin divided by two.



CPU PROCESSOR CLOCK RELATIONSHIPS

CLKX2 is an input pin which determines the full speed clock or the maximum CPU clock rate. The frequency of this input should be twice the desired CPU clock frequency. This input would be one of three sources used for PROCCLK .

CLKASN is an input pin that is the source for SYSCLK (system Clock), and as an alternate PROCCLK source. The frequency of this input would be divided by two to provide the alternate PROCCLK source for low speed or special I/O operations. It is again divided by two to provide the SYSCLK (system clock) output which is typically used for system bus clock (BCLK) on an AT compatible bus. A 32MHz input frequency is used to provide an 8MHz SYSCLK output to meet the IEEE P996 AT compatible bus specification and would result in a 16MHz low speed PROCCLK frequency for an 8MHz processor speed.

HISPEED is an input pin used to define two speed modes and is used to determine two sources of PROCCLK . A high level on this pin would indicate the high speed mode and PROCCLK source from CLKX2. A low on this pin would indicate the low speed mode and PROCCLK source from CLKASN. In some applications this pin could be used in conjunction with 'Turbo' or high speed/low speed switch.

SYSCLK is an output pin typically used as BCLK (system bus clock) source for AT compatible bus applications. To insure full IEEE P996 compatibility the SYSCLK should be a maximum of 8MHz.

X1 is an input pin used to provide the clock for an internal programmable interval timer. This timer is an 8254 equivalent and can be programmed by the CPU and provides signals for system timing, refresh, and speaker tone generation.

Internal Clocks: Clocks internal to the HT18.

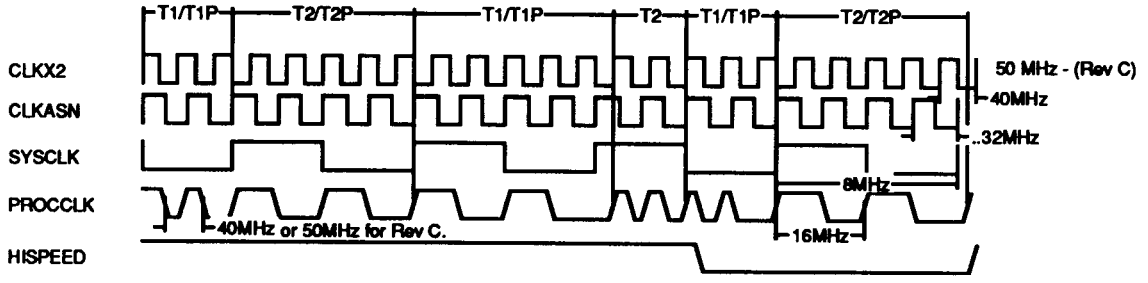
DMACLK is used for internal DMA use and is the PROCCLK + 4.

CPU Clock Switching

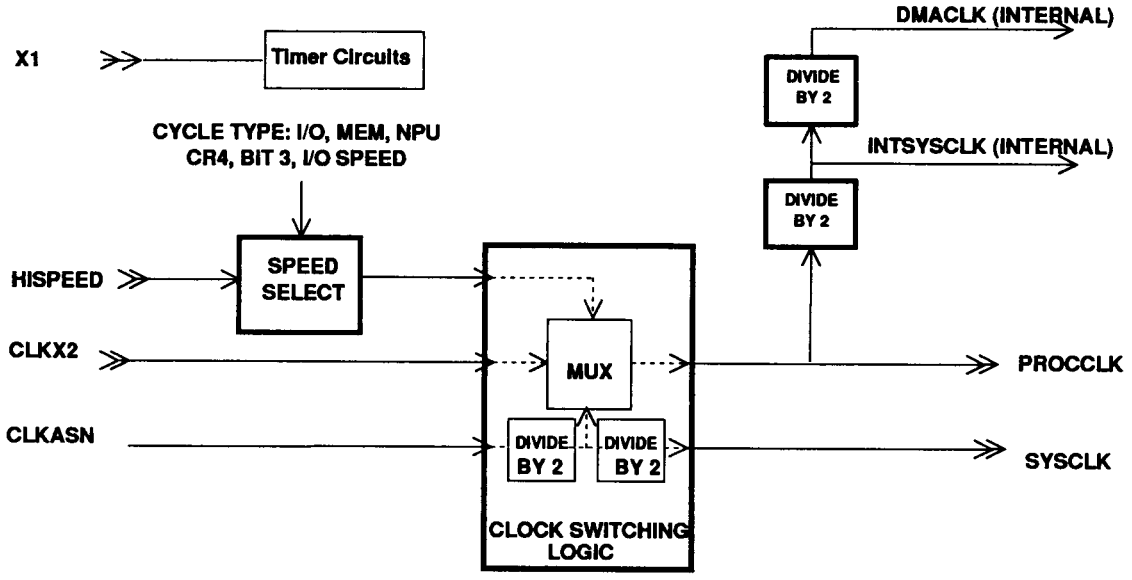
To maintain the highest level of compatibility with AT I/O bus specifications, while running at higher processor speeds, the HT21 allows switching between two asynchronous clock sources. A standard 20MHz CPU configuration supporting the IEEE, P996 Spec of a maximum 8MHz bus clock (SYSCLK) requires two asynchronous clock sources. The high speed CPU clock source would be a 40MHz CLocK X2 (CLKXS = CPU frequency X2). The standard 8MHz I/O bus clock or SYSCLK and the 16MHz low speed CPU clock (for AT compatible I/O cycles) are derived from a second source CLKASN. A 32 MHz CLKASN + 4 provides an 8MHz SYSCLK and + 2 provides a 16MHz PROCCLK during I/O cycles.

A standard 16MHz system would use a single 32MHz source for both CLKX2 and CLKASN inputs. A single 24 MHz source could provide a 24MHz CPU CLKX2 and a 6MHz system clock or bus clock.

PROCCLK switching synchronization requirements will cause the last phase low period of a processor clock cycle, TS, T1, or T1P, to be extended until the clocks are synchronized. In a high speed (CLKX2 = PROCCLK source) to low speed (CLKASN = PROCCLK source) switch, the low period will be extended until the rising edge of SYSCLK. A low to high speed switch has no additional qualification requirements and will switch within one CLKASN period and one CLKX2 period.



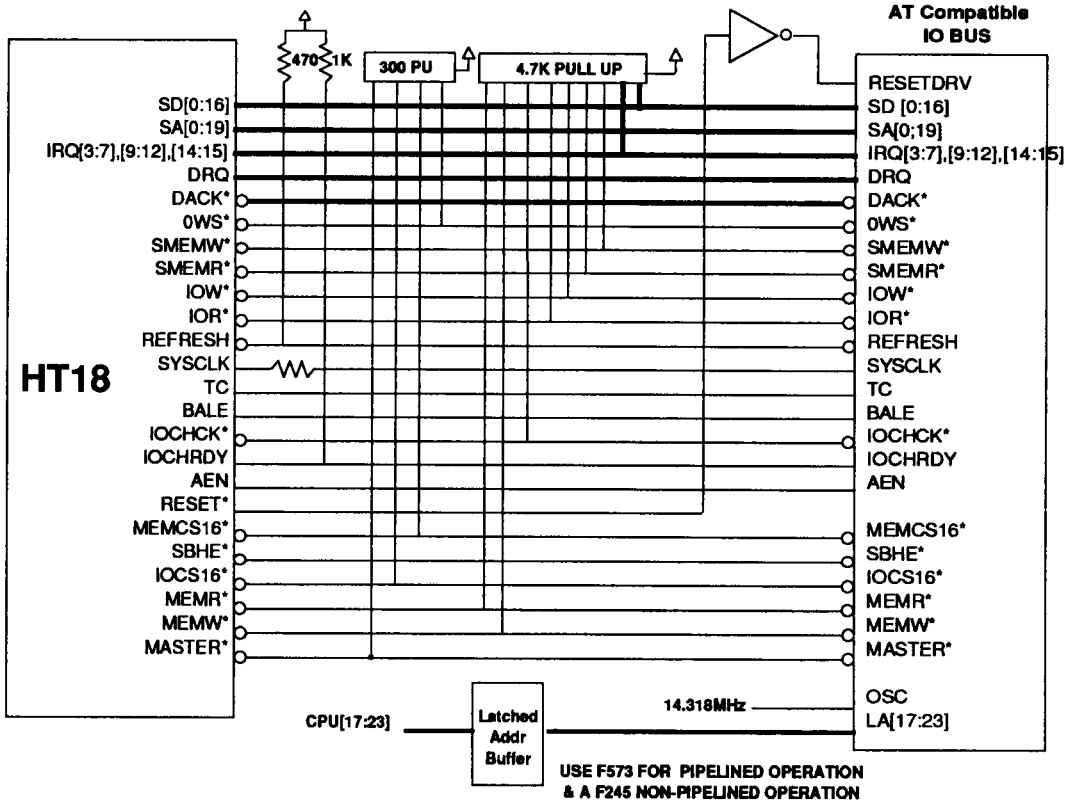
CLOCK SWITCHING DIAGRAM PROCessor CLocK - High speed CLocK X 2 switch to Low speed1/2 CLocKASN Input - Low speed, 1/2 CLKASN to High speed, CLKX2 - HISPEED Switch High to Low



Clock Switching Diagram

I/O Channel Interface

The HT18 I/O Channel Interface includes all system I/O devices as well as an AT compatible 8 or 8/16 bit Bus as defined by the IEEE P996 specification. This interface is managed by an internal Peripheral Controller that is used to control all I/O channel bus cycles. From a system standpoint, these I/O channel bus cycles are defined as all CPU cycles not claimed by internal memory address decode logic and resulting CPU local bus memory cycles. This can include typical system board resources such as RTC and keyboard. These external devices are explained in detail in a separate section.



I/O Channel Interface

I/O Bus

The Peripheral Controller contains an I/O Bus state machine that synthesizes the address strobe signal (BALE), and many of the bus command signals (IOR*, IOW*, MEMR*, and MEMW*). It also monitors the state of the IOCS16* and MEMCS16* signals to determine if the device on the bus is capable of 16-bit operations for I/O and memory respectively. If a 16-bit operation is attempted with an 8-bit device, the HT18 performs the necessary conversions of 16-bit CPU operations to paired 8-bit bus cycles. Typical system implementations include an external Data bus or XD-bus that can connect 8-bit system peripherals to the CPU. The HT18 supports an external buffer connecting XD to the SD bus with an eXternal Data bus DIRection (XDDIR) output.

Basic I/0 channel cycle operation occur as follows:

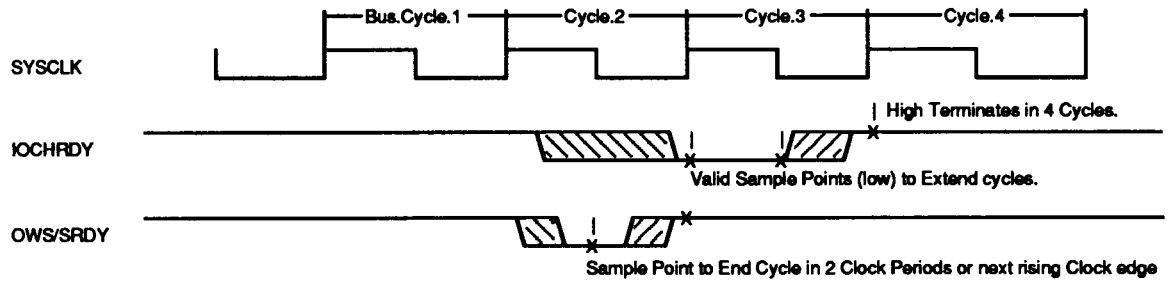
1. During processor state Ts, T1 or T1P internal decodes determine if a bus cycle should be performed.

2. The PROCCLK frequency is switched to CLKASN divided by 2 to provide 8MHz AT Bus compatibility. This clock switching operation may be disabled by use of the IOSPEED bit, D3, of Control Register 4.

3. The HT18 bus controller initiates the bus cycle by generating BALE during the I/O bus state Ts. The bus controller then times out the COMMAND DELAY interval and asserts the appropriate command output.

	AT BUS MEMORY		AT BUS I/O		AT BUS INTERRUPT
	8-BIT	16-BIT	8-BIT	16-BIT	ACKNOWLEDGE
COMMAND DELAY	YES	NO	YES	YES	YES
WAIT STATES	4	1	4	1	-

4. In response to the asserted command, the internal wait-state logic times out for the number of processor BUSCLK's before beginning to monitor the IOCHRDY input. When the IOCHRDY input sampling is active, the bus controller deactivates the command. If the cycle in process does not require conversion cycles (8-Bit to 16-Bit) the HT18 asserts READY* and the cycle terminates. The setup time to this IOCHRDY sampling point must be maintained to properly extend the cycle.

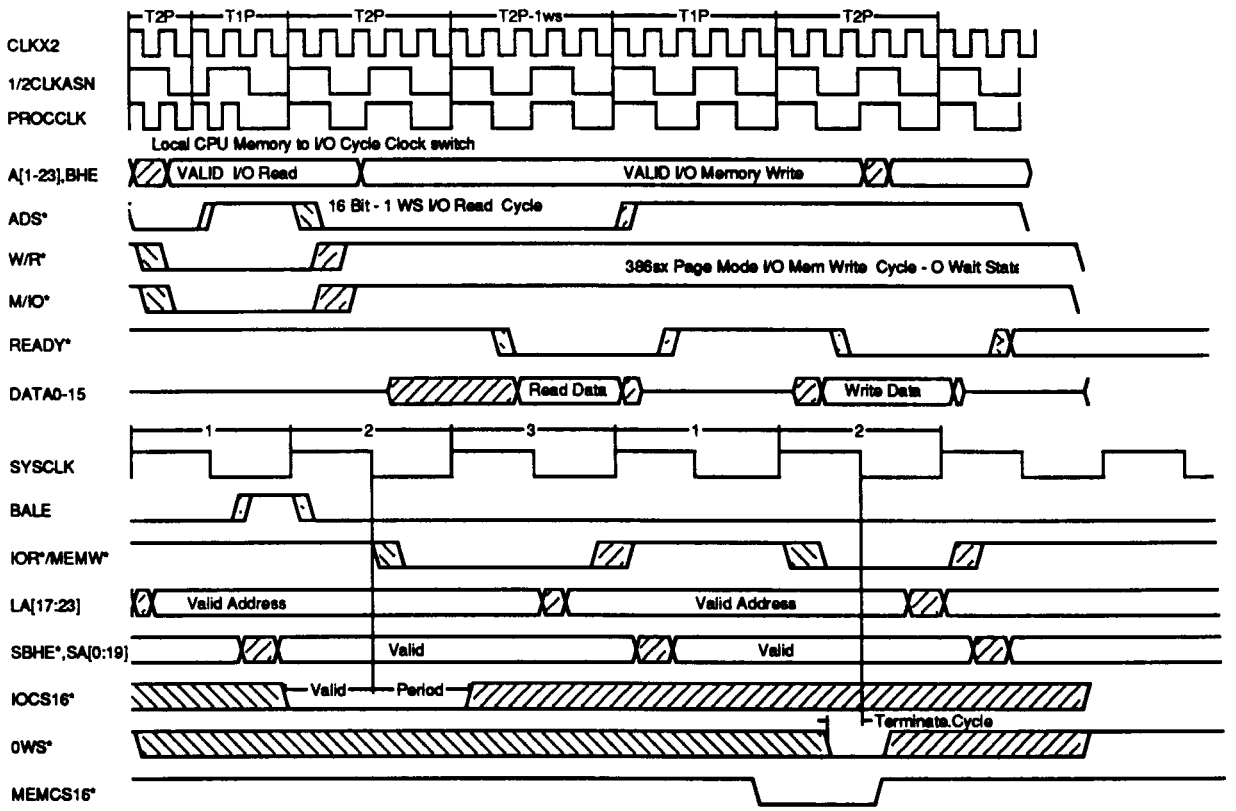


IOCHRDY & OWS - VALID SAMPLE AND TERMINATION POINTS

5. If the cycle in progress requires a conversion cycle (8-Bit to 16-Bit), the I/O state machine sets this mode and begins to time out the BALE DELAY interval. At the end of this interval, the bus controller will be retriggered to produce another cycle as described in (3) and (4). Note that another BALE is not generated for the second cycle.

6. At the end of the second cycle, the HT18 generates processor READY*, and the CPU cycle terminates.

The I/O channel clock signal, SYSCLK, is fixed at 1/4 CLKASN but internal DMACLK and SYSCLK are always divided from the PROCCLK. See the clock generation section to understand these relationships more fully.



I/O BUS FUNCTIONAL TIMING - Standard Read Cycle and 0ws I/O Memory Write Cycle

Master Arbitration Cycle

A Master device will start the master arbitration cycle by asserting an assigned DMA Request (DRQ) and waits for the corresponding DMA Acknowledge (DACK*) as in a standard DMA Cycle, but for correct master device operation the assigned DMA channel must be programmed for Cascade Operation. In this mode the DMA controller ignores all inputs except CPUHLDA and DRQ on the active channel. When the DACK* is received by the Master device, it will drive the MASTER* signal. This will reverse the direction of various bus drivers and forces AEN to deassert, which indicates that the Master device has control of the bus.

The Master can remain in control indefinitely if it maintains System Refresh and can perform I/O or memory cycles as needed. In actual practice, most Master devices limit transfers to 4 or 5 cycles and then re-arbitrate by deasserting MASTER* and DRQ. Some Master devices are able to generate very short command pulse widths in high speed, non-AT Bus compatible operations and must be set to slow or moderate speed/command pulse width timing.

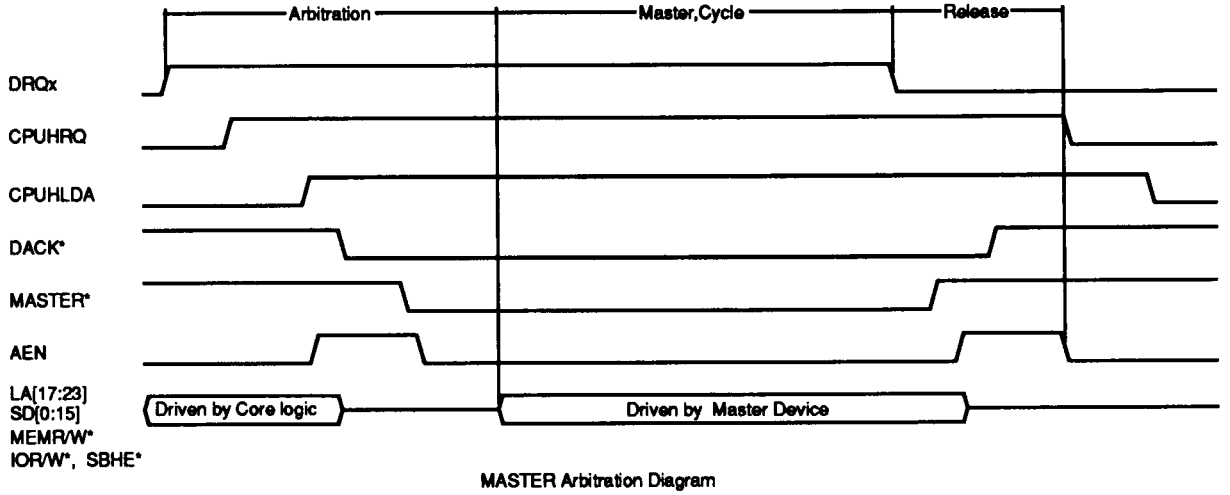
The HT18 supports DMA masters on the I/O channel. A device on an I/O channel can become master and control I/O channel operations and memory access. The MASTER* line is sampled during DMA to determine if an external bus master wishes to control the I/O channel. If the line is active, the HT18 expects that the external address buffers have reversed direction. The HT18 address lines also reverse direction (they normally drive out during DMA), so the internal memory controller can obtain the address.

The memory and I/O control signals also reverse while MASTER* is active. The following diagram shows how an add-on bus master device obtains and releases control of the system.

The HT18 will retain byte swapping responsibilities with the Master device being treated as a 16-Bit resource. The Master device should not drive the SD[0:7] and SD[8:15] in a manner that would conflict with the normal byte swapping activites being performed by the HT18.

The HT18 generates MEMCS16* or IOCS16* internally as required for DRAM and internal register accesses, but they are not driven on the bus.

The REFRESH* line is also bi-directional in the master environment. If the master holds the I/O channel more than 15us, it should initiate a refresh cycle. To accomplish this it should hold the REFRESH* line active until the HT18 refresh control circuit asserts MEMR* and brings it high again.



MASTER Arbitration Diagram

I/O Decode

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS RANGE(HEX)	SELECTED DEVICE
0	0	0	0	0	X	X	X	X	X	000 - 01F	DMA1
0	0	0	0	1	X	X	X	X	X	020 - 02F	PIC1
0	0	0	1	0	X	X	X	X	X	040 - 05F	PTC
0	0	0	1	1	0	X	X	X	0	060 - 06F	KBC, Port B
0	0	0	1	1	1	X	X	X	X	070 - 07F	RTC, NMI
0	0	1	0	0	X	X	X	X	X	080 - 08F	DMAPAGE
										090 - 091	Reserved(Rev A/B)
											Available (Rev C)
0	0	1	0	0	1	0	0	1	0	092	SYS CTRL PORT
										093-09F	Reserved (Rev A/B)
											Available (Rev C)
0	0	1	0	1	X	X	X	X	X	0A0 - 0BF	PIC2
0	0	1	1	0	X	X	X	X	X	0C0 - 0DF	DMA2
0	0	1	1	1	X	X	X	X	0	0F0 -	CLR BUSYCOP
0	0	1	1	1	X	X	X	X	1	0F1 -	RESETCOP 287
0	0	1	1	1	X	1	X	X	X	0F08- 0FF	NPCS*
0	0	1	1	1	0	1	1	X	X	1EC - 1EF	EMS/CONFIG REGISTER

60-6F is KBC if A0=0, and Port B if A0=1; 070-07F is RTC if A0=1 and NMI if A0=0

I/O Address Map

The following table defines the I/O ports supported by the HT18. Certain address locations may not be used or reserved locations. Addresses shown in numerical order.

I/0 TYPE

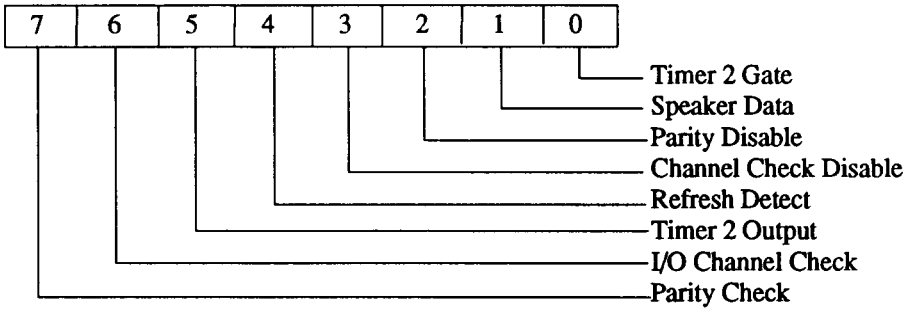
Addr Port	Read/ Write	Description
DMA Controller #1		
0000H	R/W	Channel 0 current address
0001H	R/W	Channel 0 current word count
0002H	R/W	Channel 1 current address
0003H	R/W	Channel 1 current word count
0004H	R/W	Channel 2 current address
0005H	R/W	Channel 2 current word count
0006H	R/W	Channel 3 current address
0007H	R/W	Channel 3 current word count
0008H	R/W	Command/Status Register
0009H	R/W	Request Register
000AH	R/W	Single Bit Mask Register
000BH	R/W	Mode Register
000CH	R/W	Clear Byte Pointer
000DH	R/W	Master Clear
000EH	R/W	Clear Mask Register
000FH	R/W	Write All Mask Register Bit
Programmable Interrupt Controller #1		
0020H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte
0021H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)
0023H - 003FH		Reserved
Timer/Counter		
0040H	R/W	Timer 0 Count Load/Read
0041H	R/W	Timer 1 Count Load/Read
0042H	R/W	Timer 2 Count Load/Read
0043H	W	Timer Control Word
0044H - 005FH		Reserved

Addr Port	Read/ Write	Description
Write Keyboard Controller		
0060H	R/W	Keyboard Data
0062H - 0063H		Reserved
0064H	R/W	Keyboard Control/Status
Port B		
0061H	R/W	Port B Status Port
Real Time Clock		
0070H	W	Real-Time Clock Index and NMI Mask
0071H	R/W	Real-Time Clock Data Port
DMA Page Registers		
0080H	W	Not Used
0081H	W	Channel 2 Page Register
0082H	W	Channel 3 Page Register
0083H	W	Channel 1 Page Register
0087H	W	Channel 0 Page Register
0089H	W	Channel 6 Page Register
008AH	W	Channel 7 Page Register
008BH	W	Channel 5 Page Register
System Control Port		
0090H - 0091H		Reserved
0092H	R/W	System Control Port
0093H - 009FH		Reserved
Programmable Interrupt Controller #2		
00A0H	W	ICW1
	W	OCW2
	W	OCW3
	R	Interrupt Request Register (IRR)
	R	In-Service Register (ISR)
	R	Polling Data Byte
00A1H	W	ICW2
	W	ICW3
	W	ICW4
	W	OCW1
	R	Interrupt Mask Register (IMR)

Addr Port	Read/ Write	Description
DMA Controller #2		
00C0H	R/W	Channel 0 current address
00C4H	R/W	Channel 0 current word count
00C6H	R/W	Channel 1 current address
00C8H	R/W	Channel 1 current word count
00CAH	R/W	Channel 2 current address
00CCH	R/W	Channel 2 current word count
00CEH	R/W	Channel 3 current address
00CFH	R/W	Channel 3 current word count
00D0H	R/W	Command/Status
00D2H	R/W	Request Register
00D4H	R/W	Single Bit Mask Register
00D6H	R/W	Mode Register
00D8H	R/W	Clear Byte Pointer
00DAH	R/W	Master Clear
00DCH	R/W	Clear Mask Register
00DEH	R/W	Write All Mask Register Bit
00DFH - 00EFH		Reserved
Co-processor Registers		
00F0H	W	Clear Co-processor Busy
00F1H	W	Reset Co-processor
00F8H	W	Co-processor Chip Select
00FAH	W	Co-processor Chip Select
00FCH	W	Co-processor Chip Select
EMS Page Registers and Control Registers		
01ECH	R/W	EMS Map Register
01EDH	R/W	Control Register Index Indexed 0 to 5H for CR[0:5]Rev. A/B, 0-6H [0:6]for Rev.C
01EEH	R/W	EMS Map Address Register Indexed offset 00 to 1FH for 64 EMS Pages (2 sets if 32)
01EFH	R/W	Control RegisterData Port (8-bits)

IBM™ PC AT-Compatible Registers

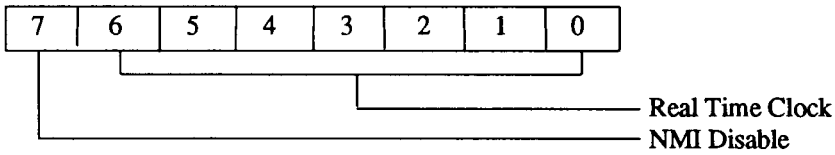
I/0 Port 61 H Port B 0061H R/W



This port controls several system level functions. The port can be accessed through any odd I/O port address between (and including) 61H and 6FH.

BIT	Description / State
7	Parity Check (read only). This bit indicates an error has occurred on the planar memory. 0 = no error occurred. 1 = an error occurred.
6	I/O Channel Check (read only). This bit indicates an I/O channel check has occurred (usually a parity error) on the system I/O channel. 0 = no error occurred. 1 = an error occurred.
5	Timer 2 Out (read only). This bit returns the condition of the timer 2 output.
4	Refresh Detect (read only). This bit toggles on each refresh cycle.
3	Channel Check Disable (read/write). This bit disables NMI generation for channel check errors. 0 = disables NMI (default). 1 = enables NMI.
2	Parity Disable (read/write). This bit is used to disable parity error contribution to the NMI. This bit is logically ORed with Parity Checking Option bit 2 of Control Register 5. With this method a system parity is disabled if either this bit (PARITY DISABLE) or Bit 2 of CR 5 is set to a logical 1. 0 = parity is enabled (default). 1 = parity is disabled.
1	Speaker Data (read/write). This bit gates the output of channel 2 of the timer/counter. 0 = output is disabled (default). 1 = output is enabled.
0	Timer 2 Gate (read/write). This bit controls operation of timer channel 2. 0 = channel 2 timer operation is disabled (default). 1 = channel 2 timer operation is enabled.

I/O Port 70 H RTC Index and NMI Mask 0070H W



RTC/CMOS Index and NMI mask - This register is used to access the RTC and its CMOS RAM.

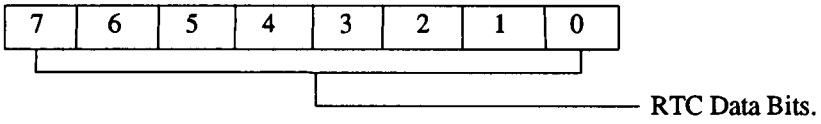
Bit 7 is an NMI Mask bit used to mask NMIs from accessing the CPU. Bits [6:0] would be used by external RTC chip. Reading this location causes RTCAS and RTCRD* signal activation. Writing will cause RTCAS and RTCWR* signal activation.

BIT Description / State

7 NMI Disable (write only). This bit disables the generation of NMIs.
0 = enables generation of NMIs (default).
1 = disables the generation of NMIs.

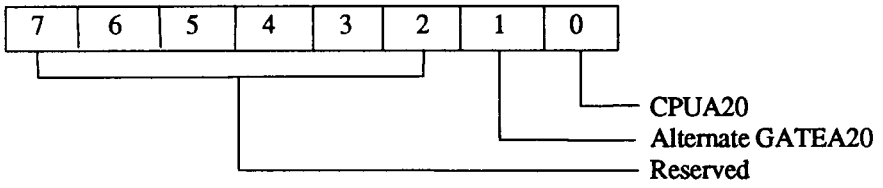
[6:0] RTC Index [6:0]. These bits are used as index pointers for external real-time clock.

I/O Port 71H RTC Data 0071H R/W



This port is used to transfer data to and from an external real-time clock. The RTC register is selected by bit [6:0] of I/O port 70H as described above. Reading this location causes RTCAS and RTCRD* signal activation. Writing will cause RTCAS and RTCWR* signal activation.

I/O Port 92H System Control Port 0092H R/W
Reset State 00H



This register is used as a faster alternative to gating A20 and resetting the CPU rather than using the 8042 keyboard controller. This register is compatible with IBM PS/2 architecture and is explained more completely in the OS/2 Optimization section.

BIT Description / State

[7:2] Reserved.

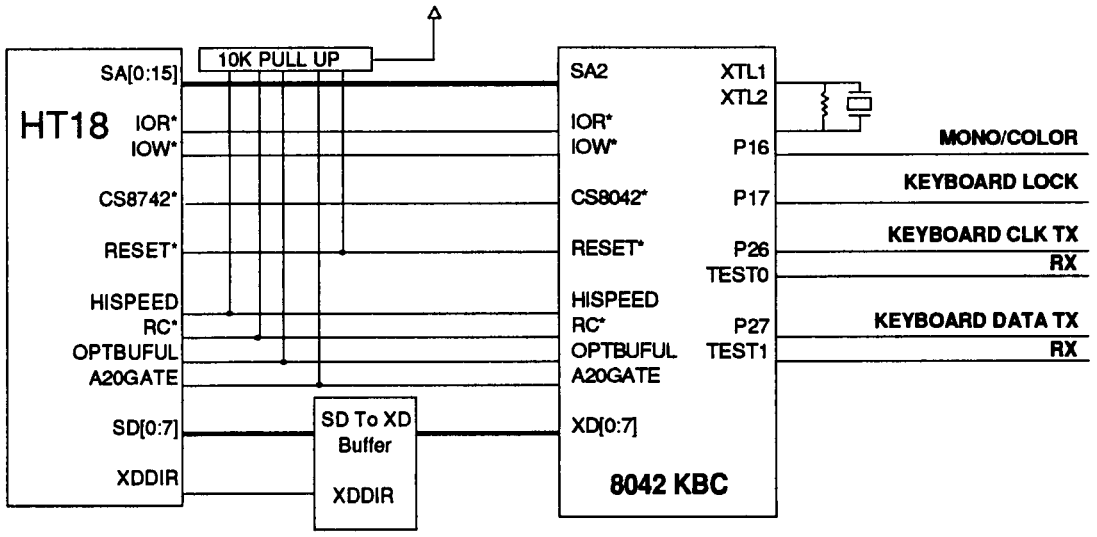
1 Alternate GATEA20.
0 = CPUA20 is forced low. (If A20 Gate Pin is low)
1 = Address bit A20 (on the CPU) goes directly to the CPUA2O pin.

0 CPUA20 RESET.
0 to 1 transition = a reset pulse is provided on the RESETCPU pin to reset the CPU. After setting, the state is maintained after a CPU reset so the BIOS can determine if the reset was caused by a CPU RESET condition.

Keyboard Controller Interface 0060H, 0062H, 0064H R/W

The HT18 uses an external 8042 to handle keyboard operations. The clock for the 8042 may be derived from SYSCLK or separate OSC circuit and should have a frequency that is between 6 MHz and 10 MHz when used with standard keyboard controllers.

The 8042 interfaces with the HT18 through OPTBUFUL (IRQ1) and a chip select line CS8042*. The 8042 also provides three output signals: HISPEED, (used for programmable speed switching) A20GATE, and RC (Reset CPU). These signals are brought into the HT18 and combined internally with Alternate Port 92 FAST GATEA20 and FAST CPU RESET functions.

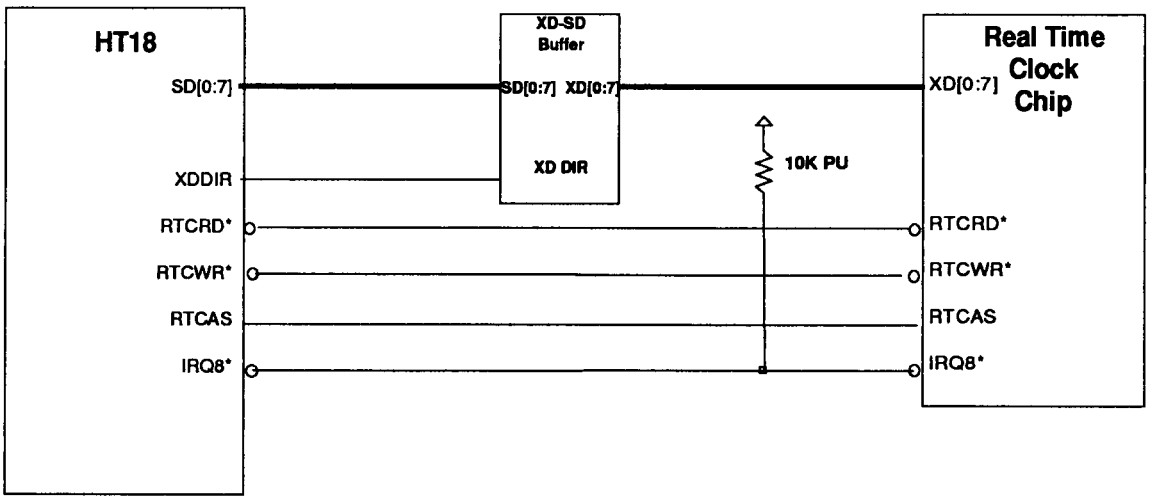


Keyboard Controller Interface

Real-time Clock Interface 0070H W 0071H R/W

The HT18 supports several types of external MC146818 compatible Real Time Clock (RTC) devices with the Standard AT type interface. This includes standard register access with the RTC index register at I/O port 70H used to latch the address of the desired register to be accessed on subsequent reads or write to data I/O port at 71H. A write access to I/O port 70H will activate the RTC Address Strobe (RTCAS) and bring the external Data DIRection (XDDIR) signal high. This combination is used to latch the address for subsequent read or write accesses to I/O port 71H.

A read from I/O port 71H will activate the RTC ReaD (RTCRD*) signal along with bringing the XDDIR signal low to read the data addressed on the previous I/O port 70H address cycle. Conversely a write to I/O port 71 will activate the RTC WRite (RTCWR*) signal and bring the XDDIR signal high to read the data addressed on the previous I/O port 70H address cycle. The use of IRQ8* interrupt request signal completes the RTC interface. This Interrupt signal is active low unlike the remaining IRQ signals. For complete register bit definitions see the standard PC-AT Register section on the I/O address map for Port 70 and 71. Refer to the actual RTC documentation for configuration and programming sequences.



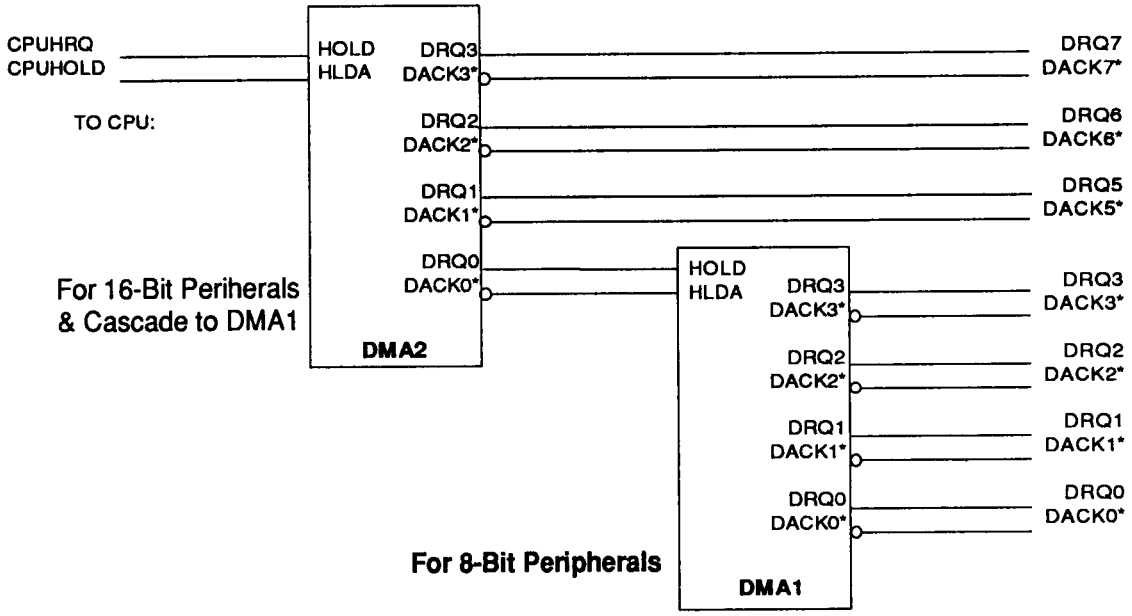
Real Time Clock Interface

DMA Controller 0000H-000FH, 00C0H, C4, C6, C8, CA, CE, CF, D0,D2, D4, D6, D8, DA, DC, 00DEH, R/W

The HT18 integrated peripheral controller contains two DMA controllers that are compatible with the Intel 8237. Each controller is a four-channel DMA device that can generate the control signals and memory addresses necessary to transfer information between a peripheral device and memory directly. These two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection for the two DMA devices.

This arrangement is used to maintain IBM PC AT bus compatibility as documented by the IEEE P996 specification. The DMA function is arbitrated with internal logic and will gain control of the local bus as an independent bus owner. To facilitate this operation the HT18 utilizes the HOLD/HLDA protocol of the microprocessor.

Figure below shows how the two DMA controllers are cascaded for standard AT bus applications. DMA channels [0:3] are used for 8-bit transfers, while channels [5:7] are used for 16-bit transfers. DMA operations are allowed within the full range of 16MB memory through the use of DMA page registers.

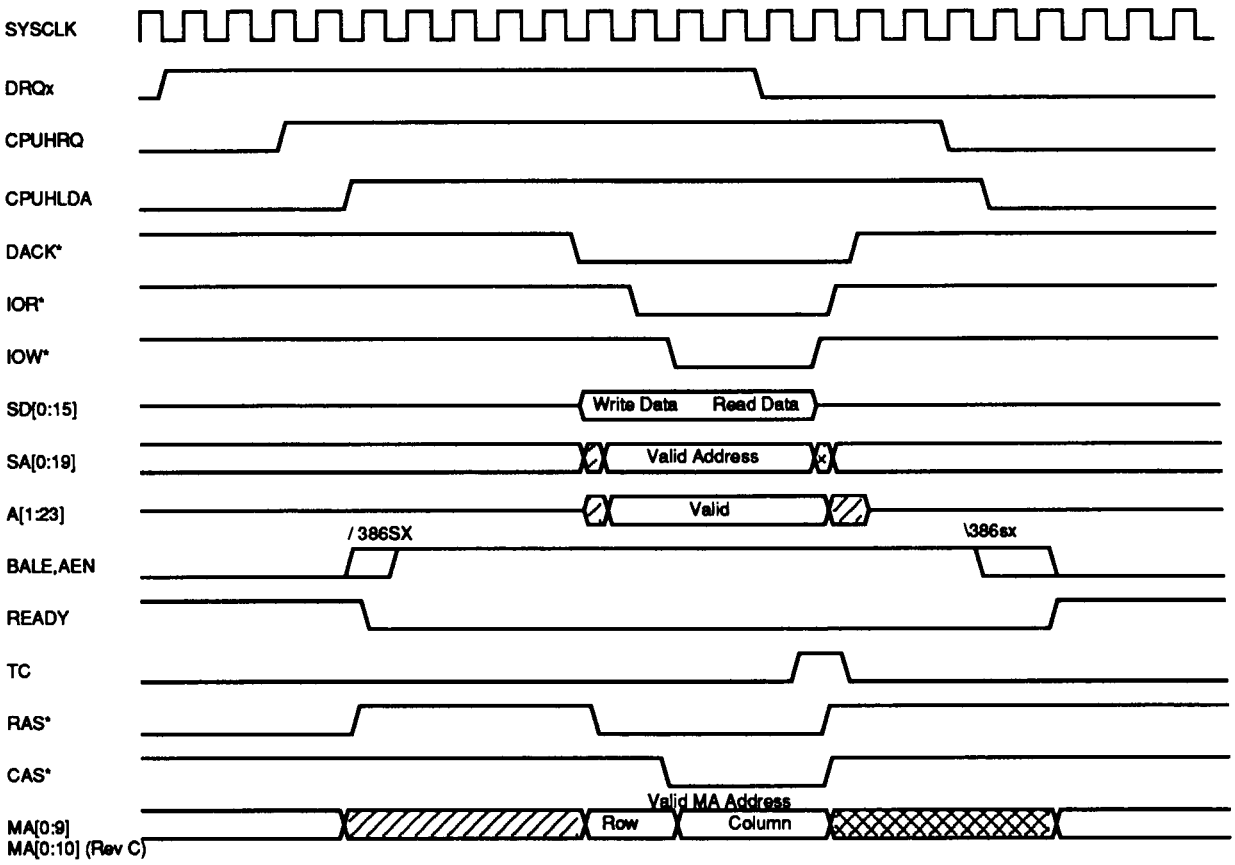


Cascaded DMA Controllers

The DMA clock (DMACLK) will be 1/4 the PROCCLK rate and controls the DMA transfer rate and timing. The PROCCLK frequency is application dependent as defined in the Clock Switching section.

During DMA cycles the PROCCLK is always CLKASN/2. DMA wait state selection is based on the AT compatible IEEE P996 bus specification defining cycle length. All DMA transfers have 1 DMA wait state unless extended by IOCHRDY.

The DMA channels have a pair of 16-bit counters and corresponding reload registers. Each 16-bit counter allows the DMA to transfer blocks as large as 65,536 words. The register associated with each counter can allow the channel to re-initialize without reprogramming. The following description of the DMA operation pertains to cascaded DMA controllers 1 and 2 unless noted otherwise.



DMA CYCLE FUNCTIONAL TIMING - Standard Memory Read or I/O Write Cycle

DMA Operation

During normal operation of the HT18, the DMA controllers are in either an Idle mode, a Program mode, or an Active mode. While in the idle mode the DMA controller state machine will stay in the idle state. This is the default mode, and the controller remains in this mode until the device has been initialized and a DMA request (DRQ) is active. If the CPU access one of the internal registers the device will enter the programming mode.

When a DMA request becomes active (DRQ[0:3],[5:7]) the controller enters the Active mode and issues a hold request that is past on to the microprocessor(CPUHRQ). The CPU responds with an acknowledge (CPUHLDA) and the HT18 sets the appropriate DMA acknowledge (DACK*[0:3],[5:7]) and generates the necessary memory addresses and command signals to accomplish a memory-to-I/O, or an I/O-to-memory transfer. During transfers between memory and I/O, data is present on the system bus from either memory or requested device and the transfer is completed in one cycle.

During transfers between memory and I/O, two commands may be active during the same cycle. On a memory-to-I/O transfer, the HT18 asserts both MEMR* and IOW* to allow data to be transferred directly to the requesting device from memory. The HT18 will not latch data from nor drive the data bus on this type of cycle. (Note: MEMR* is delayed 1 DMA Clock from 8237 timing.)

The number of clock cycles required to transfer a word of data is fixed for Standard Access Memory Cycles or optionally extended by the peripheral device utilization of IOCHRDY. During an active cycle the DMA state machine sequences through a series of states with each state being one DMA clock cycle long. The number of states in a cycle varies depending on how each device is programmed and the type of cycle to be performed. These states are labeled S[0:4] and are explained in more detail in the section called Active Mode.

Idle Mode

When no device is requesting service or the device has not been programmed, the DMA controller is in an idle mode that will maintain the state machine in the S1 state. While in this state the HT18 samples the DREQ input pins every clock cycle. The internal DMA select from the I/O decoder and HLDA are also sampled at the same time to determine if the CPU is attempting to access the internal DMA registers. When either these situations occurs, the DMA exits the idle mode. Access to the internal registers cause the controller to enter the Program mode and any other decode with in the select range or valid CPU hold acknowledge will cause it to enter the Active mode.

Program Mode

The Program mode is entered whenever HLDA is inactive and internal DMA select has been decoded. At this time the address lines A[0:3] become inputs when DMA1 is selected, or A[1:4] become inputs when DMA2 is selected. Address line A0 is not used by DMA2 as transfers are word wide instead of byte wide. These address inputs will select the DMA controller register that is to be read or written to. An internal Byte pointer flip-flop is used to supplement access to the count and address registers by selecting the high and low bytes of these registers. This flip-flop will toggle each time a read or write occurs to any of the word count or address registers in the DMA. It is cleared by a POWERGOOD reset and may be set or cleared by issuing one of the special commands outlined below and in the Special Commands section.

These Special commands are supported through the Program mode to control the individual DMA controllers. The commands do not use the data bus but are derived from a combination of I/O address decode and IOW* or IOR* access. Commands available are; Set and Clear Byte Pointer Flip-Flop; Master Clear; Clear Mode Register Counter; and Clear all Mask Registers. The access to these commands are explained in the special command section.

The HT18 will enable the programming mode when HLDA has been inactive for at least one DMA clock cycle. Systems operation must ensure that programming mode and HLDA are mutually exclusive. Otherwise the HT18 can experience erratic operation if a request for service occurs on an unmasked channel that has not been fully programmed. To prevent servicing a operation with a channel that is only partially programmed the channel should first be masked or DMA activity disabled.

Active Mode

The HT18 DMA controller will enter the Active mode when a DMA request is made on an unmasked channel or when a software request is made and the device is not in the Program mode. This will start a DMA transfer cycle. Each DMA controller can be programmed on a channel-by-channel basis to operate in one of four modes of operation. Each mode is described below.

- Single transfer operation--This mode allows the DMA channel to execute only one transfer cycle at a time. The DRQ must be held active until DACK* is activated. If DRQ is held active throughout cycle the DMA controller will release CPUHRQ and the bus once the transfer is complete. Once CPUHLDA is inactive the same DMA controller will reassert CPUHRQ and complete another cycle

on the same DMA channel unless a higher priority channel service request is received and it will be allowed to complete its cycle in the same way. In this mode, the CPU is allowed to execute at least one bus cycle between transfers and a higher priority DMA transfer will take precedence.

Following each transfer on a given channel, the word count is decrement and the address is increment or decrement. When the word count decrements from 0000H to FFFFH indicating the DMA terminal count has been reached, a terminal count bit in the status register is set and the TC output pin is pulsed high. If the automatic initialization option has been enabled, the channel will re-initializes itself. if option is not enabled the DMA controller will set the DMA request mask bit and suspend transfers on the channel.

- Block Transfer operation--When Block Transfer Mode is selected, the HT18 begins transfers in response to either a DRQ or a software request. The transfer will continue until a terminal count (FFFFH) is reached setting the status register terminal count bit and cause the TC output pin to be pulsed high. This operation mode only requires DRQ to be held active until corresponding DACK* is asserted. if the automatic initialization option has been enabled, the channel will re-initializes itself. if option is not enabled the DMA controller will set the DMA request mask bit and suspend transfers on the channel.

- Demand Transfer Operation--in Demand Transfer mode, the DMA begins transfers in response to the assertion of DRQ and continues until either terminal count is reached or DRQ becomes inactive. This mode is normally used for peripherals that have limited buffering. With this operation a peripheral can initiate a transfer and complete a cycle based on its buffer capacity. In this way the peripheral continue service by reactivating DRQ. During idle periods where terminal count has not been met, the CPU is released to operate and can monitor the status of the operation by reading intermediate values from the address and word count registers. This mode of operation allows other higher priority channels to receive service pending its own completion by reaching terminal count. This results in the TC output to be pulsed high and the setting of the appropriate terminal count bit in the status register, and auto-initialization to occur if option is set.

- Cascade Operation--This mode is used to interconnect the second DMA controller. In the Cascade operation mode, the master DMA controller does not generate address or control signals for the channel operating in this mode. Instead the DRQ and DACK* signals of the master device are used to interface the HRQ and HLDA signals of the external slave DMA devices. Once the master device has received an CPUHLDA in response to a DRQ caused by the HRQ from a slave DMA Controller, the master DMA controller ignores all inputs except CPUHLDA and DRQ on the active channel. This method prevents conflicts between the DMA devices.

DMA Transfers

Three types of transfer operations are supported in the HT18 DMA subsystem. These transfer types are:

- Read Transfer--Read transfers move data from memory to an I/O device by generating the memory address and asserting MEMR* and IOW* during the same cycle. In a read cycle for example, after receiving a DRQ, the HT18 issues an CPUHRQ to the system. Until an CPUHLDA is returned, the DMA remains in an idle state. On receiving the CPUHLDA the DMA controller exits idle on the next clock cycle and enters an arbitration state (S0) where the device resolves priority and issues DACK* on the highest priority channel requesting service. The DMA then proceeds to addressing

state (S1), where the multiplexed addresses are output and latched. In the next memory read state (S2) the HT18 asserts MEMR* and the device then transitions into the I/O write state (S3) where the IOW* command is asserted. The HT18 then remains in this state until the wait-state counter has decrement to zero and IOCHRDY is true. At least one additional I/O write state occurs unless Compressed Timing is selected. Once a ready mode (DRQ and IOCHRDY de-asserted), is detected, the DMA enters the last state (S4) where both commands are terminated. In Burst Operation Mode and Demand Operation Mode subsequent cycles begin in memory read state unless the intermediate addresses require updating. In these subsequent cycles, the lower addresses are changed in memory read state(S2).

- Write Transfer--A Write transfer moves data from an I/0 device to memory by generating the memory address and asserting IOR* and MEMW*.

- Verify Transfer--The verify transfer is a pseudo-transfer that is useful for diagnostics. in this type of transfer, the DMA operates as if it is performing a Read or Write Transfer by generating CPUHRQ, addresses, and DACK, but does so without asserting a command signal. Since no transfer actually takes place, IOCHRDY is ignored during Verify transfer cycles.

Auto-Initialization Option

Each of the Three DMA channel Mode Registers contains a bit that causes the channel to re-initialize after reaching terminal count. During this process, referred to as Auto-initialization option, the Base Address and Base Word Count Registers, which were originally written by the CPU, would be reloaded into the Current Address and Current Word Count Registers with out additional CPU intervention. The base register remains unchanged during DMA Active cycles and can only be changed by the CPU. If the channel is set to auto-initialize the request mask bit is not set upon reaching terminal count and DMA operation may continue without additional CPU intervention.

DRQ Priority

The HT18 supports two schemes for establishing DRQ priority. The first is fixed priority, which assigns priority based on channel position, in this method Channel 0 is assigned the highest priority. Priority assignment then progresses in order down through the channels, with Channel 7 receiving the lowest priority.

The second type of priority assignment is rotating priority. in this scheme the ordering of priority from Channel [0:3] is maintained but the actual assignment of priority changes. The channel most recently serviced is assigned the lowest priority and, since the order of priority assignment remains fixed, the remaining three channels rotate accordingly. The rotating priority assignment is illustrated in the following table.

First Arbitration	Second Arbitration	Third Arbitration	Priority
Channel 0	Channel 2	Channel 3	Highest
Channel 1	Channel 3	Channel 0	
Channel 2	Channel 0	Channel 1	
Channel 3	Channel 1	Channel 2	Lowest

Rotating Priority Scheme

In instances where multiple requests occur at the same time, the HT18 issues an HRQ but does not freeze the priority logic until HLDA is returned. Once HDLA becomes active, the priority logic is frozen and DACK* is asserted on the highest requesting channel. Priority is not re-evaluated until HLDA is deactivated.

Address Generation

The DMA Page Register is a set of 16 8-bit registers in the HT18 that are used to generate the high order addresses during DMA cycles. Only eight of the registers are actually used, but all sixteen are included to maintain IBM PC/AT compatibility. Each DMA channel has a register associated with it with the exception of Channel 0 of DMA2, which is used for internal cascading to DMA1. Assignment of each of these registers is shown in Table below along with its Read/Write address. For further information refer to the IBM Technical Manual.

During Demand and Block Transfers, the HT18 generates multiple sequential transfers. For most of these transfers the information in the external address latches remains the same, eliminating the need to be re-latched. Since the need to update the latches occurs only when a carry or borrow from the lower 8-bits of the Address Counter exists, the HT18 updates the latch contents only when necessary. The HT18 therefore executes S1 cycles only when necessary, resulting in an overall through-put improvement.

080H	Unused(Normally used for external diagnostic and test functions.)
081H	8-bit DMA Channel 2 (DACK2*)
082H	8-bit DMA Channel 3 (DACK3*)
083H	8-bit DMA Channel 1 (DACK1*)
084H	Unused
085H	Unused
086H	Unused
087H	8-bit DMA Channel 0 (DACK0*)
088H	Unused
089H	16-bit DMA Channel 2 (DACK6*)
08AH	16-bit DMA Channel 3 (DACK7*)
08BH	16-bit DMA Channel 1 (DACK5*)
08CH	Unused
08DH	Unused
08EH	Unused
08FH	Refresh Cycle

DMA Page Register I/O Ports

Register Descriptions

This section describes the registers used during DMA functions.

Current Address Register 0000H, 02, 04, 06, 00C0H, C6, CA, 00CEH R/W

Each DMA channel has a 16-bit Current Address Register that holds the address used during transfers. Each channel can be programmed to Increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. if Auto-Initialization is selected, this register is reloaded from the Base Address Register upon reaching terminal count in the Current Word Count Register. Channel 0 can be prevented from incrementing or decrements by setting the Address Hold Bit in the Command Register.

Current Word Count Register 0001H,03,05,07, 00C4H,C8,CC,CE,00CFH R/W

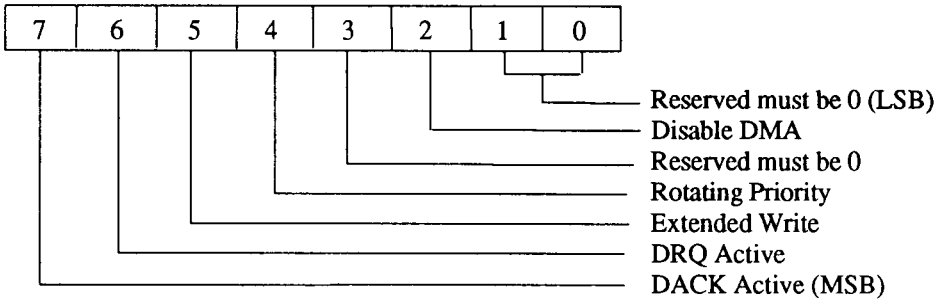
Each channel has a Current Word Count Register that determines the number of transfers to perform. The actual number of transfers performed is one greater than the value programmed into the register. The register is decrement after each transfer until it goes from zero to FFFFH. When this roll-over occurs, the HT18 generates TC, suspends operation on that channel, sets the appropriate Request Mask Bit or Auto-Initialize, and continues.

Base Word Count Register

This register preserves the initial value of the Current Word Count Register. It is also a write-only register that is loaded by writing to the Current Word Count Register. This register is loaded in the Current Word Count Register during Auto-Initialization.

Command Status Register 0008H, 00D0H R/W

This register controls the overall operation of a DMA subsystem. The register can be read or written to by the CPU and is cleared by either a RESET or a Master Clear command.



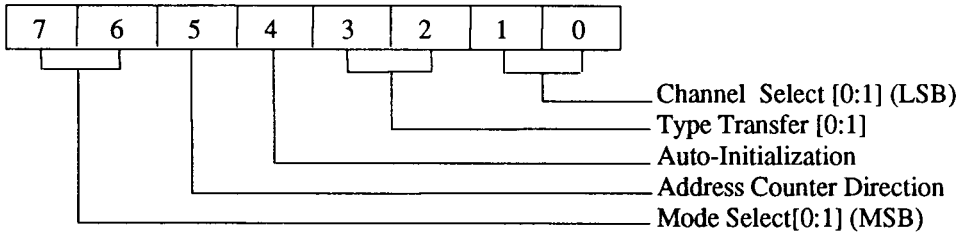
BIT	Description/State
7	DACK active level is determined by bit 7. Programming a one in this bit position makes DACK an active high signal.
6	DRQ active level is determined by bit 6. Writing a one in this bit position causes DRQ to become active low.

5	Extended Write is enabled by writing a one to bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.
4	Rotating Priority Writing a one to bit 4 causes the HT18 to utilize a rotating priority scheme for honoring DMA requests. The default mode is fixed priority.
3	Reserved must be 0.
2	Disable DMA: Bit 2 is the master disable for the DMA controller. Writing a one to this location disables the DMA subsystem (DMA1 or DMA2). This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occurring.
[1:0]	Reserved must be 0

Mode Register **000BH, 00D6H** **R/W**

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits [0:1] of the Write Mode Register command determine which channel's Mode Register is written to. The remaining six bits control the mode of the selected channel. Each channel's Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point.

During mode read operation, bits 0 and 1 are one.



BIT	Description/State
[7:6]	Mode Select 0, 1 for each channel is accomplished by bits [6:7].

M1	M0	
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

5	Address Counter Direction:Determines direction of the address counter. A one in bit 5 decrements the address after each transfer.
4	Auto-Initialization function is enabled by writing a one in bit 4 of the Mode Register.

[3:2] Transfer Type [1:0] Bits [2:3] control the type of transfer that is to be performed.

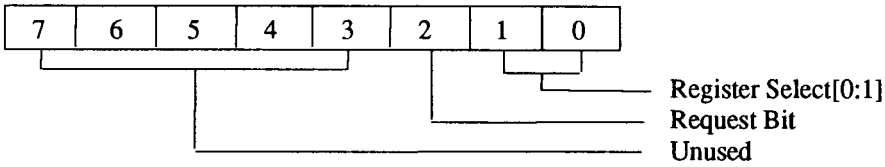
T1	T0	
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Don't use

[1:0] Channel Select [1:0] Bits [1:0] determine which channel's Mode Register is written to. Read back of a mode register results in bits [1:0] both being ones.

CS1	CS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

Request Register **0009H, 0002H** **W**

This is a four bit read register 3 bit write register used to generate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or reset independently by the CPU. The Request Mask has no effect on software generated requests. All request bits are cleared to zero by a RESET.



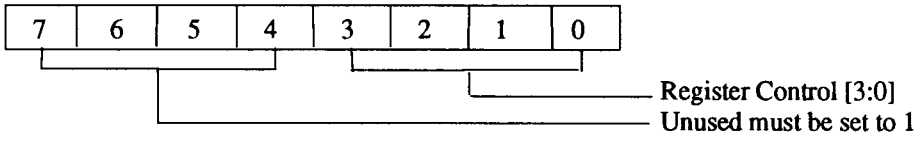
BIT Description/State

2 Request Bit is set by writing a one to bit 2.

[1:0] Register Select [1:0] determine which channel's Mode Register is written to. Read back for the mode register results in bits [0:1] both being ones.

RS1	RS0	Channel
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 select

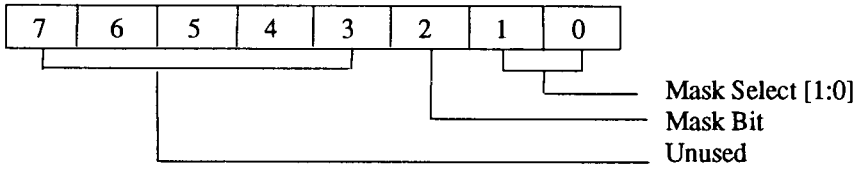
Request Register **0009H, 0002H** **R**



BIT	Description/State
[3:0]	During a Request Register Control read, the state of the request bit associated with each channel is returned in bits [0:3] of the byte. The bit position corresponds to the channel number.

Single Bit Mask Register **000AH, 00D4H** **R/W**

Each channel can be independently masked by writing to the Write Single Mask Bit location. The operation of this register is explained below.

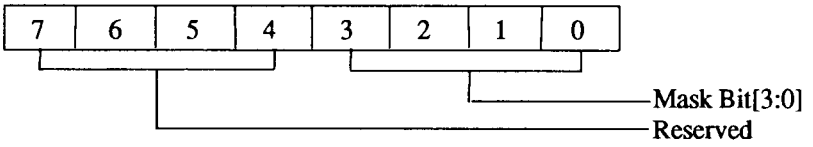


BIT	Description/State
2	Mask Bit sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a one in this bit position sets the mask, inhibiting external requests.
[1:0]	Mask Select [1:0] -These two bits select the specific mask bit that is to be set or reset.

MS1	MS0	
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 select

Write All Mask Register Bit **000FH, 00DEH** **R/W**

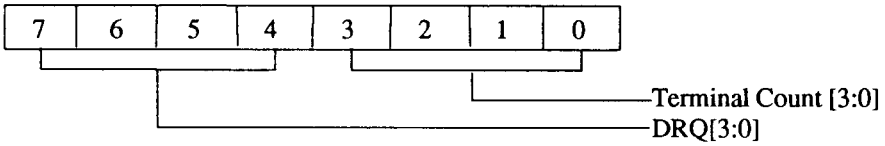
The Write All Mask Register is a set of four bits that are used to inhibit external DMA requests from generating transfer cycles. All four mask bits can be programmed in one operation by writing to the Write All Mask Bit address. The data format for this function is shown below.



Mask Bits [3:0] Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit. All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits are set as a result of terminal count being reached, if Auto-Initialize is disabled. The entire register can be cleared, enabling all four channels, by performing a Clear Mask Register operation.

Status Register **0008H** **00D0H** **R**

The status of all four channels can be determined by reading the Status Register. Information is available to determine if a channel has reached terminal count and whether an external service request is pending. Bit [3:0] of this register are cleared by a POWERGOOD reset, a Master Clear, or each time a Status Read takes place. Bits [7:4] are cleared by a POWERGOOD reset, a Master Clear, or the pending request not asserted. Bits [7:4] are not affected by the state of the Mask Register Bits. The Channel number corresponds to the bit position.



Special Commands

Five special commands are provided to make programming the device easier. These commands are activated as a result of a specific address and assertion of either an IOR* or IOW*. Information on the data lines is ignored by the HT18 whenever an IOW* activated command is issued. Thus data returned on IOR* activated command is invalid. Descriptions of the five special commands follow:

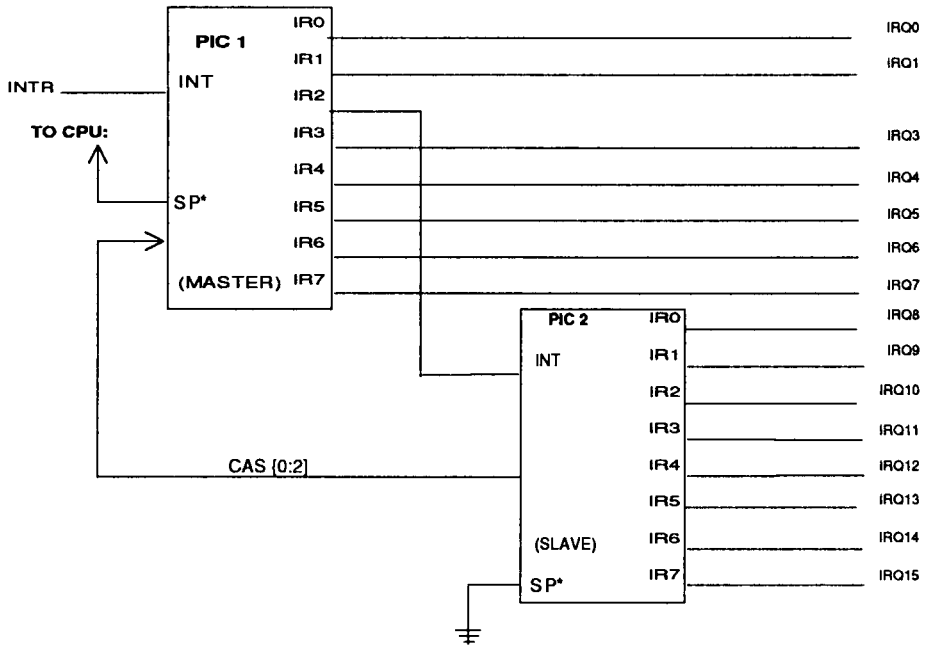
- Clear Byte Pointer Flip-Flop - This command is normally executed prior to reading or writing to the address or word count register. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.
- Set Byte Pointer Flip-Flop - Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an address or word count register.
- Master Clear - This command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter, and Byte Pointer Flip-Flop are cleared and the Request Mask Register is set. Immediately following Master Clear or RESET, the DMA is in the Idle Mode.
- Clear Request Mask Register - This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

- Clear Mode Register Counter - in order to allow access to four Mode Registers while only using one address, an additional counter is used. After clearing the counter, all four Mode Registers may be read by doing successive reads to the Read Mode Register address. The order in which the register is read is Channel 0 first and Channel 3 last.

Interrupt Controller 0020H, 0021H, 00A0H, 00A1H R/W

The HT18 incorporates two programmable interrupt controllers that are functionally compatible with the Intel 8259A. The controllers accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector that is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided, which can be changed at any time during system operation, allowing the complete interrupt subsystem to be restructured, based on the system requirements. The controllers are cascaded in a fashion compatible with the IBM PC AT and to be compatible with IEEE AT Bus Specification P996.



Cascaded Interrupt Controllers

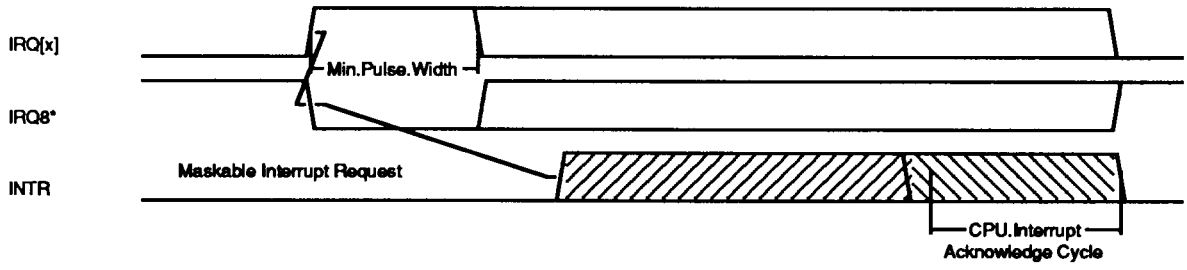
Table below shows interrupt levels used by the system board and AT compatible I/O bus.

Interrupt	System Functions	I/O Bus
NMI	Parity Check	IOCHCK
IRQ0	Timer	Not Available
IRQ1	Keyboard	Not Available
IRQ3	Serial Port 2	Available
IRQ4	Serial Port 1	Available
IRQ5	Parallel Port 2	Available
IRQ6	Floppy Disk	Available
IRQ7	Parallel Port 1	Available
IRQ8	Real-Time Clock	Not Available
IRQ9	Not Used	Available
IRQ10	Not Used	Available
IRQ11	Not Used	Available
IRQ12	Not Used	Available
IRQ13	Co-Processor	Not Available
IRQ14	Hard Disk	Available
IRQ15	Not Used	Available

Typical System Interrupts and AT compatible I/O Channel

The two devices interconnected in chained fashion with the interrupt output of Programmable Interrupt Controller 2 (PIC2) connected to interrupt input 2 on PIC1. To insure that all 16 interrupt channels operate correctly in arrangement all channels must be programmed to operate in Cascade Mode. PIC1 is located at addresses 020H-021H and is configured for Master operation (defined below) in Cascade Mode. PIC2 is a Slave device (defined below) and is located at addresses 0A0H-0A1 H. The address decoding and Cascade interconnection insures compatibility with AT compatible bus specifications.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the Counter/Timer subsystem is connected directly to the input of Channel 0 (IR0) of PIC1 and does not have an external connection. In a standard AT system implementation IRQ1 is reserved exclusively for the Keyboard output Buffer full flag. Therefore the input pin for this interrupt has been named OPTBUFUL or Output Buffer Full and should only be used as an input from the keyboard controller. IRQ8* has an inverter between the Pin and PIC (This Interrupt is committed to the Real Time Clock and this device requires an inverted sense for proper operation.)



INTERRUPT FUNCTIONAL SIGNAL TIMING - Interrupt Signal Source and Acknowledge Cycle

The following description of the Interrupt Subsystem pertains to both PIC1 and PIC2 unless otherwise noted. When register addresses are given, the address for PIC1 register is listed first, and the address for the PIC2 register is listed second, for example 020H/0A0H would indicate an 020 Hex address for PIC1 and 0A0 Hex for PIC2.

Interrupt Controller Operation

The figure on page 43 is a block diagram of the major elements in the Interrupt controller. The Interrupt Request Register (IRR) is used to store requests from all the channels that are requesting service. Interrupt Request Register bits are labeled using the Channel Name IRQ[0:7], The In-Service Register (ISR) contains all the channels that are currently being serviced (more than one channel can be in service at a time). In-Service Register bits are labeled IS[0:7]. The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels. The Priority Resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device that is compared in the Cascade Buffer/Comparitor with a three bit ID code previously written. If a match occurs in the slave controller, it generates an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during INTerrupt Acknowledge (INTA) cycles.(See Interrupt Acknowledge Cycle Timing.)

Interrupt Sequence

The HT18 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device, The indirect jump is based on a vector that is provided by the HT18 on the second of two CPU generated INTA cycles (the first INTA cycle is used for resolving priority; the second cycle is used for transferring the vector to the CPU). The events that occur during an interrupt sequence are as follows:

1 One or more of the interrupt requests (IRQ[7:0]) becomes active, setting the corresponding IRR bit(s).

2 The interrupt controller resolves priority based on the state of IRR, IMR, and ISR and asserts the INTR output if appropriate.

3 The CPU accepts the interrupt and responds with two INTA cycles.

4 During the first INTA cycle, the highest is reset. The internal Cascade address is generated and D[0:7] outputs remain three-stated.

5 The CPU executes a second INTA cycle, during which the HT18 drives an 8-bit vector onto the data pins D[0:7], which is in turn latched by the CPU. The format of this vector is shown in the following table. Note that V[3:7] in the table are programmable by writing to Initialization Control Word 2 (see Initialization Command Words section and table below.

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR6	V7	V6	V5	V4	V3	1	1	0
IR5	V7	V6	V5	V4	V3	1	0	1
SLAVE IR4	V7	V6	V5	V4	V3	1	0	0
IR3	V7	V6	V5	V4	V3	0	1	1
IR2	V7	V6	V5	V4	V3	0	1	0
IR1	V7	V6	V5	V4	V3	0	0	1
IR0	V7	V6	V5	V4	V3	0	0	0

6 At the end of the second INTA cycle, the ISR bit is cleared if the Automatic End-of-Interrupt mode is selected (see End-of-Interrupt section below). Otherwise, the ISR bit must be cleared by an End-of-Interrupt (EOI) command from the CPU at the end of the interrupt service routine.

If no interrupt request is present at the beginning of the first INTA cycle (i.e., a spurious interrupt), PIC1 issues an interrupt level 7 vector during the second INTA cycle.

End-of-Interrupt (EOI)

EOI is defined as the condition that causes an ISR bit to be reset. Determination of which ISR bit is to be reset can be done by a CPU command (specific EOI) or the Priority Resolver can be instructed to clear the highest priority 1ST bit (non-specific EOI).

The HT18 can determine the correct ISR bit to reset when operated in modes that do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in Special Mask Mode by an IMR bit, is not cleared by a non-specific EOI command. Optionally, the interrupt controller can generate an Automatic End-of-Interrupt (AEOI) on the trailing edge of the second INTA cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 has the lowest, and priority assignment is fixed (Fixed Priority Mode). Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming Operational Command Word 2 (OCW2).

Fixed Priority Mode

This is the default condition that exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown:

	Lowest							Highest
Priority	7	6	5	4	3	2	1	0

Nesting allows interrupts with higher priorities to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus, and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority interrupt that occurs during an interrupt service routine, is acknowledged only if the CPU has internally re-enabled interrupts.

Specific Rotation Mode

Specific Rotation allows the system software to re-assign priority levels by issuing a command that redefines the highest priority channel.

Before Rotation

	Lowest							Highest
Priority	7	6	5	4	3	2	1	0

(Specific Rotation cmd issued with Channel 5 specified)

After Rotation

	Lowest							Highest
Priority	5	4	3	2	1	0	7	6

Automatic Rotation Mode

In applications in which a number of equal priority peripherals are requesting interrupts, Automatic Rotation may be used to equalize the priority assignment. In this mode a peripheral, after being serv iced, is assigned the lowest priority. All peripherals connected to the controller are serv iced at least once in eight interrupt requests to the CPU from the controller. Automatic rotation occurs, if enabled, due to the occurrence of EOI (automatic or CPU generated).

Before Rotation (IR4 is highest priority request being serviced.)

ISR	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
Status Bit	0	1	0	1	0	0	0	0

	Lowest							Highest
Priority	7	6	5	4	3	2	1	0

After Rotation (IR4 service completed.)

ISR	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
Status Bit	0	1	0	0	0	0	0	0

	Lowest							Highest
Priority	4	3	2	1	0	7	6	5

Two types of commands are used to control the HT18 interrupt controllers: Initialization Command Words (ICWs) and Operational Command Words (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of four bytes to each interrupt controller. The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H / 0A0H with a one on bit 4 of the data byte. The interrupt controller interprets this as the start of the initialization sequence and does the following:

1 The Initialization Command Word Counter is reset to zero.
2 ICW1 is latched into the device.
3 Fixed Priority Mode is selected.
4 IR7 is assigned the highest priority.
5 The interrupt Mask Register is cleared.
6 The Slave Mode Address is set to seven.
7 Special Mask Mode is disabled.
8 The IRR is selected for Status Read operations.

The next three I/Os write to address 021H / 0A1H will load ICW2-ICW4. See table below for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all four bytes must be written for the controller to be properly initialized) by writing to address 020H / 0A0H with a zero in data bit 4. Note, this causes OCW2 or OCW3 to be written.

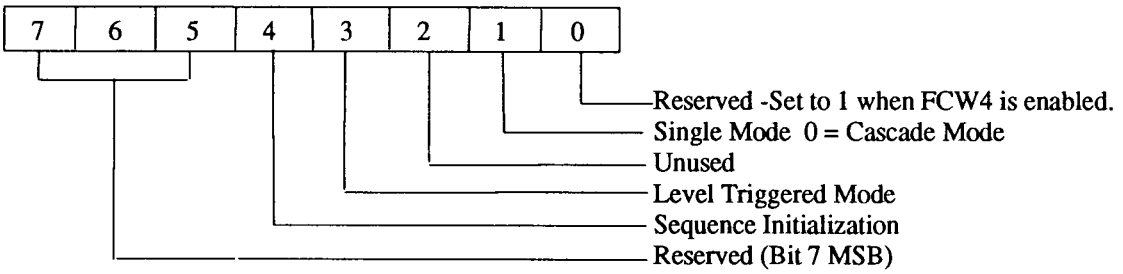
START
Write ICW1 A0 = 0 D4 = 1
Write ICW2 A0 = 1

Check CASCADE Mode?
YES - Write ICW3 A0 = 1
NO - Optionally Write ICW4

END OF INITIALIZATION Controller Ready

Initialization Sequence

ICW1 (Address 020H / 0A0H) Write Only



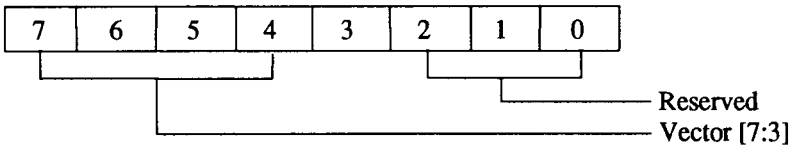
Bit

4 Sequence Initialization - indicates to the interrupt controller that an Initialization Sequence is starting and must be a one to write ICW1.

3 Level Triggered Mode - selects level or edge triggered inputs to the IRR. If a one is written to LTM, a high level on the IRR input generates an interrupt request. The IR must be active until the first INTA cycle is started to generate the proper interrupt vector (an IR7 vector is generated if the IRR input is de-asserted early), and the IR must be removed prior to EOI to prevent a second interrupt from occurring.

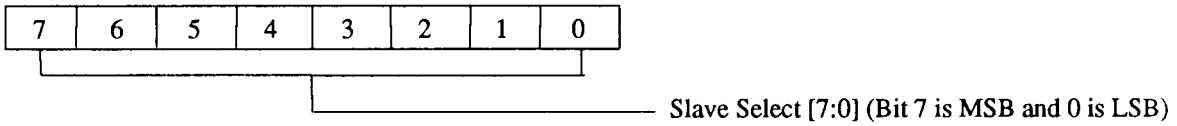
1 Single Mode - selects between Single Mode and Cascade Mode. Single Mode is used whenever only one interrupt controller (PIC1) is used and is not recommended for this device. Cascade Mode allows the two interrupt controllers to be connected through IR2 of PIC1. PIC1 allows PIC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest priority IR pending is from an PIC2 input. PIC1 and PIC2 must be programmed for Cascade Mode for both devices to operate.

ICW2 (Address O21H / 0A1H) (Write Only)



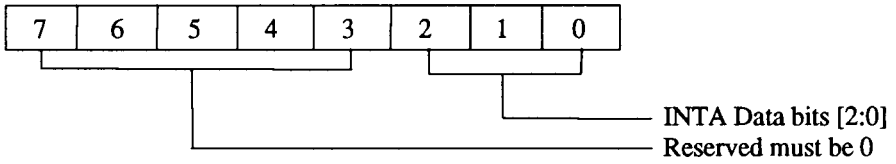
- Vector[7:3]: These bits are the upper five bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during INTA. PIC1 and PIC2 need not be programmed with the same value as ICW2.

ICW3 Format for PIC1 (Address 021H Write Only)



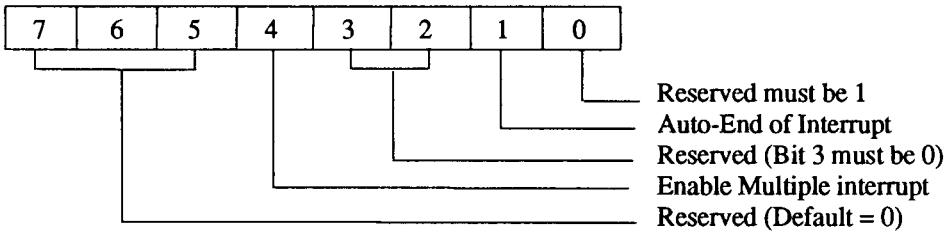
- Slave Select [7:0] Select which IR inputs have Slave Mode controllers connected. ICW3 in PIC1 must be written with 04H for PIC2 to function.

ICW3 Format PIC2 (Address 0A1H Write Only)



- INTA Data [2:0] Determine the Slave Mode address the controllers will respond to during the cascaded INTA sequence. ICW3 in PIC2 should be written with 02H for Cascade Mode operation. Note that bit [7:3] must be zero.

ICW4 (Address 021H /0A1H Write Only)



Bit

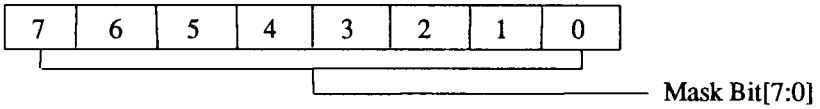
4 Enable Multiple Interrupts-Enables Multiple Interrupts from the same channel in fixed Priority Mode. This allows PIC2 to fully nest interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by PIC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to PIC2 and to check its In Service Register for zero when exiting an interrupt serv ice routine. If zero, a nonspecific EOI command should be sent to PIC1. If non-zero, no command is issued.

1 AEOI - Auto End-of-Interrupt is enabled when ICW14 is written with a zero in both. The interrupt controller performs a non-specific EOI on the trailing edge of the second INTA cycle. Note that this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.

Operational Command Words

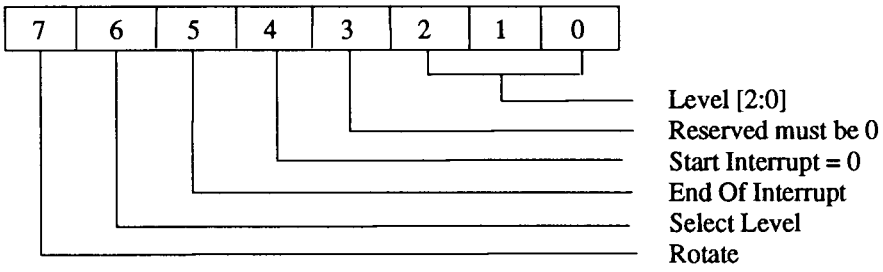
Operational Command Word One (OCW1) is located at address 021H/0A1H and may be written any time the controller is in Initialization Mode. Operational Command Words Two and Three (OCW2 and OCW3) are located at address 020H/0A0H. Writing to address 020H/0A0H with a zero in bit 4 places the controller in operational mode and loads OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1 (Address 021H / 0A1H Read/Write Register)



– Mask Bits [7:0] These bits control the state of the interrupt Mask Register. Each interrupt Request can be masked by writing a one in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no affect on lower priority requests. All IMR bits are cleared by writing ICW1.

OCW2 (Address 020H / 0A0H Write Only)



Bit

7 Rotate This bit in conjunction with Select Level and End Of Interrupt selects operational function. Writing a one in bit 7 causes one of the rotate functions to be selected.

6 Select Level - This bit in conjunction with Rotate and End Of Interrupt selects operational function. Writing a one in this bit position causes a specific or immediate function to occur. All specific commands require Level 2-0 to be valid except for no operation.

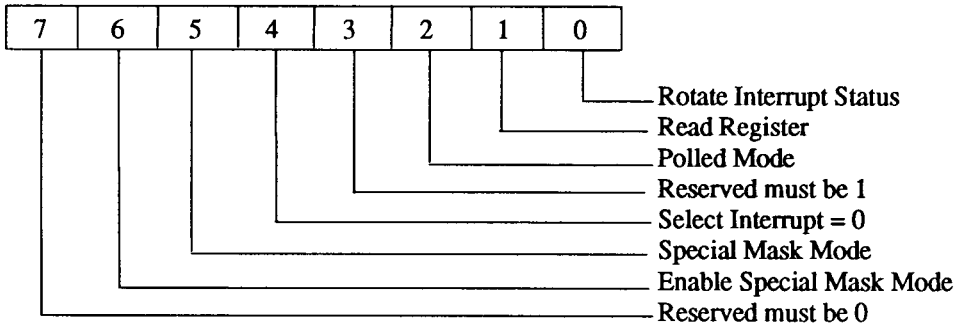
5 End Of Interrupt This bit in conjunction with Rotate and Select Level selects operational function. Writing a one in this bit position causes a function related to End of Interrupt to occur.

Rotate	Select Level	End Of Interrupt	
0	0	0	Function disabled
0	0	1	Non-Specific EOI Command
0	1	0	No Operation
0	1	1	Specific EOI Command
1	0	0	Rotate on auto EOI enable
1	0	1	Rotate on non-specific EOI
1	1	0	Specific Rotate Command
1	1	1	Rotate on Specific EOI

4 Start Interrupt Writing a zero in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

[2:0] Level[2:0] These three bits are internally decoded to select which interrupt channel is to be affected by the Specific command. Level [2:0] must be valid during three of the four specific cycles when Select Level bit is set to high.

OCW3 (Address 020H /0A0H Write Only)



Bit

6 Enable Special Mask Mode Writing a one in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5. Enable Special Mask Mode allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

5 Special Mask Mode If Enable Special Mask Mode and Special Mask Mode are written with a one, the Special Mask Mode is enabled. Writing a one to Enable Special Mask Mode and a zero to Special Mask Mode disables Special Mask Mode. During Special Mask Mode, writing a one to any bit position inhibits interrupts and a zero enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition for the ISR.

4 Select Interrupt Writing a zero in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

2 Polled Mode is enabled by writing a one to bit 2 of OCW3 causing the HT18 to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle sets bit 7 if an interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request is encoded on bits [2:0]. The IRR remains frozen until the read cycle is completed, at which time the Polled Mode bit is reset.

1 Read Register When the bit is one, reading the Status Port at address 020H/0A0H causes the contents of IRR or ISR (determined by Rotate Interrupt Status) to be placed on D[7:0]. Asserting Polled Mode forces Read Register reset.

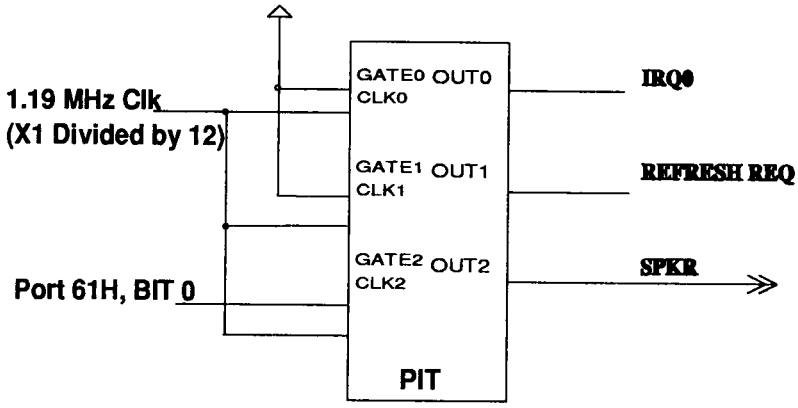
0 Rotate Interrupt Status This bit selects between the IRR and the ISR during Status Read operations if Read Register = 1 IRR is selected . ISR is selected if this bit is set to zero

Programmable Interval Timer

The HT18 intergrates a Programmable Interval Timer (PIT), which is functionally equivalent to the Intel 8254 Programmable Internal Timer/Counter. The PIT is programmable through internal I/O ports addressed at 0040H through 0043H.

The inputs of the three channels are connected to a 1.19MHz clock. The 1.19MHz clock is internally generated by dividing X1 oscilator input pin (14.31818MHz) by 12. The output of the three channels are as follows:

- Channel 0 is a general purpose and software interrupt timer. The output of this channel is connected directly to the IRQ0 pin of the internal programmable interrupt controller.
- The output of Channel 1 is used internally by the HT18 to generate refresh requests.
- The output of Channel 2 supports tone generation for the audio speaker.



Programmable Interval Timer

The Programmable Interval Timer (PIT) in the HT18 is general purpose, and can be used to generate accurate time delays under software control. The PIT contains three 16-bit counters (Counter [0:3]) that can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter.

All three of the counters are controlled from a common set of control logic. The control logic decodes control information written to the PIT and provides the controls necessary to load, read, configure, and control each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the lack of an external hardware trigger signal. Counter 2 can be operated in any of six modes listed below.

- Mode 0 - Interrupt on terminal count
- Mode 1 - Hardware re-triggerable one-shot
- Mode 2 - Rate generator
- Mode 3 - Square wave generator
- Mode 4 - Software triggered strobe
- Mode 5 - Hardware re-triggerable strobe

All three counters in the PIT are driven from a common clock input pin (X1) that is derived by dividing X1 14.31818MHz input frequency by 12. Counter zeros output (Out0) is connected to IRQ0 of PIC1 (see the Interrupt Controller Functional Description) and may be used as an interrupt to the system for time keeping and task switching. Counter 1 is programmed to generate pulses for use by the refresh generator. The third counter (Counter 2) is a full function Counter/Timer. This channel can be used as an internal timer, a counter, or as a gated rate/pulse generator. The HT18 uses this signal as SPeaKeR (SPKR) tone output on pin 76 of the device.

Counter Description

Each counter in the PIT contains a Control Register, a Status Register, a 16-bit Counting Element (CE), a pair of 8-bit Counter Input Latches (CIL and CIH), and a pair of 8-bit Counter Output Latches (COL and COH). Each counter also has a clock input for loading and decrementing the CE, a mode defined GATE input for controlling the counter (only GATE2 is controlled by I/O port 61 , bit 0), and an OUT signal. The OUT signal's state and function are controlled by the Counter Mode and condition of the CE (see Mode Definitions).

The Control Register stores the mode and command information used to control the counter. The Control Register may be loaded by writing a byte, containing a pointer to the desired counter, to the Write Control Word address (043H). The remaining bits in the byte contain the mode, the type of command, and count format information.

The Status register allows the software to monitor counter condition and read back the contents of the Control Register.

The Counting Element is a loadable 16-bit synchronous down-counter. The CE is loaded or decremented on the falling edge of TMRCLK. The CE contains the maximum count when a zero is loaded; this is equivalent to 655536 in binary operation or 10000 in BCD. The CE does not stop when it reaches zero. In Modes 2 and 3, the CE is reloaded and in all other modes it wraps around to FFFFH in binary operation or 9999 in BCD.

The CE is indirectly loaded by writing one or two bytes (optional) to the Counter Input Latches, which are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle. The CE is also read indirectly by reading the contents of the Counter Output Latches. COL and COH are transparent latches that can be read while transparent or latched (see Latch Counter Command).

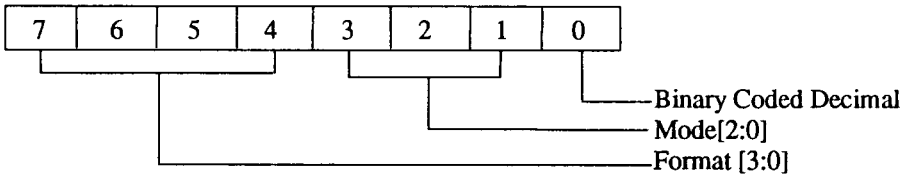
Programming the PIT

After power-up, the condition of PIT Control Registers, counter registers, CE, and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word and then an initial count. The Control Register of a counter is written to by writing to the Control Word address (see the following table). The Control Word is a write-only location.

I/O ADDR	Function
040H	Counter 0 (Read/Write)
041H	Counter 1 (Read/Write)
042H	Counter 2 (Read/Write)
043H	Counter Control (Write)

Counter Control Register (043H Write Only)



- Format [3:0] Bits [7:4] determine the command to be performed as shown in Command Table.
- Mode [2:0] Bits [3:1] determine the counter's mode during Read/Write Counter Commands (see Read/Write Counter Command) or select the counter during a Read-Back Command (see ReadBack command). Bits [3:1] become "don't care" during Latch Counter Commands.
- Binary Coded Decimal - Bit 0 selects counting format during Read/Write Counter Commands. Where bit 0 is set to zero, the count is binary 1, when bit 0 is set to one, the count is Binary Coded Decimal. Note that during Read-Back Command this bit must be zero.

Read/Write Counter Command

When writing to a counter, two conventions must be observed:

- Each counter's Control Word must be written before the initial count is written.
- Writing the initial count must follow the format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte, then most significant byte).

F3	F2	F1	FO	Command
0	0	0	0	Latch Counter 0 (Counter Latch Command)
0	0	0	1	Read/Write Counter 0 LSB Only
0	0	1	0	Read/Write Counter 0 MSB Only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (Counter Latch Command)
0	1	0	1	Read/Write Counter 1 LSB Only
0	1	1	0	Read/Write Counter 1 MSB Only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (Counter Latch Command)
1	0	0	1	Read/Write Counter 2 LSB Only
1	0	1	0	Read/Write Counter 2 MSB Only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	x	x	Read-Back Command (Counter RB Command)

Command Table

MSB = most significant byte
LSB = least significant byte

A new initial count can be written into the counter any time after programming without rewriting the Control Word, as long as the programmed format is observed.

During Read/Write Counter Commands M[2:0] are defined as follows:

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
x	1	0	Select Mode 2
x	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Latch Counter Command

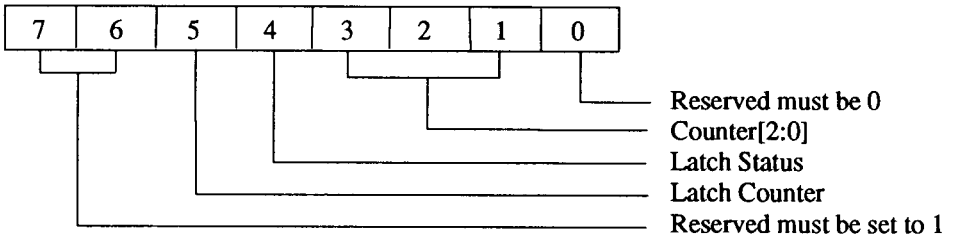
When a Latch Counter Command is issued, the counter's output latches (COL and COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition, the latches are enabled and the contents of the CE may be read directly.

Latch Counter Commands may be issued to more than one counter before reading the first counter to which the command was issued. Also, multiple Latch Counter Commands issued to the same counter.

Read-Back Command

The Read-Back Command allows the user to check the count value, mode, and state of the OUT signal and Null Count Flag of the selected counter(s).

The format of the Read-Back Command is:



Bits

5 Latch Counter - Writing a zero causes the selected counter(s) to latch the state of the CE in COL and COH.

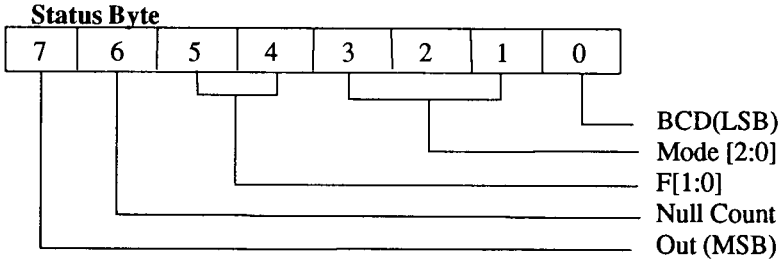
4 Latch Status - Writing a zero causes the selected counter(s) to latch the current condition of its Control Register, Null Count, and Output into the Status Register. The next read of the Counter results in the contents of the Status Register being read (see Status Read).

[3:1] Counter [2:0] Writing a one in bit 3 causes Counter 3 to latch one or both of the registers specified by LC and LS. The same is true for bits 2 and 1 except that they enable Counters 1 and 0 respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS = LC = 0, status is returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned.

Status Byte



Bit

7 OUT - contains the state of the OUT signal of the counter.

6 Null Count - contains the Null Count Flag. This flag is used to indicate that the contents of the CE are valid. Null Count is set to a one during a write to the Control Register or the counter. It is cleared to a zero whenever the counter is loaded from the counter input registers.

[5:4] F[1:0] contain the F[1:0] Command bits, which were written to the Command Register of the counter during initialization. This information is useful when determining whether the high byte, the low byte, or both must be transferred during counter read/write operations.

[3:1] Mode [2:0] These bits reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

0 BCD - indicates the CE is operating in BCD format.

Counter Operation

Due to the previously stated restrictions in Counter 0 and Counter 1, Counter 2 is used as the example in describing counter operation, but the description of Mode 0, 1, 2, 3, and 4 is relevant to all counters.

The following terms are defined for describing PIT operation.

- TMRCLK pulse - A clock equivalent to X1 input (14.31818MH2) divided by 12.

- Trigger - The rising edge of the GATE2 input.

- Counter load-The transfer of the 16-bit value in CIL and CIH to the CE.

- Initialized - A Control Word written and the Counter lnput Latches loaded.

Counter 2 operates in one of the following modes.

Mode 0 - Interrupt on Terminal Count

Writing the Control Word causes OUT2 to go low and remain low until the CE reaches zero, at which time it returns to high and remains high until a new count or Control Word is written. Counting is enabled when GATE2 = 1. Disabling the count has no effect on OUT2. The CE is loaded with the first TMRCLK pulse after the Control Word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written (see Write Operations). This TMRCLK pulse does not decrement the count (for an initial count of N, OUT2 does not go high until N + 1 TMRCLK pulses after initialization). Writing a new initial count to the counter reloads the CE on the TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2 = 0, it is still loaded on the next TMRCLK pulse but counting does not begin until GATE2 = 1. Therefore, Out2 goes high N TMRCLK pulses after GATE2 = 1.

Mode 1 - Hardware Re-Triggerable One-Shot

Writing the Control Word causes OUT2 to go high initially. Once initialized, the counter is armed and a trigger causes OUT2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches zero. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT2 is low causes the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH does not affect the current one-shot unless the counter is retriggered.

Mode 2 - Rate Generator

Mode 2 functions as a divide-by-N counter, with OUT2 as the carry. Writing the Control Word during initialization sets OUT2 high.

When the initial count is decremented to one, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE, and the process is repeated. In Mode 2, the counter continues counting (if GATE2 = 1) and generates an OUT2 pulse at the end of every N TMRCLK cycles. Note that a count of one is illegal in Mode 2.

GATE2 = 0 disables counting and forces OUT2 high immediately. A trigger reloads the CE on the TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect current operation unless a trigger is received. Otherwise, the new count is loaded at the end of the current counting cycle.

Mode 3 - Square Wave Generator

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 is 50% (high = low = N/2). For odd count values, OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N + 1)/2 and low = (N - 1)/2.

Mode 4 - Software Triggered Strobe

Writing the Control Word causes OUT2 to go initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting but has no effect on OUT2. Also, a trigger does not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later. OUT2 goes low for one TMRCLK cycle, (N+1) cycles after the initial count is written. If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be re-triggered by software.

Mode 5 - Hardware Triggered Strobe

Writing the Control Word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE 2 = 0 disables counting.

The CE is loaded during counting, the current counting sequence is not affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter re-triggerable.

GATE2

In Modes 0, 2, 3, and 4 GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3, and 5 the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop whose output is sampled on the neAt rising edge of TMRCLK. The flip-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge- and level-sensitive.

Gate Pin Function

Mode	Condition		
	Low	Rising	High
0	Disable Count	-	Enable Count
1	-	a)Initial Count b)Reset Out	-
2	a)Disable Count b)Out High	Initial Count	Enable Count
3	a)Disable Count b)Out High	Initial Count	Enable Count
4	Disable Count	-	Enable Count
5	-	Ititial Count	-

Bus Control

The HT18 internal bus controller provides all the 8-bit to 16-bit Data bus translations and is functionally similar to an 82288 bus controller device. The primary function of the bus controller section is to provide the means to impliment an AT compatible 8- or 16-bit data bus as a integral part of the overall system. To accomplish this objective this control function has been primarily designed to provide command generation and timing control for an AT compatible bus as defined in the IEEE P996 specification.

Proper adherance to this specification requires that the AT compatible bus have a maximum bus clock speed of 8 MHz. Flexible design criteria options allow the processor cycles to be run at a faster speed and switch to the lower speed during any access to the AT bus. This would be required to maintain compliance with this specification and still operate the processor at higher speeds. If a designer has more control over system I/O access, faster bus speeds can be used. The I/O channel may be programmed to select full processor speed for all I/O operations(except HOLD Acknowledge cycles which always switch to PROCCLK = CLKASN/2 speed) via bit 3 of Control Register 4. Alternately, the CLKASN frequency can be increased.

The HT18 has the following data and address buses:

Pin Symbol	Bus	Description
D[0:15]	Local Data	16-bit Bi-directional bus connecting CPU, Memory, NPU and HT18
SD[0:15]	System Data	16-bit Bi-directional bus connecting I/O slots, XD bus buffer and HT18.
SA[0:19]	System Address	20-bit Bi-directional bus connecting I/O slots and HT18.
A[0:16]	Local Address	17-bit Address bus from CPU to HT18.
A[17:23]	Local Address	7-bit Bi-directional Addresses between CPU and HT18.
MA[0:9]	Muxed Address	10-bit Muxed Addresses to local DRAM. Rev A/B
MA[0:10]	Muxed Address	11-bit Muxed Addresses to local DRAM. Rev C

Local bus arbitration is supported by use of CPU Hold ReQuest (CPUHRQ) and CPU HoLD Acknowledge (CPUHLDA) signals. In this method the CPU can relinquish control of bus for MASTER, DMA and REFRESH cycles, as shown in the respective timing diagram.

NPU Interface

The HT18 contains interface logic that supports use of an 80387SX with 80386SX microprocessor. The following timing diagram shows the NPU signal relationships that exsist when interfacing with a 387SX NPU chip.

It should be noted that the Intel NPU devices specify a maximum ratio of NPU Clock to PROCCLK that may be violated with the HT18 when the NPU operates in the asynchronous mode.. The Cyrix NPU compatible devices ignore the asyncronous Clock input. We recommend that NPU's be operated only with an syncronous Clock input.

The co-processor will monitor ADS*, READY* and CPU Address bit 23 to detect I/O operations addressed to it. It will operate a 16-Bit data resource with the following differences:

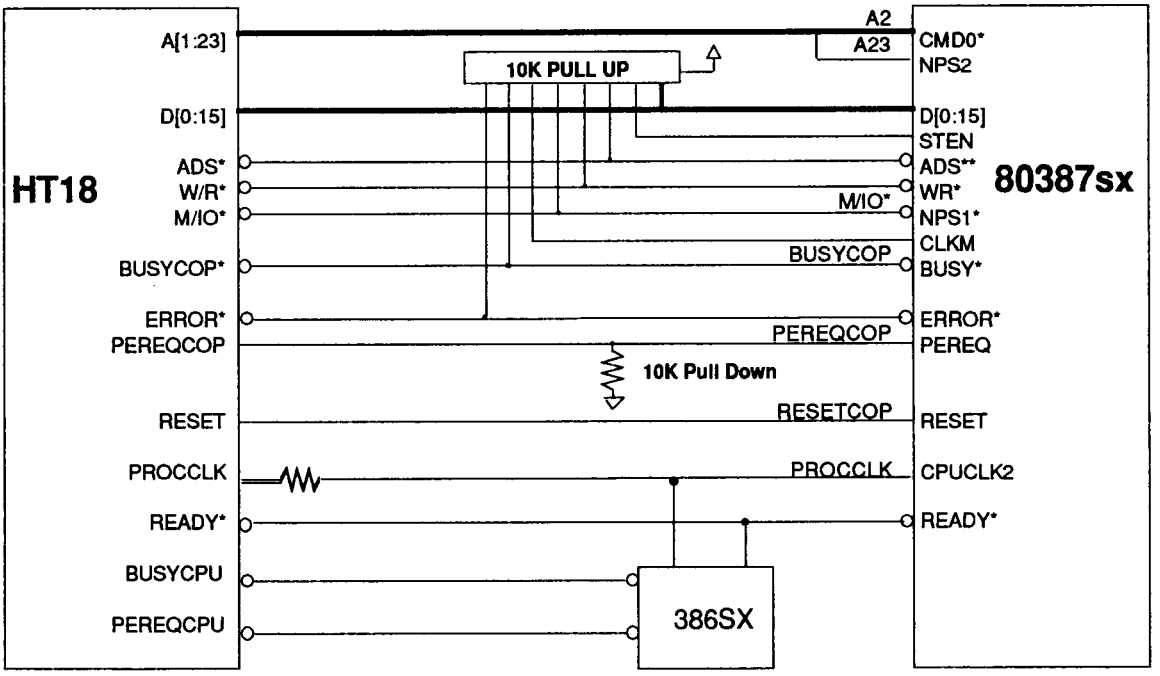
> HT18 Revision A will have NPU operations clocked with the CPU set to I/O clock speed.
> Revisions B/C NPU operations will occur at full PROCCLK speed.

The logic provides the following features:

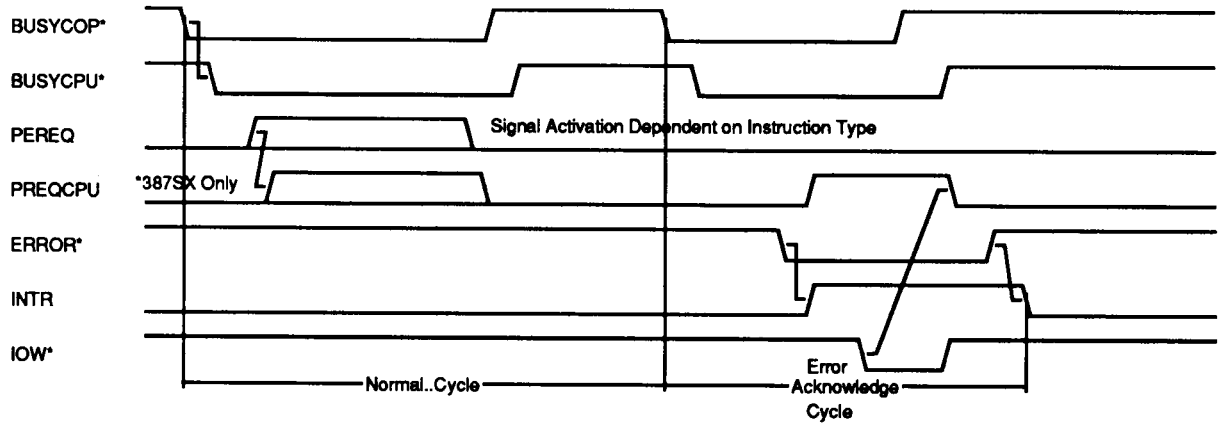
- Generates an interrupt (IRQ13) to the system when an error occurs
- Error latches BUSY state and is cleared by write to I/O Port F0h. (See I/O Address Map.)

SX Mode

- BUSY toggled by REFRESH when no 80387SX is installed.
- PEREQ is forced High on ERROR cleared by a Write to I/O Port F0h.
- Detects and latches co-processor error status



NPU Interface



NPU FUNCTIONAL TIMING DIAGRAM - NPU Bus/CPU Interface Cycles

System Control Port - Port 92H

OS/2 Optimization

OS/2 Optimization consists of two specific enhancements to the original AT design. These are the Alternate Gate A20 (Bit 1 of the Port 92H) and Alternate Hot Reset (Bit 0 of the Port 92H) features.

The Alternate Gate A20 feature is used to force address A20 to low (inactive) whenever the processor is in Real Address Mode. (This is required to insure 8086 compatibility). The CPU Reset feature is used to change the CPU from Virtual Address Mode back to Real Address Mode. A CPU reset is the only way to make this mode change.

In the original AT both of these functions were handled through the keyboard controller. The keyboard controller, however, is a very slow device. Therefore, in order to improve the performance of these features, the HT18 implements parallel circuitry that performs the same functions at a much faster speed. The new circuitry is implemented in parallel and the old circuitry is retained to ensure full AT compatibility.

These enhancements are referred to as OS/2 Optimization because these features are used by OS/2 which gains performance from the enhancement. Alternate Gate A20 is a read/write bit controlling address bit A20 when CPU is in the Real Address Mode.

1 = A20 is active
0 = A20 is inactive (if A20GATE [pin 37] is low)

This bit is set to 0 during system reset.

Alternate Hot Reset is also a read/write bit providing an alternate CPU reset function, which supports faster operation than the original implementation on the standard AT using the 8042 controller for a mode switch from the Protected Virtual Address Mode to the Real Address Mode.

This Alternate Hot Reset is used to increase system performance when switching from protected to real mode. This bit must be set to 0 either by a system reset or a write operation. When a write operation changes this bit from 0 to 1, this Alternate Hot Reset pin is pulsed high for 100 to 125 ns, the reset takes place after a minimum delay of 6.72 microseconds. After writing this bit from 0 to 1 the latch remains set to 1.

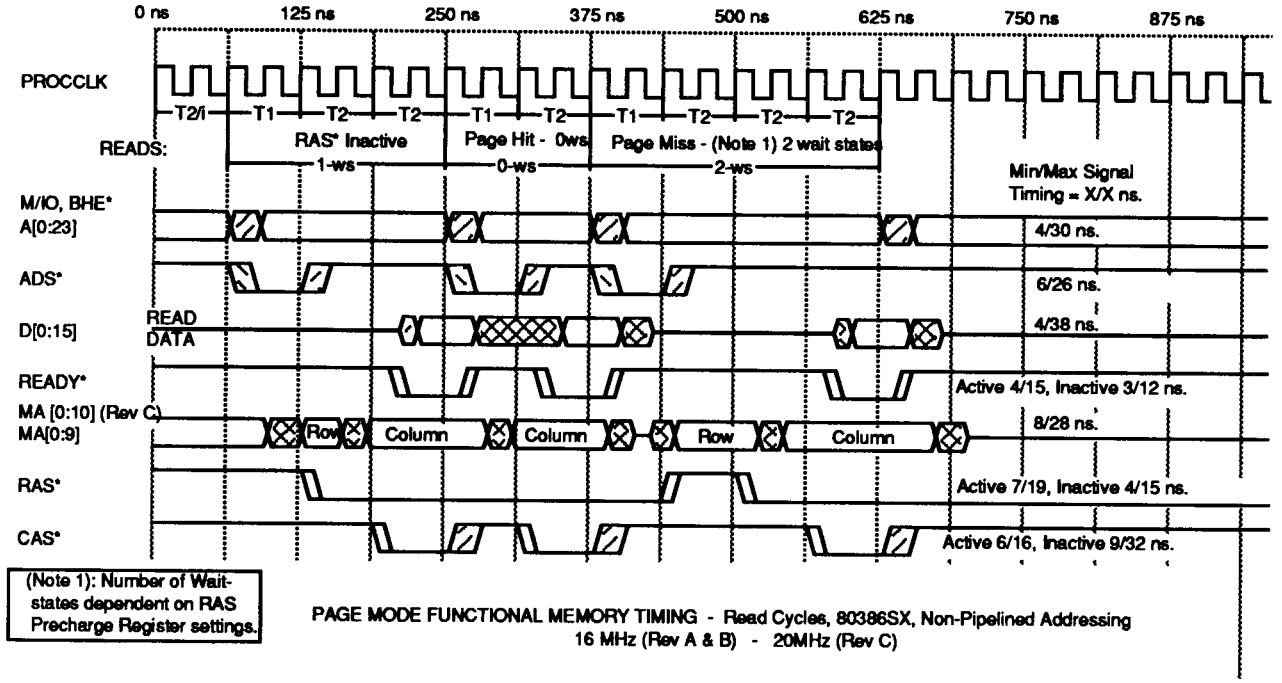
1 = Assumes a switch from the Protected Mode to Real Mode has taken place.
0 = Assumes the system was just powered on.

Memory Architecture

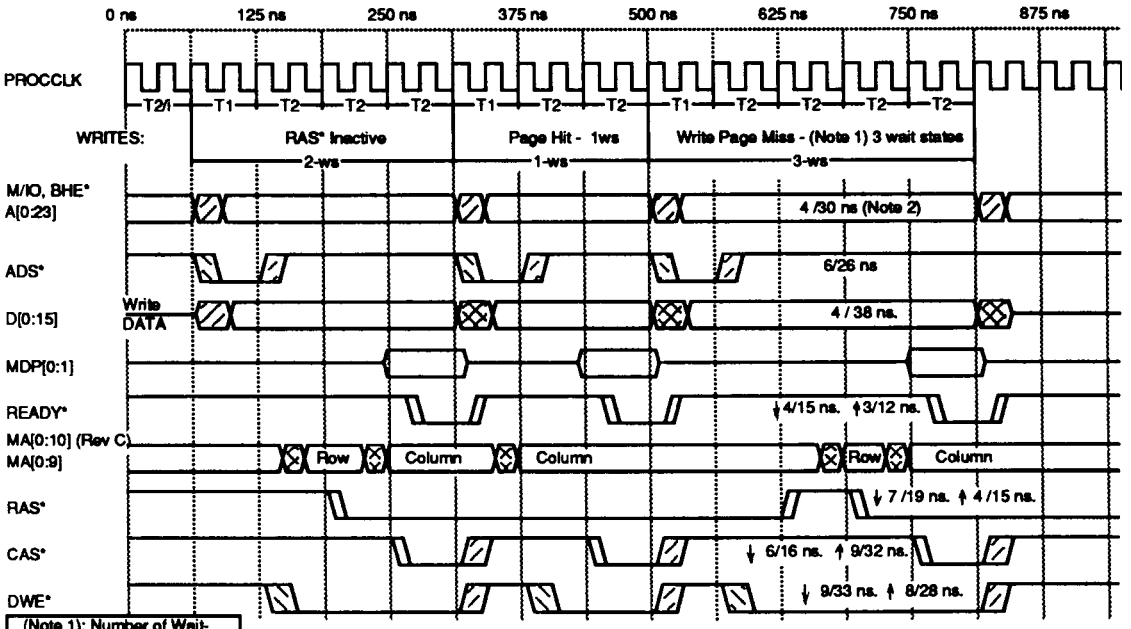
The HT18 Memory Architecture support several Memory configurations and operational modes but for the purpose of this guide, only true 0ws operation and Fast Page Mode operations will be covered. Numerous other custom configurations and modes are possible when designing with the HT18.

True 0ws operation is only possible with very fast memory devices, typically 60ns devices for 16MHz operation and sub-50ns rated devices for 20MHz and higher operation. These type devices are not available and this mode is not recommended. If this mode of operation is the primary design goal. Headland Technology has products specifically designed for this mode.

The Page Interleave mode utilizes readily available low cost memory devices operating in the Fast Page Mode. In this mode one extra processor wait state is used to enter a page boundry, (up to a 8K page) with subsequent accesses being at the fastest zero wait state memory cycles. While in this large page boundry the controller will hold several RAS* lines active and toggle the appropriate CAS* lines depending on which interleave mode is used and if access is within the same page.

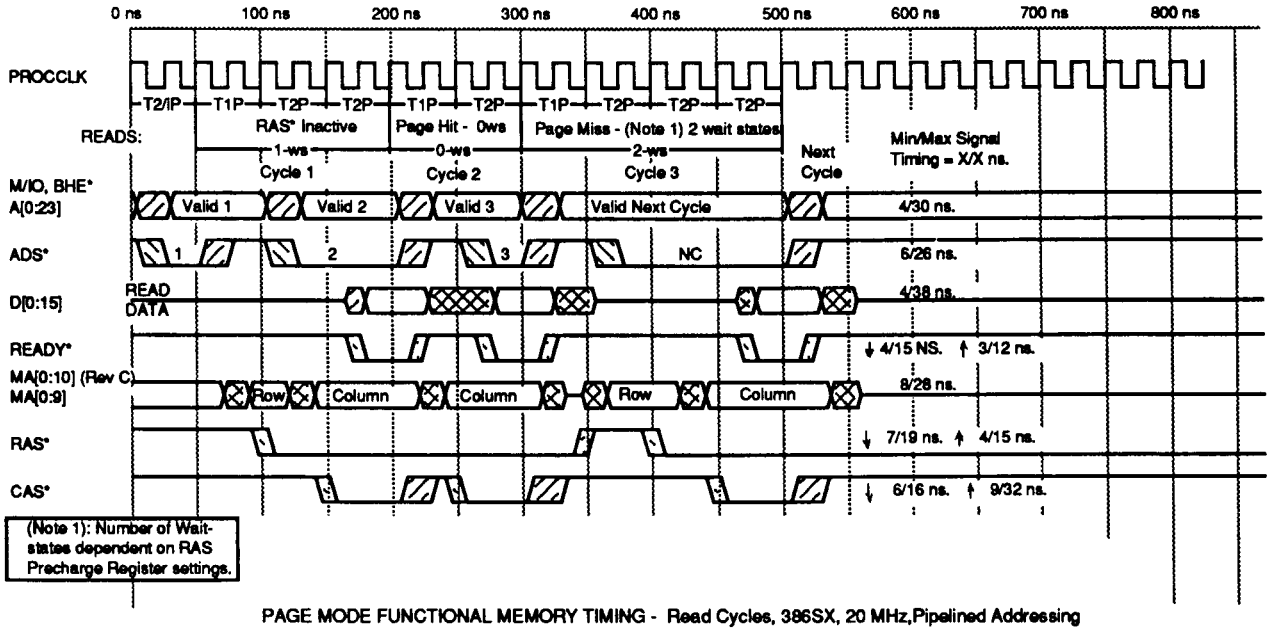


PAGE MODE FUNCTIONAL MEMORY TIMING - Read Cycles, 80386SX, Non-Pipelined Addressing
16 MHz (Rev A & B) - 20MHz (Rev C)

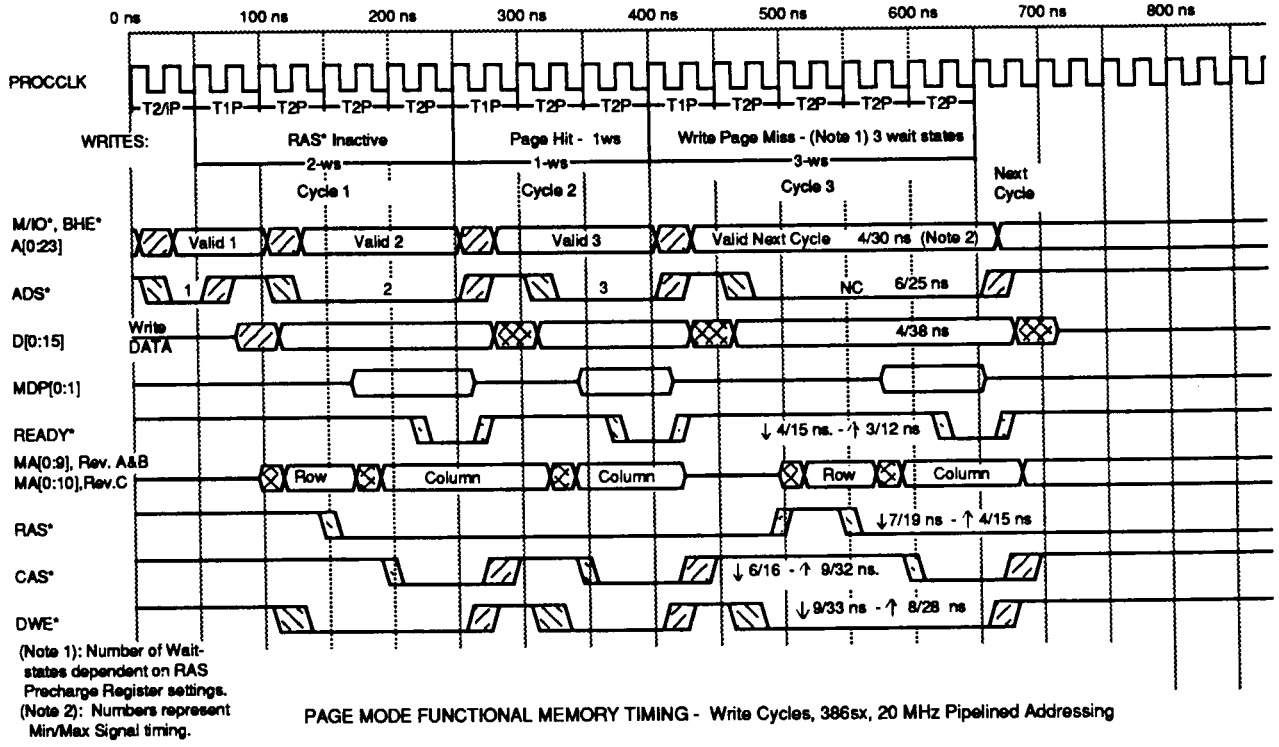


PAGE MODE FUNCTIONAL MEMORY TIMING - Write Cycles, 80386SX, Non-Pipelined Addressing
16 MHz (Rev A & B) - 20 MHz (Rev C)

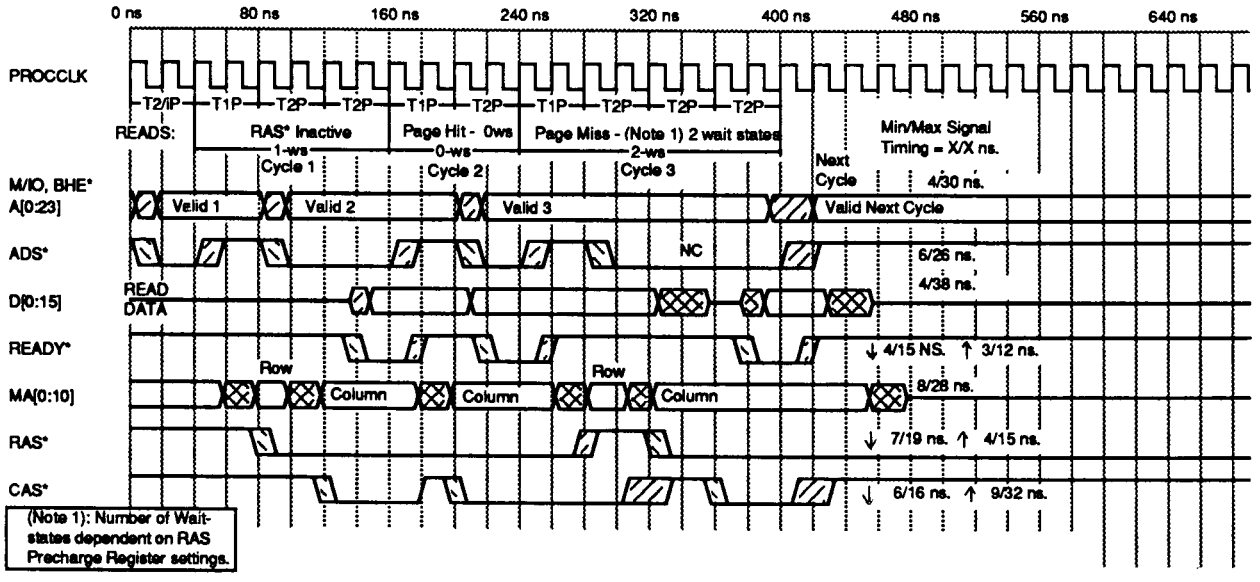
In the pineline addressing mode, the shortest possible local memory read cycle is two processor cycle states, T1P and T2P, or zero wait state access. The shortest possible pipelined write would be three processor cycle states, T1P, T2P and T2P. This extra wait state is needed for parity generation during memory writes.



PAGE MODE FUNCTIONAL MEMORY TIMING - Read Cycles, 386SX, 20 MHz,Pipelined Addressing



PAGE MODE FUNCTIONAL MEMORY TIMING - Write Cycles, 386sx, 20 MHz Pipelined Addressing



PAGE MODE FUNCTIONAL MEMORY TIMING - Read Cycles, 386SX, (Rev. C Only) 25 MHz, Pipelined Addressing

For custom applications, or to use slower memory devices the RAS* and CAS* precharge time and CAS* active times can be extended. Changing these values has the effect of adding additional processor wait states.

A Bank Switch cycle or a Page Miss cycle occurs when the memory access is outside the page boundry or in a different bank not currently active. The timing relationship is shown in the following diagram. This timing is the same for the first memory access following a REFRESH, DMA or MASTER cycle, or when a RAS time out is inserted. During certain page miss cycles such as when the same bank must be re-accessed, an additional wait state may occur to satisfy RAS* precharge timing requirements, for a total of 2 wait states. A normal page miss with the same bank being re-accessed (RAS* Active and valid) results in only a 1 wait state start cycle in order to re-establish 0ws page mode operation.

The Rev A/B has the ability to interleave 2 or 4 banks of memory operating in the fast page mode, while Rev C will interleave 2 banks even when only 3 banks are installed. In this case the first 2 banks are interleaved and access to the third bank will have an extra wait state. With 2-way interleave the RAS* signals for 2 banks stay active for all access within the page boundary each RAS* line establishes. With 4-way interleave all four RAS* signals are active and the page size is increased to its maximum size. Correspondingly, longer time is spent accessing data with in a page boundry.

Memory Controller

The HT18 Memory Controller contains three types of memory interface. These types include the ROM, DRAM and I/O Channel interface. The ROM interface supports 16-bit modes and can be placed in a shadow RAM mode where the ROM information is copied in DRAM for faster access. The DRAM interface has numerous major options such as EMS, shadow RAM, Parity, pipelined address and page mode operation. Additional minor options are defined in the DRAM interface section. An internal Linear Address Decoder controls all accesses to system memory resorces. The address locations of these resouces are defined in the Memory Address Map.

The following table indicates the memory addresses used in the HT18. For more detailed information about memory addressing, refer to the IBM PC AT Technical Reference Manual.

Address	R/W	Description
000000-09FFFFH	R/W	System RAM
0A0000-0BFFFFH	R/W	Video Memory or Shadow RAM
0C0000-0EFFFFH	R/W	BIOS extension or Shadow RAM
0E0000-0EFFFFH	R/W	Shadow RAM (RevB/C, ROM option)
0F0000-0FFFFFH	R/W	ROM or Shadow RAM
100000-FDFFFFH	R/W	Expanded or Extended Memory
FE0000-FEFFFFH	R/W	BIOS extension
FF0000-FFFFFFH	R/W	ROM

Memory Address Map

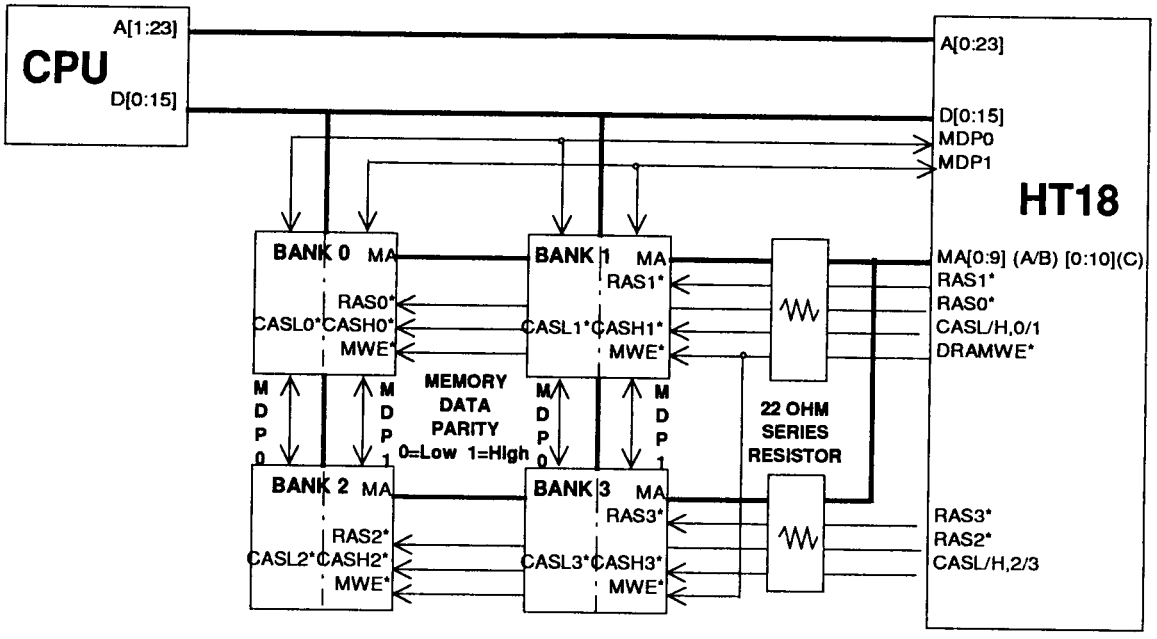
DRAM Interface

The HT18 includes a memory controller that supports up to 8MB of memory in four 16-bit (no-parity) or 18-bit (including two parity bits) banks. Maximum DRAM interface design flexibility is supported by numerious programming options configured by using 6 internal Control Registers numbered CR[0:5] (Rev A/B), or 7 internal register CR[0:6] for Rev C. Options include, mixing of 256K, 1M and 4M (18/C) DRAM in different banks, BIOS Shadow mode, Extended EMS support, Parity disable mode, special Page Interleave CAS Sharing mode, Page memory Mode and Interleave memory mode. EMS support and ROM interface are explained in their respective sections. The Rev C supports up to 20M of Memory with the additional support of 4M Devices.

To access any one of the four banks, the HT18 asserts one of the four RAS signals (RAS*[0:3]) along with one of eight CAS signals (CASL*[0:3] or CASH*[0:3]) to specify the low or high byte of the selected bank. RAS and CAS signal combinations are used for different Page and Interleave memory configurations. For write operations, the DRAMWE* signal is asserted. The HT18 multiplexes the A[1:20] address lines for DRAM accesses during assertion of RAS* and CAS* (See Address Translations tables.)

Memory is accessed on the D-bus (local bus) using Multiplexed Addresses (MA[0:9] for Rev A/B MA[0:10] for Rev C) except when the address exceeds the top of memory address value loaded in the internal Control Register 3. Memory access above this value will pass the address on to the SA bus for a bus cycle on the I/O channel. In this way additional memory can be configured on the I/O channel.

Dynamic Random Access Memory (DRAM) device selection and arrangement are application dependent but the following information should serve as a general guide.



DRAM Memory Interface

For normal PC/AT Applications full 4 Bank Memory support does not require external buffering for any memory interface signal. Series dampening resistors are suggested for increased noise immunity and a very reliable memory interface.

Local DRAM timing values can be programmed by selecting RAS and CAS timing options in Control Registers 1 and 2 (CR1/CR2). Bits 5 to 3 in CR1 is used to select RAS precharge timing. Bits 3 and 2 in CR2 define the CAS Precharge time and bits 1 and 0 define CAS active time. Remaining bits in CR1 and CR2 define Page Mode options and DRAM mix option.

CAS Sharing Mode

The CAS sharing mode is used to support special memory modules (CAS shared SIMM) where CAS lines are shared between pairs of banks. Usage of this SIMM requires the CAS sharing memory control option in the HT18 to be enabled by setting bit 1 of Control Register 5 high. Once enabled the following changes will occur.

Pairs of CAS outputs will be or'd onto common outputs.

CASL0*+CASL1*=CASL0*
CASH0*+CASH1*=CASH0*
CASL2*+CASL3*=CASL2*
CASH2*+CASH3*=CASH2*

NOTE: The unused outputs must be left open as they will retain their original timing.
In this mode RAS lines will be made mutually exclusive; which is to say that RAS0* and RAS1* will never be active simultaneously, and likewise with RAS2* and RAS3*.

WORD Interleave Mode Address Translations (Rev A/B)

		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9
Memory Type 256K (Mixed with 1M or Not)											
No Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS	A10	A11	A12	A13	T14	T15	T16	T17	T18	T20
2 Way Interleave	CAS	A10	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS	BK0	A11	A12	A13	T14	T15	T16	T17	T18	T20
4 Way Interleave	CAS	A10	A11	A3	A4	A5	A6	A7	A8	A9	T19
	RAS	BK0	BK1	A12	A13	T14	T15	T16	T17	T18	T20
Memory Type 1M (Only)											
No Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS	T19	A11	A12	A13	T14	T15	T16	T17	T18	T20
2 Way Interleave	CAS	A11	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS	BK0	T19	A12	A13	T14	T15	T16	T17	T18	T20
4 Way Interleave	CAS	A11	A12	A3	A4	A5	A6	A7	A8	A9	A10
	RAS	BK0	BK1	T19	A13	T14	T15	T16	T17	T18	T20
256K with 64K (Maximum Memory 640K)											
No Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	T17	T19
	RAS	A10	A11	A12	A13	T14	T15	T16	A9	T18	T20
Refresh											
	CAS	NO CHANGE									
	RAS:	A1	A2	A3	A4	A5	A6	A7	A0	A8	A9

Page Interleave is accomplished in a similar manner. In Page Interleave mode, only 256K and 1Meg devices are supported. 256K devices will result in a 4K Page Size and 1Meg devices will result in a 8K page size.(Rev A/B)

PAGE Interleave Mode Address Translations (Rev A/B)

		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9
Memory Type 256K(Mixed with 1M)											
No Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS	A10	A11	A12	A13	T14	T15	T16	T17	T18	T20
2 Way Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS	A10	BK0	A12	A13	T14	T15	T16	T17	T18	T20
4 Way Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19
	RAS	A10	T21	T22	A13	T14	T15	T16	T17	T18	T20
Memory Type 1 M Only											
No Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS	T19	A11	A12	A13	T14	T15	T16	T17	T18	T20
2 Way Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS	T19	BK0	A12	A13	T14	T15	T16	T17	T18	T20
4 Way Interleave	CAS	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
	RAS	T19	BK0	BK1	A13	T14	T15	T16	T17	T18	T20

The upper addresses (A[19:23]) are used to generate the RAS* signal for each bank. The A0 address line, in conjunction with BHE* signal, is used for CASL*[0:3] and CASH*[0:3] generation for high byte or low byte or word. The addresses are sourced by the CPU or DMA controller inside the HT18 or by EMS page registers inside the HT18, or by a master on the I/O channel.

PAGE Interleave Mode Address Translations (Rev C)

The Page interleave chart showing the RASA and RASB signals and address translation is shown below. In Page Interleave mode 256K, 1M, and 4M devices are supported.

Device	# of Banks Installed			
	1	2	3	4
256K	1K	2K	2K + 1K	2K + 2K
1M	2K	4K	4K + 2K	4K + 4K
4M	4K	8K	8K + 4K	8K + 8K

Interleave Mode

	I/L	RASA	RASB	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10
Memory Type 256K														
CAS	0	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19	T21
RAS				A10	A11	A12	A13	T14	T15	T16	T17	T18	T20	T22
CAS	2	A10	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	T19	T21
RAS				BK0	A11	A12	A13	T14	T15	T16	T17	T18	T20	T22
Memory Type 1 M														
CAS	0	BL0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	T21
RAS				T19	A11	A12	A13	T14	T15	T16	T17	T18	T20	T22
CAS	2	A11	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	T21
RAS				T19	BK0	A12	A13	T14	T15	T16	T17	T18	T20	T22
Memory Type 4M														
CAS	0	BK0	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
RAS				T19	T21	A12	A13	T14	T15	T16	T17	T18	T20	T22
CAS	2	A12	BK1	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
RAS				T19	T21	BK0	A13	T14	T15	T16	T17	T18	T20	T22

BK = Bank A= Address T=Translated Address

The upper addresses (A[19:23]) are used to generate the RAS* signal for each bank. The A0 address line, in conjunction with BHE* signal, is used for CASL*[0:3] and CASH*[0:3] generation for high byte or low byte or word. The addresses are sourced by the CPU, DMA controller, EMS page registers, or by a master on the I/O channel.

Memory Parity

The HT18 optionally supports even parity for each byte. Each time a byte or a word is written, an even parity bit is generated and written along with the byte. When a read occurs, the written parity bit is compared against calculated parity from the read byte. If a mismatch occurs during this read operation, a parity error is reported and an NMI is generated indicating a problem with memory. The NMI generation for parity errors can be disabled using bit 2 of internal Control Register 5 (CR5) or bit 2 of I/O port 61 H. If the Parity is not implemented bits should be disabled.

The Rev A/B allows the system designer to utilize up to four banks of memory using either 256K or 1 M DRAM. One configuration utilizing 64K devices for a 640K memory configuration is supported. Memory type and configuration selection is programmable by the use of bits 5, 6 and 7 of Control Register 0 (CR0) and bit 6 of Control Register 1 (CR1). The following table defines the valid configurations:

REGISTER BITS				DRAM TYPE for Banks					TOTAL
CR0	CR1	CR0						Interleave	MEM
D7	D6	D6	D5	1	2	3	4	Mode	SIZE
0	0	0	0	256K	None	None	None	0	512K
0	0	0	1	256K	256K	None	None	2	1M
0	0	1	0	256K	256K	256K	None	0	1.5M
0	0	1	1	256K	256K	256K	256K	4	2M
0	1	0	0	256K	64K	None	None	0	640K
0	1	0	1	256K	256K	None	None	2	1M
0	1	1	0	256K	256K	1M	None	0	3M
0	1	1	1	256K	256K	1M	1M	2	5M
1	0	0	0	1M	None	None	None	0	2M
1	0	0	1	1M	1M	None	None	2	4M
1	0	1	0	1M	1M	1M	None	0	6M
1	0	1	1	1M	1M	1M	1M	4	8M
1	1	0	0	1M	None	None	None	0	2M
1	1	0	1	1M	1M	None	None	2	4M
1	1	1	0	1M	1M	256K	None	0	4.5M
1	1	1	1	1M	1M	256K	256K	2	5M

The Rev C allows the system designer to utilize up to four banks of memory using either 256K, 1M or 4M DRAM and 25MHz CPU speed for increased speed. Memory type and configuration selection is programmable by the use of bits 5, 6 and 7 of Control Register 0 (CR0), bit 6 of Control Register 1 (CR1) and bit 0 of Control Register 6 (CR6). The following table defines the valid configurations:

REGISTER BITS					DRAM TYPE for Banks				TOTAL MEM	
CR1	CR6	CR0								
D6	D0	D7	D6	D5	1	2	3	4	SIZE	I/L
0	0	0	0	0	256K	None	None	None	512K	0
0	0	0	0	1	256K	256K	None	None	1M	2
0	0	0	1	0	256K	256K	256K	None	1.5M	2*
0	0	0	1	1	256K	256K	256K	256K	2M	2x2
0	0	1	0	0	1M	None	None	None	2M	0
0	0	1	0	1	1M	1M	None	None	4M	2
0	0	1	1	0	1M	1M	1M	None	6M	2*
0	0	1	1	1	1M	1M	1M	1M	8M	2x2
0	1	0	0	0	4M	None	None	None	8M	0
0	1	0	0	1	4M	4M	None	None	16M	2
0	1	1	0	1	1M	4M	None	None	10M	0
0	1	1	1	0	1M	4M	4M	None	18M	2
1	0	0	1	0	256K	256K	1M	None	3M	2*
1	0	0	1	1	256K	256K	1M	1M	5M	2
1	0	1	1	0	1M	1M	256K	None	4.5M	2*
1	0	1	1	1	1M	1M	256K	256K	5M	2
1	1	0	1	0	256K	256K	4M	None	9M	2*
1	1	0	1	1	256K	256K	4M	4M	17M	2
1	1	1	1	0	1M	1M	4M	None	12M	2*
1	1	1	1	1	1M	1M	4M	4M	20M	2

* Banks 1 and 2 only

Note: The HT18 supports memory mapping up to 16MB DRAM; beyond 16MB, memory is addressed by EMS mapping.

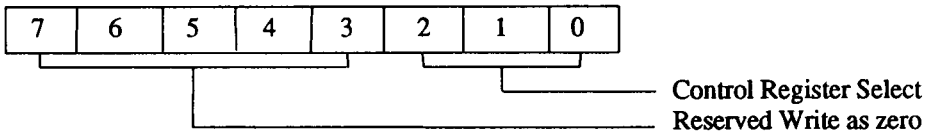
All HT18 specific operational modes and configurations are contained in the following section and accessed by first insuring the desired Control Register Index value points to the Control Register to be accessed. I/O data port accesses at hex address 1EF will display or modify the specific Control Register address contained in the Control Register Index. EMS functions are controlled with a Map Address Register with 64 indices located at I/O port register 1EE and a 10-bit (Rev A/B) 12-bit (Rev C) Map Register at I/O port 1EC.

Control Registers

PC/AT Registers not specific to the HT18 operation are contained in the explainatory text for these common peripheral controller functions.

Control Register Index **8R/W bits, at I/O 1ED (Hex)** **Reset State: 0**

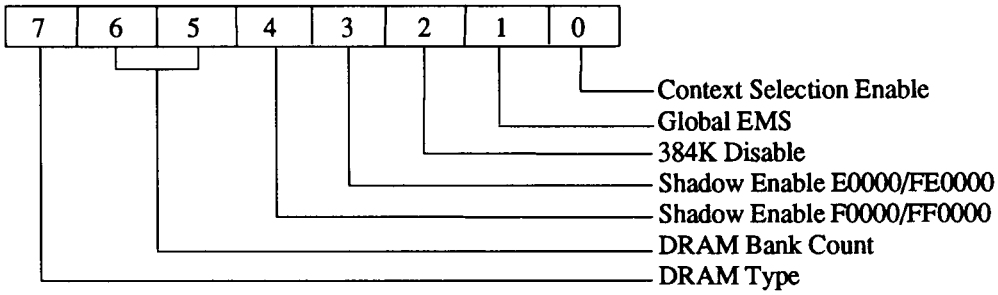
The Control Register Index is used to select which Control Register is selected on a read or write to I/O port address 01EFH. Use of this port first requires writing the Control Register Select number to the Control Register Index at I/O port 01EDH followed by the desired access to Control Register I/O port at 01EFH. The binary values for CR Index is defined below.



D[2:0]: Control Register Select:

D2	D1	D0	
0	0	0	Control Register 0
0	0	1	Control Register 1
0	1	0	Control Register 2
0	1	1	Control Register 3
1	0	0	Control Register 4
1	0	1	Control Register 5
1	1	0	Control Register 6 (Rev C Only)

Control Register 0 **8 R/W bits, Data Port 1EFH** **Reset State: all 0's**



D7 DRAM Type

1 = 1M DRAMs

0 = 256K DRAMs (default) (Rev C) 4 M DRAMs

D[6:5] DRAM Bank-count

This register is used to program the number of banks installed under BIOS control.

D6	D5	RAM Banks Enabled	Interleave Mode Rev A/B	Interleave Mode Rev C
0	0	1	0	0
0	1	2	2	2
1	0	3	0	2-Way Interleave on lower 2 banks
1	1	4	4	2 Two-way interleaves

D4 Shadow Enable F0000 and FF0000

1 = Shadow Disable

0 = Shadow Enable

64K page of DRAM that would have been located from F0000 to FFFFF in ROM is now enabled between 0F0000 to 0FFFFF and is duplicated at FF0000 to FFFFFF. The ROM chip select will now be disabled. Data should be written to this DRAM before enabling this bit.

Note: DRAM is write protected in this Range and is READ only.

D3 Shadow Enable E0000 and FE0000

1 = Shadow Disable

0 = Shadow Enable

The 64K page of DRAM that would have been located from E0000 to EFFFF in ROM is now enabled between 0E0000 and 0EFFFF and is duplicated at FE0000 to FEFFFF. The ROM chip select will now be disabled. Data should be written to this DRAM before enabling this bit.

Note: DRAM is write protected in this Range and is READ only.

D2 384K Memory Relocation

1= Disables the extra 384K and usable as shadow RAM or as EMS.

0 = Enables 384K, Normally this address range, located between A0000 and FFFFFh is relocated above the 1M border. This preserves the lower addresses for system use.

D1 Global EMS

1= EMS Enabled. You must initialize the EMS registers before D1 is set high.

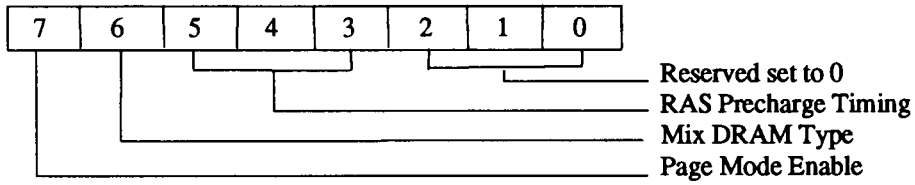
0 = EMS Disabled

D0 EMS Context Selection

1 = Alternate context. This bit operates in the same manner as bit D5 of Map Address Register 1EE except this determination of context is used during Memory cycles.

0 = Standard context is selected

Control Register 1 **8 R/W bits at I/O address 1EF (Hex)** **Reset State: 0**



D7 Page Mode Enable

1 = Page mode enabled, uses page mode memory timing except during DMA and bus master

0 = Page mode disabled, uses normal read/write timing for normal memory access

D6 Mix Dram Type Mode Register

1 = Selected type for first 2 banks, other type for last two banks

Special CASE when 256K DRAMs selected and only 1 bank is selected. The use of 256K DRAMs in the first bank and 64K DRAMs in the second bank is allowed for a total of 640K RAM. Extra 384K must be disabled.(Rev A/B only)

0 = Same type all four banks

D[5:3] RAS Precharge Timing

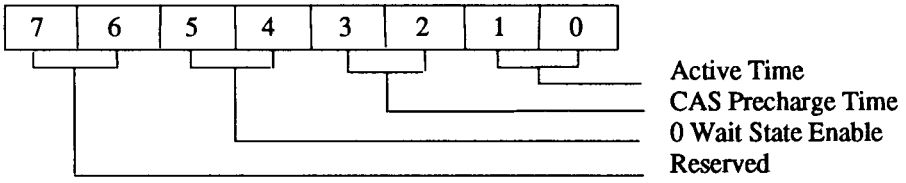
D5	D4	D3	PROCCLK Cycles
0	0	0	16
0	0	1	14
0	1	0	12
0	1	1	10
1	0	0	8
1	0	1	6
1	1	0	4
1	1	1	2

These bits determine the RAS precharge time for page mode cycles when there is a page miss access to a bank.

D[2:0] RAS Active Time Out (Rev C) (Rev A/B Reserved, must be set to 0)

D2	D1	D0	Time(uSec)
1	1	1	200
1	1	0	150
1	0	1	120
1	0	0	100
0	1	1	80
0	1	0	60
0	0	1	30
0	0	0	10

Control Register 2 **8 R/W bits, at I/O address 1EF (Hex)** **Reset State: 0**



Values are adjustable to provide values for almost all DRAMs at any speed and configuration. All timing is based on a fixed PROCCLK signal. If changes are made to the PROCCLK signal, adjustments may be required to this register to compensate. DD Hex is the recommended value for 80386SX 0-wait state operation. C8 Hex should be used for 1-wait state 386SX systems.

D[7:6] Reserved must be set to 1 in order to execute operations properly.

D[5:4] 0 Wait State Enable

CR1	CR2		
D7	D5	D4	
1	x	0	Page Mode operation with 1 Wait State when Page Hit(1)
1	x	1	Page Mode operation with 0 Wait State when Page Hit
0	1	x	Non-page mode operation with 0 Wait State memory operation
0	0	x	Non-page mode operation with 1 Wait State Memory Operation

D[3:2] CAS Precharge Time(2)

D3	D2	PROCCLK Cycles	Configuration	
1	0	2	C8	1ws
1	1	1	DD, CC	0ws, 1ws

D[1:0] CAS Active Time(2)

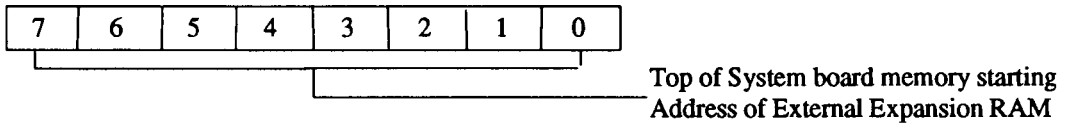
D1	D0	PROCCLK Cycles	Configuration	
0	0	4	C8, CC	1ws
0	1	3	DD	0ws

Note:

(1) Valid only when CR1 Bit 7 is set to 1.

(2) CAS active cycles plus CAS precharge must total 4 or less for 0 wait states and 6 or less for 1 wait state. Bits D[3:0] have no effect when page mode is disabled - CR1 Bit 7.

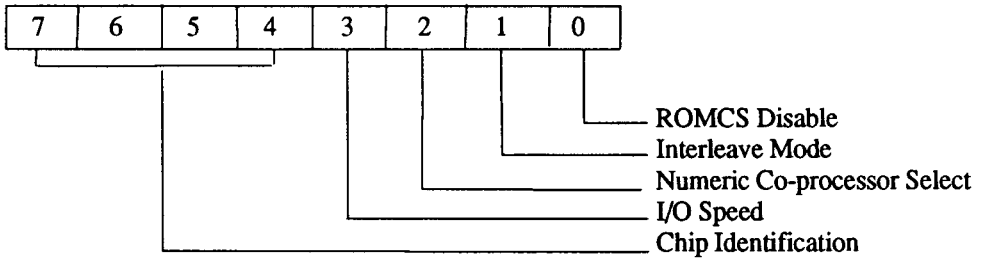
Control Register 3 **8 R/W bits at I/O address 1EF (Hex)** **Default Memory Size (A[23:16])**



D[7:0] Starting Addr of External Expansion Ram

From 0 to 255 numbers of 64K segments before expansion memory should be decoded. For example 0 would indicate that all system board RAM should be disabled for all but EMS and shadow. After RESET* will be 0.

Control Register 4 **8 R/W Bits at I/O address 1EF (Hex)** **Reset State: 0**



D[7:4] Chip ID 0001 For Rev. A
0010 For Rev. B
1000 For Rev. C

D3 I/O Speed
0 = PROCCLK is CLKASN/2 for all I/O and non-local DRAM cycles to accomodate I/O memory, peripherals (Default)(All AT bus cycle)
1 = Full speed For all cycles PROCCLK is CLKX2 except DMA*.

D2 Numeric Co-processor Select
0 = Numeric Co-processor does not exist (default)
1 = Numeric Co-processor exists

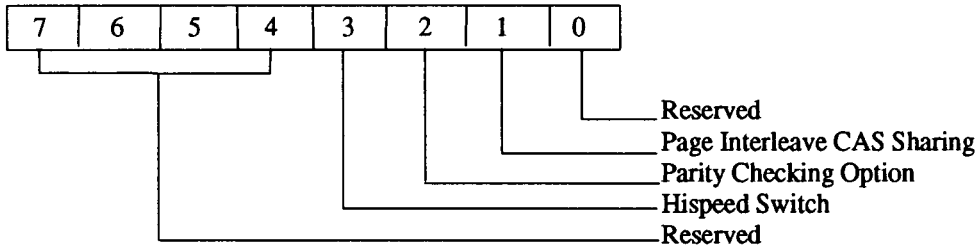
D1 Interleave Mode (Re.v A/B)
0 = Word Interleave
1 = Page Interleave

Time-Out Enable (Rev. C)
0 = Defeat RAS Time-out
1 = Enable RAS Time-out

D0: ROM Chip Select Disable (Rev A must be set to 0)
0 = ROMCS Enabled E0000-FFFFF (Rev B/C)
1= ROM Chip Select disabled E0000 to EFFFF (Rev B/C)

*NOTE: DMA cycles always run at slow speed (PROCCLK is CLKASN/2) for Rev A/B.
Rev C: DMA cycles run at high speed with I/O full speed enabled.

Control Register 5 **8 R/W bits at I/O address 1EF (Hex)** **Reset State: 0**



D[7:4] Reserved Must be 0

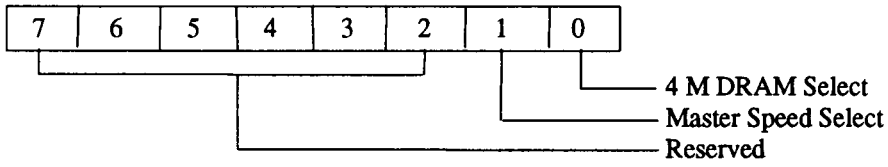
D3 Hispeed Switch
1= Enable switch to Hispeed on idle (Rev B/C)

D2 Parity Checking Option
0 = Normal (default)
1 = Parity Checking Disabled

D1 Page Interleave CAS Sharing
0 = Normal (default)
1 = Page Interleave CAS Sharing Mode Enabled

D0 Reserved

Control Register 6 (Rev C) **8 R/W bits at I/O address 1EF(Hex)** **Reset State 0**



D1 Master Speed Select
0 = PROCCLK runs at low speed in master mode
1 = PROCCLK runs at high speed in master mode

D0 4M DRAM Select
0 = No 4M DRAMs
1 = 4M DRAMs in any bank

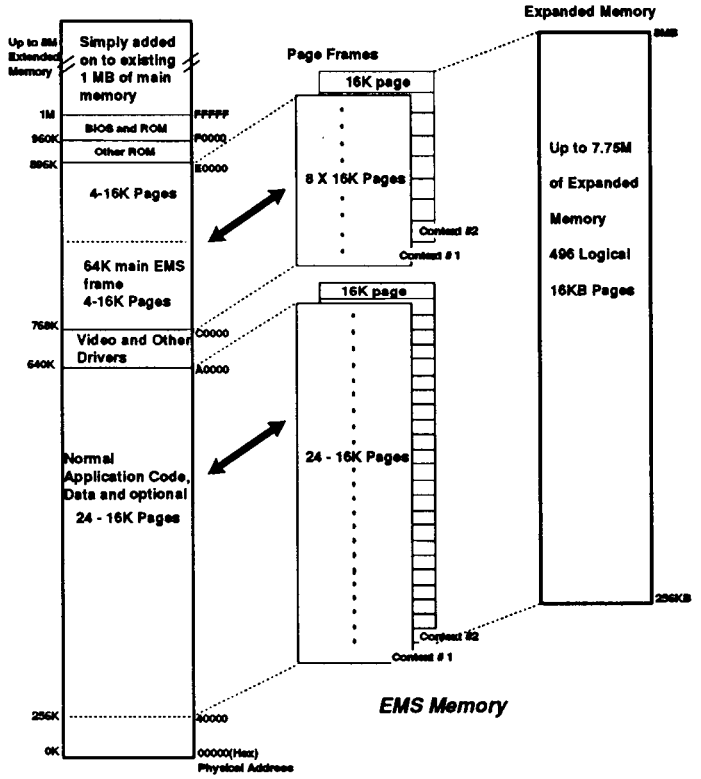
Extended Memory

The HT 18 can support a combination of extended and expanded memory as well as expansion memory that is located on the I/O bus. Extended memory is any memory at a physical address above 1MB that has not been configured for EMS use and is below the expansion memory address placed in Control Register 3 (CR3). The value in this register should indicate the top of total physical memory on the system board that would be available as extended memory. For example a 10H value in CR3 would cause all physical memory accesses above 1MB to be passed on to the I/O bus. This would cause all system board RAM above 1MB to be reserved for EMS and Shadow RAM options.

EMS - Expanded Memory

The HT18 has built in EMS hardware support the LIM 4.0 specification. This hardware provides EMS software drivers with a more efficient page mapping scheme in accessing memory greater than the DOS 1 MB limitation. Once the internal EMS re-map option has been configured and under EMS driver control operating systems and applications software have access to two sets of 32, 16KB EMS pages (or two EMS Page Frames 64K to 512K in size).

A built in EMS Auto-Increment feature provides the capability to rapidly configure multiple contexts or two sets of 32 registers associated with the configuration for each available EMS page (referred as standard and alternate context). This feature can particularly effective with advanced multi-tasking requirements. Both application software or an EMS driver can take advantage of these advanced EMS features in allowing applications programs to access more memory than allowed by DOS. The dual Context option allows more programming flexiblity and can make switching between multiple programs almost instantaneous. More information on software implementation can be found in the HT21 Programming Application Note as well as various Lotus™, Intel™ and Microsoft™ publications.



On power up the EMS function is disabled, all the DRAM addresses are left as standard linear addressing mode; ie. without any EMS address translations. Implementation and configuration of all EMS functions can be controlled in software and are accessed by registers defined in the EMS Register Summary section. Major EMS options includ EMS Bank selection, Individual Map Enable and address translation functions are accessed by the Map Register. Additional programming options are accessed by the Map Address Register and Control Registers.

Both sets of the 32 EMS page frames are physically mapped into the address space from 256KB to 640KB (040000H - 09FFFFH) and from 768KB to 896KB (0C0000H - 0DFFFFH). These are the physical addresses at which the EMS page frames will appear. The EMS page register will define the physical to logical address translation of address bits A[20:14]. In this way a physical address location below 1MB will automatically result in an access to a logical address location that can be above the 1MB DOS limitation. A standard EMS page requires 64KB of contiguous program memory and would require four 16KB pages.

EMS Register Summary

The following is a short summary of the EMS Register functionally. For more detailed information see Application Note 756-0068 for details of programming the HT18.

The HT18 EMS Hardware Support functions are configured and controlled by the use of four Read/Write registers, all accessed via I/O operations. These registers are the Map Register (MR), Map Address Register (MAR), Control Registers Index (CRI), and Control Register 0 (CR0). The Map Register is 10 bits wide(Rev A/B) 12 bits wide (Rev C) and requires I/O word accesses. This register is used to define 64 seperate EMS I/O Page Registers that can be used to re-map two sets of memory using 32 16KB EMS pages. Addressing for this Map Register is provided by the Map Address Register. Control Register 0 is used to enable the EMS option and select standard or alternate context. To access this Control Register it must first be selected by the use of the Control Register Index. The I/O address for these Registers are shown below.

I/O Address	Width	Index	Description
01EE H	8 Bit		Map Address Register(MAR)
		00-3FH	64 16KB Page Addresses
01EC H	10 Bit		Map Register(MR)
01ED H	8 Bit		Control Register Index(CRI)
		00 H	Control Register 0 Select(CR0)
		01 H	Control Register 1 Select(CR1)
		02 H	Control Register 2 Select(CR2)
		03 H	Control Register 3 Select(CR3)
		04 H	Control Register 4 Select(CR4)
		05 H	Control Register 5 Select (CR5)
		06 H	Control Register 6 Select (CR6)(Rev C only)
01EF H	8 Bit		Control Register Data Port(CDP)

During I/O cycles, the Map Address Register(1EE) provides a 6-bit address to the Map Register (a 64x10 Static RAM). This selects the register for programming or reading the maps. Writing data to the Map Register(1EC) programs the RAM, and that data becomes the uppermost address bits (translated A[14:19] Rev A/B and A[14:22] Rev C) when addressing DRAM in EMS operation. By selecting the auto-increment operation of the Map Address Register, you can write once to the Map Address Register, and follow that with 64 writes to the Map Register and fully program the RAM pages with the address translations. This programs both the standard and alternate context maps.

During memory cycles, address pins and a single bit from the Control Register(1EF) provide the 6-bit address to the Map Register(1EC). The Map Register then puts its programmed data onto the system's external DRAM address lines.

The Map Register contains two sets of 32 registers; used as standard context maps and alternate context maps. This allows two programs to maintain separate and simultaneous register mappings, so switching between two programs is practically instantaneous. In systems with only a single set of 32 registers, when a second program needs to perform EMS operations, it must save the current mapping and then write it's own maps before starting. This requires time, and data may be lost in fast-moving communications programs. The two sets of 32 registers in the HT18 alleviate this problem.

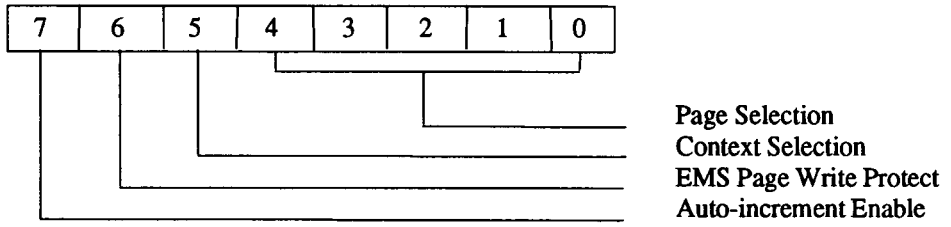
For I/O cycles, the Map Address Register(1EE) page bits (D[0:4]) select 1 of 32 registers, and its Context bit (D5) selects between the two pairs of 32 registers. 0 selects the standard context maps, and 1 selects the alternate context maps. These six bits drive the address lines of the 64x10 RAM, or Map Register. An additional bit determines whether auto-incrementing is enabled (D7). If enabled, when a count of all ones is reached on D[0:6], D7 is cleared and auto-incrementing ceases.

For the memory cycles, 6 address pins select pages among the 32 registers. The address pins are either A[14:19] or SA[14:19], depending upon whether the CPU has control of the system or not. Multiplexing of the 3 upper addresses, ie A[17:19], reduces this 6-bit address to 5 inputs to the Map Register. As with I/O cycles, there is a Context bit to select between the 2 sets of 32 registers. D0 of the Control Register (1EF) provides context information; a 0 selects the standard context maps.

The Map Register outputs 10 lines, the 7 least significant provide DRAM addresses (Rev A/B), 12 output lines(Rev C)7 least significant and 2 most significant provide DRAM addresses, Bits[8:7] provide bank selection , and thus generate RAS*[0:3], and D9 is for bank enable. When EMS memory accesses occur, A[0:13] are passed unfiltered to the DRAM. A[14:19] are redirected to the MR as addresses, and the Map Register outputs the translated addresses on its D[0:6] lines. (The smaller 256K DRAM uses only D[0:4] outputs.)

The full EMS register descriptions follow.

Map Address Register 8 R/W bits at I/O address 1EE (Hex) **Reset State:0**



D7 Auto-increment Enable

When 1, each read or write of the Map Register (1EC) increments the count on D[7:0]. These bits can be treated as a 8-bit counter, which auto-increments under D7 control. The counter consists of Auto-increment enable (D7), EMS Page Write Protect (D6), Context Selection (D5), and Page Address bit (D[4:0]).

By initializing the counter to 80 hex (auto-incrementing on, standard context, and page 40000 H) the maximum number of automatic accesses is available. 32 standard-context writes are followed by 32 alternate-context writes will bring the count to C0. Then, 32 reads in each context would increment the counter to 00. The 64th read clears the auto-incrementing enable (D7), and prevents further increments until D7 is manually set back to 1.

D6: EMS Page Write Protect

0, Do not write protect the selected page when data is written to the Map Register to select the physical memory to map into this EMS page.

1, Write protect the selected page when data is written to the map register to select the physical memory to map.

D5: Context Selection

0 standard context is the default

1 alternate context

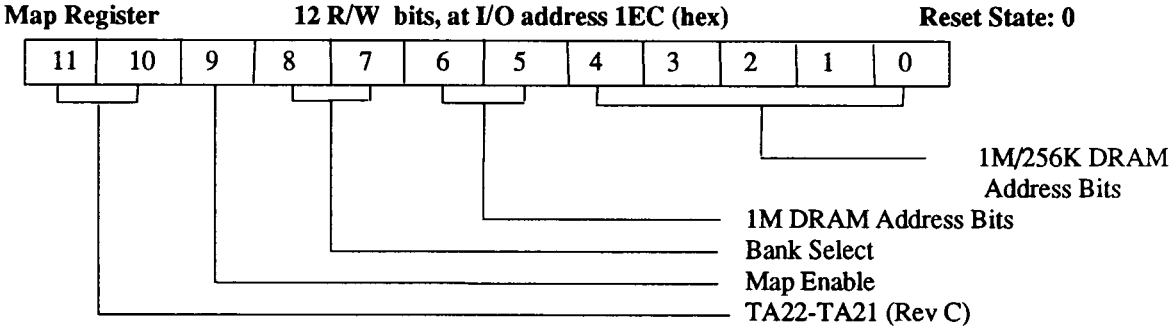
The HT18 contains two sets of 32 registers, each maps to different available pages. Bit D5 switches between the two sets of registers during I/O cycles. (CR's D0 is context selection during memory cycles.) This allows one program to access its 32 mapping registers (standard context), and a second program has an alternate set of register maps (alternate context). With two pairs of registers available, changing between two programs is almost instantaneous, and data integrity is maintained. D5 selects the active set of map registers during I/O EMS cycles.

D[4:0]: Page Selection

Page selection is determined by these 5 bits. Once latched in the MAR, with incrementing enabled, they generate the address lines to the Map Register for I/O cycles. Select the appropriate page(s) by setting D[4:0] according to table below. A minimum of 4 contiguous 16k pages must be selected for EMS operation. (EMS requires a Page Frame size of 64K or more, thus four 16K pages.) Note that page addresses are presented in the following table as both hexadecimal and decimal numbers.

Hex Page Address	Decimal Page Address	Register 1EE Bits				
		4	3	2	1	0
DC000-DFFFF	880-896K	1	1	1	1	1
D8000-	864 -	1	1	1	1	0
D4000-	848 -	1	1	1	0	1
D0000-	832 -	1	1	1	0	0
CC000-CFFFF	816 - 832K	1	1	0	1	1
C8000-	800 -	1	1	0	1	0
C4000-	784 -	1	1	0	0	1
C0000-C3FFF	768 - 784K	1	1	0	0	0
....	... ...	....				
9C000-9FFFF	624 - 640K	1	0	1	1	1
98000-	608 -	1	0	1	1	0
94000-	592 -	1	0	1	0	1
90000-	576 -	1	0	1	0	0
8C000-8FFFF	560 - 576K	1	0	0	1	1
88000-	544 -	1	0	0	1	0
84000-	528 -	1	0	0	0	1
80000-	512 -	1	0	0	0	0
7C000-7FFFF	496 - 512K	0	1	1	1	1
78000-	480 -	0	1	1	1	0
74000-	464 -	0	1	1	0	1
70000-	448 -	0	1	1	0	0
6C000-6FFFF	432 - 448K	0	1	0	1	1
68000-	416 -	0	1	0	1	0
64000-	400 -	0	1	0	0	1
60000-	384 -	0	1	0	0	0
5C000-5FFFF	368 - 384K	0	0	1	1	1
58000-	352 -	0	0	1	1	0
54000-	336 -	0	0	1	0	1
50000-	320 -	0	0	1	0	0
4C000-4FFFF	304 - 320K	0	0	0	1	1
48000-	288 -	0	0	0	1	0
44000-	272 -	0	0	0	0	1
40000-43FFF	256 - 272K	0	0	0	0	0

4000 increments in hex. 16K increments in decimal.



D[11:10] Translated Address [22:21] for 4M DRAM(Rev C)

D9 Map Enable

When the Global EMS Enable bit in Control Register 0 is a 1, the Map Enable bit associated with each 16K page acts as an individual page mapping enable. If Map Enable is a 1, then its corresponding page is remapped by the HT18. If the Map Enable bit is 0, the CPU address lines are passed through untranslated. If the Global EMS Enable bit is a 0, all address remapping is turned off regardless of the state of the individual Map Enable bits.

D[8:7] Bank Select

For 1M/256k, selection as follows:

D8	D7	
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

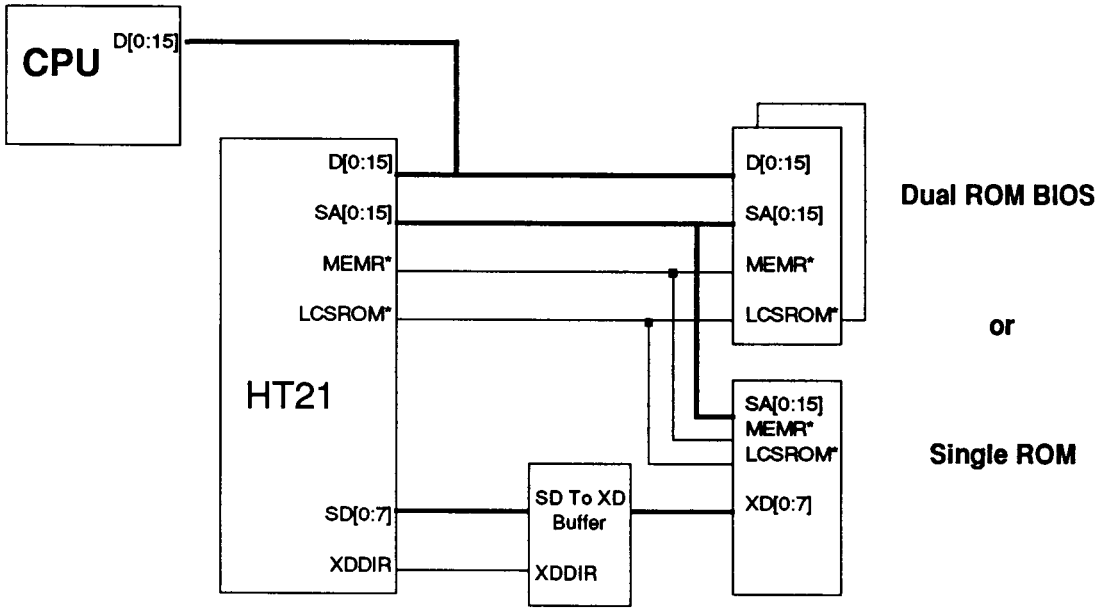
D[6:5] Translated address bits for 1 Meg DRAMS

They drive A[20:19] on system DRAMs.

D[4:0] Translated address bits for 256K/1M DRAMs

They drive A[18:14] on system DRAMs.

ROM/BIOS Interface



ROM Memory Interface

The HT18 ROM interface has three modes of operation, based on desired BIOS Data location and system configuration. The traditional mode has BIOS code stored in two ROM devices on the CPU data bus. The single BIOS mode utilizes one ROM device on the XD bus. Both of these modes support the third Shadow RAM mode where BIOS data is copies from either source into system RAM that shadows the slower ROM device allowing the ROM device to disabled.

The HT18 utilizes a Single BIOS (SBIOS*) input pin used to select two of the interface modes. A low level on the SBIOS* input pin is used to activate the single BIOS, 8-bit mode and a high level places the ROM interface in the two chip BIOS, 16-bit mode. Both of these modes utilize a Latched Chip Select ROM output pin (LCSROM*). This signal is activated by memory accesses between 0E0000H to 0FFFFFH and FE0000H to FFFFFFH allowing upto 128KB of addressable ROM space The E0000 to EFFFF Range of LCSROM* can be disabled using Control Register 4 bit 0. ROM access can be disabled by switching to the shadow RAM mode.

When the ROM interface is in the single BIOS mode the HT18 will read twobytes of data from the low byte of the SD[0:7] inputs while placing a low level on the eXternal Data DIRection output pin (XDDIR), which will source the data from the eXternal Data BUS (XD[0:7]0. This is the standard method of converting 8-bit I/O accesses to one 16-bit word required by the CPU. ROM reads are at slow speed.

The third ROM mode supported by the HT18 is called the shadow RAM mode. This is where an image of the BIOS (which is in ROM) is copied into an area of RAM and the normal ROM access are disabled. The purpose of this feature is to allow operating systems and software applications to make faster accesses to the shadowed BIOS data contained in RAM (rather than the much slower ROM devices).

The performance improvement derived from the use of shadow RAM is primarily dependent on the difference in access times between ROM and DRAM cycles. At higher system speeds, the difference can be significant. The normal use of the shadow RAM mode allows higher system performance and can be combined with the single 8-bit ROM interface to reduce circuit board size requirements and component count. This combination reduces system cost without sacrificing system performance..

Shadow RAM mode can be implemented using internal Control Register 0 (01EFH). The following procedure defines a suggested programming sequence to enable the shadow RAM mode.

1. Disable any remap for F0000-FFFFF.
2. Switch to context 0. It is necessary to copy the System BIOS into shadow RAM. Hence, the System BIOS addresses F0000-FFFFF cannot be remapped elsewhere.
3. Remap four pages e.g. 90000 to F0000, 94000 to F4000, 98000 to F8000, and 9C000 to FC000 in context 0.
4. Enable EMS if it is not already enabled.
5. Block copy F0000-FFFFF to 90000-9FFFF.
6. Enable the shadowing of the System BIOS. Note that the shadow enable bits (bits 3 and 4 of Control Register 0) have no effect unless the global EMS enable bit is set.

When the 384K Memory Relocation feature is enabled, (CR0, bit 2 = 0) local memory in the A0000 address range is relocated upward by 384K and is not available for shadow RAM.

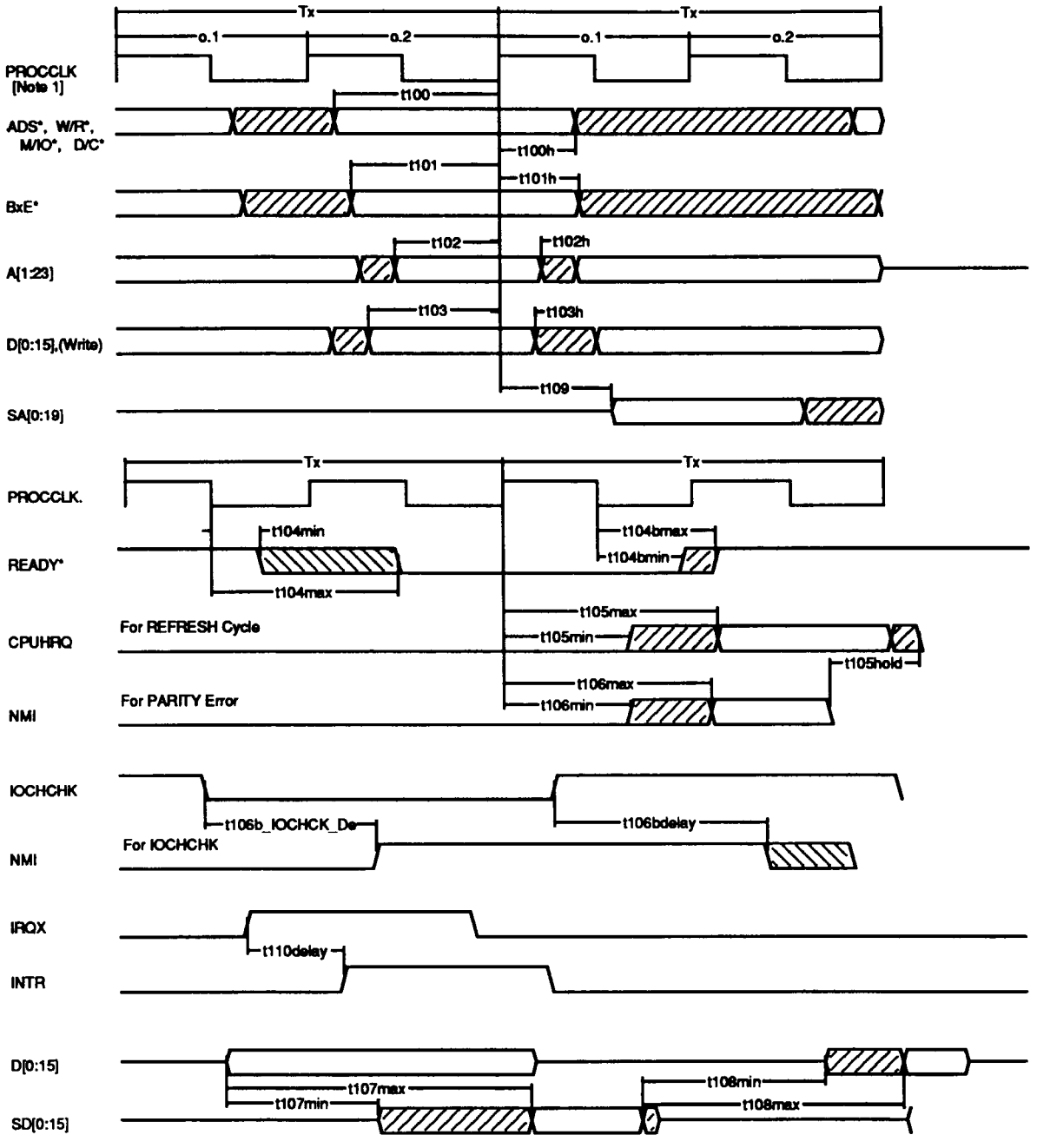
A.C. Timing Specifications for HT18

CPU Interface

Signal timing Characteristics

Note: Values are for 25(Rev C) 20 and 16 MHz CPU Clock speeds unless other wise noted All values measured in Nano Seconds

Reference	Parameter	Min	Max
t100setup	ADS*, M/IO*, W/R*, D/C* Setup time to PROCCLK (Pipeline)	19	
t100hold	ADS*, M/IO*, W/R*, D/C* Hold time to PROCCLK	6	
t102setup	A Bus Setup time to PROCCLK	17	
t102hold	A Bus Hold time to PROCCLK	4	
t109	PROCCLK to SA Bus Propagation Delay (20 Mhz)	12	24
t101setup	BHE* Setup time to PROCCLK	17	
t101hold	BHE* Hold time to PROCCLK	4	
t103setup	D Bus Setup time to PROCCLK	14	
t103hold	D Bus Hold time to PROCCLK	4	
t108	SD to D Bus Data Valid Delay 16-Bit	5	18
t108	SD to D Bus Data Valid Delay 16-Bit to 8-Bit		
t107	D to SD Bus Propagation Delay (16-Bit Xfer)	22	46
t107	D to SD Bus Propagation Delay (16-Bit to 8-Bit Xfer)	—	—
t110	INTR Valid Delay from IRQ [3:7]	11	39
t110	INTR Valid Delay from IRQ[9:15]	15	54
t106	NMI Valid Delay from PROCCLK (for local RAM parity error)	—	—
t106b	NMI Valid Delay from IOCHCK (for I/O devices)	–	–
t104	READY* Valid Active Delay from PROCCLK	4	15
t104b	READY* Valid Inactive Delay from PROCCLK	3	12
t105	CPUHRQ Valid Delay from PROCCLK	3	28
t156delay	RESETCPU Valid Delay from PROCCLK	3	14



A.C. WAVEFORMS - CPU Interface Specifactions

A.C. Specifications for HT18

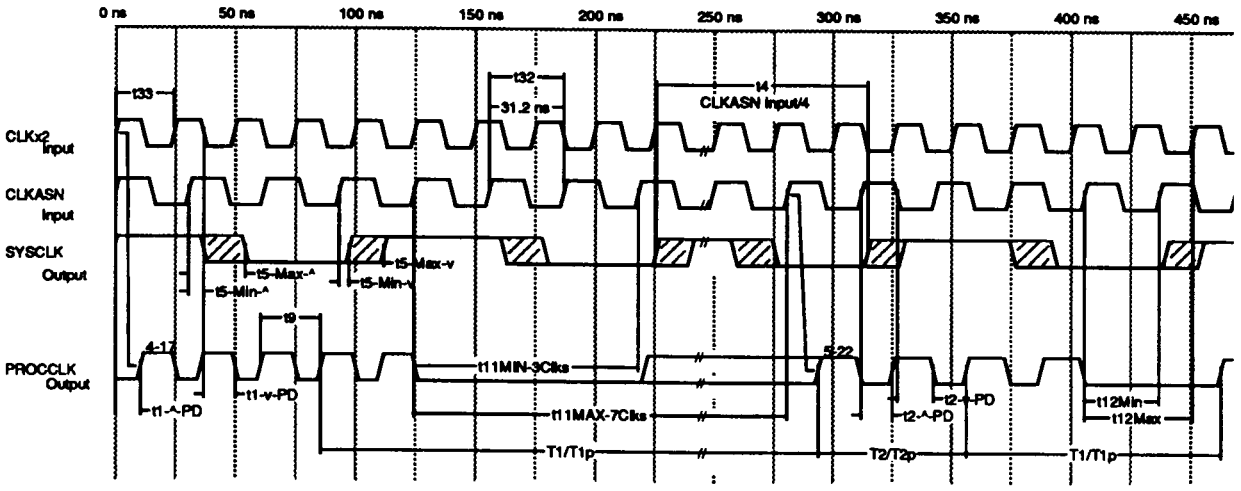
Clock Generation

Signal timing Characteristics

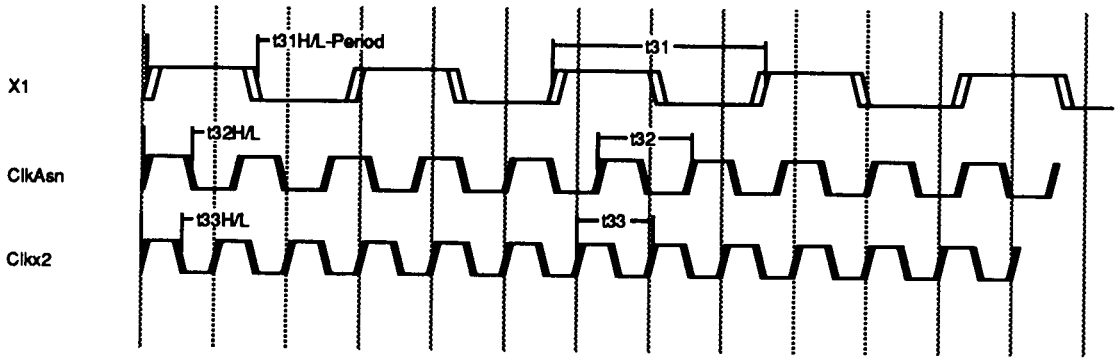
Reference	Parameter	Min	Max
	CLKX2 Input Frequency Rev. A/B	.5	40MHz
	CLKX2 Input Frequency Rev. C	.5	50MHz
t33	CLKX2 Cycle Time (Osc Input)		27.5ns
	CLKASN Input Frequency (Non-AT Bus Compatible Mode)	.5	48 MHz
	CLKASN Input Frequency (AT Compatible 8MHz Bus)	.5	32MHz
t32	CLKASN Cycle Time (Osc Input)		34.4ns
	X1 Input Frequency	14.318 MHz	+/- 5 %
t31	X1 Cycle Time (Osc Input)	0	76.8ns
t33 Period	CLKX2, Low/High Pulse (Osc Input)	12.5	15.0ns
t32 Period	CLKASN, Low/High Pulse (Osc Input)	15.6	18.8
t31 Period	X1 High/Low Pulse	34.9	41.9
t1 ↑ PD	↑ CLKX2, to PROCCLK ↑ Delay	4	17
t1↓ PD	↓ CLKX2 to PROCCLK ↓ Delay	5	21
t2 ↑PD	↑ CLKASN to PROCCLK ↑ Delay	5	22
t2 ↓ PD	↓ CLKASN to PROCCLK ↓ Delay	6	25
t9	PROCCLK Period CLKX2 Source(40MHz CLK)	25	
t10	PROCCLK Period CLKASN/2 Source (16MHz CLK)	62	
t11	PROCCLK Switch Time Low Period, Fast (Source CLKX2) to Slow (Source CLKASN)		
	CLKX2 = CLKASN (# of clock cycles)	3.5	5
	CLKX2 ≠ CLKASN (# of clock cycles)	3	7
t12	PROCCLK Switch Time Slow (Source CLKASN) to Fast (Source CLKX2)		
	CLKX2 = CLKASN (# of clock cycles)	1	2
	CLKX2 ≠ CLKASN (# of clock cycles Min=1 CLKASN)	1	2(1)
t5	↑ CLKASN to ↑ SYSCLK Delay	4	18
t5	↑ CLKASN to ↓ SYSCLK Delay	8	23
t4	SYSCLK Frequency (CLKASN/4 with 32MHz CLKASN)		8MHz
	HISPEED Setup to PROCCLK 18A	8ns	
	18B/C	0ns	

NOTE: PD = Prop Delay

(1) 2 Cycles = 1 CLKASN cycle + 1 CLKX2 cycle.



A.C. CLOCK SWITCH SPECIFICATION - High to Low and Low to High



A.C. CLOCK INPUT SPECIFICATION - Input Tolerance Variations passed to outputs.

A.C. Specifications for HT18

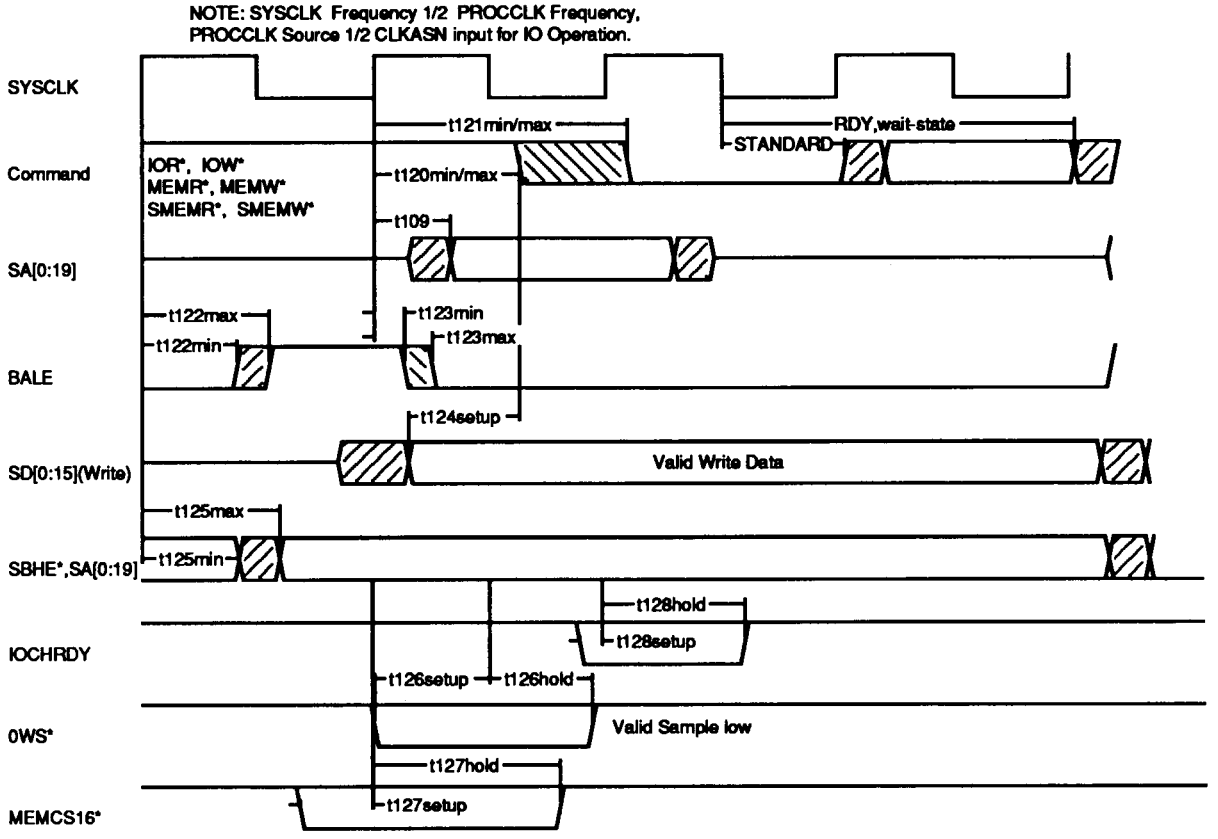
I/O Channel Interface

Signal timing Characteristics

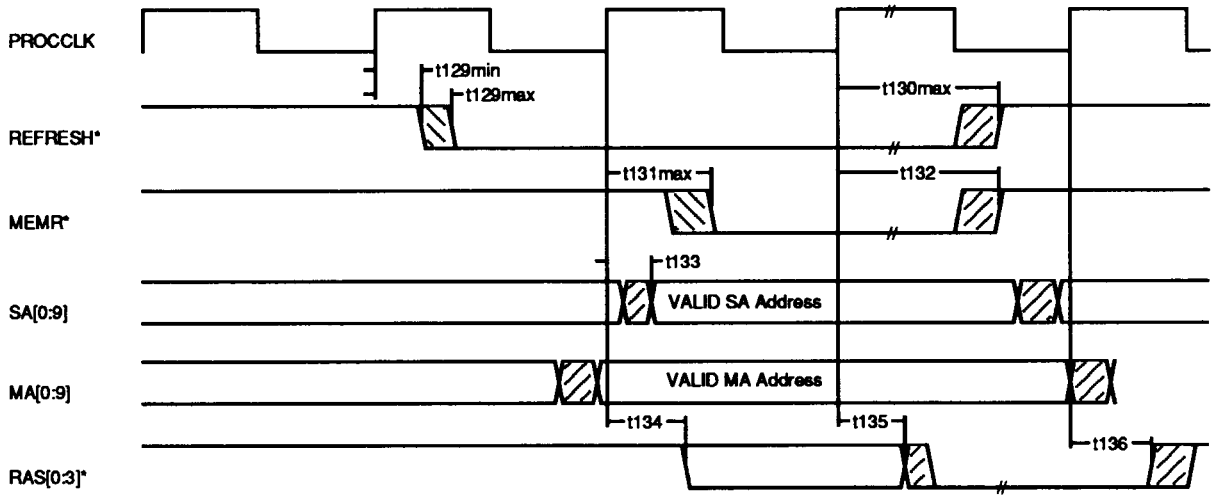
Reference	Parameter	Min	Max
t122	BALE Active Delay fm PROCCLK Active/Inactive	6/8	23/27
t12xsetup/hold	IOCHCK*		
t128setup/hold	IOCHRDY Setup and Hold time	9	
t12xsetup/hold	IOCS16* Setup and Hold time	9/0	
t127set/hold	MEMCS16* Setup and Hold time	13/2	
t120/t121	IOR* Command Active delay / Inactive	7/5	23/19
t120/t121	IOW*Command Active delay / Inactive	7/5	23/19
t120/t121	MEMR* Command Active delay / Inactive	7/6	25/20
t120/t121	MEMW* Command Active delay / Inactive	7/6	25/20
t120/t121	SMEMR* Command Active delay / Inactive	7/6	26/21
t120/t121	SMEMW* Command Active delay / Inactive	7/6	26/21
t125	SBHE* Command Active delay / Inactive	10/9	19/18
t133	Clock to SA Bus Propagation Delay (REFRESH*)	8	31
t108	SD[0:15] to D Bus delay	1	7
t126setup/hold	0WS*	12/0	

Refresh Timing

t129	Refresh active delay	5	19
t130	Refresh inactive delay	4	16
t131	MEMR active delay	6	25
t132	MEMR inactive delay	6	26
t134	RAS* active delay (REFRESH*)	8	30
t135	Staggered RAS* active delay	5	18
t136	RAS* inactive delay	6	26



REFRESH Cycle Timing



A.C. WAVEFORMS - IO INTERFACE Timing

A.C. Specifications for HT18

Keyboard Interface

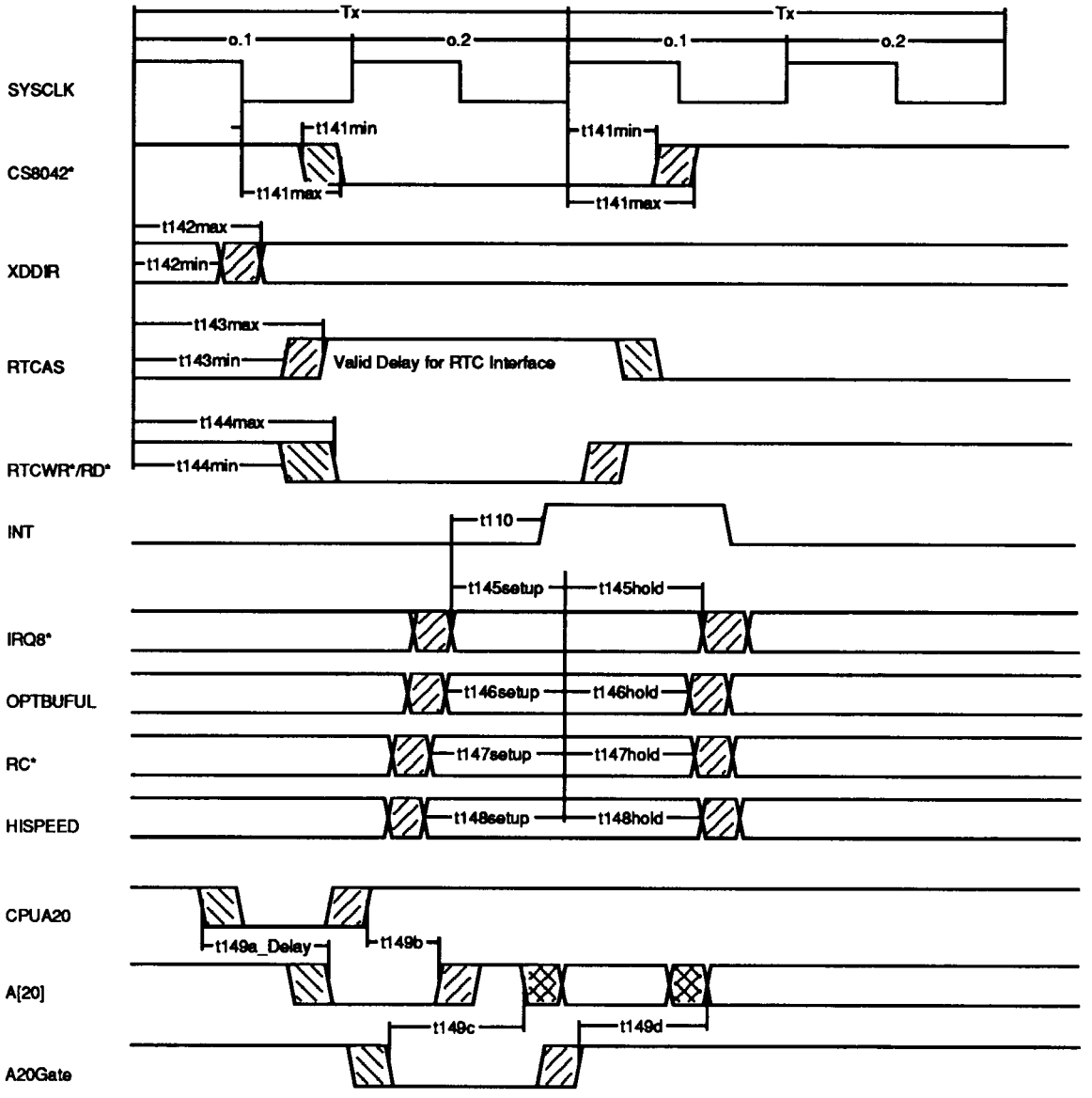
Signal timing Characteristics

Reference	Parameter	Min	Max
t141	CS8042* Active delay / Inactive	7	27
t148setup/hold	HISPEED Setup and Hold time Rev A	5	
	Rev B/C	0	
t120/121	IOR* Command Active delay / Inactive	7/5	23/19
	IOW *Command Active delay / Inactive	7/5	23/19
t146	OPTBUFUL to INT delay	9	36
t147setup/hold	RC *Setup and Hold time	0	
t142	XDDIR Command Active delay / Inactive	7/32	7/30
t149setup	A20GATE delay to A20		
	CPUA20 to A20 dealy		

Real-time Clock Interface

Signal timing Characteristics

Reference	Parameter	Min	Max
t110setup/hold	IRQ8* delay to INT	15	54
t143min/max	RTCAS Active delay / Inactive	9/7	
t144min/max	RTCRD *Active delay / Inactive	7/8	29/31
t144min/max	RTCWR* Active delay / Inactive	7/8	29/30
t142min/max	XDDIR Active delay / Inactive	7/32	7/30



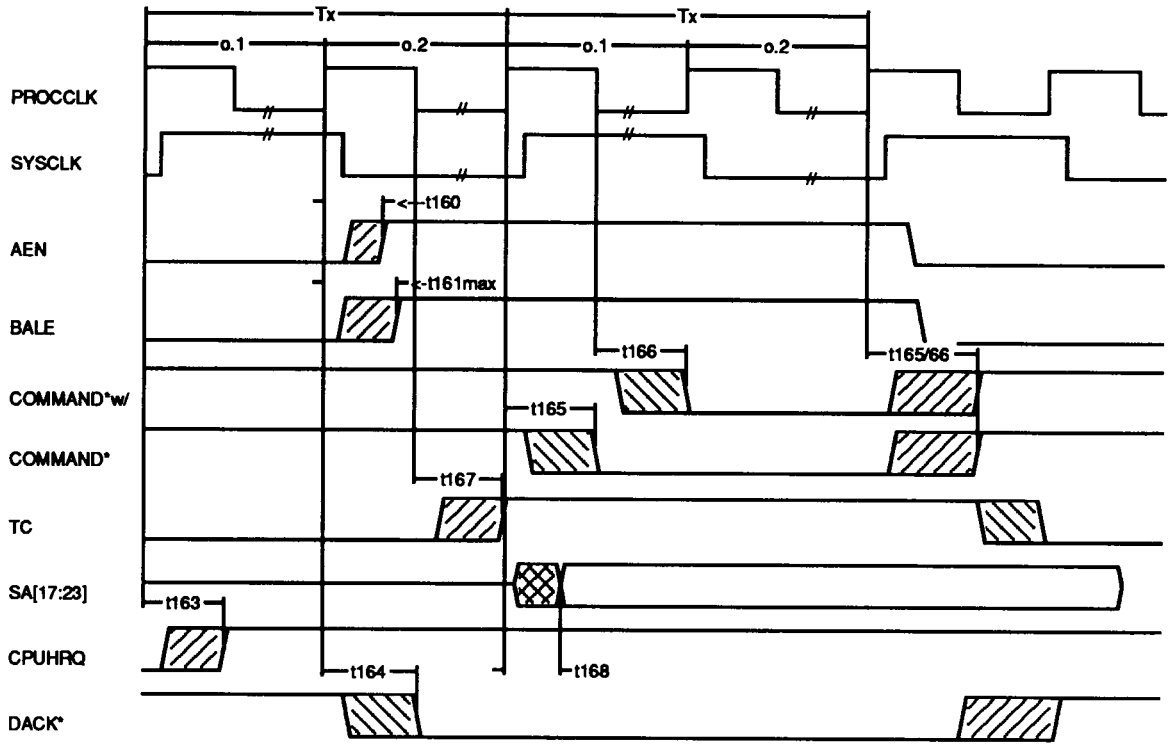
A.C. WAVEFORMS - Valid Delay, Setup and Hold timing for Keyboard and RTC Interface

A.C. Specifications for HT18

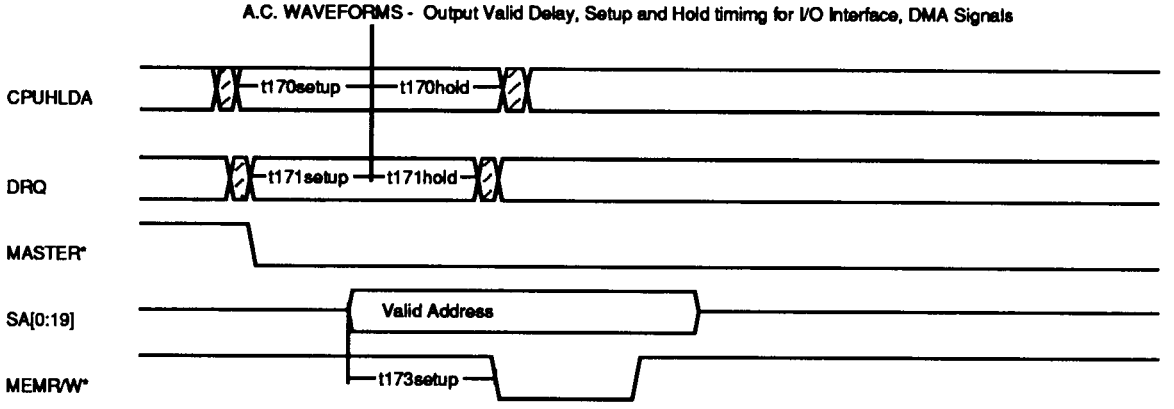
DMA Controller

Signal timing Characteristics

Reference	Parameter	Min	Max
t160	AEN Active delay / Inactive (from PROCCLK)		20/21
t161	BALE Active delay / Inactive (from PROCCLK)		25/28
t170	CPUHLDA Setup and Hold time		20/4
t163	CPUHRQ Active delay / Inactive	3/4	28/20
t164	DACK* Active delay / Inactive	8/	32/26
t171	DRQ Setup and Hold time	4/17	3/19
t172	AEN delay from MASTER* AEN↓		15
	AEN ↑	3	11
t165/t166	IOR* Active delay / Inactive	8	31
t165/t166	IOW* Active delay / Inactive	8	31
t165/t166	MEMR* Active delay / Inactive	8	29
t165/t166	MEMW* Active delay / Inactive	9	31
t173	SA[0:19] Address Valid Delay in MASTER* mode		
t169	SBHE* Active delay / Inactive	13/13	46/47
t167	TC Active delay / Inactive	9/8	30/29
t168	SA[17:23] delay	3	19



A.C. WAVEFORMS - Output Valid Delay, Setup and Hold timimg for I/O Interface, DMA Signals



A. C. WAVEFORMS - MASTER Mode Valid Address Input Specifacation

A.C. Specifications for HT18

Interrupt Controller and RESET timing

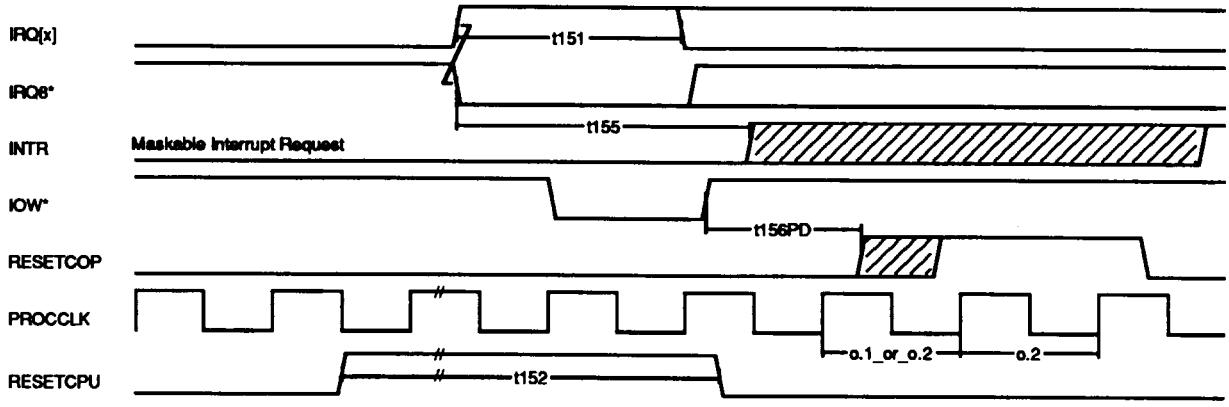
Signal timing Characteristics

Reference	Parameter	Min	Max
t151	Valid Interrupt Pulse Width	65	
t150	INTR Valid delay time from IRQ[3:7],[9:12],[14:15]		
t156	RESETCOP Active Delay from PROCCLK		
t152	Reset Valid Pulse Width	250	

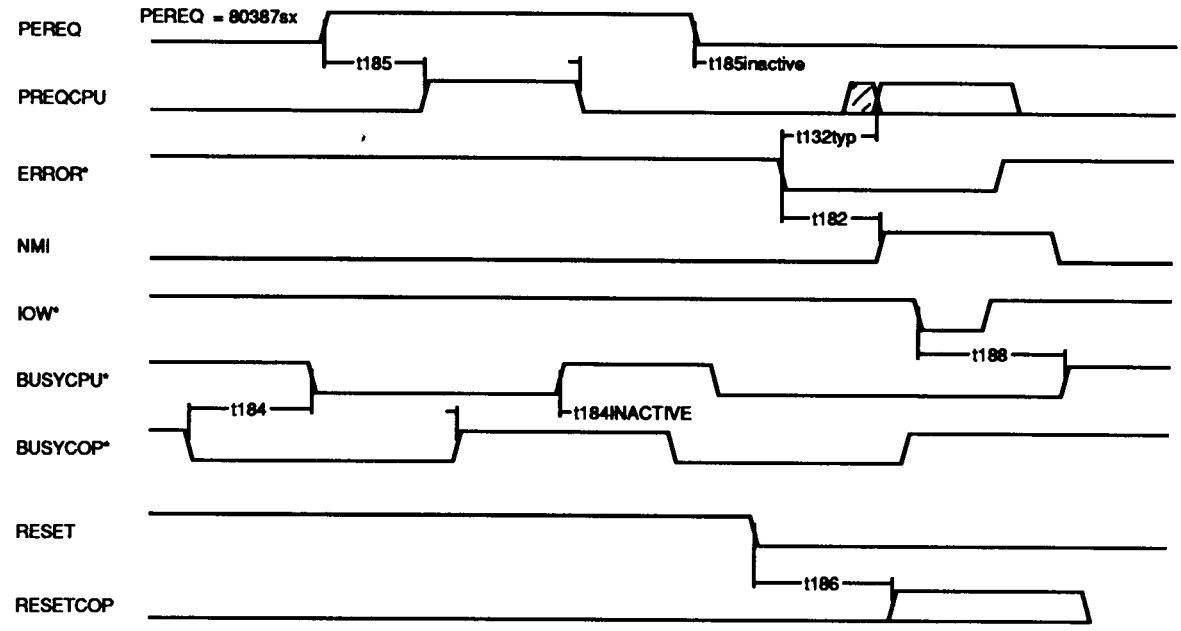
NPU Interface

Signal timing Characteristics

Reference	Parameter	Min	Max
t180setup/hold	PEREQ*		
t181setup/hold	BUSYCOP*	16/7	18/20
t182setup/hold	ERROR* delay to NMI		
t184	BUSYCPU* Active Delay from BUSYCOP*	5	19
t185	PEREQCPU Active Delay from PEREQ		
t186	RESETCOP Active Delay		
t188	IOW* ↓ to BUSYCPU* Inactive	3	12



A.C. WAVEFORMS - INTERRUPT AND RESET SIGNAL SPECS - Interrupt Signals and Reset

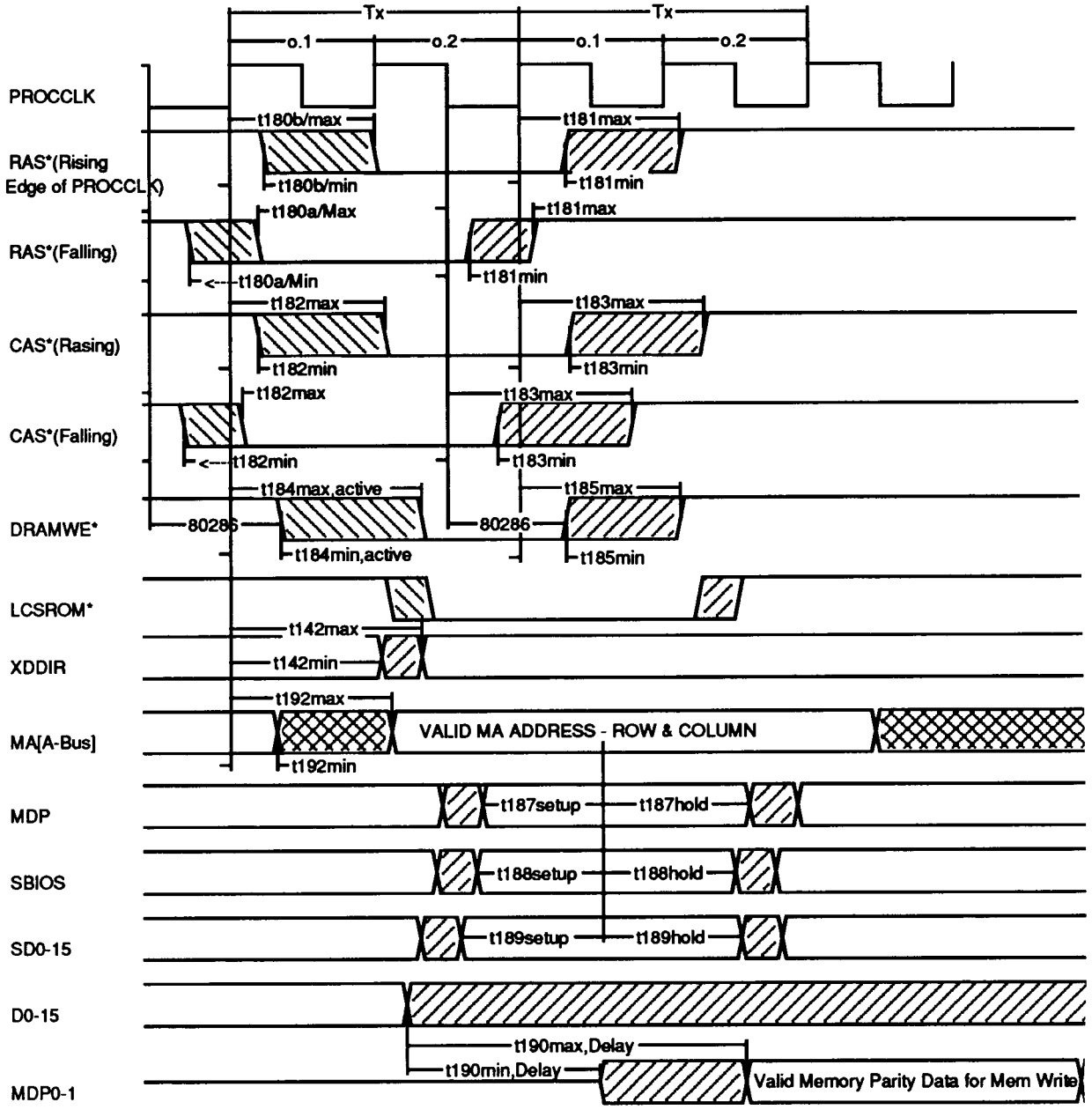


A.C. WAVEFORMS - NPU Interface - Signals shown for timing reference

AC Specifications for HT18

Memory Interface

Reference	Parameter	Min	Max
t180a/b	RAS*[0:3] Active delay from PROCCLK 80386SX ↓ Pipelined ↑ Non-pipelined	7	19
t181a/b	RAS*[0:3] Inactive delay from PROCCLK 80386SX ↓ Pipelined ↑ Non-pipelined	4	15
t182a/b	CAS*[0:3] Active delay PROCCLK 80386SX ↓ Pipelined ↑ Non-pipelined	6	16
t183a/b	CAS*[0:3] Inactive delay PROCCLK 80386SX ↓ Pipelined ↑ Non-pipelined	9	32
t 184	DRAMWE* Active delay from PROCCLK 80386SX ↑	9	33
t185	DRAMWE* Inactive delay from PROCCLK 80386SX ↑	8	28
t186	LCSROM* Active delay from PROCCLK		
t120/121	MEMR* Command Active delay from PROCCLK	6	
t187setup/hold	MDP[0:1] Setup and Hold time (Memory Read)		
t189setup/hold	SD[0:15] to D Bus delay	22	46
t191delay	MA[0:9] Addrss delay from A bus	38	65
t190	MDP[0:1] Valid Data from D bus (Mem Write)		
t192	MA Delay from PROCCLK ↓ before CAS*	8	28
t192	MA Delay from PROCCLK ↓ before RAS*	8	28



A.C. WAVEFORMS - MEMORY SPECIFACATION - Output Valid Delay for Memory Interfac

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC Input Current	IIN	10	mA
Storage Temperature Range (Plastic)	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	VDD	+4.75 to +5.25	V
Operating Ambient Temperature Range (Commercial)	TA	0 to +70	C

DC Characteristics: VDD = 5V +/- 5%, TA = 0C to 70C

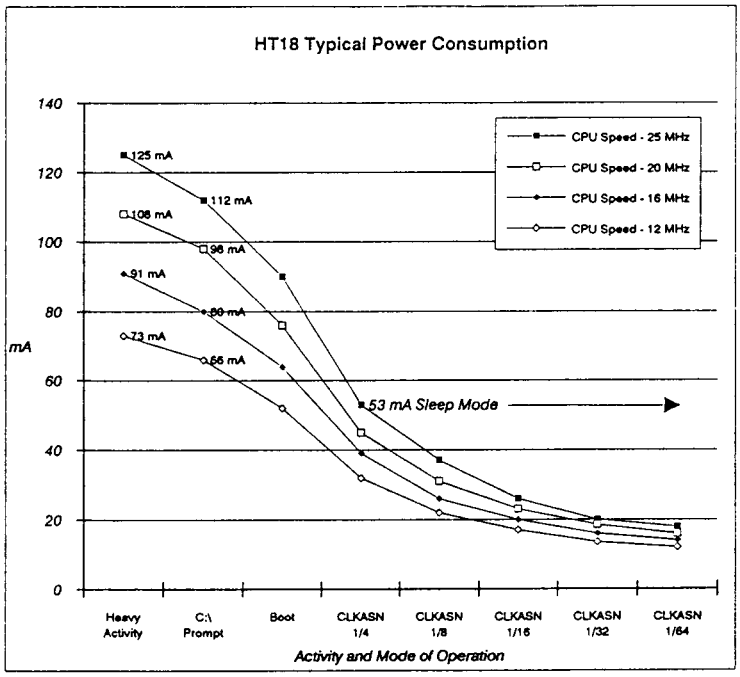
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input LOW	VIL				0.8	V
Voltage Input HIGH	VIH		2			V
Input Current	IIH		-10	1	10	uA
Voltage Output High	VOH					V
PROCCLK		IOH=-8mA	4.2			
MA[0:9](A/B)MA[0:10](C), RAS*[0:3], DRAMWE*		IOH=-12mA	2.4	4.5		
CAS*[0:3] MDP[0:1], SD[0:15], IOCHRDY*		IOH=-8mA	2.4	4.5		
RESET*, REFRESH*, (open drain)		IOH=8mA	2.4	4.5		
READY*, CPUHRQ, NMI, IOR/W*, RC*, SA[0:19],ADS*, RESETCOP, INTR, BUSYCPU*, RESETCPU, SYSCLK, CS8042*, RTCAS, RTCWR*, ERROR, RTCRD*, MDP[0:1], D[0:16], A[17:23], MEMR/W* SPKR, LCSROM*, DACK*[0:3],[5:7], PEREQCPU		IOH=-6mA IOH=-4mA	2.4	4.5		
Voltage Output Low	VOL			0.4	0.8	V
PROCCLK		IOL=8mA				
CAS*[0:3], MDP[0:1],MA[0:9](A/B) [0:10](C),DRAMWE*		IOL=12mA				
SD[0:15], IOCHRDY*		IOL-24mA				
RESET*, REFRESH*, (open drain) SA[0:9], IOR/W*, SYSCLK, MEMR/W*, RAS*[0:3]		IOL=12mA				
READY*, CPUHRQ, NMI, IOR/W*, RC, DACK*[0:3],[5:7],ADS*, RESETCOP, INTR, BUSYCPU*, RESETCPU, SYSCLK, CS8042*, RTCAS, RTCWR*, ERROR, RTCRD*, MDP[0:1], D[0:16], A[17:23],MEMR/W* SPKR, LCSROM*, PEREQCPU		IOL=6mA IOL=4mA				
3-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	1	10	uA
Output Short Circuit Current	IOS	VDD=Max, V0=VDD	20	110	220	mA
		VDD=Max. V0=OV	-10	-90	-190	mA
Supply Current	IDD	CLK=16MHz, CL=50pf		80		mA

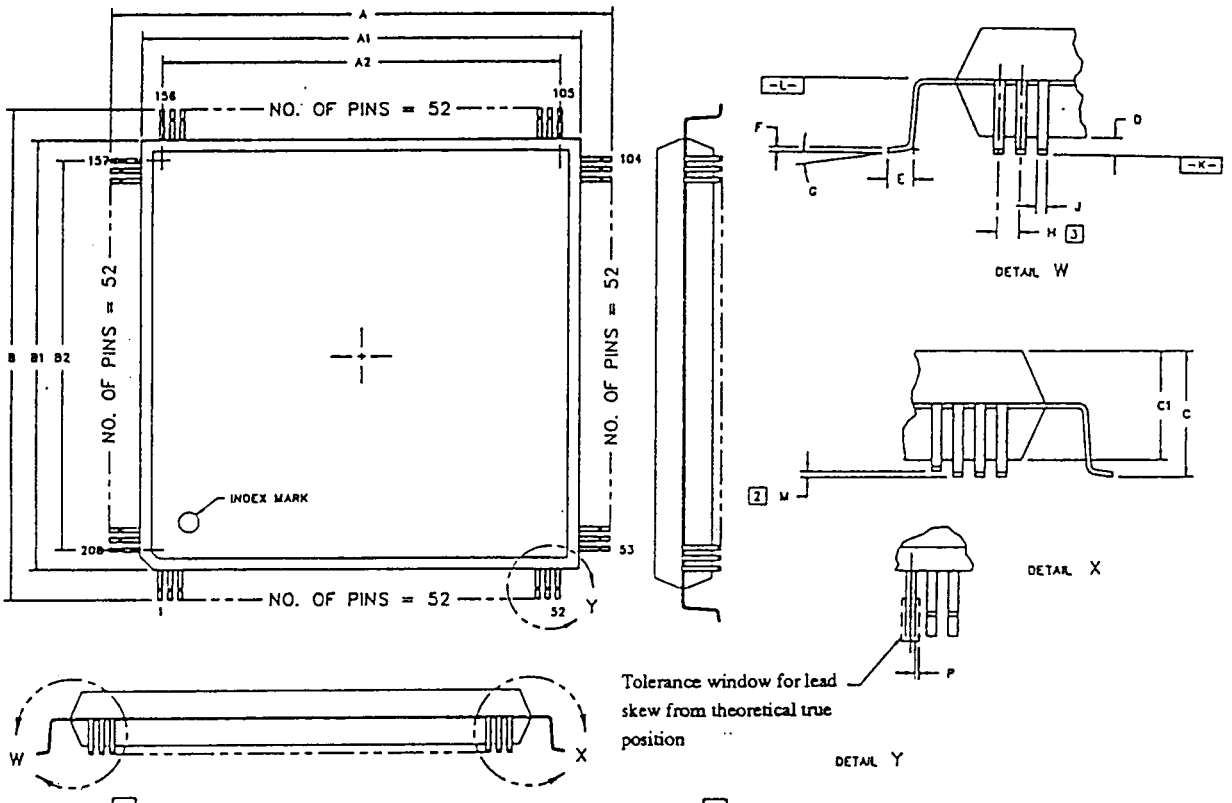
Note: Not more than one output may be shorted at a time for a maximum duration of one second.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input Low	VIL					
TTL Inputs		PEREQ Input Pin (A/B)			0.8	V
CMOS Levels (A/B)(1) (C)*		POWERGOOD Input Pin (C)			.3VDD	V
Volttage Input High	VIH					
TTL Inputs		PEREQ Input Pin (A/B)	2			V
CMOS Levels (A/B)(1) (C)*		POWERGOOD Input Pin (C)	.7VDD			V
Switching Threshold	VT	CMOS		2.5		V
		TTL		1.5		V
Schmitt Trigger, Positive-going Threshold*	VTT	CMOS		3	4	V
		TTL			1.8	V
Schmitt Trigger, Negative-going Threshold*	VTT	CMOS	1	1.5		V
			0.7	0.9		V
Hysteresis, Schmitt Trigger*		CMOS VIL to VIH	1	1.5		V
		TTL VIL to VIH	0.4	0.8		V

(1) For PEREQ Signal REV. A/B
* For POWERGOOD Signal

Pullup/Pulldown Resistor Values	Internal Resistor Type	Resistance Range	
		Min	Max
Rev. A, B Parts	PU	38K	330K
	PD	45K	500K
Rev. C Parts	PU/PD	15K	143K





1

DIMENSIONS IN MM		
SYM	MINIMUM	MAXIMUM
A	30.30	30.90
A1	27.90	28.10
A2	25.50 REF.	
B	30.30	30.90
B1	27.90	28.10
B2	25.50 REF.	
C	3.68	4.01
C1	3.43	3.66
D	0.25	0.36
E	0.30	0.70
F	0.10	0.25
G	0°	10°
H	0.40	0.60
J	0.15	0.25
M	0.10 MAX.	
P	0.05 MAX.	
TOTAL NO. OF PINS	208	

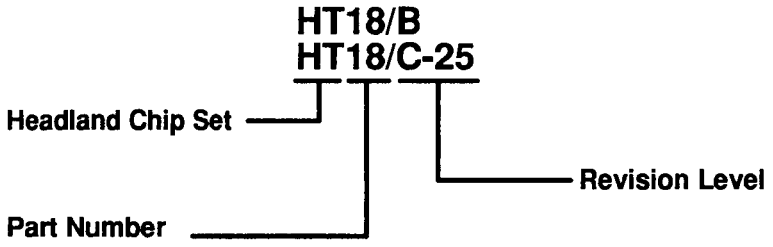
1

DIMENSIONS IN INCHES		
SYM	MINIMUM	MAXIMUM
A	1.193	1.216
A1	1.098	1.106
A2	1.004 REF.	
B	1.193	1.216
B1	1.098	1.106
B2	1.004 REF.	
C	.145	.158
C1	.135	.144
D	.010	.014
E	.012	.028
F	.004	.010
G	0°	10°
H	.020 ±.004	
J	.006	.010
M	.004 MAX	
P	.002 MAX.	
TOTAL NO. OF PINS	208	

Notes: Unless otherwise specified

1. Nominal dimensions in millimeters. Inches rounded to the nearest .001 inch. Controlling dimension in millimeters.
2. Coplanarity of all leads shall be within 0.1MM (0.004") (Difference between highest and lowest lead with seating plane -K- as reference)
3. Lead pitch determined at Datam -L-

Product Order Information



IMPORTANT: Contact your local sales office for the current Order Code/Part Number