Headland
Technology Inc

GCK131
80386 AT Compatible Chip Set

Features

- Highly-integrated 25 MHz, AT-compatible (80386) three chip set.
- Each device includes an integral, register-level configuration system to manage system performance.
- Software programmable wait-state generator and memory manager that supports page mode and interleaved memory access.
- Supports 'shadow RAM' for system and video BIOS ROM.
- Supports 24 Mbytes of DRAM and either 256K or 1 Mb devices.
- Supports 128K or 64K EPROM space.
- Includes software configured decode logic for serial and parallel I/O.
- Supports 80387 or 80287 numeric coprocessor.
- Supports connection to an EEPROM for non-volatile storage of configuration setup data. Eliminates DIP switches and jumpers.
- Low board space requirements - laptop design is feasible.
- Designed in 0.9 micron HCMOS.

The GCK131 Chip Set, of three highly integrated HCMOS microchips, supports an 80386 microprocessor-based computer system in AT-compatible mode at speeds up to 25 MHz.

This high performance three chip set allows the implementation of a powerful computer system with just these components: an 80386 Microprocessor, a keyboard controller, a real time clock, six bipolar devices and up to 24 Mb of memory.

System configuration data is stored in an external EEPROM to eliminate the need for DIP switches and jumpers. Register data for memory and I/O wait states, command delays, and recovery times can be conveniently programmed for the system user through software.

The chip set, using interleaving and page mode access techniques, supports six banks of 32-bit RAM. System BIOS and video BIOS can be 'shadowed' to RAM for faster operation. And ROM accesses can be configured to as low as 1 wait state for optimum performance.

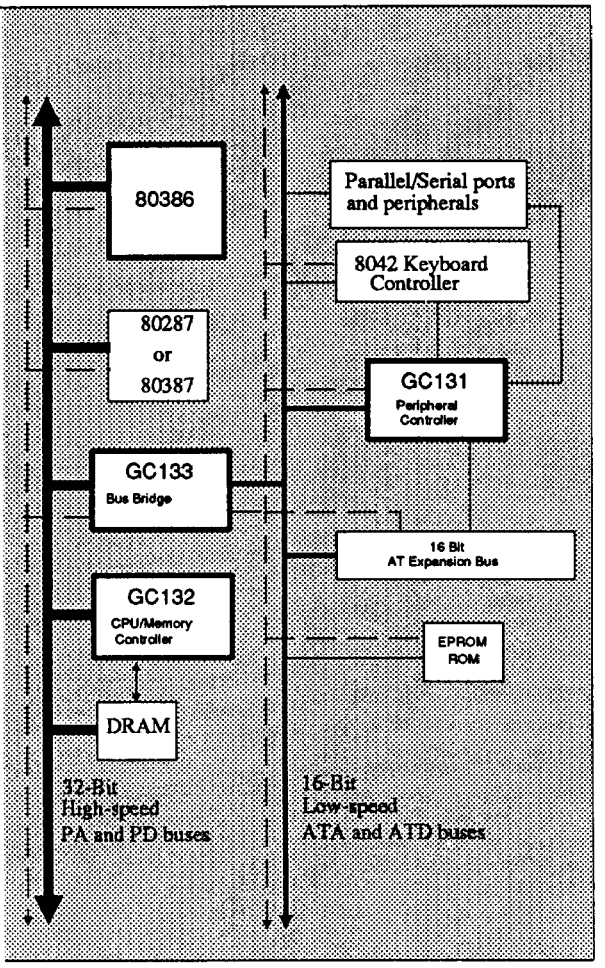

Figure 1—80386 System, block diagram

A highly integrated three chip set

GC131 Peripheral Controller

This single chip effectively replaces two 8259, two 8237, 8254 , an LS612, and other devices. The chip interfaces with an 8042 keyboard controller, real time clock, parallel ports, serial ports, speaker and the EEPROM used for power up configuration.

GC132CPU/Memory Controller

This powerful chip decodes the processor address and control lines and generates the RAS, CAS, and chip select signals required for memory management. Both static and dynamic memories can be used. The *GC132 Controller* features both paged and interleaved memory access techniques that improve overall system throughput.

GC133 Bus Bridge Interface

About this document(*)

Of interest to designers of AT-compatible personal computer systems who wish to employ the inherent speed and added features offered by the 80386 Microprocessor, this technical description of the *GCK131 Chip Set* is organized as shown in the Table of Contents. An Index will be found as the last pages of this document.

Notation

The following notations are used to refer to the configuration registers internal to the *GCK131 Chip Set.*

Notation	*Indicates*
'/'	Indicates ACTIVE LOW signals. Names prefixed with '/' are negated. This notation is equivalent to the use of the asterisk(*), or suffixing the letter 'N' to the signal name. Thus, /REFRESH is used rather than *REFRESH or REFRESHN.
INDEX NNh	NNh denotes the internal register number in hexadecimal notation.
SIGNAL 0,1	A shorthand way of stating SIGNAL 0 and SIGNAL 1. (Where SIGNAL means any signal name.)
SIGNAL 0..7	A shorthand way of stating a series from SIGNAL 0 to and including SIGNAL 7

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Section - 1 System overview

The *GCK131 Chip Set* offers many advantages as a major component of an 80386 Microprocessor-based personal computer system designed to support the 'AT' standard bus.

By incorporating the compact *GCK131 Chip Set* system designers achieve the significant advantages of the 80386 Microprocessor—especially the system's speed, memory capacity, and flexibility—that will boost an AT-compatible microcomputer to superb levels of performance. And, at the same time, the three compact 160-pin ASICs of the chip set reduce the geographical space requirements of the system motherboard. Result: a powerful machine with a smaller system 'footprint'.

Extensive configuration options
An extensive range of built-in configuration registers provides powerful and precise control of operating characteristics of the design.

Connections to the major system blocks of RAM, ROM and cache memory are easily implemented using the available control signals. And a simple interface with the 80386 Microprocessor and the 80287 or 80387 Numerical Coprocessor helps reduce the system design cycle time.

Separation of 32-bit and 16-bit 'worlds'
For system implementation several buses are supported by the *GCK131 Chip Set.* Of these, the 32-bit processor address (PA) and data (PD) bus and the 16-bit address (ATA) and data (ATD) bus are particularly important to the system designer.

The PA and PD bus
The PA and PD bus is the high speed address and data bus that interfaces with the 80386 Microprocessor and the 80287 or 80387 Numerical Coprocessor. This bus also provides the 'local' information path between all three chips of the *GCK131 Chip Set.* The address and the data paths of this bus are 32-bits wide as required to handle the full range of address and data values. In an AT system, I/O devices should not be directly connected to this bus: it is intended, solely, as a high-speed interface.

The ATA and ATD bus
The ATA and ATD bus provides the address and data requirements of the XT/AT expansion bus. This bus, a local to the *GC131 Peripheral Controller,* the *GC133 Bus Bridge Interface,* and the AT expansion bus, has a data width of 16 bits and the 24 bits of addressing that is required for 'AT' standards.
The upper address bits required for the AT expansion bus are supplied by

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buffering the PA17 to PA23 liñes of the PA bus. These, with ATA0 to ATA19, provide the necessary addresses for proper connection to the AT expansion bus.

The ATA and ATD bus, which generally operates at a slower speed than the PA and PD bus, allows the connection of all types of peripheral devices to the *GCK131* supported AT-system. To transfer data between the high-speed PD bus and the slower ATD bus, the *GC133 Bus Bridge Inteface* is used at appropriate times.

Block diagrams
Figures 2a through 2c illustrate the functions of each of the chips in the *GCK131 Chip Set.*

- The *GC131 Peripheral Controller* block diagram (Figure 2a) shows the range of services provided by this chip. The *GC131 Controller* is responsible for the AT controllers of the chip set supporting the system with INTERRUPT , TIMER , DMA/REFRESH , and I/O services.
  The input and output signals are described, in this document, in a later Section. (See ' *GC131—Pin Descriptions*'.)

- The *GC132 CPU/Memory Controller* block diagram (Figure 2b) shows the range of services provided by the chip. These services, which are used in the control of the CPU and memory, include: timing, synchronization, addressing, parity, bus conversion, and the AT bus module.
  The input and output signals are described, in this document, in a later Section. (See '*GC132—Pin Descriptions*'.)

- The *GC133 Bus Bridge Interface* block diagram (Figure 2c) shows the range of services provided by the chip. This chip, the simplest of the three, is essentially a buffer, latch, and comparitor. The main modules are: data buffer and bridge, page mode violation detection, memory address multiplexer, and address latch.
  The input and output signals are described, in this document, in a later Section. (See '*GC133—Pin Descriptions*'.)

Programmable configuration registers in each chip.
In each of the block diagrams a configuration module is shown. Configuration, as explained in the *Configuration Register* section, allows the chip set and the 80386-based AT system to be used in a variety of applications.

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1 - 1 GC131 Peripheral Controller, Block Diagram

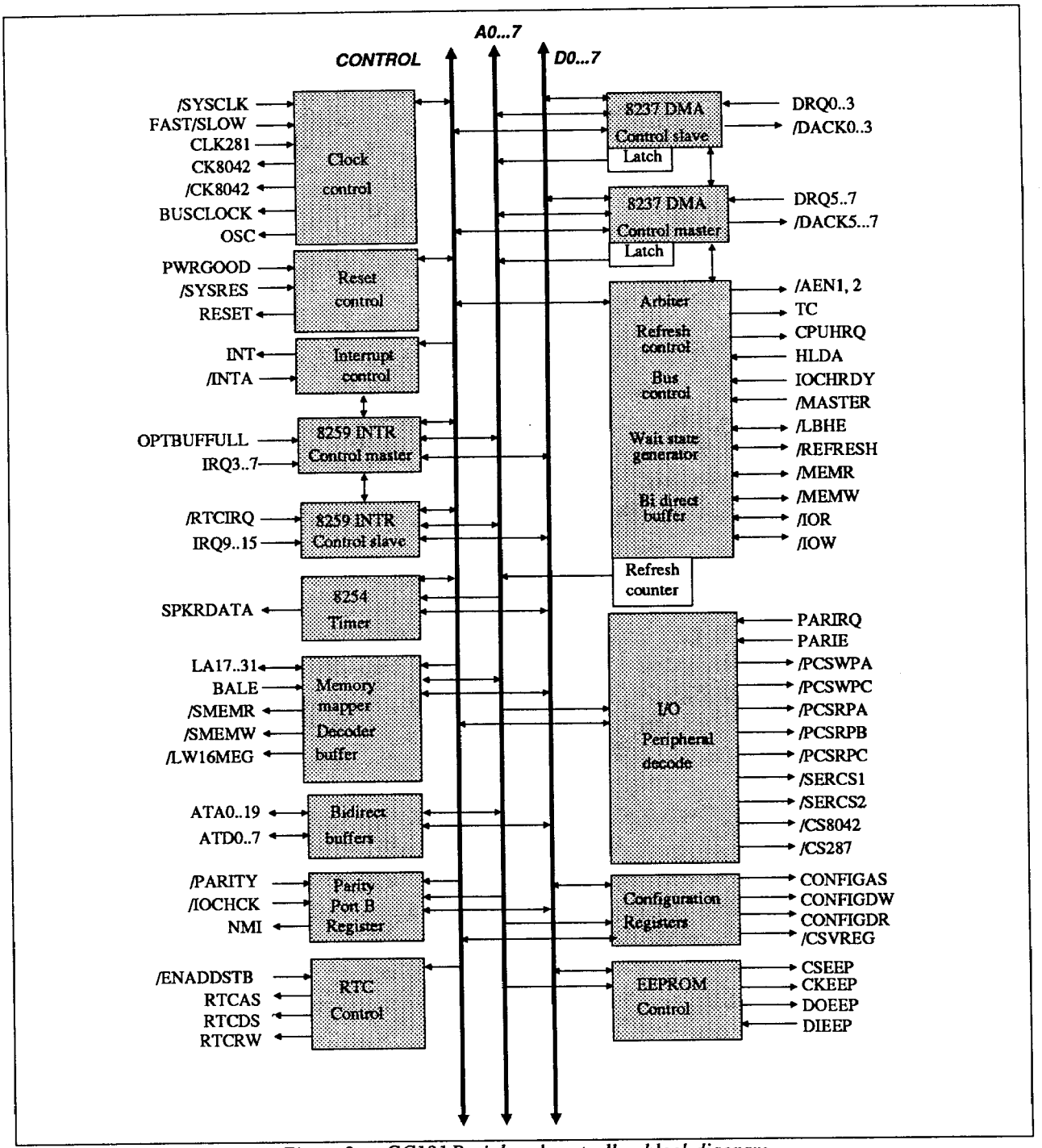


Figure 2a—GC131 Peripheral controller, block diagram

1 - 2 GC132 CPU/Memory Controller, Block Diagram

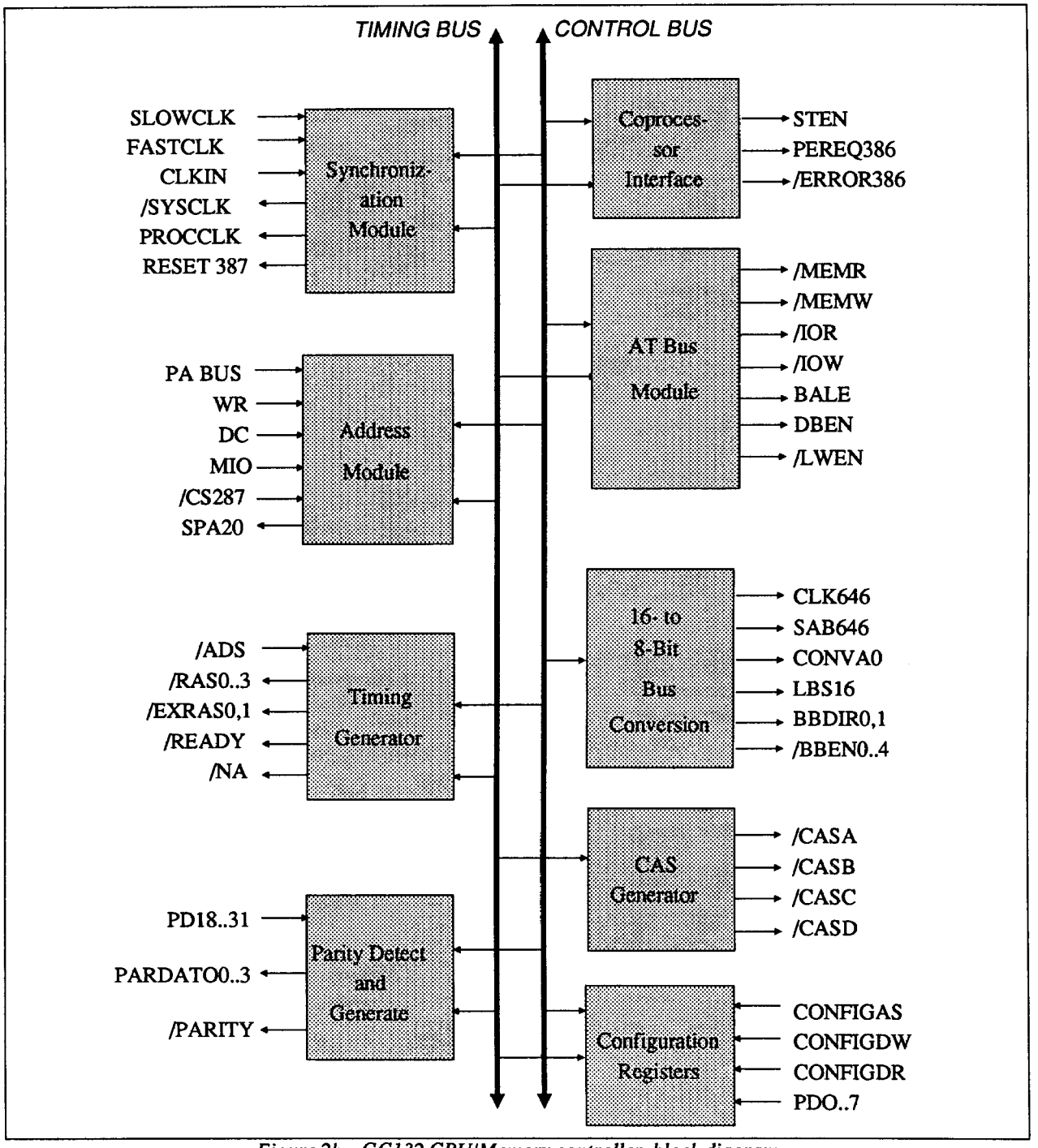


Figure 2b—GC132 CPU/Memory controller, block diagram

1 - 3 GC133 Bus Bridge Controller, Block Diagram

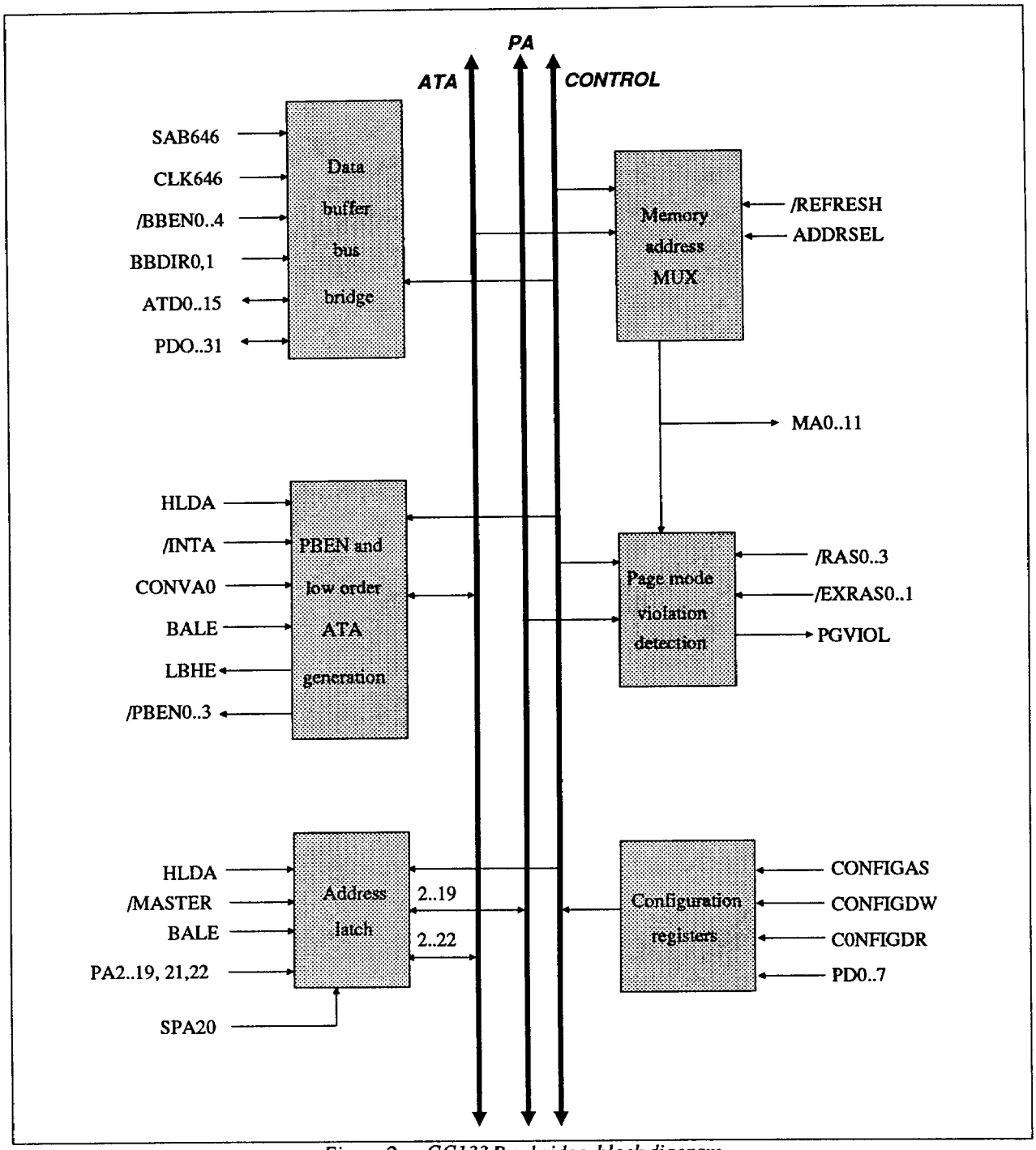


Figure 2c—GC133 Bus bridge, block diagram

Section - 2 Installing the GCK131 Chip Set

This Section of the *GCK131 Chip Set Data Sheet* includes:

Pinouts - *See Note(*)*

- *GC131 Peripheral Controller - Pinouts*
- *GC132 CPU/Memory Controller - Pinouts*
- *GC133 Bus Bridge Interface - Pinouts*

Pin Descriptions

- *GC131 Peripheral Controller - Pin Descriptions*
- *GC132 CPU/Memory Controller - Pin Descriptions*
- *GC133 Bus Bridge Interface - Pin Descriptions*

(*) Note:
Mechanical specifications. *The chips of the GCK131 Chip Set are packaged in 160-pin, plastic flat packs fitted with gull-wing connectors. Details of the physical characteristics of this package will be found later, in the Specifications Section of this Data Sheet.*
Electrical specifications. *Details of the electrical characteristics of each pin will be found in the Specifications Section.*

2 - 1 GC131 Peripheral Controller - Pinouts

Pinouts and Pin Descriptions

The pin connections for the *GC131 Peripheral Controller* are shown in Figure 3a. The pins are numbered sequentially in a counter clockwise direction from the index mark as viewed from the top of the chip.

Each pin, in a listing by pin names, is described in detail within the next few pages of this document. Electrical and mechanical specifications are listed in a later section.

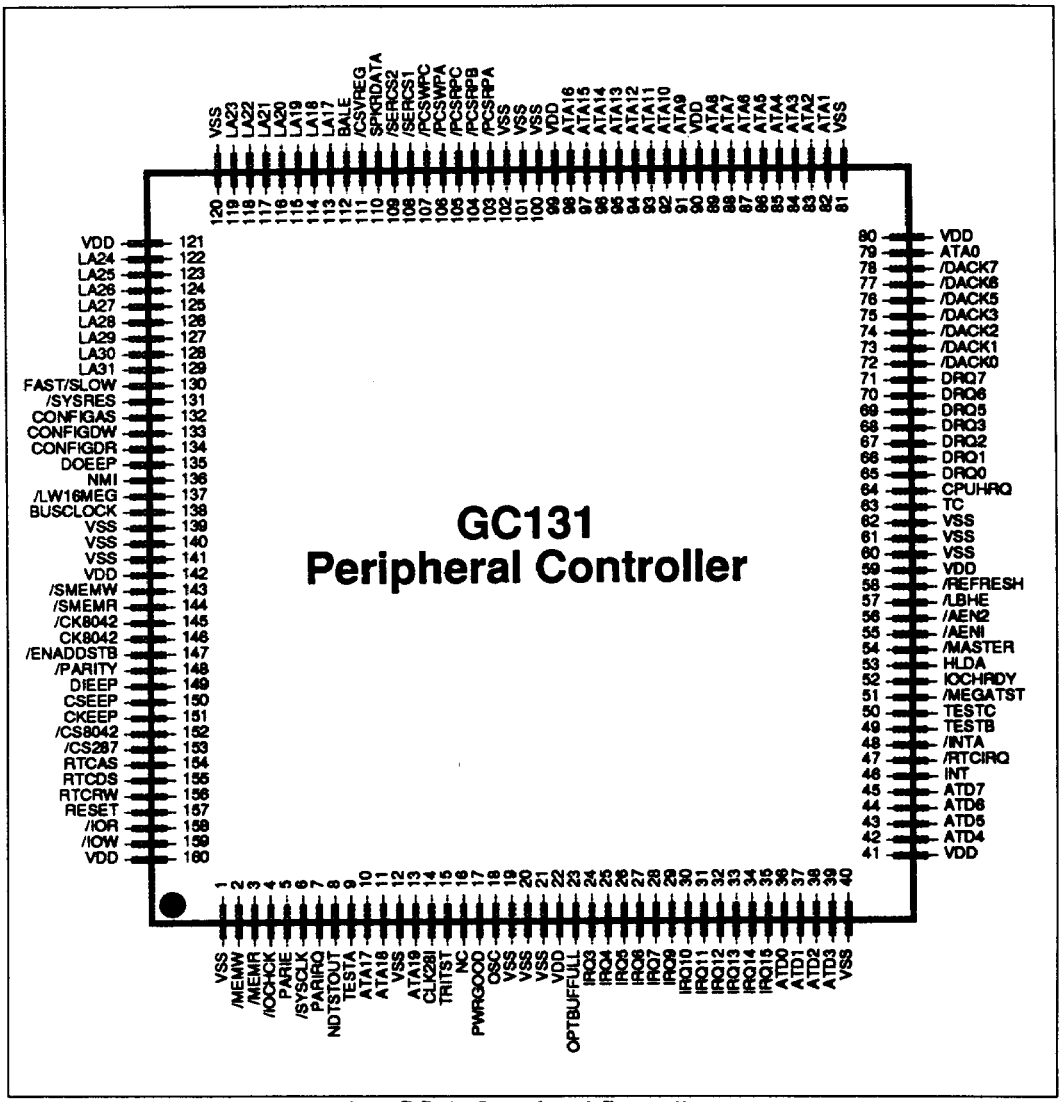


Figure 3a—GC131 Peripheral Controller, pinouts

2 - 2 GC132 CPU/Memory Controller—Pinouts

The pin connections for the *GC132 CPU/Memory Controller* are shown in Figure 3b. The pins are numbered sequentially in a counter clockwise direction from the index mark as viewed from the top of the chip.

Each pin is described in detail within the next few pages of this document. Electrical and mechanical specifications are listed in a later section.

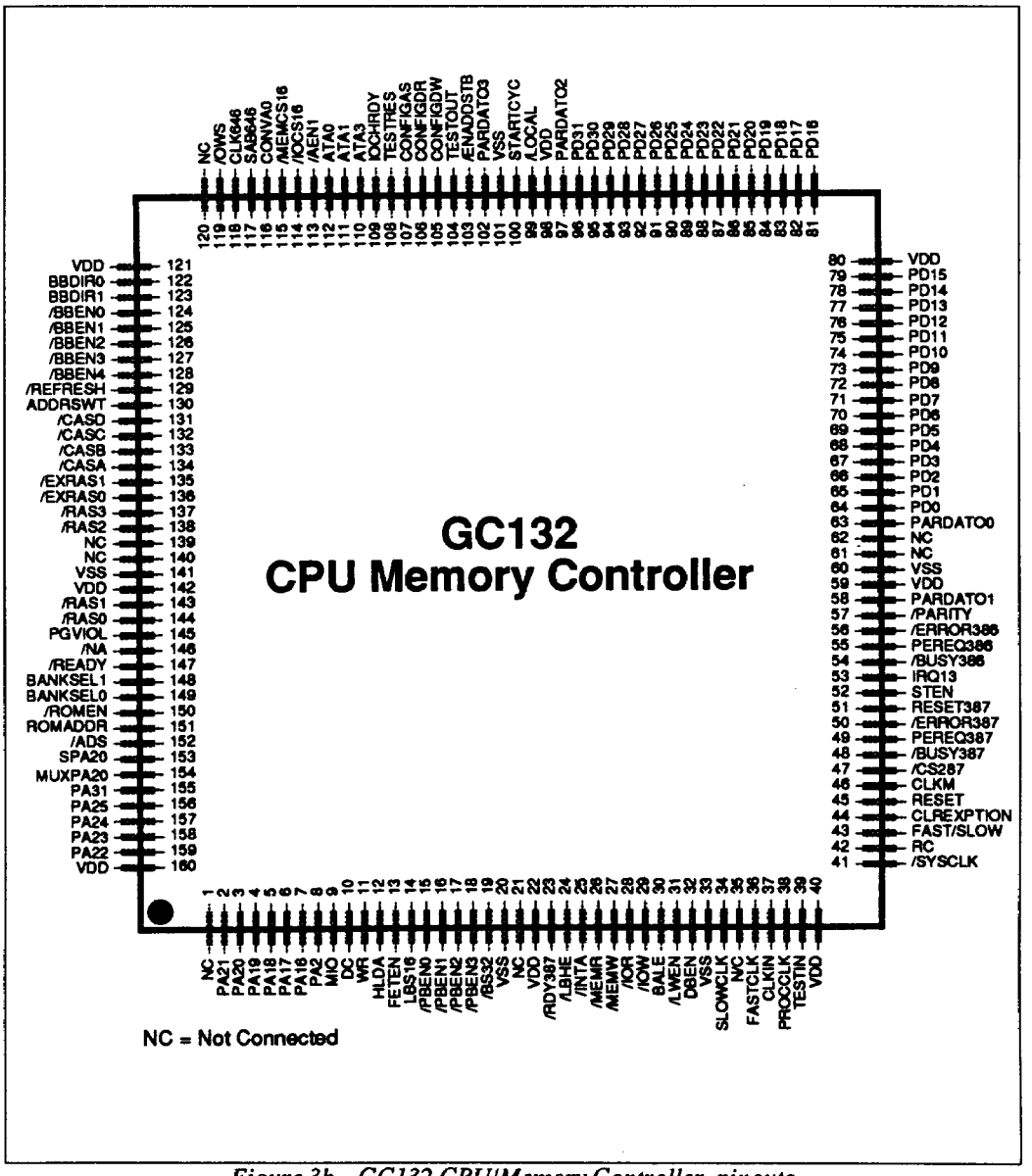


Figure 3b—GC132 CPU/Memory Controller, pinouts

2 - 3 GC133 Bus Bridge Interface—Pinouts

Pinouts and Pin Descriptions

The pin connections for the *GC133 Bus Bridge* are shown in Figure 3c. The pins are numbered sequentially in a counter clockwise direction from the index mark as viewed from the top of the chip.

A description of each pin follows in the next few pages of this document. Electrical and mechanical specifications are listed in a later section.

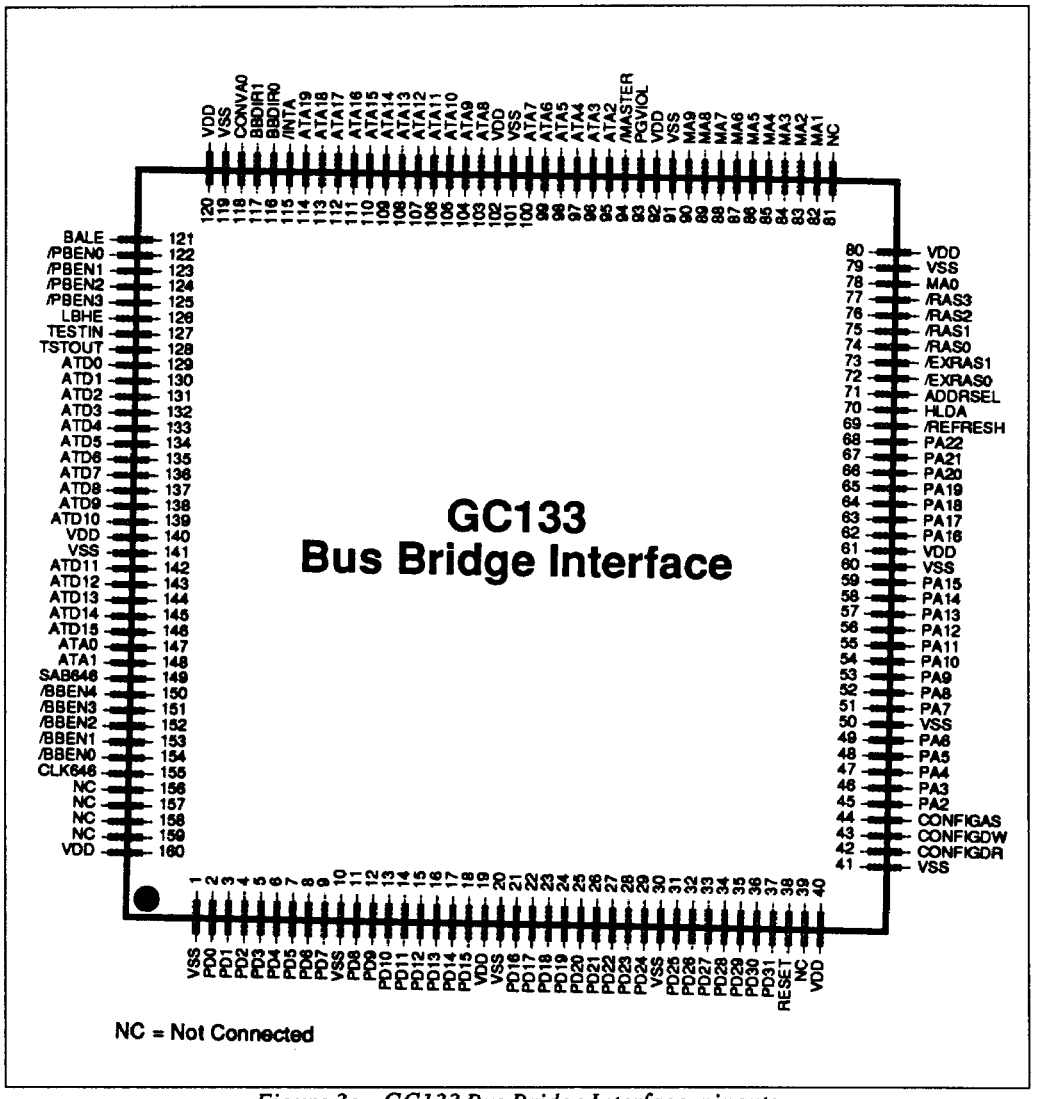


Figure 3c—GC133 Bus Bridge Interface, pinouts

2 - 4 GC131 Peripheral Controller Pin Descriptions

The following Figures (numbered 4a through 4g) describe the pins of the *GC131 Peripheral Controller*. The pin identification numbers correspond with those shown in *Figure 3a—GC131 Peripheral Controller, pinouts.*

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
/AEN1	55	*GC132*	O	**Address Enable** (DMA Controller—1). When active /AEN1 indicates that the system is performing an 8-bit DMA transaction.
/AEN2	56	NC	O	**Address Enable** DMA Controller—2). When active /AEN2 indicates that the system is performing a 16-bit DMA transaction.
ATA0 to ATA16	79, 82-89, 91-98	Backplane	I/O	**Latched AT Address** bus: Used for memory and I/O devices. These addresses are gated from the system bus when BALE is set HIGH , and are latched on the falling edge of BALE. These signals are generated by the CPU or DMA controller (in the *GC131*), or may be driven by an external bus master on the I/O channel.
ATA17 to ATA19	10, 11, 13	Backplane	O	**AT address** lines. These lines are driven only during DMA and Refresh cycles and represent a copy of LA 17 to LA 19.
ATD0 to ATD7	36-39, 42-45	Backplane	I/O	**AT Data** bus, LOW byte. The *GC131* uses only 8-bit transfers for accessing its internal registers.
BALE	112	*GC132*	I	**Buffered Address Latch Enable:** Connects with the *GC132* 'BALE' line. Used to latch valid addresses and memory decodes from the CPU. It indicates valid CPU or DMA address for the I/O channel. BALE is HIGH during 'Hold Acknowledge DMA', 'Refresh', or 'Master' cycles.
BUSCLOCK	138	Backplane	O	**Bus Clock** drives the backplane clock signal whose frequency is divided by the value set in the configuration register and output on this line. *(See* 'INDEX *40h' and* 'INDEX *41h'*)
CK8042	146	Keyboard controller	O	**Clock Driver Phase 1** (Frequency = 7.16 MHz): Connects with the Keyboard Controller clock input. The signal on pin CLK281 is divided by four.
/CK8042	145	Keyboard controller	O	**Clock Driver Phase 2**: 180 degrees out of phase with CK8042.
CKEEP	151	EEPROM	O	**Clock for EEPROM** (NVRAM).

Figure 4a—Pin Description, GC131 Peripheral Controller

GC131 Peripheral Controller Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
CLK28I	14	XTAL	I	**Clock 28 In** (Frequency = 28.6363MHz): At twice the Backplane OSC frequency the oscillator is used to drive the internal timers and the Keyboard Controller oscillator.
CONFIGAS	132	*GC132, GC133*	O	**Configuration Registers Address Strobe**: On the trailing edge of this signal, data is latched into the *GC131, GC132* and *GC133* index registers.
CONFIGDR	134	*GC132, GC133*	O	**Configuration Registers Data Read**: When active and selected by the INDEX value (within an appropriate range), one of the *GC131, GC132, GC133 Controllers* will output the indexed value onto the data bus.
CONFIGDW	133	*GC132, GC133*	O	**Configuration Registers Data Write**: When active and selected by the INDEX value (within an appropriate range), one of the *GC131, GC132* or *GC133 Controllers* will latch in the data to the indexed register on the trailing edge of this signal.
CPUHRQ	64	80386	O	**CPU Hold Request**: Connects with the 80386 Microprocessor HOLD pin.
/CS287	153	*GC132*	O	**Chip Select for 80287/ 80387**: When active /CS287 indicates that the processor is accessing the coprocessor I/O in the range F0h to FFh.
/CS8042	152	Keyboard controller	O	**Chip select** for the 8042 Keyboard Controller.
CSEEP	150	EEPROM	O	Chip Select for EEPROM (NVRAM): Used to save the last selected configuration register values.
/CSVREG	111	Video board	O	**Video Configuration Register Write** strobe. (See *'Index Address 44h'*).
/DACK0 to /DACK3, /DACK5 to /DACK7	72 - 78	Backplane	O	**DMAAcknowledge**: When active, indicates that the device requesting DMA now has service and can remove the DRQ.
DIEEP	149	EEPROM	I	**Data Input for EEPROM** (NVRAM): Connects directly with the EEPROM 'data out' line.
DOEEP	135	EEPROM	O	**Data Output for the EEPROM** (NVRAM).

Figure 4b—Pin Descriptions, GC131 Peripheral Controller

GC131 Peripheral Controller Pin Descriptions (Continued)

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
DRQ0 to DRQ3, DRQ5 to DRQ7	65-71	Backplane	I	**DMA Requests**: Priorities decrease from DRQ0 to DRQ7. A request is generated by driving a 'DRQ' line HIGH until the corresponding '/DACK' line goes LOW. DRQ 0 to DRQ 3 perform 8-bit transfers, and DRQ 5 to DRQ 7 perform 16-bit transfers.
/ENADDSTB	147	*GC132*	I	**Enable Address Strobe on the Real-Time Clock**: When active it prevents any accesses to or from the Real Time Clock.
FAST/SLOW	130	Keyboard controller	I	**Fast/Slow clock speed select** from 8042 Keyboard Controller. SLOW indicates a 7 MHz clock speed, and FAST indicates 25 MHz or 16 MHz.
HLDA	53	80386	I	**HoldAcknowledge**: Indicates that the CPU is no longer driving the buses. Used in the DMA controller section.
INT	46	80386	O	**Interrupt Request** to the CPU, from the 8259 Interrupt controller in the *GC131 Controller*.
/INTA	48	*GC132*	I	Interrupt acknowledge: Decoded from 'CPU STATUS' by the *GC132 Controller*, /INTA instructs the *GC131 Controller* to place the interrupt vector (to the CPU) on the system data bus.
/IOCHCK	4	Backplane	I	I/O Channel Check: When active, indicates that a fatal system PARITY error has occurred on a backplane memory board.
IOCHRDY	52	Backplane	I	**I/O Channel ready**: When LOW the current cycle is extended (in multiples of the CLOCK signal) until IOCHRDY is released. IOCHRDY will extend 'CPU', 'DMA', and 'Refresh' cycles.
/IOR	158	*GC132*	I/O	**I/O Read**: Normally an input, except during a DMA but not a MASTER, it is driven by the DMA Controller.
/IOW	159	*GC132*	I/O	**I/O Write**: Normally an input, except during a DMA but not a MASTER, it is driven by the DMA controller.

Figure 4c—Pin Descriptions, GC131 Peripheral Controller

GC131 Peripheral Controller Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
IRQ3 to IRQ7, IRQ9 to IRQ15	24-35	Backplane	I	**Interrupt Requests**: Interrupts from the I/O channel, indicate that an external peripheral on the backplane is requesting service by the CPU. These inputs are used by the 8259 Interrupt Controller in the *GC131 Controller*. Priorities decrease from IRQ9 to IRQ15, and then from IRQ3 down to IRQ7. An interrupt request is generated on the rising edge of an 'IRQ' line—which must be held HIGH until acknowledged by the interrupt service routine.
LA17 to LA31	113 to 119, and 122 to 129	Backplane	I/O	**I/O Buffered (unlatched) Processor Address bus:** Used for memory and I/O devices. LA17 to LA23 are used in AT implementation, to provide addressing up to 16 Mb. They are valid only when BALE is HIGH. These signals are generated by the CPU or the DMA controller (in the *GC131 Controller)*, or they may be driven by an external bus master on the I/O channel. In the AT implementation, the unused addresses (LA24 through LA31) must be connected through resistors to ground.
/LBHE	57	*GC133*	I/O	**Bus High Enable**: When active /LBHE indicates that data is valid on the upper half of the AT data bus. Normally this signal is an input—except during DMA when it is driven by the DMA controller; but, during MASTER cycles, /LBHE is driven from the backplane and is therefore an input.
/LW16MEG	137	Backplane	O	**Lower 16 Mb Address**: Not used in the AT implementation. Indicates address is in lower 16 Mb.
/MASTER	54	Backplane	I	**Master Mode request**: When active the peripheral device on the backplane is requesting that it become the SYSTEM MASTER, where it will drive the 'address', 'command', 'refresh' and 'data' lines. The device may drive /REFRESH to request a refresh cycle.
/MEGATST	51		I	**Factory test pin**: Normally connected to VDD.
/MEMR	3	*GC132*	I/O	**Memory Read**: Normally an input—except during DMA when the DMA controller will drive it—this signal is generated by the *GC132 Controller* (for CPU bus cycles), by the *GC131 Controller* (for DMA cycles), or by an external bus master on the I/O channel. It is also generated by the *GC131 Controller* for refresh cycles.

Figure 4d—Pin Description, GC131 Peripheral Controller

GC131 Peripheral Controller Pin Descriptions (Continued)

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
/MEMW	2	GC132	I/O	**MemoryWrite:** Normally an input—except during DMA when the DMA controller will drive it—this signal is generated by the *GC132 Controller* (for CPU bus cycles), by the *GC131 Controller* (for DMA cycles), or by an external bus master on the I/O channel.
NDTSTOUT	8	Test output	O	**Factory test pin,** normally left unconnected.
NMI	136	80386	O	**Non-Maskable Interrupt** to the 80386: A request to the CPU for immediate service. This signal is generated by /PARITY or /IOCHCK. It is enabled by bit 7 of the NMI Mask register. /PARITY and /IOCHCK are individually enabled by bits in the Port B register of the *GC131 Controller*.
OSC	18	Backplane	O	**Oscillator** (Frequency = 14.31818 MHz): Four-times the color-burst frequency to the backplane.
OPTBUFFULL	23	Keyboard controller	I	**Keyboard Output Buffer Full:** Interrupt request from the 8042 Keyboard Controller. This is used as IRQ 1 to the 8259 Interrupt Controller in the *GC131 Controller*.
PARIE	5	External logic	I	**Parallel Port Interrupt Enable** from the printer control register implemented on the system board.
PARIRQ	7	External logic	I	**Parallel Port Interrupt Request** from a printer. A configuration register *(See 'INDEX 43h')* allows enabling and the direction of this interrupt to either IRQ 7 (for Port 1) or IRQ5 (for Port 2).
/PARITY	148	*GC132*	I	**Memory Parity Error** from *GC132*, sampled 1 '/SYSCLOCK' cycle after the MEMR command.
/PCSRPA	103	Parallel port	O	**Parallel Port Printer Data Read** strobe.
/PCSRPB	104	Parallel port	O	**Parallel Port Printer Status Read** strobe.
/PCSRPC	105	Parallel port	O	**Parallel Port Printer Control Register Read** strobe.
/PCSWPA	106	Parallel port	O	**Parallel Port Printer Data Write** strobe.
/PCSWPC	107	Parallel port	O	**Parallel port Printer Control Register Write** strobe.

Figure 4e—Pin Descriptions, GC131 Peripheral Controller

GC131 Peripheral Controller Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
PWRGOOD	17	Power supply	I	**Power good:** Indicates that the power levels are ready and stable. The machine is held in 'reset' until PWRGOOD is active. This signal must become active before RESET goes inactive.
/REFRESH	58	Backplane	I/O	**Refresh cycle for DRAMs:** Indicates the DMA cycle is actually a 'refresh' cycle.
RESET	157	Everywhere	O	**System reset:** When active the system is in a 'reset' state.
RTCAS	154	RTC	O	**Real-Time Clock Address Write** strobe.
RTCDS	155	RTC	O	**Real-Time Clock Data Read** strobe.
/RTCIRQ	47	RTC	I	**Real-Time Clock Interrupt Request:** Used as /IRQ8 to the Interrupt Controller in the *GC131 Controller*. It is active LOW.
RTCRW	156	RTC	O	**Real-Time Clock Data Read/Write** strobe.
/SERCS1	108	Serial port	O	**Chip Select for Serial Port 1:** Implemented on the system board.
/SERCS2	109	Serial port	O	**Chip Select for Serial Port 2:** Implemented on the system board.
/SMEMR	144	Backplane	O	**Memory Read** command for addresses within the low 1 MByte provided for the I/O channel.
/SMEMW	143	Backplane	O	**Memory Write** command for addresses within the low 1 MByte provided for the I/O channel.
SPKRDATA	110	Speaker	O	**Speaker Output** signal to a transistor driving a speaker. It is generated by Counter 2 of the 8254 Timer function and gated by bit 1 of Port B register in the *GC131 Controller*.
/SYSCLK	6	*GC132*	I	**Main GC131 System Clock:** Connects with the *GC132Controller's* /SYSCLK. The '/SYSCLK' frequency is half that of the CPU 'CLK2'.
/SYSRES	GC131	External logic	I	**System reset:** Derived from VCC and the RESET pushbutton. /SYSRES is LOW while VCC is LOW, or while the pushbutton is pressed, and goes HIGH after a debounce period. The debounce period should not end while PWRGOOD is still LOW.

Figure 4f—Pin Descriptions, GC131 Peripheral Controller

GC131 Peripheral Controller Pin Descriptions (Continued)

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
TC	63	Backplane	O	**Terminal Count** from the DMA controllers in the *GC131 Controller* to the device on the I/O channel that is doing the current DMA cycle—indicating that this is the last transfer for this DMA channel.
TESTA	9	Ground	I	**Factory test pin**, normally connected to Ground.
TESTB	49	Ground	I	**Factory test pin**, normally connected to Ground.
TESTC	50	Ground	I	**Factory test pin**, normally connected to Ground.
TRITST	15	Ground	I	**Factory test pin**, normally connected to Ground.
VDD	22,41, 59,80, 90,99, 121,142, 160	PWR		**+5 volts**
VSS	1, 12, 19, 20,21, 40,60, 61,62, 81,100, 101,102, 120,139, 140 141			Ground

Figure 4g—Pin Descriptions, GC131 Peripheral Controller

2 - 5 GC132 CPU/Memory Controller Pin Descriptions

Pinouts and Pin Descriptions

The following Figures (numbered 5a through 5g) describe the pins of the *GC132 CPU/Memory Controller*. The pin identification numbers correspond with those shown in *Figure 3b—Pinouts, GC132 CPU/Memory Controller*.

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
ADDRSWT	130	*GC133*	O	**Address Select**: Selects either row or column addresses.
/ADS	152	80386	I	**Address strobe**: This marks the beginning of the current cycle. Indicates when status and addresses are valid.
/AEN1	113	*GC131*	I	**Address Enable**: Active during DMA but not during a MASTER access. Indicates 8 bit DMA access.
ATA0, ATA1, ATA3	112, 111, 110	*GC133*	I	**AT Backplane Address A0, A1, A3.**
BALE	30	*GC133*	O	**Buffered Address Latch Enable**: When HIGH the addresses are transparent between the processor side to the backplane side. On the falling edge the addresses are latched and held until another BALE.
BANKSEL0 BANKSEL1	149, 148	CAS Steering Logic	O	**Demultiplexer Select** specifies which bank is to receive the CAS strobes.
/BBEN0 to /BBEN4	124, 128	*GC133*	O	**Bus Bridge Data Enable:** BBEN 0-3 enable the data buffers between the processor and the backplane. One signal per byte. BBEN 4 enables the buffer between the upper and lower bytes on the 16 bit backplane bus.
BBDIR0 BBDIR1	122 123	*GC133*		**Bus Bridge Direction Indicators:** BBDIR 0 turns the direction of the buffer between ATD 0-7 and ATD 8-15. When HIGH the buffer will drive from lower 8 bits to upper 8 bits. The BBDIR 1 signal indicates the data flow from processor to/from backplane. When HIGH the data will flow from the processor to the backplane, when LOW vice versa.
/BS32	19	External logic	I	**Bus Size 32-bits**: When LOW, this signal indicates that the current cycle is intended for local 32-bit access: LBS16 is inactive and /BBENs are in the OFF condition. (*See also* FETEN)

Figure 5a—Pin Descriptions, GC132 CPU/Memory Controller

GC132 CPU/Memory Controller Pin Descriptions (Continued)

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
/BUSY386	54	80386	O	**Busy 386**: Connects to the 'BUSY' line of the 80386.
/BUSY387	48	80387	I	**Busy 387** Connects to the 'BUSY' line on the 80387.
/CASA to /CASD	134 to 131	DRAM	O	**Column Address Timing Strobe** for the 4 bytes. These signals must be steered to the correct bank using BANKSEL or external logic for banks 4 and 5.
CLK646	118	*GC133*	O	**Clock** the LS646 megafunction in the *GC133*: The rising edge latches the data presented on the lower 8 bits of the backplane. This is used on an 8 to 16 bit read conversion cycle.
CLKIN	37	80386 PROC-CLK	I	**Clock**: This clock drives the entire chip on the rising edge. This clock is the same as used by the 80386 Microprocessor.
CLKM	46	80387	O	**Clocking Mode**: when LOW it selects the asynchronous clocking mode of the 80387, when HIGH , the synchronous mode. (*See* 'INDEX *01h*')
CLREXPTION	44	80386	O	**Clear exception**: Connects to the RESET of the 80386. This is a synchronous reset.
CONFIGAS	107	*GC131*	I	**Configuration Register Address Strobe**: The configuration register index is strobed in on the falling edge of this signal from the data bus LD0-7. Results from an IOW to address 024h.
CONFIGDR	106	*GC131*	I	**Configuration Register Data Read**: Data is read from the configuration register addresses by the value written in by the CONFIGAS pulse. This results from an IOR from address 028h.
CONFIGDW	105	*GC131*	I	**Configuration Register Data Write**: Data is written on the falling edge into the register addressed by the Index latched in by CONFIGAS .
CONVA O	116	*GC131*	O	**Conversion Address 0**: During an 8- to 16-bit conversion cycle, the 'address 0' line must be forced to a '1' during the second half. This signal tells the GC133 when to force A0 to A1 on the backplane.
/CS287	47	*GC131*	I	**Chip Select 287 (coprocessor)**. When LOW the processor is addressing an I/O location between F0h-FFh.

Figure 5b—Pin Descriptions, GC132 CPU/Memory Controller

GC132 CPU/Memory Controller Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
DBEN	32	/BBEN0-4 Control	O	**Data Bus Enable**: when LOW, the local bus is expecting data from the *GC133*, when HIGH the *GC133* should not put data onto the local bus.
DC	10	80386	I	**Data or Control**: Status line from 80386.
/ENADDSTB	103	*GC131*	O	**Enable Address Strobe**: when LOW the *GC131* disables any access to the Real Time Clock. This signal is LOW from reset to the first processor access.
/ERROR386	56	80386	O	**Error (Coprocessor)**: Signals the processor that an error has occurred in the coprocessor
/ERROR387	50	80387	I	**ERROR** line from the 80387.
/EXRAS0, /EXRAS1	136, 135	DRAM	O	**Row Address Strobes** for BANKS 4 and 5.
FASTCLK	36	XTAL	I	**Main Oscillator Clock**: between 32 and 50 MHz.
FAST/SLOW	43	8742	I	**Speed switch**: when HIGH the output of the clock synchronization circuit (PROCCLK) is a buffered version of the FASTCLK input, when LOW the PROCCLK signal is a buffered version of the SLOWCLK input. This signal comes from the 8042.
FETEN	13	VCC/Ground	I	**Feature Enable**: When HIGH the features associated with pins /BS32, STARTCYC, and /LOCAL are enabled.
HLDA	12	80386	I	**HoldAcknowledge**: when HIGH the processor has relinquished the address, data and status bus, when LOW the 80386 is the bus master.
/INTA	25	*GC131*	O	**InterruptAcknowledge**: indicates that the interrupt vector should be read into the processor.
IOCHRDY	109	Backplane	I	**I/O Channel Ready**: A signal from the AT backplane requesting additional command active time. When LOW the chip will add any number of wait states until the signal is released.
/IOCS16	114	Backplane	I	**I/O Chip Select** is 16 bits: When asserted by a 16 bit device on the AT backplane, the chip will not perform a 8 to 16 bit conversion cycle. If it is inactive the *GC132* will assume the I/O cycle is to an 8 bit device. (NOTE: this signal refers to the device responding to the cycle, not the cycle itself.)

Figure 5c—Pin Descriptions, GC132 CPU/Memory Controller

GC132 CPU/Memory Controller Pin Descriptions (Continued)

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
/IOR	28	Backplane	I/O	**I/O Read:** normally an output, see the output pin definitions, but during DMA or MASTER mode, it becomes in input driven by the DMA controller.
/IOW	29	Backplane	I/O	**I/O Write:** normally an output, (See the *Pin Definitions*), but during DMA or MASTER mode, it becomes an input driven by the DMA controller.
IRQ13	53	*GC131*	O	**Interrupt Request 13:** when HIGH the coprocessor has detected an exception and has raised an interrupt.
/LBHE	24	GC133	I	**Latched Bus HIGH Enable In:** Indicates when the upper 8 data bits of the 16 bit backplane is active.
LBS16	14	80386	O	**Latched Bus Size 16:** when active the *GC132* is signalling the processor that the current cycle is inappropriate for 16 bit backplane operations, and the processor will adjust its cycle or issue another.
/LOCAL	99		O	**Local Bus Access:** When LOW indicates that the current cycle is used for local bus access and not for the backplane. (*See also* FETEN .)
/LWEN	31	DRAM	O	**Latched Write Enable:** When active the current cycle is a write. A latched version of (WR). Used to indicate a write operation to the DRAM s.
/MEMCS16	115	Backplane	I	**Memory Chip Select is 16 bits:** indicates that the current cycle is addressing a 16 bit memory device and the *GC132 Controller* will not perform an 8 to 16 bit conversion cycle.
/MEMR	26	*GC131*	I/O	**Memory Read:** Normally an output, but during a DMA or MASTER mode cycle, it becomes an input and is used for determining the direction and duration of the *GC133 Bus Bridge* buffers.
/MEMW	27	*GC131*	I/O	**Memory Write:** Normally an output, but during a DMA or MASTER mode cycle, it becomes an input and is used for determining the direction and duration of the *GC133 Bus Bridge* buffers.
MIO	9	80386	I	**Memory or I/O status line** from the 80386.

Figure 5d—Pin Descriptions, GC132 CPU/Memory Controller

GC132 CPU/Memory Controller Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
MUXPA20	154	8742	I	**Multiplex Processor Address 20**: When LOW the output SPA20 follows PA20 exactly. When HIGH SPA20 is forced LOW.
/NA	146	80386	O	**Next Address**: when active the *GC132* is requesting that the next cycles address and ADS be issued.
/OWS	119	Backplane	I	**0 Wait State**
PA2	8	80386	I	**Processor Address line 2**: Used to determine which bank of DRAM will be interleaved next.
PA16 to PA25	7-2, 159-156	80386		**Processor Address lines 16 through 25**: Used for memory map control.
PA31	155	80386	I	**Processor Address line 31**: Used for coprocessor interface and the restart vector.
PARDATO 0 to PARDATO 3	63, 58, 97, 102	DRAM	I/O	**Parity Data Out 0 through 3**: During a memory read these pins are inputs which contain the parity data bit from the DRAM. These will be checked against a calculated version based on the LD0-31 lines. If there is an error the /PARITY signal will go active in the next bus cycle. During a memory write, these lines are outputs containing the calculated parity for each byte.
/PARITY	57	*GC131*	O	**PARITYCheck**: when active at the end of a memory read cycle it indicates a parity error on the DRAM.
/PBEN0 to /PBEN3	15-18	80386	I	**Processor Byte Enable**: Indicates which of the four processor data bytes has valid data.
PD0 to PD7	64-71	DRAM	I/O	**Processor or DRAM data lines**: lower 8 bits are actually bi-directional. They are inputs during a configuration register write or a memory read for parity generation.
PD8 to PD31	72-79, 81-96	DRAM	I	**DRAM data lines**: Always inputs, used for calculating parity during memory reads.
PEREQ386	55	80386	O	**Processor Extension Request**: Connected to the 80386 'PEREQ' line.

Figure 5e—Pin Descriptions, GC132 CPU/Memory Controller

GC132 CPU/Memory Controller Pin Descriptions (Continued)

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
PEREQ387	49	80387	O	**Processor Extension Request**: Connects to the 'PEREQ ' line of the 80387.
PGVIOL	145	*GC133*	I	**Page Violation**: During a memory operation the *GC133* will constantly compare the current DRAM page strobed in by the RAS signal with the current page presented by the processor for the next cycle. If the two pages are different this signal will go active.
PROCCLK	38	80386	O	**Processor Clock**: The main clock that drives the 80386, 80387 or 80385. This signal can be buffered or even inverted since the *GC132 Controller* does not use this clock: CLKIN is used to drive the internal state machines.
/RAS0 to /RAS3	144,143, 137,138	DRAM	O	**Row Address Strobe**: for the DRAM s.
RC	42	8742	I	**Processor Reset**: when active the 8742 keyboard controller is requesting that the CPU be reset but NOT the system.
/RDY387	23	80387	I	**Ready** (from the 80387: when LOW the 80387 is terminating its cycle.
/READY	147	80386	O	**Ready** (to the 80386): terminates the cycle.
/REFRESH	129	*GC131*	I	**REFRESH**: indicates that the current DMA cycle is a refresh operation and the *GC132* will not produce a CAS signal, just a RAS.
RESET	45	GC131	I	**RESET** (System): when active the CPU and the entire system will be reset.
RESET387	51	80387	O	**RESET** (80387): A synchronous reset to the 80387.
ROMADDR	151	EPROM	O	**HIGH ROM** Address: connects to A16 on a 27512 or VPP on a 27256. When the configuration bit is set for 27512 usage, this line will follow a latched version of PA16, when set for a EPROM 27256, it will remain at VDD.
/ROMEN	150	EPROM	O	**EPROM Enable**: Connects to the OE of the EPROM. It indicates when the device should drive the data bus.

Figure 5f—Pin Descriptions, GC132 CPU/Memory Controller

GC132 CPU/Memory Controller Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
SAB646	117	*GC133*	O	**Select Latched or Transparent data:** When LOW the *GC133* will (on a READ) allow uninhibited data flow from the backplane to the processor local bus. When HIGH the *GC133* will present the data latched by CLK646 to the lower byte on the local data bus. This is used during an 8 to 16 bit read conversion cycle.
SLOWCLK	34	*GC131*	I	**SLOW System Clock** (Frequency = 14.318 MHz): Used for the system clock during slow speed (FAST/SLOW is LOW).
SPA20	153	*GC133*	I/O	**Switched Processor Address 20:** Normally this signal is an output which follows PA20 (except when MUXPA 20 is HIGH), but during a DMA or MASTER mode, SPA20 is the Address line 20 input.
STARTCYC	100		O	**Start a DRAM cycle:** Useful when implementing a memory sub-system external to the *GC132*, this signal indicates the start of a DRAM cycle. Defined as RAS and /CAS, this signal helps with the problem of knowing when to initiate a /CAS precharge during a page mode cycle. (*See also* FETEN .)
STEN	52	80387	O	**Connects to the STEN** line on the 80387.
/SYSCLK	41	*GC131*	O	**System Clock:** Main clock for the *GC131*, equivalent to CLKIN divided by 2.
TESTIN	39	Ground	I	**Test Mode Enable:** Used for fault coverage in the fabrication process. Not user applicable.
TESTOUT	104		O	**Factory test pin.** Normally not connected.
TESTRES	108	Ground	I	**TEST Reset:** Used for fault coverage in the fabrication process. Not user applicable.
WR	11	80386		**Write-Read:** Status line for the 80386.
VDD	22,40, 59,80, 98,121, 142,160			**+5 volts**
VSS	20,33, 60,101, 141			**Ground**

Figure 5g—Pin Descriptions, GC132 CPU/Memory Controller

2 - 6 GC133 Bus Bridge Interface Pin Descriptions

The following Figures (numbered 6a through 6d) describe the pins of the *GC133 Bus Bridge Interface*. The pin identification numbers correspond with those shown in *Figure 3c—Pinouts, GC133 Bus Bridge Interface*.

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
ADDRSEL	71	*GC132*	I	**Address Multiplexer Selector:** When LOW the *GC133* places ROW addresses on the MA lines, when HIGH the COLUMN addresses are on the MA lines.
ATA0 to ATA19	147 to 148 & 95 to 100 & 103 to 114	Backplane	I/O	**AT Backplane Address lines:** A latched version of the PA2 to PA16 lines.
ATD0 to ATD15	129 to 139 & 142 to 146	Backplane	I/O	**AT Backplane Data lines:** 16-bit data lines derived from the 32-bit processor data bus LD0-31. These lines drive the AT slots.
BALE	121	*GC132*	I	**Bus Address Latch Enable:** When HIGH the addresses from the processor side (PA's) are driven through to the AT side (ATA's). The trailing edge of BALE holds the current value of the address on the AT side allowing the processor addresses to change for pipeline operation.
BBDIR0, BBDIR1	116, 117	*GC132*	I	**Bus Bridge Direction 0:** Controls the direction of data for the bridging action between ATD 0-7 and ATD 8-15. When HIGH, data is bridged from lower to higher bytes on the AT side: when LOW, from upper to lower. **Bus Bridge Direction 1:** Controls the direction of data flow from the processor side to the AT side. When HIGH, data flows from the processor to the AT data bus. (During an I/O write BBDIR 1 = '1'.) When LOW, data flows from the AT side to the processor side. (During an I/O read BBDIR 1 = '0'.)

Figure 6a—Pin Descriptions, GC133 Bus Bridge Interface

GC133 Bus Bridge Interface Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
/BBEN0 to /BBEN3	154-151	*GC132*	I	**Bus Bridge Enable**: When active, indicates the byte that the *GC133* should drive—where BBEN0 is the lowest order byte and BBEN3 the highest. For example: an I/O byte READ from port 0 has BBEN0 active; *GC133* drives data onto the processor's data bus (lower byte) from the AT data bus (lower byte) 0.
/BBEN4	150	*GC132*	I	**Bus Bridge Enable 4**: When active, enables the bridging buffer between ATD0-7 and ATD8-15. This routes the data from lower to upper bytes on the AT data bus and visa versa.
CLK646	155	*GC132*	I	**Clock LS646 Megafunction**: On the rising edge of this signal, *GC133* latches data on lines ATD0-7 and, if the direction and SAB646 is correct, presents the data to the processor's lower 8 bits.
CONFIGAS	44	*GC131*	I	**Configuration Address Strobe**: The new configuration INDEX is strobed on the trailing edge of this signal.
CONFIGDR	42	*GC131*	I	**Configuration Data Read**: If the INDEX is set within the range **10h to 1Fh**, *GC133* will place the indexed register's value on the processor's data bus. If the range is set within **0h to 0Fh**, GC133 does not drive the processor data bus at all—INDEX indicates a value for the *GC132 Controller*. If the range is within **40h to 4Fh**, GC133 lets the data come in from the AT data bus—*GC131* is driving the bus.
CONFIGDW	43	*GC131*	I	**Configuration Data Write**: On the trailing edge of this signal, data on the processor's data bus is written to the indexed register (if within RANGE 10h to 1Fh).
CONVA0	118	*GC132*	I	**Conversion Cycle A0**: When this signal is active, *GC133* forces a '1' onto ATA0. This is used during 8- to 16-bit conversion cycles.
/EXRAS0 /EXRAS1	72, 73	*GC132*	I	**RAS signals for banks 4 and 5**: *GC133* uses these signals to latch the latest 'page value' for the DRAMs. Used in PGVIOL calculations.

Figure 6b—Pin Descriptions, GC133 Bus Bridge Interface

GC133 Bus Bridge Interface Pin Descriptions (Continued)

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
HLDA	70	80386	I	**HoldAcknowledge**: When the DMA controller or 'MASTER' holds the bus (and the processor has granted it) this signal is active. Controls the generation of A0, A1 & LBHE signals.
/INTA	115	*GC132*	I	**InterruptAcknowledge**: When active, *GC133* allows the interrupt vector flow from the AT data bus to the LOW byte on the processor bus.
LBHE	126	Backplane	I/O	**Latched Byte High Enable**: When active, indicates that valid data is on the high part of the 16-bit data lines.
MA0 to MA9	78, 82-90	DRAM	O	**Multiplexed addresses** (DRAMs).
/MASTER	94	Backplane	I	MASTER Mode Request: When active and in conjunction with DMA, indicates that a peripheral board (on the backplane) is driving 'address', 'commands', 'refresh', and 'data'.
PA2 to PA16	45-49, 51-59, 62.	80386	I	**Processor Address (Lower and Upper) lines 2-22**: These lines are latched to form the AT Address lines. They are used to generate the MA lines for the DRAM.
PA17 to PA22	63 to 68		I	
/PBEN0 to /PBEN3	122 to 125	80386	I/O	**Processor Byte Enables**: Indicates the byte on which there is valid data. Used to generate A0, LBHE and A1. Normally an input; but, during DMA is an output.
PD0 to PD31	2-9, 11-18, 21-29, 31-37	80386	I/O	**Processor Data Lines.**
PGVIOL	93	*GC132*	O	**Page Violation**: This signal is the result of a COMPARE of the current address 'row' and the 'row' latched into the DRAMs. When HIGH it indicates that the two are different—thus allowing the processor access beyond the page boundary.
/RAS0 to /RAS3	74 to 77	GC132	I	**Row Address Strobe**: *GC133* uses these signals to latch the latest 'page value' for the DRAMs. Used in PGVIOL calculations.

Figure 6c—Pin Descriptions, GC133 Bus Bridge Interface

GC133 Bus Bridge Interface Pin Descriptions (Continued)

Pinouts and Pin Descriptions

Pin Symbol	Pin Number	Source/ Destination	Pin Type	Description
/REFRESH	69	*GC131*	I	/REFRESH : Indicates that the current HLDA cycle is a DRAM refresh and the refresh addresses are on ATA 0-11.
RESET	38	*GC132*	I	**RESET**: Initializes all internal registers to a known value.
SAB646	149	*GC132*	I	**Select Transparent or Latched Data**: When LOW the *GC133 Bus Bridge* lets data flow from, transparently, the processor to the AT bus. When HIGH , *GC133 Bus Bridge* presents the latched data on the next memory READ .
TESTIN	127		I	**Factory test pin**: Not to be connected.
TSTOUT	128	Not connected	O	**Test Output**: Used for factory verification of chip integrity.
VDD	19,40, 61,80, 92,102, 120, 140,160			**+5 volts**
VSS	1,10,20, 30,41, 50,60, 79,91, 101,119, 141			**Ground**

Figure 6d—Pin Descriptions, GC133 Bus Bridge Interface

2 - 7 GC131 Peripheral controller, I/O devices

I/O Address Map

Address range	Device	Operation
0h - Fh	DMA controller 1 (8237), slave	Read/Write
20h - 21h	Interrupt controller 1 (8259), master	Read/Write
24h	Configuration register - Address	Write only
28h	Configuration register - Data	Read/Write
40h - 43h	Timer/Counter (8254)	Read/Write
60h, 64h	Keyboard Controller (8042)	Chip select
61h	Port B register, PPI (8255)	Read/Write
70h	Real-time Clock register - Address, NMI Mask Bit	Write only
71h	Real-time Clock register - Data	Read/Write
80h - 9Fh	DMA Memory Mapper (Page registers)	Read/Write
A0h - A1h	Interrupt controller, slave (8259)	Read/Write
C0 - CFh	DMA controller 2, master (8237)	Read/Write
E0h - FFh	Numeric Coprocessor (80287)	Chip select
278h - 27Fh	Parallel Port 2 (Printer)	Read/Write
2F8h - 2FFh	Serial Port 2	Chip select
378h - 37Fh	Parallel Port 1 (Printer)	Read/Write
3F8h - 3FFh	Serial Port	Chip select

Access to these devices is disabled for addresses above 1 Kb and during DMA operations.

Figure 6e—I/O Address map

Port B (8255) PPI register , Address 61h

Data written	
Bit 3 = 1	Disable NMI for IOCHCK (*).
Bit 2 = 1	Disable NMI for Memory PARITY error.
Bit 1	Speaker data
Bit 0 = 1	Enable Timer (8254) for speaker
Data read back	
Bit 7 = 1	Memory PARITY error.
Bit 6 = 1	IOCHCK error(*)
Bit 5	Timer 2 (8254), output
Bit 4	REFRESH detect.
Bit 3 = 1	NMI disabled, for IOCHCK (*).
Bit 2 = 1	NMI disabled for memory PARITY error (*).
Bit 1	Speaker data
Bit 0 = 1	Timer 2 (8254) for speaker enabled.

Note (*) The default setting on RESET is 00.

Figure 6f—Port B (8255) PPI register

NMI Mask register, Address 70h	
Bit 7 = 1	Disable NMI (Default setting on RESET).
Bit 7 = 0	Enable NMI

Figure 6g—NMI Mask register

DMA Memory Mapper (Page Registers)

Operation	Mapping Address A16-23h	Mapping Address A24-31h
/DACK0	87h	97h
/DACK1	83h	93h
/DACK2	81h	91h
/DACK3	82h	92h
/DACK5	8Bh	9Bh
/DACK6	89h	99h
/DACK7	8Ah	9Ah
REFRESH	8Fh	9Fh

- All thirty-two 8-bit registers between 80h and 9Fh can be written and read back.
- If 8-bit mapping is selected in the Configuration Register then A24h to A31h produce '00' and no access is allowed to the registers at 90h to 9Fh.
- The mapped addresses are, during DMA and REFRESH cycles, driven on ATA16 to ATA19 and also on LA17 to LA31.

Figure 6h—DMA Memory Mapper (Page Registers)

Section 3. The Configuration Registers

This Section of the *GCK131 Chip Set Data Sheet* describes and explains the use of the configuration modules shown earlier in the block diagrams of Section 1. (*See Figures 2a through 2c.*)

Configuration and INDEXES

Programmable registers in each chip

The programmable configuration-bit registers in each of the three chips allow the *GCK131 Chip Set* (and the AT system) to be used in a wide variety of applications. The registers are designed for use with software which, as determined by the system designer, allows the end-user some flexibility in the way the system operates.

The programmable registers of each chip are:

- The *GC131 Peripheral Controller* configuration registers are used to select the Backplane, Refresh, and DMA clock speeds. These speeds—divisions of the system clock timing—are received by the *GC131* Controller. Mapping of the serial and parallel ports can be configured either by a register in the *GC131*, or from EEPROM control lines.
- The *GC132 CPU/Memory Controller* configuration registers control;
  a/ the general bus timing relationships for RAM and I/O,
  b/ the size of the RAM and ROM block (which can be selected by registers in the *GC132* Controller), and lastly through general setup bits, control such functions as PARITY , COPROCESSOR selection , ROM SHADOWING, and the REMAPPING features.
- The *GC133 Bus Bridge Interface* has configuration bits that;
  a/ select the DRAM configuration,
  b/ control interleaving and REMAP, and
  c/ also identify the chipset revision number from a READ ONLY register within the chip. The revision number is important for system developers—it provides a method of identifying the features available in the chip set.

The configuration registers are partitioned

The configuration registers of the chip set are partitioned into regions: each is non-overlapping and unique.

- I/O address 24h is a 'write-only' register within which is placed a 'pointer' to the required INDEX .
- I/O address 28h is a 'read/write' port within which the data for the INDEX is placed.

Configuration and INDEXES

How to read or write to the registers
It's a two-step process:

1. Write the INDEX of the desired register to address 24h.
2. Read/write the data from/to address 28h.

Each chip has its own INDEX space (or Region), as follows:

- The *GC132* INDEX space resides from 00h to 0Fh,
- The *GC133* INDEX space resides from 10h to 1Fh,
- The *GC131* INDEX space resides from 40h to 4Fh.

Signals associated with the configuration registers

CONFIGAS
When an I/O WRITE is made to register 24h, CONFIGAS goes active (HIGH) and, on the falling edge of the signal, latches the data (the INDEX pointer) on the lower eight data lines into the INDEX registers of each chip of the set.

CONFIGDW
When an I/O WRITE is made to port 28h, CONFIGDW goes active (HIGH) indicating that valid data is available on the lower eight bits of the data buses. The target chip—identified as having the INDEX register by the prescribed Region spaces noted earlier—strobes the data to the appropriate configuration register on the falling edge of CONFIGDW.

CONFIGDR
When an I/O READ to port 28h occurs, CONFIGDR goes active (HIGH) and data will be presented to the lower eight bits of the data bus. Only one chip responds: the one whose INDEX register value matches within the prescribed range.

SUMMARY OF THE INDEXES

Section 3. 1 INDEX 00h—General setup bits GC132

Configuration and INDEXES

Default value = 00h

The configuration bits of INDEX 00h are available for programming general system setup.

Coprocessor (Bits 0 and 1)

Bit 0 toggles to enable or disable the numeric coprocessor (if installed). The default (Bit 0 = '0') applies if the system is not fitted with the device. Use Bit 1 to indicate the device type. The default (Bit 1 = '0') indicates an 80387 device. If an 80287 is fitted, Bit 1 is set equal to '1'.

Parity check (Bit 3)

The default setting (Bit 3 = '0') selects parity checking OFF.

DRAM banks 4 and 5

As required to match the installed devices, use Bit 4 to enable or disable the use of DRAM Banks 4 and 5.

Lower and Middle BIOS

As detailed in a later section (*'Programming the configuration registers'*), Use Bits 6 and 7 to enable the shadowing of the lower and/or middle BIOS images of BIOS into DRAM.

Bit	*State*	*Description*
0	= 0 = 1	Coprocessor , disabled. Coprocessor, enabled.
1	= 0 = 1	Coprocessor type = 80387 Coprocessor type = 80287
2	= 0	Reserved. Should always be programmed to 0.
3	= 0 = 1	Parity, disabled. Parity, enabled.
4	= 0 = 1	DRAM Banks 4 and 5, disabled. DRAM Banks 4 and 5, enabled.
5	= 0 = 1	CAS Shift, disabled. CAS Shift, enabled. NOTE : CAS will be delayed by one-half FAST 'CLK2' cycle during a WRITE operation—to accommodate slow processors.
6	= 0 = 1	Lower BIOS, Not shadowed. Lower BIOS, Shadowed into DRAM.
7	= 0 = 1	Middle BIOS, Not shadowed. Middle BIOS, Shadowed into DRAM (If present).

Figure 7a—INDEX00h, General setup bits

Section 3. 2 INDEX 01h—General setup bits GC132

Default value = 88h

The configuration bits of INDEX 01h are also available for general system setup purposes. As indicated below, use Bit 0 to enable or disable the shadowing of Video BIOS. Use Bit 1 to control the use of PAGE mode. The BIOS EPROM type is selected by Bit 2.

Other Bits are used in this manner;

Use Bit 3 to select the 80387 coprocessor CLOCK mode as either asynchronous or synchronous.

Video BIOS shadowing is selected either OFF or ON by Bit 4. Similarly, Bit 5 controls the REMAP, Bit 6 enables or disables the use of Middle BIOS (*).

Bit	*State*	*Description*
0	= 0	Video BIOS, Not shadowed into DRAM.
	= 1	Video BIOS, Shadowed into DRAM
1	= 0	Page mode, disabled.
	= 1	Page mode, enabled.
2	= 0	BIOS EPROM type = 27256
	= 1	BIOS EPROM type = 27512
3	= 0	CLOCK mode (80387), asynchronous.
	= 1	CLOCK mode (80387), synchronous.
4	= 0	Video BIOSshadowing, disabled.
	= 1	Video BIOS shadowing, enabled.
5	= 0	REMAP (above 1, 2, or 4 Mb), disabled.
	= 1	REMAP (above 1, 2, or 4 Mb), enabled.
6	= 0	Middle BIOS, disabled
	= 1	Middle BIOS, enabled.
7	= 0	Quiet bus, disabled.
	= 1	Quiet bus, enabled. During high-speed local access, the commands are not issued to the backplane. And BALE is kept HIGH during the cycle.

Figure 7b—INDEX01h, General setup bits (Continued)

(*) Note:
The programming and use of these features is described in a later Section of this document: See 'Programming the Configuration Registers'.

Section 3. 3 INDEX 02h—High speed override bits GC132

Default value = FFh

Configuration and INDEXES

Use these configuration bits if high speed **SRAMs are installed in preference to** DRAMs in one or more banks of the system. Each bank can be individually configured to optimize system performance.

When the override bit for a particular bank is ON, the 'forced' delays indicated in Figure 8c are used rather than the programmed values of INDEX 04h and 05h.

Bit	*State*	*Description*
0	= 0	DRAM delay BANK 0, overrride ON; **forces these delays:** 0 RAS delays, 2 CAS delays, 2 CAS active, RECOVERY, PAGE VIOLATIONS are always 'false'.
	= 1	DRAM delay BANK 0, override OFF; acts on the settings of INDEX04h and 05h.
1	= 0	DRAM delay BANK 1, override ON.
	= 1	DRAM delay BANK 1, override OFF.
2	= 0	DRAM delay BANK 2, override ON.
	= 1	DRAM delay BANK 2, override OFF.
3	= 0	DRAM delay BANK 3, override ON.
	= 1	DRAM delay BANK 3, override OFF.
4	= 0	DRAM delay BANK 4, override ON.
	= 1	DRAM delay BANK 4, override OFF.
5	= 0	DRAM delay BANK 5, override ON.
	= 1	DRAM delay BANK 5, override OFF.
6	= 0	Reserved. Always program to '0'.
7	= 0	Reserved. Always program to '0'.

Figure 7c—INDEX02h, High-speed override bits

Section 3. 4 INDEX 03h—DRAM configuration GC132

Default value = A0h

This configuration register is used to **match the number and type of DRAMs** used in the system.

The selection of either 256K or 1 Mb DRAMs is made within two groups; namely, Banks 0, 1 and Banks 2 through 5. This arrangement does not allow the intermixing of DRAM types—*See the Note (*) regarding INDEX 10h.*

Interleaving and **EMS PAGE** address settings are also configured using this configuration register.

Bit	*State*		*Description*
0,1	**Bit 0**	**Bit 1**	*The combination of Bits 0 and 1 select the following:*
	= 0	= 0	DRAMs are 256K.BANK0 through BANK5.
	= 0	= 1	Reserved.
	= 1	= 0	Reserved.
	= 1	= 1	DRAMs are 1 Mb. BANK0 through BANK5.
3,2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:*
	= 0	= 0	One bank of DRAM enabled, interleave OFF.
	= 0	= 1	Two banks of DRAM enabled, interleave ON.
	= 1	= 0	Not permitted.
	= 1	= 1	Four banks of DRAM enabled, interleave ON.
7 6 5 4	See Descr-iption.		**EMS page.** The settings of Bits 7 through 4 specify a 64k 'hole' of 'OFFBOARD ' RAM (not DRAM) starting at the coded value. The default settings are: Bit 7 = 1, Bit 6 = 0, Bit 5 = 1, Bit 4 = 0; meaning, '1010'. This translates to a 64k EMS hole that starts at *A0000h.*

Figure 7d—INDEX03h, DRAM configuration

(*) Note:
In conjunction with the setting of INDEX03h used to select the use of either 256K or 1 Mb DRAMs, INDEX10h must also be similarly programmed. If not done, the system will not operate properly.

Section 3. 5 INDEX 04h—DRAM configuration (Banks 0,1,2,3) GC132

Configuration and INDEXES

Default value = FFh

This configuration register is available to set up the timing of RAS and CAS signals to the DRAM s for Banks 0 through 3. The delays (shown below) are programmed as multiples of CLKIN cycles. RAS delay is measured from the rising edge of CLKIN during /ADS active.

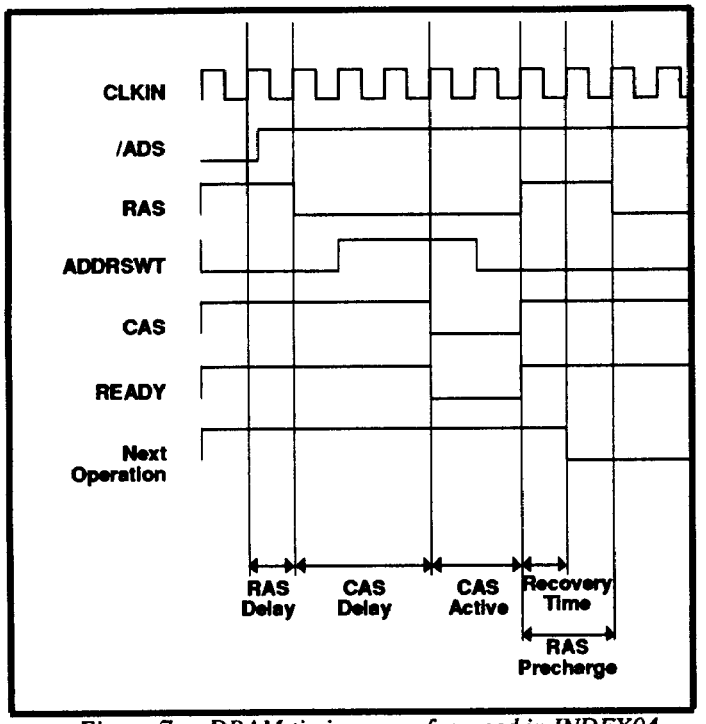


Figure 7e—DRAM timing, as referenced in INDEX04

The register settings, as programmed with INDEX 04h, are used for Banks 0 through 3 of the system *unless* (by INDEX 02h) overrides have been selected for one or more banks.

Bit	*State*		*Description*
1,0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:*
	= 0	= 0	Zero RAS delay.
	= 0	= 1	One RAS delay.
	= 1	= 0	Two RAS delays.
	= 1	= 1	Three RAS delays.
2	= 0		Two CAS delays measured from RAS in CLKIN.
	= 1		Three CAS delays.
6,3	**Bit 6**	**Bit 3**	*The combination of Bits 6 and 3 select the following:*
	= 0	= 0	Two CAS active CLKIN cycles.
	= 0	= 1	Four CAS active.
	= 1	= 0	Six CAS active.
	= 1	= 1	Eight CAS active.
4	= 0		Four RAS precharge CLKIN cycles.
	= 1		Six RAS precharge.
5	= 0		Zero recovery time
	= 1		Two recovery CLKIN cycles.

Figure 7f—INDEX04h, DRAM timing BANKS0...3

Section 3. 6 INDEX 05h—DRAM configuration (Banks 4,5) GC132

Default value = FFh

This configuration register is available to program the timing for RAS and CAS in Banks 4 and 5.
[HINT: See *INDEX 04*h for more information about delay timing.]

Bit	*State*		*Description*
1,0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select:*
	= 0	= 0	Zero RAS delays.
	= 0	= 1	One RAS delay measured in CLKIN cycles.
	= 1	= 0	Two RAS delays.
	= 1	= 1	Three RAS delays.
2	= 0		Two CAS delays measured from RAS in CLKINs.
	= 1		Three CAS delays.
6,3	**Bit 6**	**Bit 3**	*The combination of Bits 6 and 3 select:*
	= 0	= 0	Two CAS active CLKINs.
	= 0	= 1	Four CAS active.
	= 1	= 0	Six CAS active.
	= 1	= 1	Eight CAS active.
4	= 0		Four RAS precharge CLKINs.
	= 1		Six RAS precharge.
5	= 0		Zero recovery time
	= 1		Two recovery CLKINs.

Figure 7g—INDEX05h, DRAM timing for BANKS 4 and 5

Section 3. 7 INDEX 06h to INDEX09h—Tailor timing requirements GC132

Configuration and INDEXES

The configuration registers INDEX 06h through 09h are available to tailor the timing requirements for various system commands.

Delays are given as CLKIN cycles.

On the following pages, Figures 7h through 7m for configuration registers INDEX 06h through 09h indicate various 'delays'. These delays are multiples of CLKIN cycles. Figure 7i diagrams their relationships

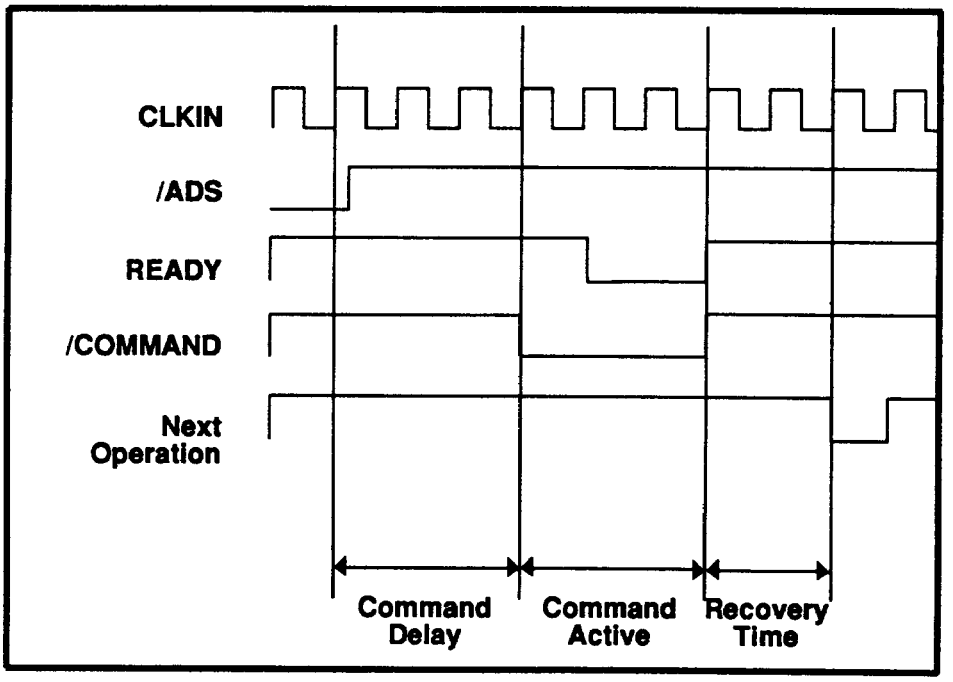


Figure 7h—Cycle timing, as referenced in INDEX06h to 09h

Section 3. 8 An example GC132

Objective:
In this example, we wish to match the I/O timing of the *GCK131 Chip Set* (operating at 25 MHz) with a 'generic' system that uses the AT-standard (running at 8 MHz).

AT-standards:
As a first step, the generic I/O timing values of the AT are used to give values useful in programming the *GCK131 Chip Set.* Figure 7i illustrates these relationships.

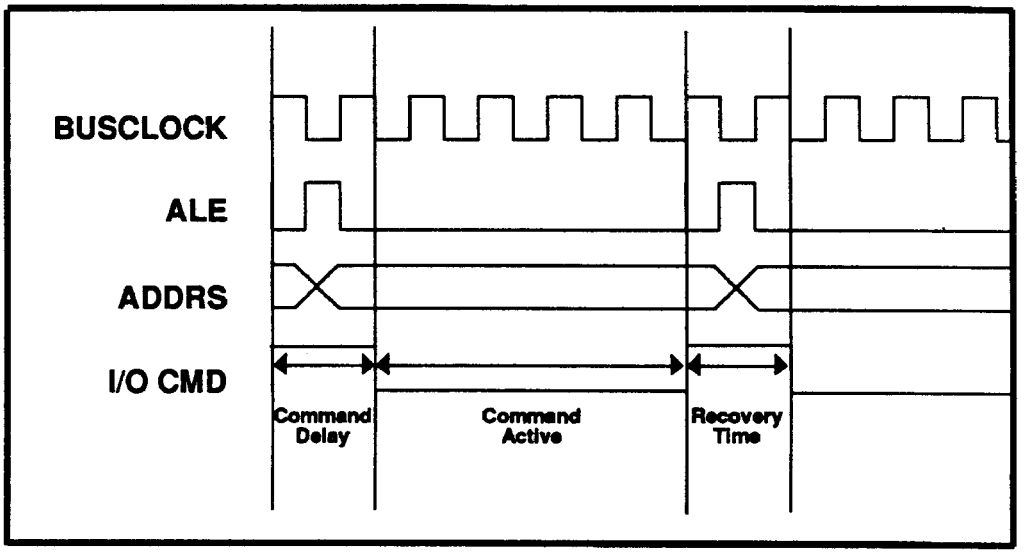


Figure 7i—Generic AT-system I/O timing, 3-wait states

(i) With a BUSCLOCK frequency (F) of 8 MHz: the period (T) is 125 ns.

(ii) With 4 wait states inserted: the total I/O command active time (4.5 x 125 ns) is 560 ns.

(iii) The command delay (1.5 x T) is 200 ns

(iv) The recovery time (1.5 x T) is 200 ns.

The chip timing relationships of the *CGK131 Controller* are referenced as multiples of CLKIN which, at 25 MHz, means the oscillator beats at 50 MHz.

(v) The reciprocal (t)—or, 1 divided by 50 MHz— is 20 ns.
Thus,

(vi) For a command active time of 560 ns we require 28 CLKINs (560 ns divided by 20ns).

(vii) For a command delay of 200 ns we require 10 CLKINs (200 ns divided by 20 ns).

(ix) For a recovery time of 200 ns we require 10 CLKINs (200 ns divided by 20 ns).

To match the generic 8 MHz timing for I/O access— and 4 wait states— we program the INDEX 08h (I/O Access) configuration register as follows:

(a) For a command delay of 10 CLKINs (*paragraph vii*);
INDEX08h, Bit 1 = '0', Bit 0 = '0'.

(b) For a command active period of 28 CLKINs (paragraph vi);
INDEX08h, Bit 3 = '1', Bit 2 = '0'.

(c) For a recovery time of 10 CLKINs (*paragraph ix*);
INDEX08h, Bit 5 = '0', Bit 4 = '1'.

With INDEX 08h, Bits 6 and 7 both programmed each as '1' the contents of **INDEX08h equals d8h.**

Section 3. 9 INDEX 06h—EPROM configuration GC132

Default value = FFh

Configuration registers INDEX 06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX 06h to INDEX 09h—Tailor timing requirements*)

On the following pages, Figures 7k through 7n introduce various timing relationships that can be programmed into the system. The relationships are multiples of CLKIN cycles. Figure 7i diagrams the relationships

Bit	*State*		*Description*
0	= 0		Three command delays in CLKINs.
	= 1		Five command delays.
2,1	**Bit 2**	**Bit 1**	*The combination of Bits 2 and 1 select the following:*
	= 0	= 0	Eight command active times in CLKINs.
	= 0	=1	Ten command active times.
	= 1	= 0	Twelve command active times.
	= 1	= 1	Fourteen command active times.
4,3	**Bit 4**	**Bit 3**	*The combination of Bits 4 and 3 select the following:*
	= 0	= 0	Two RECOVERY times in CLKINs.
	= 0	= 1	Four RECOVERY times in CLKINs.
	= 1	= 0	Six RECOVERY times in CLKINs.
	= 1	= 1	Eight RECOVERY times in CLKINs.
5	= 1		Reserved. Always program to '1'.
6	= 1		Reserved. Always program to '1'.
7	= 1		Reserved. Always program to '1'.

Figure 7j—INDEX06h, EPROM configuration

Section 3. 10 INDEX 07h—I/O Channel RAM configuration GC132

Default value = FFh

Configuration registers INDEX 06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX 06h to INDEX 09h—Tailor timing requirements*)

The timing indicated in the following Figure is related to CLKIN cycles.

Bit	*State*		*Description*
0	= 0		Five command delays in CLKINs.
	= 1		Seven command delays.
2,1	**Bit 2**	**Bit 1**	*The combination of Bits 2 and 1 select the following:*
	= 0	= 0	Seven command active times in CLKINs.
	= 0	= 1	Nine command active times.
	= 1	= 0	Eleven command active times.
	= 1	= 1	Thirteen command active times.
4,3	**Bit 4**	**Bit 3**	*The combination of Bits 4 and 3 select the following:*
	= 0	= 0	Zero RECOVERY times in CLKINs.
	= 0	= 1	Two RECOVERY times in CLKINs.
	= 1	= 0	Four RECOVERY times in CLKINs.
	= 1	= 1	Six RECOVERY times in CLKINs.
5	= 1		Reserved. Should always be programmed to '1'.
6	= 1		Reserved. Should always be programmed to '1'.
7	= 1		Reserved. Should always be programmed to '1'.

Figure 7k—INDEX07h, 16-Bit RAM configuration

Section 3. 11 INDEX 08h—I/O access configurations GC132

Default value = FFh

Configuration registers INDEX 06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX 06h to INDEX 09h—Tailor timing requirements*)

The timing indicated in the following Figure is related to CLKIN cycles.

Bit	*State*		*Description*
1,0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:*
	= 0	= 0	Ten command delay times in CLKINs.
	= 0	= 1	Twelve command delay times
	= 1	= 0	Sixteen command delay times.
	= 1	= 1	Eighteen command delay times.
3,2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:*
	= 0	= 0	Eighteen command active times in CLKINs.
	= 0	= 1	Twenty-two command active times in CLKINs.
	= 1	= 0	Twenty-eight command active times in CLKINs.
	= 1	= 1	Thirty-four command times in CLKINs.
5,4	**Bit 5**	**Bit 4**	*The combination of Bits 5 and 4 select the following:*
	= 0	= 0	Eight RECOVERY times in CLKINs.
	= 0	= 1	Ten RECOVERY times in CLKINs.
	= 1	= 0	Fourteen RECOVERY times in CLKINs.
	= 1	= 1	Sixteen RECOVERY times in CLKINs.
6,	= 1		Reserved. Should always be programmed to '1'.
7	= 1		Reserved. Should always be programmed to '1'.

Figure 7l—INDEX08h, I/O Access configuration

Section 3. 12 INDEX 09h—Interrupt acknowledge configurations GC132

Default value = FFh

Configuration registers INDEX 06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX 06h to INDEX 09h—Tailor timing requirements*)

The timing indicated in the following Figure is related to CLKIN cycles.

Bit	*State*		*Description*
0	= 0		Three command delay times in CLKIN cycles.
	= 1		Three command delay times in CLKINs.
2,1	**Bit 2**	**Bit 1**	*The combination of Bits 2 and 1 select the following:*
	= 0	= 0	Five command active times in CLKINs.
	= 0	= 1	Seven command active times
	= 1	= 0	Nine command active times.
	= 1	= 1	Eleven command active times.
3	= 0		Two RECOVERY times in CLKINs.
	=1		Four RECOVERY times in CLKINs.
4,	= 1		Reserved. Should always be programmed to '1'.
5,	= 1		Reserved. Should always be programmed to '1'.
6,	= 1		Reserved. Should always be programmed to '1'.
7	= 1		Reserved. Should always be programmed to '1'.

Figure 7m—INDEX09h,Interrupt acknowledge configuration

Section 3. 13 Indexes 0Ah through 0Fh are Test registers GC132

Indices 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, and 0Fh are test registers and should not be used.

Section 3. 14 INDEX 10h—DRAM configurations GC133

Configuration and INDEXES

Default value = 00h

This configuration register is available for programming the number and type of DRAMs used in the system—*See Note(*)*. It is also used the enable or disable the REMAP and interleave options—as programmed with INDEX 03h.

Bit	*State*		*Description*
0,1	**Bit 0**	**Bit 1**	*The combination of Bits 0 and 1 select the following:*
	= 0	= 0	DRAM s are 256K.BANK0 through BANK5.
	= 0	= 1	Reserved.
	= 1	= 0	Reserved.
	= 1	= 1	DRAM s are 1 Mb. BANK0 through BANK5.
2	= 0		1 DRAM bank, interleave OFF.
	= 1		2, 4, or 6 banks of DRAM , auto-interleave ON.
3	= 0		Disable 384K, REMAP above 1,2, or 4 Mb.
	= 1		REMAP, enable.
4,	= 0		Reserved. Always program to '0'.
5,	= 0		Reserved. Always program to '0'.
6,	= 0		Reserved. Always program to '0'.
7	= 0		Reserved. Always program to '0'.

Figure 7n—INDEX10h,DRAM configuration

(*)Note:
In conjunction with the setting of INDEX10h used to establish the use of either 256K or 1 Mb DRAMs, INDEX03h must also be similarly programmed. If not done, the system will not operateproperly.

Section 3. 15 INDEX 13h—Revision identification GC133

The contents of INDEX 13h are available for use in programming when the objective is to determine the availability—by reference to the revision number—of the *GCK131 Chip Set* features.

This document is issued concurrently with the release of chips identified '01' in INDEX 13h. Revised versions of the *GCK131 Chip Set* will be identified in INDEX 13h in the sequence '02, 03 ...'. For more information, contact your Headland Technology representative.

Bit	*State*	*Description*
7 to 0	01h	Revision ID.

Figure 7o—INDEX13h

Section 3. 16 INDEX 40h—Clock dividers for low speed(non-TURBO mode) GC131

Default value = 10h

Configuration and INDEXES

INDEX40h is available to program the desired clock rates for various functions of the *GCK131 Chip Set* when operating in non-**TURBO** mode.(*) The resultant clock rate is a division of the incoming signal at the '/SYSCLK' input.

Bits 0 and 1 control the frequency of BUSCLOCK to the backplane. Bits 2 and 3 are used to select the desired REFRESH speed. Similarly Bits 4 and 5 program the DMA speed while in non-**TURBO** mode.

Bit	*State*		*Description*
1,0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:* Back plane (BUSCLOCK) clock divider for SLOW speed.
	= 0	= 0	Divide incoming /SYSCLK by one.
	= 0	= 1	Divide incoming /SYSCLK by two.
	= 1	= 0	Divide incoming /SYSCLK by four.
	= 1	= 1	Divide incoming /SYSCLK by eight.
3,2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:* REFRESH clock divider for SLOW speed.
	= 0	= 0	Divide incoming /SYSCLK by one.
	= 0	= 1	Divide incoming /SYSCLK by two.
	= 1	= 0	Divide incoming /SYSCLK by four.
	= 1	= 1	Divide incoming /SYSCLK by eight.
5,4	**Bit 5**	**Bit 4**	*The combination of Bits 5 and 4 select the following:* DMA clock divider for SLOW speed.
	= 0	= 0	Divide incoming /SYSCLK by one.
	= 0	= 1	Divide incoming /SYSCLK by two.
	= 1	= 0	Divide incoming /SYSCLK by four.
	= 1	= 1	Divide incoming /SYSCLK by eight.
6,	= 0		Reserved. Always progam to '0'
7	= 0		Reserved. Always progam to '0'

Figure 7p—INDEX40h, Clock dividers (non-TURBO mode)

(*) Note:
For information regarding TURBO mode—See INDEX41h. Indicated by FAST/SLOW (Pin 130) of the GC131 Controller.

Section 3. 17 INDEX 41h—Clock dividers for high speed (TURBO) GC131

Default value = 3Ah

INDEX41h is available to program the desired clock rates for various functions of the *GCK131 Chip Set* when operating in **TURBO** mode.(*) The resultant clock rate is a division of the incoming signal at the '/SYSCLK' input.

Bits 0 and 1 control the frequency of BUSCLOCK to the backplane. Bits 2 and 3 are used to select the desired REFRESH speed. Similarly Bits 4 and 5 program the DMA speed while in **TURBO** mode.

Bit	*State*		*Description*
1,0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:* Back plane (BUSCLOCK) clock divider for FAST speed.
	= 0	= 0	Divide incoming /SYSCLK by one.
	= 0	= 1	Divide incoming /SYSCLK by two.
	= 1	= 0	Divide incoming /SYSCLK by four.
	= 1	= 1	Divide incoming /SYSCLK by eight.
3,2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:* REFRESH clock divider for FAST speed.
	= 0	= 0	Divide incoming /SYSCLK by one.
	= 0	= 1	Divide incoming /SYSCLK by two.
	= 1	= 0	Divide incoming /SYSCLK by four.
	= 1	= 1	Divide incoming /SYSCLK by eight.
5,4	**Bit 5**	**Bit 4**	*The combination of Bits 5 and 4 select the following:* DMA clock divider for FAST speed.
	= 0	= 0	Divide incoming /SYSCLK by one.
	= 0	= 1	Divide incoming /SYSCLK by two.
	= 1	= 0	Divide incoming /SYSCLK by four.
	= 1	= 1	Divide incoming /SYSCLK by eight.
6,	= 0		Reserved. Always progam to '0'
7	= 0		Reserved. Always progam to '0'

Figure 7q—INDEX41h, Clock dividers (TURBO mode)

(*) Note:
For information regarding non-TURBO mode—See INDEX40h.Indicated by FAST/SLOW (Pin 130) of the GC131 Controller.

Section 3. 18 INDEX 42h—DMA and REFRESH wait states GC131

Configuration and INDEXES

Default value = 00h

This configuration register is available to program the number of wait states required in REFRESH and DMA operations. In use, programmers are to be advised that this index (INDEX 42h) must be adjusted in a sequence after those of INDEX40h and INDEX 41h.

When programming the REFRESH and DMA wait states, this INDEX 42h uses a four-bit binary representation (0...15) of the number of desired wait states in multiples of the clock period programmed in INDEX40h and INDEX 41h

Bit	*Description*
3, 2, 1, 0	**REFRESH wait states.** A Bininary count of the number of wait states of REFRESH clock Where: Bits 3, 2, 1, 0 = 0 represent 0 wait states. And, Bits 3, 2, 1, 0 = 1 represents 15 wait states.
7, 6, 5, 4	**DMA wait states** A Binary count of the number of wait states of DMA clock. Where: Bits 3, 2, 1, 0 = 0 represent 0 wait states. And, Bits 3, 2, 1, 0 = 1 represents 15 wait states.

Figure 7r—INDEX42h, DMA and REFRESH wait states

Section 3. 19 INDEX 43h—Serial, parallel and mapper selections GC131

Default value = 00h

The *GCK131 Chip Set* has built-in decoding logic for I/O devices; including, two serial ports and one parallel port.

Serial port 1 is mapped to COM1 (3F8h...3FFh) and **serial port 2** is mapped to COM2 (2F8h...2FFh). The serial ports can be selected by Bits 0 and 1 of this INDEX 43h.

The parallel port decoding can be selected—for either LPT1 (378h...37Fh) or LPT2(278h...27Fh)—by Bit 2 of this INDEX 43h.

Bit	*State*	*Description*
0	= 0	Serial port 1, disable.
	= 1	Serial port 1, enable.
1	= 0	Serial port 2, disable.
	= 1	Serial port 2, enable.
2	= 0	Parallel port, configure as LPT2.
	= 1	Parallel port, configure as LPT1.
3	= 0	Parallel port, disable.
	= 1	Parallel port, enable.
4	= 0	DMA, standard AT 8-bit page mapping.
	= 1	Extended DMA 16-bit page mapping, enabled NOTE: The address for the PAGE MAPPER is the same as the AT standard; but, the additional 8 bits are mapped 10h addresses above the usual location. (See Figure 7t.) If 8-bit mapping is selected, the upper addresses produce a '0' and accesses are disallowed to I/O locations 90h to 9Fh
5, 6, 7	= 0, = 0, = 0	Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'.

Figure 7s—INDEX43h, Serial, parallel, and mapper select

Section 3.19a INDEX 43h - Extended DMA 16-bit page mapping

Operation	Mapping Address A16-23h	Mapping Address A24-31h
/DACK0	87h	97h
/DACK1	83h	93h
/DACK2	81h	91h
/DACK3	82h	92h
/DACK5	8Bh	9Bh
/DACK6	89h	99h
/DACK7	8Ah	9Ah
REFRESH	8Fh	9Fh

All thirty-two 8-bit registers between 80h and 9Fh can be written and read back.
If 8-bit mapping is selected in the Configuration Register then—A24h to A31h produce '00' and no access is allowed to the registers at 90h to 9Fh.
The mapped addresses are, during DMA and REFRESH cycles, driven on ATA16 to ATA19 and also on LA17 to LA31.

Figure 7t—INDEX 43h, Extended DMA 16-bit page mapping

Section 3. 20 INDEX 44h—Video external register strobe

Default value = 00h

A WRITE to this port clocks data to an internal register of the *GC131 Peripheral Controller*. It also strobes /CSVREG . The external strobe is intended to clock the data into the actual register and thus mimic the configuration switches on the video board.

When this port is read, data inside the *GC131 Controller* is driven onto the data bus. In effect, the controller provides a 'shadow' of the video configuration switches.

A READ to this port does not strobe /CSVREG.

Section 3. 21 INDEX 45h—EEPROM Control

Default value = 00h

Configuration and INDEXES

This configuration register is available for programming to control EEPROM accesses. It is possible to interface, directly, with an EEPROM device (like the *Monolithic Memories Type MC9306* device) using suitable programming.

With this register INDEX 45h, interface signals of CLOCK, DATA, and CHIP SELECT can be controlled in order to READ/WRITE the EEPROM.

Bit	*State*	*Description*
0		EEPROM data IN/OUT. When data is written, it appears on pin DOEEP. When read, the data comes from pin DIEEP.
1		EEPROM clock. Data, written on this bit, appears, on pin CKEEP.
2	= 0 = 1	EEPROM chip select. Output pin CSEEP = 0. Output pin CSEEP = 1.
3, 4, 5, 6, 7	= 0 = 0 = 0 = 0 = 0	Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'.

Figure 7u—INDEX45h, EEPROM control

Section - 4 Programming the configuration registers—EPROMs

This Section of the *GCK131 Chip Set Data Sheet* explains how the configuration registers can be used to optimise the EPROM s of an 80386 system. In this use, the *GC132 CPU/Memory Controller's* functions are particularly important.

The *GC132 Controller*, as noted in the *Configuration Register* Section, operates in the 32-bit mode to control: a/ the general bus timing relationships for RAM, ROM, and I/O; b/ the size of RAM and ROM blocks; and c/ to adjust the system when using a coprocessor, and so on.

Programming the Configuration Registers

The configuration registers of the *GC132* are partitioned according to their duties. One register set operates system timing, another sets up the hardware, and a third set configures the memory map.

This Section is mainly concerned with the third set of registers; in particular, the programmable features used to acheive;

- Memory map reconfiguration
- Faster operation through 'shadowing'
- Startup configuration
- Multiple banks of DRAM
- Reclaim RAM with REMAPPING

BIOS patches used to implement required defaults
A convenient method, by which the defaults can be established for the 80386 Microprocessor-system involves the use of a BIOS patch. An *Application Note* is included in a later Section of this document.

4 - 1 Reconfiguring the memory map

The memory map of the *GC132 CPU/Memory Controller* is compatible with the AT specification. It provides, in addition, several features that allow: greater memory capacity, improved performance, and the ability to use operating systems other than DOS.

Compatibility with the AT-design

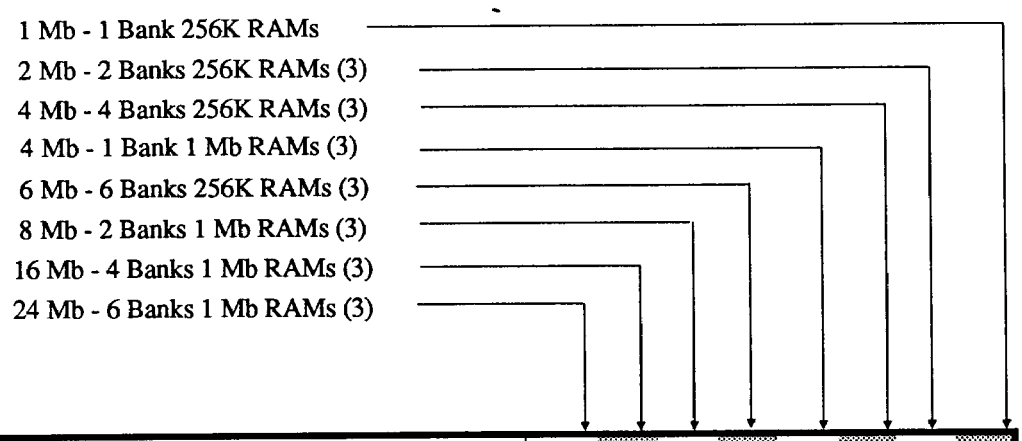
In the AT design, upward compatibility (from the XT lineage) is maintained and, in consequence, the memory map of an XT system can be described as a sub-set of an AT memory map. But, because the XT design uses a memory space of just one megabyte, only the lower 1Mb of the AT's memory map is constrained to the needs of compatibility. The remainder (15 Mb) can be designated as 'backplane' memory—with the exception of the small area of upper memory reserved to mirror an image of BIOS. The mirror image, incidentally, is needed for the RESTART vector and is located at the very top of the four gigabytes of 80386 memory.

Programming the Configuration Registers

EPROM Memory Map

The needs of compatibility require the EPROM BIOS at F0000h through FFFFFh ('Lower BIOS') and, for booting, BIOS is located at FFFF0000h ('Upper BIOS') (See Figure 8a *GC132 Memory Controller Memory Map.* Changes, however, can be made to this arrangement—as explained in the following pages where you will meet:

- MBEN, a device used to regulate the memory space associated with a copy of BIOS: Middle BIOS. MBEN, when disabled, frees this memory space when operating systems (non-DOS) do not require BIOS in this memory region. MBEN acts on a portion of memory described as 'Window 3'.
- LBSHADOW , device used to implement a 32-bit (rather than a 16-bit) version of BIOS called ' Lower BIOS'—replaced in the same memory location—acts on a portion of memory described as 'Window 2'.
- MBSHADOW , device used to implement a 32-bit version of BIOS called 'Middle BIOS' located in memory at 'Window 3'.
  MBSHADOW operates when the MBEN device is enabled.
- VBSHADOW , a device used to implement a 32-bit version of Video BIOS: a replacement of the 16-bit version in the memory region called 'Window 1'.
- VBEN, a device used to regulate the shadowing of Video BIOS. When enabled, the system takes the configuration established by VBSHADOW .



Absolute Addresses	24	16	8	6	4	4	2	1
0h - 9FFFFh	32-Bit On-board RAM							
A0000h - BFFFFh	AT-compatible RAM							
C0000h - CFFFFh	Video BIOS(2)							
D0000h - DFFFFh	AT-compatible RAM							
E0000h - EFFFFh	Lower BIOS (2)							
F0000h - FFFFFh	Lower BIOS (2)							
100000h - 1FFFFFh	32-Bit On-board RAM							
200000h - 3FFFFFh								
400000h - 5FFFFFh								
600000h - 7FFFFFh								
800000h - 9FFFFFh								
A00000h - FDFFFFh	AT-compatible RAM							
FE0000h - FEFFFFh	MBIOS(2)							
FF0000h - FFFFFFh	MBIOS(2)							
1000000h - 11FFFFFh	OBR	(1)	Not used					
1200000h - 17FFFFFh								
1800000h - FFFDFFFFh								
FFFE0000h - FFFEFFFFh	Upper BIOS (2)							
FFFF0000h - FFFFFFFFh	EPROM							

Programming the Configuration Registers

Note (1) Banks 5 and 6 operate exactly as do the other banks; but, are configured by a separate register.

(2) Memory type in these locations is dependent upon the configuration registers and the EPROM type used.

(3) When more than 1 bank of memory is used, interleaving is performed on A2

OBR = On board 32-bit RAM

Figure 8a—GC132 Memory Controller, Memory map

Offboard (or Backplane) Memory

By definition, offboard (or backplane) memory is that memory space where EPROM or DRAM is not located. By corollary, if it isn't EPROM or DRAM space then it is backplane space—this includes all of the vast area above DRAM to the 4 Gb top. Backplane memory is assumed to be either eight or sixteen bits wide as determined by /MEMCS 16 from the backplane. This is the only RAM type affected by IOCHRDY .

4 - 2 MBEN and non-DOS operation

The *GCK131 Chip Set* has programmable configuration bits (as described in the *Configuration Registers* Section). Of these, MBEN ('Middle BIOS enable') is used to alter EPROM space when running non-DOS applications.

MBEN 's purpose is to enable and disable the EPROM BIOS at FF0000h. This, as shown in Figure 8b, removes Middle BIOS from memory. It's a useful feature. When UNIX® is used as the operating system and with 24 Mbytes of DRAM in use, middle BIOS is not needed. When removed, a contiguous DRAM space is made available—without the MBEN feature, an inconvenient hole at FF0000h exists.

How to use MBEN to remove Middle BIOS
MBEN is signalled by INDEX 01h (*'General setup bits'*) where Bit 6 is set to '0' to disable and '1' to enable MBEN.

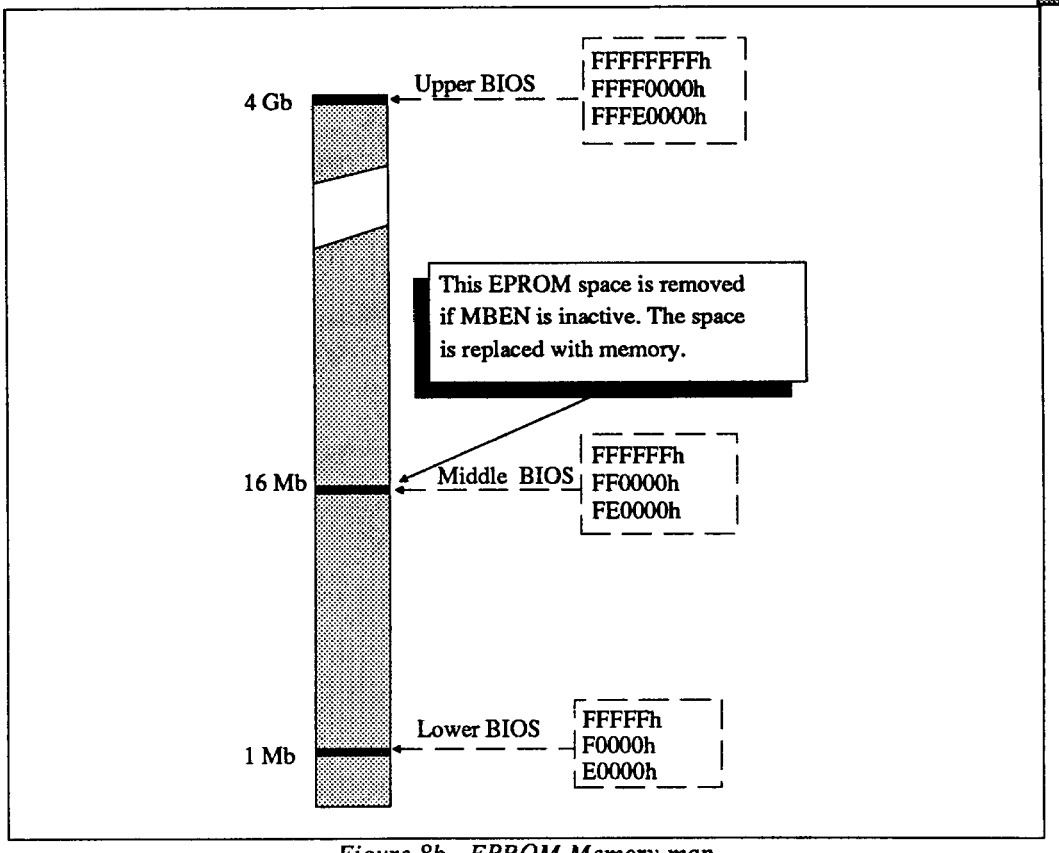


Figure 8b—EPROM Memory map

4 - 3 Programmable configuration bits allow RAM 'shadowing'

The *GCK131 Chip Set* has a built-in 'shadowing' feature that allows the copying of the BIOS (EP)ROMs to RAM for faster execution of ROM based code.

When a shadowed BIOS is accessed by the CPU, the data is fetched from high speed 32-bit RAM instead of the slower 16-bit ROM on the mother board; or even slower yet, from 8-bit access through the expansion bus.

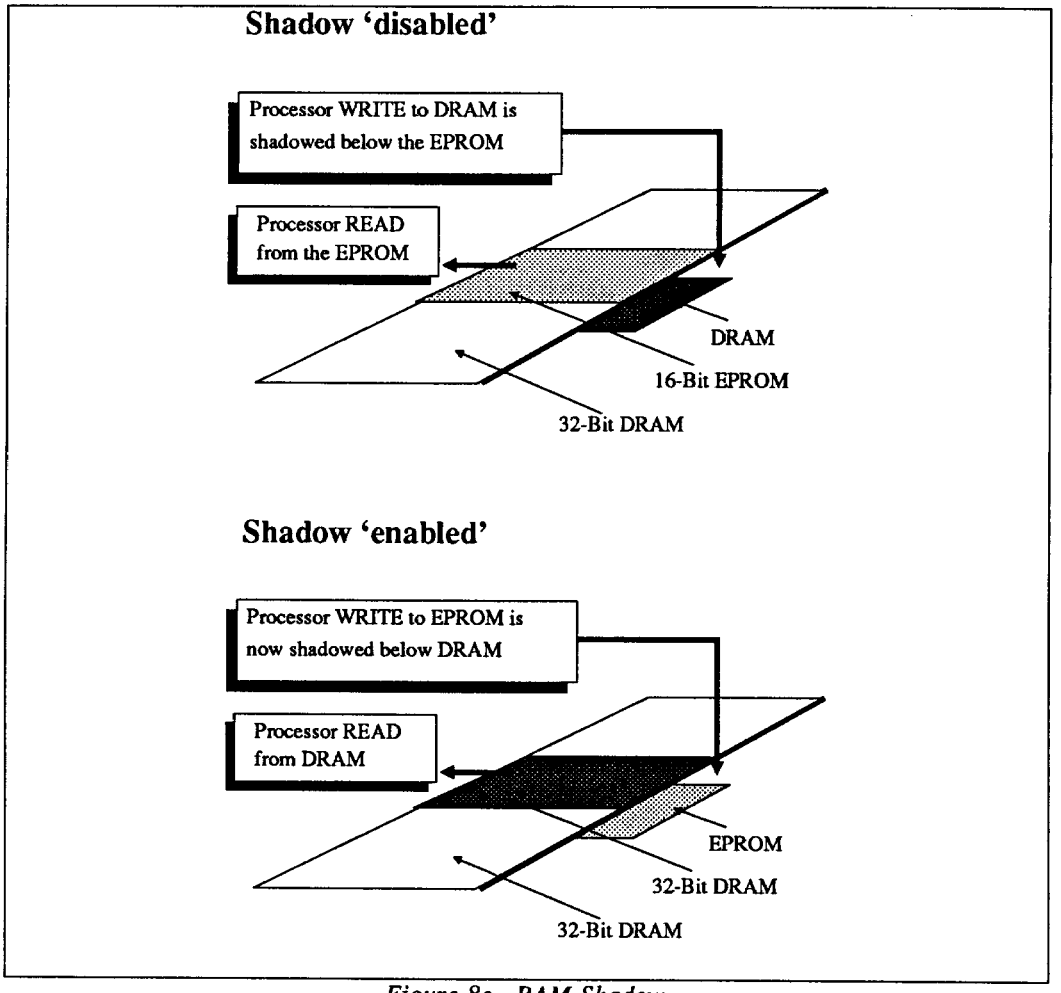


Figure 8c—RAM Shadow

How the RAM 'shadow' feature works

Essentially the shadow RAM feature works by initially routing READ operations to the physical ROM and WRITE operations to the shadow RAM.

When the system boots, a routine in the system BIOS makes a copy of the ROM modules to RAM by copying the BIOS back to itself.

The *GC132 CPU/Memory Controller* arranges the READ and WRITE operations in such a way that the ROM contents are duplicated in shadow RAM.

When the cloning operation is done, the bootstrap routines switch the *GC132 Controller* into shadow-mode. With this done, the shadow memory windows are used in this manner:

- During READ operations, access is given to the shadow RAM.
- During WRITE operations, the *GCK131 Controller* gives access to the ROMs; but, ROMEN is not active.

This effectively protects the shadow RAM from being changed—by dumping all WRITE data operations into the proverbial bit bucket it is impossible to write to ROM.

Programming the Configuration Registers

4 - 4 Four memory windows

The *GCK131 Chip Set* accesses the system ROMs through four memory 'windows'.

Two variants of the windows are used: one for each type of ROM chip used in the system. The EPROMs can be either, Type 27256 (Figure 8d) or Type 27512 (Figure 8e).

When EPROM Type 27512 is used Windows 2, 3, and 4 are larger. *See Note(*)*

Window	*Range*	*Use*
1	C0000h - CFFFFh	Video BIOS
2	F0000h - FFFFFh	Lower BIOS
3	FF0000h - FFFFFFh	Middle BIOS
4	FFFF0000h - FFFFFFFFh	Upper BIOS

Figure 8d— Memory windows (EPROM type 27256)

Programming the Configuration Registers

Window	*Range*	*Use*
1	C0000h - CFFFFh	Video BIOS
2	E0000h - FFFFFh	Lower BIOS
3	FE0000h - FFFFFFh	Middle BIOS
4	FFFE0000h - FFFFFFFFh	Upper BIOS

Figure 8e— Memory windows (EPROM type 27512)

(*) Note:
The installed chip's type is signalled by the setting of INDEX *01h 'General setup bits'. This, as noted in the ConfigurationRegister Section, Bit 2 is to be set to '0' when EPROM Type 27256 is used; and set to '1' with the 27512.*

4 - 5 RAM shadowing—Windows 1 through 3

The *GCK131 Chip Set* supports shadowing for Windows 1, 2, and 3. Access through Window 4 is always direct to the system BIOS ROMs.

Each window has its own special behaviour when shadowing.

Window 1 - Video BIOS shadowing

NOTE: The Video BIOS window is reserved for ROM modules fitted to video-adapter cards and similar devices.

By default (after startup) all READ and WRITE accesses to this window are directed to the 16-bit AT expansion bus.

Programming the Configuration Registers

The default mode for Window 1 accommodates unconventional usage of the video BIOS address range by network-adapter cards and other devices that put dual-ported RAM at this location. In the default mode, the cards function in the normal ('AT') manner.

VBEN uses *INDEX* 01h, Bit 4

To use the Video BIOS memory window for the Video BIOS set INDEX 01h Bit 4 to '1' (See *INDEX* 01h *General setup bits*). All WRITE operations are thus routed to RAM and all READ operations are routed to the expansion bus.

VBSHADOW uses INDEX 01h, Bit 0

The Video BIOS can be copied to shadow RAM by writing it byte-for-byte back to itself: the 32-bit version replaces the 16-bit. When the cloning operation is complete, high speed access of video BIOS routines (in shadow RAM) is activated by setting Bit 0 of INDEX 01h to '1'.

The physical memory used for shadowing the video BIOS is located at C0000h - CFFFFh. The system must have enough installed RAM to populate this region of the memory map.

Window 2 - Lower BIOS

By default (after startup), the Window 2 memory space is a 'shadowed' copy of the Window 4 address space. Any READ operations cause access to the Window 4 space: WRITE operations are directed to shadow RAM.

LBSHADOW uses INDEX 00h, Bit 6

In a manner similar to that of video BIOS shadowing, the bootstrap routine must copy the Lower BIOS back to itself: the 32-bit version replaces the 16-bit. When cloning is complete the program can set Bit 6 of INDEX 00h to '1' that activates the use of the 32-bit Lower BIOS access. (See INDEX00h *'General setup bits'*). (See Note(*).

The physical memory used for shadowing the Lower System BIOS is located at F0000h - FFFFFh for Type 27256 EPROM s. (Location E0000h - FFFFFh for Type 27512 EPROM s). The system must have enough installed RAM to populate this region of the memory map.

Window 3 - Middle BIOS

In a manner similar to the Video BIOS shadowing, the bootstrap must copy the Middle BIOS back to itself.

MBSHADOW uses INDEX 00h, Bit 7

When cloning is complete the program can set Bit 7 of INDEX 00h to '1' to activate high speed Middle BIOS access.

The physical memory used for shadowing the Middle BIOS is located at FF0000h - FFFFFFh for Type 27256 EPROM s. (Location FE0000h - FFFFFFh for Type 27512 EPROM s). The system must have enough installed RAM to populate this region of the memory map.

It should be noted that the cloning of Lower BIOS has no effect on Middle BIOS, nor does Middle effect Lower BIOS. If both BIOS systems are to be executed from shadow RAM, both Lower and Middle BIOS must be explicitly copied.

CAUTION

The combined use of both the shadow RAM feature and the REMAP feature (if Bit 5 of INDEX 01h is set to '1') may cause the chip set to lock up. That, very effectively, crashes the host system.

NOTE: Shadowing of Window 4 is not possible.

Sample code

The accompanying 8086 program can be included in a BIOS to 'shadow RAM' the Video and Lower BIOSs.

The minimum amount of DRAM that the machine can accommodate is 1 Mb—the LBSHADOW requires sufficient DRAM to place the shadow.

At the minimum level of installed DRAM, the chip set attempts to shadow the EPROM to backplane memory located at FF0000h. So, if shadowing is required (and DRAM does not exist at these higher addresses), it is possible to use a memory board on the backplane at the higher address and have the chipset shadow EPROM out of this RAM.


```
;
; Shadow the Lower BIOS and Video BIOS
; in a GCK131 based 80386 system.
;
; It is assumed that 27512 ROMs are being used
;
; Registers: AX, BX, and DS are modified
;
; -------------------------------
; ! shadow the lower system BIOS !
; -------------------------------
;
start:
;
; copy first 64K block to shadow RAM
;
    mov     ax,0E000H
    mov     ds,ax     ; DS < -seg of lower BIOS
    mov     bx,00000H                    ; BX <- dsp of lower BIOS
loop1:
    mov     ax,[bx]   ; read ROM
    mov     [bx],ax             ; write shadow RAM
    inc     bx        ; next 16 bit word
    inc     bx
    cmp     bx,0      ; finished ?
    jne     loop1               ; no
;
; copy second 64K block to shadow RAM
;
    mov             ax,0F000H
    mov             ds,ax
loop2:
```

Figure 8f—Shadow RAM *program code*

```
    mov     ax,[bx]             ;-read ROM
    mov     [bx],ax             ; write shadow RAM
    inc     bx                  ; next 16 bit word
    inc     bx
    cmp     bx,0                        ; finished ?
    jne     loop2               ; no
;
; activate lower BIOS shadow RAM
;
    mov     al,000H
    out     024H,al             ; select reg 00H
    in      al,028H             ; read reg 00H
    or      al,040H             ; set bit 6
    out     028H,al             ; update register
; -------------------------
; ! shadow the video BIOS !
; -------------------------
; enable the video BIOS shadow RAM feature
;
    mov     al,001H
    out     024H,al             ; select reg 01H
    in      al,028H             ; read reg 01H
    or      al,010H             ; set bit 4
    out     028H,al             ; update register
;
; copy the video BIOS to shadow RAM
;
    mov     ax,0C000H
    mov     ds,ax               ; DS < -seg of video BIOS
    mov     bx,00000H                   ; BX <- dsp of video BIOS
loop3:
    mo      ax,[bx]             ; read ROM
    mov     [bx],ax             ; write shadow RAM
    inc     bx                  ; next 16 bit word
    inc     bx
    cmp     bx,0                        ; finished ?
    jne     loop3               ; no
;
; activate video BIOS shadow RAM
    mov     al,001H
    out     024H,al             ; select reg 01H
    in      al,028H             ; read reg 01H
    or      al,001H             ; set bit 0
    out     028H,al             ; update register
; all done
;
```

Figure 8f—Shadow RAM *program code (Continued)*

4 - 6 Use the REMAP feature to save unused RAM space

In the standard AT memory map the address space from A0000h to FFFFFh is normally reserved for device and ROM usage.(*See Figure 8a.*)

When more than 640K of memory is installed on a *GCK131*-based system, RAM that might otherwise be mapped into the device/ROM region is blanked out and is not accessible. For cost sensitive applications this represents an effective loss of up to 384K of expensive RAM memory.

This region of unused RAM can be reclaimed by activating the shadowing feature. With REMAP, up to 384K of memory becomes useful and is remapped into another section of the 80386 memory map. With REMAP, the user has the option of relocating this section of RAM memory to one of the address ranges shown below

Programming the Configuration Registers

- Option 1—Append to the first megabyte. (100000h to 15FFFFh.)

  Used only when 1 Mb of memory is populated with 256K DRAMs (one bank installed).

- Option 2—Append to the second megabyte. (200000h to 25FFFFh.)

  Used only when 2 Mb of memory is populated with 256K DRAMs (two banks installed).

- Option 3—Append to the fourth megabyte. (400000h to 45FFFFh.)

  Used only when 4 Mb of memory is populated with 1 Mb DRAMs (one bank installed).

The REMAP feature cannot be used with memory configurations other than those noted above.

CAUTION
The combined use of both the shadow RAM feature and the REMAP feature (if Bit 5 of INDEX 01h is set to '1') may cause the chip set to lock up. That, very effectively, crashes the host system.

How to activate REMAP

The REMAP feature is activated when these conditions are true:

1. The Shadow RAM feature is turned OFF,
2. The amount of memory in the system has been configured, then
3. Bit 5 of the general setup register INDEX 01h is set to '1', and
4. Bit 3 of DRAM configuration register INDEX 10h is set to '1'.

CAUTION

If these three conditions are not true—and especially if the register bits 01h and 10h are set before memory has been configured—the chip set will be confused as to which REMAP option (1, 2, or 3) to use. This may result in erratic system operation.

More about REMAP

Once the REMAP feature is turned ON, 32-bit shadow RAM is not available and any user who attempts this may corrupt the memory map.

A feature associated with remapping modifies the earlier comment. The DRAM located from 640K (A0000h) to 1 Mb (FFFFFh) is remapped to a different location when REMAP is turned ON. Thus, there will be no DRAM available to shadow; instead, shadow will be to the backplane RAM. By this process, it is possible to use the backplane RAM for shadowing and still also activate the REMAP feature.

4 - 7 Memory map of the DRAM subsystem

The DRAM control system is made complex by the variety with which the INDEX registers (described in the earlier *Configuration Register* Section) can alter configuration, and affect the address space of the DRAMs used in the *GCK131 Chip Set.* The chip set can accommodate 256K DRAMs, 1 Mb DRAMs (but not a mixture of the two types). From one to six banks of page/interleaved DRAM can be configured. And, several options exist with respect to the use of address space.

Programming the Configuration Registers

One bank of RAM

This—the single bank of installed RAM—is a special case because it is the only situation in which interleaving does not occur. At least two banks are required for interleaving.

The memory map for the single and double banks of installed RAM is illustrated in Figure 8g. For clarity, the RAM shadowing, REMAP, and the EMS 'hole' features (described later in this document) are disabled.

With 256K DRAMs, the memory capacity is 1 Mb; but, due to the definition of the AT memory map, only the first 640K is reachable. The rest is defined as backplane memory.

If nothing is done to change this situation, the DRAM residing from 640K to 1 Mb is wasted. If 1 Mb DRAMs are installed the memory capacity is 4 Mb; but again, the 384K above 640K is wasted. (See the *REMAP* Section).

The *GCK131 Chip Set* has allotted, within it, two shadow regions between 640K and 1 Mb. These are described in the previous Section as EPROM shadowing and Video shadowing.

Two banks of DRAM

As soon as two banks of DRAM are recognized, the *GCK131 Chip Set* starts interleaving. Interleaving takes place on double-word boundaries. The memory map (Figure 8h) shows two configurations—banks of 256K DRAMs and banks of 1 Mb DRAMs.

Shadowing works, as before; but, REMAP does not. In order to allow the internal address decoder to be as simple as possible, the REMAP feature is implemented only on smaller configurations. For two banks of 1 Mb DRAMs REMAP is NOT implemented. It is, however, implemented for two banks of 256K DRAMs. This is illustrated in the following Figures.

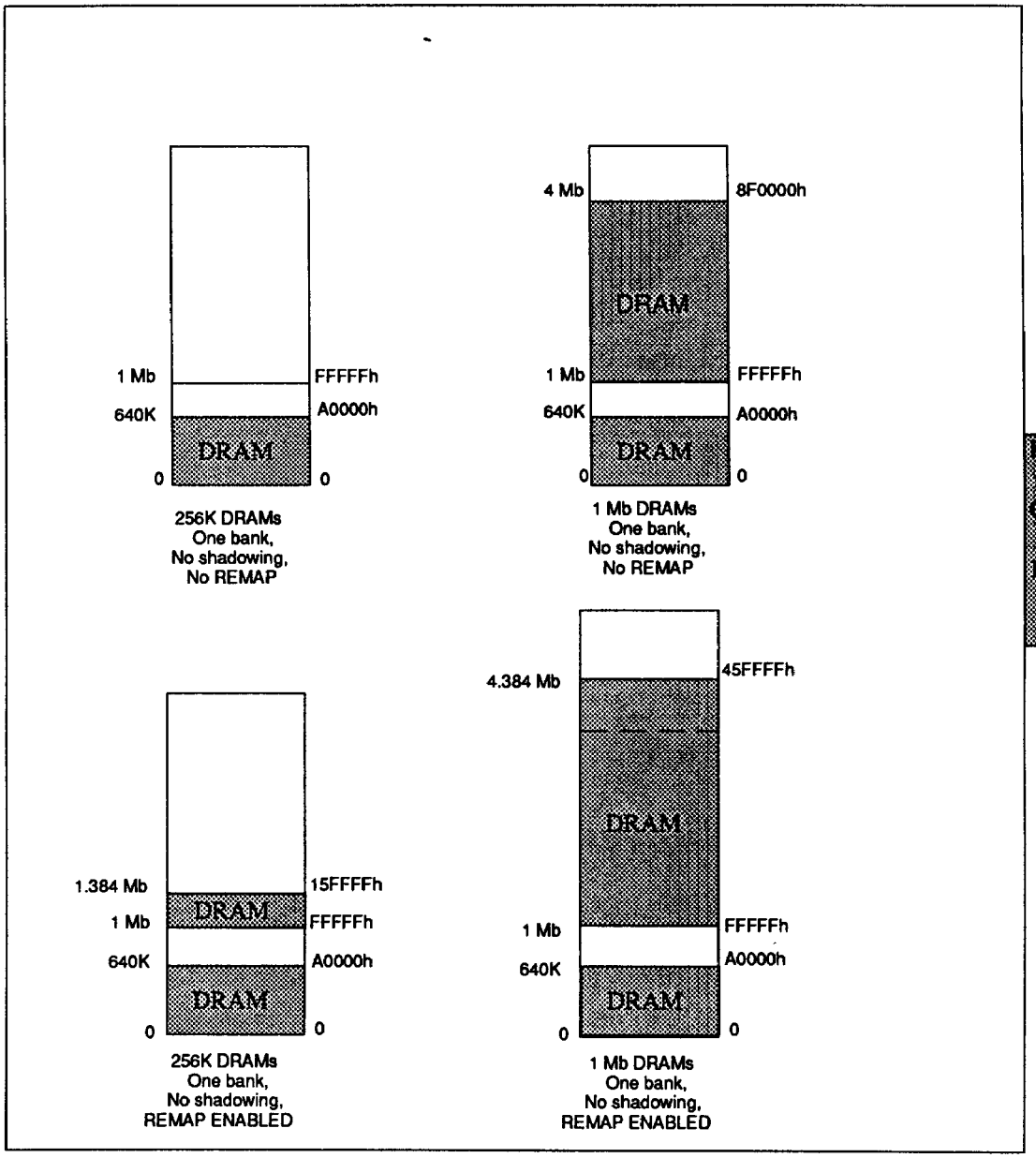


Figure 8g—The effects of REMAP with one bank of RAM

Four banks of DRAM

As with the two banks of DRAM, four banks of DRAM will interleave but this is not, strictly speaking, four-way interleaving. As shown in Figure 8i, if the processor is accessing Location 0, the consecutive reads are: BANK 0, BANK1, BANK0, BANK1, BANK0, and so on.

This continues until (at a much higher address) the chip set switches to BANKS 2 and 3. The interleaving then cycles in this manner: BANK2, BANK3, BANK2, BANK3, and so on.

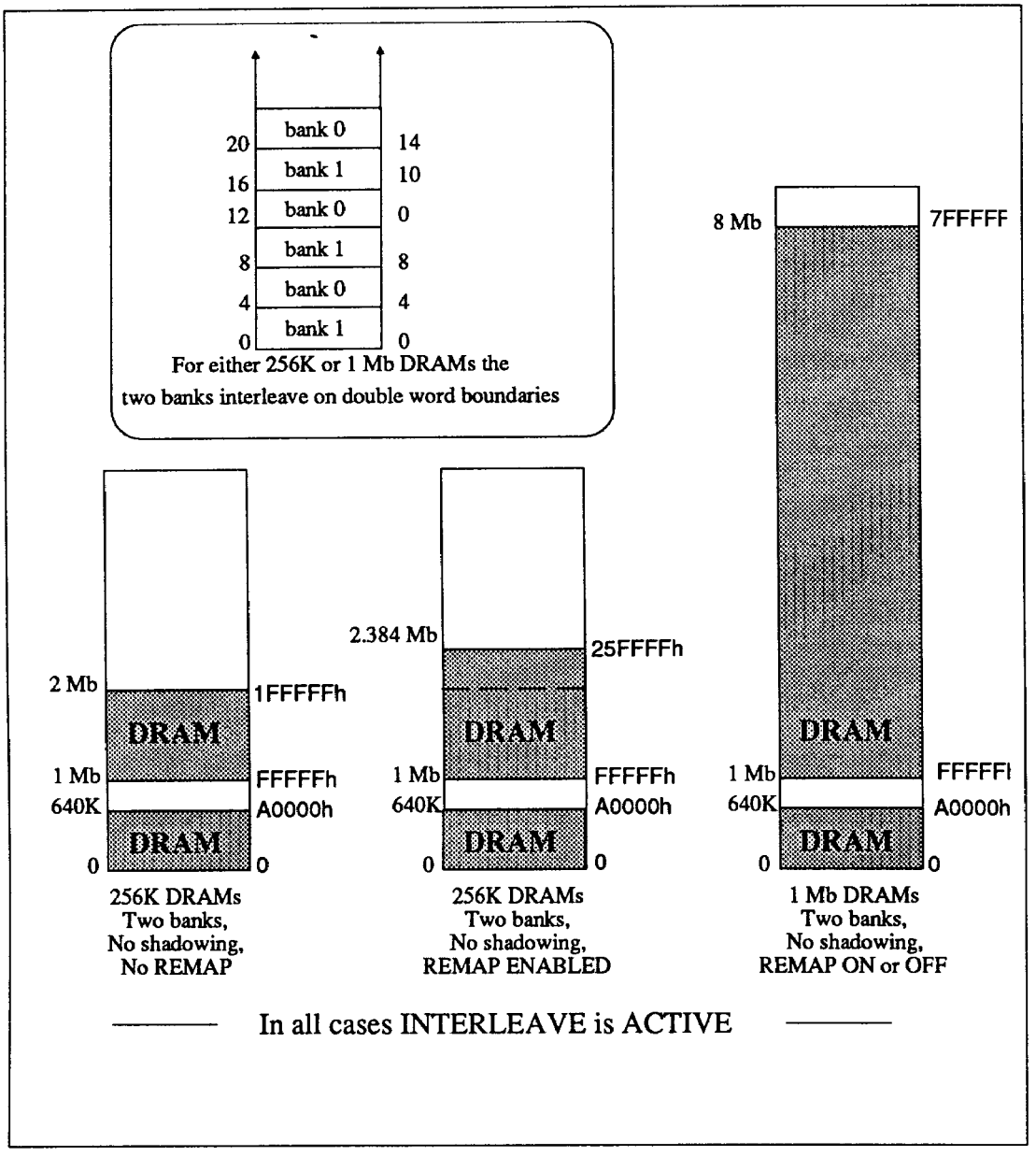


Figure 8h—The effects of REMAP with two banks of RAM

The change (from BANK0/BANK1 to BANK2/BANK3 interleaving) takes place at 2 Mb for 256K RAMs and 8 Mb for 1 Mb RAMs.

True 'four-way' interleaving requires the use of either four or eight banks
Incidentally, an example of 'true' four-way interleaving would follow the sequence: BANK 0, BANK1, BANK2, BANK3, BANK 0, BANK1, BANK2, BANK3, and so on. But, for this to work properly, the user's system must be fitted with an even multiples of four banks (either, 4 banks or 8 banks).

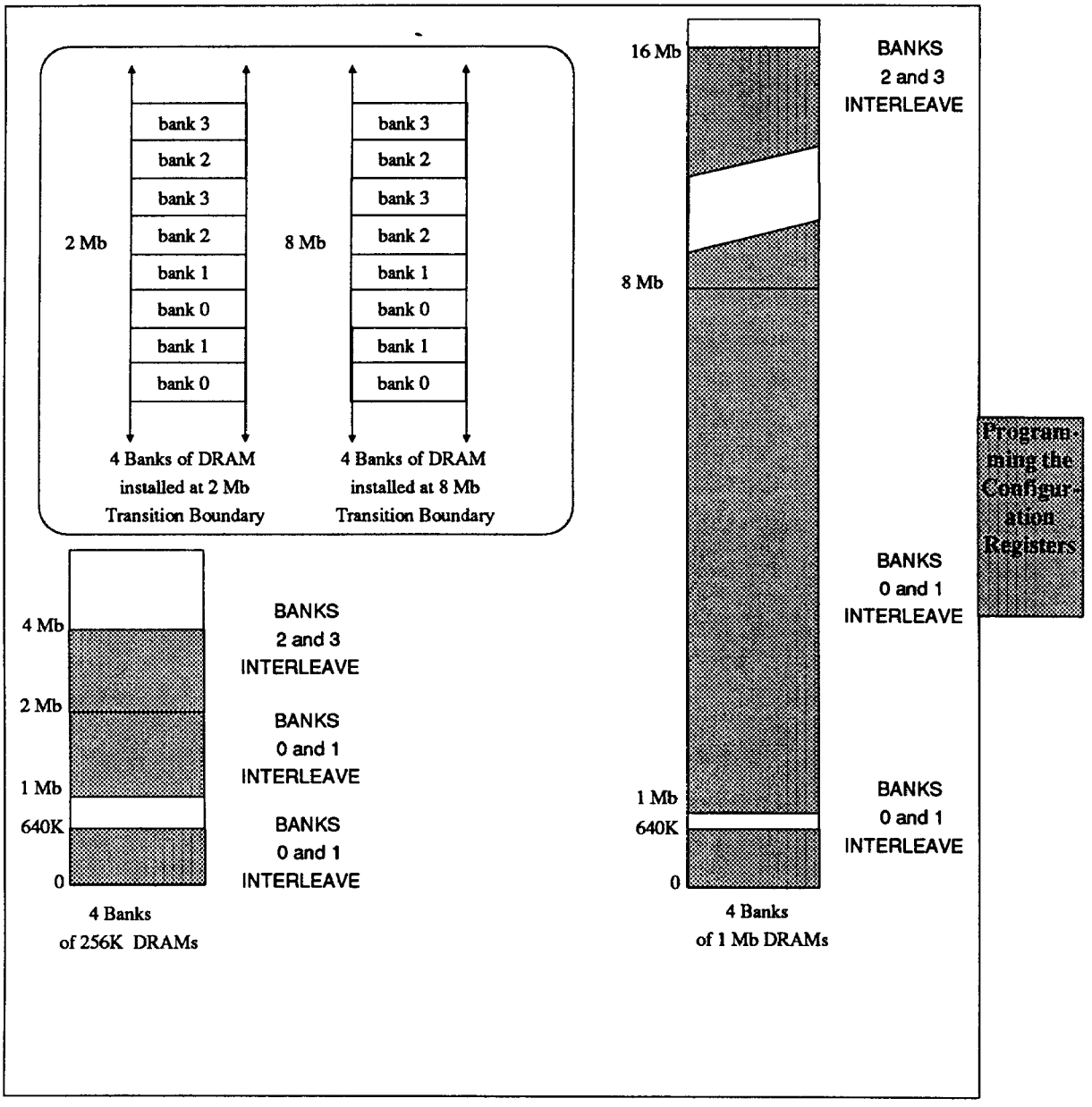


Figure 8i—The effects of REMAP with four banks of RAM

The user couldn't use this interleaving method with (for example) five banks of installed DRAMs. The modified four-way interleaving, on the other hand, which requires the use of paired DRAM s is less restrictive on the user's configuration).

Six Banks

When the last two banks are added, DRAM is treated in a different manner. The fifth and sixth banks have their own ENABLE configuration bits (See INDEX 0h, Bit 4) and their own set of timing configuration regsisters (See INDEX 05h). Typically, no machine has more than four banks of DRAM on the main memory board (due to the expense): above this point, in design, plug-in memory boards are used. The plug-in boards (typically) have buffered DATA, ADDRESS, and RAS/CAS signals which would necessarily have timing that differs from those of the on-board DRAM; hence, a new set of timing configuration registers are needed.

Once the banks are enabled, they must be populated with the same DRAMs as Banks 2 and 3. This means that Banks 0,1,2, and 3 must be populated before Banks 4 and 5 are turned ON.

Summary of available DRAM configurations

Total Amount of RAM	Total Usable DRAM	DRAM Type for each bank 0	1	2	3	4	5	REMAP Available	LB SHADOW	VB- & MB-SHADOW
1 Mb	1 Mb	256K	-	-	-	-	-	Yes	Yes	Yes
2 Mb	2 Mb	256K	256K	-	-	-	-	Yes	Yes	Yes
4 Mb	3.64 Mb	256K	256K	256K	256K	-	-	No	Yes	Yes
6 Mb	5.64 Mb	256K	256K	256K	256K	256K	256K	No	Yes	Yes
4 Mb	4 Mb	1 Mb	-	-	-	-	-	Yes	Yes	Yes
8 Mb	7.64 Mb	1 Mb	1 Mb	-	-	-	-	No	Yes	Yes
16 Mb	15.64 Mb	1 Mb	1 Mb	1 Mb	1 Mb	-	-	No	Yes	Yes
24 Mb	23.64 Mb	1 Mb	1 Mb	1 Mb	1 Mb	1 Mb	1 Mb	No	Yes	Yes

Figure 8j—Summary of available DRAM configurations

4 - 8 EMS Hole

The *GCK131 Chip Set* can be configured to accommodate a 64K 'hole', in the memory map, below 640K. This feature enables the use of EMS memory cards that need a 64K spot to position their memory (within the range 256K to 768K).

The 64K hole appears, to the system, as offboard RAM.

INDEX0 3h, in the *GC132 Controller*, configures this feature. The startup default places the 64K hole at A0000h. Figure 8k shows a sample memory map with the 'hole' placed at 40000h

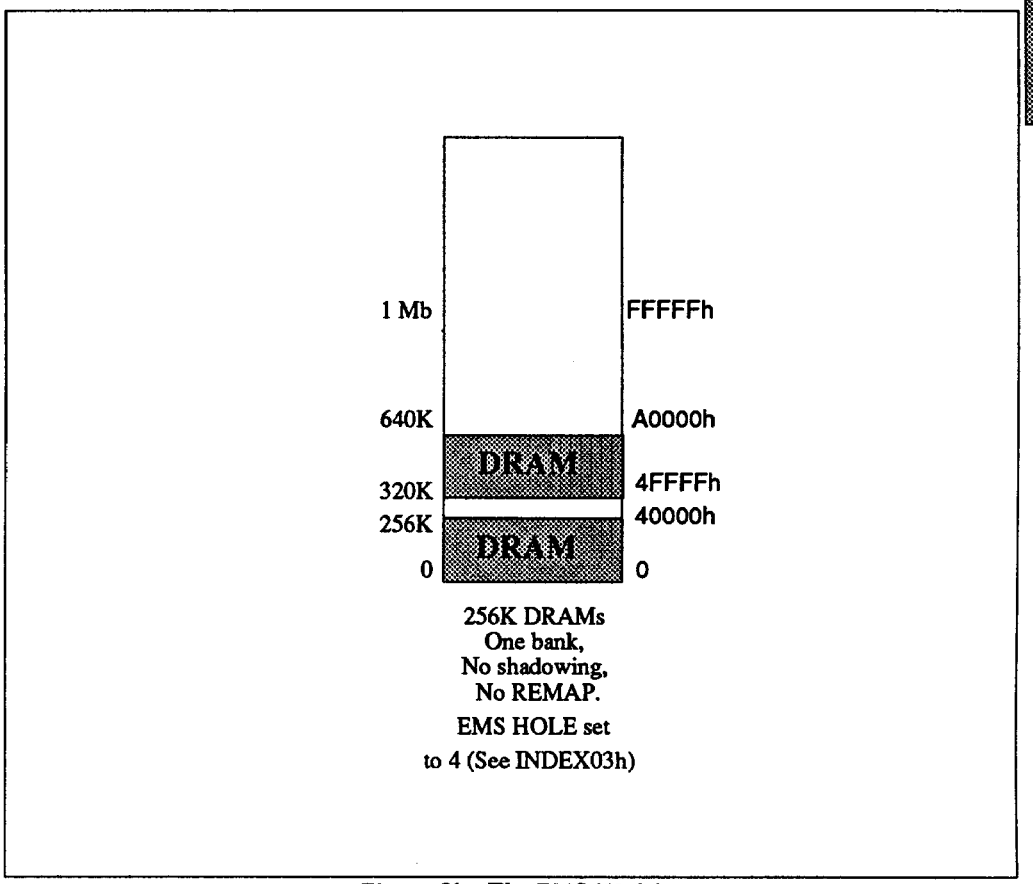


Figure 8k—The EMS 'Hole'

4 - 9 Connecting multiple banks of DRAM to the CGK131 Chip Set

Up to four banks

The recommended method by which up to four banks of DRAM can be connected is shown in Application schematics 386APP_1 (Figure 9a).

Six banks

Since only two BANKSEL signals are available (and when six banks of DRAM are installed), Banks 4 and 5 must be selected in a manner different to that used for Banks 0 through 3.

For Banks 4 and 5, the recommended system makes use of the /EXRAS_0 and /EXRAS 1 signals (when the upper banks are selected). This is shown in Application schematic 386APP_2 *(Figure 9b)*.

Programming the Configuration Registers

In drawing 386APP_2, the NAND gate is required to ensure that only one bank can be selected at one time.

The individual /RAS lines (/RAS0.../RAS3 and /EXRAS 0, /EXRAS 1) are buffered by the 74F244 package for application directly to the corresponding bank. *Drawing 386APP_5 (Figure 9c)* shows the recommended buffering and bank assignments.

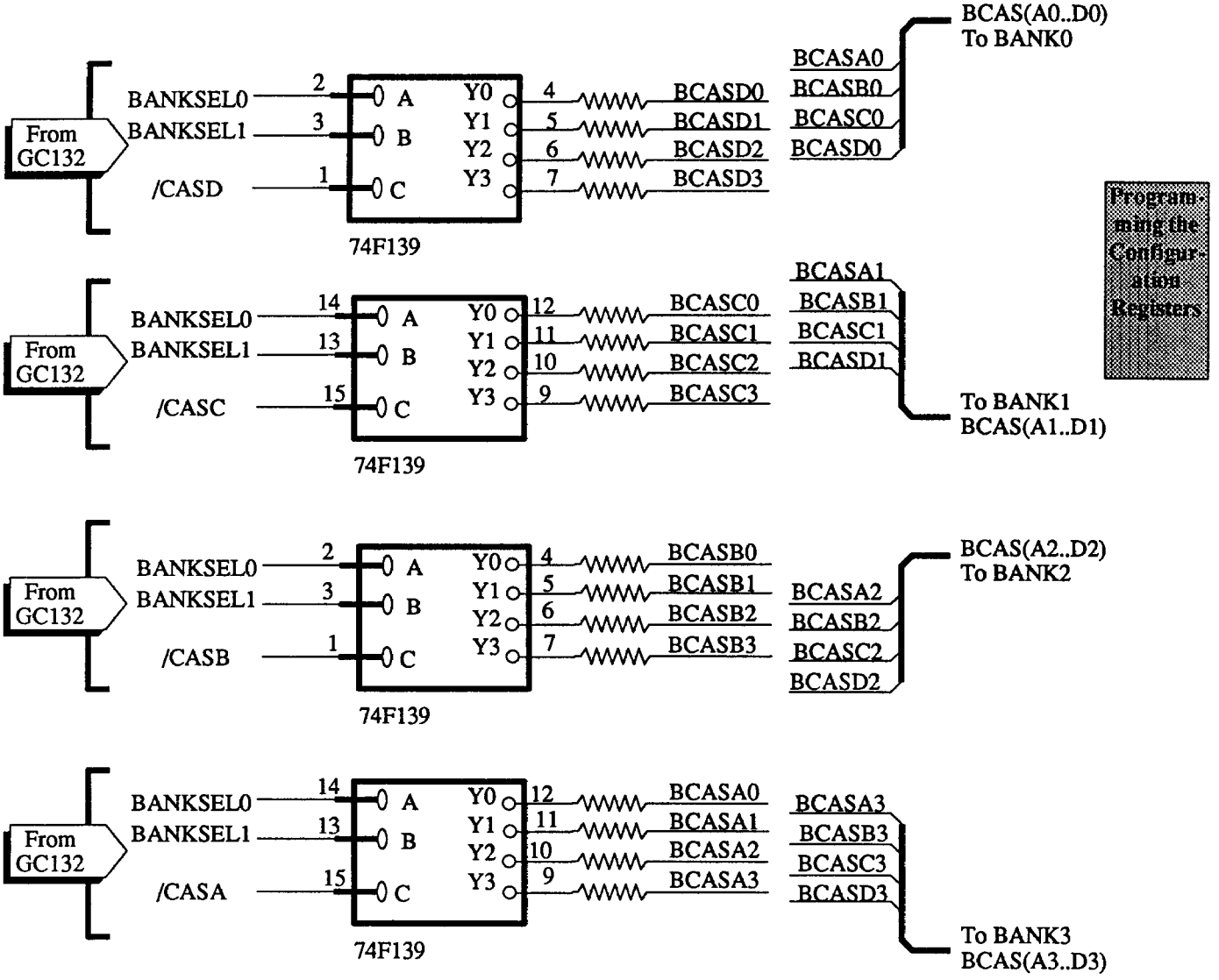


Figure 9a—Connecting 4 banks of RAM - 386APP_1

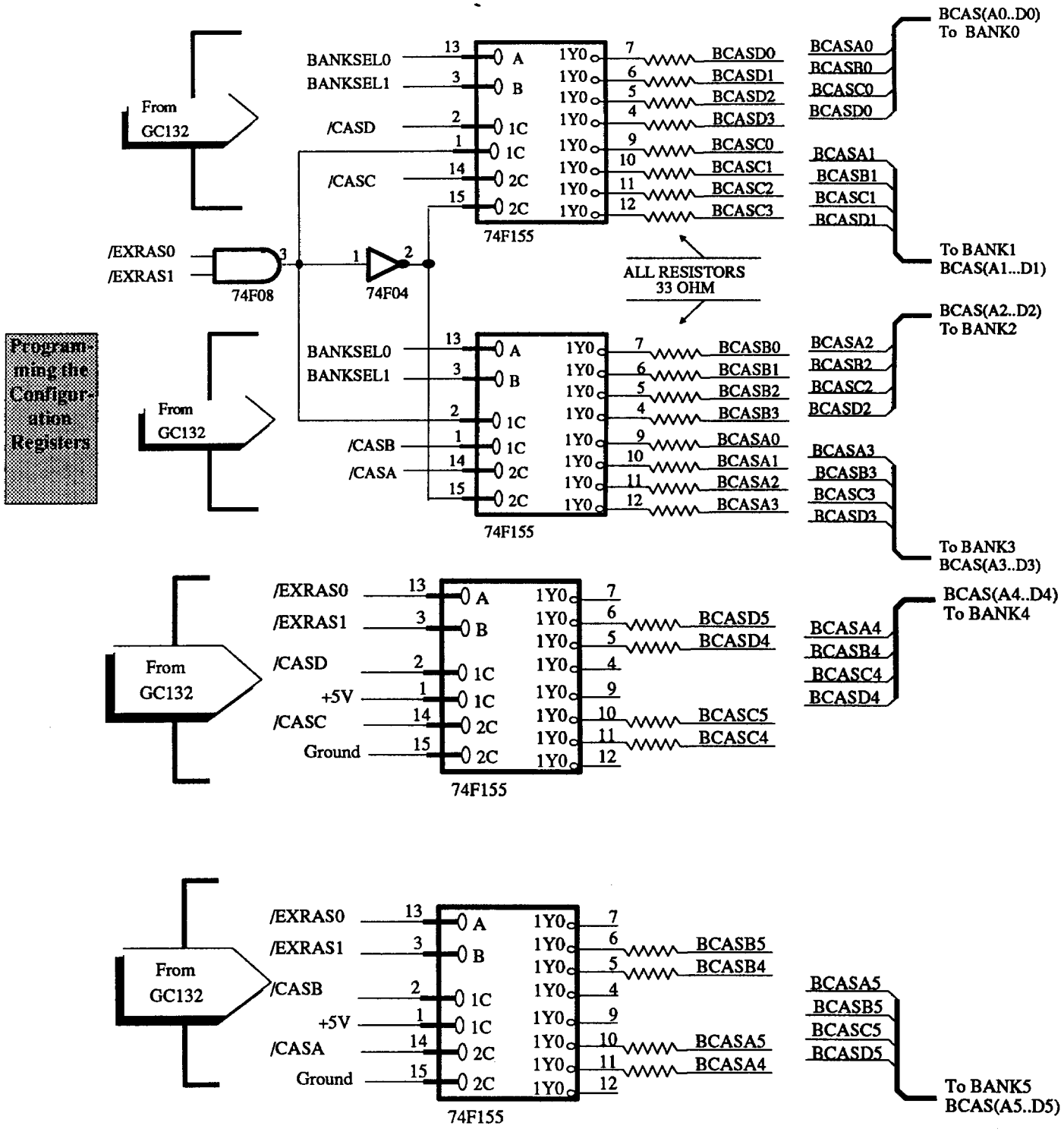


Figure 9c - Connecting RAS signals to the DRAMs - 386 APP_1

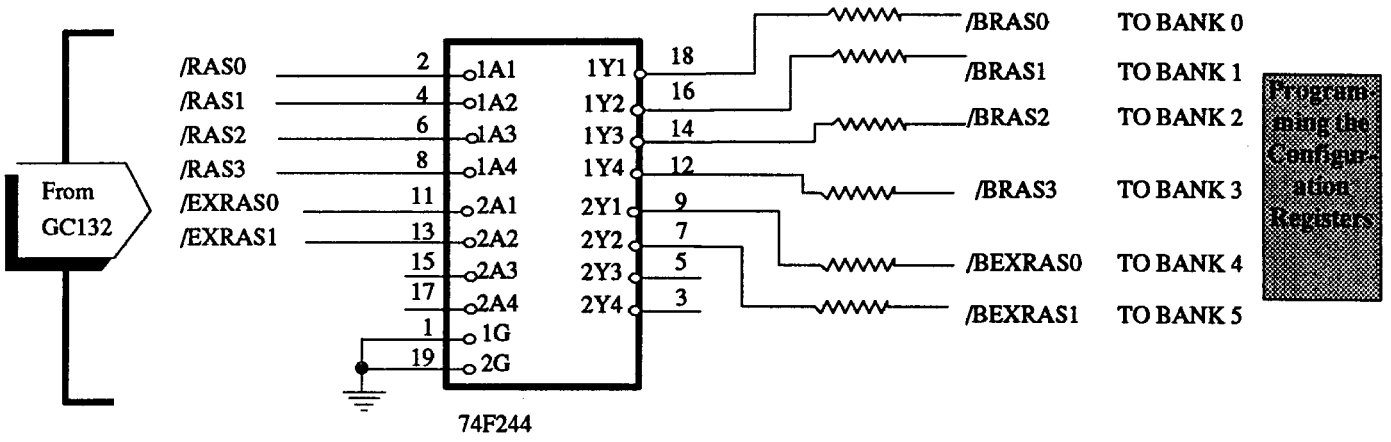


Figure 9c—Connecting RAS signals to the DRAMs - 386APP_5

Programming the Configuration Registers

Section - 5 GCK131 Chip Set, timing diagrams

This Section of the *GCK131 Chip Set Data Sheet* includes:

- Processor and Coprocessor timing
- RAM timing
- DMA timing
- REFRESH timing
- Interrupt timing
- NMI timing
- ROM access timing
- I/O timing
- Expansion bus timing

Timing diagrams

5 - 1 Processor and Coprocessor timing

Figure 10a shows the timing relationships between the *GCK131 Chip Set*, the 80386 Microprocessor and the 80387 Numeric Coprocessor.

An IRQ 13 signal is generated on the receipt of the /ERROR 387 'active' signal.

Note: The *GCK131 Chip Set* will not perform pipelined operations between the 80386 Microprocessor and the 80387 Numeric Coprocessor.

Timing diagrams

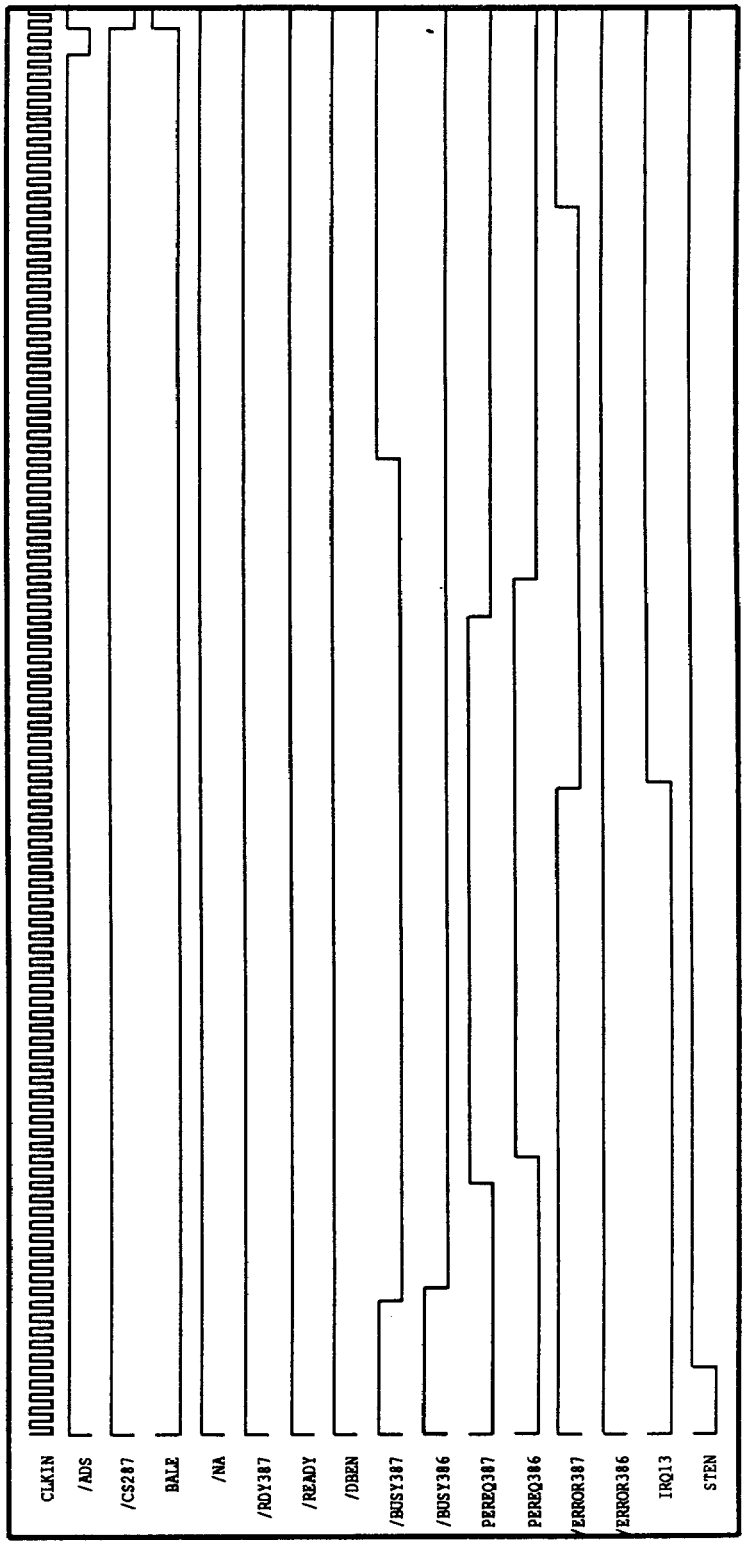


Figure 10a—CPU/Coprocessor Interface Timing

Timing diagrams

5 - 2 I/O READ timing

Figure 10b shows the timing relationships for an I/O READ cycle using the *GCK131 Chip Set.*

IOCHRDY is **not** activated during this cycle. All timings are relative to CLKIN as shown.

The test conditions are as follows:

Command Delays	10 CLKINs
Command Active	18 CLKINs
RECOVERY time	8 CLKINs

Timing diagrams

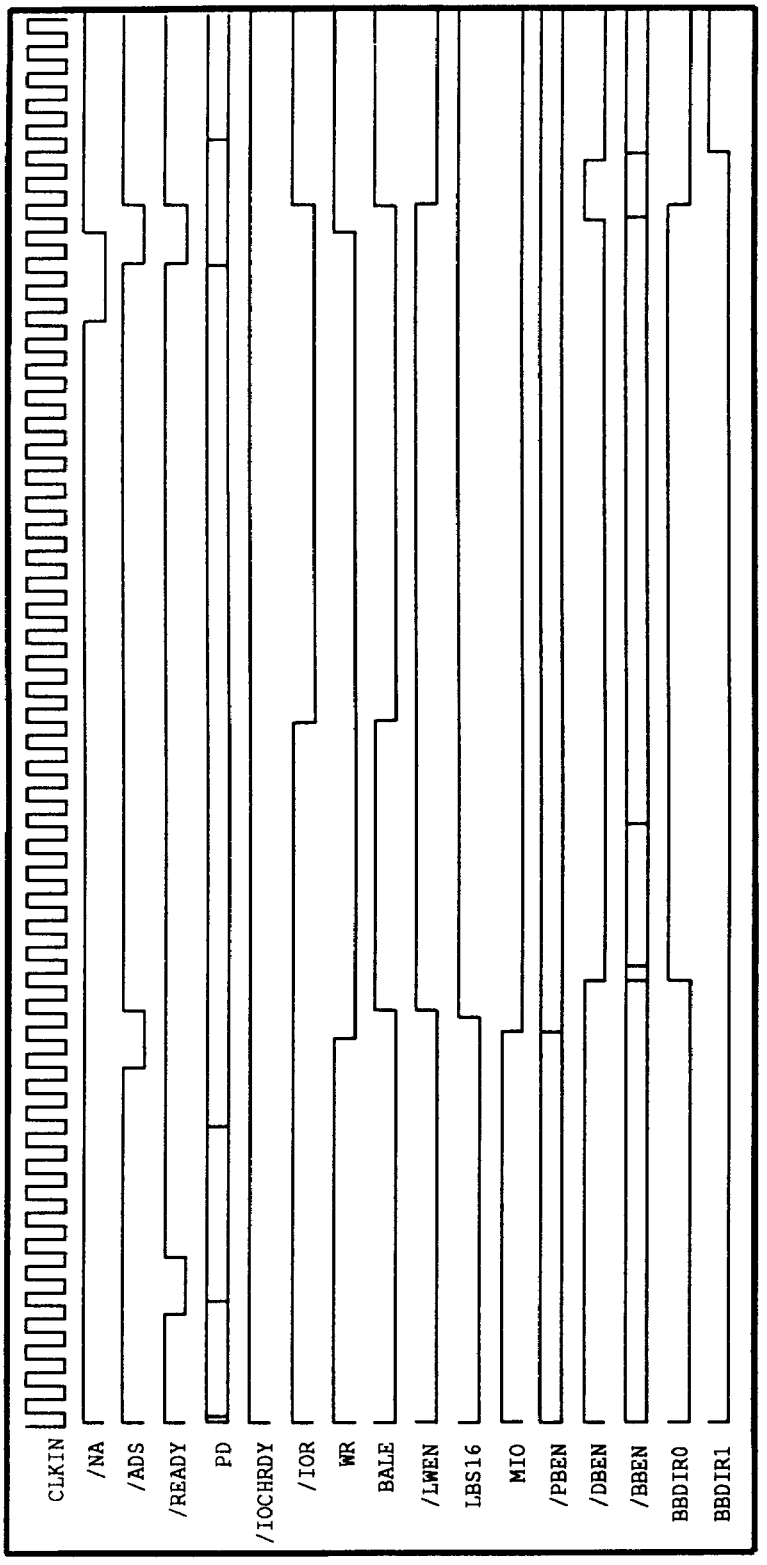


Figure 10b—I/O READ timing

5 - 3 I/O WRITE timing

Figure 10c shows the timing relationships for an I/O WRITE cycle using the *GCK131 Chip Set.*

The test conditions are as follows:

Command Delays	10 CLKINs
Command Active	18 CLKINs
RECOVERY time	8 CLKINs

Timing diagrams

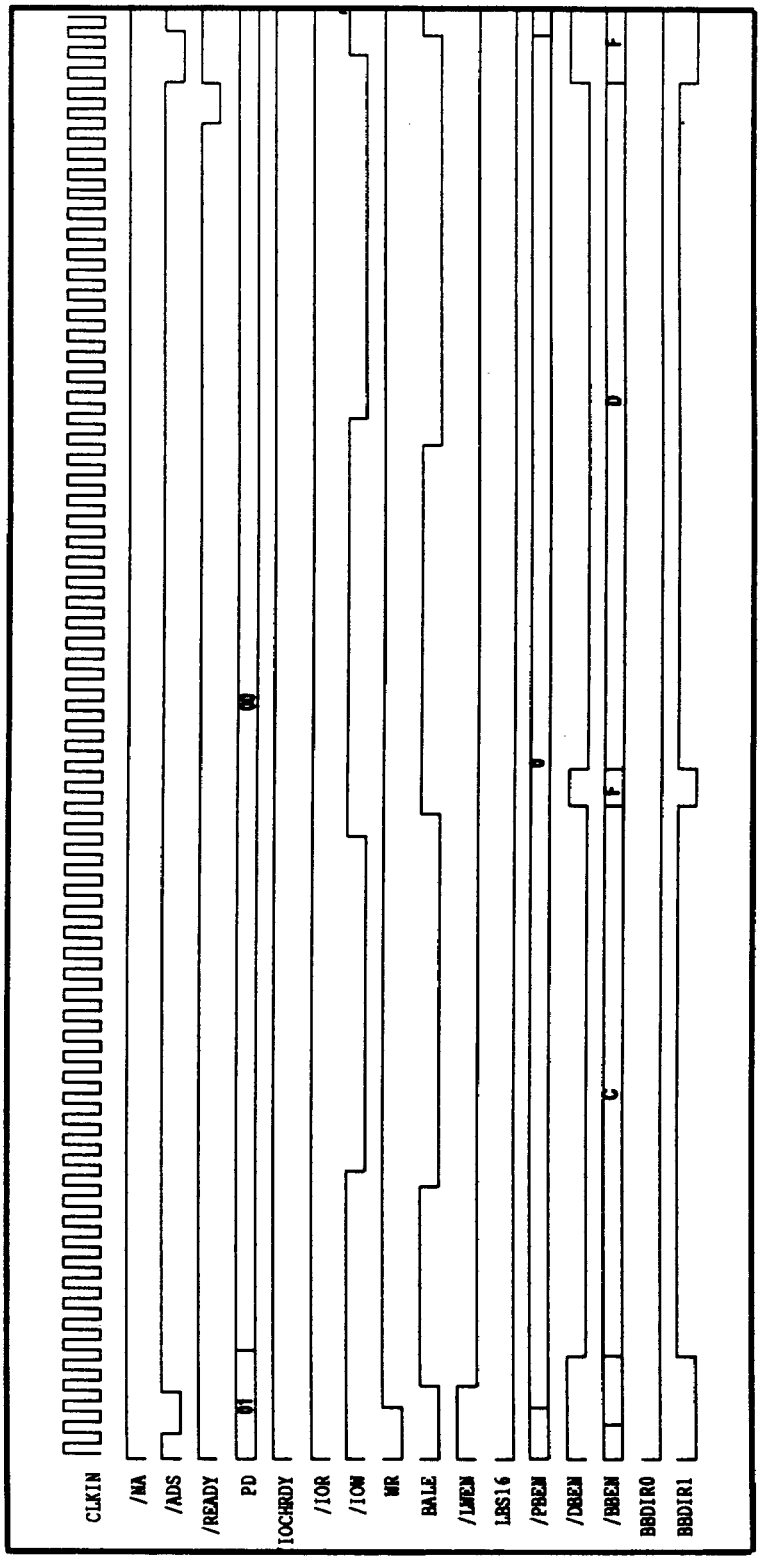


Figure 10c—I/O WRITE timing

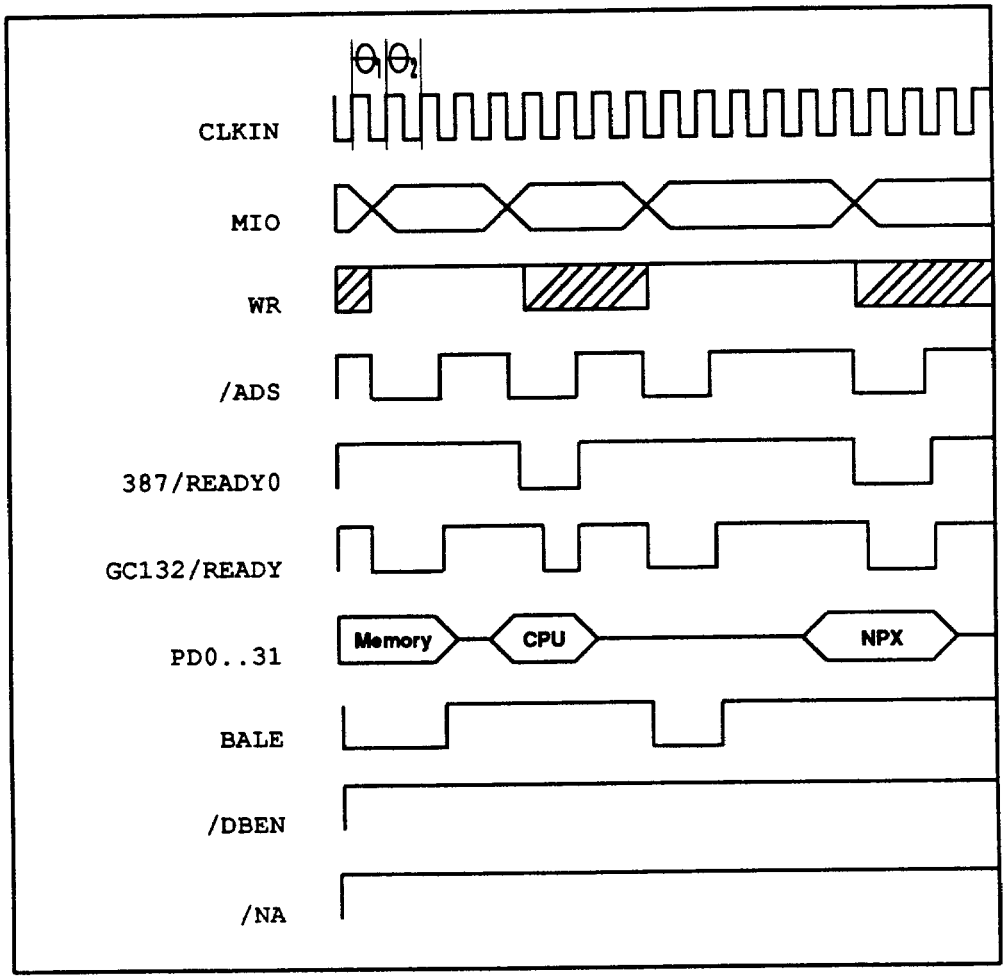
5 - 4 Coprocessor, READ/WRITEtiming

Figure 10d shows the timing relationships between the *GCK131 Chip Set*, the 80386 CPU and the 80387 Numeric Processor Unit (NPU).

A WRITE CPU/NPU cycle is followed by a non-related cycle, then by a READ CPU/NPU cycle.

An access to or from the NPU is detected by the *GCK131 Chip Set* when the MIO signal is LOW and PA31 is HIGH. If these conditions are met, the chip set allows the '387' operation and awaits the /RDY387 signal before commencing the next cycle.

Timing diagrams



5 - 5 CPU RESET timing

Figure 10e shows the timing relationships between the signals CLREXP - TION and the 80386's CLK when using the GCK131 Chip Set.

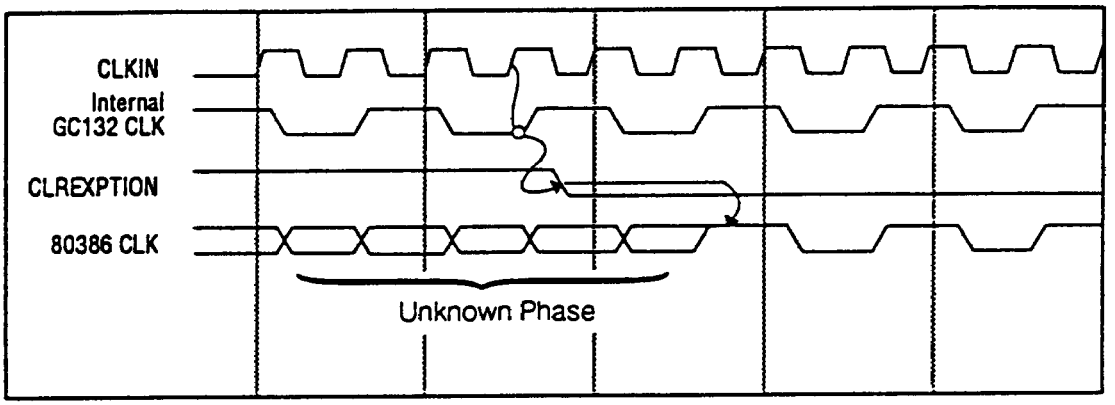


Figure 10e—CPU/CLREXPTION timing

5 - 6 Non-interleaved DRAM timing

Figure 10f shows the timing relationships for a non-interleaved, on-board DRAM access using the *GCK131 Chip Set.*

A pipelined READ cycle is followed by a pipelined WRITE to Bank0 of the RAM.

The test conditions are as follows:

RAS Delay	3 CLKINs
CAS Delay	3 CLKINs
CAS Active	8 CLKINs
RAS Precharge	8 CLKINs
Recovery time	2 CLKINs
MODE	Turbo ON
Interleave	OFF

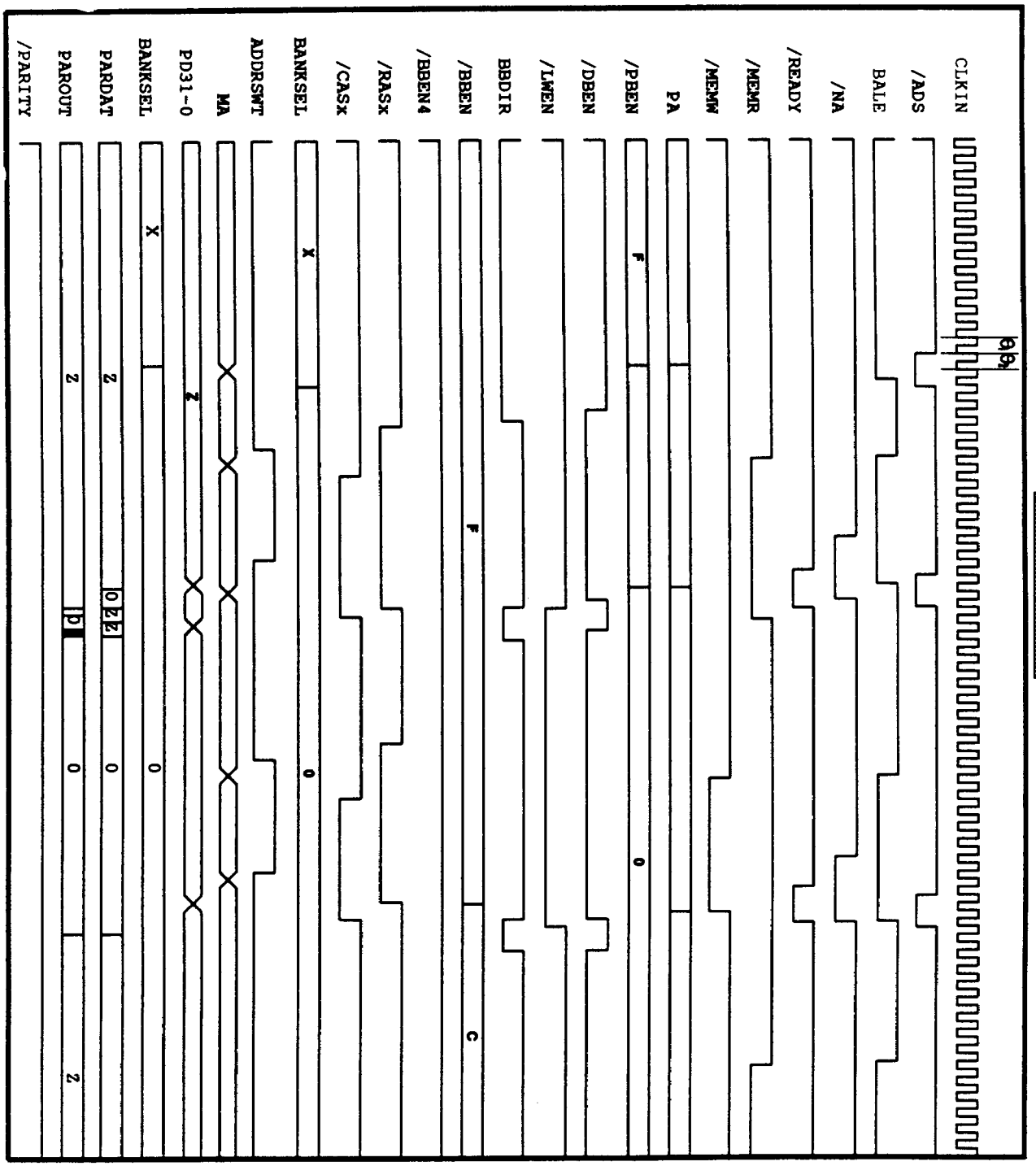


Figure 10f—Non interleaved DRAM timing

Timing diagrams

5 - 7 Interleaved DRAM timing, fastest configuration

Figure 10g shows the timing relationships when using interleaved access to/from the DRAMs.

Two DRAM accesses are shown—with interleave enabled and with configuration registers set to the fastest access possible.

The test conditions are as follows:

RAS Delay	1 CLKINs
CAS Delay	2 CLKINs
CAS Active	2 CLKINs
RAS Precharge	4 CLKINs
Recovery time	0 CLKINs
Interleave	ON

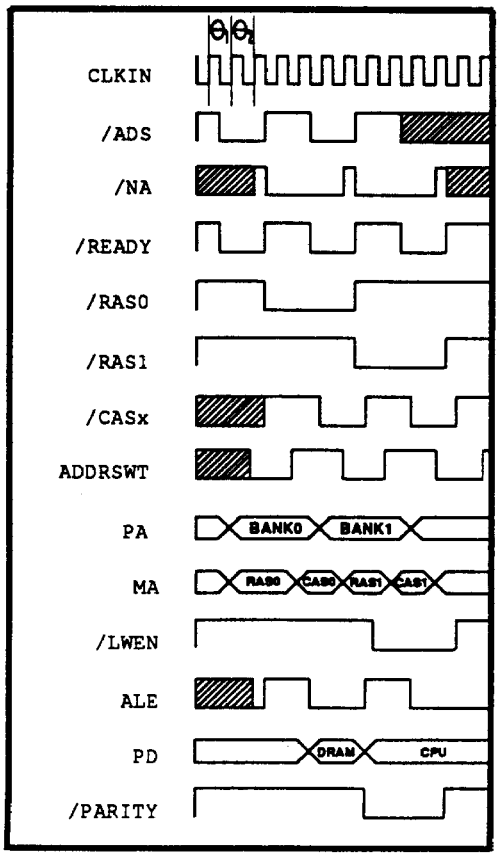


Figure 10g—Interleaved DRAM timing,fastest configuration

5 - 8 16-bit access to 8-bit offboard RAM

Figure 10h shows the timing relationships when accessing 8-bit RAM on the AT-expansion bus using the *GCK131 Chip Set.*

The 16-bit access, from the CPU, is broken into two 8-bit accesses to this backplane memory.

The first 8-bit READ supplies the lower byte. This is followed by the upper byte READ and, together, they yield the whole 16-bit word.

In the illustration, IOCHRDY is asserted during the READ of the lower byte.

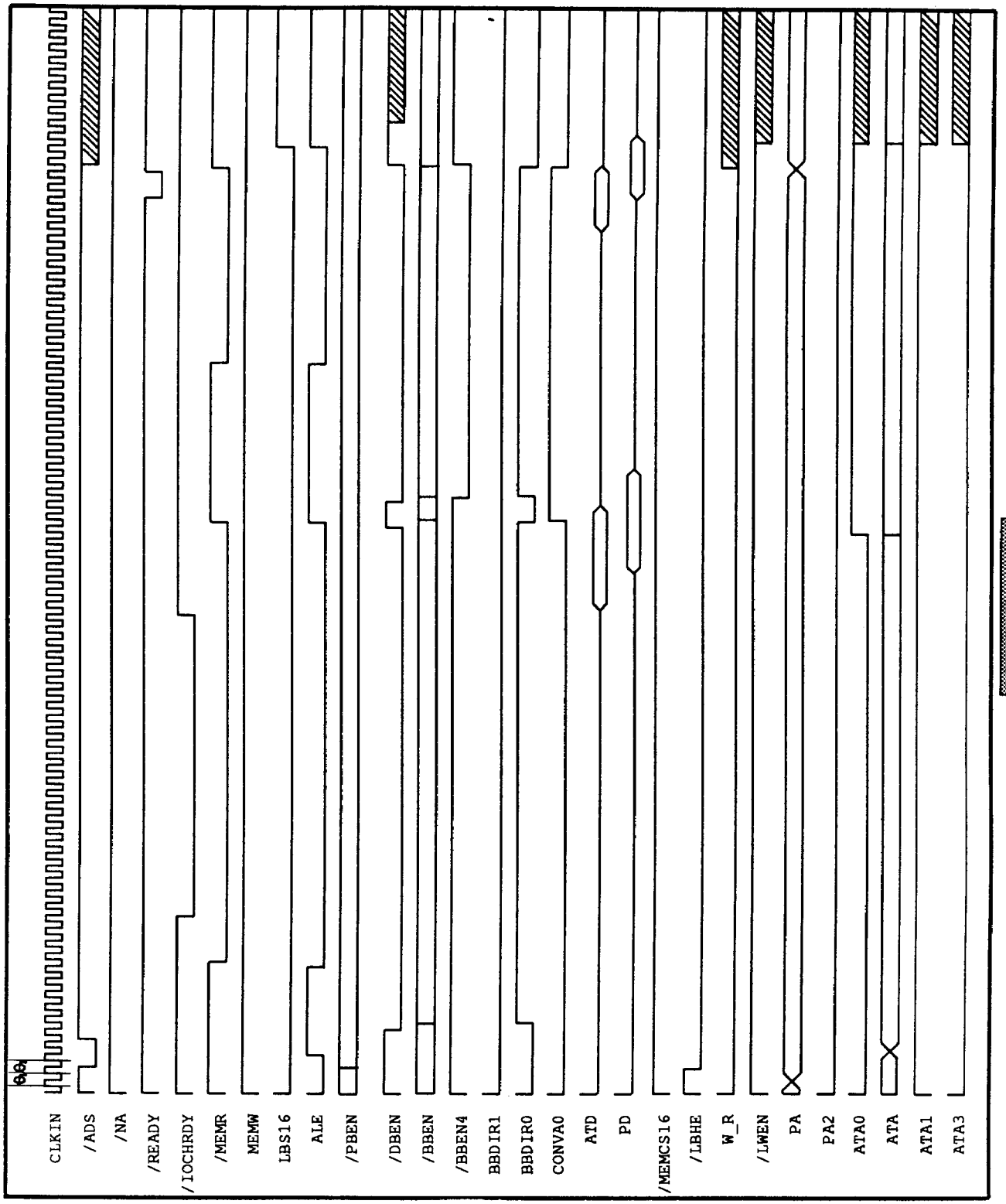


Figure 10h—16-bit access to 8-bit offboard RAM

5 - 9 16-bit access to 16-bit offboard RAM

Figure 10i shows the timing relationships when accessing 16-bit RAM on the AT-expansion bus using the *GCK131 Chip Set.*

An offboard READ command is followed by an offboard RAM WRITE.

In the illustration, IOCHRDY is **not** activated.

The test conditions are as follows:

Command Delay	7 CLKINs
Command Active	13 CLKINs
Recovery time	6 CLKINs

Timing diagrams

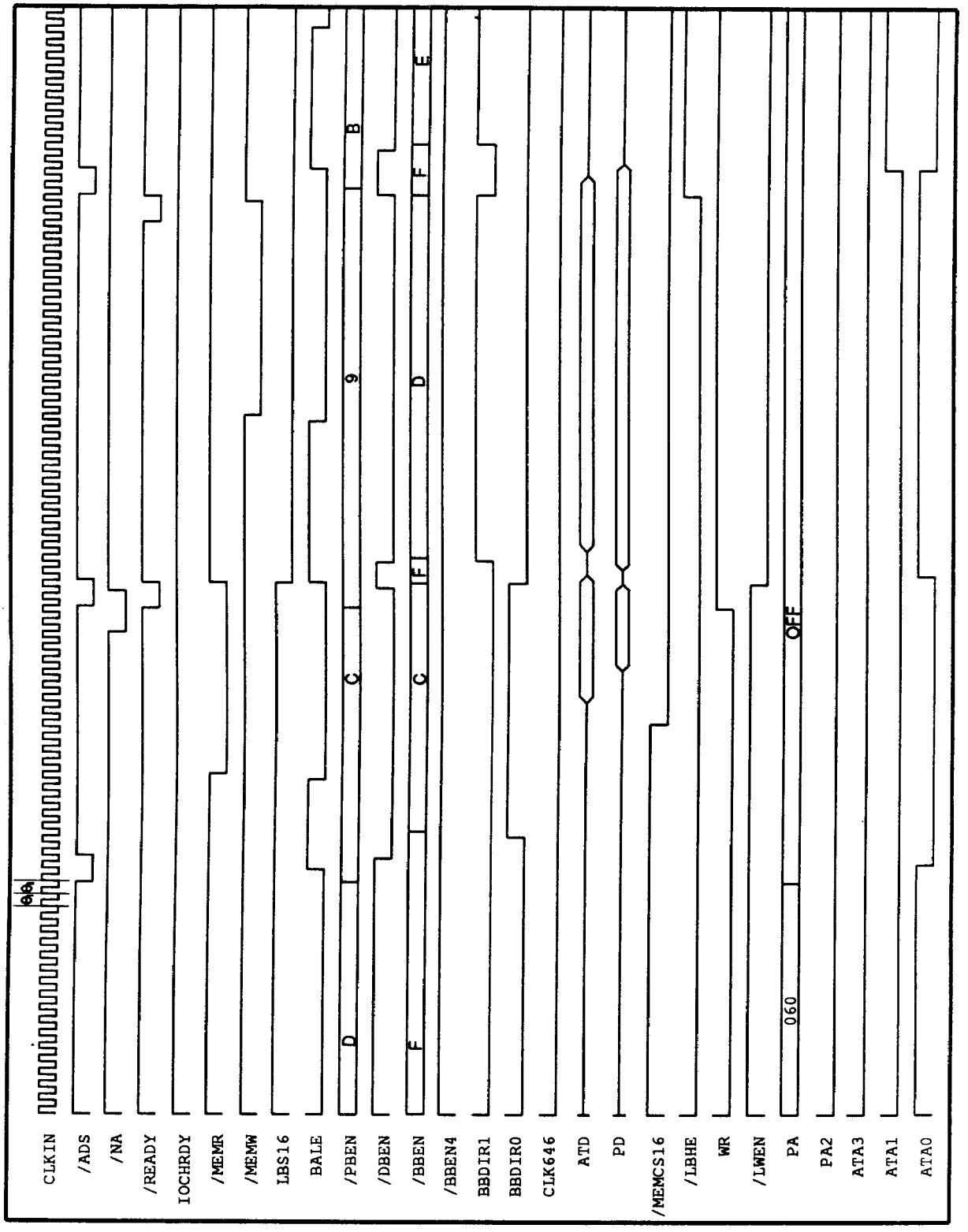


Figure 10i—16-bit access to 16-Bit offboard RAM

5 - 10 PAGED-mode DRAM timing

Figure 10j shows the timing relationships for a PAGED -mode DRAM access using the *GCK131 Chip Set.*

The paging shown is performed on Bank0 of the DRAM .

A page violation (PGVIOL) is also shown, resulting from the next command—a DRAM access to/from another bank.

The test conditions are as follows:

RAS Delay	2 CLKINs
CAS Delay	2 CLKINs
CAS Active	2 CLKINs
RAS Precharge time	4 CLKINs
Recovery time	2 CLKINs

Timing diagrams

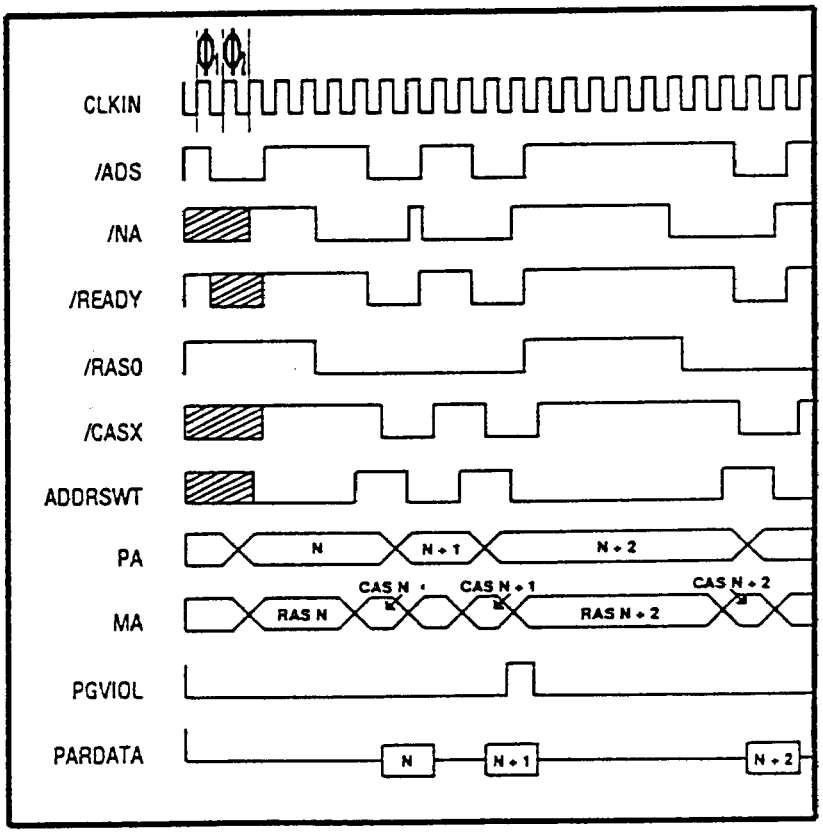


Figure 10j—PAGED mode DRAM timing

Timing diagrams

5 - 11 DMA access timing

Figure 10k shows the timing relationships for direct memory access DMA operations in the *GCK131 Chip Set.*

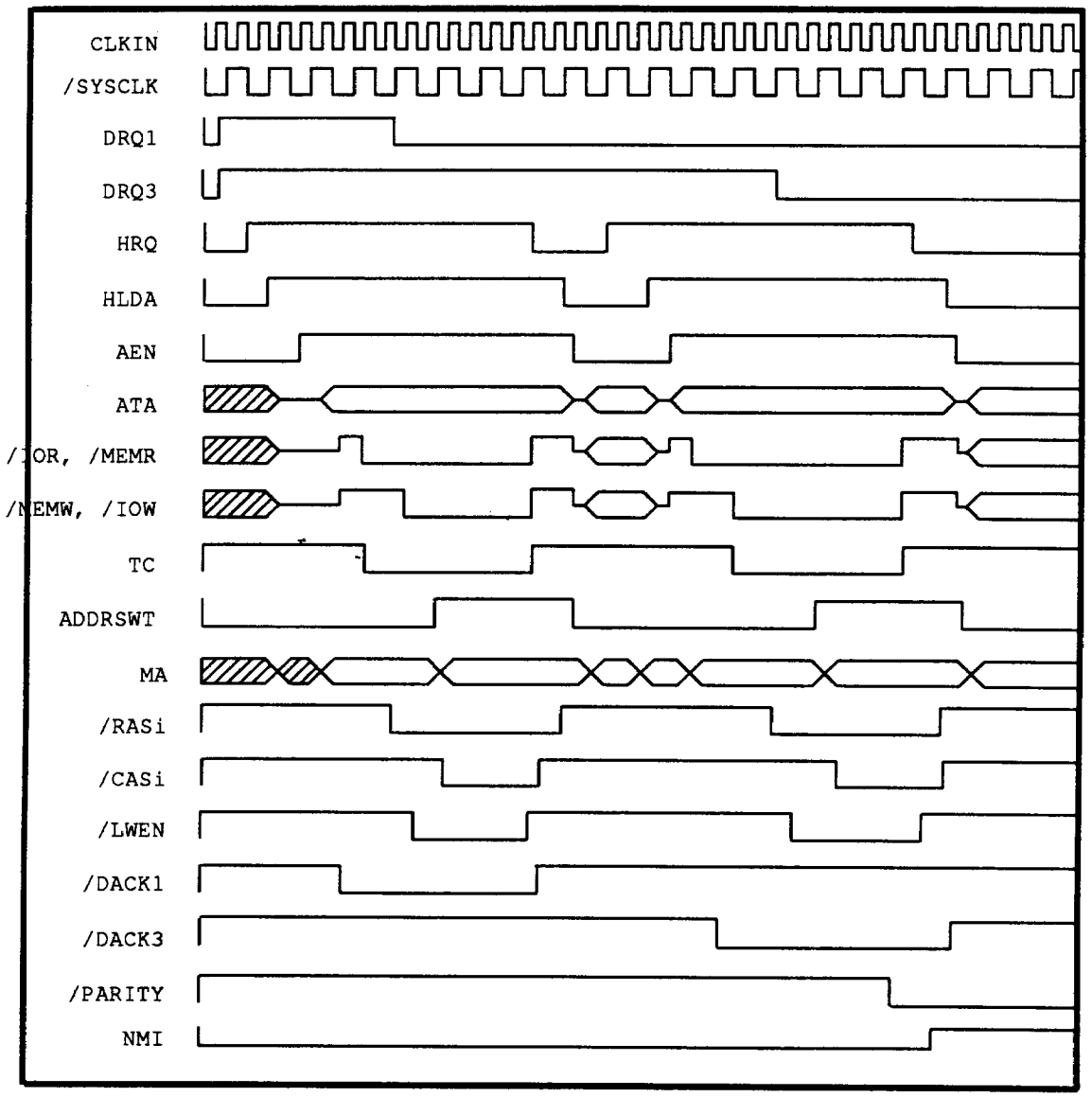
Two DMA channels (2 and 3) are requested concurrently—the channel with the higher priority receives service first.

/DACK is programmed for sense LOW.

The second DMA transfer (shown in Figure 10g) generates improper PARITY ; thus, activating NMI.

The test conditions are

DMA Clock	Division by 1
DMA Wait states	2
/DACK sense	LOW
Speed	Turbo ON



Timing diagrams

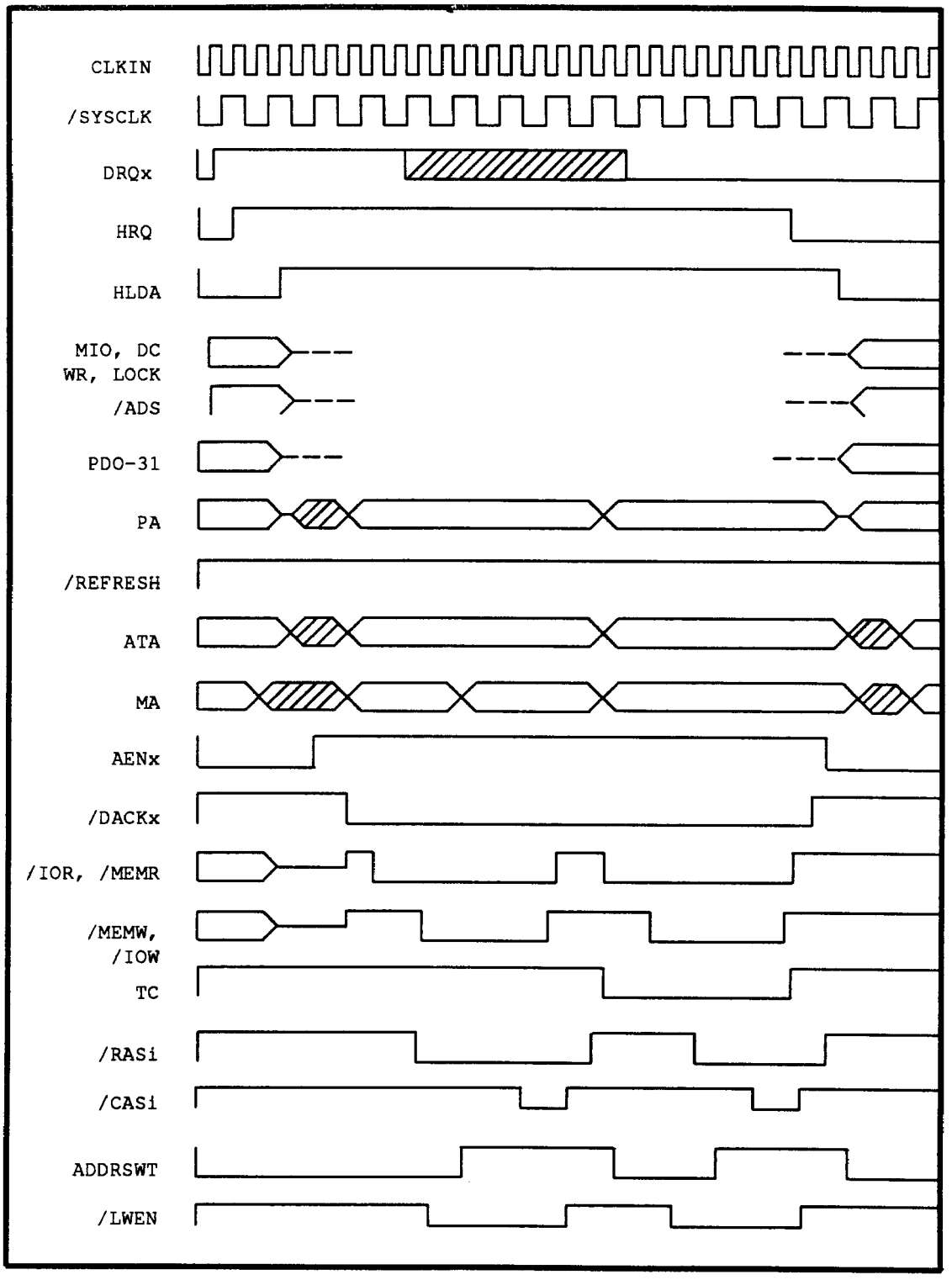
Figure 10k—DMA access timing

5 - 12 DMA timing in DEMAND mode

Figure 101 shows the timing relationships for direct memory access DMA operations in the *GCK131 Chip Set.* The particular cycle(s) shown in the Figure are those of the DMA controller in BLOCK DEMAND mode.

The test conditions are

DMA Clock	Divide by 2
DMA Wait states	2
/DACK sense	LOW
Speed	Turbo ON



Timing diagrams

Figure 10l—DMA access in DEMAND mode

5 - 13 REFRESH Timing

Figure 10m shows the timing relationships for a REFRESH cycle using the *GCK131 Chip Set.*

The cycle is a 'RAS only' type REFRESH which occurs once each 15 micro-seconds to meet the DRAM requirements.

The test conditions are as follows:

Speed	Turbo ON
REFRESH clock	Divide by 4
REFRESH Wait-states	0

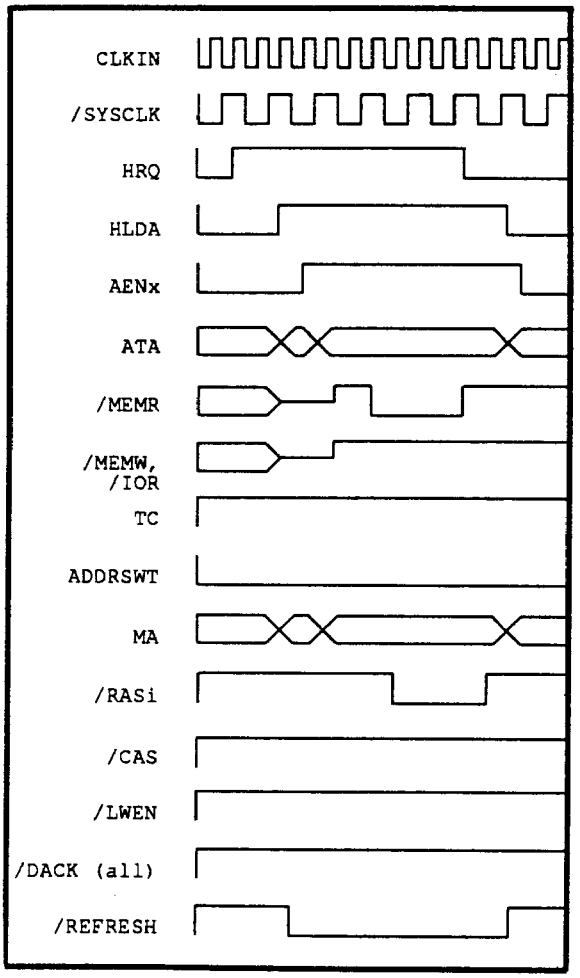


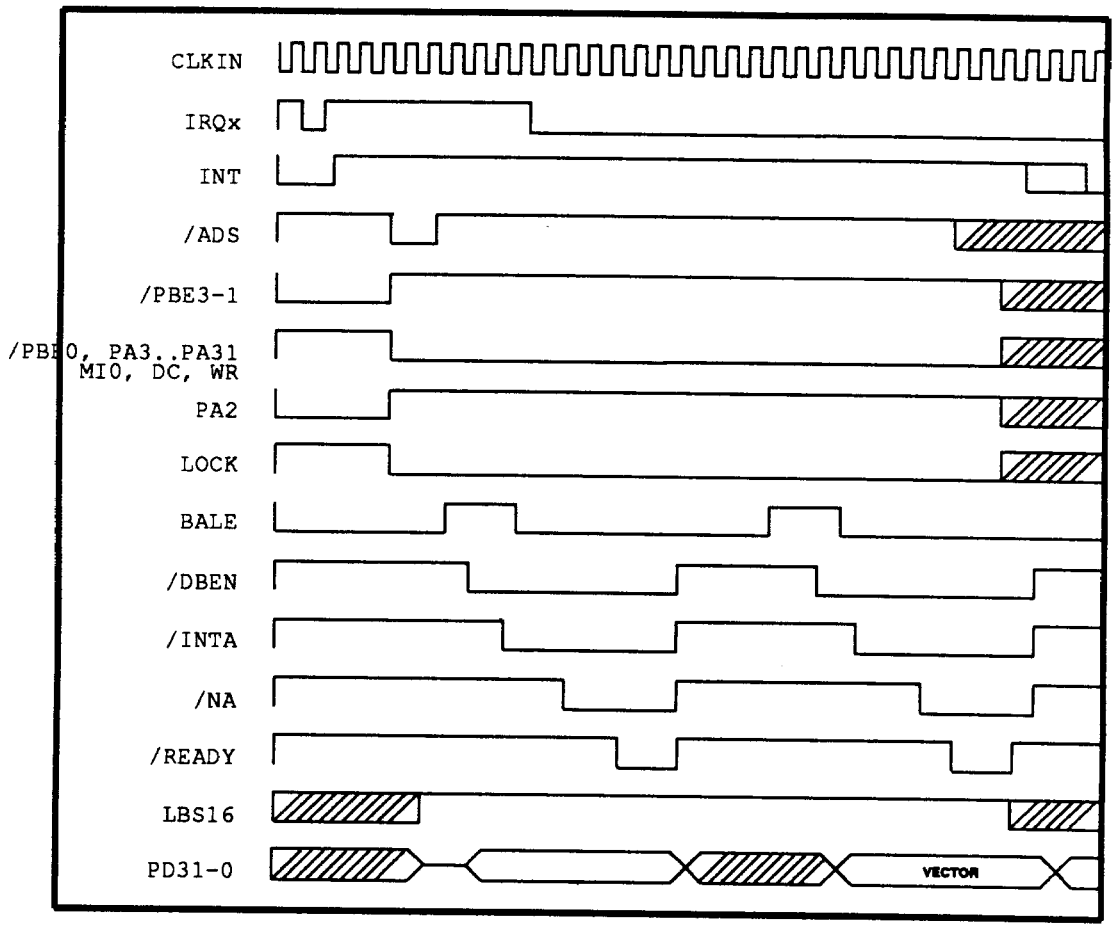
Figure 10m—REFRESH cycle timing

5 - 14 Interrupt Timing

Figure 10n shows the timing relationships within an interrupt cycle using the *GCK131 Chip Set.*

The INTERRUPT ACKNOWLEDGE cycle (shown in the Figure) has the following programmed values.

Command Delays	3 CLKINs
Command Active	7 CLKINs
RECOVERY Time	4 CLKINs



Timing diagrams

Figure 10n—Interrupt timing

5 - 15 NMI timing for on-board /MEMR cycle

Figure 10o shows the timing relationships for an on-board memory READ cycle (/MEMR that generates improper PARITY . As a consequence of the improper PARITY and its detection, the NMI signal is activated.

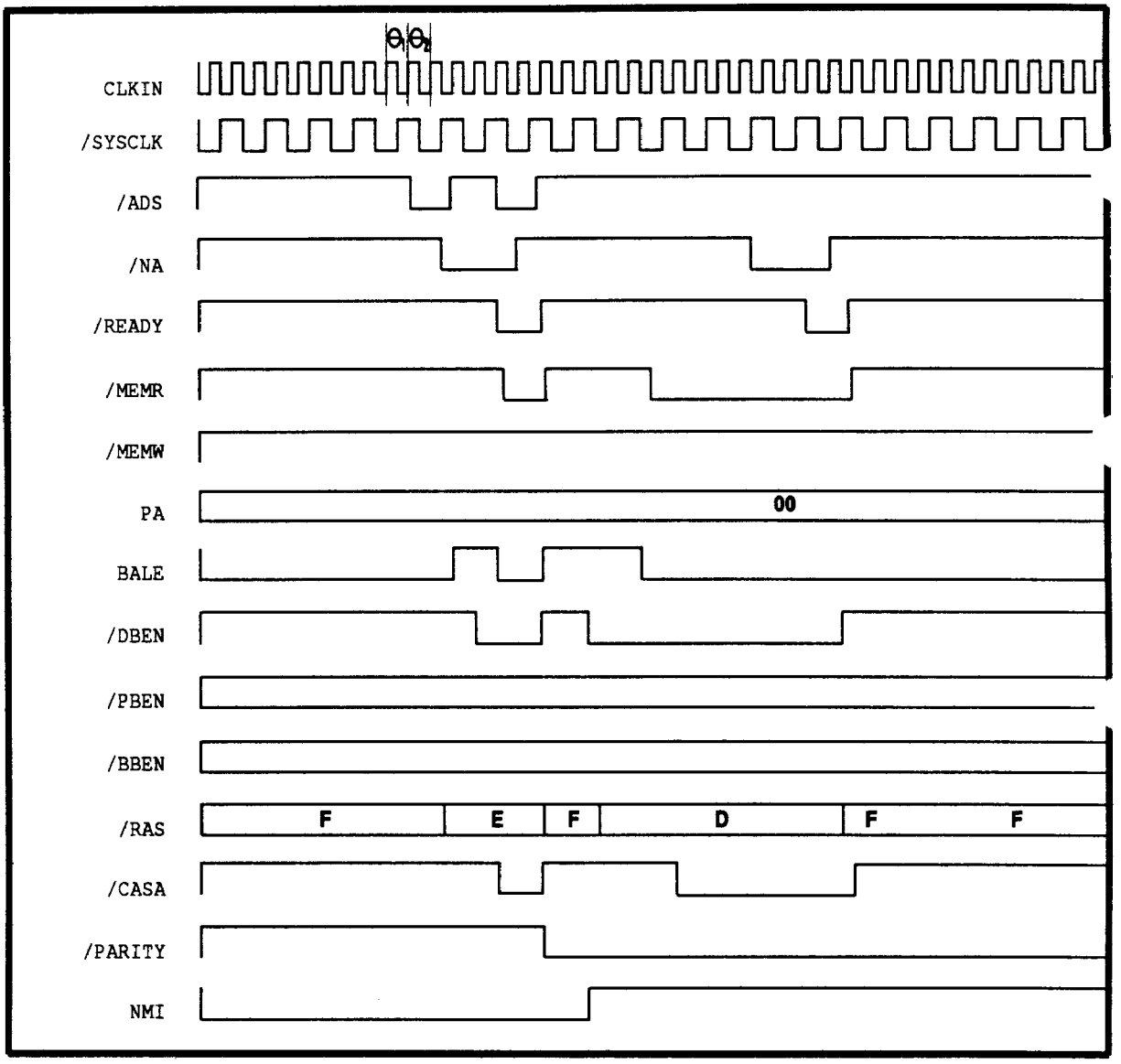


Figure 10o—NMI for on-board /MEMR cycle

5 - 16 NMI Timing for Off-board /MEMR cycle

Figure 10p shows the timing relationships for an off-board memory READ cycle (/MEMR that generates improper PARITY . The improper PARITY detection is signalled to the *GCK131 Chip Set* by /IOCHK indicating an error on the expansion bus.

The NMI is activated after the /IOCHK signal is detected within an /MEMR cycle from the expansion bus.

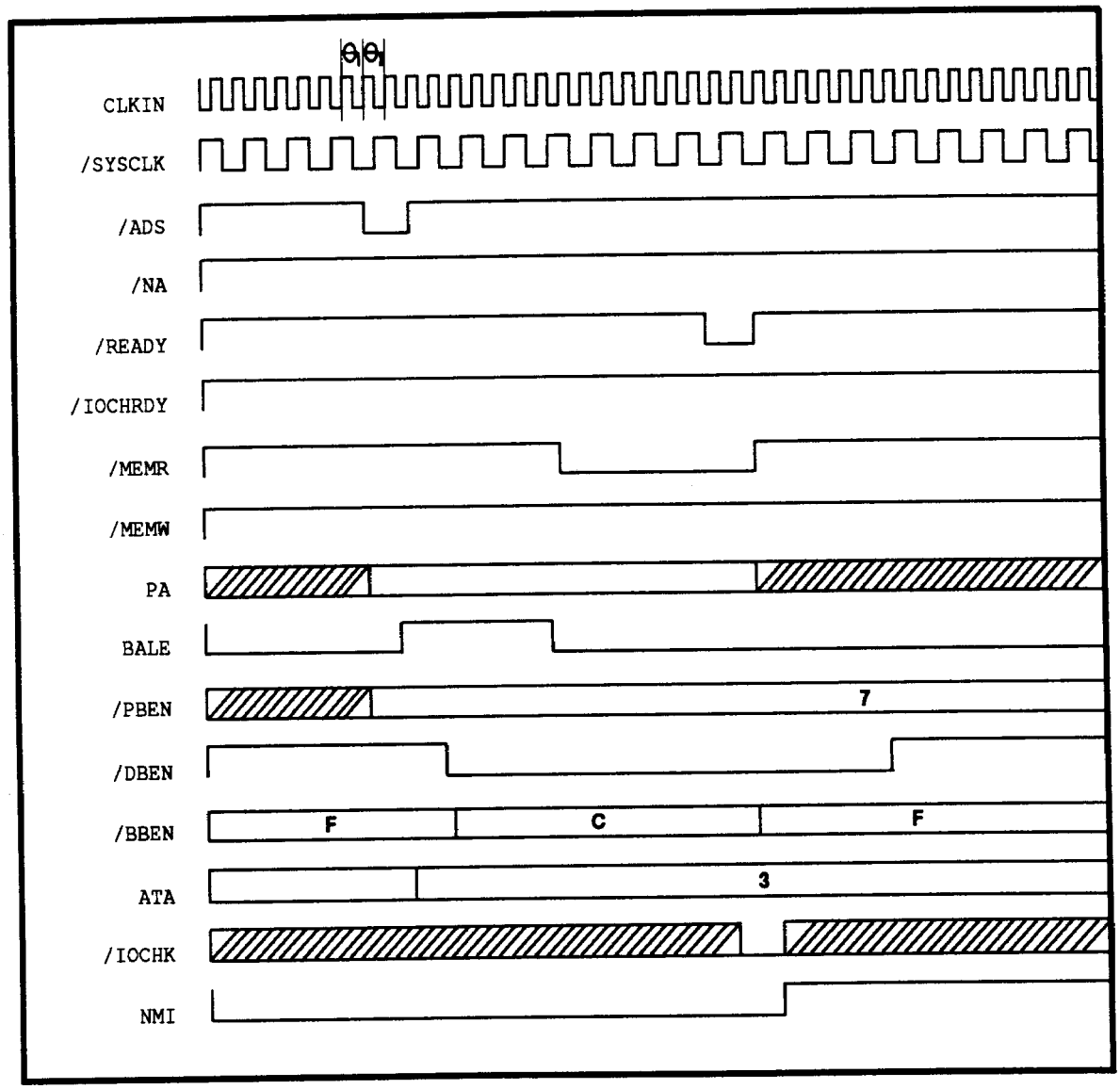


Figure 10p—NMI timing for off-board /MEMR cycle

Timing diagrams

5 - 17 EPROM READ timing

Figure 10q shows the timing relationships when accessing the EPROM using the *GCK131 Chip Set.*

The EPROM READ command is a 16-bit access and the test conditions are:

Command Delay	5 CLKINs
Command Active	14 CLKINs
Recovery time	8 CLKINs

Timing diagrams

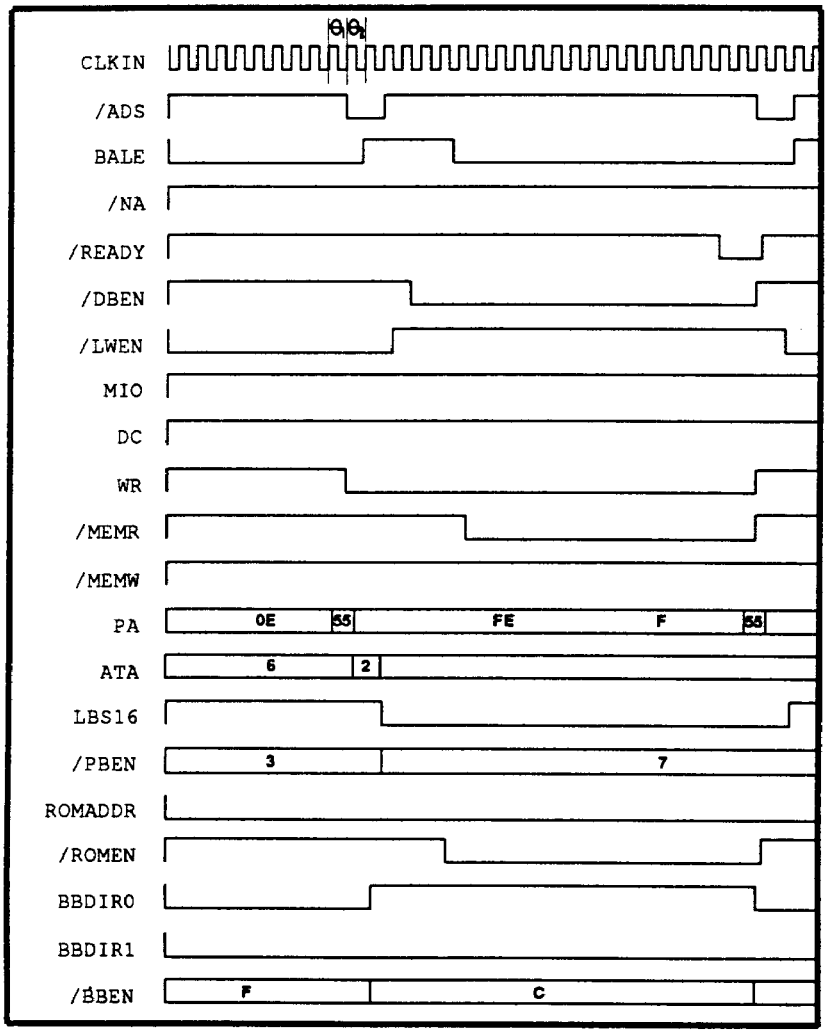


Figure 10q—EEPROM READ timing

5 - 18 Lower BIOS access

Figure 10r shows the timing relationships for an EPROM access to the Lower BIOS.

The waveform shown represents a non-pipelined, single-byte, even boundary READ from a 512K EPROM .

The test conditions are:

Shadow	Disabled
Command Delay	1.5 CLKINs
Command Active	4 CLKINs
Recovery time	2 CLKINs

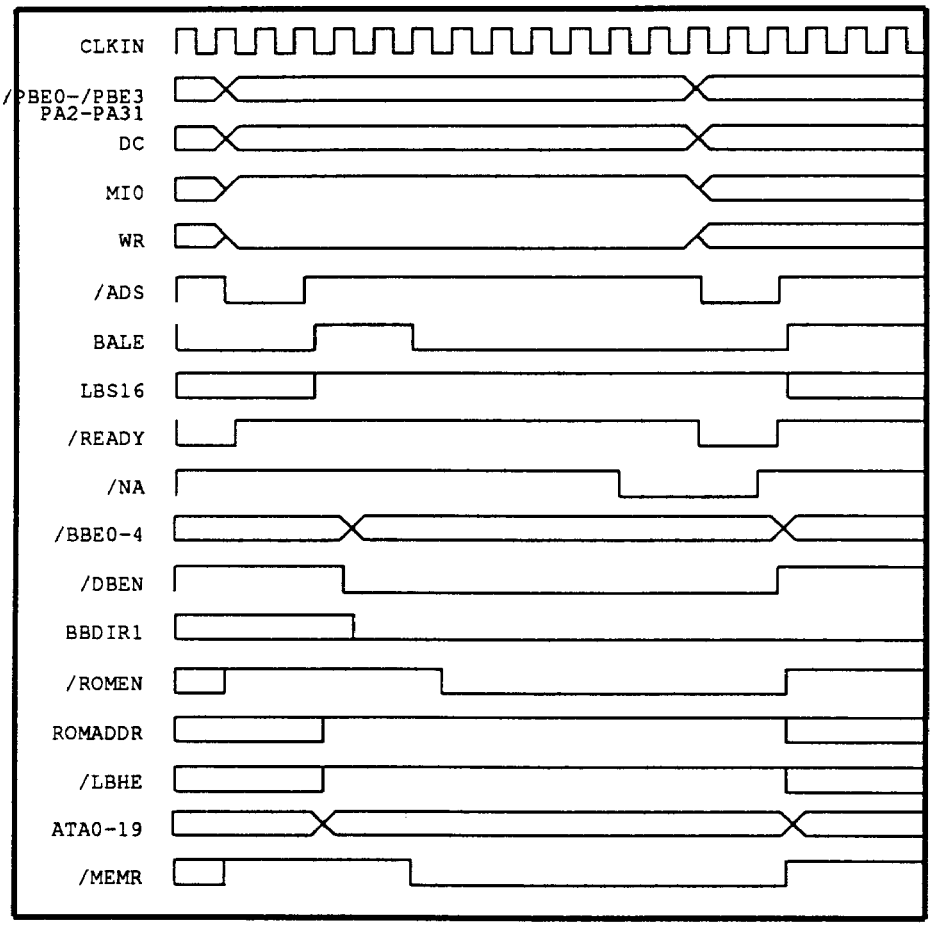


Figure 10r—Lower BIOS access timing

5 - 19 Lower BIOS WRITE

Figure 10s shows the timing relationships for a WRITE cycle to EPROM address space with 'shadow' enabled.

When the shadow is enabled (as shown) a WRITE to EPROM space is stored into the DRAM that is shadowing the BIOS at that location.

The test conditions are:

Shadow	Enabled
Command Delay	1.5 CLKINs
Command Active	6 CLKINs
Recovery time	0 CLKINs

Timing diagrams

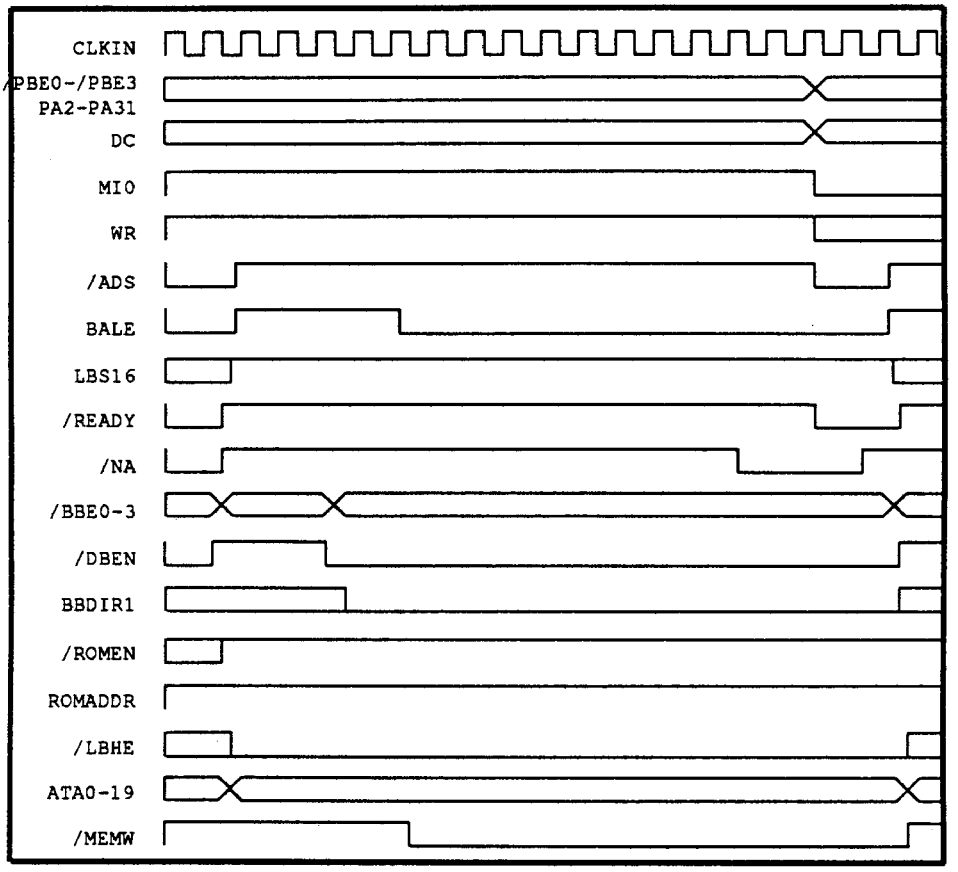


Figure10s—Lower BIOS, WRITE timing

5 - 20 Upper BIOS pipelined access

Figure 10t shows the timing relationships for an EPROM access to the Upper BIOS region.

The waveform shown represents a pipelined, three-byte READ with 256K EPROM s selected.

The test conditions are:

Command Delay	2.5 CLKINs
Command Active	3 CLKINs
Recovery time	0 CLKINs
EPROM type	256K

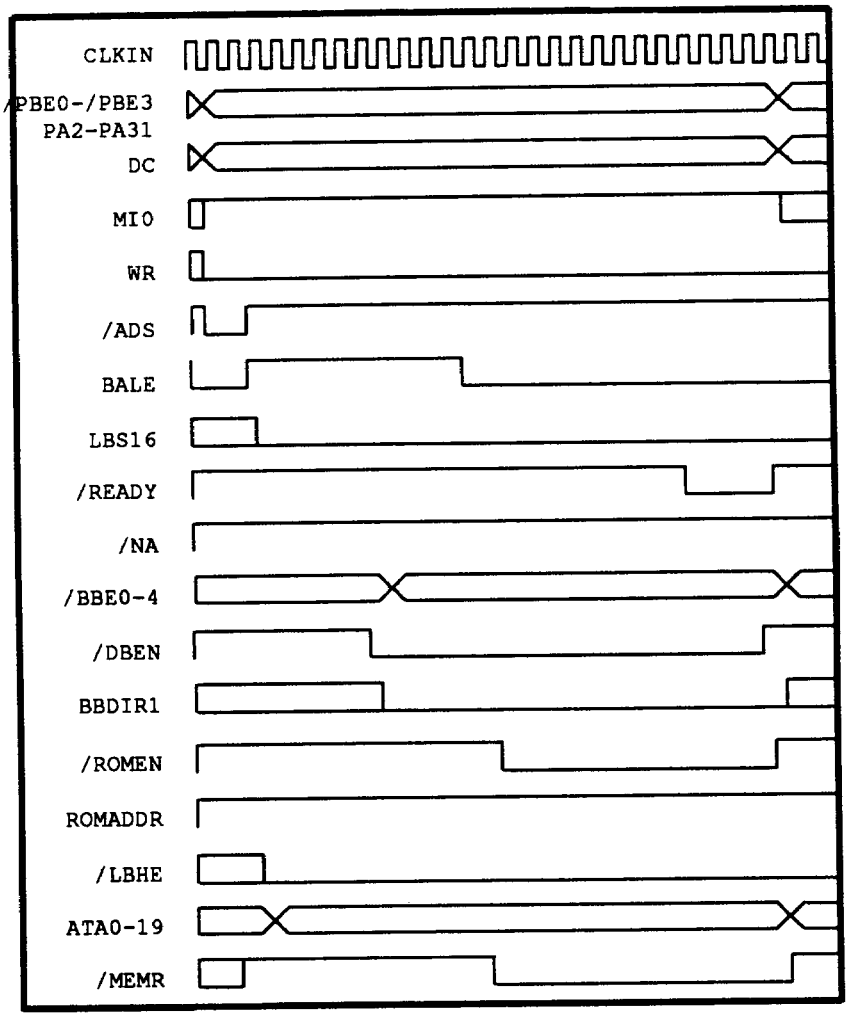


Figure 10t—Upper BIOS, pipelined access timing

Timing diagrams

5 - 21 Expansion bus timing for I/O operations

Figure 10u shows the timing relationships for I/O operations on the AT expansion bus using the *GCK131 Chip Set.*

An /IOR cycle is followed by an /IOW with IOCHRDY also shown for each command. The timings include BUSCLOCK—the clock on the AT expansion bus. BUSCLOCK, a division of CLKIN to the *GC131 Controller*, is programmable.

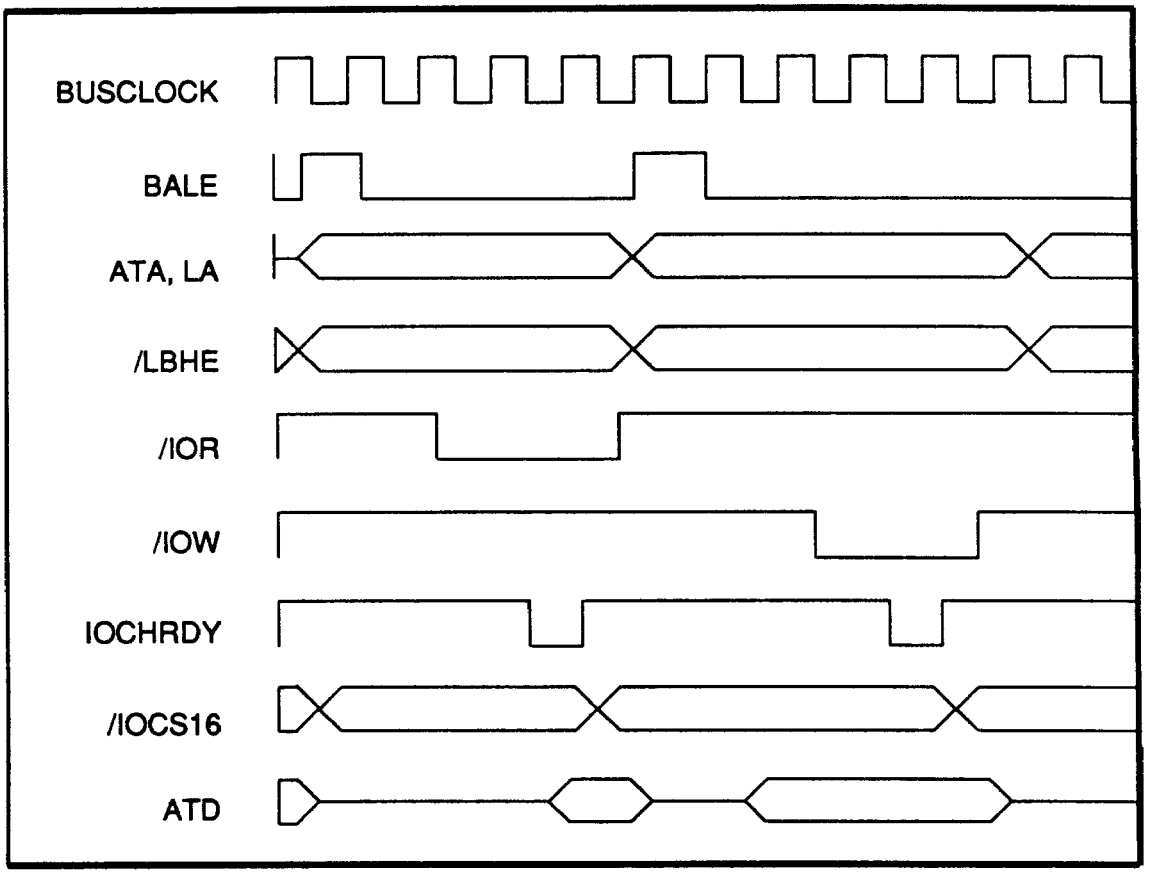
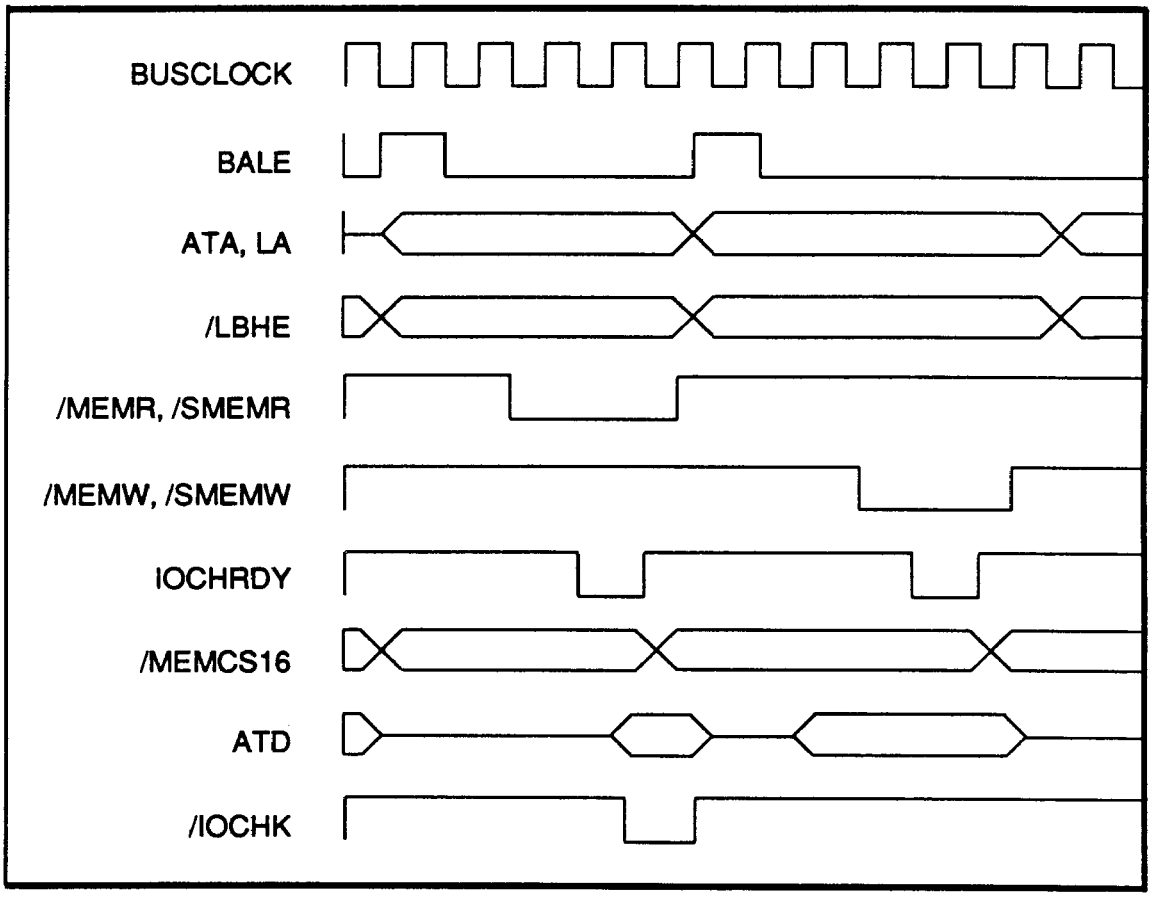


Figure 10u—Expansion bus timing for memory operations

5 - 22 Expansion bus timing for memory operations

Figure 10v shows the timing relationships for memory operations on the AT expansion bus using the *GCK131 Chip Set.*

A /MEMR cycle is followed by a /MEMW cycle. The timing relationships of /IOCHK, IOCHRDY and other signals are also shown for each cycle.



Timing diagrams

Figure 10v—Expansion bus timing for I/O operations

Timing diagrams

Section - 6 Propagation delays and Setup requirements

This Section of the *GCK131 Chip Set Data Sheet* describes the propagation delays and setup requirements associated with the principal signals of the *GCK131 Chip Set.*

These propagation delays, which reflect the characteristics of the design and CMOS techniques used in the fabrication of the chips, are typical of an average chipset (Rev. BBB) simulated under 'nominal' conditions. Nominal conditions are those applicable to 'average' silicon operating within an ambient temperature of 25°C, and with 5 V applied.

This Section describes timing relationships associated with operations within two of the three chips; namely,

- The *GC132 CPU/Memory Controller.*

  For clarity, the timing relationships of this controller are divided into:
  - Propagation delays directly associated with CLKIN, and
  - Setup timing that is not related to CLKIN.

- The *GC133 Bus Bridge Interface*

  The timing relationships in this chip are similarly divided:
  - Propagation delays directly associated with CLKIN, and
  - Setup timing that is not related to CLKIN.

6 - 1 Propagation delays of the GC132 CPU/Memory Controller

The *GCK131 Chip Set* is synchronous in its entirety and, for this reason, most delays and setup requirements have a direct relationship with CLKIN timing. Some signals transit from one value to another only on a specific CLK2 phase while others can switch on either phase.

In this Section, signals identified with an asterisk are those which transit from one value to another on a specific phase of the CLK2 cycle. All others can switch on either phase.

Propagation delays, of the GC132 Controller, associated with CLKIN. Time intervals are identified, here, by a name that is prefixed with the letter 'T'. The time values, in nanoseconds (ns), are listed below each diagram. For convenience, the following Table lists the names of the timing-intervals and the Figures in which they appear.

Propagation Delays and Setup times

Symbol	Description	Figures
TADDRHL	ADDRSEL fall	11e/f
TADDRLH	ADDRSEL rise	11e/f
TBALEHL	BALE fall	11e/f
TBALELH	BALE rise	11e/f
TBANK	BANKSEL 0, 1 and BALE	11g/h
TBBDIRHL	BBDIR fall	11c/d
TBBDIRLH	BBDIR rise	11c/d
TBBENHL	/BBEN fall	11c/d
TBBENLH	/BBEN rise	11c/d
TBUSYHL	/BUSY386/BUSY387	11i/j
TBUSYLH	/BUSY386/BUSY387	11i/j
TCASHL	/CAS fall	11a/b
TCASLH	/CAS rise	11a/b
TCOMMANDHL	COMMAND fall	11c/d
TCOMMANDLH	COMMAND rise	11c/d
TCONFDAT	Data valid and tristate delay	11k/l
TCONVHL	CONVERSION fall	11e/f
TCONVLH	CONVERSION rise	11e/f
TDBENHL	DBEN fall	11c/d
TDBENLH	DBEN rise	11c/d
TINTAHL	/INTA fall	11c/d
TINTALH	/INTA rise	11c/d
TIRQ13	Delay of IRQ13 from ERROR387	11k/l
TLBS16	LBS16 delay from BALE	11g/h
TLWEN	LWEN delay from BALE	11g/h
TMUX20	Delay of SPA20 from MUXPA20	11i/j
TNAHL	/NA fall	11a/b
TNALH	/NA rise	11a/b
TPA20	Delay of SPA20 from PA20	11i/j
TPARITYHL	/PARITY fall	11e/f
TPDAT	PARITYDATA valid	11e/f
TPEREQHL	PEREQ fall	11e/f
TPEREQLH	PEREQ rise	11e/f
TRASHL	/RAS fall	11a/b
TRASLH	/RAS rise	11a/b
TREADYHL	/READY fall	11a/b
TREADYLH	/READY rise	11a/b
TRESETHL	RESET fall	11a/b
TROMADDR	ROMADDR delay from BALE	
TROMENHL	/ROMEN fall	11g/h
TROMENLH	/ROMEN rise	11c/d
TSYSHL	/SYSCLK fall	11e/f
TSYSLH	/SYSCLK rise	11e/f

Figure 11a and 11b detail the propagation delays associated with the /CAS, EXRAS, /NA, /RAS /READY, CLREXPTION, and RESET387 signals of the *GC132 CPU/Memory Controller.*

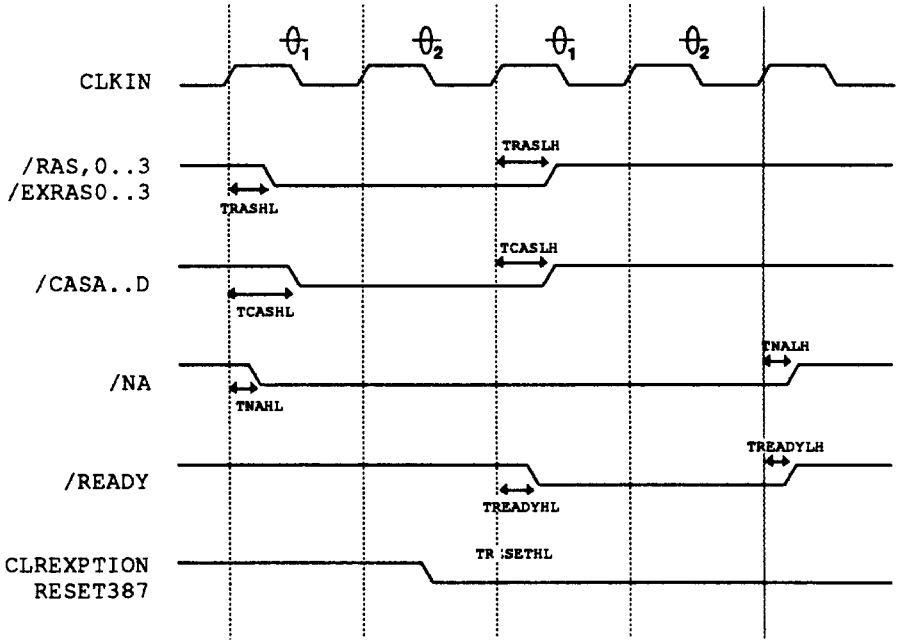


Figure 11a—Propagation delays /RAS,/CAS,/NA,/READY, RESET

Propagation Delays and Setup times

Symbol	Description	Value,Time, ns Min.	Typ.	Max.	Load, Capacitance pF
TCASHL	/CAS fall		12		40
TCASLH	/CAS rise		13		40
*TNAHL	/NA fall		10		20
*TNALH	/NA rise				
TRASHL	/RAS fall		9		20
TRASLH	/RAS rise		8.5		20
*TREADYHL	/READY fall		11		20
*TREADYLH	/READY rise		12		20
*TRESETHL	RESET fall		9		20

Figure 11b—Propagation delays /RAS,/CAS,/NA,/READY, RESET

Figure 11c and 11d diagram the propagation delays associated with the /BBEN, BBDIR,DBEN, /INTA, /IOR, /IOW, /MEMR, /MEMW and /ROMEN signals of the *GC132 CPU/Memory Controller.*

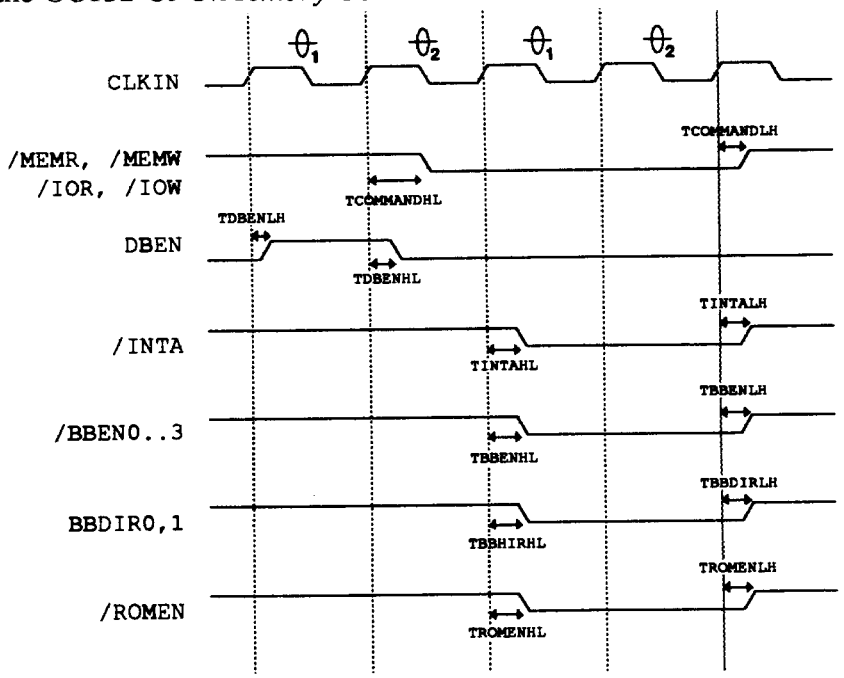


Figure 11c—Propagation delays /BBEN, BBDIR, DBEN, /INTA etc.

Propagation Delays and Setup times

Symbol	*Description*	*Value,Time, ns* Min.	Typ.	Max.	*Load, Capacitance pF*
TBBENHL	/BBEN fall		14		20
TBBENLH	/BBEN rise				
TBBDIRHL	BBDIR fall		12		20
TBBDIRLH	BBDIR rise		13		20
TCOMMANDHL	COMMAND fall		14		85
TCOMMANDLH	COMMAND rise		17		85
TDBENHL	DBEN fall		9		20
TDBENLH	DBEN rise				
TINTAHL	/INTA fall		11		20
TINTALH	/INTA rise				
TROMENHL	/ROMEN fall		25		20
TROMENLH	/ROMEN rise				

Figure 11d—Propagation delays /IOR, /IOW, MEMR, MEMW, /ROMEN

6 - 1- 3	ADDRSWT, BALE, CLK646, CONVA, /PARITY, PARITYDATO, PEREQ386, SAB646,/SYSCLK	GC132

Figure 11e and 11f diagram the propagation delays associated with the ADDRSWT, BALE, CLK646, CONVA, /PARITY, PARITYDATO, PEREQ386, SAB646, and /SYSCLK signals of the *GC132 CPU/Memory Controller.*

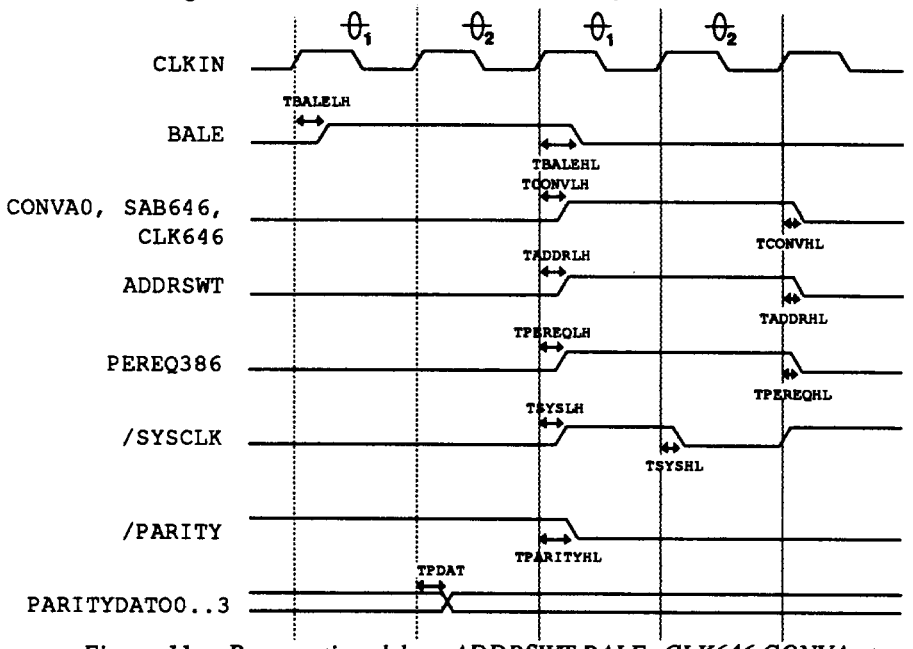


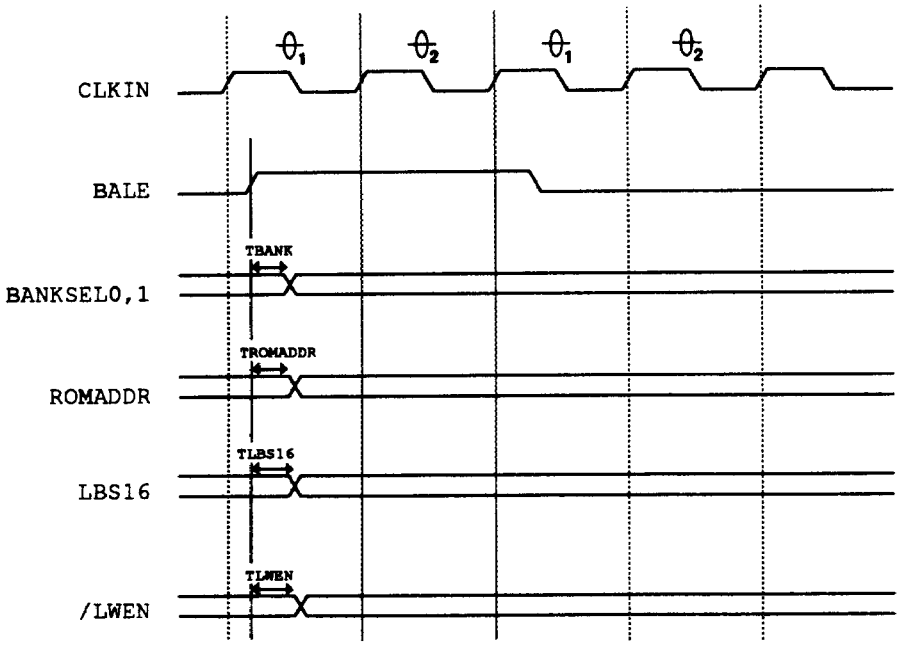
Figure 11e—Propagation delays ADDRSWT,BALE, CLK646,CONVA,etc

Propagation Delays and Setup times

Symbol	*Description*	*Value,Time, ns* Min.	Typ.	Max.	*Load, Capacitance pF*
TBALEHL	BALE fall		10		20
TBALELH	BALE rise		10		20
TADDRHL	ADDRSEL fall				
TADDRLH	ADDRSEL rise		10		20
*TCONVHL	CONVERSION fall		10		20
*TCONVLH	CONVERSION rise		10		20
TPARITYHL	/PARITY fall		14		20
TPDAT	PARITYDATA valid		15		60
TPEREQHL	PEREQ fall				
TPEREQLH	PEREQ rise		9		20
*TSYSHL	/SYSCLK fall		8		85
*TSYSLH	/SYSCLK rise		9		85

Figure 11f—Propagation delays /PARITY, PARITY, PEREQ,SA,etc.

Figure 11g and 11h diagram the propagation delays associated with the BALE, BANKSEL, ROMADDR, LBS16, and /LWEN signals of the *GC132 CPU/Memory Controller.*



Propagation Delays and Setup times

Figure 11g—Propagation delays BALE, BANKSEL, ROMADDR, /LWEN

Symbol	Description	Value,Time, ns Min.	Typ.	Max.	Load, Capacitance pF
TBANK	BANKSEL 0, 1 delay from BALE		4		20
TLBS16	LBS16 delay from BALE		5		20
TLWEN	/LWEN delay from BALE				
TROMADDR	ROMADDR delay from BALE		9		20

Figure 11h—Propagation delays BALE, BANKSEL, ROMADDR, LBS16

Figure 11i and 11j diagram the propagation delays associated with the /BUSY386, /BUSY387, MUXPA20, PA20, and SPA20 signals of the *GC132 CPU/Memory Controller.*

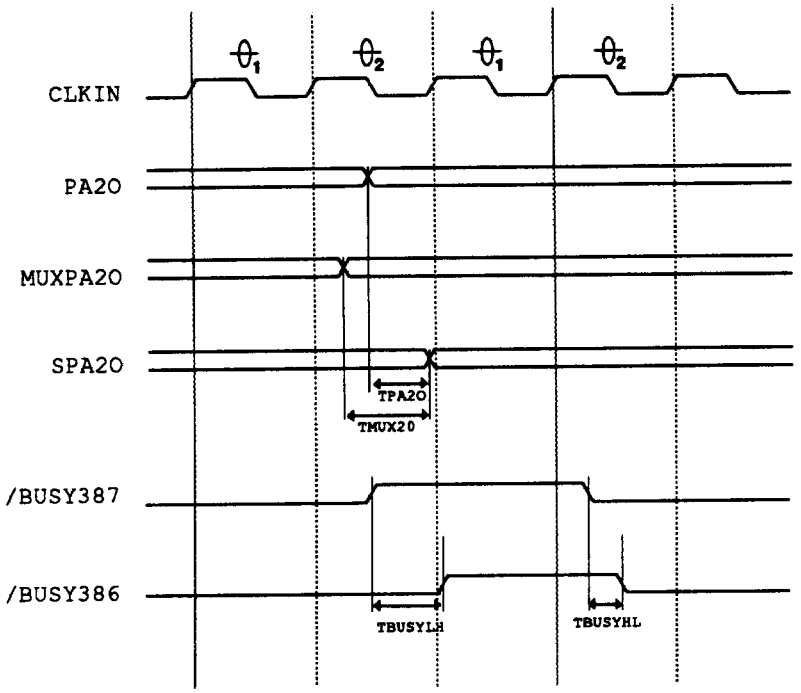
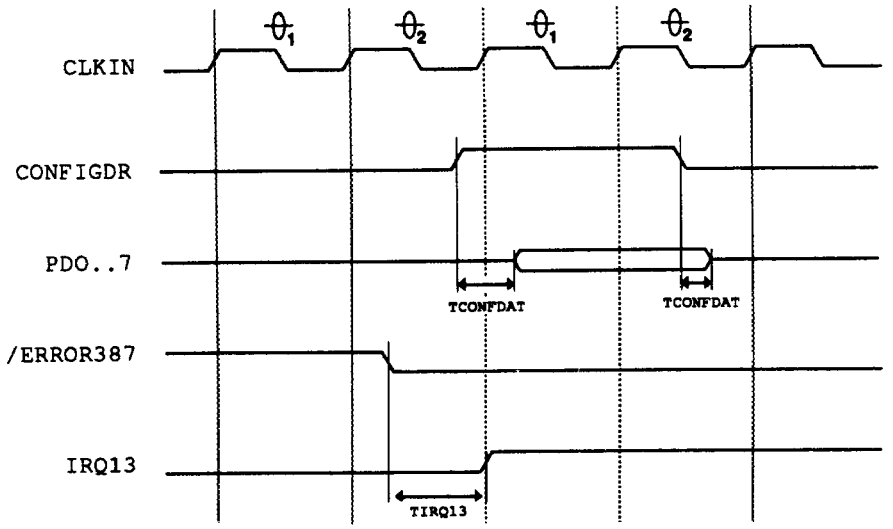


Figure 11i—Propagation delays /BUSY386,/BUSY387, MUXPA20 et.

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*	*Load, Capacitance pF*
TBUSYHL	Delay of /BUSY386 from /BUSY387				
TBUSYLH	Delay of /BUSY386 from /BUSY387		6.5		20
TMUX20	Delay of SPA20 from MUXPA 20		4.5		20
TPA20	Delay of SPA20 from PA203.5				20

Figure 11j—Propagation delays /BUSY386,/BUSY387,MUXPA,PA,etc

Figure 11k and 111 diagram the propagation delays associated with the CONFIGDR, /ERROR387, IRQ, and PD signals of the *GC132 CPU/Memory Controller.*



Propagation Delays and Setup times

Figure 11k—Propagation delays /CONFIGDR,/ERROR387,IRQ,LD

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*	*Load, Capacitance pF*
TCONFDAT	Data valid and tristate delay		11		85
TIRQ 13	Delay of IRQ 13 from /ERROR 387		7.5		20

Figure 111—Propagation delays /CONFIGDR,/ERROR387,IRQ,LD

6 - 2 Signals whose delays depend on other than CLKIN sources

The setup requirements, of the *GC132 Controller* are shown in this Section.

Time intervals are identified by a name that is prefixed with the letter 'T'. The time values, in nanoseconds (ns), are listed below each diagram. For convenience, the following Table lists the names of the timing-intervals and the Figures in which they appear.

Symbol	Description..... Figures
TADS	/ADS active setup time at start of cycle..... 11m/n
TDCON	LD setup time for configuration data. 11o/p
TDPAR	LA setup time for parity at start of cycle..... 11m/n
TPA	PA setup time at start of cycle..... 11m/n
TPBEN	PBEN setup time at start of cycle..... 11m/n
TPGVIOL	PGVIOL setup time at end of cycle. 11m/n
TSTATUS	MIO, DC, WR setup time at start of cycle..... 11m/n

6 - 2- 1	/ADS, DC, LD, MIO, PA, /PBEN, PGVIOL, WR	GC132

Figure 11m and 11n diagram the setup time requirements associated with the /ADS, DC, LD, MIO, PA, /PBEN, PGVIOL, and WR signals of the *GC132 CPU/Memory Controller.*

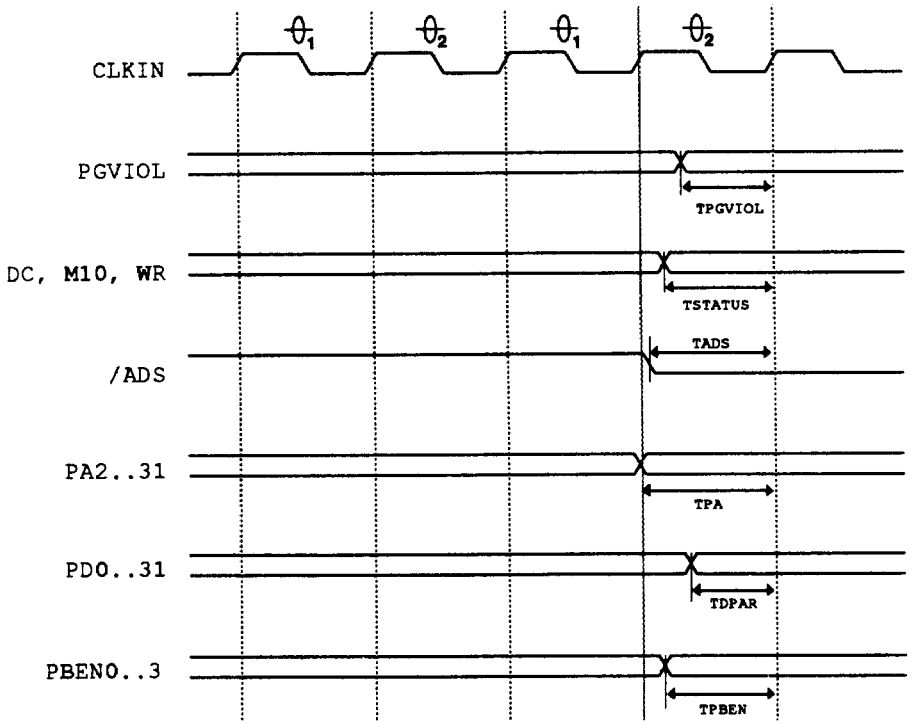


Figure 11m—Setup requirements: /ADS, DC, LD, MIO, PA, etc.

Propagation Delays and Setup times

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*
TADS	/ADS active setup time at start of cycle.		15	
TDPAR	LA setup time for parity at start of cycle.		4	
TPA	PA setup time at start of cycle.		10	
TPBEN	/PBEN setup time at start of cycle.		3	
TPGVIOL	PGVIOL setup time at end of cycle.		4.5	
TSTATUS	MIO, DC, WR setup time at start of cycle		10	

Figure 11n—Setup requirements:/ADS,D_C,PBEN,PGVIOL,W_R etc.

Figure 11o and 11p diagram the setup time requirements associated with the CONFIGAS, CONFIGDW, and LD signals of the *GC132 CPU/Memory Controller.*

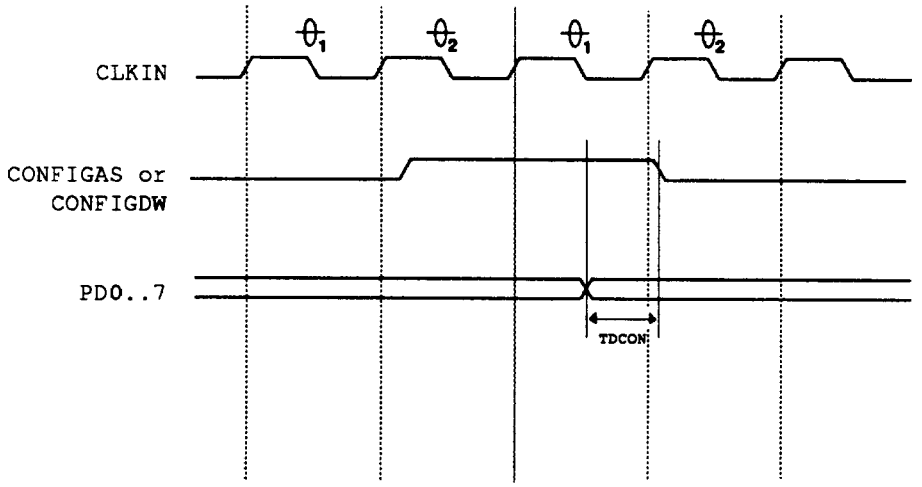


Figure 11o—Setup time requirements: CONFIGAS, CONFIGDW, LD

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*
TDCON	PD setup time for configuration data.		3	

Figure 11p—Propagation delays CONFIGAS, CONFIGDW, LD

Propagation Delays and Setup times

6 - 3 GC133 Bus Bridge Interface, Propagation delays

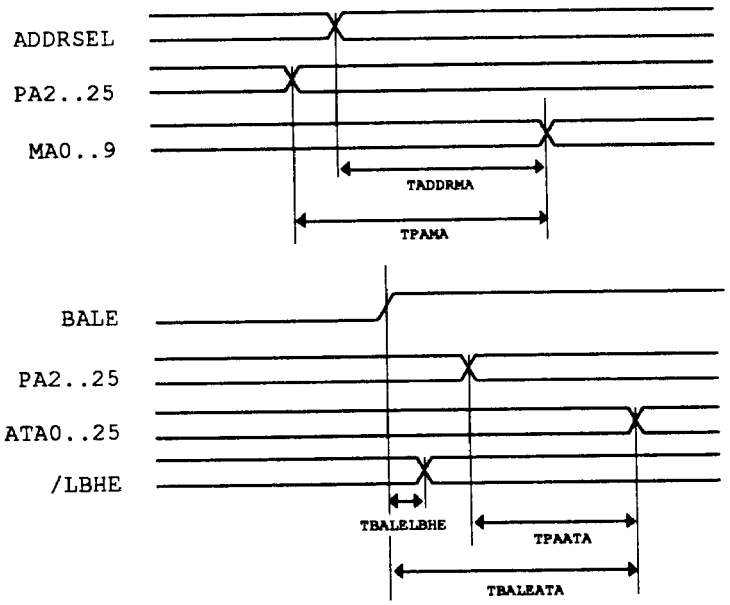
The *GC133 Bus Bridge Interface* provides a bridge between the 32-bit processor data activities and the 16-bit AT-compatible data paths. The *GC133 Interface* latches addresses and provides (to the DRAM) the appropriate MA addresses. The commands that initiate these functions originate with the *GC132 CPU/Memory Controller*: an association in which the *GC133 Controller* can be imagined as a 'muscle-bound' slave of the *GC132 Controller*.

Timing is measured, typically as that period starting from the *GC132 Controller* command to the activity created in or by the *GC133 Controller*. In some cases, different inputs can effect a change to the same output; for example, the MA address lines change as a result of ADDRSEL or PA changes.

Symbol	Description..... Figures	Symbol	Description ..... Figures
TADDRMA	Delay from ADDRSEL to MA line change..... 12a/b	TPAATA	Delay from PA to ATA 12a/b
TBALEATA	Delay from BALE to ATA 12a/b	TPAMA	Delay from PA to MA 12a/b
TBALELBHE	Delay from BALE to / LBHE..... 12a/b	TPAPGV	PGVIOL active delay 12i/j
TATDPD	Delay from ATD bus to PD bus READ 12e/f	TPBENATA	Delay from PBEN to ATA 0,1, or /LBHE 12c/d
TATDZ	Delay from ATD to HIGH-Z 12e/f	TPDATD	Delay from PD bus to ATD bus (WRITE) 12e/f
TATHL	Delay from ATD higher to lower byte (conversion).... 12g/h	TPDHATL	Data bridge from high PA to low ATD ... 12i/j
TATLH	Delay from ATD lower to higher byte (conversion).... 12g/h	TPDZ	Delay from PD active to HIGH-Z 12e/f
TBRIDGZ	Data bridge active to HIGH-Z time 12g/h	TZATD	Delay from HIGH-Z to ATD active..... 12e/f
TCONFDZ	Configuration data active to HIGH -Z delay 12i/j	TZBRDG	Data bridge HIGH-Z to active time..... 12g/h
TCONVA0	Delay from CONVA 0 to ATA 12c/d	TZCONFD	Configuration data HIGH-Z to active delay 12i/j
		TZPD	Delay from HIGH-Z to PD active..... 12e/f

Propagation Delays and Setup times

Figure 12a and 12b diagram the propagation delays associated with the ADDRSEL, BALE, /LBHE, MA, PA, and MA signals of the *GC133 Bus Bridge Interface*.



Propagation Delays and Setup times

Figure 12a—Propagation delays ADDRSEL, BALE, /LBHE, MA, PA

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*	*Load, Capacitance pF*
TADDRMA	Delay from ADDRSEL to MA line change		6.6		20
TBALEATA	Delay from BALE to ATA		12.5		20
TBALELBHE	Delay from BALE to /LBHE		9.5		20
TPAATA	Delay from PA to ATA with BALE=1		10.5		20
TPAMA	Delay from PA to MA		10.5		20

Figure 12b—Propagation delays ADDRSEL, BALE, LBHE, MA, PA

Figure 12c and 12d diagram the propagation delays associated with the ATA, CONVA, /LBHE, and /PBEN signals of the *GC133 Bus Bridge Interface.*

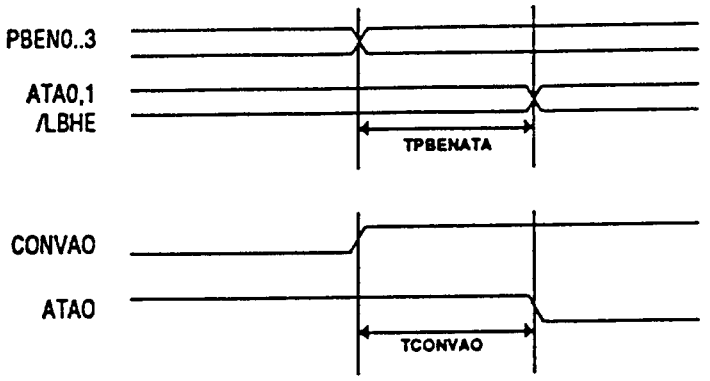


Figure 12c—Propagation delays ATA, CONVA, /LBHE, /PBEN

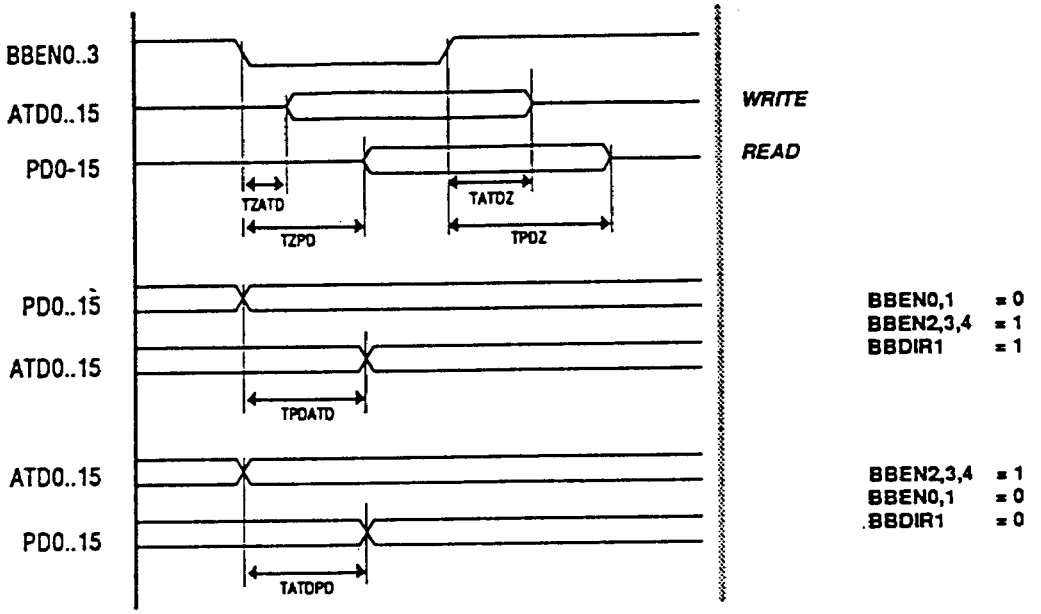
Propagation Delays and Setup times

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*	*Load, Capacitance pF*
TCONVA0	Delay from CONVA 0 to ATA 0 = 1		6.5		20
TPBENATA	Delay from /PBEN to ATA 0,1, or /LBHE		9		20

Figure 12d—Propagation delays ATA, CONVA, /LBHE, /PBEN

6 - 3- 3 ATD,/PBEN,PD - GC133

Figure 12e and 12f diagram the propagation delays associated with the ATD, /PBEN, and PD signals of the *GC133 Bus Bridge Interface*.



Propagation Delays and Setup times

Figure 12e—Propagation delays ATD, /PBEN, and PD

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*	*Load, Capacitance pF*
TATDPD	Delay from ATD bus to PD bus READ		11		20
TATDZ	Delay from ATD to HIGH-Z		14		20
TPDATD	Delay from PD bus to ATD bus (WRITE)		12		20
TPDZ	Delay from PD active to HIGH-Z		12		20
TZATD	Delay from HIGH-Z to ATD active		14		20
TZPD	Delay from HIGH-Z to PD active		13		20

Figure 12f—Propagation delays ATD, /PBEN, and PD

Figure 12g and 12h diagram the propagation delays associated with the ATD and BBEN signals of the *GC133 Bus Bridge Interface.*

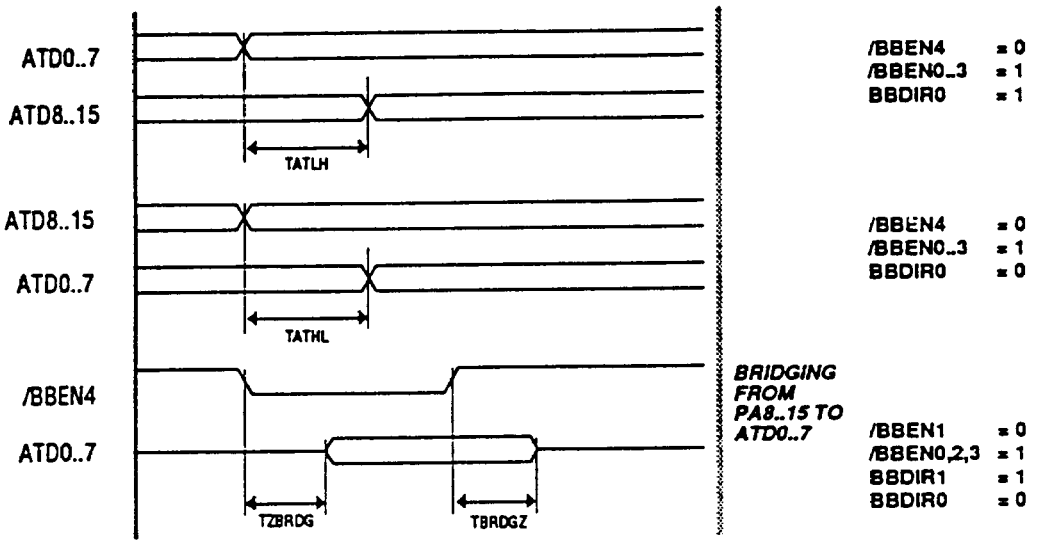


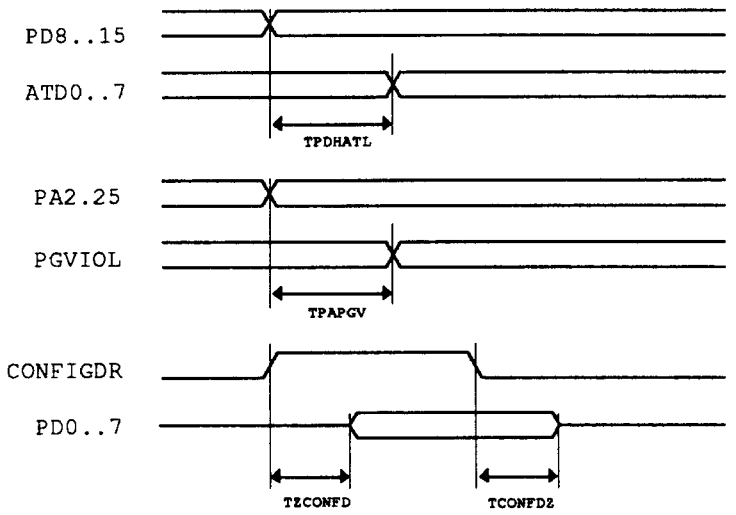
Figure 12g—Propagation delays ATD and BBEN

Propagation Delays and Setup times

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*	*Load, Capacitance pF*
TATHL	Delay from ATD higher to lower byte (conversion)		11		20
TATLH	Delay from ATD lower to higher byte (conversion)		11		20
TZBRDG	Data bridge HIGH-Z to active time		15		20
TBRIDGZ	Data bridge active to HIGH-Z time		14.5		20

Figure 12h—Propagation delays ATD and BBEN

Figure 12i and 12j diagram the propagation delays associated with the ATD, CONFIGDR, PA, PD and PGVIOL signals of the *GC133 Bus Bridge Interface.*



Propagation Delays and Setup times

Figure 12i—Propagation delays ATD,CONFIGDR,PA,PD, and PGVIOL

Symbol	*Description*	*Value,Time, ns* Min.	Typ.	Max.	*Load, Capacitance pF*
TZCONFD	Configuration data HIGH-Z to active delay		14.5		20
TCONFDZ	Configuration data active toHIGH -Z delay		11		20
TPAPGV	PGVIOL active delay		7.5		20
TPDHATL	Data bridge from high PA to low ATD		12		20

Figure 12j—Propagation delays ATD,CONFIGDR,PA,PD and PGVIOL

6 - 3- 6 ATD,BALE,CONFIGAS,CONFIGDW,PA,/PBEN,/RAS GC133

Figure 12k and 12l diagram the propagation delays associated with the ATD, BALE CONFIGAS, CONFIGDW, PA, /PBEN, and /RAS signals of the *GC133 Bus Bridge Interface.*

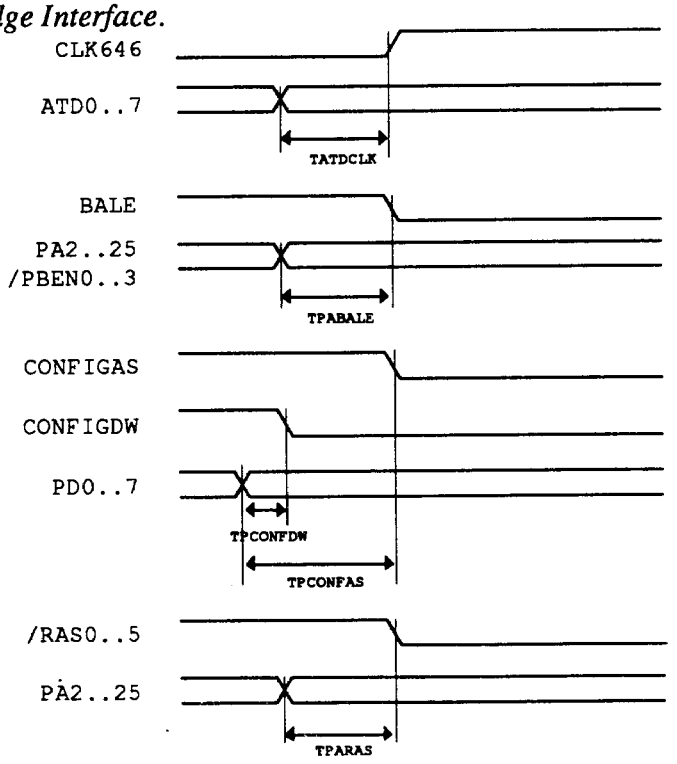


Figure 12k—Propagation delays BALE,ATD,CONFIGAS,CONFIGDW,etc

Propagation Delays and Setup times

Symbol	*Description*	*Value,Time, ns* *Min.*	*Typ.*	*Max.*	*Load, Capacitance pF*
TATDCLK	Setup time of ATD with reference to CLK646		2		
TPABALE	Setup time of PAs with reference to BALE		2		
TPCONFDW	Setup time of PDs with reference to CONFIGDW		-1		
TPCONFAS	Setup time of PDs with reference to CONFIGAS		0		
TPARAS	Setup time of PAs with reference to /RAS		7		

Figure 12l—Propagation delays ATD,BALE,CONFIGAS,PBEN,/RAS

Propagation Delays and Setup times

Section - 7 Specifications

This Section of the *GCK131 Chip Set Data Sheet* outlines, in several Figures, the physical and electrical specifications of the chip set.

General Specifications

The *GCK131 Chip Set* consists of three highly integrated microchips; named, *GC131 Peripheral Controller, GC132 CPU/Memory Controller,* and *GC133 Bus Bridge Interface.*

Designed in 0.9 micron HCMOS technology and fabricated for use as surface-mount components within either a conventional desktop, or a laptop design, the *GCK131 Chip Set* supports an 80386-based personal computer system in AT-compatible mode.

The chips, each in a 160-pin gull-wing plastic package, are designed for use as a set. Two versions are available:

Part Number

GCK131-20 ..... 20 MHz

GCK131-25 ..... 25 MHz

Power requirements

See *Section 7-2 Electrical characteristics*

Space requirements

See *Section 7-1 Physical characteristics*

Environmental characteristics

Temperature

Operating ..... 0° to 70°C

Storage ..... -40° to +125°C

Humidity

Operating ..... *8% to 80% (non-condensing)*

Storage ..... *5% to 95% (non-condensing*

Altitude

Operating ..... *0 to 3000 m*

Storage ..... *0 to 5000 m*

Physical and Electrical characteristics

7 - 1 Physical characteristics -

Size

Length ..... 32 mm

Width ..... 32 mm

Height ..... 3.55 mm

(For further information see Figure 14a)

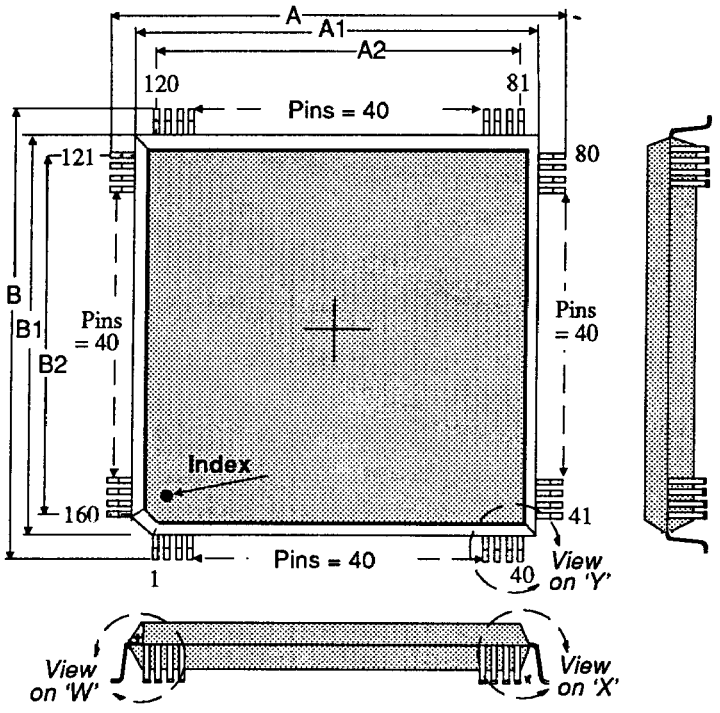
Weight

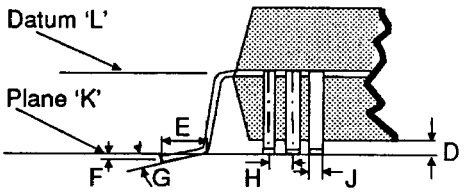
..... *(To be determined)*

Regulatory compliance

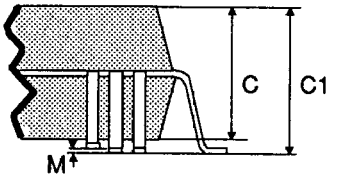
FCC Class B ..... *(To be determined)*

#37,779

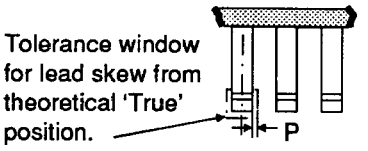




Detail 'W'



Detail 'X'



Detail 'Y'

Dimensions

Millimetres (Nominal)			*Inches*		
Symbol	Minimum	Maximum	*Symbol*	*Minimum*	*Maximum*
A	31.60	32.40	A	1.244	1.276
A1	27.90	28.10	A1	1.098	1.106
A2	25.35 Ref.		A2	0.998 Ref.	
B	31.60	32.40	B	1.244	1.276
B1	27.90	28.10	B1	1.098	1.106
B2	25.35 Ref.		B2	0.998 Ref.	
C	3.94 Max.		C	0.155 Max.	
C1	3.55 Ref.		C1	0.140 Ref.	
D	0.00	0.30	D	0.000	0.012
E	0.60	1.00	E	0.024	0.039
F	0.10	0.25	F	0.004	0.010
G	0°	10°	G	0°	10°
H	0.65 ± 0.15		H	0.026 ± 0.006	
J	0.25	0.35	J	0.010	0.014
M	0.10 Max.		M	0.004 Max.	
P	0.05 Max.		P	0.002 Max.	

Total Number of pins = 160

Notes:

Unless otherwise specified—

1. Nominal dimensions in mm. Inch measurements are rounded to the nearest 0.001".
2. Flatness—all leads to seat within 0.10 mm (0.004") of Plane 'K' (Detail W).
3. Lead pitch determined at Datum 'L' (Detail W).

Figure 14a—160-pin plastic gull-wing package, Dimensions

7 - 2 Electrical Characteristics

DC Characteristics

The DC characteristics (as shown in Figure 14b) are specified with reference to VDD at 5 V± 5%, ambient temperature 0°C to 70°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Voltage input LOW				0.8	V
V_{IH}	Voltage input HIGH		2.0			V
VT+	Schmitt-Trigger, positive-going threshold			3.0	4.0	V
VT-	Schmitt-Trigger, negative-going threshold		1.0	1.5		V
⊓	Hysteresis, Schmitt Trigger	V_{IL} to V_{IH} V_{IH} to V_{IL}	1.0	1.5		V
V_{OH}	Voltage output HIGH		2.4	4.5		V
	GC131 Controller: ATA0-19, ATD0-7, BUSCLOCK, /CS8042, /DACK0-3, /DACK5-7, LA17-31, /LBHE, OSC, RESET, RTCDS, RTCRW, /SMEMR, /SMEMW, TC	I_{OH} = -8 mA				
	GC132 Controller: ADDRSWT, BALE, BANKSEL0,1, /CASA-D, /EXRAS0,1, /IOR, /IOW, /MEMR, /MEMW, PARDATO0-3, PD0-7, /RAS0-3	I_{OH} = -8 mA				
	GC133 Interface: ATA0-19, ATD0-15, LBHE, MA0-9, PGVIOL	I_{OH} = -8 mA				
	All others (*GC131, GC132,* and *GC133)*	I_{OH} =-4 mA				

More . . .>

Figure 14b—DC Characteristics

Physical and Electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OL}	Voltage output LOW			0.4	0.8	V
	GC131 Controller: ATA0-19, ATD0-7, LA17-31,	I_{OL} = 24 mA				
	BUSCLOCK, /CS8042, /DACK0-3, /DACK5-7, /LBHE, OSC, RESET, RTCDS, RTCRW, /SMEMR, /SMEMW, TC	I_{OL} = 12 mA				
	GC132 Controller: ADDRSWT, BALE, BANKSEL0,1, /CASA-D, /EXRAS0,1, /IOR, /IOW, /MEMR, /MEMW, PARDATO0-3, PD0-7, /RAS0-3	I_{OL} = 12 mA				
	GC133 Interface: ATA0-19, ATD0-15,	I_{OH} = 24 mA				
	LBHE, MA0-9, PGVIOL	I_{OH} = 12 mA				
	All others (*GC131, GC132,* and *GC133)*	I_{OL} = 6 mA				
I_{IN}	Input current, Inputs with pulldown resistors Inputs with pullup resistors.	V_{IN} = V_{DD} or V_{SS} V_{IN} = V_{DD} V_{IN}=V_{SS}	-10 10 -100	± 1 35 -30	10 120 -8	µA µA µA
I_{OZ}	3-state output leakage current	V_{OH} = V_{SS} or V_{DD}	-10	+1	10	µA
I_{OS}	Output short circuit current(*)	V_{DD}=Max.V_O=V_{DD} V_{DD}=Max.V_O=0V	20 -10	110 -90	220 -190	mA mA
I_{DD}	Quiescent supply current	V_{IN} = V_{DD} or V_{SS} CLK = 20 MHz, CL = 50 pF		30		µA
C_{IN}	Input capacitance	Any input		2		pF
C_{OUT}	Output capacitance	Any output		4		pF

Physical and Electrical characteristics

Figure 14b—DC Characteristics (Continued)

Ratings, absolute maximum (Reference to VSS)			
Parameter	*Symbol*	*Limits*	*Unit*
Supply Voltage, DC	VDD	-0.3 to +7	V
Input Voltage, DC	VIN	-0.3 to VDD +0.3	V
Input current, DC	IIN	+10	mA

Figure 14c—Absolute maximum ratings

Recommended operating conditions			
Parameter	*Symbol*	*Limits*	*Unit*
Supply Voltage, DC	VDD	+3 to +6	V
Temperature, ambient operating range	TA	0° to 70°	C

Figure 14d—Recommended operating conditions

GC131 Peripheral Controller—Output signals, pins and drive capability at low Voltage output (VOL)

Pin Symbol	Pin No.	Slew Rate	Drive Capability
/AEN1	55	R	6 mA
/AEN2	56	R	6 mA
ATA0 to ATA16	79, 82-89, 91-98	R	24 mA
ATA17, ATA18, ATA19	10, 11, 13	R	24 mA
ATD0 to ATD7	36-39, 42-45	R	24 mA
BUSCLOCK	138	RP	12 mA
CK8042	146	None	6 mA
/CK8042	145	None	6 mA
CKEEP	151	R	6 mA
CONFIGAS	132	R	6 mA
CONFIGDR	134	R	6 mA
CONFIGDW	133	R	6 mA
CPUHRQ	64	R	6 mA
/CS287	153	R	6 mA
/CS8042	152	R	12 mA
CSEEP	150	R	6 mA
/CSVREG	111	R	6 mA
/DACK0 to /DACK3, /DACK5 to /DACK7	72 - 78	R	12 mA
DOEEP	135	R	6 mA
LA17 to LA31	113 to 119, and 122 to 129	R	24 mA
/LBHE	57	R	12 mA
/LW16MEG	137	R	6 mA
/MEMR	3	R	6 mA
/MEMW	2	R	6 mA
NDTSTOUT	8	R	6 mA
NMI	136	R	6 mA
OSC	18	RP	12 mA

Figure 14d—GC131; signals, pins and current

Physical and Electrical characteristics

Pin Symbol	Pin No.	Slew Rate	Drive Capability	Pin Symbol	Pin No.	Slew Rate	Drive Capability
PCSRPA	103	R	6 mA				
/PCSRPB	104	R	6 mA	RTCDS	155	R	12 mA
/PCSRPC	105	R	6 mA	RTCRW	156	R	12 mA
/PCSWPA	106	R	6 mA	/SERCS1	108	R	6 mA
/PCSWPC	107	R	6 mA	/SERCS2	109	R	6 mA
/REFRESH	58	None	OD	/SMEMR	144	R	12 mA
RESET	157	R	12 mA	/SMEMW	143	R	12 mA
RTCAS	154	R	6 mA	SPKRDATA	110	R	6 mA
				TC	63	R	12 mA

Note: With reference to 'Slew rate:'
R = Maximum Slew Rate Control. RP = Moderate Slew Rate Control. None = No Slew

Figure 14d (Cont.)—GC131, signals, pins and current

GC132 CPU/Memory Controller—Output signals, pins, and drive capability at low Voltage output (VOL)

Pin Symbol	Pin No.	Slew Rate	Drive Capability	Pin Symbol	Pin No.	Slew Rate	Drive Capability
ADDRSWT	130	None	12 mA	/INTA	25	R	6 mA
BALE	30	RP	12 mA	/IOR	28	RP	12 mA
BANKSEL0 BANKSEL1	149, 148	R	12 mA	/IOW	29	RP	12 mA
/BBEN0 to /BBEN4	124, 128	R	6 mA	IRQ13	53	R	6 mA
BBDIR0 BBDIR1	122 123	R	6 mA	/LBHE	24	R	6 mA
/BS32	19	R	6 mA	LBS16	14	None	6 mA
/BUSY386	54	R	6 mA	/LOCAL	99	None	6 mA
/CASA to /CASD	134 to 131	None	12 mA	/LWEN	31	None	6 mA
CLK646	118	R	6 mA	/MEMR	26	RP	12 mA
CLKM	46	R	6 mA	/MEMW	27	RP	12 mA
CLREXPTION	44	None	6 mA	/NA	146	None	6 mA
CONVAO	116	R	6 mA	PARDATO 0 to PARDATO 3	63, 58, 97, 102	None	12 mA
DBEN	32	None	6 mA	/PARITY	57	R	6 mA
/ENADDSTB	103	R	6 mA	PD0 to PD7	64-71	R	12 mA
/ERROR386	56	R	6 mA	PEREQ386	55	R	6 mA
/EXRAS0, /EXRAS1	136, 135	None	12 mA	PEREQ387	49	R	6 mA
				PROCCLK	38	None	6 mA

Figure 14e—GC132, signals, pins and current

Physical and Electrical characteristics

Pin Symbol	Pin No.	Slew Rate	Drive Capability	Pin Symbol	Pin No.	Slew Rate	Drive Capability
/RAS0 to /RAS3	144,143, 137,138	None	12 mA	SAB646	117	R	6 mA
/READY	147	None	6 mA	SPA20	153	R	6 mA
RESET387	51	None	6 mA	STARTCYC	100	None	6 mA
ROMADDR	151	R	6 mA	STEN	52	R	6 mA
/ROMEN	150	R	6 mA	/SYSCLK	41	None	6 mA
				TESTOUT	104	R	6 mA

Figure 14e (Cont.)—GC132, signals, pins and current

Physical and Electrical characteristics

GC133 Bus Bridge Interface—Output signals, pins, and drive capability at low Voltage output (VOL)

Pin Symbol	Pin No.	Slew Rate	Drive Capability	Pin Symbol	Pin No.	Slew Rate	Drive Capability
ATA0 to ATA19	147 to 148 & 95 to 100 & 103 to 114	R	24 mA	LBHE	126	None	12 mA
				MA0 to MA9	78, 82-90	None	12 mA
				PGVIOL	93	None	12 mA
				TSTOUT	128	None	6 mA
ATD0 to ATD15	129 to 139 & 142 to 146	None	24 mA				

Note: With reference to 'Slew rate:'
R = Maximum Slew Rate Control. RP = Moderate Slew Rate Control. None = No Slew Rate Control. OD = Open Drain.

Figure 14f—GC133, signals, pins and current

Section - 8 Application notes

This Section of the *GCK131 Chip Set Data Sheet* starts a series of Application Notes—information that should be used to develop AT-compatible 80386-based personal computer systems.

Concurrent with the release of the First Edition of the *GCK131 Chip Set Data Sheet* and, for convenience, the following Application Notes are included as part of the *Data Sheet.*

Application Notes

- Setting the system defaults (Section 8-1)
- System configuration defaults stored in EEPROM (Section 8-2)

Application Notes to be released from time to time

The *GCK131 Chip Set* offers a richness and versatility that will undoubtably present opportunities to enhance the operation of products that incorporate the Set. As information becomes available, it will be released as an Application Note; usually, each Note will cover a specific subject. As opportunity allows, future updates to the *GCK131 Chip Set Data Sheet* will incorporate all of the then current Application Notes.

8 - 1 Application note—Setting the system defaults

The startup default settings of the *GCK131 Chip Set* are not necessarily the optimum settings for every system design; but, by means of a simple patch to the BIOS programs, the defaults can be tailored to establish the required defaults. The patch code (such as the example described below) is placed in an empty space within the ROM addressing range.

How the *GCK131 Chip Set's* configuration registers are accessed.
The configuration registers are partitioned into regions. Each region is non-overlapping and unique. The I/O registers used to gain access to the registers are 024h and 028h.

- Register 024h is a write-only index resister.
- Register 028h is the data register.

Regardless of the chip in the chipset, each can be read or written by these two registers.

The standard way to read or write one of these registers is as follows:

1. Write the INDEX of the desired register to address 024h
2. Read/write the data from/to address 028h.

Each chip of the chipset has a unique INDEX space:

- GC132 resides from 00h to 0Fh,
- GC133 resides from 10h to 1Fh,
- GC131 resides from 40h to 4Fh.

Application note:

The INDEXES —the individual bits and their functions— are described earlier, in the *Configuration* section of this Data Sheet. When preparing the BIOS patch you should refer to the appropriate information.

Example of a BIOS Patch

Project:
To prepare a patch which will establish the correct configuration for a new system.

Defaults required:
The defaults of the *GCK131 Chip Set* are suitable with the following exceptions;

1. Quiet bus is to be disabled—Ref: *GC132 CPU/Memory Controller.*

2. 1 Mb DRAMs are installed in Bank 0 and Bank 1—Configured by the *GC132 Controller.*

3. The DRAMs in Bank 0 and Bank 1 are 1 Mb—Configured in the *GC133 Bus Bridge.*

Plan:
To implement these defaults, the 80386 BIOS is to be altered as follows:

After RESET, the CPU begins executing code at F000:FFF0 within the EPROM BIOS. One of the first instructions includes a jump to the location of the regular AT startup routine.

To implement the BIOS patch, change this instruction to have the jump directed to an empty section within the ROM space. At his new location execute the instructions required to reconfigure the GCK131 Chip Set. Then insert a jump to return to the regular AT startup routine.

Implementation.
For this example, there is an empty space in ROM at F000:5100. The regular 80386 AT startup routine is located at F000:E05B.

The finished code:

```
F000:5100  B001      mov     AL,01     ; Offset for GC132 setup register
F000:5102  E624      out     24,AL     ; Load index register
F000:5104  B008      mov     AL,08     ; Data for general setup register
F000:5106  E628      out     28,AL     ; Send data to register
F000:5108  B003      mov     AL,03     ; Offset for GC132 DRAM config
F000:510A  E624      out     24,AL     ;
F000:510C  B0A1      mov     AL,A1     ; Data for 1 Mb DRAMs in Bank 0,1
F000:510E  E628      out     28,AL     ;
F000:5110  B010      mov     AL,10     ; Offset for GC133 DRAM config
F000:5112  E628      out     4,AL      ;
F000:5114  E628      mov     AL,01     ; Data for 1 Mb DRAMs in Bank 0,1
F000:5116  B003      out     28,AL     ;
F000:5118  EA5BBE000F0   jmp  F000:E05B; Jump back to main program
```

Application note

Figure 15—BIOS Patch Code, System defaults

8 - 2 Application note—System configuration defaults stored in EEPROM

Project

This Application Note describes the use of an EEPROM device to store the *GCK131 Chip Set's* configuration data.

The device selected for this application is the National EEPROM Type MMC9306. The device has 256 bits of READ /WRITE memory and has 16 registers each of 16 bits.

Plan

Access to the EEPROM is to be restricted. We recommend, the use of a ROM-based setup program that will avoid improper programming of the EEPROM 's registers.

The *GCK131 Chip Set* has the required hardware to interface, directly, with EEPROM *MMC9306* and similar storage devices. Control of the EEPROM is accomplished with the use of a configuration register in the *GC131 Peripheral Controller*. The register, INDEX 45h, has configuration bits used in the selection of clocking, chip-select, and EEPROM data in/out. (For more information see *INDEX45h—EEPROM Control*).

Implementation

Development of product and BIOS configuration associated with the *GCK131 Chip Set* should be done in this manner.

1. As a general principle, the information stored within the EEPROM should support the changes required by a user (or a technician); but with a proven certainty, nothing associated with these user-selected changes should cause the system to crash.

Application note

2. In the event that the EEPROM loses its contents, the system should be able to boot using default parameters stored in a table within the system ROM.

In the design of the system, the important timing parameters (which become part of the default table stored in ROM) should not be accessible to the setup program.

Other limitations (such as maximum installed RAM, coprocessor type, and so on) are incorporated into the BIOS development using two levels of setup. The levels accommodate the needs of a/ manufacturing and b/ the system user.

In manufacture, the system is configured to match the exact amount of RAM installed, the size of EPROM used, and so on.

The user-accessible options include choices with respect to coprocessor type, PARITY , and others.

The values associated with these two types of allowable selections are stored in the EEPROM . A table, such as the following, should be translated for storage into the EEPROM and a similar default table should be available from within BIOS for use in the event that the EEPROM loses its memory.

Important registers that should be stored in EEPROM and accessible for user selection by a 'Setup' routine.

INDEX	Contents	Defaults
00h	*General setup bits* (Bits 0, 1, 3, 4, 6, 7)	00h
01h	*General setup bits* (Bits 0, 1, 3, 4, 5, 6, 7)	88h
03h	DRAM *configuration* (Bits 4, 5, 6, 7)	A0h
10h	DRAM *configuration* (Bit 3)	00h

Verification using the CHECKSUM routine.

An important part of the startup routine should include the execution of a 'checksum' verification to ensure the validity of the EEPROM and its contents. If the EEPROM is absent or its contents invalid, the system should revert to the default parameters in the table stored within the ROM. If, on the other hand, the checksum routine is correct then the EEPROM stored parameters can be used.

Under this procedure, of course, any new values programmed following user-initiated (or manufacturing) changes should, by the setup routine, be reflected in the 'checksum' value.

Application note:

Program code

The assembler code on the next pages details the steps necessary to READ and WRITE with the *MMC9306 EEPROM* .

The code includes several sub-routines called from a main routine.

Similar routines can be incorporated, directly, into the BIOS setup program for configuration register initialization.

```
TITLE     NVRAM HIGH SPEED ROUTINES
_TEXT     SEGMENT BYTE PUBLIC 'CODE'
_TEXT     ENDS

_DATA     SEGMENT WORD PUBLIC 'DATA'
_DATA     ENDS

CONST     SEGMENT WORD PUBLIC 'CONST'
CONST     ENDS

_BSS      SEGMENT WORD PUBLIC 'BSS'
_BSS      ENDS

DGROUP    GROUP          CONST, _BSS, _DATA
   ASSUME      CS:_TEXT, DS:DGROUP, SS:DGROUP, ES:DGROUP

_TEXT     SEGMENT

REGO      equ    028h
REGI      equ    028h      ; Location of register for clock toggle
REGP      equ    024h      ; Pointer register
REGN      equ     45h      ; Register associated with EEPROM
NVDI      equ    01h
NVDO      equ    01h
NVCS      equ    04h
NVCLK     equ    02h

; NVRAM program code functions */

EWEN      equ    30h       ;* Enable chip WRITE function */
ERASEOP   equ    0c0h      ;* Enable ERASE function */
WRITEOP   equ    40h       ;* Enable LOCATION DATA WRITE */
EWDS      equ    00h       ;* Disable chip WRITE function */
READOP    equ    80h       ;* Enable chip READ function*/

; Other constants

FALSE     equ    0
```

Figure 16—Assembler code to READ/WRITE to the EEPROM

Application note:

```
;====================================
;   Subroutine to give the command and address
;   to the NVRAM
;
;====================================

    PUBLIC      _nvaddr

_nvaddr proc near

    push    BP
    mov     BP,SP
    sub     SP,+04

    mov     bx,[bp+4]       ; Get command and address to write
    mov     dx,REGP         ; Tell GC131 to point to EEPROM data
    mov     al,REGN
    out     dx,al

    mov     dx,REGO
    in      al,dx           ; Get the register image
    and     al,not NVDI
    out     dx,al
    call qdel               ; Short delay
    or      al,NVCS
    out     dx,al
    call qdel               ; Short delay
    or      al,NVCLK
    out     dx,al
    call qdel               ; Short delay
    and     al,not NVCLK
    out     dx,al
    call qdel               ; Short delay
    or      al,NVDI
    out     dx,al
    call qdel               ; Short delay
    or      al,NVCLK
    out     dx,al
    call qdel               ; Short delay
    and     al,not NVCLK
    out     dx,al
    call qdel               ; Short delay
    mov     bh,80h          ; Set up the scanner bit
    mov     cx,8            ; Set to truck out 8 bits to nvram

nva1:       test    bl,bh
    jnz     nva2
```

Figure 16—Assembler code to READ/WRITE the EEPROM(Cont.)

Application note:

```
    and     al,not NVDI
    jmp     short nva3
nva2:       or      al,NVDI
nva3:       out     dx,al
    call qdel                   ; Short delay
    or      al,NVCLK
    out     dx,al
    call qdel                   ; Short delay
    and     al,not NVCLK
    out     dx,al
    call qdel                   ; Short delay
    shr     bh,1
    loop    nva1

    mov     SP,BP               ; Proper exit back to "C" code
    pop     BP
    ret

_nvaddr endp

;=====================================
;   Subroutine to write into the NVRAM at a
;   particular address.
;=====================================

    PUBLIC          _nvwrt

_nvwrt      proc near

    push    BP
    mov     BP,SP
    sub     SP,+04
    push    si

    mov     dx,024h             ; Tell GC131 to point to EEPROM data
    mov     al,45h
    out     dx,al

    mov     ax,EWEN             ; Enable the NVRAM ERASE function
    push    ax
    call    _nvaddr
    pop     ax
    mov     dx,REGO
    in      al,dx
    and     al,not NVCS         ; Disable the chip select
    out     dx,al
    call qdel                   ; Short delay
```

Figure 16—Assembler code to READ/WRITE the EEPROM(Cont.)

Application note:

```
    mov     bx,[bp+4]           ; Get location to erase
    or      bx,ERASEOP
    push    bx
    call    _nvaddr
    pop     bx
    mov     dx,REGO
    in      al,dx
    and     al,not NVCS         ; Disable the chip select again
    out     dx,al
    call qdel                   ; Short delay
    mov     ax,100
    push    ax                  ; Needs time to ERASE
    call    _delay
    pop     ax

    mov     bx,[bp+4]           ; Get back location to write again
    or      bx,WRITEOP
    push    bx
    call    _nvaddr
    pop     bx
    mov     dx,REGO
    mov     cx,16               ; Set up to send 16 data bits
    mov     bx,[bp+6]           ; Get data word to write
    mov     si,bx
    mov     bx,8000h
    in      al,dx               ; Get register image
nvw1:
    test    si,bx
    jz      nvw2
    or      al,NVDI
    jmp     short nvw3
nvw2:       and     al,not NVDI
nvw3:       out     dx,al
    call qdel                   ; Short delay
    or      al,NVCLK
    out     dx,al
    call qdel; Short delay
    and     al,not NVCLK
    out     dx,al
    call qdel                   ; Short delay
    shr     bx,1
    loop    nvw1

    and     al,not NVCS
    out     dx,al
    call qdel                   ; Short delay
    push    dx
```

Figure 16—Assembler code to READ/WRITE the EEPROM(Cont.)

Application note:

```
    mov     ax,100
    push    ax
    call    _delay
    pop     ax
    mov     ax,EWDS
    push    ax
    call    _nvaddr
    pop     ax
    pop     dx
    in      al,dx
    and     al,not NVCS
    out     dx,al
    call qdel                   ; Short delay
    pop     si
    mov     SP,BP               ; Proper exit back to"C" code
    pop     BP
    ret

_nvwrt      endp

;=====================================
;   Subroutine to read the NVRAM at a
;   particular address.
;=====================================

    PUBLIC          _nvrd

_nvrd       proc near

    push    BP
    mov     BP,SP
    sub     SP,+04
    push    si
    mov     dx,024h             ; Tell GC131 to point to EEPROM data
    mov     al,45h
    out     dx,al
    mov     bx,[bp+4]           ; Get location to read
    or      bx,READOP           ; Send read code and address to nvram
    push    bx
    call    _nvaddr
    pop     bx
    mov     cx,1000             ; Wait till the NVRAM is ready
nr1: mov    dx,REGI
    in      al,dx
    test    al,NVDO
    jz      nr2
;   call    _delay              ; Might be necessary
```

Figure 16—Assembler code to READ/WRITE the EEPROM(Cont.)

Application note:

```
    loop    nr1
nr2: and    cx,cx           ; If zero then we timed out
    jnz     nr3
    mov     ax,0ffh         ; Return ERROR STATUS
    jmp     short nrx

nr3: mov    dx,REGO
    mov     bx,8000h        ; Set up the scan bit
    mov     cx,16
    mov     si,0            ; This is the register that will assemble the character
                            ; from the NVRAM

; Now clock in 16 bits of data

nr4: in     al,dx
    or      al,NVCLK
    out     dx,al
    call qdel               ; Short delay
    push    dx
    mov     dx,REGI         ; Now get in the data bit
    in      al,dx
    test    al,NVDO
    jz      nr5
    or      si,bx           ; Sum in the bit
nr5: shr    bx,1            ; Shift the scan bit
    pop     dx
    in      al,dx
    and     al,not NVCLK
    out     dx,al
    call qde        l       ; Short delay
    loop    nr4
    and     al,not NVCS
    out     dx,al
    call qdel               ; Short delay
    mov     ax,si           ; Return the assembled word
nrx: pop    si
    MOV     SP,BP           ; Proper exit back to "C" code
    POP     BP
    RET

_nvrd       endp

_delay      proc near

    push    cx
    mov     cx,1000
del1:       in      al,REGP ; Delay element
```

Figure 16—Assembler code to READ/WRITE the EEPROM(Cont.)

Application note:

```
    loop    del1
    pop     cx
    ret

_delay      endp

qdel        proc    near
    push    ax
    push    cx
    mov     cx,5
qd1:        in      al,REGP    ; Delay element
    loop    qd1
    pop     cx
    pop     ax
    ret
qdel        endp


_TEXT       ends

    end
```

Figure 16—Assembler code to READ/WRITE the EEPROM(Cont.)

Application note:

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