Headland Technology
G2 Product Line

GC103

PRELIMINARY

EMS 4.0 Controller and Address Buffer

T-52-33-05

FEATURES

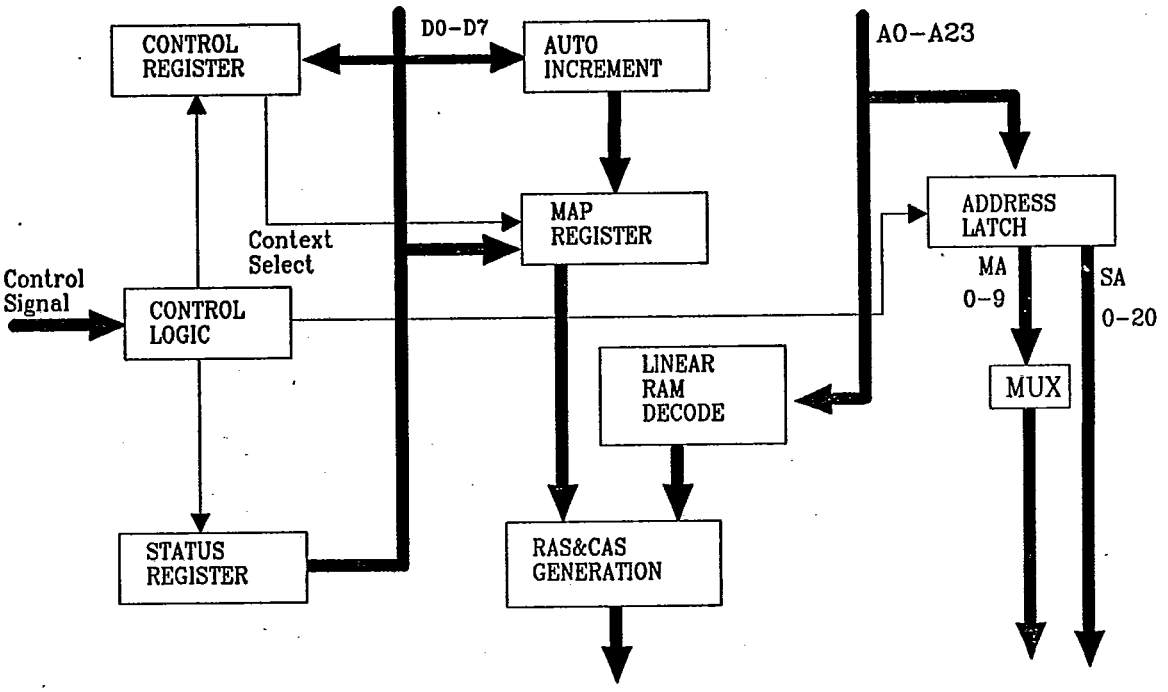
- **Hardware implementation of LIM EMS Version 4.0**
- **Includes Expanded Memory Manager Software**
- **Supports the use of up to 8 MB of on-board system memory**
- **Supports Shadow RAM**
- **Contains 2 sets of 32 EMS MAP Registers**
- **Supports 256K or 1M DRAMs**
- **Provides Address Buffer functionality**
- **Higher Integration; reduces system discrete device count**
- **HCMOS Technology**

DESCRIPTION

The GC103 is a companion chip to the GC101 / 102 AT chip set. Replacing the GC102 in its Address Buffer mode, this chip adds logic to fully implement LIM EMS 4.0. This device expands the capabilities of the GC101/102 chip set. It adds support for up to 8MB of memory and Shadow RAM for systems and video BIOS. The register-intensive design, combined with the use of system memory, offers extremely high EMS throughput compared with EMS systems using fewer mapping registers or expansion memory. The GC103 contains a chip mapping register that allows EMS to operate at full system speed without adding wait states. With 2 sets of 32 EMS registers context switching in hardware as well as software is supported.

The GC103 provides address buffering for the expansion bus, local I/O bus, and the system board DRAM. Address , DMA, and Refresh controls are included in the GC103. The chip integrates additional logic previously implemented discretely in the GC101/102 board design. This device is packaged in a 160 pin quad flatpack.

Chip Block Diagram



EMS and Address Buffering

The GC103 EMS Controller provides the necessary control to buffer the addresses of the A, SA, XA, LA, and MA buses. It also includes all the logic necessary for a hardware implementation of the Expanded Memory Specification. The CPUHLDA signal controls direction of the Address bus (A) flow; between the CPU and the Slot expansion (SA) bus. The Memory Address (MA) bus is generated by multiplexing the expansion (SA) bus with ADRSEL and /REFRESH.

EMS Address Translation

On power up the EMS function is disabled, all the DRAM addresses are left as flat linear addresses; ie without any EMS translations. An internal Linear Address Decoder accessses the lower 0-640K and 1 Meg and above -- to the upper limit of the system's memory. The top of the linear address space is defined by 2 switch settings. These switches (RAMSW1, RAMSW2) determine the number of RAM banks connected to the GC103. When the switches are left floating, bank selection can be controlled in software; where bits D5 and D6 of the Map Register (1EC) determine the number of banks.

Another I/O register selects the EMS pages; with the address space from 256K to 640K (decimal) and from C0000 to DFFFF (hex) being decoded as 32 pages. To get 64K of program memory, four contiguous pages are required. The EMS pages are accessed through the Map Address Register located at I/O address 1EE (hex); which is a read/write register.

Register Summary

The GC103 contains three internal EMS registers, all accessed via I/O operations, all read/writable. They are the Map Address Register (MAR) at 1EE, the Control Register (CR) at 1EF, and the Map Register (MR) at 1EC. The first two registers are 8 bits wide (I/O byte operations); the Map Register is 10 bits wide and thus requires I/O word accesses.

During I/O cycles, the MAR (1EE) provides a 6-bit address to the Map Register (a 64x10 Static RAM). This selects the register for programming or reading the maps. Writing data to the MR (1EC) programs the RAM, and that data becomes the uppermost address bits (translated A14-A19) when addressing DRAM in EMS operation. By selecting the auto-increment operation of the MAR, you can write once to MAR, and follow that with 64 writes to MR and fully program the RAM pages with the address translations. This programs both the standard and alternate context maps.

During memory cycles, address pins and a single bit from the CR (1EF) provide the 6-bit address to the Map Register (1EC). The MR then puts its programmed data onto the system's external DRAM address lines. After this summary concludes, there is a bit-by-bit description of these three registers.

The Map Register contains two sets of 32 registers; used as standard context maps and alternate context maps. This allows two programs to maintain separate and simultaneous register mappings, so switching between two programs is practically instantaneous. In systems with only a single set of 32 registers, when a second program needs to perform EMS operations, it must save the current mapping and then write it's own maps before starting. This requires time, and data may be lost in fast-moving communications programs. The two sets of 32 registers in the GC103 alleviate this problem.

For I/O cycles, the MAR (1EE) page bits (D0-D4) select 1 of 32 registers, and its Context bit (D5) selects between the two pairs of 32 registers. 0 selects the standard context maps, and 1 selects the alternate context maps. These six bits drive the address lines of the 64x10 RAM, or Map Register. An additional bit determines whether auto-incrementing is enabled (D7). If enabled, when a count of all ones is reached on D0-D6, D7 is cleared and auto-incrementing ceases.

For the memory cycles, 6 address pins select pages among the 32 registers. The address pins are either A14-A19 or SA14-SA19, depending upon whether the CPU has control of the system or not. Multiplexing of the 3 upper addresses, ie A17-A19, reduces this 6-bit address to 5 inputs to the Map Register. As with I/O cycles, there is a Context bit to select between the 2 sets of 32 registers. D0 of the Control Register (1EF) provides context information; a 0 selects the standard context maps.

The MR outputs 10 lines, the 7 least significant provide DRAM addresses, the next two perform bank selection and thus generate RAS0-RAS3, and D9 is for bank enable. When EMS memory accesses occur, A0 to A13 are passed unfiltered to the DRAM. A14 to A19 are redirected to the MR as addresses, and the Map Register outputs the replacement A14 to A19 addresses on its D0-D6 lines. (The smaller 256k DRAM uses only D0-D4 outputs.)

Four other bits within the CR, D7-D5 and D2, are software switches to select DRAM type (1M vs 256k DRAM), bank count, and extra 384K disable . The same functions can be controlled by grounding four pins on the GC103, respectively: RAM1M, RAMSW2 and RAMSW1 and SPLSW. The full EMS register descriptions follow.

MAP ADDRESS REGISTER 8 R/W bits, at I/O address 1EE(hex)	
D7	Auto-increment Enable Bit
D6	Carry Bit
D5	Context Selection
D4-D0	Page Selection 1 page (or more) of 32

D7: Auto-increment, Enable

When 1, each read or write of the Map Register (1EC) increments the count on D7-D0. These bits can be treated as a 8-bit counter, which auto-increment under D7 control. The counter consists of Auto-increment Enable (D7), Carry (D6), Context Selection (D5), and Page Address bits (D4-D0). When the count reaches all 1's (FF), the Enable bit is set to zero and auto-incrementing is turned off until another 1 is written to D7.

By initializing the counter to 80 hex (auto-incrementing on, carry off, standard context, and page 40,000 hex) the maximum number of automatic accesses is available. 32 standard-context writes are followed by 32 alternate-context writes; bringing the count to A0. Then, 32 reads in each context would increment the counter to 00. The 64th read clears the auto-incrementing enable (D7), and prevents further increments until D7 is manually set back to 1.

D6: Auto-increment, Carry Bit

This is the carry bit for D5-D0. If auto-incrementing is enabled (D7=1), the count on D7-D0 increments after every read/write access. When the count reaches all 1's, auto-incrementing mode is disabled.

With D6 = 0, and presuming the lowest page address and standard context, the counter stands at 80 hex. An initializing pass (of 64 writes to the Map Regsiter - 1EC) would automatically access the 32 standard-context registers, then the 32 alternate-context registers. The Map Address Register counter points to address A0. The second pass (64 reads of the Map Register) accesses the same 32 standard then 32 alternate-context registers. The counter reachs all 1's. This resets D7 and disables further incrementing.

With D6 = 1, the counter is preset to A0. A single pass (reading OR writing alone) through both the standard and alternate register maps forces bit D7 to 0, and disables auto-incrementing mode.

D5: Context Selection

When 0, standard context is the default
When 1, alternate context

The GC103 contains two sets of 32 registers, each maps to different available pages. Bit D5 switches between the two sets of registers during I/O cycles. (CR's D0 is context selection during memory cycles.) This allows one program to access its 32 mapping registers (standard context), and a second program has an alternate set of register maps (alternate context). With two pairs of registers available, changing between two programs is almost instantaneous, and data integrity is maintained. D5 selects the active set of map registers during I/O EMS cycles.

D4-D0: Page Selection

Page selection is determined by these 5 bits. Once latched in the MAR, with incrementing enabled, they generate the address lines to the Map Register for I/O cycles. Select the appropriate page(s) by setting D4-D0 according to Table 1 below. A minimum of 4 contiguous 16k pages must be selected for EMS operation. (EMS requires a Page Frame size of 64K or more, thus four 16K pages.) Note that page addresses are presented in the table below as both hexadecimal and decimal numbers.

Hexadecimal Page Address	Decimal Page Address	Register 1EE Bits D 4	DDDD 3210
DC000-DFFFF	880 - 896k	1	1111
D8000 -	864 -	1	1110
D4000 -	848 -	1	1101
D0000 -	832 -	1	1100
CC000-CFFFF	816 - 832k	1	1011
C8000 -	800 -	1	1010
C4000 -	784 -	1	1001
C0000-C3FFF	768 - 784k	1	1000
....	... ...		....
9C000-9FFFF	624 - 640k	1	0111
98000 -	608 -	1	0110
94000 -	592 -	1	0101
90000 -	576 -	1	0100
8C000-8FFFF	560 - 576k	1	0011
88000 -	544 -	1	0010
84000 -	528 -	1	0001
80000 -	512 -	1	0000
7C000-7FFFF	496 - 512k	0	1111
78000 -	480 -	0	1110
74000 -	464 -	0	1101
70000 -	448 -	0	1100
6C000-6FFFF	432 - 448k	0	1011
68000 -	416 -	0	1010
64000 -	400 -	0	1001
60000 -	384 -	0	1000
5C000-5FFFF	368 - 384k	0	0111
58000 -	352 -	0	0110
54000 -	336 -	0	0101
50000 -	320 -	0	0100
4C000-4FFFF	304 - 320k	0	0011
48000 -	288 -	0	0010
44000 -	272 -	0	0001
40000-43FFF	256 - 272k	0	0000
(4000 increments hex)	16k increments) decimal		

MAP REGISTER 10 R/W bits, at I/O address 1EC (hex)	
D9	Bank Enable
D8-D7	Bank Select
D6-D5	1M DRAM Address Bits
D4-D0	1M/256k DRAM Address Bits

D9 Bank Enable When 1, enables access to 1M/256k RAMs

D8-D7 Bank Select For 1M/256k, selection as follows:

D8	D7	
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 3

D6-D0 Translated address bits for 1 Meg DRAMs
They drive A20 to A14 on system DRAMs.

D6-D5 Unconnected for 256k DRAMs
D4-D0Translated address bits for 256k DRAMs
They drive A18 to A14 on system DRAMs.

CONTROL REGISTER 8 R/W bits, at I/O address 1EF (hex) Initial state: all 0's	
D7	DRAM-type Override
D6-D5	DRAM Bank-count Override
D4	Shadow Enable, F,0000 and FF,0000
D3	Shadow Enable, E,0000 and FE,0000
D2	Extra 384k Disable
D1	Global EMS Enable
D0	Context Selection

D7 DRAM-type Override. If RAM1M (input pin 36) is floating, this register bit selects the DRAM type. 1 Selects 1M DRAMs and 0 Selects 256k DRAMs

If a switch is connected to the RAM1M pin, the inverse level is read on bit D7 during the I/O read. RAM1M tied to ground is read as a 1, selecting 1M DRAMs. RAM1M tied to a pull up is read as 0, selecting 256k DRAMs. (default)

D6-D5 DRAM Bank-count Override.

Normally RAMSW1 and RAMSW2 define the number of RAM banks on the board. The operation of those 2 input pins follows:

RAMSW2 (pin 41)	RAMSW1 (pin 43)	RAM banks enabled
open	open	1 (default)
open	gnd	2
gnd	open	3
gnd	gnd	4

If RAMSW2 and RAMSW1 are floating, D6 and D5 are used to program the number of RAM banks installed, under BIOS control. D6 and D5 select the number of banks, as follows:

D6	D5	banks enabled
0	0	1
0	1	2
1	0	3
1	1	4

When reading D6 and D5 register bits back, their software settings are ORed with the inverse values on the RAMSW2 and RAMSW1 pins, respectively. For example:

if D6 = 0 and RAMSW2 = gnd read 1
if D6 = 0 and RAMSW2 = open read 0
if D5 = 1 and RAMSW1 = floating read 1

D4 Shadow Enable F0000 (source) and FF0000 (shadow)
D3 Shadow Enable E0000 (source) and FE0000 (shadow)

If D4=1, memory between F,0000 and F,FFFF is enabled and the contents are duplicated at FF,0000 to FF,FFFF. The 64k page of physical RAM that is accessed through this section is also enabled at addresses 15 Mega bytes away.

If D3=1, the base memory is between E,0000 and E,FFFF, the shadow memory is located at FE,0000 to FE,FFFF. The 64k page of physcial RAM accessed between E,0000 and E,FFFF is also enabled 15 Meg addresses away.

Enabling shadow RAM disables the RAM chip select; therefore data must be written into RAM before D4 and D3 are set high. To access this memory, you must reserve specific EMS pages for shadow RAM use. Select the type of board RAM, and whether both D3 and D4 are enabled, then reserve the appropriate 4 or 8 pages listed below. These RAM locations become read-only.

with:	256k DRAM	
and:	D4=1	D3=1
Shadow Pointer Registers	0298, 0299, 029A, 029B	029C,029D, 029E, 029F
with:	1 Meg DRAM	
and:	D4=1	D3=1
Shadow Pointer Registers:	0238, 0239, 023A, 023B	023C, 023D, 023E, 023F

D2 Extra 384k Disable

If the SPLSW (input pin 19) is floating, this register bit disables/enables the 384K. A 1 written to D2 disables the extra 384K, a 0 enables it. If the SPLSW is grounded, the extra 384K is disabled.

Normally the 384K address range, located between A000 and 1 Meg, is relocated above the 1M border. This preserves the lower addresses for system use. With the SPLSW floating and D2=1, the relocated 384K is disabled and usable as shadow RAM or as EMS. When this bit is read back, the result is D2 ORed with the inverse of SPLSW.

D1 Global EMS Enable

If D1 = 1, EMS memory is enabled. You must initialize the EMS registers before D1 is set high.

D0 Context Selection

If D0 = 0, the standard context is selected; if 1, the alternate context. This bit operates in the same manner as bit D5 of Register 1EE, except this determination of context is used during Memory cycles.

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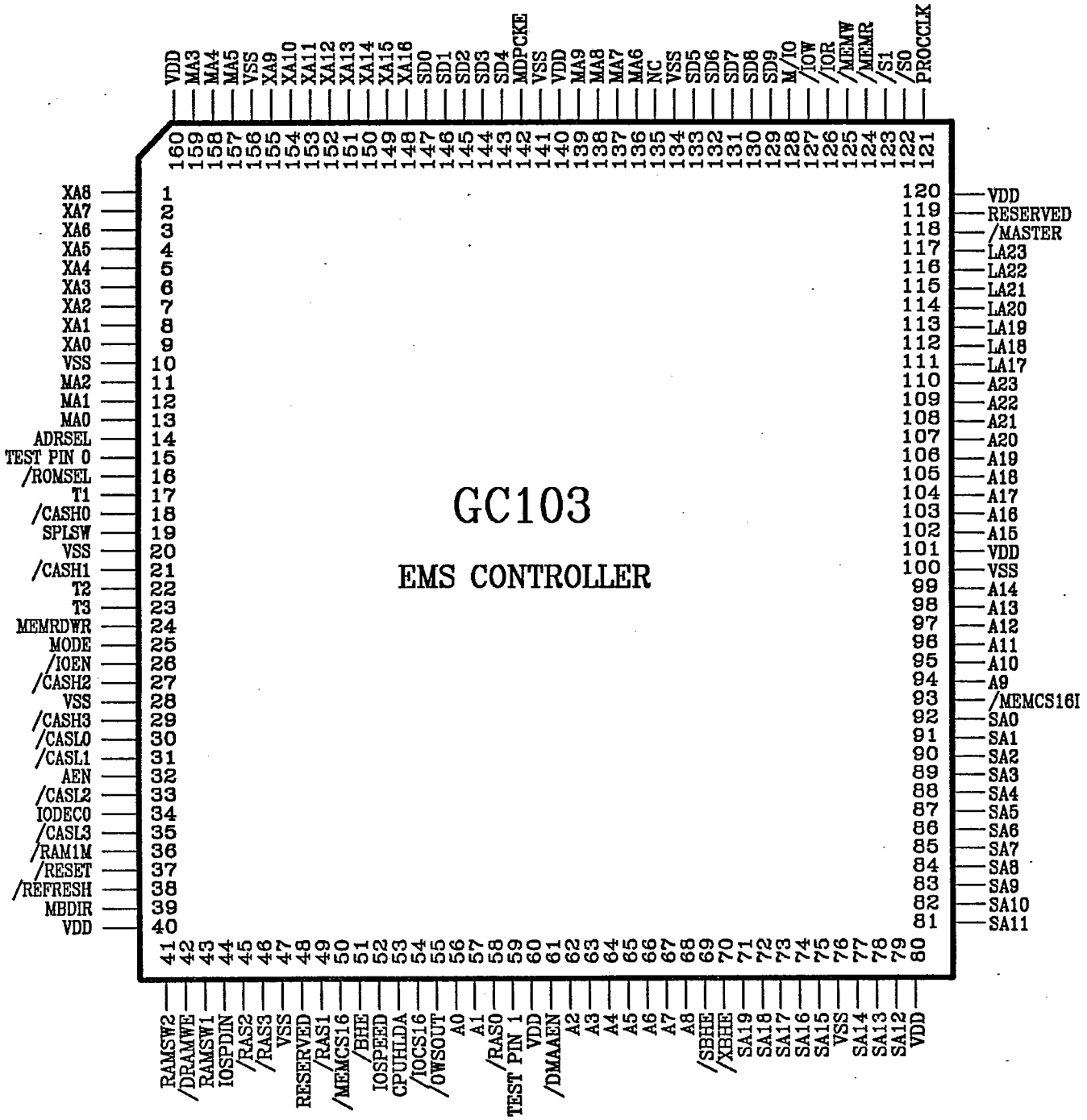
Pin Diagram



Pin Symbol	Pin Numbers	Pin Type	Description
A0-A16	56,57,62-68,94-99,102-103	I	Address bits 0-16: Inputs from 80286 CPU. The GC103 takes the address bus inputs and generates SA bus for I/O slots, the XA bus for peripherals, and the MA bus for the system DRAM.
A17-A23	104-110	I/O	Address bits 17-23: Input lines from 80286 CPU. See above.
ADRSEL	14	I	ADDress SELection: This input from on-board delay logic determines when the RAS or CAS address of MA9 is output. (Pertinent only for 1 Megabyte DRAMs, which use MA9 as uppermost address bit.)
AEN	32	I	DMA Address ENable: When high, the DMA controller inside the GC101 controls the address and data buses, I/O read/write lines, and memory read/write signals.
/BHE	51	I	Byte High Enable: A low at this input enables the high-order byte of the D bus, D15-8.
/CASH0-/CASH3	18, 21, 27, 29	O	Column Address Strobe, High order byte: these control up to four banks of DRAMs.
/CASL0-/CASL3	30, 31, 33, 35	O	Column Address Strobe, Low order byte: these control the four banks of DRAMs.
CPUHLDA	53	I	CPU HoLD Acknowledge: The 80286 drives this input high to indicate that it has released control of its buses.
/DMAAEN	61	I	DMA Address ENable:. A low input indicates a DMA operation is in progress.

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Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
/DRAMWE	42	O	DRAM Write Enable: Generates the write strobe to DRAMs controlled by GC103. This is a gated signal derived from the /MEMW input.
/IOCS16	54	O	IO Chip Select, 16 bits: Open drain output to indicate that the current I/O operation is a 16 bit operation. Input to the GC101.
IODEC0	34	O	I/O Decode 0: A decode of I/O address 1EC, 1ED, or 1EF drives this output high.
/IOEN	26	I	I/O ENable: Decode input for registers internal to the GC103. Connected to IODEC0 output, for address decode of 1EC-1EF. External decode logic may be used if other I/O addresses are required.
IOSPDIN	44	I	I/O SPeeD INput: Slower external devices force this input high, requesting a reduced I/O frequency for off-borad memory or peripherals. The GC103 responds by setting its output, IOSPEED, high. A low at this input allows the system clock to run at full speed. (See IOSPEED below)
IOSPEED	52	O	I/O SPEED: This output drives the GC101 IOSPEED pin. It indicates that the system clock is to be slowed down (1/2 speeed) to accomodate off-board memory and peripherals. A high signal indicates half speed, a low - full speed.
/IOR	126	I	I/O Read: Input from the GC101.
/IOW	127	I	I/O Write: Input from the GC101.
LA17-23	111-117	I/O	Latched Address bits, 17-23: I/O addresses available on the AT expansion slots. Direction is controlled by the /MASTER input.

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Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
MA0-MA9	13-11,159-157,136-139	O	Multiplexed Address bus: to DRAMs.
/MASTER	118	I	MASTER: Control signal from the AT expansion bus. When low, allows a peripheral on the expansion bus to have system control.
MBDIR	39	O	Memory Bus DIRection control: When high, data flows from the MD0-15 bus to the SD0-15 bus. When low, the data flow is reversed. RAM and ROM data is transmitted on the MD bus.
MDPCKE	142	O	Memory Data Parity CheckK Enable: A high on the pin enables the parity checking logic of the GC102 data buffer.
/MEMCS16	50	I	MEMory Chip Select, 16 wide: External devices drive this input low for 16-bit data transfers. In turn, the GC103 sets it's output pin /MEMCS16I low, alerting the GC101 of the 16-bit transfer.
/MEMCS16I	93	O	MEMory Chip Select, 16-bits: A low on this output alerts the GC101 that the current memory access is 16 bits wide. The polarity of this output is controlled by the level on the input pin, /MEMCS16. A low at that input, forces this output low.
/MEMR	124	I	MEMory Read: A low from GC101 indicates a read is in progress.
MEMRDWR	24	O	MEMory ReaD or WRite cycle: to delay line input .
/MEMW	125	I	MEMory Write: A low from GC101 indicates a write cycle.
M/IO	128	I	Memory or I/O status from 80286 CPU.

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Pin Description

Pin Symbol	Pin Numbers	Pin Type	Description
MODE	25	I	"1" = 286, "0" = 386SX
PROCCLK	121	I	PROCcessor CLocK: Internal system clock. Driven by GC101.
/RAM1M	36	I	RAM 1 Megabyte: Tie this input to Ground, for 1 Megabyte DRAM. Connect the input to VCC for 256K byte DRAM.
RAMSW1, RAMSW2	43, 41	I	RAMSW1 / RAMSW2 / # OF BANKS INSTALLED VCC / VCC / 1 VCC / VCC / 2 VCC / ground / 3 ground / ground / 4 If these pins are floating, Register 1EC, bits D6 and D5 define the number of banks installed. See the register description section for more details.
/RAS0-/RAS3	58,49,45,46	O	Row Address Strobe: RAS selection for 4 banks of DRAM.
/REFRESH	38	I, OD	Refresh: Input from the GC101 is low when the current cycle is a memory refresh. (Open Drain)
/RESET	37	I, OD	RESET: A low from the GC101 resets internal logic. (Open Drain)
/ROMSEL	16	O	ROM SELect: A low enables signals from the BIOS ROMS or EPROMS.
SA0	92	I	System Address bit 0: Address input from GC101.
SA1-SA19	91-81, 79-77, 75-71	I/O	System Address bus: Bi-direction bus to/from the PC expansion slot.

Pin Symbol	Pin Numbers	Pin Type	Description
/SBHE	69	I/O	System Byte High Enable: Low when peripherals are performing a transfer on the upper byte.
SD0-SD9	147-143, 133-129	I/O	System Data bus: to/from PC bus.
SPLSW	19	I	Enable last 384K section of RAM SPLSW = 0 Extra 384K section disable SPLSW = 1 Extra 384K section enable If this pin is floating, Register 1EF, bit D2 determines whether the additional 384k of RAM is enabled. See register description section.
/S0, /S1	122,123	I	Status bits 0 and 1: inputs from the 80286 CPU. When these 2 pins are low, INTA is low, and M/IO is high, a shutdown or halt of the 80286 occurs. The level on A1 selects which of those two events; A1=0 is system shutdown, A1=1 is a halt.
TEST PIN 0,1	15, 59		Reserved.
T1-T3	17, 22, 23	I	Time Delays: MEMRDWR is the input to a delay counter. The counter generating successively longer delays called ADRSEL, T1, T2 and T3 respectively. Used for CAS input timing.
XA0	9	I	External Address 0: This input from the GC101 enables low byte transfers between the SD and MD buses.
XA1-XA16	8-1, 155-148	I/O	External Address: bus to/from the GC101.

Pin Symbol	Pin Numbers	Pin Type	Description
/XBHE	70	I/O	EXternal Byte High Enable: Low when peripherals are performing a transfer on the upper byte.
/0WSOUT	55	O	Zero Wait State OUTput to the GC101 indicates the current memory access should not have any wait states inserted.
VDD	40, 60, 80, 101, 120, 140,160		Power pins.
VSS	10,20,28,47,76,100, 134,141,156		Ground Power Pins.
NC	135		No Connection.
RESERVED	119		Reserved for IOCHRDY on the GC113.
RESERVED	48	I	Reserved for 1MMIX on the GC113.

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DC Characteristics

Absolute Maximum Ratings (Referenced to VSS)

Parameter	Symbol	Limits	unit
DC Supply Voltage	VDD	-0.3 to +7	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
DC Input Current	IIN	+10	mA
Storage Temperature Range (Plastic)	TSTG	-40 to +125	C

Recommended Operating Conditions

Parameter	Symbol	Limits	unit
DC Sypply Voltage	VDD	+3 to +6	V
Operating Ambient Temperature Range Commercial	TA	0 to +70	C

DC Characteristics: VDD = 5V + 5%, TA = 0 C to 70 C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Voltage Input LOW	VIL				0.8	V
Voltage Input HIGH	VIH		2			V
Input Current	IIN	VIN = VDD OR VSS	-10	+1	+10	uA
w/internal pulldown		VIN = VDD	10	35	120	uA
w/internal pullup		VIN = VSS	-100	-30	-8	uA
Voltage Output High	VOH		2.4	4.5		V
/RAS0-3,//DRAMWE,MA0-9		IOH=12mA				
/MEMCS16I, /CASL0-3,						
/CASH0-3,SD0-9,		IOH=8mA				
SA1-19, A17-23,/XBHE,/SBHE		IOH=6mA				
XA1-18,LA17-23,MEMRDWR		IOH=4mA				
/ROMSEL,MDPCKE,MBDIR,						
IODEC0,IOSPEED		IOH=2mA				
Voltage Output LOW	VOL			0.4	0.8	V
/RAS0-3,/DRAMWE,MA0-9		IOL=24mA				
/MEMCS16I,/CASL0-3,/IOCS16						
/CASH0-3,SD0-9,/0WSOUT		IOL=16mA				
SA1-19,A17-23,/XBHE,/SBHE		IOL=12mA				
XA1-18,LA17-23,MEMRDWR		IOL=8mA				
/ROMSEL,MDPCKE,MBDIR,						
IODEC0,IOSPEED		IOL=4mA				
3-State Output Leakage Current	IOZ	VOH=VSS or VDD	-10	+1	10	uA
Output Short Circuit Current	IOS	VDD=Max,VO=VDD	20	110	220	mA
		VDD=Max,VO=0V	-10	-90	-190	mA
Supply Current	IDD	CLK=16MHz,CL=50pf		150		mA

Note: Not more than one output may be shorted at a time for a maximum duration of one second.

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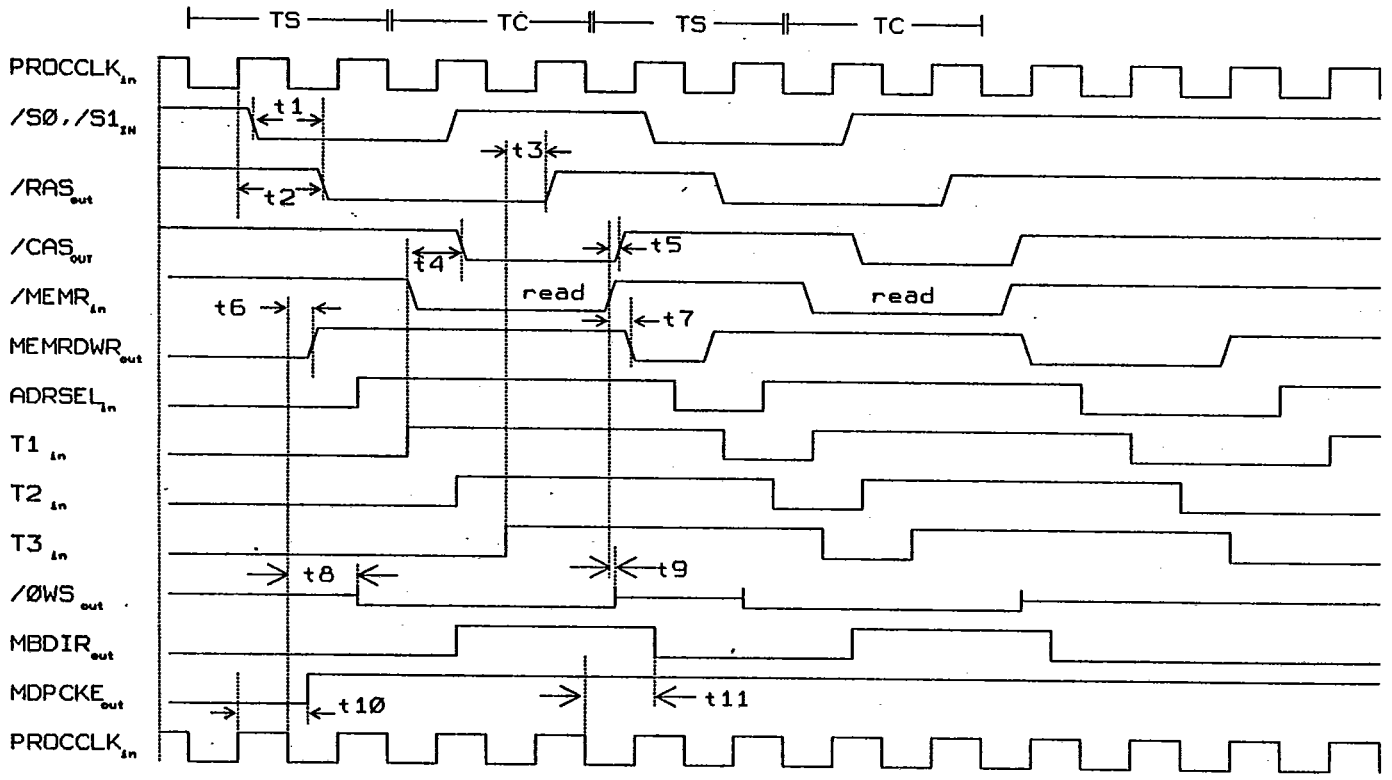
AC Characteristics

Sym	Description	Min ns	Typ ns	Max ns
t1	/S1 to /RAS low		28	
t2	PROCCLK to /RAS low		31	
t3	T3 to /RAS high		9	
t4	T1 to /CAS low		9	
t5	/MEMR to /CAS high		10	
t6	PROCCLK to MEMRDWR high		10	
t7	/MEMR to MEMRDWR low		6	
t8	PROCCLK to /0WS low		19	
t9	/MEMR to /0WS 3s		5	
t10	PROCCLK to MDPCKE high		15	
t11	PROCCLK to MDPCKE low		18	
t12	/MEMW to /RAS low		12	
t13	T3 to /RAS hgih		9	
t14	T1 to /CAS low		9	
t15	/MEMW to /CAS high		10	
t16	/MEMW to DRAMWE low		7	
t17	/MEMW to DRAMWE high		5	
t18	/MEMW to MEMRDWR high		5	
t19	/MEMW to MEMRDWR low		6	
t20	PROCCLK to MBDIR low		18	
t21	PROCCLK to /ROMSEL low		19	
t22	/MEMR to MBDIR high		10	
t23	/MEMR to MBDIR low		16	
t24	A bus to LA bus output		14	
t25	PROCCLK to SA bus output		22	
t26	PROCCLK to XA bus output		24	
t27	PROCCLK to MA bus output		24	
t28	ADRSEL to MA bus		14	
t29	ADRSEL to MA bus		13	
t30	/MASTER to SA bus output		16	
t31	/MASTER to LA bus output		16	
t32	SA to MA bus valid		12	
t33	LA to MA bus invalid		8	
t34	SA to XA bus		16	
t35	SA to XA bus invalid		16	
t36	PROCCLK to IODEC low		26	
t37	/IOR, /IOW to / IOCS16 low		9	
t38	/IOR, /IOW to /IOCS16 high		5	
t39	PROCCLK to /MEMCS16I low		14	
t40	PROCCLK to /MEMCS16I high		15	
t41	/MEMCS16 to /MEMCS16I low		8	
t42	/MEMCS16 to /MEMCS16I high		6	
t43	/DMAAEN to /XBHE, /SBHE		15	
t44	/XBHE to /SBHE		13	
t45	/S0, /S1 to /XBHE, /SBHE		14	
t46	/BHE to /XBHE, /SBHE		10	



MEMORY READ, ZERO WAIT STATE

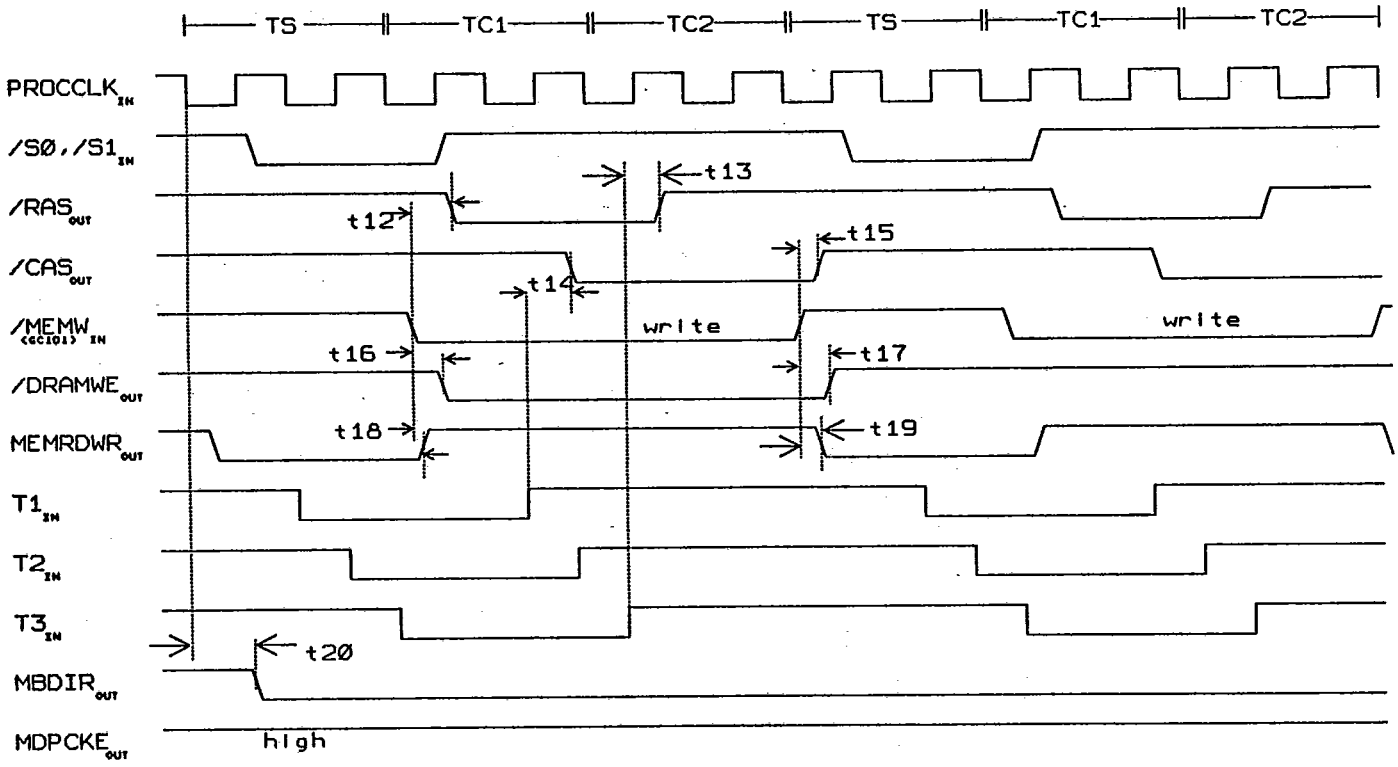
Figure 1

PRELIMINARY
GC103 7-7-89

Headland Technology
G2 Product Line

PRELIMINARY

GC103
Timing



MEMORY WRITE, 1 WAIT STATE

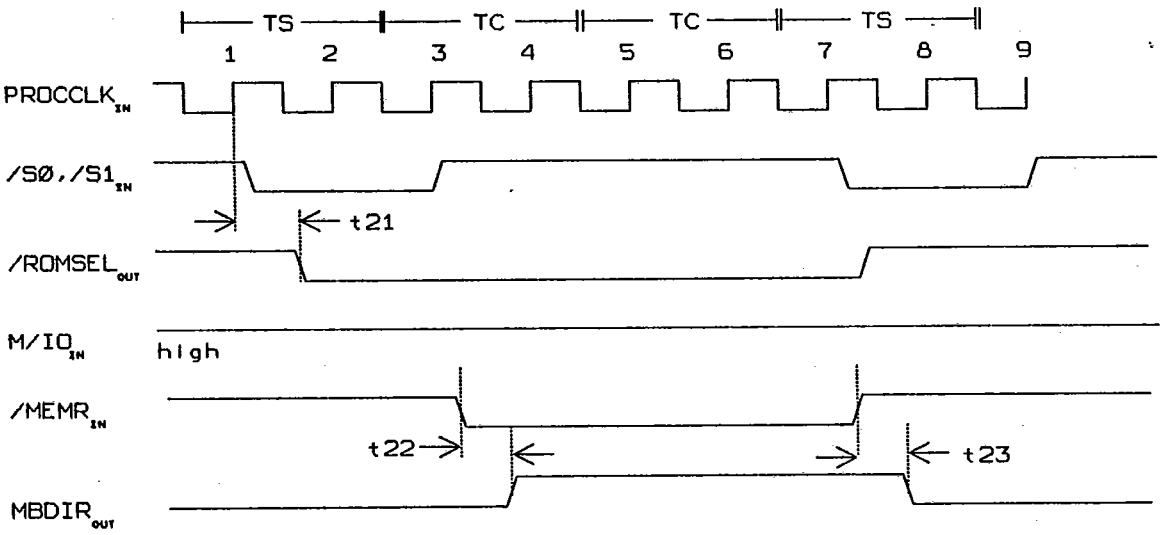
Figure 2

PRELININARY
GC103 7-7-89

Headland Technology
G2 Product Line

PRELIMINARY

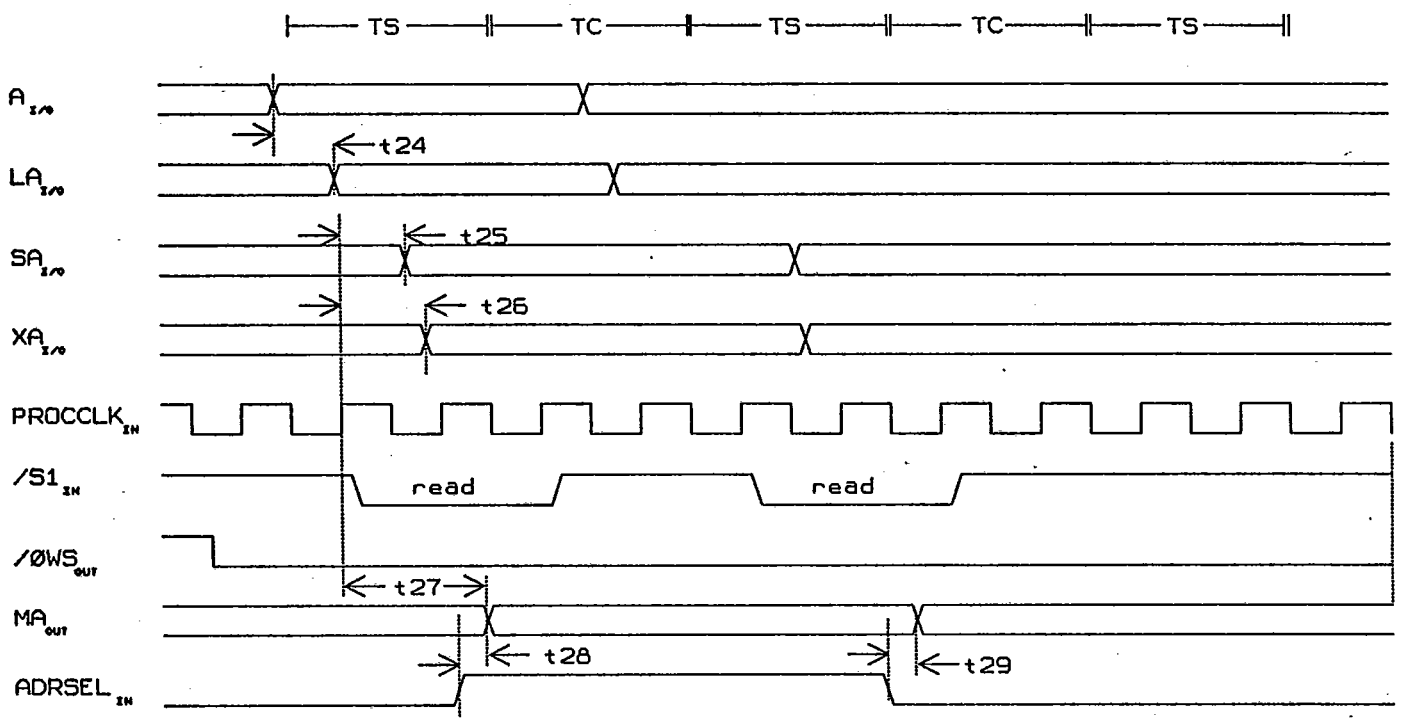
GC103
Timing



GC103 OUTPUT TIMING

Figure 3

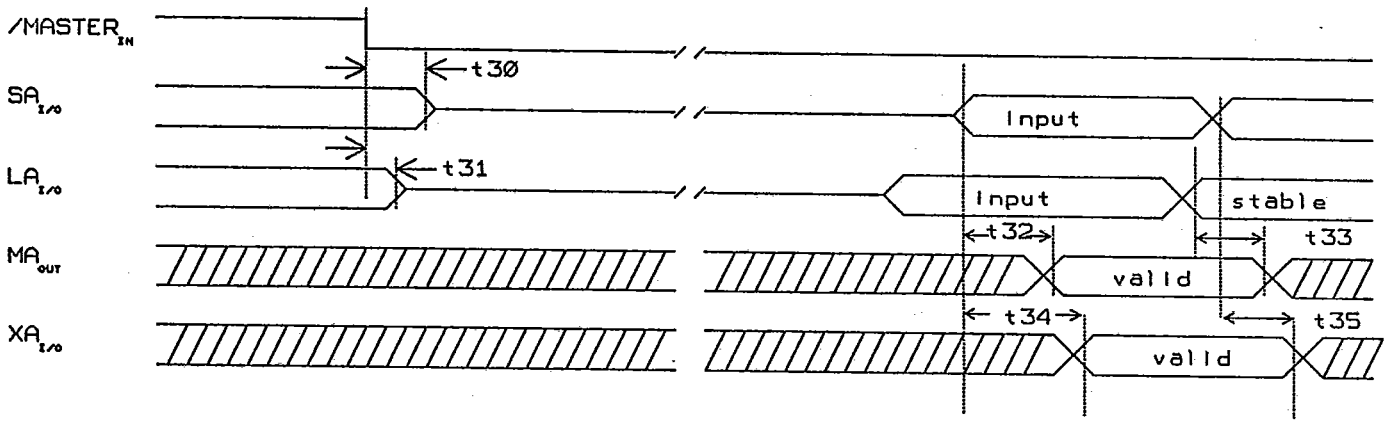
PRELIMINARY
GC103 7-7-89



ADDRESS BUS TIMING (Read Cycle)

Figure 4

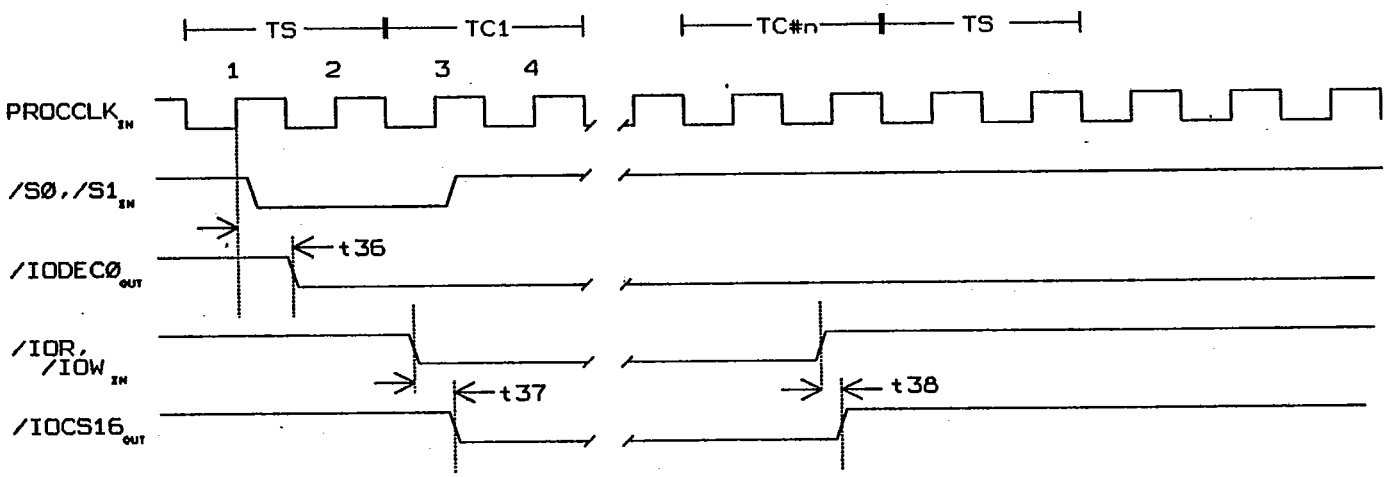
PRELIMINARY
GC103 3-06-89



BUS MASTER ADDRESS BUS TIMING

Figure 5

PRELIMINARY
GC103 3-06-89



OUTPUT CONTROL SIGNAL TIMING

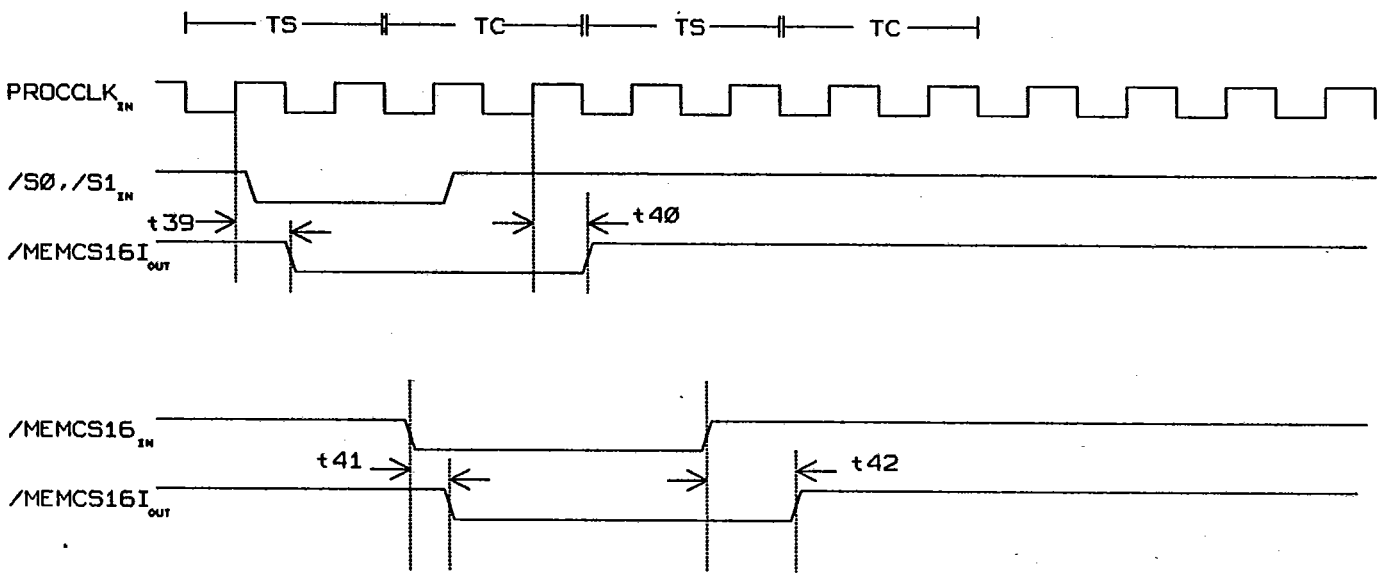
Figure 6

PRELIMINARY
GC103 7-7-89

Headland Technology
G2 Product Line

PRELIMINARY

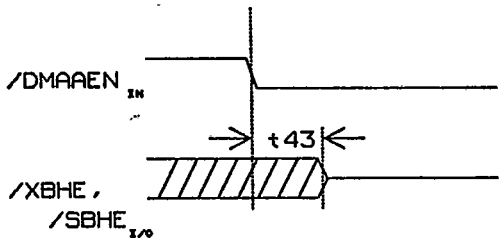
GC103
Timing

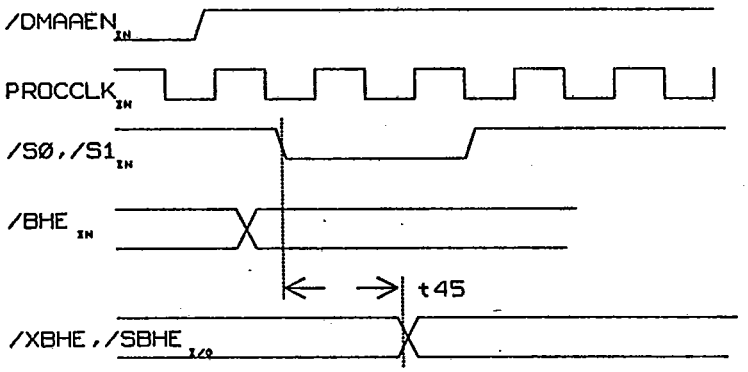


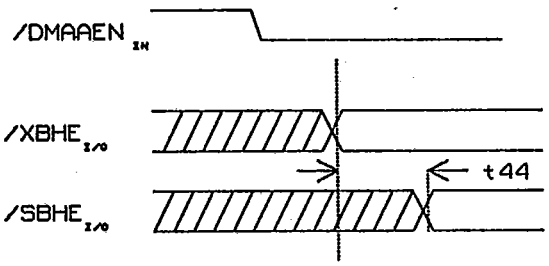
OUTPUT CONTROL SIGNAL TIMING

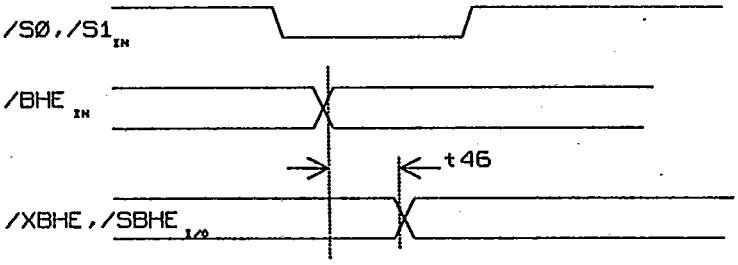
Figure 7

PRELIMINARY
GC103 7-10-89









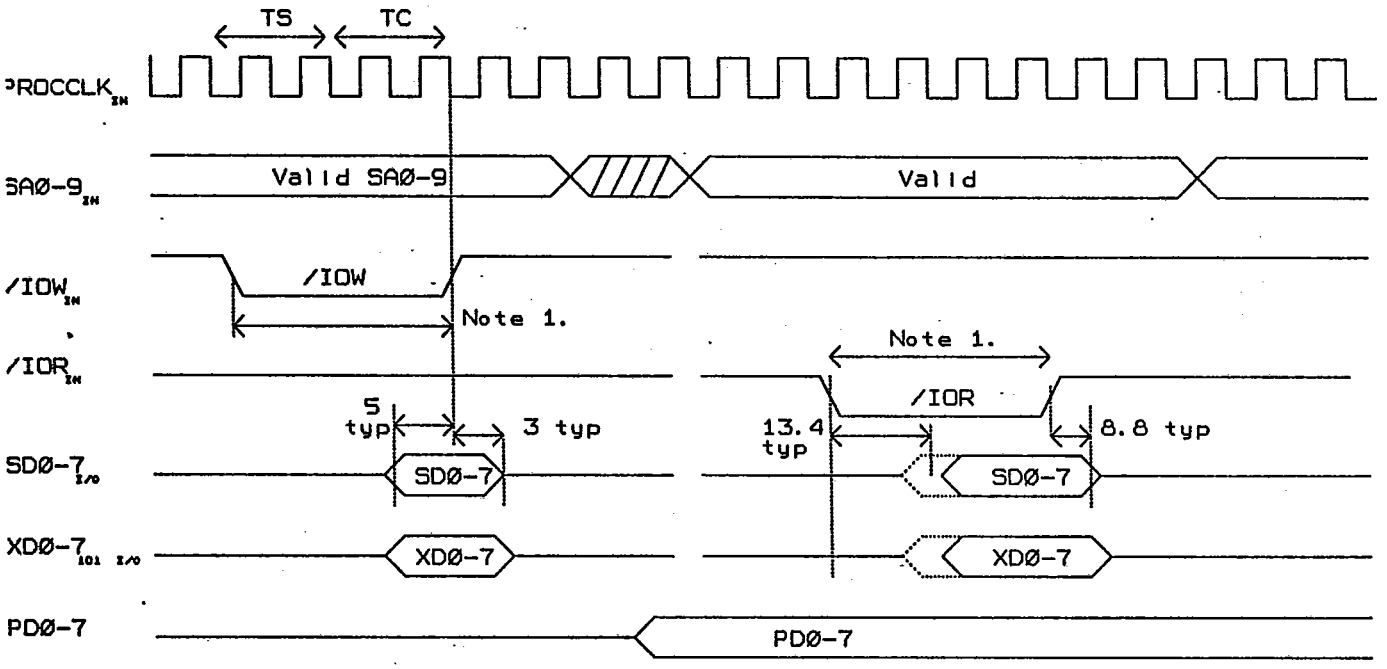
I/O TIMING
Figure 8

PRELIMINARY
GC103 3-06-89

Headland Technology
G2 Product Line

PRELIMINARY

GC103
Timing



Note 1:
3 Procclk cycles min

ADDRESS BUS TIMING

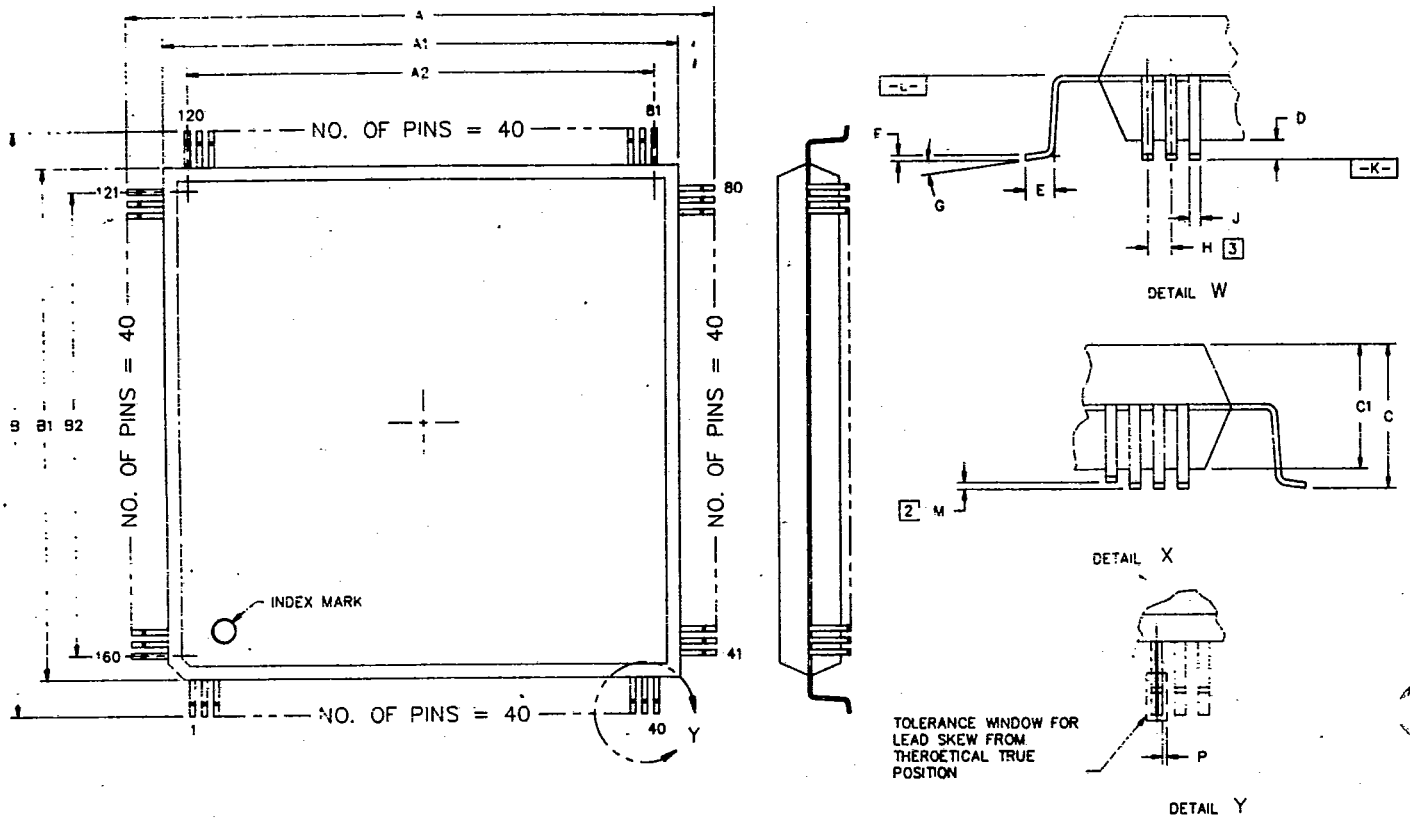
Figure 9

PRELIMINARY
GC103 4-11-89

Headland Technology
G2 Product Line

GC103
Package Outline

160-Pin Flat Pack (Gull Wing)



NOTES: UNLESS OTHERWISE SPECIFIED

1. NOMINAL DIMENSIONS IN MILLIMETERS. INCHES ROUNDED TO THE NEAREST .001 INCH.
2. COPLANARITY OF ALL LEADS SHALL BE WITHIN 0.1 MM (0.004") (DIFFERENCE BETWEEN HIGHEST AND LOWEST LEAD WITH SEATING PLANE -K- AS REFERENCE)
3. LEAD PITCH DETERMINED AT DATUM -L-

[1]

DIMENSIONS IN MM		
SYM	MINIMUM	MAXIMUM
A	31.60	32.40
A1	27.90	28.10
A2	25.35 REF	
B	31.60	32.40
B1	27.90	28.10
B2	25.35 REF	
C	3.94 MAX	
C1	3.55 MAX	
D	0.00	0.30
E	0.60	1.00
F	0.10	0.25
G	0°	10°
H	0.65 ±0.15	
J	0.25	0.35
M	0.10 MAX	
P	0.05 MAX	
TOTAL NO. OF PINS	160	

[1]

DIMENSIONS IN INCHES		
SYM	MINIMUM	MAXIMUM
A	1.244	1.276
A1	1.098	1.106
A2	0.998 REF	
B	1.244	1.276
B1	1.098	1.106
B2	0.998 REF	
C	0.155 MAX	
C1	0.140 MAX	
D	0.000	0.012
E	0.024	0.039
F	0.004	0.010
G	0°	10°
H	0.026 ±0.006	
J	0.010	0.014
M	0.004 MAX	
P	0.002 MAX	
TOTAL NO. OF PINS	160	

IMPORTANT NOTE

If designing in inches, ALL pin positions should be calculated in millimeters (mm) then converted to inches. The inches listed have been rounded.