4. e88C411 ELECTRICAL & TIMING SPECIFICATION

4.1 Absolute Maximum Ratings

(Vss = 0 volts)

Stresses above the conditions listed in this section may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at these or any other conditions above those indicated in the Recommended Operating Conditions section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute Minimum Ratings for e88C411

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	-0.3	7.0	Volts
Input Voltage	V_i	-0.3	V_{cc} + 0.3	Volts
Storage Temperature	T_{stg}	-40.0	125.0	degrees C

4.2 e88C411 Recommended Operating Conditions

(Vss = 0 volts)

Table 4-2. Recommended Operating Conditions for e88C411

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	4.75	5.25	Volts
Input Voltage	V_i	0	V_{cc}	Volts
Ambient Temperature	T_a	0	50	degrees C

4.3 e88C411 DC Characteristics

(Vcc = 5V +/- 5%, Ta = 0 to 70° C)

Table 4-3. e88C411 DC Characteristics

PARAMETER	SYMBOL	VALUE MIN	VALUE MAX	UNIT
Input Low Voltage	Vil			
TTL level			.8	Volts
Schmitt level			1.0	Volts
Input High Voltage	Vih			
TTL level		2.0		Volts
Schmitt level		4.0		Volts
Input Low Current	Iil	-10	-10	μA
W/ Pull-up Resistor		-200	-10	μA
Input high current	Iih	-10	10	μA
Output low voltage 2 mA buffer, IOL = 2mA 4 mA buffer, IOL = 4mA 8 mA buffer, IOL = 8mA 12 mA buffer, IOL = 12 mA	Vol		0.4	Volts
Output high voltage 2 mA buffer, IOH = -2mA 4 mA buffer, IOH = -4mA 8 mA buffer, IOH = -8mA 12 mA buffer, IOH = -12mA	Voh	2.4		Volts
High Impedance Leakage Current	Ioz	-10	10	μA
Device Quiescent Supply Current	Iccq		TBD	μA
Supply Current	Icc		TBD	mA
Power Dissipation	Pdis		TBD	mW
Input Capacitance	Cin		7	pF
Output or I/O Capacitance	Cout		10	pF

4.4 e88C311 AC Characteristics

(Vcc = 5V +/- 5%, Ta = 0 to 70° C)

4.4.1 Clock Timing

		25MHZ		33MHZ		
	SYMBOL	MIN	MAX	MIN	MAX	UNIT
411CLK period	T101		40		30	ns
411CLK high at 3.7V	T102	5		4		ns
411CLK low at 0.8V	T103	5		4		ns
411CLK rise time (0.8V to 3.7V)	T104		6		4	ns
411CLK fall time (3.7V to 0.8V)	T105		6		4	ns
ATSCLK period	T106	125	167	125	167	ns
ATSCLK high at 3.7V	T107	55*		55*		ns
ATSCLK low at 0.8V	T108	55*		55*		ns
ATSCLK rise time (0.8V to 3.7V)	T109		12		12	ns
ATSCLK fall time (0.8V to 3.7V)	T110		12		12	ns
CLKOUT delay from OSCIN falling edge	T111	6	13	4	12	ns
CLKOUT delay from OSCIN rising edge	T112	7	15	5	13	ns

*NOTE: Assuming an 8 MHz AT bus

4.4.2 Reset Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
RESET1- setup time to 411CLK rising edge	T201	14		10		ns
RESET3 active from 411CLK rising edge	T202	5	10	4	10	ns
RESET3 inactive from 411CLK rising edge	T203	5	10	4	10	ns
RESET3 pulse width	T204	40Δ		40Δ		
RESET4 active from 411CLK rising edge	T205	5	17	4	13	ns
RESET4 inactive from 411CLK rising edge	T206	5	17	4	13	ns
RESET4 pulse width	T207	40Δ		40Δ		
NPRST active from 411CLK rising edge	T208	5	17	4	13	ns
NPRST inactive from 411CLK rising edge	T209	5	17	4	13	ns
NPRST pulse width	T210	40Δ		40Δ		
RESET3 active from 411CLK rising edge	T211	5	17	4	13	ns
NPRST active from 411CLK rising edge	T212	5	17	4	13	ns
RESET2- Set up to 411CLK rising edge	T215	14		10		ns

Δ = 411CLK

4.4.3 AT Bus Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
BALE active from ATSCLK falling edge	T301		20		15	ns
BALE inactive from ATSCLK rising edge	T302		20		15	ns
COMMAND active from ATSCLK rising edge	T303		18		14	ns
COMMAND inactive from ATSCLK rising edge	T304		18		14	ns
XA0-XA16, XBHE valid from ATSCLK falling Edge	T305		18		14	ns
XA0-XA16, XBHE hold time after COMMAND invalid	T306	60		60		ns
LA17-LA23 valid from ATSCLK rising edge	T307		20		15	ns
LA17-LA23 hold time after COMMAND invalid	T308	60		60		ns
IOCS16- setup time to ATSCLK falling edge	T309	18		18		ns
IOCS16- hold time from ATSCLK falling edge	T310	10		10		ns
0WS- setup time to ATSCLK rising edge	T311		16		16	ns
0WS- hold time from ATSCLK rising edge	T312	10		10		ns
IOCHRDY setup time to rising edge of ATSCLK	T313	18		18		ns

AT Bus Cycle Timing (Cont.)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
IOCHRDY hold time from rising edge of ATSCLK	T314	10		10		ns
DBAM(4:0) valid from ATSCLK falling edge	T315		20		18	ns
DBAM(4:0) hold time after COMMAND invalid	T316	40		40		ns
DLE Valid from falling edge of ATSCLK	T317		20		18	ns
DLE hold time after COMMAND invalid	T318		5		5	ns
ROMCS- active from 411CLK rising edge	T319	6	29	5	28	ns
ROMCS- inactive from 411CLK falling edge	T320	5	26	4	24	ns
MEMCS16- set-up time to BALE falling edge	T321	20		20		ns
MEMCS16- hold time to BALE falling edge	T322	10		10		ns

4.4.4 DMA Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
HOLD valid from 411CLK rising edge	T401	5	24	4	19	ns
HOLD invalid from 411CLK rising edge	T402	5	24	4	19	ns
HLDA1 valid from HLDA valid	T403	5	20	4	15	ns
HLDA1 invalid from HOLD invalid	T404	5	20	4	15	ns
DBAM<4:0> valid from command valid	T405	7	24	6	22	ns
DBAM<4:0> invalid from command invalid	T406	7	24	6	22	ns
BNKSL<1:0> valid from command valid	T407	7	28	6	20	ns
BNKSL<1:0> invalid from command invalid	T408	7	28	6	20	ns
RASn-<1:0> valid from command valid	T409	6	22	5	20	ns
RASn-<1:0> invalid from command invalid	T410	6	22	5	20	ns
MA<10:8>, MAXD<7:0> valid from 411CLK rising edge	T411	6	22	5	20	ns
MA<10:8>, MAXD<7:0> invalid from 411CLK rising edge	T412	6	22	5	20	ns
CASn- valid from 411CLK rising edge	T413	6	22	5	20	ns
CASn- invalid from 411CLK rising edge	T414	6	22	5	20	ns

4.4.5 Cache Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
MATCH<0:1>- set up time to 411CLK falling edge	T501	12		9		ns
MATCH<0:1>- hold time to 411CLK falling edge	T502	7		5		ns
CRD<1:0>- low from 411CLK falling edge	T503	6	18	5	14	ns
CRD<1:0>- high from 411CLK falling edge	T504	5	17	4	13	ns
READY- low from MATCH<0:1>- delay	T505	6	20	5	15	ns
READY- high from 411CLK rising edge	T506	6	20	5	15	ns
SRAMA3/SRAMA2 valid from A3/A2 valid	T507	6	22	4	20	ns
CWE<1:0>- active from 411CLK falling edge	T508	6	20	5	18	ns
CWE<1:0>- active from 411CLK rising edge	T509	6	18	5	18	ns
CBS<3:0>- valid from BE<3:0>- valid	T510	5	20	4	18	ns
CBS<3:0>- invalid from 411CLK rising edge	T511	7	25	6	22	ns
TAOE low from 411CLK falling edge	T512	6	18	5	14	ns
TAOE high from 411CLK rising edge	T513	6	17	4	13	ns

Cache Cycle (Cont.)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
TA<25:15>- tri-stated from TAOE falling edge	T514	6	16	5	14	ns
TA<25:15>- active from TAOE rising edge	T515	6	16	5	14	ns
XA bus active from TAOE falling edge	T516	6	16	5	14	ns
XA bus tri-stated from TAOE rising edge	T517	5	17	4	13	ns
SRAMA3/SRAMA2 valid from 411CLK rising edge	T518	6	18	5	14	ns
CRD<1:0>- low from 411CLK rising edge	T519	6	18	5	14	ns
BRDY- low from 411CLK rising edge	T520	6	20	5	15	ns
BRDY- high from 411CLK rising edge	T521	6	20	5	15	ns
READY- low from 411CLK rising edge	T522	6	20	5	15	ns
READY- high from 411CLK rising edge	T523	6	20	5	15	ns
CWE<1:0>- active from 411CLK rising edge	T524	6	18	5	15	ns
TAGWE- active from 411CLK rising edge	T525	6	18	5	14	ns
TAGWE- inactive from 411CLK rising edge	T526	5	17	4	12	ns

Cache Cycle (Cont.)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
VALID- low from 411CLK rising edge	T527	6	18	5	14	ns
VALID- high from 411CLK rising edge	T528	7	20	6	14	ns
READY- low from 411CLK rising edge	T529	6	20	5	15	ns
TAOE low from 411CLK rising edge	T530	6	18	5	14	ns
MAA1 valid from 411CLK rising edge	T531	6	18	5	14	ns
MBA1 valid from 411CLK rising edge	T532	6	18	5	14	ns
KEN- low from 411CLK rising edge	T533	5	17	4	12	ns
KEN- high from 411CLK rising edge	T534	6	20	5	15	ns
MAA1 invalid from 411CLK falling edge	T535	6	18	5	14	ns
MBA1 invalid from 411CLK falling edge	T536	6	18	5	14	ns

4.4.6 DRAM Memory Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
DWE- active from 411CLK rising edge	T601	6	20	5	18	ns
DWE- inactive from 411CLK falling edge	T602	7	24	6	22	ns
RAS- inactive from 411CLK falling edge (page miss precharge)	T603	6	22	5	20	ns
RAS- active from 411CLK falling edge (page miss precharge)	T604	6	22	5	20	ns
CASBn- active from 411CLK falling edge	T605	5	16	4	10	ns
CASBn- inactive from 411CLK falling edge	T606	5	18	4	15	ns
MA<10:8>, MAXD<7:0> valid from 411CLK falling edge	T607	6	22	5	20	ns
MA<10:8>, MAXD<7:0> invalid from 411CLK falling edge	T608	6	22	5	20	ns
DLE valid from 411CLK rising edge	T609	6	20	5	18	ns
DLE invalid from 411CLK falling edge	T610	6	20	5	15	ns

DRAM Memory Cycle Timing (Cont.)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
WDLE valid from 411CLK rising edge	T613	7	25	6	22	ns
WDLE invalid from 411CLK rising edge	T614	6	22	5	20	ns
BNKSL<1:0> from 80486 address valid	T615	7	28	6	24	ns
MA<10:8>, MAXD<7:0> valid from CPU address valid	T618	6	22	5	20	ns
CASBn- active from 411CLK rising edge	T619	12	20	10	18	ns

4.4.7 AT Style Refresh Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
HOLD active from 411CLK rising edge	T701	5	24	4	19	ns
HOLD inactive from 411CLK rising edge	T702	5	24	4	19	ns
REF- active from ATSCLK rising edge	T703		25		22	ns
REF- inactive from ATSCLK rising edge	T704		25		22	ns
MEMR-, SMEMR- active from rising edge of ATSCLK	T705		25		22	ns
MEMR-, SMEMR- inactive from rising edge of ATSCLK	T706		25		22	ns
RAS0-, RAS2- active from 411CLK falling edge	T707	6	22	5	20	ns
RAS0-, RAS2- inactive from 411CLK falling edge	T708	6	22	5	20	ns
RAS1-, RAS3- Active from 411CLK rising edge	T709	6	22	5	20	ns
RAS1-, RAS3- inactive from 411CLK rising edge	T710	6	22	5	20	ns
XA<10:0> valid from rising edge of ATSCLK	T711		25		22	ns
XA<10:0> invalid from rising edge of ATSCLK	T712		25		22	ns

4.4.7 AT Style Refresh Cycle Timing (Continued)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
MA<10:8>, MAXD<7:0> valid from 411CLK rising edge	T713	6	22	5	20	ns
MA<10:8>, MAXD<7:0> invalid from 411CLK rising edge	T713	6	22	5	20	ns

4.4.8 Hidden, Burst Mode Refresh Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
RAS<0,2>- low from 411CLK rising edge	T801	6	22	5	20	ns
RAS<0,2>- high from 411CLK rising edge	T802	6	22	5	20	ns
RAS<1,3> low from 411CLK falling edge	T803	6	22	5	20	ns
RAS<1,3> low from 411CLK falling edge	T804	6	22	5	20	ns