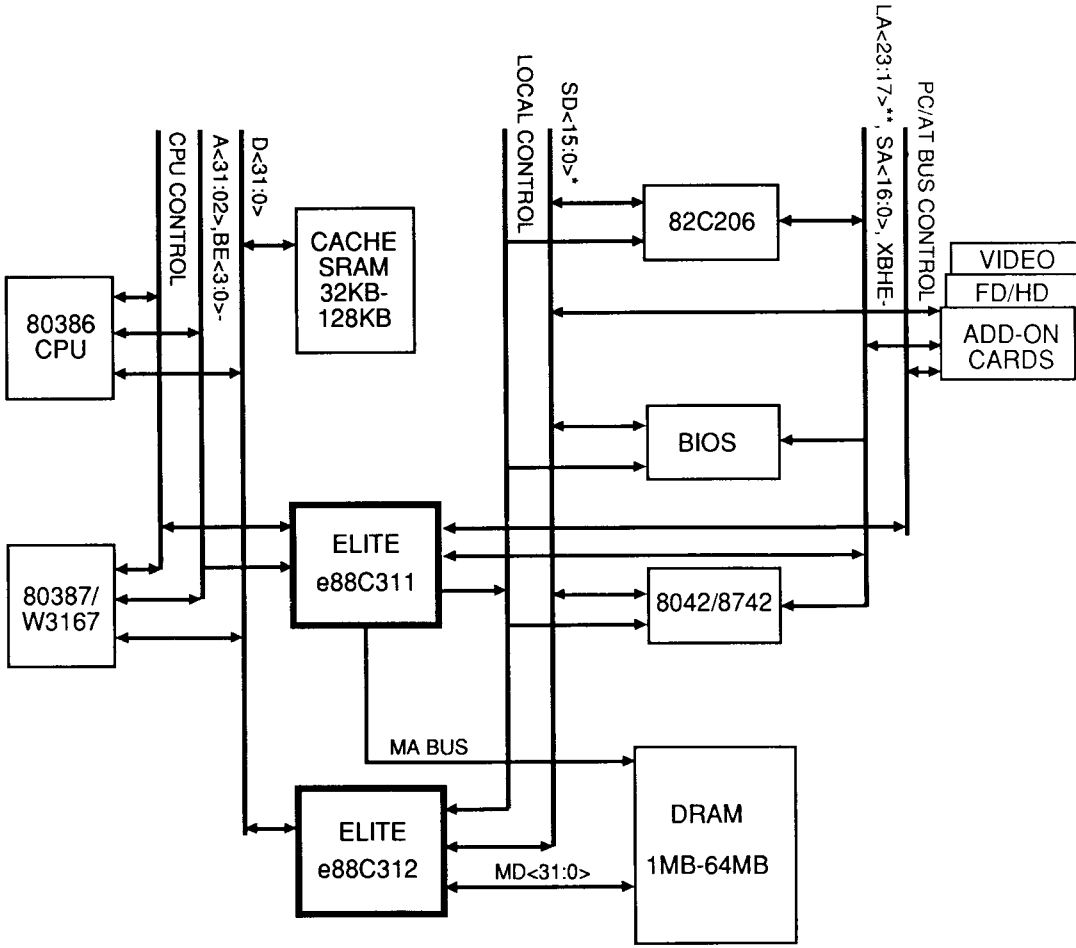
ELITE 80386 PC/AT EAGLE CHIPSET
e88C311 & e88C312

An Overview

The Eagle 386 AT chip set is designed for high performance PC-ATs with 80386DX running at 20/25/33 MHz. Major features of the Eagle chip set include:

- 100% IBM PC-AT compatible 386DX chip set
- Supports 20, 25 and 33 MHz 386DX based PC-ATs
- Fully integrated cache controller along with DRAM controller improves overall system performance
  - Supports direct mapped and two way set-associative cache organizations
  - Provides buffered write-through DRAM updating scheme to minimize write cycle penalty
  - Supports 32KB, 64 KB and 128 KB of data cache
  - Provides four blocks of non-cacheable regions ranging from 4KB to 4MB to offer software compatibility
  - Provides cache freeze facility for frequently used program codes
  - ZERO wait state for both pipelined/non-pipelined cache read hit access
- Highly optimized DRAM controller
  - Supports up to 64MB of system memory
  - Supports 256Kb, 1Mb and 4 Mb of DRAM configurations
  - Provides both Page and Page-interleaved operations
  - Supports 256KB of shadow RAM with 16KB granularity
  - Provides hidden, burst and PC-AT style refresh modes
  - Provides sophisticated memory remapping scheme to maximize the usage of physical memory installed
  - ZERO wait state for both pipelined/non-pipelined cache miss/page hit operation
- Supports both 80387 and Weitek WTL3167 math coprocessors
- Provides both the Fast GATEA20 and Fast Reset for OS/2 optimization
- Provides programmable PC-AT bus clock to allow both synchronous and asynchronous operations



*XD<7:0> Share the same BUS as SD<7:0>
**XA<23:00> Share the same BUS as LA<23:17> and SA<16:00>

Figure 0-1. System Block Diagram

- Provides on-board chip selection logic for one parallel and two serial ports
- Provides on-board chip select logic for two software programmable I/O ports
- Requires less than 24 devices (including CPU, ROM, KBC) plus DRAMs/SRAMs for a complete cache based 386DX PC-ATs
- Supports both Cache/Cacheless PC-ATs with same design
- Provides 60 configuration registers to offer product differentiation and optimization

The Eagle 386DX AT chip set consists of the e88C311 and e88C312. Along with the commonly available Integrated Peripheral Controller, e.g., the 82C206, a high-performance, compact and cost-effective cache based 386DX PC-ATs can be implemented efficiently. This is achieved through a very high level of function integration and system partition. The Eagle chip set is designed to provide 100% IBM PC-AT compatibility while offering flexibility in addressing both the requirements of cache and non-cache based 386 PC-ATs. The Eagle chip set also provides system designers with sixty software programmable configuration registers in controlling the operation features of their designs.

e88C311 CPU/CACHE/DRAM Controller, an Introduction

The e88C311 generates and synchronizes all the control signals for buses and manages the interfaces of all functional blocks inside the chip, e.g., reset/shutdown logic, CPU/local memory/AT/Cache state machines, arbitration and refresh logic, DRAM controller, and the cache controller. The highly integrated cache controller with built-in TAG RAM supports both direct mapped or two way set-associative cache organization with data cache size ranging from 32KB, 64KB to 128KB. It implements a buffered write-through DRAM updating scheme and a Least Recently Used (LRU) replacement algorithm to improve the system performance.

By integrating the cache controller along with the DRAM controller, the e88C311 can further enhance system performance by time-sharing cache and DRAM cycles. For example, when a read cycle starts, cache access and DRAM access are performed in parallel and DRAM cycle can continue and/or be terminated depending on the outcome of the cache hit/miss detection. In such case, the time penalty associated with non-integrated cache/DRAM architecture is reduced because the e88C311 does not have to wait for the hit/miss signal from the TAG RAM directory to start the DRAM operation. The e88C311 thus can achieve ZERO wait state operation, for both pipelined and non-pipelined modes, during a cache hit access.

To further enhance system performance, the e88C311 provides an optimized page-interleaved DRAM operation. A ZERO wait state DRAM access can still be obtained during a page hit cycle following a cache read miss in a pipelined operation. In addition, the refresh scheme of the e88C311 is designed in such a way that when the Hidden/Burst mode option is enabled, the CPU can keep operating out of cache while the DRAM refresh logic is servicing the refresh requests. This would result in further improvement of the system performance.

The e88C311 is available in 184 Pin PQFP (Plastic Quad Flat Package) with the more preferable 25 mil lead pitch to allow higher reliability during surface mount manufacturing process.

e88C312 DATA Controller, an Introduction

The e88C312 contains the control logic to manage the interface between the CPU data bus, local/main memory data bus, local system bus, PC-AT bus, ROM, and on-board peripherals. It also implements the byte alignment and byte swapping logics for data transfer where source and target are of different bus widths. The parity logic embedded in the e88C312 generates and writes the parity bits into the DRAM array during main memory write cycles. It also latches the data parity for each byte during memory read cycle. The parity handler and associated NMI logic is designed to assure data integrity throughout the system operation. The built-in coprocessor detection/interface circuitry supports both Intel 80387 and Weitek WTL3167 math coprocessors without additional discrete logic. The e88C312 also provides on-board chip selects for one parallel port, two serial ports and two software programmable I/O ports.

The e88C312 is available in 160 Pin PQFP (Plastic Quad Flat Package) with 25 mil lead pitch to allow higher reliability during surface mount manufacturing process.

e88C311 CPU/CACHE/DRAM CONTROLLER

An Overview

The e88C311 incorporates following function blocks:

1) Reset and shutdown logic
2) Clock generation and selection logic
3) Port B register and NMI generation logic
4) Action mode codes generation
5) CPU state machine, local memory state machines, cache state machines, and AT bus state machine
6) Bus arbitration
7) Coprocessor support
8) Cache controller
9) Page interleaved DRAM controller
10) Configuration registers

By utilizing the e88C311 together with the e88C312, the system designer can incorporate the most powerful cache based system while maintaining 100% compatibility with the IBM PC-AT architecture. In addition, the sixty (60) configuration registers provide OEMs with vast opportunities to offer product differentiation by fine tuning the system parameters.

1. e88C311 FUNCTIONAL DESCRIPTION

1.1 Reset and Shutdown Logic

The e88C311 takes RESET1- and RESET2- inputs and generates the signals RESET3, RESET4 and RST387 that trigger both warm and cold reset. RESET1- is the Power Good signal and originates at the power supply. When RESET1- is active, the e88C311 will assert RESET3, RESET4 and RST387 initiating a cold reset of the complete system. If RESET2- is asserted by the keyboard controller (8042 or 8742) a system warm reset is generated, the e88C311 asserts RESET3 to reset the CPU. RESET3 is also asserted by the e88C311 when a shutdown bus cycle is detected. Additionally, a fast reset option is provided in the e88C311 to generate a warm reset without the long delay normally associated with the keyboard controller. This is done by writing bit 5 of configuration register 12h.

Both RESET3 and RESET4 should last for at least 80CLK2 cycles. The HIGH to LOW transition of RESET3 and RESET4 signal must be synchronous with CLK2 input signal to the 80386. This guarantees that the phase of the internal clock of the e88C311 state machine is the same as the phase of the internal clock of the 80386.

RST387 is the coprocessor reset signal. RST387 is activated by RESET3 or an I/O write operation to port F1. The High to Low transition of RST387 must meet the set-up and hold time requirement of the 80387. RST387 is held active for at least 80 CLK2 cycles and the 80386 will not receive a READY- signal from the coprocessor until at least 50 CLK2 periods after RST387 goes inactive.

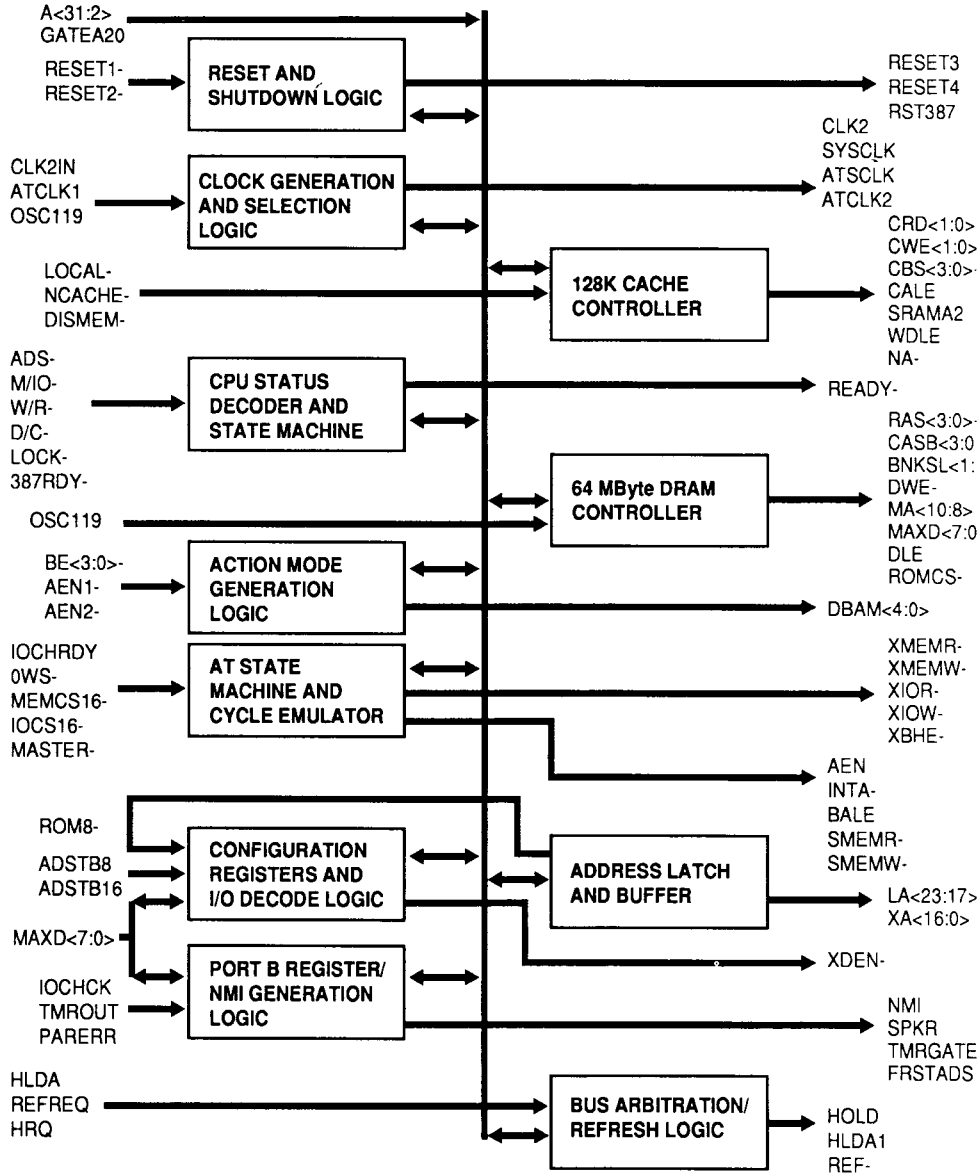


Figure 1-1. e88C311 Block Diagram

1.2 Clock Generation and Selection Logic

The e88C311 receives three clock inputs: CLK2IN, ATCLK1 and OSC119. It generates various clock signals to drive the 80386, the coprocessor, DRAM/Cache/AT state machines and the AT bus system. CLK2IN is derived from a crystal oscillator running at twice the rated frequency of the 80386, e.g., 66 MHZ for a 33 MHZ 80386 system. ATCLK1 is derived from another TTL crystal oscillator running at twice the frequency of the AT bus clock. OSC119 is a 1.19 MHZ clock generated by the 88C312 to control page mode RAS- time out in the DRAM controller.

The e88C311 generates four clock output signals: CLK2, SYSCLK, ATCLK2 and ATSCLK. The processor clock CLK2 drives the CLK2 inputs of the 80386 and the coprocessor. It is also used to drive e88C311 internal DRAM/Cache state machines. The SYSCLK signal is derived by dividing the CLK2 signal in half and is in phase with the internal state of the 80386. ATCLK2 is the AT bus state machine clock. ATSCLK is always ATCLK2/2 and is used to drive the AT bus clock.

Under normal condition, CLK2 is derived from CLKIN2 to allow the 80386 to operate at the maximum speed. ATCLK2 can be either a sub-division of CLK2IN or can be derived from ATCLK1 input. ATCLK1 may be selected as CLK2 source to slow down code execution.

By setting bits <7:6> of configuration register 11h and bit 7 of configuration register 12h, the ATCLK2 frequency can be programmed to be ATCLK1, CLK2IN/3, CLK2IN/4 or CLK2IN/5. The CLK2 signal can be programmed to run at the same frequency as CLK2IN or ATCLK1.

1.3 Port B Register and NMI generation logic

The e88C311 provides access to the Port B defined for PC/AT system level function control. The port can be accessed through any odd I/O port address between 61h and 6Fh. Table 1 shows the register definition:

Table 1-1 Port B Register Definition

BITs	READ/WRITE	DEFINITION	
7	READ ONLY	PCK	Memory Parity Check
6	READ ONLY	IO CH CK	IO Channel Check
5	READ ONLY	OUT 2	Timer 2 (8254) Out
4	READ ONLY	REF DET	Refresh Detect
3	READ/WRITE	ENA IO CK–	Enable IO Channel Check
2	READ/WRITE	ENA RAM PCK–	Enable RAM Parity Check
1	READ/WRITE	SPKR DATA	Speaker Data
0	READ/WRITE	T2GATE SPK	Timer 2 Gate Speaker

The master enable for NMI (non-maskable interrupt) is programmed through bit 7 of system I/O port 70h inside the e88C311. If this bit is set to 1, NMI generation is disabled and if set to 0, it is enabled.

After bit 7 of system I/O port 70h is set to 0 and the corresponding NMIs are enabled in Port B, a non-maskable interrupt is generated to the CPU and the source of the NMI is latched in Port B. Bits <7:6> indicate a memory parity error (PCK) or an IO Channel Check error (IOCHCK). The e88C311 also generates NMI due to a cache access error if the tag field and valid field of the two tag directories both match the incoming addresses.

1.4 Action Mode Codes Generation

This logic performs Data Buffer Action Mode (DBAM) codes generation for CPU accesses to devices on the CPU(D) bus, system (SD) bus, or memory(MD) bus. The AT bus conversions are performed for 16-, and 8-bit read or write operations. 32-bit transfers to and from the CPU are broken into several 16- or 8- bit AT bus cycles. The e88C311 generates five bits of Data Buffer Action Mode codes (DBAM<4:0>) to the e88C312. These bits control the buffers in the e88C312 for byte alignment, direction control and data conversion between the D, MD and SD data buses. Refer to the e88C312 technical specification for detailed definitions regarding Action Mode codes. DBAM codes are also used by e88C312 to decode Chip Select (CS-) signals for on-board I/O ports.

1.5 CPU State Machine, Local Memory State Machines, Cache State Machine, AT Bus State Machine

In the original IBM AT architecture, the CPU and AT bus run at the same speed. In order to maintain AT compatibility and to achieve the highest system performance; the CPU, the local DRAM and cache memory are driven by CLK2 while the AT bus is driven by ATCLK2. This allows the CPU and memories to operate at much higher frequencies, whereas the AT bus runs at an AT compatible 8 MHz speed. For synchronization, the e88C311 contains several state machines to control all the accesses initiated by the CPU, DMA/AT Bus Master or Refresh Request Timer.

The CPU state machine, DRAM and Cache state machines control all the accesses to the local bus (DRAM, Cache SRAM or coprocessor cycles). These state machines support only 32-bit data transfers between the CPU and the system memory; therefore no bus conversions are required.

The AT bus state machine is responsible for all non-local bus accesses and controls the AT bus for proper bus conversions.

1.5.1 CPU State Machine

In e88C311, the CPU state machine provides the interface to the 80386 processor. The CPU state machine monitors and decodes the bus status lines, ADS-, W/R-, M/IO-, D/C- and establishes the type of bus cycle to be performed. The CPU state machine begins its cycle upon assertion of ADS- and terminates the cycle upon generation of READY- at completion of the access.

For each new CPU cycle, the CPU state machine generates an internal signal CYCSTART (cycle start). It is sent to other state machines to indicate the beginning of a CPU cycle. For a non-pipelined cycle, CYCSTART is generated after ADS- is asserted. In contrast, for a pipelined cycle, CYCSTART is generated when both ADS- and READY- of the previous CPU cycle are detected.

Another internal signal LMEM32- is generated by the memory controller module to distinguish a local memory access (DRAM or SRAM) from a non-local memory access. After generation of CYCSTART, the CPU state machine samples the LMEM32- signal. If LMEM32- is active, it is a local memory cycle and control passes to the local DRAM and Cache state machines. DRAM or cache state machine generates the READY- to terminate the CPU cycle. However, if LMEM32- is inactive, the control is passed to the AT state machine. The CPU state machine then waits for the generation of the READY- signal from the AT state machine to terminate the cycle.

1.5.2 Local Memory State Machines

The DRAM array can be accessed by three different sources: CPU memory cycles, DMA/MASTER to local DRAMs, and refresh requests from the 82C206 timer output. These different accesses are controlled by three different state machines in the e88C311 DRAM module.

The e88C311 DRAM controller can support one, two, three, or four banks of local DRAMs. Each RAS- line drives one DRAM bank, and each CASB- line drives one byte of memory data. External demultiplexers (74F139s) combine CASB<3:0>- and BNKSL<1:0> lines to generate byte select signals for each memory bank. The DRAM row and column addresses are output on the MA<10:8>, MAXD<7:0> address pins.

When a memory location is decoded to be within the local DRAM range (LMEM32- active) and a cache miss/or a write hit cycle is detected, the CPU and Cache state machines pass control to the local DRAM state machine. The local DRAM state machine generates RAS<3:0>-, CASB<3:0>-, BNKSL<1:0>, DWE-, and row/column address signals. The DRAM state machine also generates CWE<1:0>- to update the data cache during the cache read miss cycle. During a read miss, in the 128KB cache option, the local DRAM state machine initiates two DRAM accesses with inverted and non-inverted A2 address for each cycle respectively.

The e88C311 provides configuration registers to store memory system information for page/page interleave mode, DRAM wait states RAS- time-out period option, and shadow DRAM. For a "page hit" cycle, RAS- stays asserted after the previous accesses. For a "page miss" or RAS- time-out cycles, DRAM cycle starts by first de-asserting the RAS- corresponding to the accessed bank. The local DRAM state machine also inserts programmed wait states into the DRAM cycle.

Local DRAMs can also be accessed by a DMA controller or an AT bus master. DMA/MASTER local DRAM access is initiated by asserting HLDA1. The XMEMR- and XMEMW- determine if it is a read or write memory access per DMA/Master bus cycle.

Local memory refreshes are controlled by a separate refresh state machine. During a refresh cycle, all four RAS- lines are asserted low for the DRAMs to be refreshed. RAS0- and RAS2- are activated first; followed by RAS1- and RAS3- with a CLK2 cycle delay. This staggering of RAS- signals reduces the system noise.

1.5.3 Cache State Machine

The main function of the cache state machine in the e88C311 is to manage the internal tag directories and external cache memory through various CPU and DMA/Bus Master cycles. Apart from the difference between I/O, Halt, Shutdown, Interrupt Acknowledge cycles and memory read/write cycles, the e88C311 can be programmed to run in pipelined or non-pipelined mode. With the non-pipelined mode, it is also possible to run with zero or one wait state. For data coherency between the data SRAM and main memory, the cache state machine has to monitor the system bus used by the DMA controller or AT Bus Master. During a DMA/MASTER write hit cycle, when the other master overwrites DRAM contents of which the SRAM also has a copy, the cache state machine has to invalidate the data in the cache memory.

In the non-pipeline, zero wait states mode, and without any DMA/MASTER cycles running concurrently, a CPU cache read hit cycle completes the access in two T states. The cache state machine generates the READY- signal back to CPU a quarter way into the second T state to terminate the cycle. For direct mapped cache, one of the CRD- signals is activated from the middle of T1 until the end of T2. In the two way set associate mode, the CRD- is not generated until a quarter way into T2.

For non-pipeline mode and one wait state, or pipeline mode, a CPU cache read hit cycle takes three T states to complete the access. The cache state machine generates a READY- signal to the CPU at the beginning of the third T state. In the pipeline mode, the ADS- for the next cycle overlaps with the READY- of the current cycle.

For CPU memory cycles that are not cache read hits, the cache state machine passes control over to the DRAM or the AT state machine. This occurs at the middle of the second T state after ADS- is active. One of the state machines generates the READY- signal to the CPU and terminate the cycle. For the DRAM state machine, the number of T states between ADS- and READY- depends on whether RAS- is active or inactive, page hit or miss, and the number of DRAM wait states programmed. Writing to cache SRAM is controlled by the cache state machine for cache write hit cycles. For read misses or cache line fill, the DRAM state machine controls the write operation to cache SRAM. In addition, during read miss cycles in the 128 KB cache mode, the DRAM state machine activates two sub-cycles to read in the DRAM contents and write back into the data cache.

DMA/MASTER write cycles, with or without Bus Snooping, require three T states to search through the cache directories and invalidate the tag entry if needed. The cache state machine will read the tag directories in the first T state, compare the contents with the DMA/MASTER address inputs in the second T state, and invalidate the tag entry for DMA/MASTER write hit access in the third T state. In the Bus Snooping mode, the access to the internal cache directories has to be shared between the CPU and DMA/MASTER. The cache state machine manages the tag accesses from the CPU cycle and DMA/MASTER write cycle simultaneously with negligible interference to CPU cache read hit cycles.

1.5.4 AT Bus State Machine

The AT bus state machine is invoked when CYCSTART is generated and LMEM32- is inactive. The AT state machine is driven by ATCLK2, which runs twice the frequency of the AT bus clock (ATSCLK). The AT bus cycle is initiated by asserting the BALE signal decoded from the CPU status signals and is terminated by asserting READY-. The e88C311 supports 8-, 16-, or 32-bit transfers between the processor and 8- or 16- memory or I/O devices located on the AT bus. MCS16- and IOCS16- are sampled during the AT cycle to determine the bus size conversion and necessary byte alignment. For the AT memory cycle, MCS16- is sampled at the falling edge of BALE. For the AT I/O cycle, IOCS16- is sampled one-half of the ATSCLK after the falling edge of BALE to accommodate some slower I/O cards. If none of these 16-bit status signals are asserted, 8-bit transfers are assumed and the request is converted into 1, 2, 3, or 4 I/O channel cycles based on BE<3:0>-.

After BALE goes inactive, the AT state machine enters the command cycle. The command signals for the memory or I/O access remain active until the programmed number of wait states are executed. Bits <3:0> of register 11 control the I/O channel wait state generation for 8- and 16-bit accesses. Bits <5:4> provide the option to ensure enough recovery time for back to back I/O commands. The second I/O command is activated only after the programmed recovery time is satisfied.

After the programmed number of wait states are executed, IOCHRDY is sampled. If IOCHRDY is active (ready), the command becomes inactive after the next ATSCLK cycle. If IOCHRDY is not active (not ready), the commands are extended for an additional cycle (i.e., one ATSCLK) and IOCHRDY is sampled again. This process continues until IOCHRDY becomes active.

The AT bus cycle can also be terminated earlier by detecting an active 0WS- signal. This signal is sampled one ATSCLK after BALE becomes inactive.

1.6 Bus Arbitration

The e88C311 provides bus arbitration between CPU, DMA, AT bus Master and AT style refresh logic (Burst and Hidden refresh cycles do not initiate a HOLD signal to the CPU). HRQ, a level triggered signal from the 82C206, is active when a DMA or a Master is requesting a bus cycle. REFREQ, an edge triggered signal from the 82C206, initiates a DRAM refresh request from refresh interval timer. The e88C311 arbitrates between HRQ and REFREQ by sending a hold request (HOLD) to the CPU in a non-preemptive manner. The CPU responds to hold request (HOLD) by issuing HLDA to e88C311 and relinquishes the CPU bus. The e88C311 then issues HLDA1 or REF- depending on which device prevailed during arbitration. With the Bus Snoop feature enabled, the e88C311 issues HLDA1 without sending a hold request (HOLD) to the CPU.

During a normal DMA cycle (with the Bus Snooping feature disabled), the DMA controller has control of the bus until HRQ becomes inactive. With the Bus Snoop feature enabled, the e88C311 issues HLDA1 without sending a hold request (HOLD) to the CPU. The CPU access can then run concurrently with DMA/MASTER cycles. During AT style refresh cycle, the refresh logic has control of the bus until REF- goes inactive and will generate separate control signals for local DRAM as well as AT bus memory. For local DRAM refresh, the internal refresh counters provide DRAM refresh addresses onto MA<10:8>, MAXD<7:0> bus and all RAS- lines are activated. For AT bus memory refresh, refresh addresses are latched into the SA<10:0> bus and XMEMR- is asserted. Refer to section 1.9.2 for other types of refresh operations.

1.7 Coprocessor Support

Both 80387 and Weitek processors are supported by the e88C311. After power up, bits 3,2 of configuration register 4D indicate the presence of the 80387 or Weitek WTL 3167 coprocessor respectively.

During 80387 operations, the CPU generates one or more I/O cycles to addresses 800000F8h through 800000FCh. The e88C311 executes a local (non-AT) cycle and no DRAM or AT commands will be activated. When present, the 80387 generates 387RDY- at the end of the coprocessor cycle. e88C311 samples 387RDY- signal and returns a ready signal READY- to the CPU. In the absence of 80387, the e88C311 will generate a ready signal READY- to terminate the cycle.

The Weitek coprocessor will respond to memory access of address C0000000h through C1FFFFFFh. When the Weitek coprocessor is present, the coprocessor generates ready signal READY- to the CPU without any involvement from the e88C311. When the Weitek coprocessor is not present, the e88C311 generates READY- to the CPU and terminate the cycle.

1.8 Cache Controller

The memory system in a PC/AT design is usually implemented with inexpensive, slow dynamic DRAMs. A cache memory is a small, high speed unit that resides between the CPU and the main memory. It increases the effective speed of the main memory by providing access to a copy of the most frequently used code or data from the main memory. When the CPU tries to read data from main memory, the high speed cache memory will respond first if the data resides in the cache memory (hit cycle). Otherwise (miss cycle), a normal main memory cycle will take place.

A cache system can further enhance system performance by time-sharing cache and DRAM cycles. During write cycles, the data is held in a temporary buffer inside the e88C312. Before the write cycle to main memory is completed, the CPU can access cache memory during a read hit cycle . However, if another read miss cycle or write cycle is performed, it has to wait until the previous write cycle is completed. While DRAMs are being refreshed in hidden refresh mode, the CPU can also access cache memory at the same time if it is a read hit cycle.

The e88C311 integrates the cache controller and the DRAM controller into a single chip. When a read cycle starts, cache access and DRAM access are performed in parallel. In the case of a cache hit, DRAM commands to main memory are terminated and cache memory provides the data to the CPU. In the case of a miss, a DRAM cycle will be completed. The integrated cache controller reduces the time penalty during a miss cycle because it does not have to wait for a HIT/MISS signal from the external cache tag RAM to start a DRAM operation.

To further enhance system performance, the e88C311 provides the user with a page-interleaved DRAM access option. A zero wait state (pipelined mode) or a one wait state (non-pipelined mode) DRAM access can be achieved during a page hit cycle, even if it is a cache read miss.

1.8.1 Cache Performance

A cache reduces the average memory access time if it holds the most frequently requested code and data. The effectiveness of the cache is determined by the data cache size, line size, cache mapping scheme, cache replacement algorithm, and type of program execution.

The cache miss rate decreases with increasing data cache size. The gain is marginal, however, if the cache is 64KB or larger. The cache controller moves data from main memory to the cache during a miss cycle. A *block* is the basic unit of memory in that process. A typical block size (line size) is 4, 8, or 16 bytes. A large line size increases the hit rate if the CPU is accessing consecutive addresses or repeating a short loop. On the other hand, a large line size takes longer to transfer and increases the likelihood of unneeded data being placed in the cache.

In a direct mapped cache, each block can hold only one set of memory locations. The index field addresses are used to select one entry in the tag directory. The tag field addresses are compared with the contents of the tag directory to determine whether the access is a hit or a miss. Unlike the set associate cache, the direct mapped cache restricts the possible contents of the cache. More than one location with the same index cannot reside in the cache simultaneously. The result is a lower hit rate and increased data transfers from main memory to cache memory. However, it is easier to implement in hardware because only one comparator is required to determine whether the access is a hit or a miss.

In a set associative cache (2-way or 4-way), the index field addresses select multiple entries. In the case of a 2-way associative cache, there are two locations for each index field. This increases the likelihood of caching two accessed locations at the same time. Since two comparators are required to determine if the requested data resides in that cache, the process requires more hardware and extra time delay.

The Least Recently Used (LRU) algorithm is the most popular among set-associative cache designs. Upon miss access, the LRU algorithm selects for replacement, the item that has been least recently used by the CPU.

1.8.2 e88C311 Cache Organization

The e88C311 supports 32KB/64KB/128KB data cache options. It can also be programmed as a two way set associative or as a direct mapped cache. For a given cache size, the two way set associative scheme will result in a higher hit rate as compared to a direct mapped cache. The gain becomes marginal, however, as cache size increases. Since less time delay is needed to detect a hit/miss access with direct mapped cache, it is the most viable organization for 33MHz systems.

Table 1-2 illustrates two way associative set as well as direct mapped cache organization for the 32KB, 64KB and 128KB cache. It lists the physical address assignments of line select, set select, and tag field for all cache options supported by the e88C311.

Table 1-2 Direct Mapped & Two Way Set-Associative Cache Organization for 32KB, 64KB, and 128 KB Data Cache

	CACHE DATA SIZE	32KB	64KB	128KB
2 WAY	Line Size (Byte per Line)	4	4	8
	Set Size (Line per Set)	8	16	16
	Set #	512	512	512
	Line Select	A2–A4	A2–A5	A3–A6
	Set Select	A5–A13	A6–A14	A7–A15
	Tag Field	A14–A25	A15–A25	A16–A25
DIRECT MAPPED	Line Size (Byte per Line)	4	4	8
	Size (Line per Set)	8	16	16
	Set #	1024	1024	1024
	Line Select	A2–A4	A2–A5	A3–A6
	Set Select	A5–A14	A6–A15	A7–A16
	Tag Field	A15–A25	A16–A25	A17–A25

1.8.3 General Operations

In this section the following operations are illustrated in detail:

Read hit cycle
Read miss cycle
Write cycle
DMA/Master cycle
Bus snooping
128KB cache cycle

1.8.3.1 Read Hit Cycle

When the CPU starts a read cycle, the block (index) field of physical addresses selects a line from the cache directory. The tag bits and the valid bit stored in that location are compared with the CPU address inputs. A hit cycle is indicated when the tag field matches and the corresponding valid bit for the decoded sub-line is set. The e88C311 generates CRD<1:0>- to transfer data from cache memory to the CPU. A *ready* signal (READY-) is sent to the CPU to terminate the cycle.

After power up, the tag directory is automatically flushed within 2048 CLK2 cycles. (During this time, the e88C311 forces all local memory accesses to be DRAM cycles.) All valid bits in the cache directory should be invalidated. The hit rate starts with zero and the cache data RAM is empty. As the program is executed, the cache directory is filled and the hit rate increased. This mechanism avoids a cache error condition that occurs when the current address matches the tag field of both sets and both sets are valid. The tag directory can also be flushed via the software program by writing to index register 12 with bit 1 set to 1. If, due to an erroneous write operation to the tag RAM, a cache error occurs, the e88C311 allows the user to set up an interrupt through index register 64h. The tag RAM address that causes the cache error can be accessed through index register 64h and 65h.

1.8.3.2 Read Miss Cycle

In a read miss cycle, the DRAM memory provides the data to the CPU and write the same data to cache memory. The next time the same address is accessed, it will result in a hit cycle. In direct mapped cache, the cache controller will update the tag entry and corresponding cache memory data. In a two-way set associative cache, the set that has not been used recently (and therefore the least likely to be accessed) will be replaced.

1.8.3.3 Write Cycle

In a cache miss access during a write cycle, no cache write and tag updates are performed. The CPU writes the data to the DRAM array without any interaction with cache memory.

In the case of a hit access during a write cycle, CPU data should be written to cache memory as well as to the DRAM array. This will ensure that cache memory maintains the same copy of data or code as the main memory so that no "stale data" problem occurs. Since a SRAM write is much faster than a DRAM write, additional wait states will be needed before the CPU data is copied into DRAM. In order to enhance system performance, the e88C311 incorporates a "post write" scheme. During the write operation (hit or miss), the e88C311 will return a ready signal (READY-) to the CPU and a write data latch enable (WDLE) signal to e88C312. The data is latched into a write buffer inside the e88C312 during the write operation, while the CPU is released to begin another cycle before the current write cycle is completed.

If the next cycle does not require DRAM accesses (cache hit, AT, I/O cycles), the write cycle is running an equivalent of a zero wait state to the CPU. However, if the following cycle requires another DRAM access while the DRAM is busy with the first write cycle, additional wait states will be asserted until the DRAM has completed its previous cycle.

1.8.3.4 DMA/MASTER Cycle

In an AT system, bus masters other than the CPU can access the main memory and alter its contents. When a cache hit access occurs within a master write cycle, data coherence between DRAM and cache memory must be maintained. The e88C311 will invalidate the cache for that tag location. Subsequent CPU memory access to the same memory location will be a cache miss until the cache is re-filled with new data. For local memory read cycles initiated by another master or DMA controller, only local DRAM accesses will be activated. For this reason, only local DRAM accesses are needed for DMA/MASTER write miss cycles.

1.8.3.5 Bus Snooping

During DMA Master write cycles, the e88C311 monitors the system address bus (XA). If another master writes into the main memory, the cache controller latches the system addresses and compares them with the current tag directory contents. If they match up (snoop hit), the cache entry is invalidated in the cache directory. The snoop address look-up and invalidation of the tag directory is time multiplexed with 80386 CPU access. The result is that all snoops are monitored and serviced without slowing down the CPU. Even local address and data buses are running zero wait states.

If bit 4 of index register 12 is set to zero, the snoop feature is disabled. Every DMA Master cycle will put the CPU on hold when the tag directory is searched to determine whether a cache write hit access has occurred. Cache invalidation will take place if it is a cache hit.

1.8.3.6 128KB Cache Cycle

In the case of a 128KB cache option, there are 8 bytes for each subline and one valid bit is allocated to two double words. For read miss cycle, two double words must be moved into the cache memory before the corresponding valid bit is set. Two DRAM accesses have to be completed before the current cycle can be terminated. With a two double word move-in scheme, the e88C311 can support a 128KB data cache with the same block size that supports a 64KB data caches RAM (Table 1).

During the first data move-in and DRAM access, SRAMA2 drives inverted A2 address to data caches RAM and A2 is inverted to drive the DRAM address output. During the second data move-in and DRAM access, SRAMA2 returns to non-inverted A2 state and that same A2 drives the DRAM address output. At the end of the second DRAM access (non-inverted A2 access), the requested data is available on the CPU data bus and the ready signal, READY- is generated to terminate the cycle.

1.8.4 Other Issues in Cache System Design

1.8.4.1 Non-Cacheable Regions

The e88C311 provides four non-cacheable regions to allow the user to set aside four blocks (size ranges from 4KB to 4MB) of address space as non-cacheable. The starting address of any non-cacheable region has to be on a boundary of that region's size. These regions can then be used as ROM area, memory-mapped I/O space, shared memory accessed by multiple masters, or any other memory areas that should not be cacheable. Once the region is defined as non-cacheable, the memory operation can be re-directed to either local DRAM access or AT memory access via the DSDRAM<3:0> bits in index register 50h to 59h. Non-cacheable features are defined through index registers 50h to 5Bh.

Non-cacheable regions can also be hardware programmed by decoding the corresponding address to control the NCACHE- input to the e88C311. All memory accesses within the address range will be local DRAM cycles. However, there is a minimum set-up time requirement so that the e88C311 will recognize this input for the current cycle to be non-cacheable.

1.8.4.2 Direct SRAM and Tag RAM access

For diagnostic purposes, the contents of data cache and TAG RAM can be directly accessed by the CPU. Direct SRAM access is defined in index register 60h. If this feature is enabled, then the cache data RAM will be treated as an extension of main memory with 32KB / 64 KB / 128Kb block size at starting address 040000h. The on-chip tag RAM directory can also be accessed through the 8-bit I/O peripheral data bus (XD). The I/O write cycle loads the desired values into the directory. These features make system debugging and initialization easier, i.e., line invalidation, tag RAM, or data caches RAM purge.

1.8.4.3 Cache Freeze

The e88C311 provides a feature to allow the user to freeze data cache contents. If a cache freeze is enabled through index register 60h, a read miss cycle cannot change the contents of data cache RAM nor can it update the tag directory. However, a cache write hit will write data into cache RAM. A DMA/Master cache write hit access will invalidate the corresponding tag RAM entry.

1.9 Page/Interleaved DRAM Controller

1.9.1 Page/Interleaved DRAM Operation

The e88C311 supports page mode (default) or page interleaved mode DRAM access providing higher performance over conventional DRAM access schemes. The access mode is programmed through bit-3 of index register 40h.

For normal DRAM access, both RAS- and CAS- have to be activated. The memory access time is determined by the Row Address Access time (Trac) rather than the much faster Column Address Access time (Tcac). Page mode DRAMs allow a number of locations within an area of memory (page) to be accessed without repeating the entire address. After providing the row address and asserting RAS-, the column address can be changed a number of times to access a series of locations. Each time a new column address is strobed by CAS-, RAS- must be kept asserted throughout the process. The number of cycles that can be performed is limited by the maximum length of the RAS- active pulse width. The effectiveness of the page-mode DRAM subsystem is determined by the page size and the locality of the program being executed. The page size can be increased by using higher density DRAMs.

The e88C311 also supports both 2-way and 4-way interleaved modes for DRAM access. For interleaved operation, the RAS- lines for each interleaved bank can be held active until the RAS- timeout period for that bank is reached. Therefore, it is possible to make access between the two (or four) banks by interleaving the CAS- precharge time of one bank with the CAS- active time of the other bank(s). As shown in the table below, the effective page size is increased when RAS- lines for memory banks are active.

Table 1-3 Effective Page Size for Page/Interleaved Mode DRAM

DRAM type	One bank	Two banks	Four banks
256Kb x N	2 KBytes	4 KBytes	8 KBytes
1Mb x N	4 KBytes	8 KBytes	16 KBytes
4Mb x N	8 KBytes	16 KBytes	32 KBytes

The address assignment for page, 2 Way, or 4-way interleaved modes for different memory types are shown in the following tables.

Table 1-4. Address Assignment for Page, 2-Way, 4-Way Interleaved Mode

Page (non-interleaved) Mode Operation		
	Row	Column
256Kb DRAMs	A<19:11>	A<10:2>
1Mb DRAMs	A<21:12>	A<11:2>
4Mb DRAMs	A<23:13>	A<12:2>

2-Way Interleaved Mode Operation			
	Row	Column	Even/Odd Bank
256Kb DRAMs	A<20:12>	A<10:2>	A11
1Mb DRAMs	A<22:13>	A<11:2>	A12
4Mb DRAMs	A<24:14>	A<12:2>	A13

4-Way Interleaved Mode Operation				
	Row	Column	Hi/Lo Bank Pair	Even/Odd Bank
256Kb DRAMs	A<21:13>	A<10:2>	A12	A11
1Mb DRAMs	A<23:14>	A<11:2>	A13	A12
4Mb DRAMs	A<25:15>	A<12:2>	A14	A13

1.9.2 Refresh Logic

The e88C311 provides the following refresh schemes:

- AT style refresh
- Hidden Refresh
- Burst mode refresh
- Slow refresh option

1.9.2.1 AT Refresh

This is the default refresh mode. In an AT style refresh scheme, the e88C311 arbitrates the bus after receiving the REFREQ from the refresh interval timer and generates HOLD request to the CPU. The CPU relinquishes the bus by issuing the HLDA. The e88C311 in turn will respond with the REF and starts the AT refresh cycle. The local DRAM will be refreshed with RAS- active for all banks at the same time the AT bus is refreshed.

1.9.2.2 Hidden Refresh

When the hidden refresh option is enabled, No HOLD signal will be generated to keep the CPU on hold and the refresh operation is transparent to the CPU access. The e88C311 monitors the AT bus as well as the local DRAM activities. If the AT bus is free while local DRAMs are busy, the AT bus refresh will be performed and the refresh of local DRAMs will be postponed. If cache option is enabled, the CPU will be able to operate cache memory independently. Assuming a cache read hit scenario, the refresh cycle can still proceed concurrently. The CPU will have to wait for its access to DRAM in other situations (e.g., cache read miss or write cycles). In the same way, DMA, and other AT bus accesses will be postponed until the current DRAM refresh cycle is completed.

1.9.2.3 Burst Refresh

The burst refresh allows multiple local DRAM refresh cycles to run once the burst mode is activated. The e88C311 refresh logic allows up to 8 refresh requests to accumulate. It will begin to service these requests when the local DRAM is not being accessed. Depending on the option set in the burst mode configuration register 48h, the e88C311 is able to run multiple refresh cycles until the number of remaining refresh requests in the burst mode counter equals to 0. However, if the DRAM controller becomes active while the burst mode refresh is running, the refresh logic will relinquish control upon completion of the current burst refresh cycle. It will then wait to perform another burst mode refresh whenever the local DRAM becomes available. The burst mode refresh must be hidden as the CPU can not access the DRAM while the current refresh cycle is running. In addition, all AT memory refresh requests must be serviced every time a refresh is requested as it cannot run in a burst fashion.

1.9.2.4 Slow Refresh

Slow refresh is an option provided for local DRAM refresh, not for an AT style refresh. Instead of generating refresh request at a rate of 256 per 4 ms, the Refresh control register (index 48H, bit 1 & 0) of the e88C311 can be set to allow slower refresh rate, e.g., 128 per 4 ms, 64 per 4 ms or 32 per 4 ms. The ability to run slow refresh option depends on the local DRAM used. This option is usually applicable when Low Power DRAMs are used for local memory.

The e88C311 refresh logic also provides a special mechanism to reduce system noise during simultaneous refreshing of each DRAM bank. RAS1- and RAS3- are delayed, after RAS0- and RAS2- are generated, to allow the refresh cycle for bank 1 and bank 3 to be performed immediately after refresh of bank 0 and

bank 2. This "stagger Refresh" scheme results in a reduction of system level noise when multi-bank local DRAMs are installed.

1.9.3 Shadow RAM

It is preferable to execute codes through the faster local memory (DRAM or Cache RAM) than through the slower EPROMs. System performance can be enhanced by having the executable BIOS codes reside in local memory, rather than in EPROMs. This is especially true for applications with extensive BIOS calls. The e88C311 provides a SHADOW RAM feature that, when enabled, allows the BIOS codes stored in the EPROMs to be executed (shadowed) from the local RAM area. However, these BIOS codes need to be transferred from EPROMs into local RAMs prior to use the SHADOW RAM feature. In the e88C311 implementation, this transfer is accomplished at system initialization by means of the following procedure:

1) Set register bits in configuration register 42h~45h for different memory access method
2) Copy ROM block to Shadow DRAM block
3) Set Corresponding bits in configuration 42~45 for blocks that are write protected.

The e88C311 can shadow any DRAM block with an address from 0C0000H to 0FFFFFH (i.e., the C, D, E and F block) in 16KByte granularity. In another word, 256KBytes of total DRAM at 16KByte per chunk can be selectively activated for shadowing. With the cache option turned on, the shadow RAM region is then cacheable after the BIOS or other codes are copied into local DRAM. Special attention needs to be made to prevent any write operation onto the shadowed area. This is accomplished by setting write protection bits in procedure 3.

1.9.4 Memory Remapping

The e88C311 memory remapping logic is able to remap physical memory locations between 640KB to 1MB (address 0A0000 to 0FFFFFH) in 64KByte chunks to the top of total system memory, provided that no portion of the 64KByte is shadowed. This feature is designed not to be limited by the amount of populated system DRAM. A 64KByte block is not remappable even if only one 16KByte chunk is shadowed.

Special consideration has been given to the remapping logic so that the e88C311 not only provides up to 384KBytes of remapping capability, but also assures all remapped memory to be contiguous on top of the total system memory.

The 384KByte reserved area at memory locations between 0A0000 and 0FFFFFH can be subdivided into A, B, C, D, E and F blocks, each with 64 KByte. The e88C311 supports the following remapping schemes:

1) A,B
2) A,B,D
3) A,B,D,E
4) A,B,D,E,C
5) A,B,D,E,C,F

While block A, B are remapped on top of the system memory, block "X" is remappable if no shadowed area exists within the block. Block "X" will be remapped by the e88C311 if and only if:

i) It is remappable and
ii) corresponding remap control bit in index register 46h is set to 1;
iii) Other block(s) to the left of block "X" is also remapped, based on the series of combination stated above.

Refer to Remapping Scheme Figure on the next page for detailed remap implementation.

1.9.5 EPROM Control Logic

The e88C311 provides control logic to generate the ROMCS- signal for a EPROM access. The AT bus state machine generates the READY- for this cycle. ROMCS- is connected to the EPROM chip enable (CE-) input. Since the e88C311 supports both 8 and 16 bits of ROM, it needs to generate appropriate action codes DBAM<4:0> indicating 8 bits or 16 bits ROM access. DMAM<4:0> are passed on to its companion chip, the e88C312 to transfer ROM data to the CPU data bus.

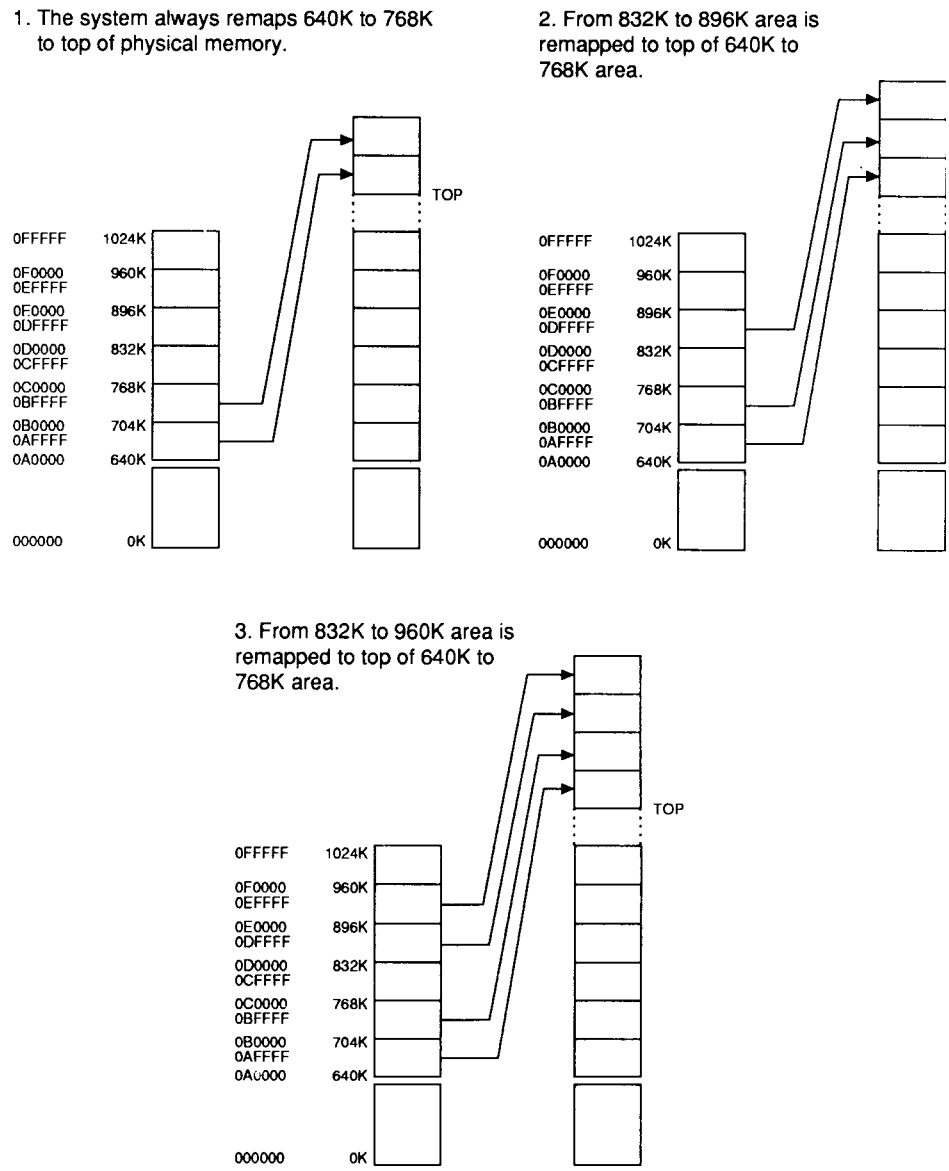
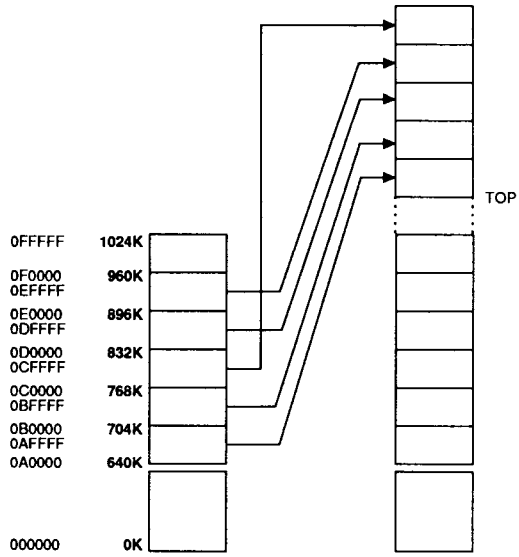


Figure 1-2. e88C311 Remapping Scheme

4. From 768K to 832K area is remapped to top of 832K to 960K area.



5. 960K to 1M area is mapped to top of all.

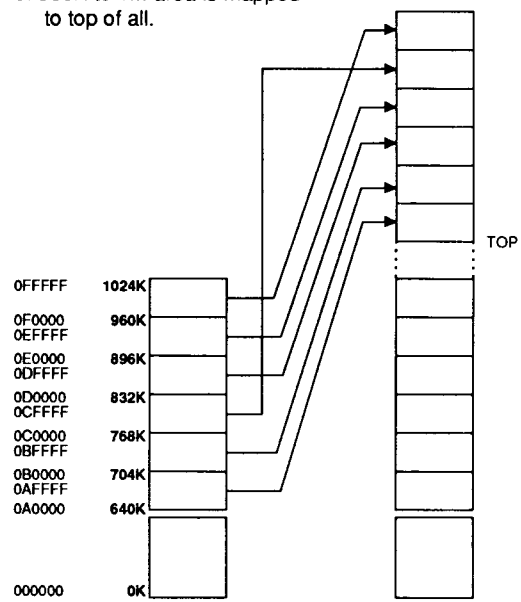


Figure 1-3. e88C311 Remapping Scheme (Continued)

1.9.6 OS/2 Optimization

The Eagle chip set provides two specific features that are further enhancements to the original IBM AT design:

.Fast Gate A20 (bit 6 of register 12h)
.Fast Reset3 (bit 5 of register 12h)

The OS/2 operating system developed by IBM and Microsoft has two operating mode. The OS/2 mode operates on CPU protected address region while DOS mode operates on CPU real address region. In the OS/2 mode, the operating system can make many function calls in DOS mode. The CPU needs to switch from Protected Address Mode to Real Address mode before the DOS call could be executed. A CPU reset (RESET3) is one way to make the mode change without executing a cold reset (Power Down/On). The address A20 must be switched low before CPU changes to Real Address mode. This is necessary to assure downward compatibility with the 8086.

Both functions in the original PC/AT design were handled through the keyboard controller (8042). The interface between the CPU and the keyboard controller is very slow. To switch from Protected to Real mode, the CPU needs to set A20 low and reset the CPU. For each operation, the CPU checks the keyboard controller ready status and issues commands to the keyboard controller. The e88C311 provides both functions through much faster I/O operations.

In the e88C311 implementation, Fast Gate A20 is a read/write bit controlling internal address bit A20. This bit is set to 1 during system reset allowing CPUA20 from the 80386 to pass onto address A20. Writing a 0 into this bit will set Gate A20 to 0 (inactive) and forces the address A20 to be low.

The Fast Reset3 read/write bit (bit 5 of register 12h) is set to 0 during system reset (cold reset). To generate Fast Reset3 during normal operation, the CPU only needs to execute two I/O write cycles for this bit to make 0 to 1 transition. The RESET3 pin is pulled high after a 2μs delay or until a HALT state is detected, whichever is earlier.

1.9.7 Memory Subsystem Design Specification

The following table describes the SRAM, DRAM speed required for certain performance level as related to the 386DX clock frequency.

Eagle e88C311

Table 1-5. 386DX/SRAM/DRAM Speed vs. Wait States*

386DX	SRAM	DRAM		Cache Read Hit**	
Clock Freq.	Addr. Access	t_{RAC}	t_{CAC}	NP	P
20 MHz	45 ns	100ns	~25ns	0 w.s.	0 w.s.
25 MHz	35 ns	80 ns	~20 ns	0 w.s.	0 w.s.
33 MHz	25 ns	60 ns	~15 ns	0 w.s.	0 w.s.

* Applicable to both direct map and Two Way set associative.

** First write is always zero wait state.

2. CONFIGURATION REGISTERS

The Eagle chip set provides the most flexible and extensive features in the PC industry. All features can be set up by programming the corresponding registers provided inside the chip set. There are 60 registers provided in the Eagle chip set. They are classified into 6 groups: the local/AT bus operation control, the local DRAM access control, the local DRAM shadow/remap control, the non-cache/non-local memory blocks control, the cache memory control, and the EMS mapper support.

The local/AT bus operation control registers are indexed from 10H to 19H. The local DRAM access control registers are indexed from 30H to 37H. The local DRAM shadow/remap control registers are indexed from 40H to 4DH. The non-cache/non-local memory blocks control registers are indexed from 50H to 5BH. The cache memory control registers are indexed from 60H to 65H. The EMS mapper support registers are indexed from 70H to 75H and also include 4 non-indexed I/O ports. Only register 4DH is in e88C312. All other registers are in e88C311.

The following two sections describe the definitions of all the registers and include examples on how to program them.

2.1 How To Program the Configuration Registers

All registers except the 4 non-indexed I/O ports can be accessed by the CPU through the system I/O ports, 22H and 23H. To access a register, first write the index number of the register being programmed on the system I/O port 22H then write/read data through I/O port 23H to/from this register. The Eagle chip set also provides a special feature: lock or unlock the chip set registers. The registers need to be unlocked before any write operation and normally are locked after all write operations are completed. This, however, is not necessary for read operations. In order to avoid an I/O timing problem, a delay is needed between the consecutive I/O access unless bits 5 & 4 of register 11H are properly programmed. Here is an example of an assembler program which programs the register 11H with value 04H:

```
        MOV     AL,10H    ; LOCK/UNLOCK REGISTER INDEX
        OUT     22H,AL    ; LATCH REGISTER INDEX
        JMP     $+2       ; GIVE I/O DEVICE RECOVERY TIME
        JMP     $+2       ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV     AL,0      ; REGISTER BIT 0= 0
        OUT     23H,AL    ; UNLOCK REGISTERS
        JMP     $+2       ; GIVE I/O DEVICE RECOVERY TIME
        JMP     $+2       ; GIVE MORE I/O DEVICE RECOVERY TIME
P0:     MOV     AL,11H    ; REGISTER INDEX 11H
        OUT     22H,AL    ; LATCH REGISTER INDEX
        JMP     $+2       ; GIVE I/O DEVICE RECOVERY TIME
        JMP     $+2       ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV     AL,04H    ; VALUE TO BE WRITTEN TO REGISTER
        OUT     23H,AL    ; WRITE TO REGISTERS
        JMP     $+2       ; GIVE I/O DEVICE RECOVERY TIME
P1:     JMP     $+2       ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV     AL,10H    ; LOCK/UNLOCK REGISTER INDEX
        OUT     22H,AL    ; LATCH REGISTER INDEX
        JMP     $+2       ; GIVE I/O DEVICE RECOVERY TIME
        JMP     $+2       ; GIVE MORE I/O DEVICE RECOVERY TIME
        MOV     AL,1      ; REGISTER BIT 0= 1
        OUT     23H,AL    ; LOCK REGISTERS
```

An assembler program example which reads the value of register 11H back is provided as follows.

```
P0:     MOV     AL,11H      ; REGISTER INDEX 11H
        OUT     22H,AL      ; LATCH REGISTER INDEX
        JMP     $+2         ; GIVE I/O DEVICE RECOVERY TIME
        JMP     $+2         ; GIVE MORE I/O DEVICE RECOVERY TIME
        IN      AL,23H      ; READ DATA FROM PORT 23H
        JMP     $+2         ; GIVE I/O DEVICE RECOVERY TIME
P1:     JMP     $+2         ; GIVE MORE I/O DEVICE RECOVERY TIME
```

If more registers are to be read/written, the steps between P0 and P1 mentioned above should be repeated with an individual index number and value.

2.2 The Definition of Configuration Registers

There are some notation conventions in this section. A default value of a register is the value in the register after the system is powered on. An "X" in a default state means unknown value. An "*" in front of a state value indicates the default value of the specific bits. The "R/W" item indicates "R" (read value), "W" (write value), or "R/W" (read/write value) for each individual bit.

This section includes a brief description of grouped registers and a detailed description of each register in that group.

2.2.1 Local/AT Bus Operation Control Registers

There are 10 registers in this group. The index registers 11H and 12H are used to select clocks and control the I/O operation while the registers from 13H through 19H are used to control the I/O ports. There are 2 programmable I/O, 2 serial I/O, and 1 parallel I/O chip selects in the Eagle chip set.

The following table briefly describes the function of the registers in this group:

Index	Functions
10H	To identify the chip set, and to lock or unlock registers.
11H	To set the AT bus clock, the I/O recovery time, and the wait states.
12H	To set the CPU clock, the bus snooping, and the CPU pipelined request; to do the fast reset, the fast gate A20, and the cache controller Tag RAM flush; and to show the status of the coprocessor.

13H	To control the programmable I/O chip select #0.
14H	To provide the programmable I/O #0 starting address high byte.
15H	To provide the programmable I/O #0 starting address low byte.
16H	To control the programmable I/O chip select #1.
17H	To provide the programmable I/O #1 starting address high byte.
18H	To provide the programmable I/O #1 starting address low byte.
19H	To enable or disable on board serial and parallel I/O ports.

The following tables describe in more detail the registers in this group:

Index	Default Value	Description
10H	[0011,0100]	This register provides the ID and revision number of the Eagle chip set when read. This registers in the Eagle chip set. The bit 0 of this register should be set to 0 before programming the registers and set to 1 when programming is done. This is to protect the registers from being overwritten accidentally.

Bits	R/W	State	Meaning
<7:0>	R		Chip set ID bits 7 - 0.
0	W	0	All configuration registers are readable and writable (unlocked).
		1	All configuration registers except registers 10H, 41H and some specific bits of registers 12H, 49H, and 64H are read only (locked).

Index	Default Value	Description
11H	[1000,0110]	This register is used to select the AT bus clock and to set the I/O recovery time and wait states.

Bits	R/W	State	Meaning
<7:6>	R/W	00	AT state machine clock frequency is the same as ATCLK1.
		01	AT state machine clock frequency is 1/3 of CPU clock frequency.
		*10	AT state machine clock frequency is 1/4 of CPU clock frequency.
		11	AT state machine clock frequency is 1/5 of CPU clock frequency.

Note: The CPU clock frequency is 2 times the CPU speed while the AT state machine clock frequency is 2 times the AT bus speed. A 25 MHZ system with 8 MHZ AT bus means the system has a 50 MHZ CPU clock frequency and a 16 MHZ AT state machine clock frequency. To select the AT state machine clock frequency at 1/3 of the CPU clock frequency, the AT state machine clock frequency will be 16.6 MHZ for a 25 MHZ system while the AT state machine clock frequency is 22 MHZ for a 33 MHZ system.

<5:4>	R/W	*00	1 AT bus clock for a back-to-back I/O cycle recovery time. The recovery time will be 125 ns if the AT bus cycle time is 125 ns (a 16 MHZ AT state machine clock frequency).
		01	2 AT bus clocks for back-to-back I/O cycle recovery time.
		10	3 AT bus clocks for back-to-back I/O cycle recovery time.
		11	4 AT bus clocks for back-to-back I/O cycle recovery time.
<3:2>	R/W	00	0 wait state for 16-bit AT bus operation.
		*01	1 wait state for 16-bit AT bus operation.
		10	2 wait states for 16-bit AT bus operation.
		11	3 wait states for 16-bit AT bus operation.
<1:0>	R/W	00	2 wait states for 8-bit AT bus operation.
		01	3 wait states for 8-bit AT bus operation.
		*10	4 wait states for 8-bit AT bus operation.
		11	5 wait states for 8-bit AT bus operation.

Index	Default Value	Description
12H	[0110,XX01]	This register is used to select the CPU clock and enable or disable the bus snooping and pipelined mode request. It also provides the fast gate A20, the fast reset, and the cache flush. The bits 6 & 5 of this register are writable even if this register is locked. The keyboard controller (8042/8742) has the same function as that of bits 5 and 6. However, reset CPU and activate gate A20 through these 2 bits is faster than through using 8042/8742. Bits 3 & 2 will be written once and

can be read only afterwards. These 2 bits (3 & 2) should be obtained from bits 3 & 2 of register 4DH before any memory is accessed during system power-up.

Bits	R/W	State	Meaning
7	R/W	*0	CPU clock source is CLK2IN.
		1	CPU clock source is ATCLK1.
6	R/W	0	Address bit A20 is forced to 0 no matter what the value of the CPUA20.
		*1	Address bit A20 is the same as CPU address bit CPUA20.
5	R/W		A transition from 0 to 1 will activate RESET3 which resets the 80386 CPU.
4	R/W	*0	The cache controller bus snooping is disabled. The CPU, DMA, and I/O channel bus master will share all of the bus through arbitration (hold request and hold acknowledge protocol).
		1	The cache controller's bus snooping function is enabled. The CPU can use local bus while the DMA or bus master is using the DRAM and AT buses.
3	R	0	INTEL 80387 is not installed.
		1	INTEL 80387 is installed.
2	R	0	Weitek 3167 is not installed.
		1	Weitek 3167 is installed.
1	R/W	*0	Cache controller's Tag RAM is kept the same or a flush operation has been done.
		1	All cache controller's Tag RAM is invalidated. It takes 2048 CLK2 cycles to flush the Tag RAM to zero. During the flush process, cache access is always a miss.
0	R/W	0	80386 runs pipelined mode if possible.
		*1	80386 always runs non-pipeline mode.

Index	Default Value	Description
13H	[0XXX,XXXX]	This register controls the attribute and mask bits of PIO chip select #0.
16H	[0XXX,XXXX]	This register controls the attribute and mask bits of PIO chip select #1.

Bits	R/W	State	Meaning
7	R/W	*0	Programmable I/O (PIO) ports are not used.
		1	PIO ports are used.
<6:5>	R/W	00	Reserved.
		01	Use these PIO ports only if I/O operation is to write to the location specified as in the bits 3-0 of this register and PIO ports starting address.
		10	Use these PIO ports only if I/O operation is read from the location specified as in the bits 3-0 of this register and PIO ports starting address.
		11	Use these PIO ports if I/O operation is write/read to/from the location specified as in the bits 3-0 of this register and PIO starting address.
4			Reserved.
3	R/W	0	The bit 3 of PIO ports address low byte is part of I/O ports address.
		1	The bit 3 of PIO ports address low byte is not part of I/O ports address.
2	R/W	0	The bit 2 of PIO ports address low byte is part of I/O ports address.
		1	The bit 2 of PIO ports address low byte is not part of I/O ports address.
1	R/W	0	The bit 1 of PIO ports address low byte is part of I/O ports address.
		1	The bit 1 of PIO ports address low byte is not part of I/O ports address.
0	R/W	0	The bit 0 of PIO ports address low byte is part of I/O ports address.
		1	The bit 0 of PIO ports address low byte is part of I/O ports address.

Index	Default Value	Description
14H	[XXXX,XXXX]	This register provides the I/O ports address high byte for PIO chip select #0 if the bit 7 of register 13H is 1.
17H	[XXXX,XXXX]	This register provides the I/O ports address high byte for PIO chip select #1 if the bit 7 of register 16H is 1.

Bits	R/W	State	Meaning
<7:0>	R/W		PIO chip select ports address bits 15 - 8.

Note: If PIO chip select ports address is above 3FFH, the lower 10 address bits 9 - 0 must not be the same as any IBM standard I/O ports address below 400H. This applies to both PIO chip selects.

Index	Default Value	Description
15H	[XXXX,XXXX]	This register provides the I/O ports address low byte for PIO chip select #0 if the bit 7 of register 13H is 1.
18H	[XXXX,XXXX]	This register provides the I/O ports address low byte for PIO chip select #1 if the bit 7 of register 16H is 1.

Bits	R/W	State	Meaning
<7:0>	R/W		PIO ports address bits 7 - 0.

Index	Default Value	Description
19H	[XXXX,X000]	This register is used to enable or disable the chip select generation for the on board serial I/O ports and parallel I/O ports.

Bits	R/W	State	Meaning
<7:3>			Reserved
2	R/W	*0	On Board Parallel I/O #1 (ports 378H - 37FH) is disabled.
		1	On Board Parallel I/O #1 (ports 378H - 37FH) is enabled.
1	R/W	*0	On board Serial I/O #2 (ports 2F8H - 2FFH) is disabled.
		1	On board Serial I/O #2 (ports 2F8H - 2FFH) is enabled.
0	R/W	*0	On board Serial I/O #1 (ports 3F8H - 3FFH) is disabled.
1			On board Serial I/O #1 (ports 3F8H - 3FFH) is enable.

2.2.2 Local DRAM Control Registers

The Eagle chip set supports 4 local memory banks which address up to 64M bytes. Each bank is controlled by a register pair, 30H and 31H, 32H and 33H, 34H and 35H, and 36H and 37H.

The following table briefly describes the function of the registers in this group:

Index	Functions
30H	To set the DRAM type, the wait states, and the RAS time-out for memory bank 0.
31H	To provide the starting address for memory bank 0.
32H	To set the DRAM type, the wait states, and the RAS time-out for memory bank 1.
33H	To provide the starting address for memory bank 1.
34H	To set the DRAM type, the wait states, and the RAS time-out for memory bank 2.
35H	To provide the starting address for memory bank 2.
36H	To set the DRAM type, the wait states, and the RAS time-out for memory bank 3.
37H	To provide the starting address for memory bank 3.

The following tables describe in more detail the registers in this group:

Index	Default Value	Description
30H	[0110,01XX]	This register is used to select the DRAM type depending on the DRAM installed on the system board and to set the DRAM access wait states and the RAS time-out limit for memory bank 0.
32H	[00XX,XXXX]	This register is used to select the DRAM type depending on the DRAM installed on the system board and to set the DRAM access wait states and the RAS time-out limit for memory bank 1.
34H	[00XX,XXXX]	This register is used to select the DRAM type depending on the DRAM installed on the system board and to set the DRAM access wait states and the RAS time-out limit for memory bank 2.

36H [00XX,XXXX] This register is used to select the DRAM type depending on the DRAM installed on the system board and to set the DRAM access wait states and the RAS time-out limit for memory bank 3.

Bits	R/W	State	Meaning
<7:6>	R/W	00	DRAM bank is disabled or DRAM is not installed.
		01	DRAM type of memory bank is 256Kx1 or 256Kx4.
		10	DRAM type of memory bank is 1Mx1 or 1Mx4.
		11	DRAM type of memory bank is 4Mx1 or 4Mx4.
<5:4>	R/W	00	DRAM access in pipelined mode when page hit has 0 wait state.
		01	DRAM access in pipelined mode when page hit has 1 wait state.
		10	DRAM access in pipelined mode when page hit has 2 wait states.
		11	Reserved.
<3:2>	R/W	00	DRAM RAS time-out checker is disabled.
		01	DRAM RAS time-out limit is 10 µs.
		10	DRAM RAS time-out limit is 100 µs.
		11	Reserved.
<1:0>			Reserved.

Index	Default Value	Description
31H	[XX00,0000]	This register provides the starting address for local memory bank 0.
33H	[XXXX,XXXX]	This register provides the starting address for local memory bank 1.
35H	[XXXX,XXXX]	This register provides the starting address for local memory bank 2.
37H	[XXXX,XXXX]	This register provides the starting address for local memory bank 3.

Note: The starting address of each bank depends on whether memory banks are in page-only or page-interleaved mode. The starting address for all banks which have the same DRAM type should be the same if memory access is set to

page-interleaved mode. The starting address for each bank which has a different DRAM type should be a multiple of 1M, 4M, or 16M depending on DRAM types of 256K, 1M, or 4M bits respectively.

Bits	R/W	State	Meaning
<7:6>			Reserved.
<5:0>	R/W		Local memory bank starting address bits 25 - 20.

2.2.3 Local DRAM Shadow/Remap Control Registers

There are 14 registers in this group. The index registers from 42H through 47H are used to establish shadow RAM or remap RAM in the ROM BIOS area. The registers 49H through 4DH give the local DRAM parity error information. The rest of the registers are used to provide a DRAM refresh feature, a bus master local memory access capability, and a local/AT ROM/RAM access scheme.

The following table briefly describes the functions of the registers in this group:

Index	Functions
40H	To set the access scheme of 128K bytes memory below 16M, to enable or disable the local/AT memory, to set the local DRAM access in page-only or page-interleaved mode and to show system ROM size.
41H	To provide I/O bus master the capability to access local memory up to 64M bytes.
42H	To provide ROM/shadow RAM at memory block C (C0000H - CFFFFH).
43H	To provide ROM/shadow RAM at memory block D (D0000H - DFFFFH).
44H	To provide ROM/shadow RAM at memory block E (E0000H - EFFFFH).
45H	To provide ROM/shadow RAM at memory block F (F0000H - FFFFFH).
46H	To remap DRAM blocks A (A0000H - AFFFFH), B (B0000H - BFFFFH), C (C0000H - CFFFFH), D (D0000H - DFFFFH), E (E0000H - EFFFFH), F (F0000H - FFFFFH).
47H	To provide local DRAM remap starting address.
48H	To select classic AT, hidden, and burst refresh options, RAS pulse width of DRAM refresh, and refresh rates.
49H	To enable or disable DRAM parity error, and provide parity error address bits 26 - 24.

4AH	To provide memory parity error address bits 23 - 16.
4BH	To provide memory parity error address bits 15 - 8.
4CH	To provide memory parity error address bits 7 - 2
4DH	To provide memory parity error address bits 1 - 0, and latch coprocessors status.

The following tables describe in more detail the registers in this group:

Index	Default Value	Description
40H	[1100,0XXX]	The bits 5 & 4 of this register are intended to be used for local/AT memory detection. The local memory access mode should not be set to page-interleaved if each bank has a different DRAM type.

Bits	R/W	State	Meaning
<7:6>	R/W	00	Memory located at 0FE0000H - 0FFFFFFH access scheme is to read from AT bus ROM and write to local or AT bus RAM.
		01	Memory located at 0FE0000H - 0FFFFFFH access scheme is to read from local ROM and write to local or AT bus RAM.
		10	Memory located at 0FE0000H - 0FFFFFFH access scheme is to read from local or AT bus RAM and RAM is write protected.
		*11	Memory located at 0FE0000H - 0FFFFFFH access scheme is to read from local or AT bus RAM and write to local or AT bus RAM.
<5:4>	R/W.	*00	Both local DRAM and AT bus DRAM access are enabled.
		01	Local DRAM access is enabled but AT bus DRAM access is disabled.
		10	Local DRAM access is disabled but AT bus Dram access is enabled.
		11	Both local DRAM and AT bus DRAM access are disabled.
3	R/W	*0	DRAM access is in page-only mode.
		1	DRAM access can be in 2-way or 4 way page-interleaved mode depending on the number (2 or 4) of banks of the same DRAM type.

2	R	0	System ROM is 16-bit device.
		1	System ROM is 8-bit device.
<1:0>			Reserved.

Index	Default Value	Description
41H	[0XXX,XXXX]	The traditional AT bus master can only access local memory up to 16M bytes. This register provides the AT bus master the capability to access local memory up to 64M bytes. This register may be used by DMA too. If the programmer wants to use multi-channel DMAs, address bits A26 - A24 must be the same for all channels.

Bits	R/W	State	Meaning
7	R/W	*0	I/O bus master accessing local memory can be up to 16M bytes only.
		1	I/O bus master accessing local memory can be up to 64M bytes.
<6:3>			Reserved.
<2:0>	R/W		These 3 bits are the I/O bus master local memory access address bits 26 - 24 if bit 7 of this register is 1. These 3 bits together with LA (23 - 17), XA (16 - 1), and XBHE-, will form address for the I/O bus master to access local memory up to 64M bytes.

Index	Default Value	Description
42H	[0000,0000]	There are 4 x 16K bytes of DRAM located from C0000H to CFFFFH. Every 16K bytes of this block can be used as a shadow RAM to improve ROM data access speed.
43H	[0000,0000]	There are 4 x 16K bytes of DRAM located from D0000H to DFFFFH. Every 16K bytes of this block can be used as a shadow RAM to improve ROM data access speed.
44H	[0000,0000]	There are 4 x 16K bytes of DRAM located from E0000H to EFFFFH. Every 16K bytes of this block can be used as a shadow RAM to improve ROM data access speed.

45H [0101,0101] There are 4 x 16K bytes of DRAM located from F0000H to FFFFFH. Every 16K bytes of this block can be used as a shadow RAM to improve ROM data access speed.

Bits	R/W	State	Meaning
<7:6>	R/W	00	The access scheme of the fourth 16K bytes region located at C000H - FFFFH of a memory block C, D, E, or F is to read from the AT bus ROM and write to the local or AT bus RAM.
		01	The access scheme of the fourth 16K bytes region located at C000H - FFFFH of a memory block C, D, E, or F is to read from the local ROM and write to the local or AT bus RAM.
		10	The access scheme of the fourth 16K bytes region located at C000H - FFFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and the RAM is write protected.
		11	The access scheme of the fourth 16K bytes region located at C000H - FFFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and write to the local or AT bus RAM.
<5:4>	R/W	00	The access scheme of the third 16K bytes region located at 8000H - BFFFH of a memory block C, D, E, or F is to read from the AT bus ROM and write to the local or AT bus RAM.
		01	The access scheme of the third 16K bytes region located at 8000H - BFFFH of a memory block C, D, E, or F is to read from the local ROM and write to the local or AT bus RAM.
		10	The access scheme of the third 16K bytes region located at 8000H - BFFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and the RAM is write protected.

		11	The access scheme of the third 16K bytes region located at 8000H - BFFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and write to the local or AT bus RAM.
<3:2>	R/W	00	The access scheme of the second 16K bytes region located at 4000H - 7FFFH of a memory block C, D, E, or F is to read from the AT bus ROM and write to the local or AT bus RAM.
		01	The access scheme of the second 16K bytes region located at 4000H - 7FFFH of a memory block C, D, E, or F is to read from the local ROM and write to the local or AT bus RAM.
		10	The access scheme of the second 16K bytes region located at 4000H - 7FFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and the RAM is write protected.
		11	The access scheme of the second 16K bytes region located at 4000H - 7FFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and write to the local or AT bus RAM.
<1:0>	R/W	00	The access scheme of the first 16K bytes region located at 0000H - 3FFFH of a memory block C, D, E, or F is to read from the AT bus ROM and write to the local or AT bus RAM.
		01	The access scheme of the first 16K bytes region located at 0000H - 3FFFH of a memory block C, D, E, or F is to read from the local ROM and write to the local or AT bus RAM.
		10	The access scheme of the first 16K bytes region located at 0000H - 3FFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and the RAM is write protected.
		11	The access scheme of the first 16K bytes region located at 0000H - 3FFFH of a memory block C, D, E, or F is to read from the local or AT bus RAM and write to the local or AT bus RAM.

Note: The procedure to load ROM data into DRAM is as follows. This procedure applies to all shadow RAM area.

- Set the proper memory access scheme to "00" or "01" depending on whether a ROM is located on the local or AT bus.
- Read data from ROM and write the same data back to RAM at the same location. Repeat this operation until all data in ROM has been copied.
- Set memory access scheme to "10" (DRAM read only).

Index	Default Value	Description
46H	[XXXX,0000]	This register is used to remap the memory located at A0000H-FFFFFH to the top memory location specified by register 47H.

Bits	R/W	State	Meaning
<7:4>			Reserved.
<3:0>	R/W	0000	Remap local memory at 0A0000H - 0BFFFFH to the starting address specified by register 47H.
		0100	Remap local memory at 0A0000H - 0BFFFFH and 0D0000H - 0DFFFFH to the starting address specified by register 47H.
		0110	Remap local memory at 0A0000H - 0BFFFFH and 0D0000H - 0EFFFFH to the starting address specified by register 47H.
		1110	Remap local memory at 0A0000H - 0EFFFFH to the starting address specified by register 47H.
		1111	Remap local memory at 0A0000H - 0FFFFFH to the starting address specified by register 47H.
		Else	Reserved.

Index	Default Value	Description
47H	[X000,0001]	This register provides the remap starting address. This address will be determined after the system memory size is decided.

Bits	R/W	State	Meaning
7			Reserved.
<6:0>	R/W		Local memory remap starting address bits 26 - 20.

Index	Default Value	Description
48H	[0X11,0000]	This register is used to select the local DRAM refresh mode, the refresh RAS pulse width, and the refresh rate. The AT bus refresh is always in the classic refresh mode and the refresh rate is always at 256 times per 4 ms.

Bits	R/W	State	Meaning
7	R/W	*0	Local DRAM refresh is AT classic refresh.
		1	Local DRAM refresh is hidden refresh. The CPU will not be put on hold when refresh is in progress.
6			Reserved.
<5:4>	R/W	00	Local DRAM refresh RAS pulse width is 5 CLK2s.
		01	Local DRAM refresh RAS pulse width is 6 CLK2s.
		10	Local DRAM refresh RAS pulse width is 7 CLK2s.
		*11	Local fresh RAS pulse width is 8 CLK2s.
<3:2>	R/W	*00	Local DRAM burst refresh is disabled.
		01	Local DRAM refresh has a burst of 2 if the hidden refresh is enabled.
		10	Local DRAM refresh has a burst of 4 if the hidden refresh is enabled.
		11	Local DRAM refresh has a burst of 8 if the hidden refresh is enabled.
<1:0>	R/W	*00	Local DRAM refresh rate is 256/4ms (typical).
		01	Local DRAM refresh rate is 128/4ms.
		10	Local DRAM refresh rate is 64/4ms.
		11	Local DRAM refresh rate is 32/4ms.

Index	Default Value	Description
49H	[00XX,XXXX]	This register is used to enable or disable the parity checker, to open the error address latches, and to show the parity error address. The bits 7 and 6 of this register are writable even when bit 0 of index register 10H has been set. The bit 6 of this register will be set to 1 when a parity error occurs. The address bits 26 - 2 will be latched and can be read through registers 49H - 4CH while byte enable information is in register 4DH. After reading the parity error address, the bit 6 should be set to 0 to reopen the parity error address latches.

Bits	R/W	State	Meaning
7	R/W	*0	DRAM parity check is disabled.
		1	DRAM parity check is enabled.
6	W	*0	To open DRAM parity error address latches.
	R	0	No DRAM parity error has occurred.
		1	DRAM parity Error has occurred.
<5:3>			Reserved.
<2:0>	R		Local memory parity error address bits 26 - 24 if parity error has occurred.

Index	Default Value	Description
4AH	[XXXX,XXXX]	This register provides 8 address bits of parity error.

Bits	R/W	State	Meaning
<7:0>	R		Local memory parity error address bits 23 - 16 if parity error has occurred.

Index	Default Value	Description
4BH	[XXXX,XXXX]	This register provides 8 address bits of parity error.

Bits	R/W	State	Meaning
<7:0>	R		Local memory parity error address bits 15 - 8 if parity error has occurred.

Index	Default Value	Description
4CH	[XXXX,XXXX]	This register provides 6 address bits of parity error.

Bits	R/W	State	Meaning
<7:2>	R		Local memory parity error address bits 7 - 2 if parity error has occurred.
<1:0>			Reserved.

Index	Default Value	Description
4DH	[XXXX,XXXX]	This register provides the status of the coprocessors and the byte enable bits of a parity error. The bits 3 & 2 are the INTEL 80387 and the Weitek 3167 coprocessors status respectively when the first read after system is powered on. It is the BIOS' responsibility to read the data of these 2 bits and write them to register 12H for later use.

Bits	R/W	State	Meaning
<7:4>			Reserved.
3	R	0	INTEL 80387 is not installed or DRAM byte 3 has no parity error.
		1	INTEL 80387 is installed or DRAM byte 3 has parity error.
2	R	0	Weitek 3167 is not installed or DRAM byte 2 has no parity error.
		1	Weitek 3167 is installed or DRAM byte 2 has parity error.
1	R	0	Byte 1 has no parity error.
		1	Byte 1 has parity error.
0	R	0	Byte 0 has no parity error.
		1	Byte 0 has parity error.

2.2.4 Non-Cache/Non-Local Memory Blocks Control Registers

The Eagle chip set provides four 3-register sets which will be used to dedicate up to four non-cache or non-local memory blocks. These four blocks are used to allocate four non-cachable region or to direct local memory access to AT memory access.

The following table briefly describes the function of the registers in this group:

Index	Functions
50H	To select non-cache or non-local memory block #0 and the block size.
51H	To provide non-cache or non-local memory block #0 starting address bits 26 - 20.
52H	To provide non-cache or non-local memory block #0 starting address bits 19 - 12.
53H	To select non-cache or non-local memory block #1, and the block size.
54H	To provide non-cache or non-local memory block #1 starting address bits 26 - 20.
55H	To provide non-cache or non-local memory block #1 starting address bits 19 - 12.
56H	To select non-cache or non-local memory block #2, and the block size.
57H	To provide non-cache or non-local memory block #2 starting address bits 26 - 20.
58H	To provide non-cache or non-local memory block #2 starting address bits 19 - 12.
59H	To select non-cache or non-local memory block #3, and the block size.
5AH	To provide non-cache or non-local memory block #3 starting address bits 26 - 20.
5BH	To provide non-cache or non-local memory block #3 starting address bits 19 - 12.

The following tables describe in more detail the registers in this group:

Index	Default Value	Description
50H	[00XX,XXXX]	The bits 7 and 6 of this register are used to set the memory block 0 as a non-cache or a non-local memory region while the bits 3 - 0 provide the block size. The starting address of block 0 is in registers 51H and 52H.
53H	[00XX,XXXX]	The bits 7 and 6 of this register are used to set the memory block 1 as a non-cache or a non-local memory region while the bits 3 - 0 provide the block size. The starting address of block 1 is in registers 54H and 55H.
56H	[00XX,XXXX]	The bits 7 and 6 of this register are used to set the memory block 2 as a non-cache or a non-local memory region while the bits 3 - 0 provide the block size. The starting address of block 2 is in registers 57H and 58H.

59H	[00XX,XXXX]	The bits 7 and 6 of this register are used to set the memory block 3 as a non-cache or a non-local memory region while the bits 3 - 0 provide the block size. The starting address of block 3 is in registers 5AH and 5BH.

Note: A designated non-local memory block is automatically a non-cache block.

Bits	R/W	State	Meaning
<7:6>	R/W	*00	Do not designate a non-cache or non-local memory block.
		01	Designate a non-cache block.
		10	Designate a non-local memory block.
		11	Reserved.
<5:4>			Reserved.
<3:0>	R/W	0000	Non-cache/non-local memory block size is 4K bytes.
		0001	Non-cache/non-local memory block size is 8K bytes.
		0010	Non-cache/non-local memory block size is 16K bytes.
		0011	Non-cache/non-local memory block size is 32K bytes.
		0100	Non-cache/non-local memory block size is 64K bytes.
		0101	Non-cache/non-local memory block size is 128K bytes.
		0110	Non-cache/non-local memory block size is 256K bytes.
		0111	Non-cache/non-local memory block size is 512K bytes.
		1000	Non-cache/non-local memory block size is 1M bytes.
		1001	Non-cache/non-local memory block size is 2M bytes.
		1010	Non-cache/non-local memory block size is 4M bytes.
		Else	Reserved.

Index	Default Value	Description
51H	[XXXX,XXXX]	This register provides the starting address high byte for the non-cache or non-local memory block if block 0 is used.

54H	[XXXX,XXXX]	This register provides the starting address high byte for the non-cache or non-local memory block if block 1 is used.
57H	[XXXX,XXXX]	This register provides the starting address high byte for the non-cache or non-local memory block if block 2 is used.
5AH	[XXXX,XXXX]	This register provides the starting address high byte for the non-cache or non-local memory block if block 3 is used.

Bits	R/W	State	Meaning
7			Reserved.
<6:0>	R/W		Non-cache/non-local memory block starting address bits 26 - 20.

Index	Default Value	Description
52H	[XXXX,XXXX]	This register provides the starting address low byte for the non-cache or non-local memory block if block 0 is used.
55H	[XXXX,XXXX]	This register provides the starting address low byte for the non-cache or non-local memory block if block 1 is used.
58H	[XXXX,XXXX]	This register provides the starting address low byte for the non-cache or non-local memory block if block 2 is used.
5BH	[XXXX,XXXX]	This register provides the starting address low byte for the non-cache or non-local memory block if block 3 is used.

Bits	R/W	State	Meaning
<7:0>	R/W		Non-cache/non-local memory block starting address bits 19 - 12.

2.2.5 Cache Memory Control Registers

There are 6 registers in this group. They are used to test and diagnose the cache controller and provide error information if any Tag RAM error occurred.

The following table briefly describes the function of the registers in this group:

Index	Functions
60H	To enable or disable cache operation and SRAM direct access, to select the SRAM access mode and the cache size, to set the 2-way set associative or direct map cache and the SRAM access wait states.
61H	To enable or disable the cache controller's Tag RAM direct access, to select the access of Tag field, Valid field, or LRU and to provide the Tag RAM address bit 8.
62H	To provide the cache controller's Tag RAM address bits 7 - 0.
63H	To provide an I/O port for cache controller's Tag RAM access.
64H	To enable or disable the Tag RAM error NMI, and to provide the Tag RAM error address bit 8.
65H	To provide the Tag RAM error address bits 7 - 0.

The following tables describe in more detail the registers in this group:

Index	Default Value	Description
60H	[0000,0010]	This register is used to enable or disable the cache controller and the SRAM direct access, to set the SRAM access to output enable or chip select mode, SRAM size, cache access mode to 2-way set associate or direct map, and the access wait states.

Bits	R/W	State	Meaning
7	R/W	*0	Cache Controller is disabled.
		1	Cache Controller is enabled.
6	R/W	*0	Normal cache operation if cache is enabled.
		1	Cache memory is frozen, a read miss will not cause updating of the cache, a write hit will modify the cache data.
<5:4>	R/W	*00	Cache size is 32K bytes.
		01	Cache size is 64K bytes.
		10	Cache size is 128K bytes.
		11	Reserved.
3	R/W	*0	2-way set associative cache access.
		1	Direct mapped cache access.
2	R/W	*0	Select SRAM access through output enable mode.
		1	Select SRAM access through chip select mode.

1	R/W	0	SRAM access has 0 wait state.
		*1	SRAM access has 1 wait state.
0	R/W	*0	SRAM direct access is disabled.
		1	SRAM direct access is enabled and the starting address is from location 040000H to 040000H + (size of cache - 1).

Index	Default Value	Description
61H	[0XXX,XXXX]	This register provides a way to access the Tag RAM in the cache controller. For direct mapped cache, the Tag RAM of set 0 refers to the lower half (index 0 - 511) of the Tag RAM while the Tag RAM of set 1 refers to the higher half (index 512 - 1023) of the Tag RAM.

Bits	R/W	State	Meaning
7	R/W	*0	Cache controller's Tag RAM direct access is disabled.
		1	Cache controller's Tag RAM direct access is enabled.
<6:4>	R/W	000	Tag RAM's low byte and LRU bit of set 0 can be accessed. The data bits 7 - 2 accessed through register 63H are the system address bits 19 - 14 in the Tag RAM and the bit 0 is the LRU bit.
		001	Tag RAM's high byte of set 0 can be accessed. The data bits 6 - 0 accessed through register 63H are the system address bits 26 - 20 in the Tag RAM.
		010	VALID field's low byte of set 0 is accessible.The data bits 7 - 0 accessed through register 63H are the VALID field bits 7 - 0.
		011	VALID field's high byte of set 0 is accessible. The data bits 7 - 0 accessed through register 63H are the VALID field bit 15 - 8.
		100	Tag RAM's low byte and the LRU bit of set 1 is accessible. The data bits 7 - 2 accessed through register 63H are the system address bits 19 - 14 in the Tag RAM and the bit 0 is the LRU.

		101	Tag RAM's high byte of set 1 is accessable. The data bits 6 - 0 accessed through register 63H are the system address bits 26 - 20 in the Tag RAM.
		110	VALID field's low byte of set 1 is accessable. The data bits 7 - 0 accessed through register 63H are the VALID field bits 7 - 0.
		111	VALID field's high byte of set 1 is accessable. The data bits 7 - 0 accessed through register 63H are the VALID field bits 15 - 8.
<3:1>			Reserved.
0	R/W		Tag RAM address bit 8.

Index	Default Value	Description
62H	[XXXX,XXXX]	This register with bit 0 of register 61H provides the index address, ranging from 0 to 511, of a Tag RAM.

Bits	R/W	State	Meaning
<7:0>	R/W		The Tag RAM index address bits 7 - 0.

Index	Default Value	Description
63H	[XXXX,XXXX]	This register is a data port which is used to access Tag RAM directly. To direct access a Tag RAM, first set Tag RAM index address and enable Tag RAM direct access through register 61H & 62H, then read the Tag RAM data through this register.

Bits	R/W	State	Meaning
<7:0>	R/W		Data port for directly accessing the Tag RAM which is pointed to by registers 61H and 62H, if cache controller's Tag RAM direct access is enabled.

Index	Default Value	Description
64H	[00XX,XXXX]	This register is used to enable or disable the Tag RAM error NMI, to provide the error status, and the address bit 8 of error. The bits 7 and 6 are writable even if bit 0 of index register 10H has been set. If both sets of the

Tag RAM indicate a cache hit for a memory access in the 2-way set associative mode, the bit 6 of this register will be set to indicate a cache error. The address bits 8 - 0 of the Tag RAM error will be latched in registers 64H, 65H. After reading the index address of the Tag error, bit 6 of this register should be set to 0 to reopen the latches to wait for the next error.

Bits	R/W	State	Meaning
7	R/W	*0	Tag RAM error NMI is disabled.
		1	Tag RAM error NMI is enabled.
6	W	*0	Clear Tag RAM error and reopen Tag RAM error address latches.
	R	0	No Tag RAM error has occurred.
		1	Tag RAM error has occurred.
<5:1>			Reserved.
0	R		The address bit 8 of Tag RAM error.

Index	Default Value	Description
65H	[XXXX,XXXX]	This register provides the address of a Tag RAM error if the Tag RAM error has occurred. Together with the bit 0 of index register 64, it can address up to 512 Tag RAM entries.

Bits	R/W	State	Meaning
<7:0>	R/W		The address bits 7 - 0 of Tag RAM error.

2.2.6 EMS Mapper Support Registers

There are 6 index registers and 4 I/O ports in this group. The registers 70H and 71H are EMS control register while registers 72H, 73H, 74H, 75H and the I/O ports provide a paged memory address.

The following table briefly describes the function of the registers in this group:

Index	Functions
70H	To enable or disable the EMS mapper and to set the EMS mapper access wait states.
71H	To select the EMS mapper page frame and I/O ports for setting up paged memory address.
72H	To provide EMS mapper page 0 memory address bits 26 - 21.
73H	To provide EMS mapper page 1 memory address bits 26 - 21.
74H	To provide EMS mapper page 2 memory address bits 26 - 21.
75H	To provide EMS mapper page 3 memory address bits 26 - 21.

The following tables describe in more detail the registers in this group:

Index	Default Value	Description
70H	[0XXX,XXXX]	This register is used to enable or disable the EMS mapper and set access wait states. If bit 7 of this register is 0, all EMS related registers are ignored.

Bits	R/W	State	Meaning
7	R/W	*0	EMS mapper is disabled.
		1	EMS mapper is enabled.
6	R/W	0	No extra wait state for DRAM access if the EMS mapper is enabled and accessed.
		1	1 extra wait state for DRAM access if the EMS mapper is enabled and accessed.
<5:0>			Reserved.

Index	Default Value	Description
71H	[XXXX,XXXX]	This register is used to select a 64K bytes EMS memory page frame and I/O ports to setup the 4 paged memory addresses.

Bits	R/W	State	Meaning
<7:4>	R/W	0000	Select 4 pages EMS base address location at C0000H, C4000H, C8000H, CC000H respectively.
		0001	Select 4 pages EMS base address location at C4000H, C8000H, CC000H, D0000H respectively.

		0010	Select 4 pages EMS base address location at C8000H, CC000H, D0000H, D4000H respectively.
		0011	Select 4 pages EMS base address location at CC000H, D0000H, D4000H, D8000H respectively.
		0100	Select 4 pages EMS base address location at D0000H, D4000H, D8000H, DC000H respectively.
		0101	Select 4 pages EMS base address location at D4000H, D8000H, DC000H, E0000H respectively.
		0110	Select 4 pages EMS base address location at D8000H, DC000H, E0000H, E4000H respectively.
		0111	Select 4 pages EMS base address location at DC000H, E0000H, E4000H, E8000H respectively.
		1000	Select 4 pages EMS base address location at E0000H, E4000H, E8000H, EC000H respectively.
		Else	Reserved.
<3:0>	R/W	0000	Select EMS mapper 4 page registers I/O port at 0208/0209H, 4208/4209H, 8208/8209H, C208/C209H.
		0001	Select EMS mapper 4 page registers I/O port at 0218/0219H, 4218/4219H, 8218/8219H, C218/C219H.
		0101	Select EMS mapper 4 page registers I/O port at 0258/0259H, 4258/4259H, 8258/8259H, C258/C259H.
		0110	Select EMS mapper 4 page registers I/O port at 0268/0269H, 4268/4269H, 8268/8269H, C268/C269H.
		1010	Select EMS mapper 4 page registers I/O port at 02A8/02A9H, 42A8/42A9H, 82A8/82A9H, C2A8/C2A9H.
		1011	Select EMS mapper 4 page registers I/O port at 02B8/02B9H, 42B8/42B9H, 82B8/82B9H, C2B8/C2B9H.
		1110	Select EMS mapper 4 page registers I/O port at 02E8/02E9H, 42E8/42E9H, 82E8/82E9H, C2E8/C2E9H.
			Else Reserved.

Index	Default Value	Description
72H	[XXXX,XXXX]	EMS mapper page 0 memory address high byte.
73H	[XXXX,XXXX]	EMS mapper page 1 memory address high byte.
74H	[XXXX,XXXX]	EMS mapper page 2 memory address high byte.
75H	[XXXX,XXXX]	EMS mapper page 3 memory address high byte.

Bits	R/W	State	Meaning
<7:6>			Reserved.
<5:0>	R/W		EMS mapper paged memory mapping address bits 26 - 21.

Non-indexed I/O ports:

The following table is the description of non-indexed I/O ports:

IO Port	Default Value	Description
02X8H/ 02X9H	[0XXX,XXXX]	To enable or disable the EMS mapper page 0 memory and to provide the EMS page 0 address bits 20 - 14. Together with index register 72H provides a 16K bytes memory starting address.
42X8H/ 42X9H	[0XXX,XXXX]	To enable or disable the EMS mapper page 1 memory and to provide the EMS page 1 address bits 20 - 14. Together with index register 73H, provides a 16K bytes memory starting address.
82X8H/ 82X9H	[0XXX,XXXX]	To enable or disable the EMS mapper page 2 memory and to provide the EMS page 2 address bits 20 - 14. Together with index register 74H, provides a 16K bytes memory starting address.
C2X8H/ C2X9H	[0XXX,XXXX]	To enable or disable the EMS mapper page 3 memory and to provide the EMS page 3 address bits 20 - 14. Together with index register 75H, provides a 16K bytes memory starting address.

Bits	R/W	State	Meaning
7	R/W	*0	EMS mapper paged memory is disabled.
		1	EMS mapper paged memory is enabled.
<6:0>	R/W		EMS mapper paged memory mapping address bits 20 - 14.

3. e88C311 PIN DESCRIPTION

3.1 e88C311 Pin Diagram

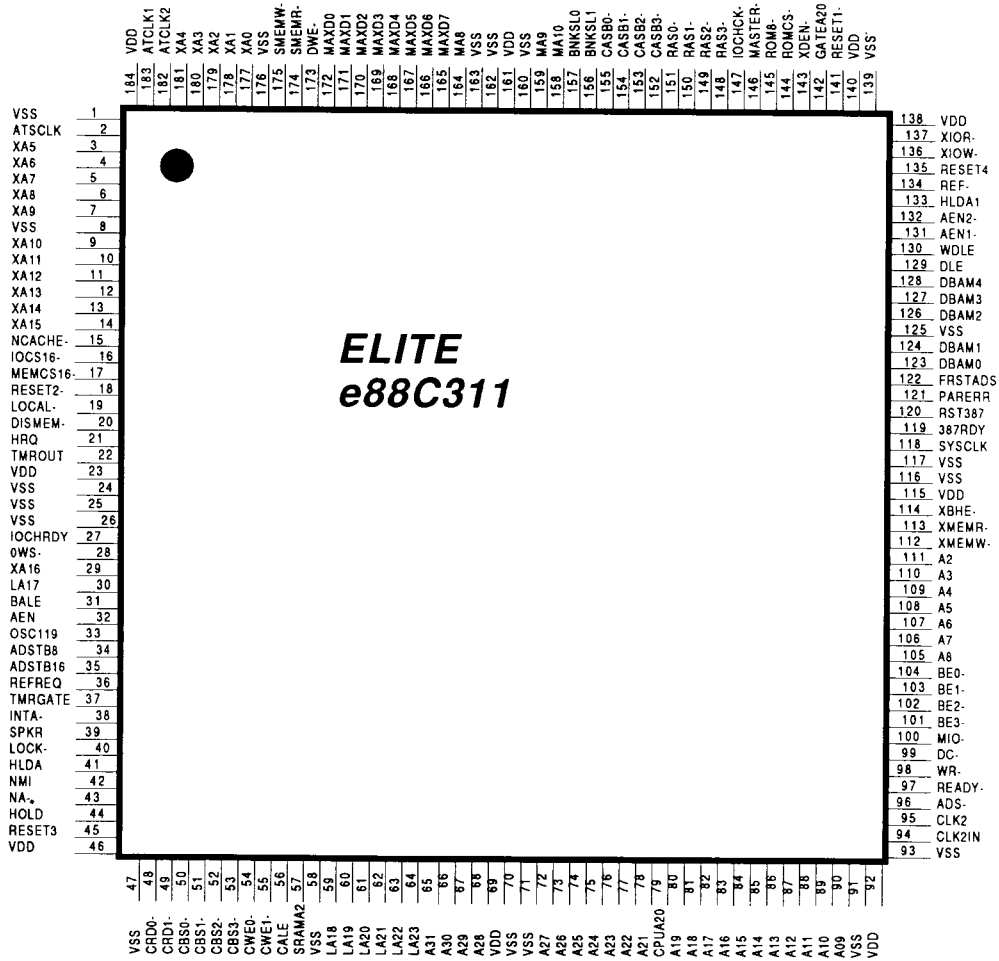


Figure 3-1. e88C311 Pin Diagram

3.2 e88C311 Pin List

PIN No.	NAME	TYPE	DESCRIPTION
94	**CLK2IN**	Input	*CLK2 input* from a packaged TTL crystal oscillator running at twice the rated frequency of the 80386.
95	**CLK2**	Output	Output to CLK2 of the 80386 and the coprocessor. It is driven normally by CLK2IN with a 50% duty cycle. It can also be programmed to have the same frequency as ATCLK1 input.
118	**SYSCLK**	Output	CLK2 divided by two. The phase relationship is the same as the 80386 internal processor clock.
183	**ATCLK1**	Input	*AT bus clock* input from a packaged TTL crystal oscillator. The AT bus state machine is driven by this signal or from a derivation of CLK2 input. This signal should be tied to VCC or GND if not used.
182	**ATCLK2**	Output	*AT Clock 2* is the AT state machine clock output, and is programmed to be one-third, one-fourth, and one-fifth of the frequency of CLK2 or the same frequency as ATCLK1.
2	**ATSCLK**	Output	*AT bus System Clock* is a clock output to the AT expansion bus, running at 1/2 the AT state machine clock (ATSCLK2).
33	**OSC119**	Input	*Oscillator 1.19Mhz clock* input from the e88C312. This signal is used by the DRAM controller for RAS low time out.
141	**RESET1-**	Input	A pulse input generated from the power supply POWER GOOD signal or push button for cold reset. This signal causes a system level reset, setting all programmable registers to their default values. It has a Schmitt Trigger input buffer.
18	**RESET2-**	Input	A pulse signal input from 8042 Keyboard Controller for a warm reset. It resets the 80386 CPU and 80387/WEITEK coprocessors.

PIN No.	NAME	TYPE	DESCRIPTION
45	**RESET3**	Output	An output signal to reset the 80386, 80387 and Weitek 3167 coprocessors. It is activated by RESET1-, RESET2-, Shutdown or Fast Reset. It lasts for at least 80 CLK2 cycles so that the 80386 can perform a Self Test. The phase relationship to CLK2 is maintained to reset 80386 properly.
135	**RESET4**	Output	Activated by RESET1-, to reset the e88C312 and other on-board peripherals. It also drives RESDRV to reset the AT I/O channel. The duration of the active period is the same as RESET3.
120	**RST387**	Output	*80387 Reset* is connected to the 80387 RESET pin. It is activated when RESET3 is active, or an I/O write to port F1 is executed.
44	**HOLD**	Output	*HOLD Request* is an active high signal output to 80386 HOLD input. When active, this signal requests that 80386 relinquish local bus control to another master (DMA, Master, or AT Refresh Controller). It is disabled when snooping feature is enabled or during hidden refresh cycles.
41	**HLDA**	Input	*Hold Acknowledge* is an active high input from 80386. When high, it indicates that 80386 CPU has relinquished the system bus in response to a HOLD request.
21	**HRQ**	Input	*Hold Request* is an active high input signal from the 82C206. It is active when a DMA or an AT Bus Master is requesting a bus cycle via the DMA channel.
36	**REFREQ**	Input	*Refresh Request* is an active high signal from timer 1 output of the 82C206. In a PC/AT implementation, it is activated every 15.6 μs for a Local/AT memory refresh request. In burst refresh mode, these requests are accumulated to the programmed number before actual refresh cycles are executed.

PIN No.	NAME	TYPE	DESCRIPTION
133	**HLDA1**	Output	*Hold Acknowledge* 1 is an active high signal to the e88C312 and 82C206. When active in response to HOLD, it indicates that the 80386 CPU has relinquished system buses to another master (DMA, Master, or AT Refresh Controller). When bus snooping feature is enabled, the HLDA1 can be activated without the HOLD-HLDA handshaking sequence with the CPU.
134	**REF-**	Input/Output	*Refresh* is an active low bidirectional signal. During the Master refresh cycle, the I/O channel master drives this signal low. During a normal AT refresh cycle, REF- is an output to the I/O channel. In both cases, e88C311 will transfer addresses XA0-XA11 onto AT bus lines SA0-SA11.
96	**ADS-**	Input	*Address Strobe* is an active low input signal from 80386 indicating a valid bus cycle. All status and address lines are driven by the 80386 pins. It is asserted during T1 and T2p bus states. A 10K pullup resistor on this pin is recommended.
100	**M/IO-**	Input	*Memory or I/O* command status is an input signal from the 80386. It indicates a memory cycle when high and an I/O cycle when low. A 10K pullup resistor on this pin is recommended.
98	**W/R-**	Input	*Write/Read command status* is an input signal from 80386. It indicates a write cycle when high and a read cycle when low. A 10K pullup resistor is recommended.
99	**D/C-**	Input	*Data/Code command status* is an input signal from 80386. It indicates a data cycle when high and a command (code) cycle when low. A 10K pullup resistor is recommended.
119	**387RDY-**	Input	*80387 Coprocessor Ready* is an active low signal connected to the READYO pin of the 80387. This signal is internally sampled by SYSCLK inside the e88C311 before driving READY- active.
97	**READY-**	Input/Output	This signal is an active low bidirectional signal. It is driven low at the end of CPU, memory, I/O or coprocessor access cycles. It is an input signal when an external local master completes its cycle.

PIN No.	NAME	TYPE	DESCRIPTION
65~68 72~78 79 80~90 105~111	**A<31:28>,** **A<27:21>,** **CPUA20,** **A<19:9>,** **A<8:2>**	Inputs	Local Address input signals from the 80386.
101~104	**BE<3:0>-**	Inputs	*Byte Enable* inputs, BE0- through BE3- are active low input signals from the 80386. These input pins indicate the bytes of the 32-bit data bus involved with the current CPU cycle. BE0- controls the least significant byte and BE3- controls the most significant byte.
40	**LOCK-**	Input	LOCK- is an active low input signal from the 80386, indicating that other system bus masters are not to gain control of the system bus. If sampled active, the e88C311 will not execute DMA/Master cycles until the locked bus cycle is completed.
43	**NA-**	Output	*Next Address* is an active low open collector output signal connected to the 80386. When sampled active, the next CPU cycle is a pipeline cycle. It is driven active by setting bit 0 of index register 12 except during bus snooping when the internal state machine is not ready for the next address input.
19	**LOCAL-**	Input	*Local-* is an active low input signal from a local bus master. The e88C311 samples this signal at one quarter of T2 or T1P states. If it is sampled active, the e88C311 will not perform any bus access. The local bus master has to generate the READY- to terminate the cycle. Note: The direct mapped cache option may cause a data bus conflict if a memory mapped device is acting as a local bus master and tries to transfer data to the local data bus while the SRAMs are driven.
15	**NCACHE-**	Input	*Non-Cacheable Access* is an active low signal. It indicates that the current cycle is non-cacheable. This signal is sampled at a quarter of T2 or T1P states. If it is sampled active, no cache access will be performed. The e88C311 also allows a system designer to designate a portion of main memory as non-cacheable through NACHE- control or through index register (50h-5Bh) programming.

PIN No.	NAME	TYPE	DESCRIPTION
20	**DISMEM-**	Input	*Disable Local Memory Access* is an active low input signal. This signal is sampled at a quarter of T2 or T1P states. Once sampled active, there will be no local memory (SRAM or DRAM) access. All memory cycles are re-directed to the AT bus.
142	**GATEA20**	Input	*Gate A20* is an active high input signal from the 8042/8742 keyboard controller. When high, the e88C311 drives CPUA20 onto the internal logical address, A20. When low, it forces A20 to be low, regardless of the CPUA20 state. It is used to keep the system address less than 1 MB during DOS operation.
49~48	**CRD<1:0>-**	Output	*CACHE READ* are active low output signals connected to the SRAM's Output Enable or Chip Select pins of cache banks 1 and 0 respectively. During a read hit cycle, CRD0- and CRD1- are enabled to drive the requested data onto the D bus. In a 2-way set associative cache, only the bank with a cache hit is selected. In direct mapped cache, CRD0- and CRD1- drive the 1st and 2nd halves of cache SRAMs respectively. In the Output Enable mode, CRD0- and CRD1- are active only during read access. In the Chip Select mode, CRD0- and CRD1- are active during all cache memory accesses (read or write).
50~53	**CBS<3:0>-**	Output	*Cache SRAM Byte Select* are active low output signals to the Chip Select pins of the cache SRAM array. During a read miss cycle, all byte select (CBS<3:0>-) are active, independent of the BE<3:0>- inputs. During a cache write hit cycle, only selected bytes are enabled.
54~55	**CWE<1:0>-**	Output	*Cache Write Enable* 1 or 0 are active low signals to the cache SRAM Write Enable (WE-) pins. They respectively enable cache bank 1 and 0 to receive data from the CPU data bus (during read miss or write hit cycles). In a two-way set associate cache, depending on which bank has a cache hit, only one SRAM bank is enabled. In a direct mapped cache, depending on the address, CWE0- controls the first half and CWE1- controls the second half of the cache SRAM.

PIN No.	NAME	TYPE	DESCRIPTION
56	**CALE**	Output	*Cache Address Latch Enable* is an output signal used to latch the low order CPU address bits to the cache SRAM address inputs. When CALE is high, the latch is transparent. On the high to low transition, CALE latches the CPU address onto the SRAM address inputs until CALE returns to an active high state. Some Cache SRAMs have the address latch built in and the design is simplified.
57	**SRAMA2**	Output	*Cache SRAM A2 Address* is an output signal to the SRAM array. It is used to control A2 inversion in 128KB data cache mode. During a read miss in 128K mode, SRAMA2 drives inverted A2 in the first half of the cycle and will switch to non-inverted A2 for the second half of the cycle.
158,159, 164	**MA<10:8>**	Output	The three MSB of DRAM memory array address lines. MA10, MA9 and MA8 should be connected to system DRAM address lines A10, A9 and A8 respectively.
165~172	**MAXD<7:0>**	Input/Output	*Multiplexed Memory Address/XD* data lines MAXD<7:0> are bidirectional signals used to interface to system DRAMs and e88C311 internal registers. During DRAM access, MAXD<7:0> represent the lower 8 address bits for the DRAM array. During e88C311 internal register access, these signals are connected to peripheral data bus (XD) through an external transceiver 74LS245. XDEN enables 74LS245 and XIOR- controls the direction of the 74LS245.
148~151	**RAS<3:0>-**	Output	*Row Address Strobe* signals are active low output to the local DRAM array. There is one RAS- signal for each bank of the local DRAM.
156~157	**BNKSL<1:0>**	Output	*Bank Select* are encoded signals used to select each DRAM bank. External demultiplexers (74F139) take BNKSL<1:0> and CASB<3:0>- as inputs to generate CAS Byte Select signals for each DRAM bank.

PIN No.	NAME	TYPE	DESCRIPTION
152~155	**CASB<3:0>-**	Output	*CAS Byte* Enable of bytes <3:0> for all DRAM Banks. It is necessary to multiplex CASB<3:0>- with BNKSL<1;0> outputs to generate CAS- control signals for each DRAM bank.
129	**DLE**	Output	*Data Latch Enable* is an active high output signal to the e88C312. On the high to low transition, data from MD, SD or XD bus are latched onto the D bus during read cycles (DRAM, AT or on board I/O).
173	**DWE-**	Output	*DRAM Write Enable* is an active low output signal to the DRAM array. This signal is buffered before connecting to the WE- inputs of DRAMs.
130	**WDLE**	Output	*Write Data Latch Enable* is an output signal to e88C312. On the high to low transition, D bus data are latched onto MD bus within the e88C312. CPU can execute the next cycle while DRAM is completing the current write operation.
121	**PARERR**	Input	*Parity Error* is an active high signal from the e88C312, indicating that a parity error has been detected. Upon detecting PARERR active, the e88C311 can initiate a NMI to the CPU and latch the error address into index register 49n - 4Cn
123~124 126~128	**DBAM<4:0>**	Output	*Data Buffer Action Mode* are encoded output control signals to the e88C312. They are used for data bus sizing and byte alignment operations. In addition, all on-board I/O chip select signals are generated by decoding these bits within the e88C312.
59~64 30	**LA<23:17>**	Input/Output	*Local Address bits 17 through23* are bidirectional signals connected to the AT I/O channel. They are output during CPU access and are inputs during Master mode operation (however, in master refresh mode, these are output signal sent to AT I/O channel.)

PIN No.	NAME	TYPE	DESCRIPTION
29 9~14 3~7, 177~181 114	**XA16** **XA<15:10>** **XA<9:0>** **XBHE-**	Input/Output	These signals are outputs to the XA-bus and SA-bus during 80386access. They are inputs to the e88C311 during DMA or Master cycles (except XA0 and XBHE-). During the DMA/Master cycle, XBHE- is driven low for 16 bit operation and it is inverted from the XA0 value for 8 bit operation. XA0 is an output and stays low during a 16 bit DMA/Master cycle.
113	**XMEMR-**	Input/Output	*Memory Read Command* is an active low bidirectional signal used by XD-bus peripherals (i.e., BIOS ROM) or I/O channel memory. When active, valid data will be driven onto the SD or the LSD bus. It is an output when the CPU controls the system bus or during a Master Refresh cycle. It is an input during DMA or other Master cycles (except Master Refresh) .
112	**XMEMW-**	Input/Output	*Memory Write Command* is an active low bidirectional signal used by XD-bus peripherals or I/O channel memory. When active, it directs peripherals to accept data from the XD or LSD bus. It is an output when the CPU controls the system bus and an input during DMA/Master cycles.
137	**XIOR-**	Input/Output	*I/O Read Command* is an active low signal used by the XD bus peripherals as well as the I/O channel. It is an output during CPU I/O read accesses and an input during DMA/Master cycles.
136	**XIOW-**	Input/Output	*I/O Write Command* is an active low signal used by XD bus peripherals as well as the I/O channel. It is an output during CPU IO write accesses and an input during DMA/Master cycles.
174	**SMEMR-**	Output	*System Memory Read* is an active low signal to the AT I/O channel. When active, it indicates an AT read access to the lower 1 Megabyte memory space.
175	**SMEMW-**	Output	*System Memory Write* is an active low signal to the AT I/O channel. When active, it indicates an AT write access to the lower 1 Megabyte memory space.

PIN No.	NAME	TYPE	DESCRIPTION
31	**BALE**	Output	*Bus Address Latch Enable* is an active high output used to validate addresses on the I/O channel. BALE is driven high during DMA or Master cycles.
131	**AEN1-**	Input	*Address Enable* for 8-bit DMA transfers is an active low signal. When active, it enables the 8-bit latch containing the upper address bits (A8-A15) onto the system address bus.
132	**AEN2-**	Input	*Address Enable* for 16-bit DMA transfers is an active low signal. When active, it enables the 8-bit latch containing the upper address bits (A9-A16) onto the system address bus.
146	**MASTER-**	Input	*Master* is an active low input signal from the I/O channel. When active, it indicates that another CPU or a DMA controller is residing on the I/O channel to control the system bus.
17	**MEMCS16-**	Input	*Memory 16-bit Chip Select* is an active low input signal from the I/O channel. When active, it indicates that the current memory cycle is a 16-bit access.
16	**IOCS16-**	Input	*I/O 16 bit Chip Select* is an active low input signal from the I/O channel. When active, it indicates that the current I/O cycle is a 16-bit access.
28	**0WS-**	Input	An active low signal from the I/O channel. It allows the present bus cycle to terminate without inserting any additional wait states. 0WS- is driven with an open collector or a tri-state driver.
27	**IOCHRDY**	Input	*I/O Channel Ready* is an active high input signal from AT IO channel. A slow I/O device on the AT bus drives it low during an AT cycle, and the e88C311 will insert extra wait states in AT I/O or Memory accesses. When high, the e88C311 will terminate AT cycles according to programmed wait states.
147	**IOCHCK-**	Input	*I/O Channel Check* is an active low input signal from the AT I/O channel, indicating an error condition. When the NMI feature is enabled and the EN IO CHK (Enable I/O Channel Check) bit in port B is set, e88C311 generates an NMI if IOCHCK- is active.

PIN No.	NAME	TYPE	DESCRIPTION
122	**FRSTADS**	Output	*First ADS* is an output signal to e88C312 indicating the first CPU cycle. It is used by the e88C312 to stop further detection of coprocessor presence. It is high during reset to the CPU and becomes low after the first ADS- pulse.
32	**AEN**	Output	*Acknowledge* is an active high signal. When active it indicates that AEN1/AEN2 or Refresh has been asserted. This signal is used to drive the AEN pin of the I/O channel. It is inverted to drive the ACK- input of the 82C206.
38	**INTA-**	Output	An active low *Interrupt Acknowledge* to the interrupt controller within the 82C206.
143	**XDEN-**	Output	*Peripheral data bus (XD) Enable.* It is an active low signal to enable data transfer between XD and MAXD<7:0> buses. XDEN- is asserted during I/O register access is (indexed or non-indexed) inside the e88C311.
144	**ROMCS-**	Output	An active low *ROM Chip Select* signal. If both ROMCS- and XMEMR- are active, EPROM data will be driven onto the local SD (LSD) bus. ROM access is also decoded into action codes that enable the e88C312 to pass local SD (LSD) data onto the D bus.
34	**ADSTB8**	Input	*Address Strobe for 8-bit DMA* is an active high signal used to latch the upper address byte (A8-A15). Upon a high to low transition, XD-bus data (<MAXD7:MAXD0>) driven by the 82C206 are latched onto an internal buffer inside the e88C311. The DMA addresses A8-A15 remain valid until the next ADSTB8 becomes active again.
37	**TMRGATE**	Output	*Timer Gate* is an output signal connected to the TMRCLK (Timer Clock) input of 80C206. It is driven by bit 0 of port 61 register to enable Timer 2 inside the 80C206.
22	**TMROUT**	Input	*Timer Out* is an input signal connected to OUT2 (Output of Timer 2) pin of the 80C206. In a PC/AT system, it is used to drive the speaker.
39	**SPKR**	Output	This signal is used to drive the speaker. It is a gated output of speaker data and the TMROUT signal from 82C206.

PIN No.	NAME	TYPE	DESCRIPTION
35	**ADSTB16**	Input	*Address Strobe for 16-bit DMA* is an active high signal used to latch the upper address byte (A9-A16). Upon a high-to-low transition, XD-bus data (<MAXD7:MAXD0>) driven by the 82C206 are latched onto an internal buffer inside the e88C311.
42	**NMI**	Output	An active high *Non-Maskable Interrupt* output connected to the NMI input of the CPU. In the e88C311, a NMI can be generated when an I/O error, a DRAM parity error, or a cache error occurs.
145	**ROM8-**	Input	An active low signal indicating an 8 bit ROM device access. It should be tied high when 16 bit ROM devices are used.
23, 46, 69 92, 115, 138 140, 161, 184	**VDD**		
1, 8, 24 25, 26, 47 58, 70, 71, 91 93, 116, 117, 125, 139, 160, 162, 163, 176	**VSS**		

4. e88C311 ELECTRICAL & TIMING SPECIFICATION

4.1 Absolute Maximum Ratings

(Vss = 0 volts)

Stresses above the conditions listed in this section may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at these or any other conditions above those indicated in the Recommended Operating Conditions section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute Minimum Ratings for e88C311

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	-0.3	7.0	Volts
Input Voltage	V_i	-0.3	V_{cc} + 0.3	Volts
Storage Temperature	T_{stg}	-40.0	125.0	degrees C

4.2 e88C311 Recommended Operating Conditions

(Vss = volts)

Table 4-2. Recommended Operating Conditions for e88C311

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	4.75	5.25	Volts
Input Voltage	V_i	0	V_{cc}	Volts
Ambient Temperature	T_a	0	50	degrees C

4.3 e88C311 DC Characteristics

(Vcc = 5V +/- 5%, Ta = 0 to 50° C)

Table 4-3. e88C311 DC Characteristics

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Input Low Voltage	Vil			
TTL level			.8	Volts
Schmitt level			1.0	Volts
Input High Voltage	Vih			
TTL level		2.0		Volts
Schmitt level		4.0		Volts
Input Low Current	Iil	-10	10	µA
W/ Pull-up Resistor		-200	-10	µA
Input high current	Iih	-10	10	µA
Output low voltage 2 mA buffer, IOL = 2mA 4 mA buffer, IOL = 4mA 8 mA buffer, IOL = 8mA 12 mA buffer, IOL = 12 mA	Vol		0.4	Volts
Output high voltage 2 mA buffer, IOH = -2mA 4 mA buffer, IOH = -4mA 8 mA buffer, IOH = -8mA 12 mA buffer, IOH = -12mA	Voh	2.4		Volts
High Impedance Leakage Current	Ioz	-10	10	µA
Device Quiescent Supply Current	Iccq		TBD	µA
Supply Current	Icc		TBD	mA
Power Dissipation	Pdis		TBD	mW
Input Capacitance	Cin		7	pF
Output or I/O Capacitance	Cout		10	pF

4.4 e88C311 AC Characteristics

(Vcc = 5V +/- 5%, Ta = 0 to 50° C)

4.4.1 Clock Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
CLK2 period	T101		20		15	ns
CLK2 high at 3.7V	T102	5		4		ns
CLK2 low at 0.8V	T103	5		4		ns
CLK2 rise time (0.8V to 3.7V)	T104		6		4	ns
CLK2 fall time (3.7V to 0.8V)	T105		6		4	ns
CLK2 to SYSCLK low	T106	4	9.5	3	7	ns
CLK2 high to SYSCLK high	T107	4	9	3	6	ns
ATSCLK period	T108	125	167	125	167	ns
ATSCLK high at 3.7V	T109	55*		55*		ns
ATSCLK low at 0.8V	T110	55*		55*		ns
ATSCLK rise time (0.8V to 3.7V)	T111		12		12	ns
ATSCLK fall time (0.8V to 3.7V)	T112		12		12	ns

*NOTE: Assuming an 8 MHz AT bus

4.4.2 Reset Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
RESET1- setup time to CLK2 rising edge	T201	14		10		ns
RESET3 active from CLK2 PHI2 rising edge	T202	5	10	4	10	ns
RESET3 inactive from CLK2 PHI2 rising edge	T203	5	10	4	10	ns
RESET3 pulse width	T204	80		80		CLK2
RESET4 active from CLK2 PHI2 rising edge	T206	5	17	4	13	ns
RESET4 inactive from CLK2 PHI2 rising edge	T207	5	17	4	13	ns
RESET4 pulse width	T208	80		80		CLK2
RST387 active from CLK2 PHI2 rising edge	T210	5	17	4	13	ns
RST387 inactive from CLK2 PHI2 rising edge	T211	5	17	4	13	ns
RST387 pulse width	T212	80		80		CLK2
RESET3 active from CLK2 rising edge	T213	5	17	4	13	ns
RST387 active from CLK2 rising edge	T214	5	17	4	13	ns
RESET2- Set up to CLK2 rising edge	T215	14		10		ns

4.4.3 AT Bus Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
BALE active from ATSCLK falling edge	T301		20		15	ns
BALE inactive from ATSCLK rising edge	T302		20		15	ns
COMMAND active from ATSCLK rising edge	T303		18		14	ns
COMMAND inactive from ATSCLK rising edge	T304		18		14	ns
XA0-XA16, XBHE valid from ATSCLK falling Edge	T305		18		14	ns
XA0-XA16, XBHE hold time after COMMAND invalid	T306	60		60		ns
LA17-LA23 valid from ATSCLK rising edge	T307		20		15	ns
LA17-LA23 hold time after COMMAND invalid	T308	60		60		ns
IOCS16- setup time to ATSCLK falling edge	T309	18		18		ns
IOCS16- hold time from ATSCLK falling edge	T310	10		10		ns
0WS- setup time to ATSCLK rising edge	T311		16		16	ns
0WS- hold time from ATSCLK rising edge	T312	10		10		ns
IOCHRDY setup time to rising edge of ATSCLK	T313	18		18		ns

AT Bus Cycle Timing (Cont.)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
IOCHRDY hold time from rising edge of ATSCLK	T314	10		10		ns
DBAM(4:0) valid from ATSCLK falling edge	T315		20		18	ns
DBAM(4:0) hold time after COMMAND invalid	T316	40		40		ns
DLE Valid from falling edge of ATSCLK	T317		20		18	ns
DLE hold time after COMMAND invalid	T318		5		5	ns
ROMCS- active from CLK2 PHI2 rising edge	T319	6	29	5	28	ns
ROMCS- inactive from CLK2 PHI1 falling edge	T320	5	26	4	24	ns
MEMCS16- set-up time to BALE falling edge	T321	20		20		ns
MEMCS16- hold time to BALE falling edge	T322	10		10		ns

4.4.4 DMA Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
HOLD valid from CLK2 rising edge	T401	5	24	4	19	ns
HOLD invalid from CLK2 rising edge	T402	5	24	4	19	ns
HLDA1 valid from HLDA valid	T403	5	20	4	15	ns
HLDA1 invalid from HOLD invalid	T404	5	20	4	15	ns
DBAM<4:0> valid from command valid	T405	7	24	6	22	ns
DBAM<4:0> invalid from command invalid	T406	7	24	6	22	ns
BNKSL<1:0> valid from command valid	T407	7	28	6	20	ns
BNKSL<1:0> invalid from command invalid	T408	7	28	6	20	ns
RASn-<1:0> valid from command valid	T409	6	22	5	20	ns
RASn-<1:0> invalid from command invalid	T410	6	22	5	20	ns
MA<10:8>, MAXD<7:0> valid from CLK2 rising edge	T411	6	22	5	20	ns
MA<10:8>, MAXD<7:0> invalid from CLK2 rising edge	T412	6	22	5	20	ns
CASn- valid from CLK2 rising edge	T413	6	22	5	20	ns
CASn- invalid from CLK2 rising edge	T414	6	22	5	20	ns

4.4.5 Cache Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
4.4.5.1 None-pipline Mode						
CALE high from CLK2 PHI1 rising edge	T501	6	20	5	18	ns
CALE low from CLK2 PHI2 rising edge	T502	6	20	5	18	ns
SRAMA2 valid from A2 valid	T503	6	22	4	20	ns
SRAMA2 valid from CLK2 PHI2 rising edge (128KB cache fill)	T504	6	25	5	24	ns
2nd SRAMA2 valid from CLK2 PHI2 rising edge (128KB cache fill)	T505	6	25	5	24	ns
CRD<1:0>- low from CLK2 PHI2 rising edge (direct map)	T506	6	18	5	14	ns
CRD<1:0>- high from CLK2 PHI1 rising edge (direct map)	T507	5	17	4	13	ns
CRD<1:0>- low from CLK2 PHI1 falling edge (two way)	T508	5	13	4	8	ns
CRD<1:0>- high from CLK2 PHI1 rising edge (two way)	T509	5	14	4	10	ns
READY- low from CLK2 PHI1 falling edge	T510	6	20	5	15	ns
READY- high from CLK2 PHI1 rising edge	T511	6	20	5	15	ns

CACHE CYCLE(Cont.)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
CBS<3:0>- valid from BE<3:0>- valid	T512	5	20	4	18	ns
CBS<3:0>- inactive from CLK2 PHI1 rising edge	T513	7	25	6	22	ns
CWE<1:0>- cache fill active from CLK2 PHI1 rising edge	T514	6	20	5	18	ns
CWE<1:0>- cache fill inactive from CLK2 PHI1 rising edge	T515	6	18	5	18	ns

4.4.5.2 Pipeline Mode

CALE low from CLK2 PHI2 rising edge	T516	6	20	5	18	ns
CALE high from CLK2 PHI1 rising edge	T517	6	20	5	18	ns
CRD<1:0>- low from CLK2 PHI2 rising edge	T518	6	18	5	14	ns
CRD<1:0>- high from CLK2 PHI1 rising edge	T519	5	17	4	13	ns
CRD<1:0>- high from CLK2 PHI2 rising edge (direct map)	T520	5	17	4	13	ns

4.4.6 DRAM Memory Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
DWE- active from CLK2 PHI1 rising edge	T601	6	20	5	18	ns
DWE- inactive from CLK2 PHI2 rising edge	T602	7	24	6	22	ns
RAS- inactive from CLK2 PHI2 rising edge (page miss precharge)	T603	6	22	5	20	ns
RAS- active from CLK2 PHI2 rising edge (page miss precharge)	T604	6	22	5	20	ns
CASBn- active from CLK2 PHI2 rising edge	T605	5	16	4	10	ns
CASBn- inactive from CLK2 PHI2 rising edge	T606	5	18	4	15	ns
MA<10:8>, MAXD<7:0> valid from CLK2 PHI2 rising edge	T607	6	22	5	20	ns
MA<10:8>, MAXD<7:0> invalid from CLK2 PHI2 rising edge	T608	6	22	5	20	ns
DLE valid after CLK2 rising edge	T609	6	20	5	18	ns
DLE invalid after CLK2 rising edge	T610	6	20	5	15	ns
DBAM<4:0> valid after CLK2 PHI2 rising edge	T611	7	24	6	22	ns
DBAM<4:0> invalid after CLK2 PHI1 rising edge	T612	7	24	6	22	ns

DRAM Memory Cycle Timing (Cont.)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
WDLE valid from CLK2 PHI1 rising edge	T613	7	25	6	22	ns
WDLE invalid from CLK2 PHI1 falling edge	T614	6	22	5	20	ns
BNKSL<1:0> from 80386 address valid	T615	7	28	6	24	ns
CWE<1:0>- (CPU write hit) valid from CLK2 PHI2 rising edge	T616	6	20	5	18	ns
CWE<1:0>- (CPU write hit) invalid from CLK2 PHI1 rising edge	T617	6	20	5	18	ns
MA<10:8>, MAXD<7:0> valid from CPU address valid	T618	6	22	5	20	ns

4.4.7 AT Style Refresh Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
HOLD active from CLK2 rising edge	T701	5	24	4	19	ns
HOLD inactive from CLK2 rising edge	T702	5	24	4	19	ns
REF- active from ATSCLK rising edge	T703		25		22	ns
REF- inactive from ATSCLK rising edge	T704		25		22	ns
MEMR-, SMEMR- active from rising edge of ATSCLK	T705		25		22	ns
MEMR-, SMEMR- inactive from rising edge of ATSCLK	T706		25		22	ns
RAS0-, RAS2- active from CLK2 rising edge	T707	6	22	5	20	ns
RAS0-, RAS2- inactive from CLK2 rising edge	T708	6	22	5	20	ns
RAS1-, RAS3- Active from CLK2 rising edge	T709	6	22	5	20	ns
RAS1-, RAS3- inactive from CLK2 rising edge	T710	6	22	5	20	ns
XA<23:0> valid from rising edge of ATSCLK	T711		25		22	ns
XA<23:0> invalid from rising edge of ATSCLK	T712		25		22	ns

4.4.7 AT Style Refresh Cycle Timing (Continued)

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
MA<10:8>, MAXD<7:0> valid from CLK2 rising edge	T713	6	22	5	20	ns
MA<10:8>, MAXD<7:0> invalid from CLK2 rising edge	T713	6	22	5	20	ns

4.4.8 Hidden, Burst Mode Refresh Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
RAS<3:0>- low from CLK2 rising edge	T801	6	22	5	20	ns
RAS<3:0>- high from CLK2 rising edge	T802	6	22	5	20	ns

4.4.9 Misc. Cycle Timing

	SYMBOL	25MHZ MIN	25MHZ MAX	33MHZ MIN	33MHZ MAX	UNIT
XDEN- valid from ATSCLK rising edge	T901		18		14	ns
XDEN- invalid from ATSCLK rising edge	T902		18		14	ns
FRSTADS valid after ADS- valid	T903		24		20	ns
DISMEM- setup time to CLK2 PHI1 falling edge	T904	12		9		ns
DISMEM- hold time from CLK2 PHI2 falling edge	T905	7		5		ns
NCACHE- setup time to CLK2 PHI1 falling edge	T906	12		9		ns
NCACHE- hold time from CLK2 PHI2 falling edge	T907	7		5		ns
NMI valid from CLK2 PHI2 rising edge	T908	7	24	5	18	ns
NMI invalid after XIOW- invalid	T909	6	28	5	20	ns
PARERR setup Time to CLK2 PHI2 falling edge	T910	12		10		ns
PARERR hold time from CLK2 PHI2 falling edge	T911	7		6		ns
LOCAL- setup time from CLK2 PHI1 falling edge	T912	12		9		ns
LOCAL- hold time from CLK2 PHI2 falling edge	T913	7		5		ns

5. e88C311 TIMING DIAGRAMS

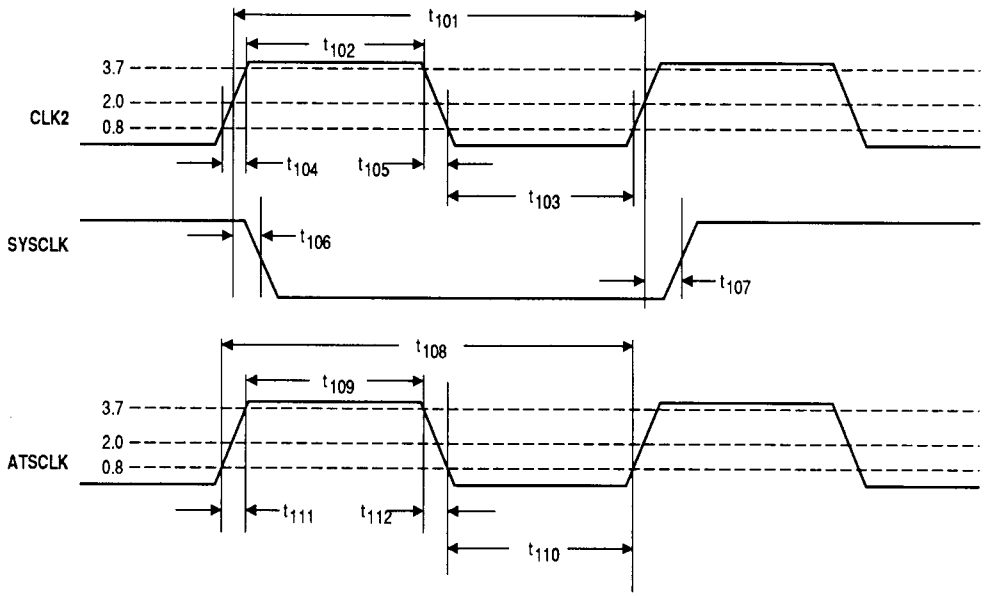


Figure 5-1. Clock Timing

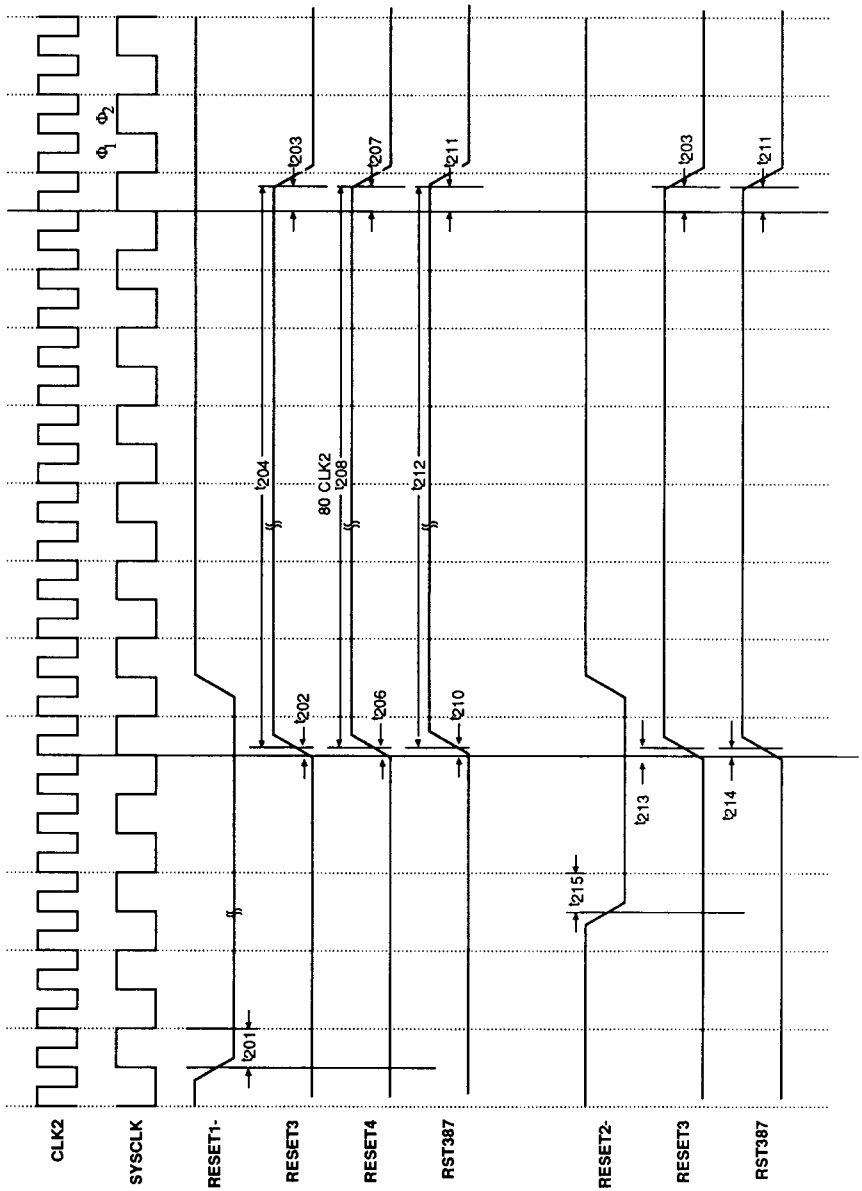


Figure 5-2. Reset Timing

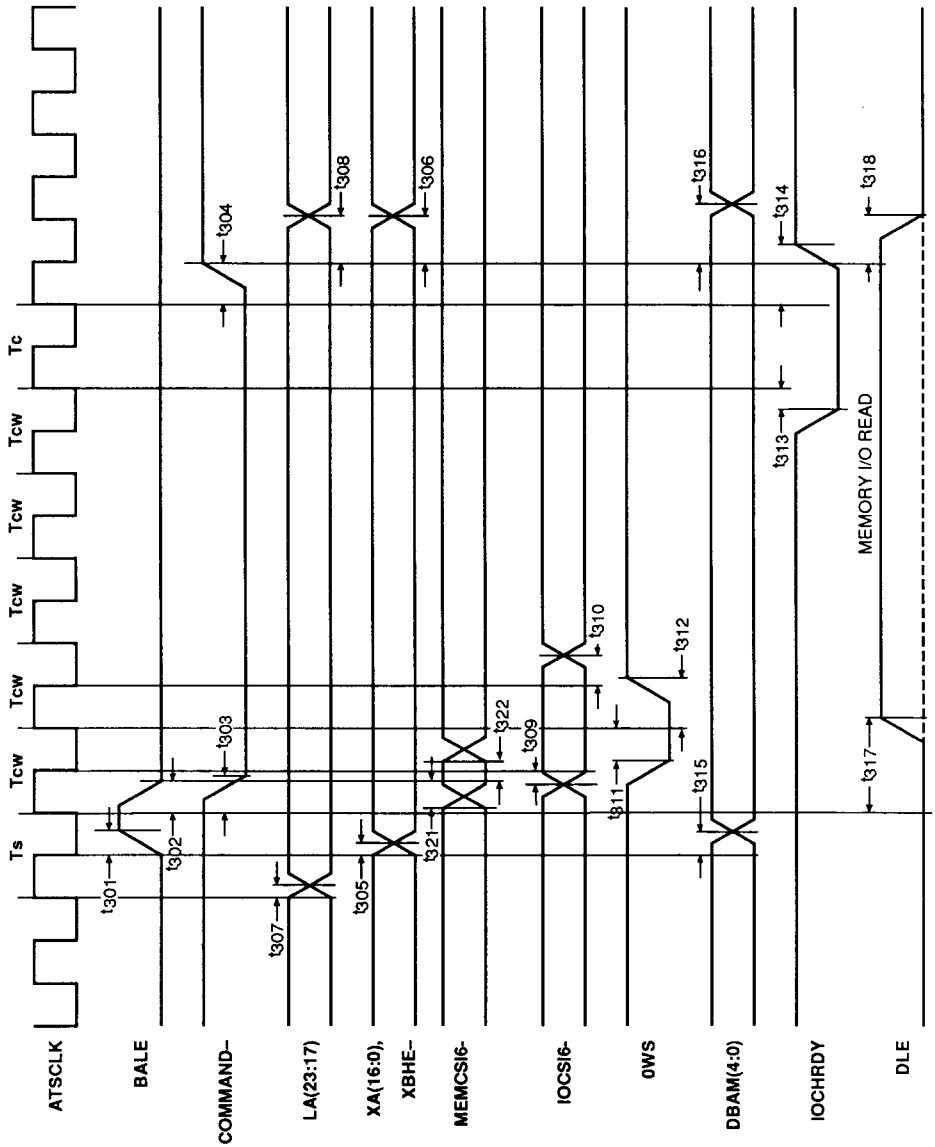


Figure 5-3. AT Bus Timing

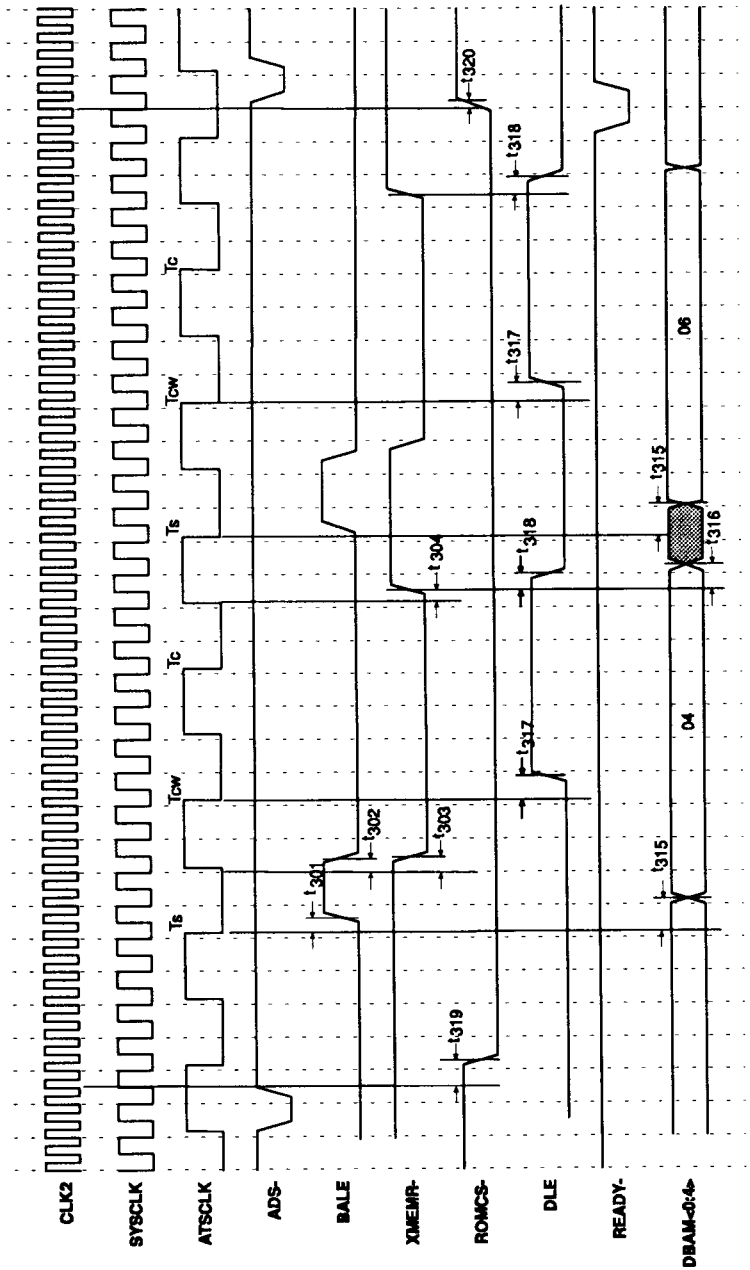


Figure 5-4. ROM BIOS Read Cycle, ATSCLK = SYSCLK/4

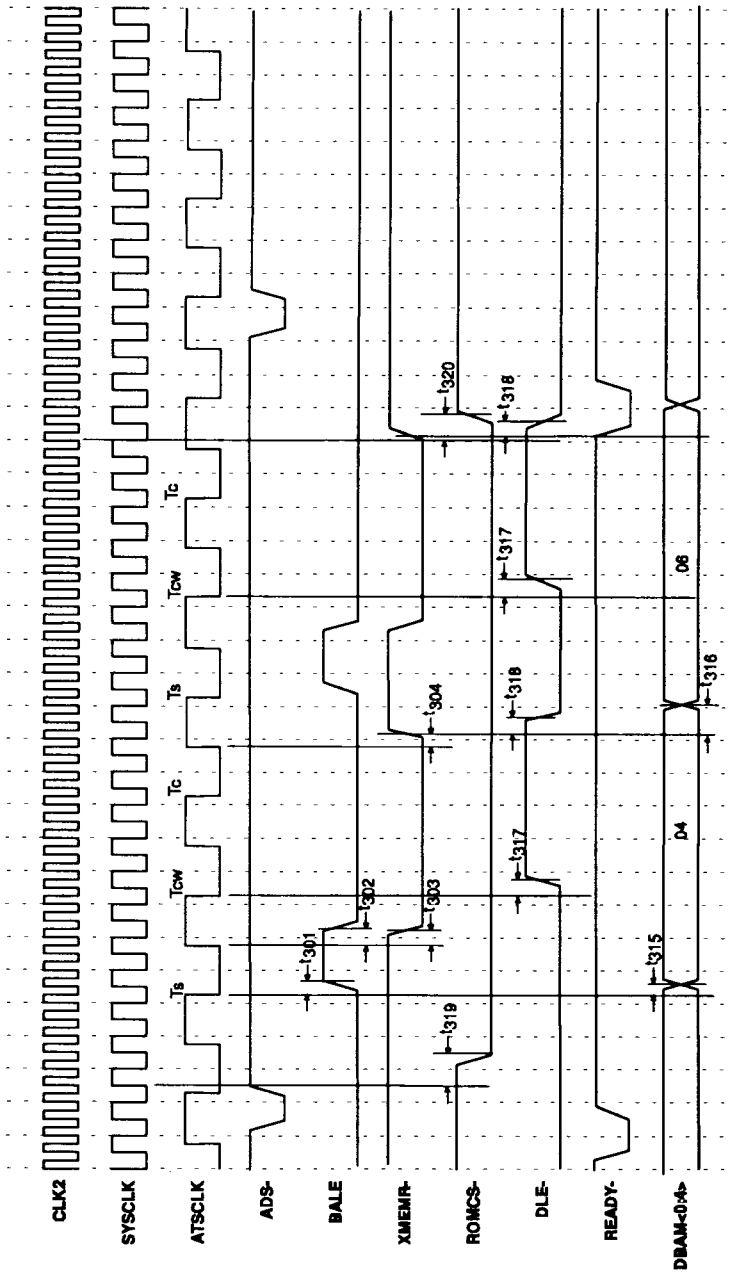


Figure 5-5. ROM BIOS Read Cycle, ATSCLK = SYSCLK/3, 16-bit

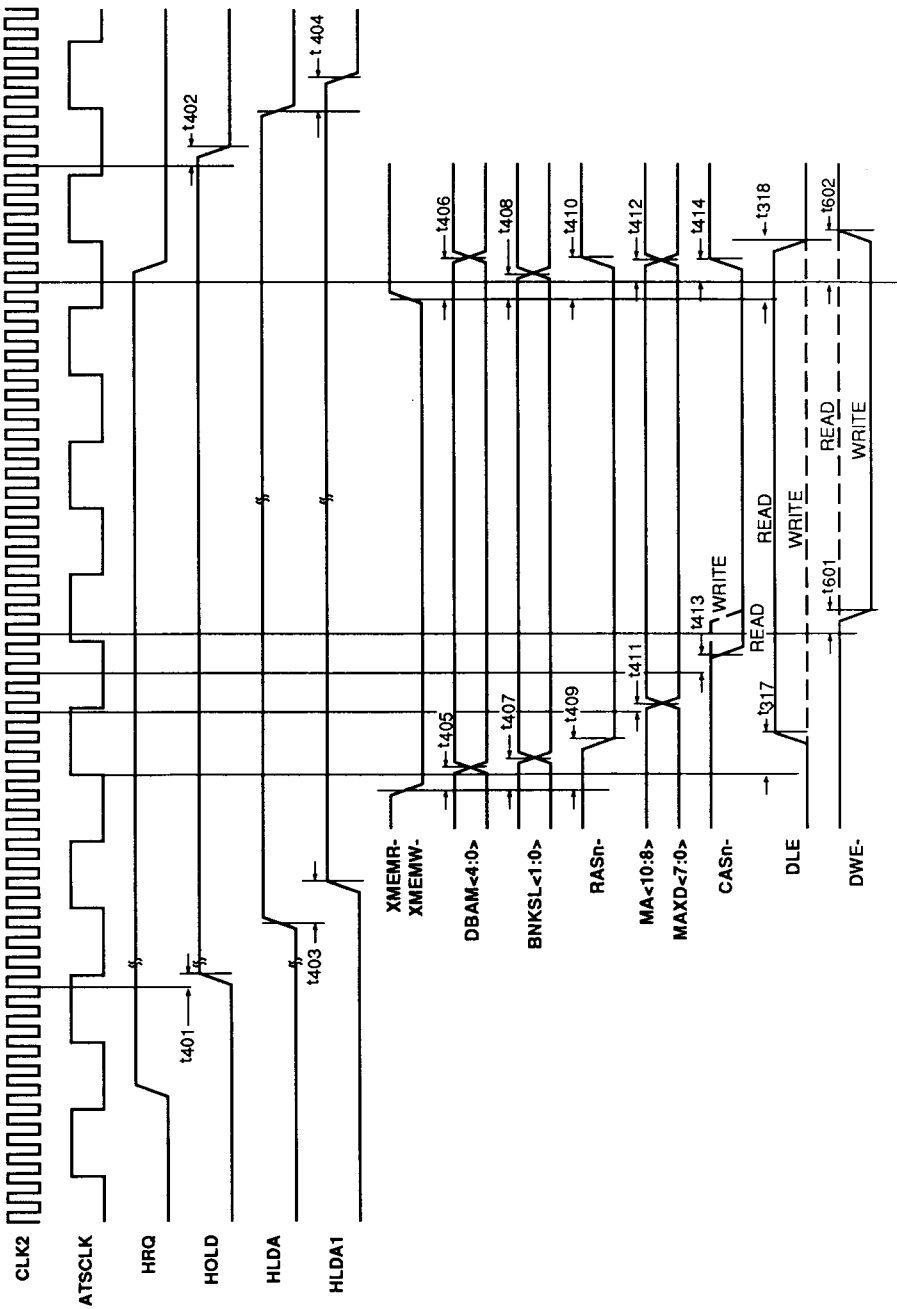


Figure 5-6. DMA Timing

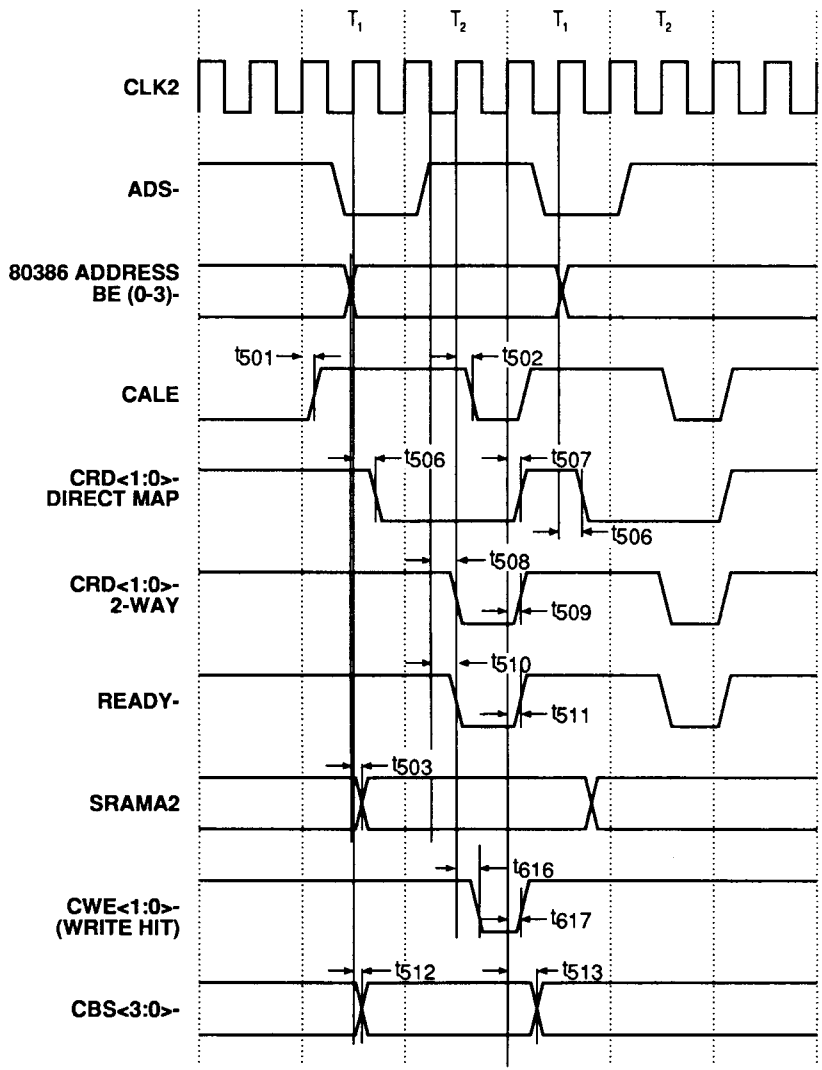


Figure 5-7. Cache Hit, Non-Pipelined, 0 WS SRAM

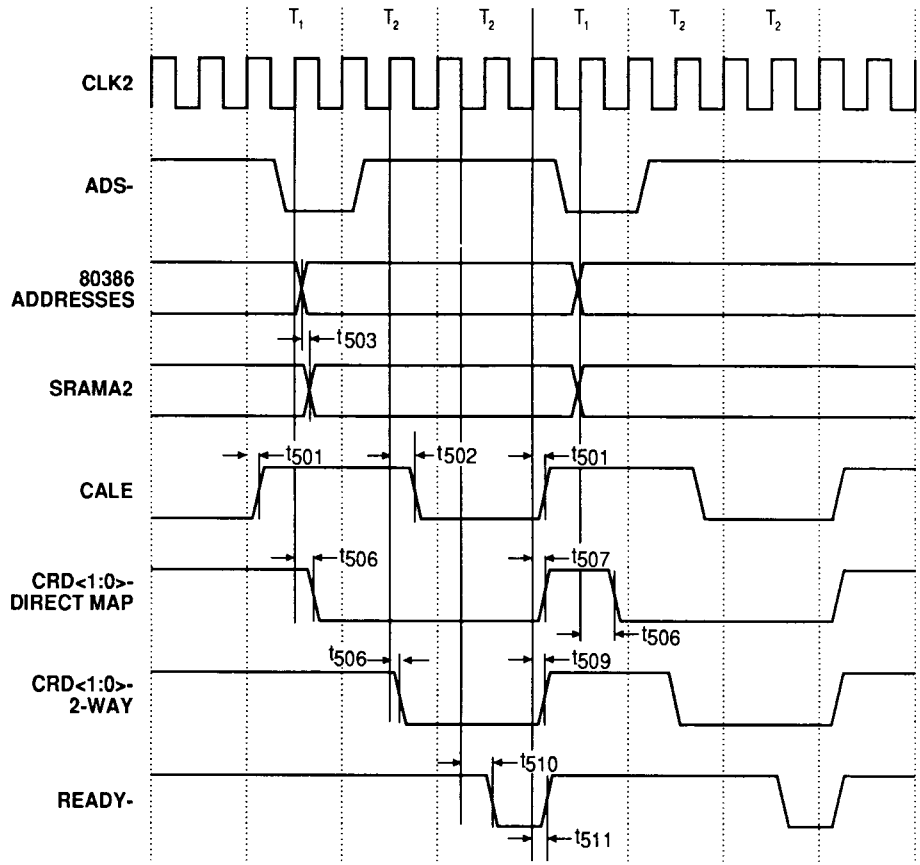


Figure 5-8. Cache Read Hit, Non-Pipelined, 1 WS SRAM

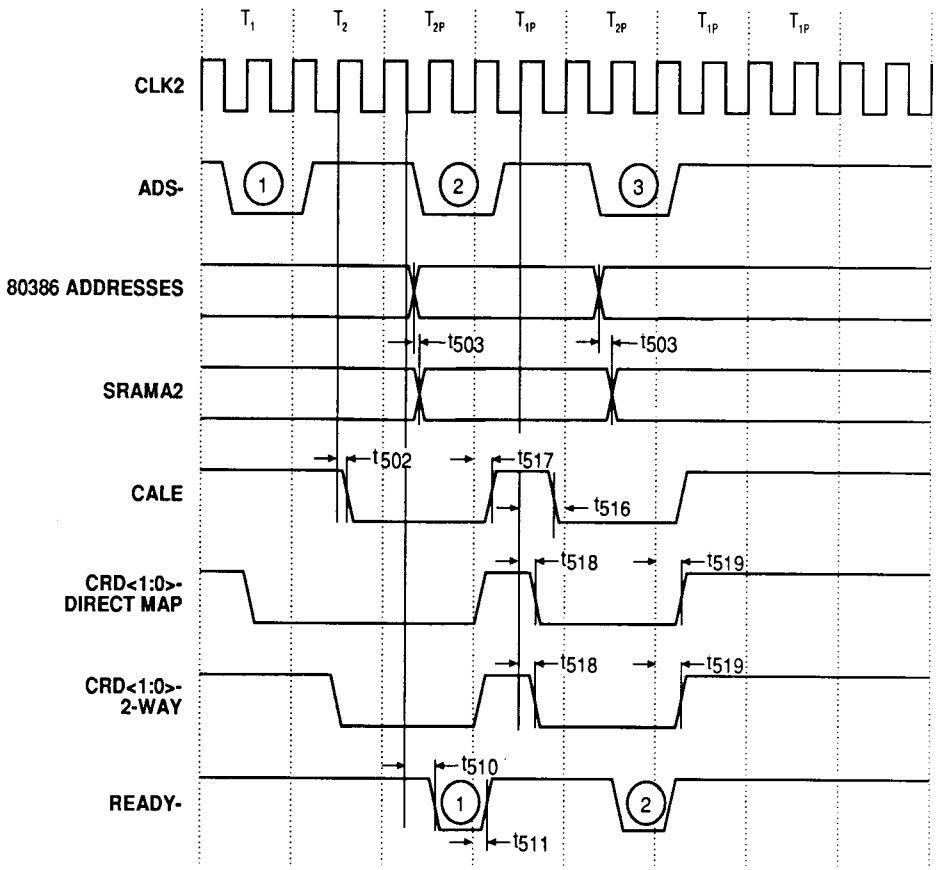


Figure 5-9. Cache read Hit, 0WS SRAM, Non-Pipelined Cycle followed by a Pipelined Cycle

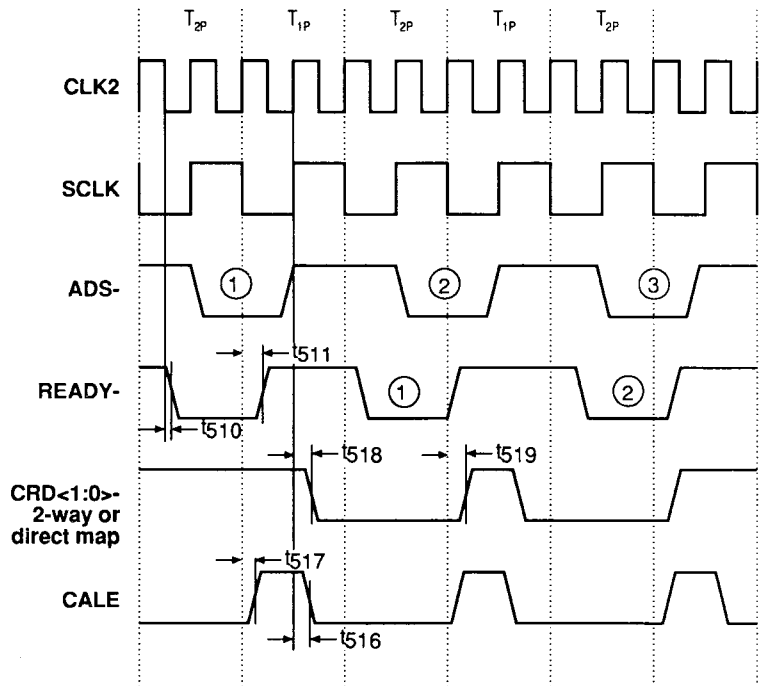


Figure 5-10. Cache Read Hit, 0/1 WS SRAM Pipelined Mode

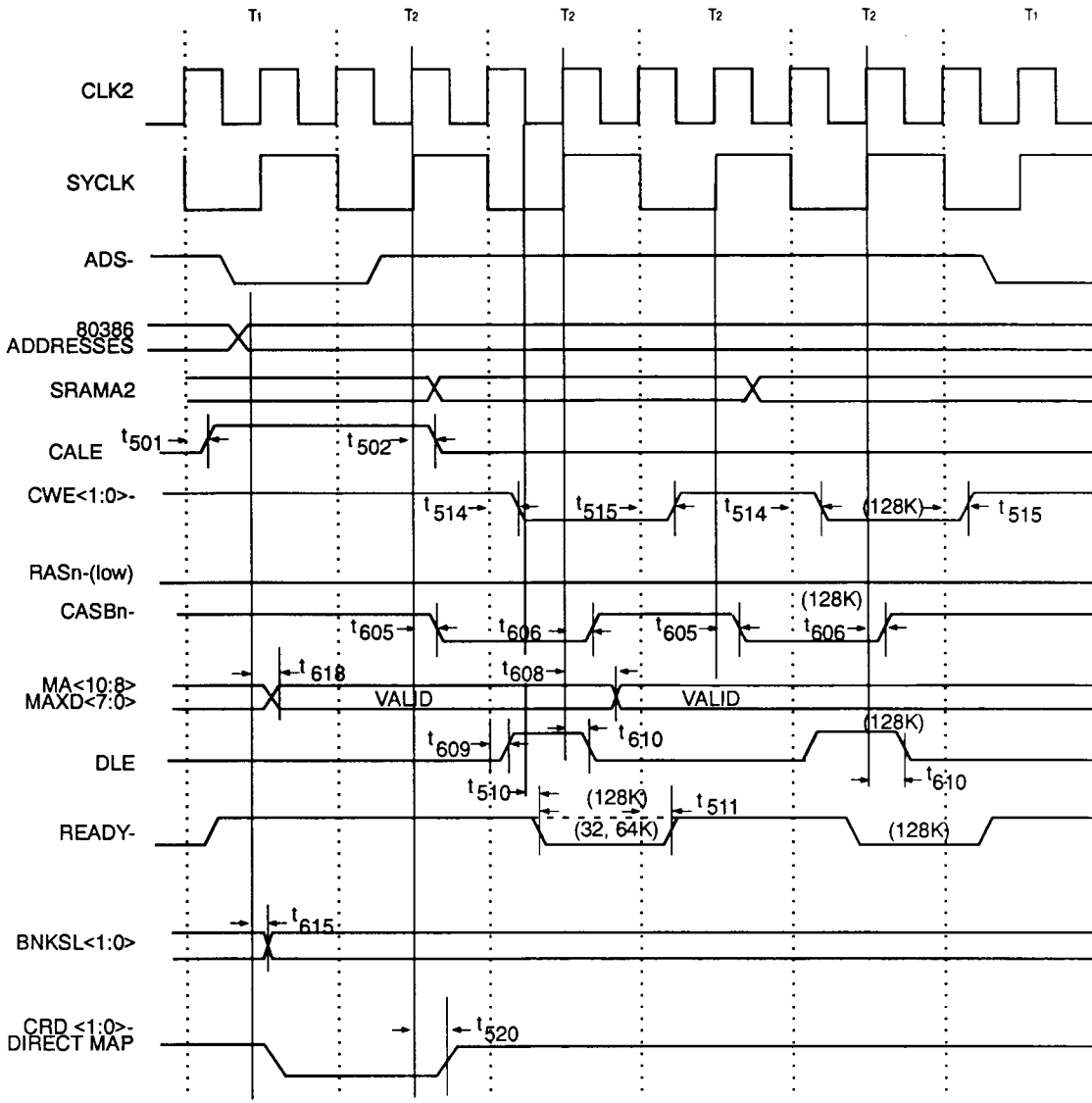


Figure 5-11. Cache read Miss, Page Hit, 0 WS SRAM, 0 WS DRAM, 32/64/128KB Non-Pipelined Mode

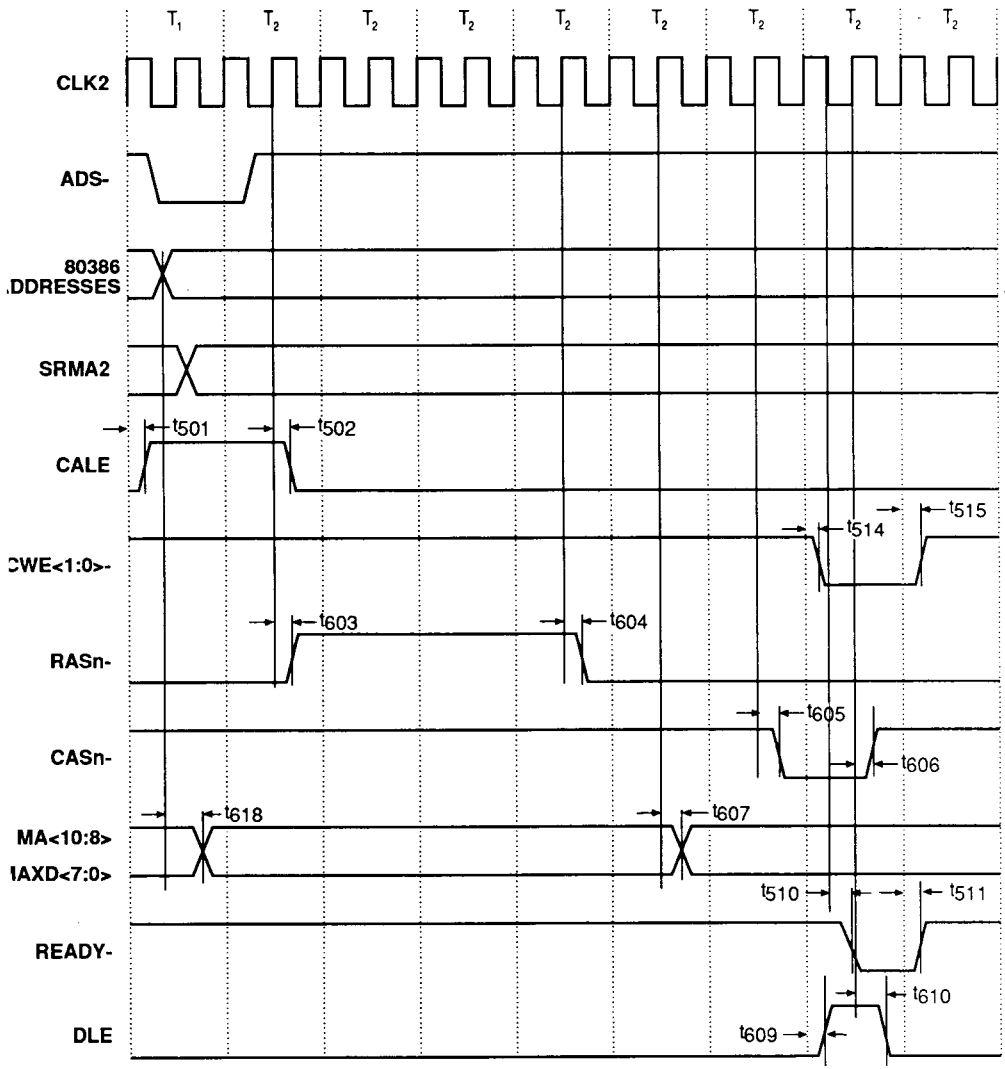


Figure 5-12. Cache Read Miss, Page Miss, 0WS SRAM, 0WS DRAM, Non-Pipelined Mode

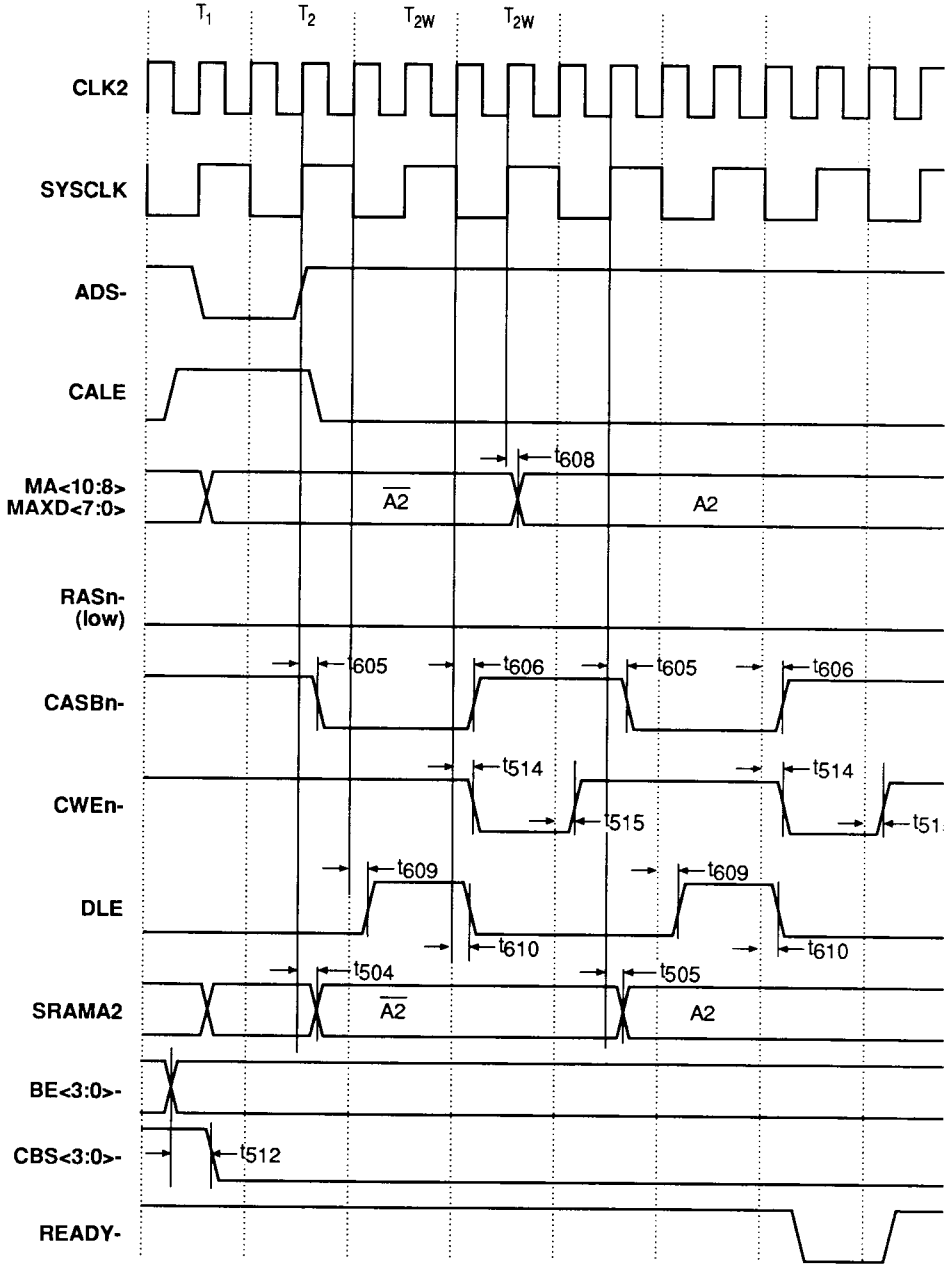


Figure 5-13. Cache Read miss, Page Hit, 0/1 WS SRAM, 1 WS DRAM, 128 KB Cache Size, Non-Pipelined Mode

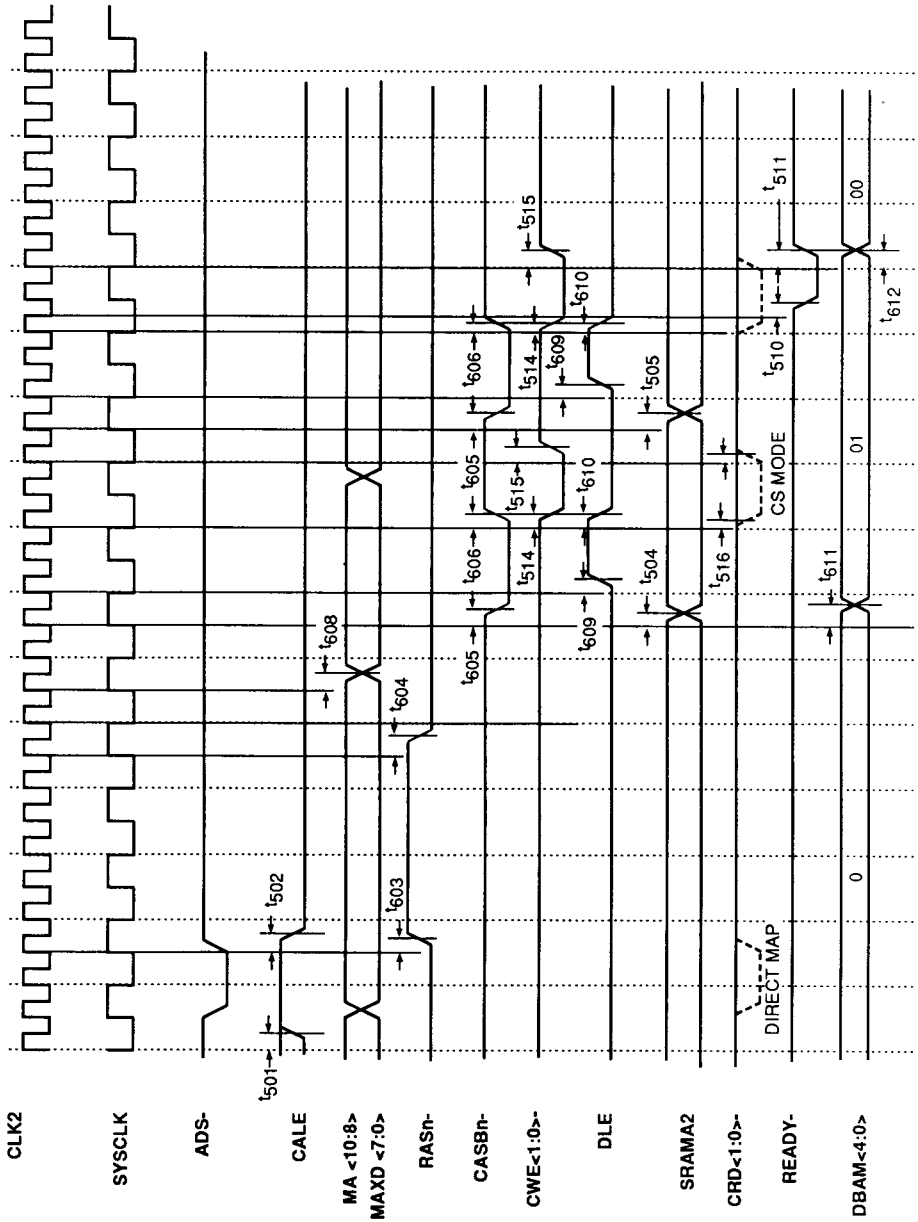


Figure 5-14. Cache Read Miss, Page Miss, 0 WS SRAM, 1 WS DRAM, 128KB Cache Size

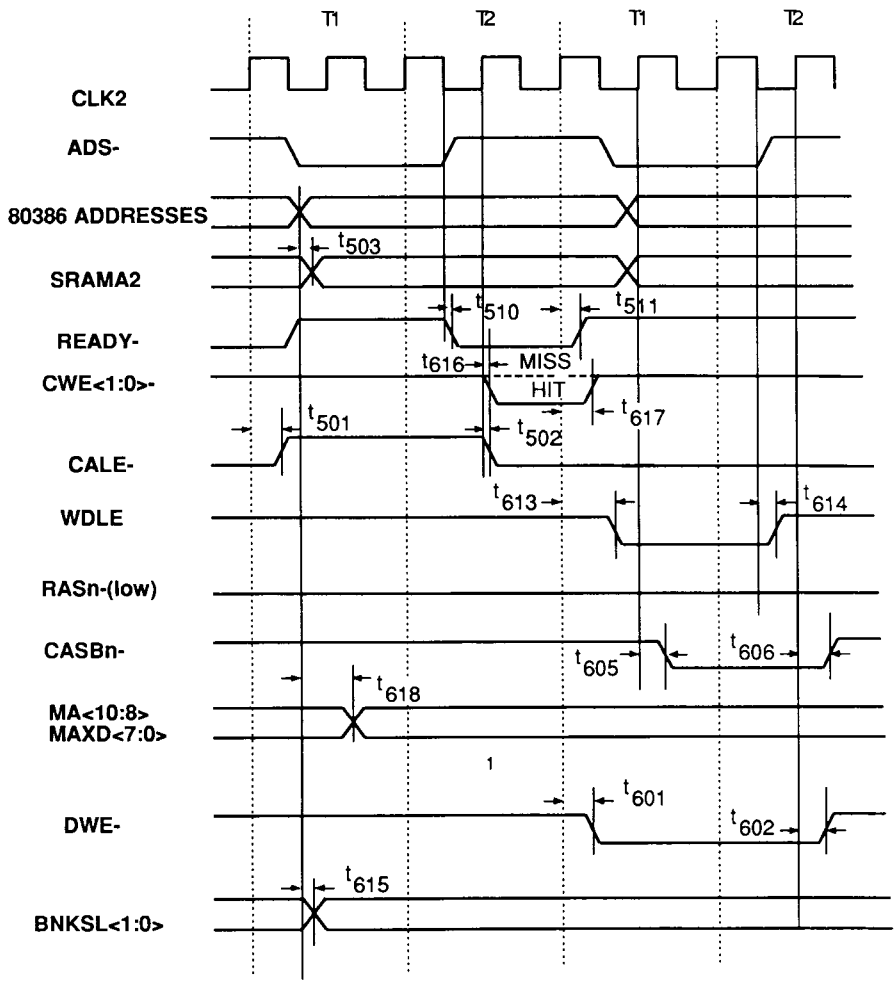


Figure 5-15. CPU Write, Page HIT, 0 WS SRAM, 0 WS DRAM, Non-Pipeline Mode

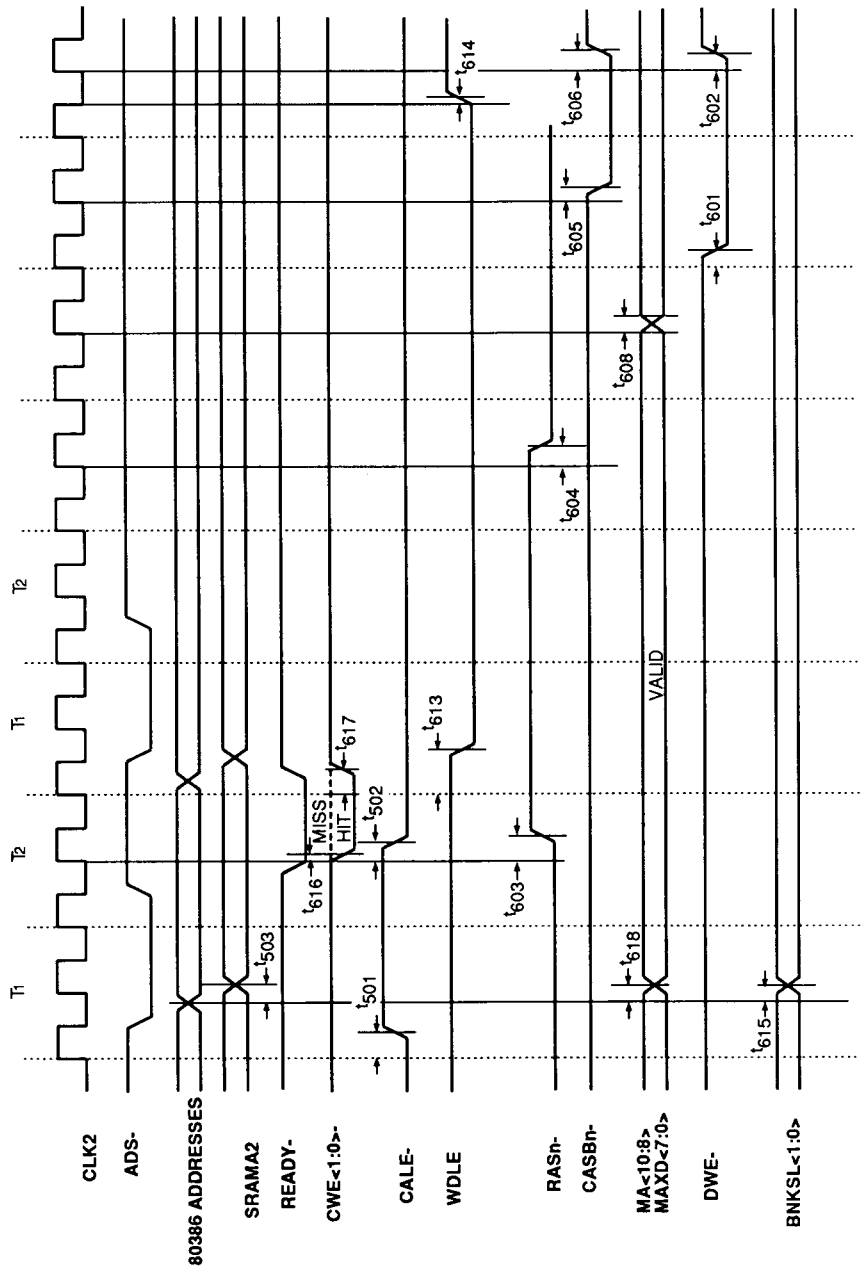


Figure 5-16. CPU Write, Page Miss, 0 WS SRAM, 0 WS DRAM, Non-Pipeline Mode

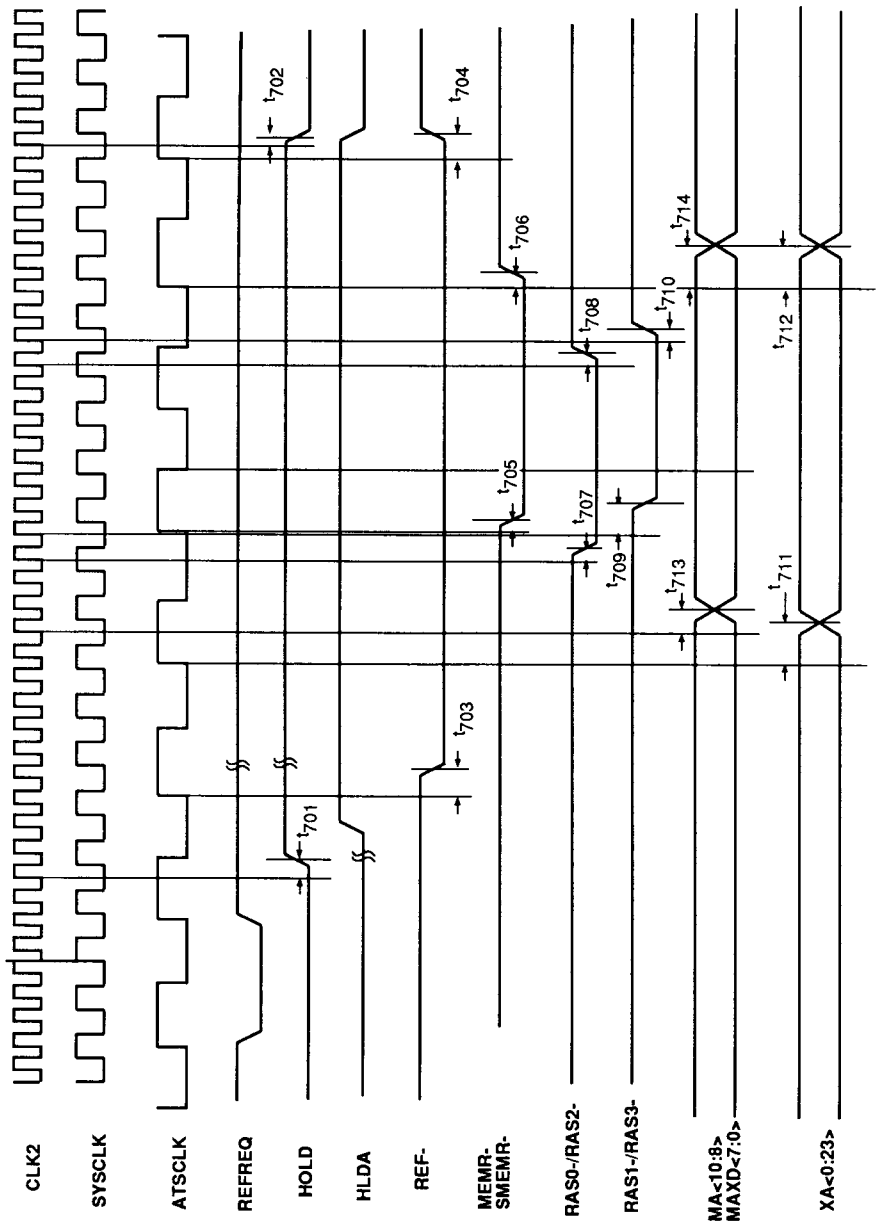


Figure 5-17. AT Refresh Timing

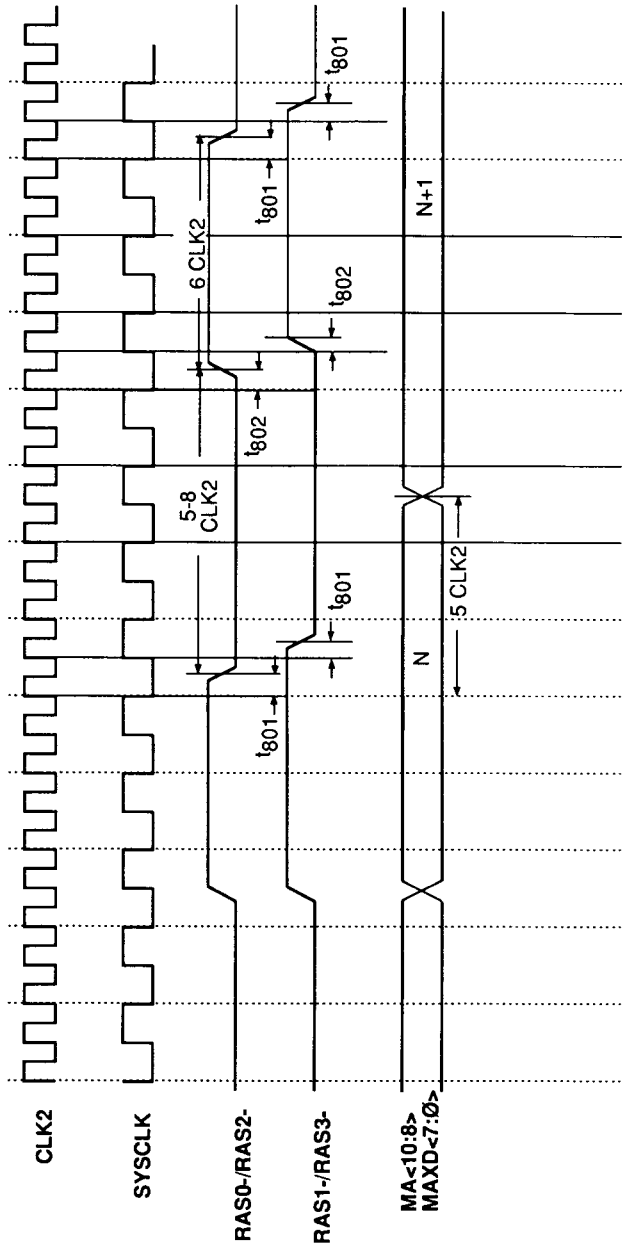


Figure 5-18. Local DRAM Burst Mode Refresh Cycle

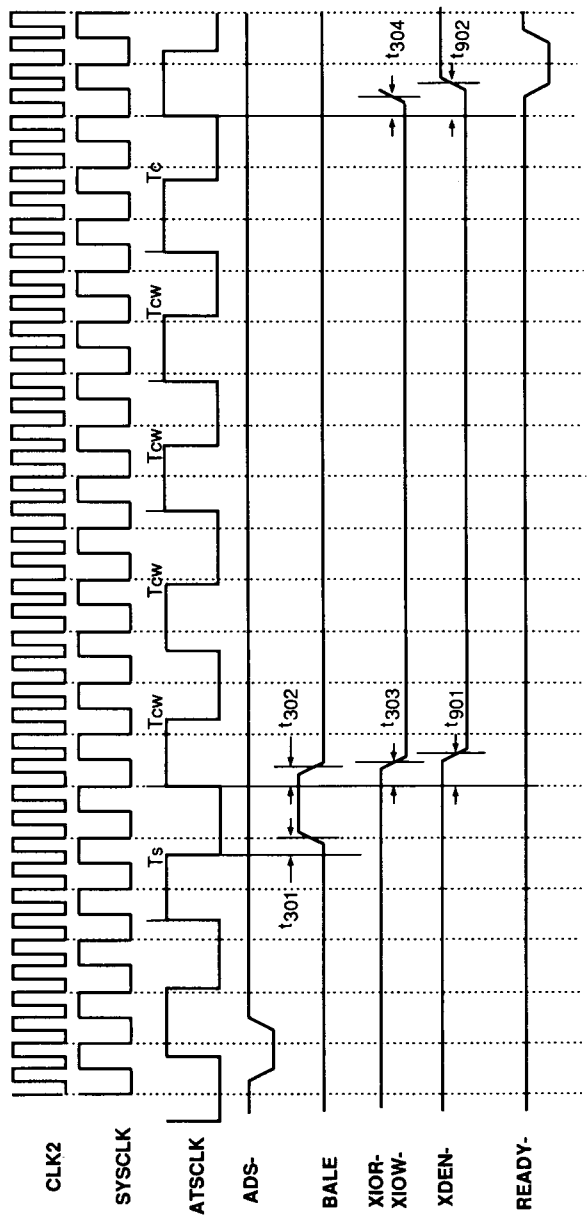


Figure 5-19. XDEN- Timing

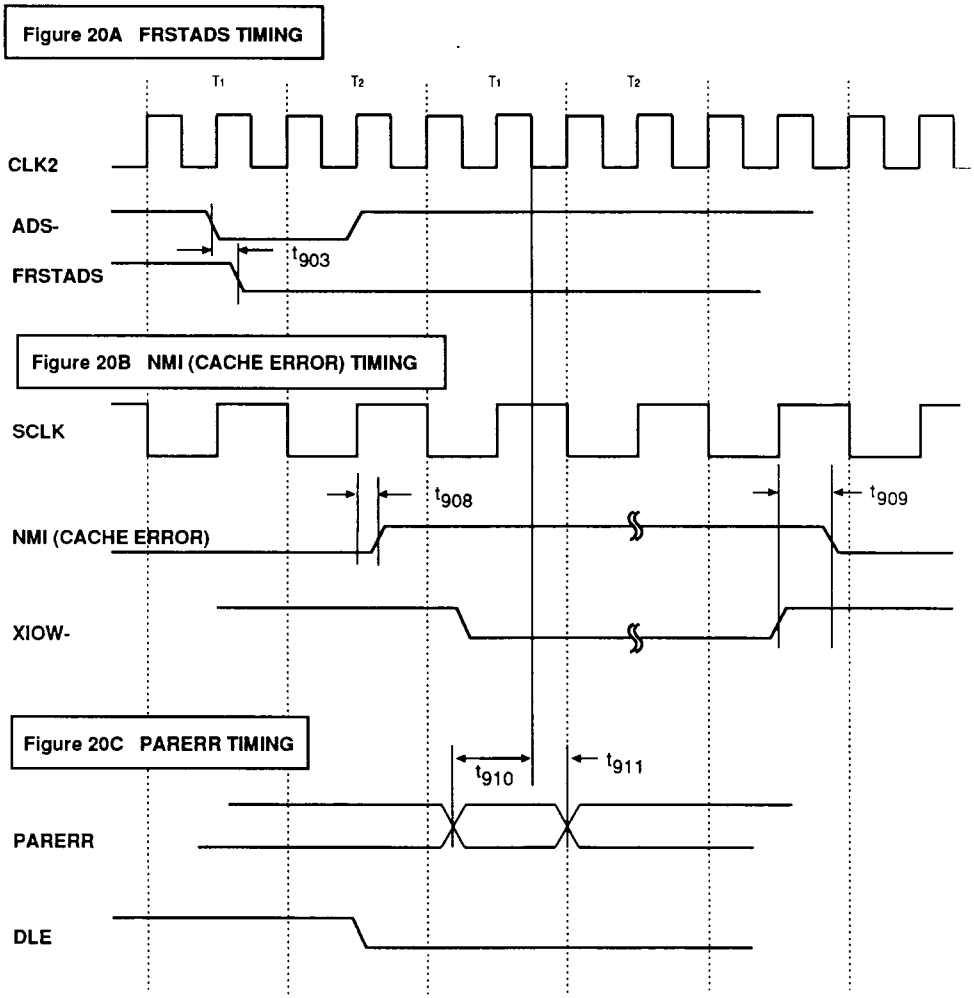


Figure 5-20A. FRSTADS Timing

Figure 5-20B. NMI (Cache Error) Timing

Figure 5-20C. PARERR Timing

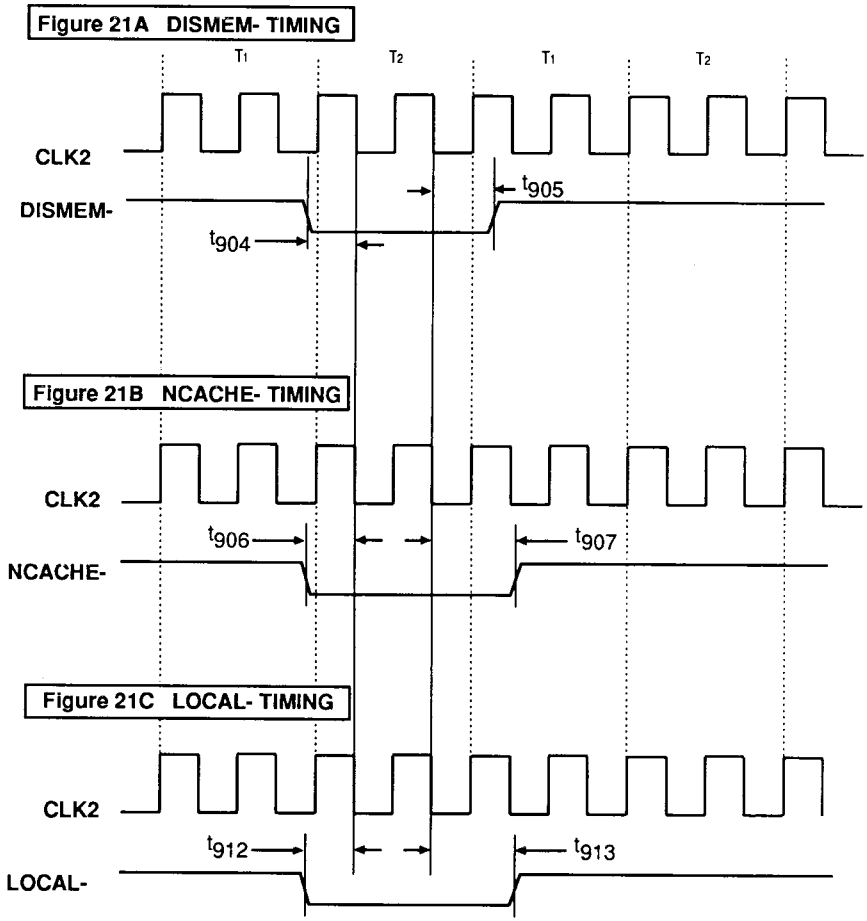
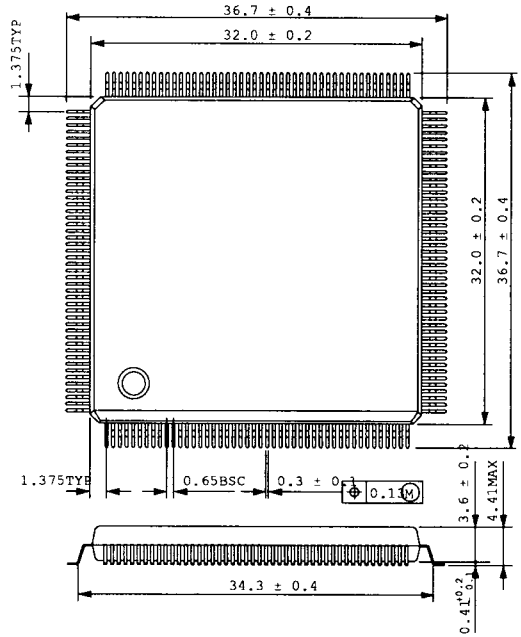


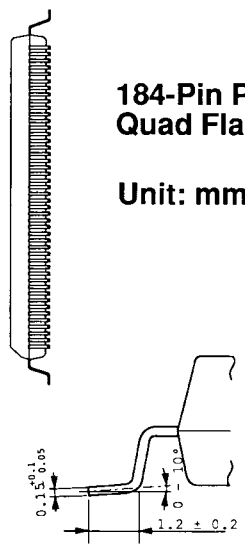
Figure 5-21A. DISMEM- Timing

Figure 5-21B. NCACHE- Timing

Figure 5-21C. LOCAL Timing

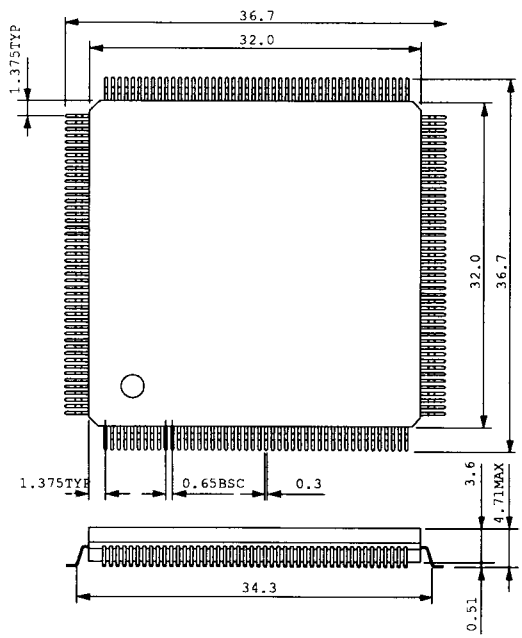
6. e88C311 MECHANICAL INFORMATION

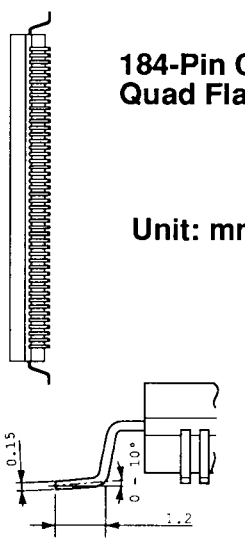




184-Pin Plastic Quad Flat Package

Unit: mm





184-Pin Ceramic Quad Flat Package

Unit: mm

Figure 6-1. e88C311: 184-Pin Quad Flat Package

6.1 e88C311 Pin Lists

6.1.1 Numerical

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	47	VSS	93	VSS	139	VSS
2	ATSCLK	48	CRD0-	94	CLK2IN	140	VDD
3	XA5	49	CRD1-	95	CLK2	141	RESET1-
4	XA6	50	CBS0-	96	ADS-	142	GATEA20
5	XA7	51	CBS1-	97	READY-	143	XDEN-
6	XA8	52	CBS2-	98	WR-	144	ROMCS-
7	XA9	53	CBS3-	99	DC-	145	ROM8-
8	VSS	54	CWE0-	100	MIO-	146	MASTER-
9	XA10	55	CWE1-	101	BE3-	147	IOCHCK-
10	XA11	56	CALE	102	BE2-	148	RAS3-
11	XA12	57	SRAMA2	103	BE1-	149	RAS2-
12	XA13	58	VSS	104	BE0-	150	RAS1-
13	XA14	59	LA18	105	A8	151	RAS0-
14	XA15	60	LA19	106	A7	152	CASB3-
15	NCACHE-	61	LA20	107	A6	153	CASB2-
16	IOCS16-	62	LA21	108	A5	154	CASB1-
17	MEMCS16-	63	LA22	109	A4	155	CASB0-
18	RESET2-	64	LA23	110	A3	156	BNKSL1
19	LOCAL-	65	A31	111	A2	157	BNKSL0
20	DISMEM-	66	A30	112	XMEMW-	158	MA10
21	HRQ	67	A29	113	XMEMR-	159	MA9
22	TMROUT	68	A28	114	XBHE-	160	VSS
23	VDD	69	VDD	115	VDD	161	VDD
24	VSS	70	VSS	116	VSS	162	VSS
25	VSS	71	VSS	117	VSS	163	VSS
26	VSS	72	A27	118	SYSCLK	164	MA8
27	IOCHRDY	73	A26	119	387RDY-	165	MAXD7
28	0WS-	74	A25	120	RST387	166	MAXD6
29	XA16	75	A24	121	PARERR	167	MAXD5
30	LA17	76	A23	122	FRSTADS	168	MAXD4
31	BALE	77	A22	123	DBAM0	169	MAXD3
32	AEN	78	A21	124	DBAM1	170	MAXD2
33	OSC119	79	CPUA20	125	VSS	171	MAXD1
34	ADSTB8	80	A19	126	DBAM2	172	MAXD0
35	ADSTB16	81	A18	127	DBAM3	173	DWE-
36	REFREQ	82	A17	128	DBAM4	174	SMEMR-
37	TMRGATE	83	A16	129	DLE	175	SMEMW-
38	INTA-	84	A15	130	WDLE	176	VSS
39	SPKR	85	A14	131	AEN1-	177	XA0
40	LOCK-	86	A13	132	AEN2-	178	XA1
41	HLDA	87	A12	133	HLDA1	179	XA2
42	NMI	88	A11	134	REF-	180	XA3
43	NA-	89	A10	135	RESET4	181	XA4
44	HOLD	90	A9	136	XIOW-	182	ATCLK2
45	RESET3	91	VSS	137	XIOR-	183	ATCLK1
46	VDD	92	VDD	138	VDD	184	VDD

6.1.2 Alphabetical

Name	Pin	Name	Pin	Name	Pin	Name	Pin
A10	89	CASB0-	155	MASTER-	146	VSS	1
A11	88	CASB1-	154	MAXD0	172	VSS	8
A12	87	CASB2-	153	MAXD1	171	VSS	24
A13	86	CASB3-	152	MAXD2	170	VSS	25
A14	85	CBS0-	50	MAXD3	169	VSS	26
A15	84	CBS1-	51	MAXD4	168	VSS	47
A16	83	CBS2-	52	MAXD5	167	VSS	58
A17	82	CBS3-	53	MAXD6	166	VSS	70
A18	81	CLK2	95	MAXD7	165	VSS	71
A19	80	CLK2IN	94	MEMCS16-	17	VSS	91
A2	111	CPUA20	79	MIO-	100	VSS	93
A21	78	CRD0-	48	NA-	43	VSS	116
A22	77	CRD1-	49	NCACHE-	15	VSS	117
A23	76	CWE0-	54	NMI	42	VSS	125
A24	75	CWE1-	55	OSC119	33	VSS	139
A25	74	DBAM0	123	PARERR	121	VSS	160
A26	73	DBAM1	124	RAS0-	151	VSS	162
A27	72	DBAM2	126	RAS1-	150	VSS	163
A28	68	DBAM3	127	RAS2-	149	VSS	176
A29	67	DBAM4	128	RAS3-	148	WDLE	130
A3	110	DC-	99	READY-	97	WR-	98
A30	66	DISMEM-	20	REF-	134	XA0	177
A31	65	DLE	129	REFREQ	36	XA1	178
A4	109	DWE-	173	RESET1-	141	XA10	9
A5	108	FRSTADS	122	RESET2-	18	XA11	10
A6	107	GATEA20	142	RESET3	45	XA12	11
A7	106	HLDA	41	RESET4	135	XA13	12
A8	105	HLDA1	133	ROM8-	145	XA14	13
A9	90	HOLD	44	ROMCS-	144	XA15	14
ADS-	96	HRQ	21	RST387	120	XA16	29
ADSTB16	35	INTA-	38	SMEMR-	174	XA2	179
ADSTB8	34	IOCHCK-	147	SMEMW-	175	XA3	180
AEN	32	IOCHRDY	27	SPKR	39	XA4	181
AEN1-	131	IOCS16-	16	SRAMA2	57	XA5	3
AEN2-	132	LA17	30	SYSCLK	118	XA6	4
ATCLK1	183	LA18	59	TMRGATE	37	XA7	5
ATCLK2	182	LA19	60	TMROUT	22	XA8	6
ATSCLK	2	LA20	61	VDD	23	XA9	7
BALE	31	LA21	62	VDD	46	XBHE-	114
BE0-	104	LA22	63	VDD	69	XDEN-	143
BE1-	103	LA23	64	VDD	92	XIOR-	137
BE2-	102	LOCAL-	19	VDD	115	XIOW-	136
BE3-	101	LOCK-	40	VDD	138	XMEMR-	113
BNKSL0	157	MA10	158	VDD	140	XMEMW-	112
BNKSL1	156	MA8	164	VDD	161	0WS-	28
CALE	56	MA9	159	VDD	184	387RDY-	119

e88C312 DATA CONTROLLER

An Overview

The e88C312 data controller controls the interface between the CPU data bus (D<31:0>), the local or main memory data bus (MD<31:0>), and the local system data bus (LSD<15:0>). The local system data bus can be connected to the AT data bus (SD<15:0>) through external buffers or directly bypassing the external buffers. In the latter case, the local system data bus LSD<15:0> is the same as the AT data bus SD<15:0>. The lower byte of the local system data bus (LSD<7:0>) is also called the peripheral data bus and is connected to all on-board peripherals. The BIOS EPROM (16-bit) resides on the LSD<15:0> bus. In the case where a single 8-bit EPROM is used in the system, the BIOS EPROM resides on the LSD<7:0> bus.

The e88C312 data buffer also implements byte alignment and byte swapping for data transfers where the source and target are of different bus widths. In order to maintain data integrity, the e88C312 generates a parity bit for each byte of data written into local memory. When data is read from the local memory, the e88C312 regenerates the parity bits for each data byte and compares then against the parity bits read from the memory array. If there is a mismatch indicating a parity error condition, the e88C312 will activate an error signal (PARERR) to prompt the e88C311 to take proper actions.

In order to simplify on-board I/O port designs, two serial port selects (SERCS1, SERCS2-, one parallel port select (PARCS-) and two software programmable chip selects (PGCS0-, PGCS1-) are implemented in the e88C312. In addition, the e88C312 also provides the math-coprocessor detection and interface logic for the Intel 80387 and the Weitek WTL3167.

7. FUNCTIONAL DESCRIPTION

The e88C312 can be divided into the following functional modules as shown in the block diagram.

Action Decode and Control
Data Transfer Logic
Parity Handler
Timer Clock
Math Coprocessor Interface Logic

7.1 .e88C312 Action Decode and Control

The activities within the e88C312 are initiated by the 5-bit action codes (DBAM<4:0>) which are generated by the e88C311. The action codes determine what the current bus cycle is and prompts the e88C312 to control the direction of data flow by decoding DBAM<4:0> together with HLDA1, AEN1, XBHE-, XA1, XA0 and REF-. Table 1.1 below summarizes the bus cycle definition. The detailed definition of the action codes are given in Tables 1.2 through 1.4.

The SDIR1 and SDIR0 outputs are decoded to support the on-board optional bidirectional buffers which interface the local I/O bus (LSD<15:0>) to the AT SD<15:0> bus. When high, these outputs direct the local bus to the AT bus and vice versa when they are low. In the absence of these bidirectional buffers, SD<15:0> outputs may be directly connected to the AT bus. The BDIR output is active (high) during CPU cycles, DMA cycles or Refresh cycles and drives the XA<16:1> address bus onto the system address bus SA<16:1>. During Master cycles, the BDIR output is low and the XA<16:1> address bus is driven by the system address bus SA<16:1>.

7.1.1 Port Select Logic

Embedded in the Action Decode and Control module is the port select logic. The outputs associated with this sub-module are the peripheral chip selects: CS8042-, SERCS1-, SERCS2-, PARCS-, PGCS1-, PGCS0- and the Real Time Clock Address Strobe signal RTCAS. The on-chip implementation of these outputs eliminates the necessity of on-board glue logic generally required for external decoding of these functions. In addition, two programmable chip selects, PGCS1- and PGCS0- are implemented to provide greater flexibility for the system/board design. These chip selects can be defined through the e88C311 configuration registers.

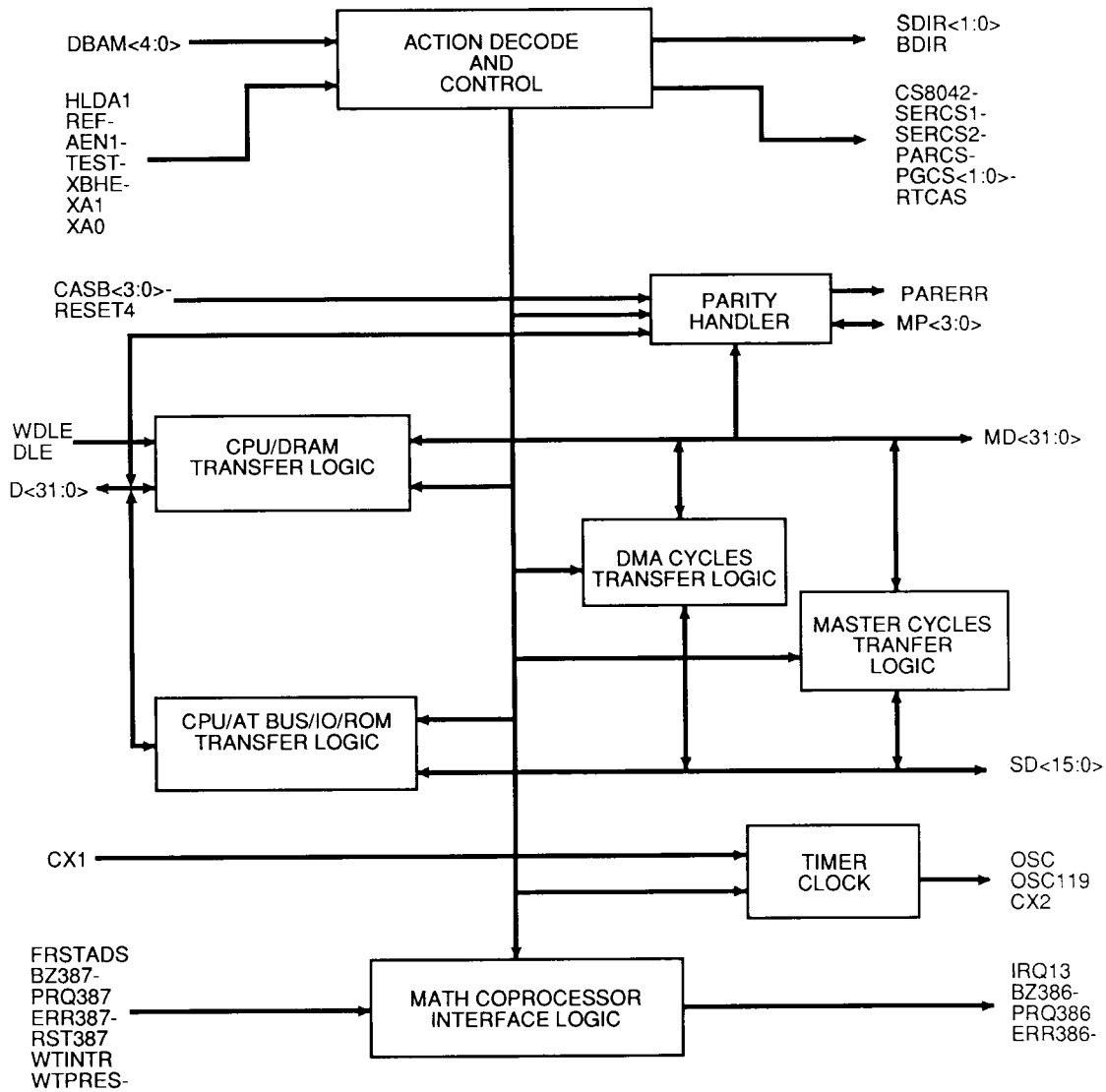


Figure 7-1. e88C312 Block Diagram

Table 7-1. Bus Cycle Definition (DBAM <4:0> in HEX format)

HLDA1	DBAM<4:0>	Bus Cycle	Source	Dest.
X	00	DEFAULT	-	-
X	02 - 03	RESERVED	-	-
0	01	CPU Read Local Memory	MD	D
0	04 - 07	CPU Read Local I/O or ROM	SD	D
0	08	CPU Write Local Memory	D	MD
		CPU Write AT	D	SD
0	09 - 0B	CPU Write AT or Local I/O	D	SD
0	0C - 0F	CPU Read AT	SD	D
1	01	Master Write Local Memory or	SD	MD
		Master Write Local I/O, AT Memory, AT I/O	-	-
1	04 - 05	Master Read Local Memory	MD	SD
1	06	Master Read Local ROM or I/O	-	-
1	07	Master Read AT Memory or AT I/O	-	-
1	08	DMA Write Local Memory or	SD	MD
		8-bit DMA Write AT Memory High Byte		
		(Byte-Swap Operation)	SD<7:0>	SD<15:8>
1	09	DMA Read Local ROM	-	-
1	0A	DMA Read AT Memory	-	-
1	0B	8-bit DMA Read AT Memory High Byte		
		(Byte-Swap Operation)	SD<15:8>	SD<7:0>
1	0C - 0F	DMA Read Local Memory	MD	SD
X	10 - 16	CPU Write Peripherals	D	SD
X	17	CPU Write, Clear 387 Busy	-	-
X	18 - 1D	CPU Read Peripherals	SD	D
X	1E	CPU Read Configuration Register 4Dh	e88C312	D & SD
X	1F	CPU Write Configuration Register 49h	D	SD

Note: (-) In the Source and Destination columns, this indicates that e88C312 does not handle the data transfer, i.e., either there is no data transfer involved, or the transfer takes place external to the e88C312.

(X) Denotes Don't Care.

Table 7-2. Action Mode Codes For CPU Cycles

HLDA1	DBAM<4:0>	CYCLE	OPERATION
0	00000	DEFAULT	
0	00001	CPU READ	LOCAL MEMORY (32-BIT)
0	00010	-	(RESERVED)
0	00011	-	(RESERVED)
0	00100	CPU READ	LOCAL ROM (16-BIT) LOW WORD LOCAL ROM (8-BIT) BYTE 0 LOCAL I/O (8-BIT) BYTE 0
0	00101	CPU READ	LOCAL ROM (8-BIT) BYTE 1 LOCAL I/O (8-BIT) BYTE 1
0	00110	CPU READ	LOCAL ROM (16-BIT) HIGH WORD LOCAL ROM (8-BIT) BYTE 2 LOCAL I/O (8-BIT) BYTE 2
0	00111	CPU READ	LOCAL ROM (8-BIT) BYTE 3 LOCAL I/O (8-BIT) BYTE 3
0	01000	CPU WRITE	32-BIT 16-BIT LOW WORD 8-BIT BYTE 0
0	01001	CPU WRITE	8-BIT BYTE 1
0	01010	CPU WRITE	16-BIT HIGH WORD 8-BIT BYTE 2
0	01011	CPU WRITE	8-BIT BYTE 3
0	01100	CPU READ	16-BIT AT BUS LOW WORD 8-BIT AT BUS BYTE 0
0	01101	CPU READ	8-BIT AT BUS BYTE 1
0	01110	CPU READ	16-BIT AT BUS HIGH WORD 8-BIT AT BUS BYTE 2
0	01111	CPU READ	8-BIT AT BUS BYTE 3

Table 7-3. Action Mode Codes For MASTER/DMA Cycles

HLDA1	DBAM<4:0>	CYCLE	OPERATION
1	00000	DEFAULT	
1	00001	MASTER WRITE	LOCAL MEMORY (16-BIT) LOCAL I/O AT BUS MEMORY (16-/8-BIT) AT BUS I/O (16-/8-BIT)
1	00010		(RESERVED)
1	00011		(RESERVED)
1	00100	MASTER READ	LOCAL MEMORY LOW WORD
1	00101	MASTER READ	LOCAL MEMORY HIGH WORD
1	00110	MASTER READ	LOCAL 16-BIT ROM (16-BIT) LOCAL 8-BIT ROM (8-BIT) LOCAL I/O (8-BIT)
1	00111	MASTER READ	16-BIT AT BUS MEMORY, I/O 8-BIT AT BUS MEMORY, I/O
1	01000	DMA WRITE	LOCAL MEMORY 16-BIT AT BUS MEMORY 8-BIT AT BUS MEMORY
1	01001	DMA READ	LOCAL 16-BIT ROM WORD LOCAL 16-BIT ROM LOW BYTE LOCAL 8-BIT ROM
1	01010	DMA READ	16-BIT AT BUS MEMORY WORD 16-BIT AT BUS MEMORY LOW BYTE 8-BIT AT BUS MEMORY
1	01011	DMA READ	16-BIT AT BUS MEMORY HIGH BYTE
1	01100	DMA READ	LOCAL MEMORY LOW WORD LOCAL MEMORY BYTE 0
1	01101	DMA READ	LOCAL MEMORY BYTE 1
1	01110	DMA READ	LOCAL MEMORY HIGH WORD LOCAL MEMORY BYTE 2
1	01111	DMA READ	LOCAL MEMORY BYTE 3

Table 7-4. Extended Action Mode Codes

HLDA1	DBAM<4:0>	CYCLE	OPERATION
X	10000	CPU WRITE	8042 CHIP SELECT
X	10001	CPU WRITE	PARALLEL PORT 1
X	10010	CPU WRITE	SERIAL PORT 1
X	10011	CPU WRITE	SERIAL PORT 2
X	10100	CPU WRITE	PROGRAMMABLE CHIP SELECT 0
X	10101	CPU WRITE	PROGRAMMABLE CHIP SELECT 1
X	10110	CPU WRITE	REAL-TIME CLOCK ADDRESS STROBE
X	10111	CPU WRITE	CLEAR 80387 BUSY
X	11000	CPU READ	8042 CHIP SELECT
X	11001	CPU READ	PARALLEL PORT 1
X	11010	CPU READ	SERIAL PORT 1
X	11011	CPU READ	SERIAL PORT 2
X	11100	CPU READ	PROGRAMMABLE CHIP SELECT 0
X	11101	CPU READ	PROGRAMMABLE CHIP SELECT 1
X	11110	CPU READ	CONFIGURATION REGISTER 4Dh
X	11111	CPU WRITE	CONFIGURATION REGISTER 49h

7.2 Data Transfer Modules

As shown in the block diagram, there are 4 data transfer modules. Each of these is controlled by the internal control signals generated by the Action Decode Control module. The description of each of these modules is given below.

7.2.1 CPU/DRAM Data Transfer Module

The CPU/DRAM Data Transfer Module controls the data flow between the CPU and the main memory. During memory write, CPU data is latched by WDLE and driven onto the MD bus. During memory read, the memory data is latched by DLE and driven onto the D bus. The data flow involved is shown in Figure 7-2.

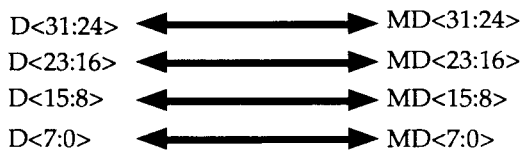


Figure 7-2. CPU/DRAM Data Transfer

7.2.2 CPU/AT/IO/ROM Data Transfer Module

The CPU/AT-BUS/IO/ROM Data Transfer Module controls data flow between the CPU and the AT-Bus, peripherals and system BIOS ROM. The CPU data is latched by WDLE during CPU write and the SD data is latched by DLE during CPU read.

The data flows for 16-bit transfers are shown in Figure 7-3.

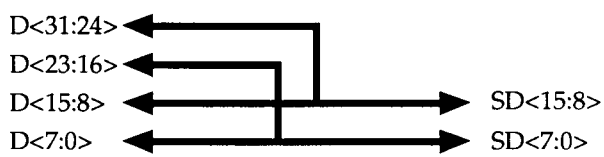


Figure 7-3. CPU/AT/IO/ROM 16-bit Data Transfer

The data flows for 8-bit transfers are shown in Figure 7-4.

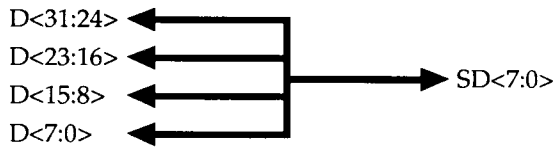


Figure 7-4. CPU/AT/IO/ROM 8-bit Data Transfer

7.2.3 DMA CYCLES Transfer Module

The DMA Cycles Transfer Module controls the data flow between the local SD bus and the main memory MD bus as well as between the local SD bus and the AT SD bus as shown in Figures 7-5A and 7-5B. During main memory read, the memory data is latched by DLE. The data transfer between an 8-bit local I/O and 16-bit AT memory is accomplished through a byte-swap mechanism as shown in Figure 7-5C.

Data flows for 16-bit DMA transfers are as follows:

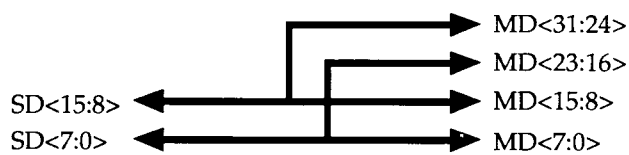


Figure 7-5A. 16-bit DMA Memory Cycles Transfer

Data flows for 8-bit DMA transfers are as follows:

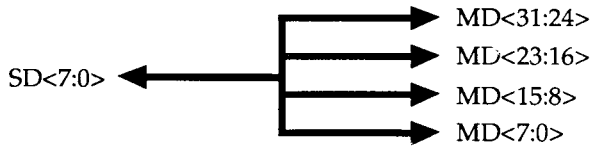


Figure 7-5B. 8-bit DMA Memory Cycles Transfer

AT memory transfer:

Figure 7-5C. Byte Swapping Between 8-bit local I/O and 16-bit AT Memory

7.2.4 MASTER CYCLES Transfer Module

The MASTER Cycles Transfer Module controls the data flow between the AT bus (SD) and the main memory bus (MD). During memory read, the memory data is latched by DLE. The memory write data is unlatched. The data flow involved is shown in Figure 7-6.

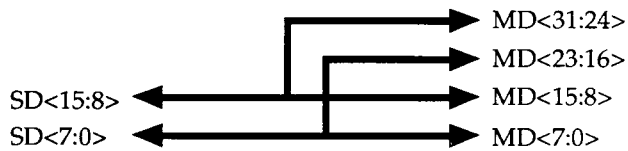


Figure 7-6 Memory Cycles Transfer

7.3 Parity Handler

In order to maintain data integrity, the e88C312 generates a parity bit for each byte of data written to local memory and also provides parity check to detect any mismatch whenever data is read from local memory.

During the local memory write cycle, source data (CPU, DMA or Master) is passed to the MD bus as well as to the parity generation logic. The parity generator generates one parity bit for each byte of write data and passes this bit to the memory parity outputs MP<3:0>. The memory write data (MD<31:0>) together with the parity bits (MP<3:0>) are written into the DRAM when the proper row address and/or column address strobes are issued by e88C311.

During the local memory read cycle, memory data MD<31:0> and memory parity bits MP<3:0> are latched into the e88C312. The MD data is redirected to the proper destinations (CPU, DMA or Master) as well as to the parity check logic. The parity check logic will regenerate new parity bits from the memory read data, one bit per byte, and compare them with the read memory parity bits. Bytes with a parity error will be latched into a 4-bit internal indexed register (4Dh). The content of this register can be read later for error diagnosis (action code DBAM<4:0> = 1Eh). Refer to Table 1.5 for the definition of register 4Dh.

The byte parity error bits are OR'ed together and latched to generate the parity error signal PARERR. When PARERR is high, it indicates a parity error has been detected. This will close the 4Dh latch and keep it closed until a reset condition has occurred or until a parity clear command (action code DBAM<4:0> = 1Fh) is issued. The e88C311 can constantly monitor the PARERR signal if the Parity Check Enable bit in register 49h is enabled. Upon detecting PARERR, it will latch the address where parity error occurred. e88C311 then generates an NMI (if it is enabled) to the CPU and executes an I/O operation to read register 4Dh in order to identify the byte(s) that have caused the error.

7.4 Timer Clock

The e88C312 also generates the AT bus color reference oscillator signal OSC. This output is a 14.31818 MHz clock signal. Another clock signal is generated by dividing the above signal by 12 to derive the OSC119 signal. This is used by the on-board Timer/Counter logic to perform the following functions under software control: timer, rate generator, pulse or square wave generators, and strobe signal. It is also used in the e88C311 to control the "RAS time-out" operation.

Table 7-5. REGISTER 4Dh Definition

NAME:	Parity Error Diagnostic Register 5 INDEX: 4Dh Default Values: XXXXXXXX
	Functions:
7-4	RESERVED
3	0 = No Parity Error 1 = Parity error is caused by BYTE 3
2	0 = No Parity Error 1 = Parity error is caused by BYTE 2
1	0 = No Parity Error 1 = Parity error is caused by BYTE 1
0	0 = No Parity Error 1 = Parity error is caused by BYTE 0
	NOTE: During power up, bits 3 and 2 reflects the presence status of Intel 80387 and WTL 3167 coprocessors respectively. 0 = Coprocessor is not installed 1 = Coprocessor is installed. After the first read from this register, it resumes the normal definition.

(The definition is also listed in e88C311 Specifications)

7.5 Math Coprocessor Interface Logic

The e88C312 supports the interface logic for the Intel 80387 as well as the WTL 3167 math coprocessor. Bus cycle generation is handled by the e88C311. Interface signals consist of input signals: FRSTADS, BZ387-, PRQ387-, ERR387-, RST387-, WINTR and WTPRES- and output signals: IRQ13, BZ386-, PRQ386 and ERR386-.

At reset, the states of the ERR387- and WTPRES- signals are sampled to detect the presence of either coprocessor. The states are latched into bits 3 and 2 of 4Dh register. The first *and only* I/O read access to 4Dh will read back these states to system BIOS (see Table 1.5). Subsequent access to 4Dh will return the parity error bits instead. The ERR387- is sampled by the trailing edge of RESET4 to generate the ERR386- output. By sampling this output during reset, the CPU (80386) is able to determine the presence of a 80387. The first ADS- signal from the CPU (FRSTADS) forces the ERR386- high thereafter. Subsequent ERR387- signals will not cause ERR386- to go low, but instead hold the busy state of the coprocessor at output BZ386- and also generate IRQ13.

The 80387 asserts ERR387- after an operation resulting in an error not masked by the coprocessor's control register. The e88C312 will use the ERR387- input to latch the BZ387- signal and generate IRQ13. As soon as BZ387- goes inactive (high), the PRQ386 is asserted. The PRQ386 is also asserted when PRQ387 becomes active. The latched BZ386- and IRQ13 will be cleared when e88C312 receives a RST387 signal from the e88C311 or when an I/O write cycle to port F0h or F1h is executed. (See action code DBAM<4:0> = 17h .)

8. e88C312 PIN DESCRIPTION

8.1 e88C312 Pin Diagram

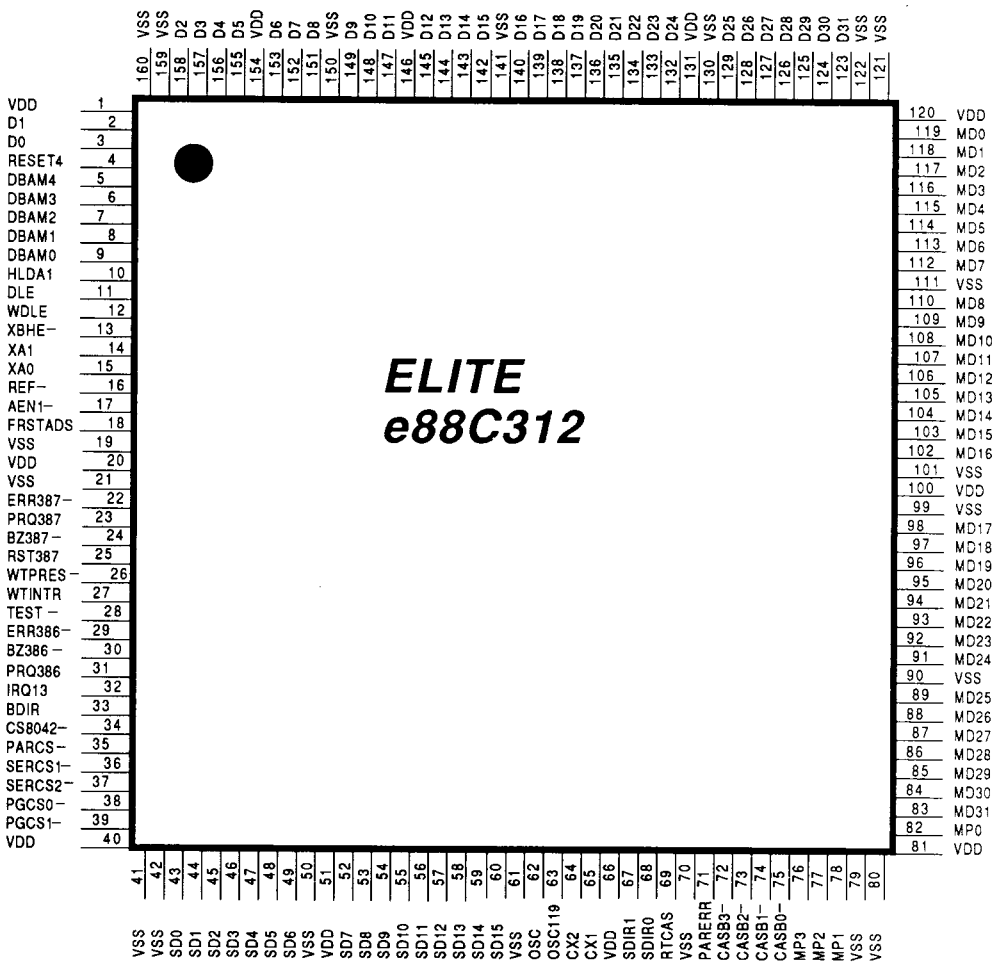


Figure 8-1. e88C312 Pin Diagram

8.2 e88C312 Pin List

PIN No.	NAME	TYPE	DESCRIPTION
123-129 132-140 142-145 147-149 151-153 155-158 2-3	**D<31:0>**	Input/Output	*Local Data* bits 0 through 31 connected to 80386 CPU.
12	**WDLE**	Input	*Write Data Latch Enable* from the e88C311. It is used to latch the CPU write data into an on-chip register for post-write operation
11	**DLE**	Input	*Data Latch Enable* from the e88C311. The high to low transition of this signal latches memory data into the e88C312.
10	**HLDA1**	Input	*Hold Acknowledge* 1 from the e88C311. It is high when the CPU relinquishes the system bus to other masters.
5-9	**DBAM<4:0>**	Input	Data controller action mode codes from the e88C311. It defines the type of current bus cycle and determines the direction of the data transfer.
17	**AEN1-**	Input	*Address Enable* of an 8 bit DMA transfer. It is used to latch the addresses for 8 bit DMA/Master cycles.
13	**XBHE-**	Input	*Byte High Enable.*
14-15	**XA<1:0>**	Input	XA address bits 1 and 0.
83-89 91-98 102-110 112-119	**MD<31:0>**	Input/Output	*Memory Data* bits 0 through 31 from memory array (DRAMs).
76-78, 82	**MP<3:0>**	Input/Output	*Memory Data Parity* bits from DRAMs.

PIN No.	NAME	TYPE	DESCRIPTION
71	**PARERR**	Output	*Latched Parity Error;* when high it indicates a parity error. The e88C311 will latch the error address upon detecting an error.
72-75	**CASB<3:0>-**	Input	*CAS Byte Enable* signals from the e88C311 latch parity error bits for each byte of data.
60-52 49-43	**SD<15:0>**	Input/Output	*System Data Bus.* SD<7:0> are tied together with the peripheral data bus signals XD<7:0>. SD<15:0> can be connected to the AT bus directly or through a pair of 245's.
67-68	**SDIR<1:0>**	Output	*SD Bus Direction Control.* These two signals are used to control the data bus direction between I/O channel data bus (SD) and local SD bus (LSD). When high, SDIR<1:0> drives the LSD bus toward the I/O Channel bus. When low, SDIR<1:0> drives the I/O Channel bus towards the LSD bus.
33	**BDIR**	Output	*Buffer Direction.* This signal is used to control the address bus direction between I/O Channel address bus (SA) and the peripheral address bus (XA). When high, BDIR drives the XA address bus toward SA address bus. When low, BDIR drives the SA address bus toward XA address bus.
16	**REF-**	Input	*AT Bus Refresh.* REF- is used to toggle the 80386 Busy signal (BZ386-) if 80387 is not present.
65	**CX1**	Input	*14.318 MHz Oscillator Input* from the crystal.
64	**CX2**	Output	*14.318 MHz Oscillator Output* to the crystal.
62	**OSC**	Output	*14.318 MHz Oscillator Output to the AT* bus.

PIN No.	NAME	TYPE	DESCRIPTION
63	**OSC119**	Output	*1.19 MHz* (14.318 MHz/12) or oscillator output. It is used by the e88C311 for RAS time-out control; it is also used as a clock input to the on-board timer/counter logic.
69	**RTCAS**	Output	*Address Strobe for the RTC.* The I/O address is conditioned with XIOW-.
34	**CS8042-**	Output	*8042 Keyboard Controller* Chip Select.
36	**SERCS1-**	Output	*Software Programmable Serial Port 1 chip select.* This feature is enabled by setting bit 0 of register 19h in the e88C311 to 1.
37	**SERCS2-**	Output	*Software Programmable Serial Port 2 Chip Select.* This feature is enabled by setting bit 1 of register 19h in the e88C311 to 1.
35	**PARCS-**	Output	*Software Programmable Parallel Port Chip select.* This feature is enabled by setting bit 2 of register 19h in the e88C311 to 1.
39-38	**PGCS<1:0>-**	Output	*Programmable Chip Select 0 and 1.* These are defined by configuration registers 13h through 18h in e88C311.
24	**BZ387-**	Input	*80387 BUSY-* signal. When active, it indicates that the coprocessor is busy executing an instruction. This input has an internal pull-up.
22	**ERR387-**	Input	*80387 ERROR-* signal. When active, it indicates that an error has been generated in a previous coprocessor cycle. This input has an internal pull-up.
23	**PRQ387**	Input	*80387 PEREQ* signal. When active, it indicates that the 80387 is requesting a data transfer cycle between the 80386 and the 80387. This input has an internal pull-down.

PIN No.	NAME	TYPE	DESCRIPTION
30	**BZ386-**	Output	*80386 BUSY*- signal. When active, it indicates that the coprocessor is still executing an instruction and is not able to accept the next instruction.
29	**ERR386-**	Output	*80386 ERROR*- signal. When active, it indicates that a previous coprocessor instruction generated an error of a type not masked by the coprocessor's control registers.
31	**PRQ386**	Output	*80386 PEREQ* signal. When active, it indicates that a coprocessor requests a data operand to be transferred to/from memory by the 80386.
26	**WTPRES-**	Input	*Weitek Coprocessor Presence.* If the Weitek coprocessor is installed, this pin will be pulled to logic 0. It should be connected to Vcc through a resistor of 10K Ohms to ensure a high logic level when the Weitek coprocessor is not installed.
27	**WTINTR**	Input	*Weitek Coprocessor Interrupt.* It is "OR'ed" with the 80387 interrupt logic to generate IRQ13. This input has an internal pull-down.
32	**IRQ13**	Output	*Interrupt Request 13.* When high, it signals an interrupt request from the coprocessor to the 80386. The service routine handles coprocessor errors.
18	**FRSTADS**	Input	*First Address Status.* An input signal from the e88C311 indicating the *first ADS- cycle.* It goes low after the first ADS- signal is issued by 80386. It is used to stop further detection of coprocessor presence after a system reset.
25	**RST387**	Input	*80387 Reset* from e88C311.
4	**RESET4**	Input	*RESET4* signal from the e88C311. It is used to reset all internal registers and to detect coprocessor presence during system reset.

PIN No.	NAME	TYPE	DESCRIPTION
28	**TEST-**	Input	*Test* signal. When low, this signal tri-states all of the e88C312 outputs. In normal operation, this signal should be tied to logic 1. This input has an internal pull-up.
1,20,40,51, 66,81,100, 120,131, 146,154	**VDD**	Input	Supply Voltage at nominal 5.0 Vdc.
19,21,41,42, 50,61,70,79, 80,90, 99,101, 111,121,122, 130,141,150, 159,160	**VSS**	Input	Ground.

9. e88C312 ELECTRICAL AND TIMING SPECIFICATION

9.1 Storage and Operating Characteristics

9.1.1 Absolute Maximum Ratings

Stresses above the conditions listed in this section may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at these or any other conditions above those indicated in the Recommended Operating Conditions section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9-1. Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	-0.3	7.0	Volts
Input Voltage	V_i	-0.3	V_{cc} + 0.3	Volts
Storage Temperature	T_{stg}	-40.0	125.0	degrees C

9.1.2 e88C312 Recommended Operating Conditions

Table 9-2. Recommended Operating Conditions

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Supply Voltage	V_{cc}	4.75	5.25	Volts
Input Voltage	V_i	0	V_{cc}	Volts
Ambient Temperature	T_a	0	50	degrees C

9.2 e88C312 DC Characteristics

(V_{CC} = 5.0 Volts +/-5%; T_a = 0 - 50° C)

Table 9-3. e88C312 DC Characteristics

PARAMETER	SYMBOL	VALUE		UNIT
		MIN	MAX	
Input Low Voltage	Vil			
TTL level			0.8	Volts
Schmitt level			1.0	Volts
Input High Voltage	Vih			
TTL level		2.0		Volts
Schmitt level		4.0		Volts
Input Low Current	Iil	–10	10	µA
W/ Pull-up Resistor		–200	–10	µA
Input high current		–10	10	µA
W/ Pull-down Resistor		10	200	µA
Output low voltage	Vol		0.4	Volts
2 mA buffer, IOL = 2mA				
4 mA buffer, IOL = 4mA				
8 mA buffer, IOL = mA				
12 mA buffer, IOL = 12 mA				
Output high voltage	Voh	2.4		Volts
2 mA buffer, IOH = -2mA				
4 mA buffer, IOH = -4mA				
8 mA buffer, IOH = -8mA				
12 mA buffer, IOH = -12mA				
High Impedance Leakage	Ioz			
Current		-10	10	µA
W/ Pull-up Resistor		-200	-10	µA
W/ Pull-down Resistor		10	200	µA
Device Quiescent	Iccq		TBD	µA
Supply Current			TBD	
Supply Current	Icc		TBD	mA
Power Dissipation	Pdis		TBD	mW
Input Capacitance	Cin		7	pF
Output or I/O Capacitance	Cout		10	pF

9.3 e88C312 AC Characteristics

(Vcc = 5.0 Volts +/- 5%; Ta = 0-50° C)

NOTE: The symbol number in the following table indicates which timing diagram the symbol is associated with. The first digit of the 3-digit number following the T indicates the figure number within section 10. For example, the timing parameter T505 can be found in Figure 10-5.

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
MD<31:0> Setup Time to DLE Low	T101	7		ns
MD<31:0> Hold Time from DLE Low	T102	5		ns
D<31:0> Valid from DBAM<4:0>	T103	8	29	ns
D<31:0> Valid from MD<31:0>	T104	4	15	ns
D<31:0> Float Delay from DBAM<4:0>	T105	8	26	ns
PARERR Valid from MD<31:0>	T106	10	35	ns
D<31:0> Setup Time to WDLE Low	T107	4		ns
D<31:0> Hold Time from WDLE Low	T108	2		ns
MD<31:0> Valid from DBAM<4:0>	T109	7	26	ns
MD<31:0> Valid from D<31:0>	T110	5	18	ns
MD<31:0> Float Delay from DBAM<4:0>	T111	6	20	ns
MP<3:0> Valid from DBAM<4:0>	T112	7	26	ns
MP<3:0> Valid from D<31:0>	T113	8	30	ns
MP<3:0> Float Delay from DBAM<4:0>	T114	6	20	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
SD<15:0> Valid from DBAM<4:0>	T201	10	35	ns
SD<15:0> Valid from MD<31:0>	T202	9	30	ns
SD<15:0> Float Delay from DBAM<4:0>	T203	9	33	ns
PARERR Valid from MD<31:0>	T204	10	35	ns
MD<31:0> Valid from SD<15:0>	T205	5	18	ns
MP<3:0> Valid from SD<15:0>	T206	9	33	ns
SD<15:0> Setup Time to DLE Low	T301	7	-	ns
SD<15:0> Hold Time from DLE Low	T302	5	-	ns
D<31:0> Valid from SD<15:0>	T303	6	19	ns
SD<15:0> Valid from D<31:0>	T304	8	28	ns
BDIR Active from DBAM<4:0>	T401	4	14	ns
BDIR Inactive from DBAM<4:0>	T402	5	17	ns
SDIR0 Active from DBAM<4:0>	T403	8	28	ns
SDIR0 Inactive from DBAM<4:0>	T404	8	27	ns
SD<7:0> Valid from SD<15:8>	T405	9	32	ns
SDIR1 Active from DBAM<4:0>	T406	8	28	ns
SDIR1 Inactive from DBAM<4:0>	T407	8	27	ns
SD<15:8> Valid from SD<7:0>	T408	9	32	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
CS8042- Active from DLE High	T501	5	16	ns
PARCS- Active from DLE High	T502	5	16	ns
SERCS1- Active from DLE High	T503	5	16	ns
SERCS2- Active from DLE High	T504	5	16	ns
PGCS0- Active from DLE High	T505	5	16	ns
PGCS1- Active from DLE High	T506	5	16	ns
RTCAS Active from DLE High	T507	5	16	ns
CS8042- Inactive from DLE Low	T508	6	18	ns
PARCS- Inactive from DLE Low	T509	6	18	ns
SERCS1- Inactive from DLE Low	T510	6	18	ns
SERCS2- Inactive from DLE Low	T511	6	18	ns
PGCS0- Inactive from DLE Low	T512	6	18	ns
PGCS1- Inactive from DLE Low	T513	6	18	ns
RTCAS Inactive from DLE Low	T514	6	18	ns
CX2 Low from CX1 High	T601	4	12	ns
OSC Low from CX1 High	T602	11	38	ns
OSC119 High from CX1 Low	T603	11	40	ns
CX2 High from CX1 Low	T604	2	6	ns
OSC High from CX1 Low	T605	9	30	ns
OSC119 Low from CX1 Low	T606	11	40	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
ERR387- Setup Time to RESET4 Low	T701	6	-	ns
ERR387- Hold Time from RESET4 Low	T702	4	-	ns
ERR386- Valid from RESET4 Low	T703	6	21	ns
ERR386- Inactive from FRSTADS Low	T704	4	13	ns
BZ387- Setup Time to ERR387- Low	T705	7	-	ns
BZ387- Hold Time from ERR387- Low	T706	4	-	ns
BZ386- Active from BZ387- Low	T707	5	16	ns
BZ386- Inactive from RST387 High	T708	6	21	ns
PRQ386 Active from BZ387- High	T709	6	20	ns
PRQ386 Inactive from RST387 High	T710	6	22	ns
IRQ13 Active from BZ387- High	T711	5	19	ns
IRQ13 Inactive from RST387 High	T712	6	21	ns
BZ386- Inactive from DLE High (DBAM<4:0> = 17 h)	T713	6	22	ns
PRQ386 Inactive from DLE High (DBAM<4:0> = 17 h)	T714	7	23	ns
IRQ13 inactive from DLE High (DBAM<4:0> = 17 h)	T715	7	23	ns
PRQ386 Active from PRQ387 High	T716	4	12	ns
PRQ386 Inactive from PRQ387 Low	T717	5	16	ns
IRQ13 Active from WTINTR High	T718	4	13	ns
IRQ13 Inactive from WTINTR Low	T719	5	17	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
D<31:24> Valid from DLE High (DBAM<4:0> = 1Eh)	T801	6	21	ns
SD<7:0> Valid from DBAM<4:0>=1Eh	T802	13	43	ns
PARERR Inactive from DBAM<4:0>=1Eh	T803	7	25	ns

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
BDIR Active from REF- Low	T901	5	16	ns
BDIR Inactive from REF- High	T902	5	16	ns
BZ386- Active from REF- Low	T903	6	20	ns
BZ386- Inactive from REF- High	T904	5	16	ns
D<31:0> Tri-Stated from TEST- Low	T905	6	21	ns
MD<31:0> Tri-Stated from TEST- Low	T906	7	23	ns
MP<3:0> Tri-Stated from TEST- Low	T907	7	23	ns
SD<15:0> Tri-Stated from TEST- Low	T908	8	25	ns
PARERR Tri-stated from TEST- Low	T909	4	15	ns
OSC Tri-Stated from TEST- Low	T910	4	17	ns
All Other Outputs Tri-Stated from TEST- Low	T911	4	15	ns
D<31:0> Enabled from TEST- High	T912	6	23	ns
MD<31:0> Enabled from TEST- High	T913	7	25	ns
MP<3:0> Enabled from TEST- High	T914	7	25	ns
SD<15:0> Enabled from TEST- High	T915	8	26	ns
PARERR Enabled from TEST- High	T916	4	14	ns
OSC Enabled from TEST- High	T917	4	15	ns
All Other Outputs Enabled from TEST- High	T918	5	18	ns

10. e88C312 TIMING DIAGRAMS

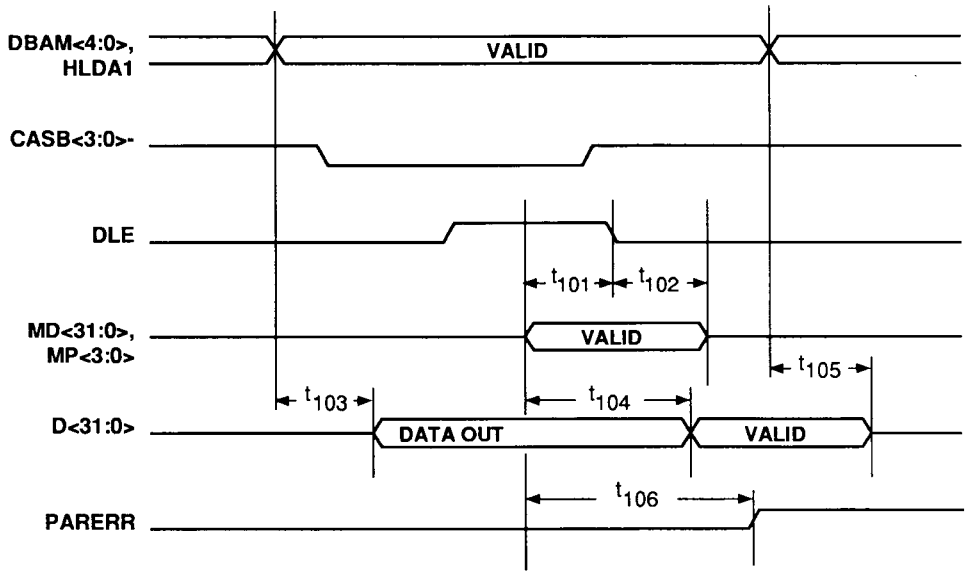


Figure 10-1A. CPU Local Memory Read

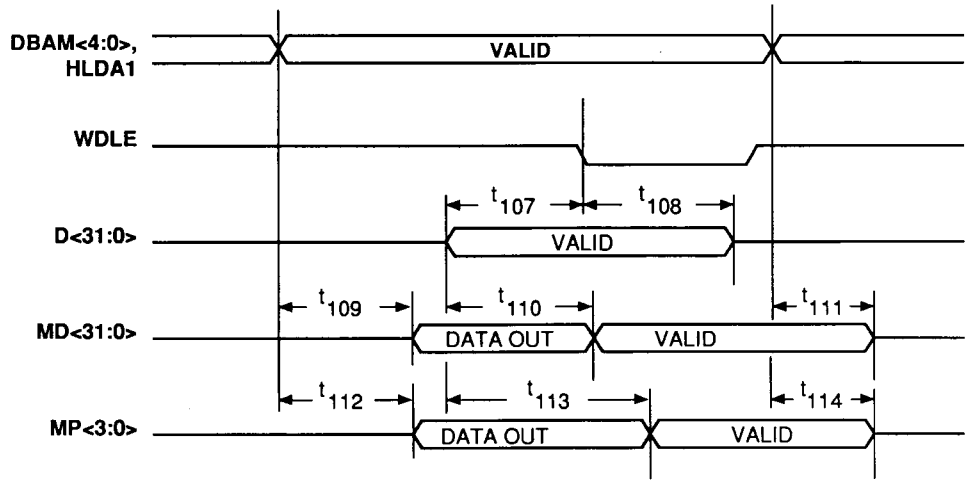
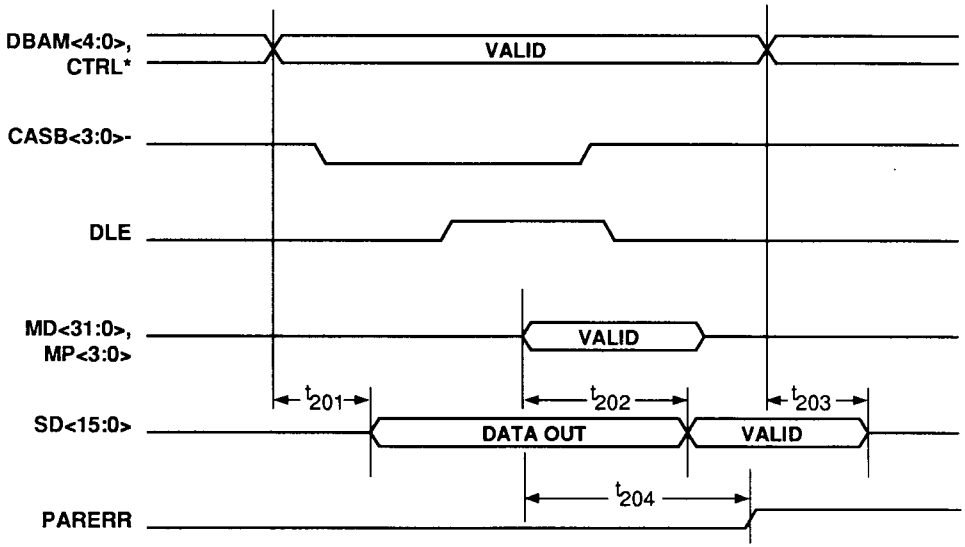
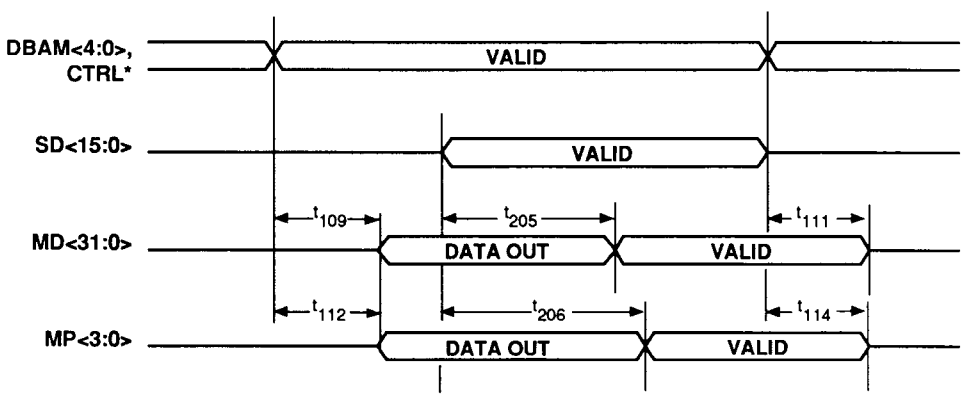


Figure 10-1B. CPU Local Memory Write



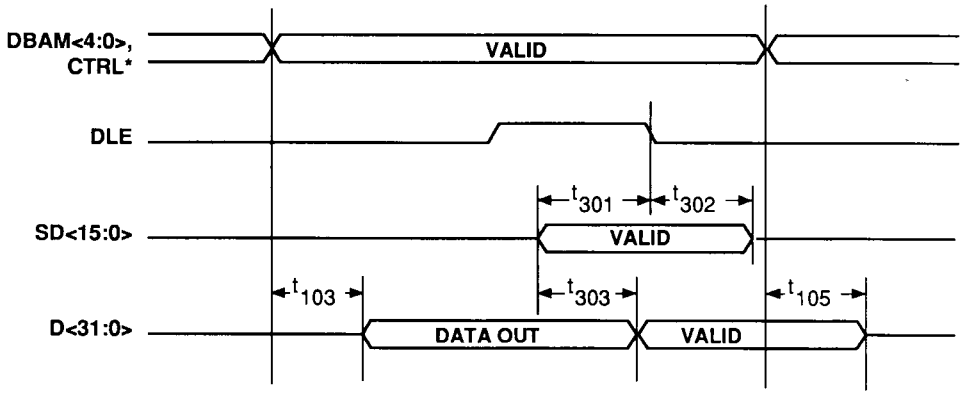
[CTRL* = HLDA1, AEN1- , XBHE-, XA1, XA0]

Figure 10-2A. Master/DMA Local Memory Read



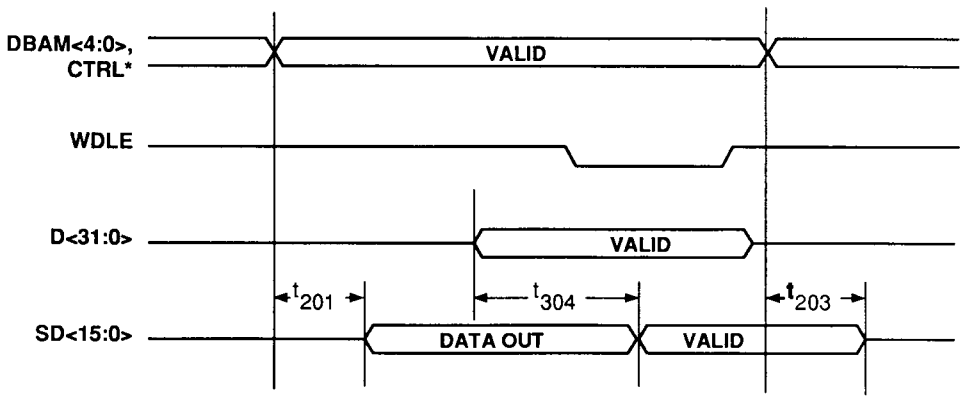
[CTRL* = HLDA1, AEN1- , XBHE-, XA1, XA0]

Figure 10-2B. Master/DMA Local Memory Write



[CTRL* = HLDA1, XBHE-, XA1, XAO]

Figure 10-3A. CPU I/O Read



[CTRL* = HLDA1, XBHE-, XA1, XAO]

Figure 10-3B. CPU I/O Write

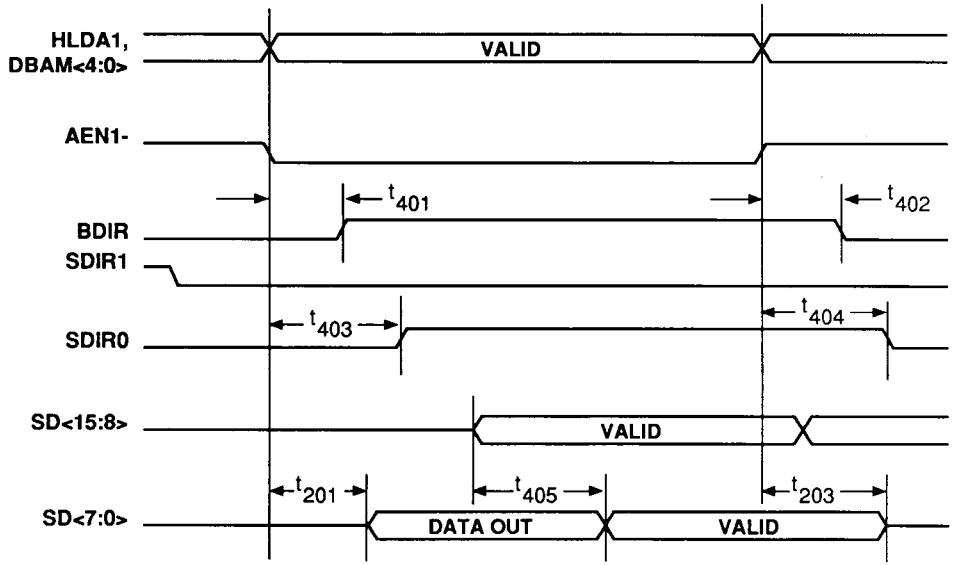


Figure 10-4A. 8-bit DMA Hi-Byte to Low-Byte Swap

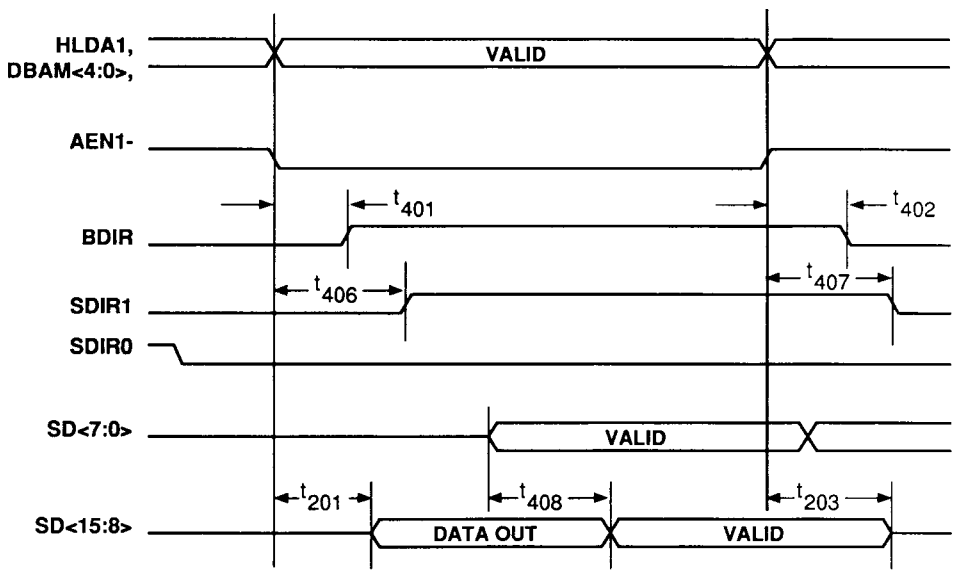


Figure 10-4B. 8-bit DMA Low-Byte to Hi-Byte Swap

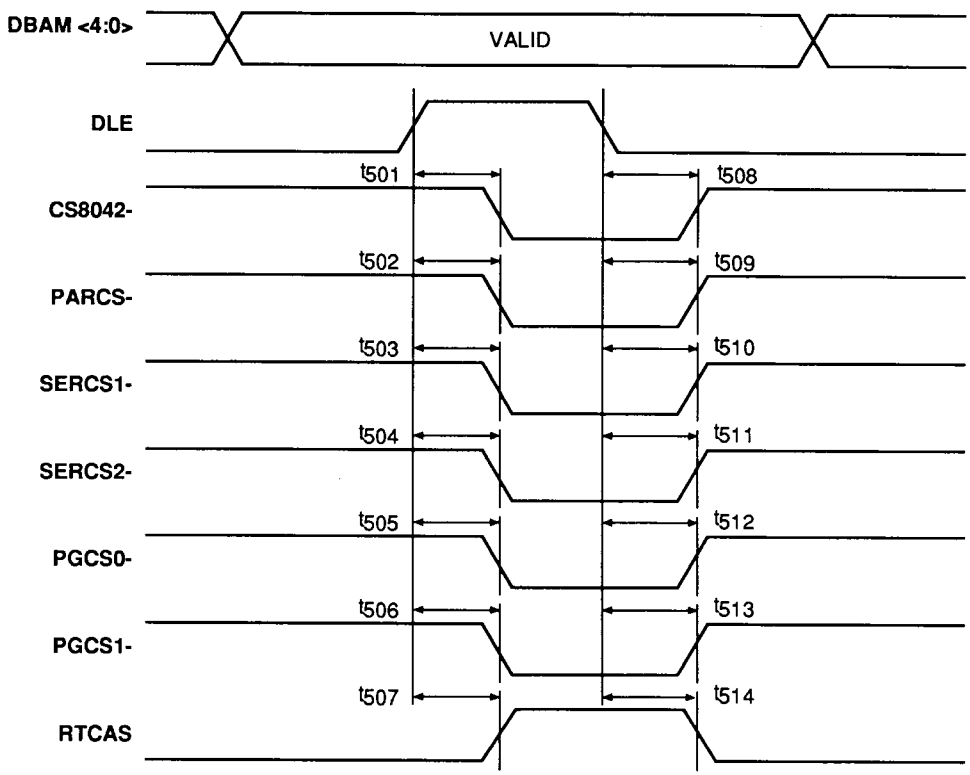


Figure 10-5. I/O Chip Selects

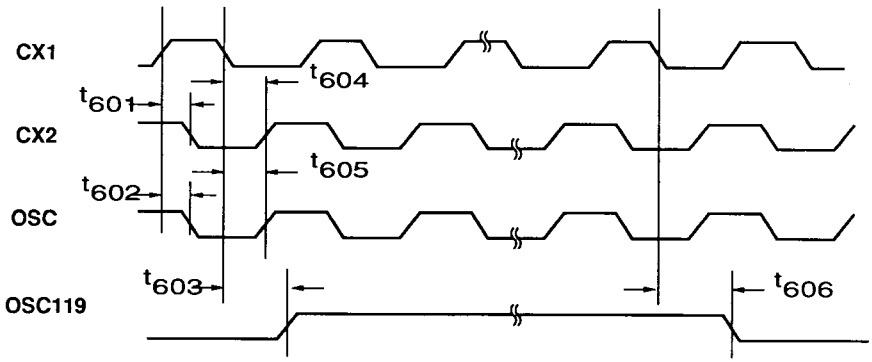


Figure 10-6. Oscillator and Timer Clock

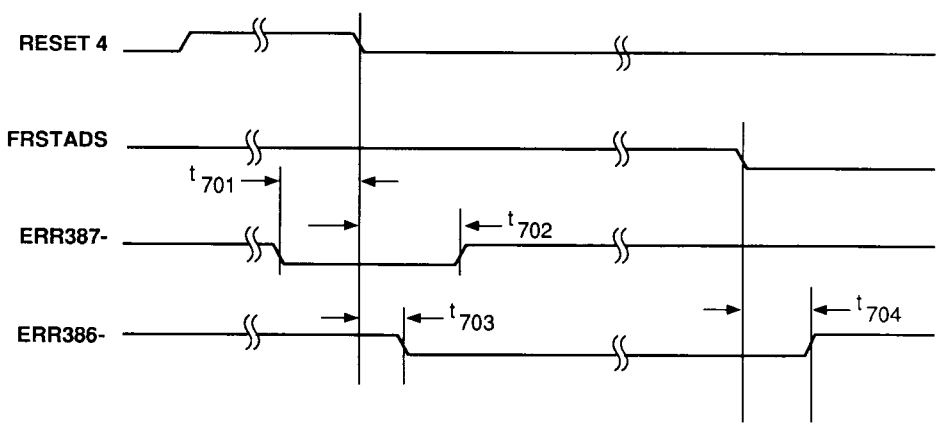


Figure 10-7A. Math Coprocessor Detection

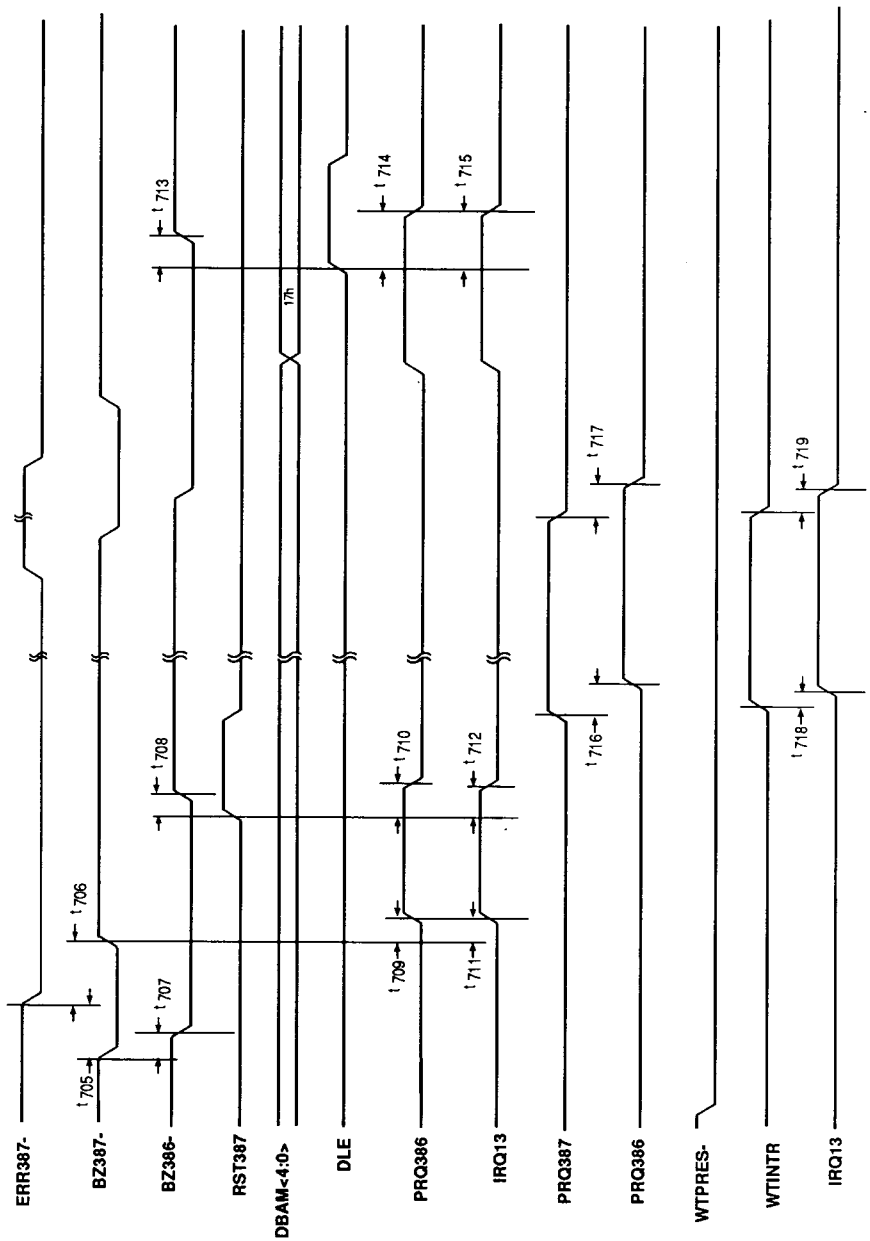


Figure 10-7B. Math Coprocessor Interface Timing

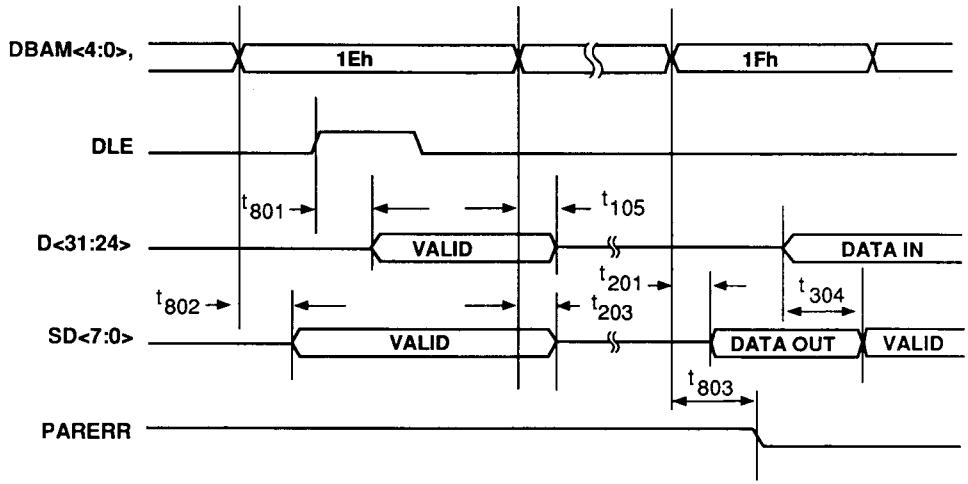


Figure 10-8. Parity Register Read and Reset

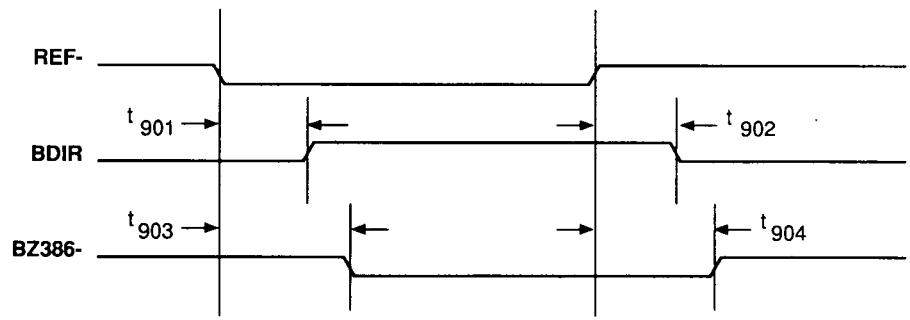


Figure 10-9A. Refresh Buffer Control and Coprocessor Busy

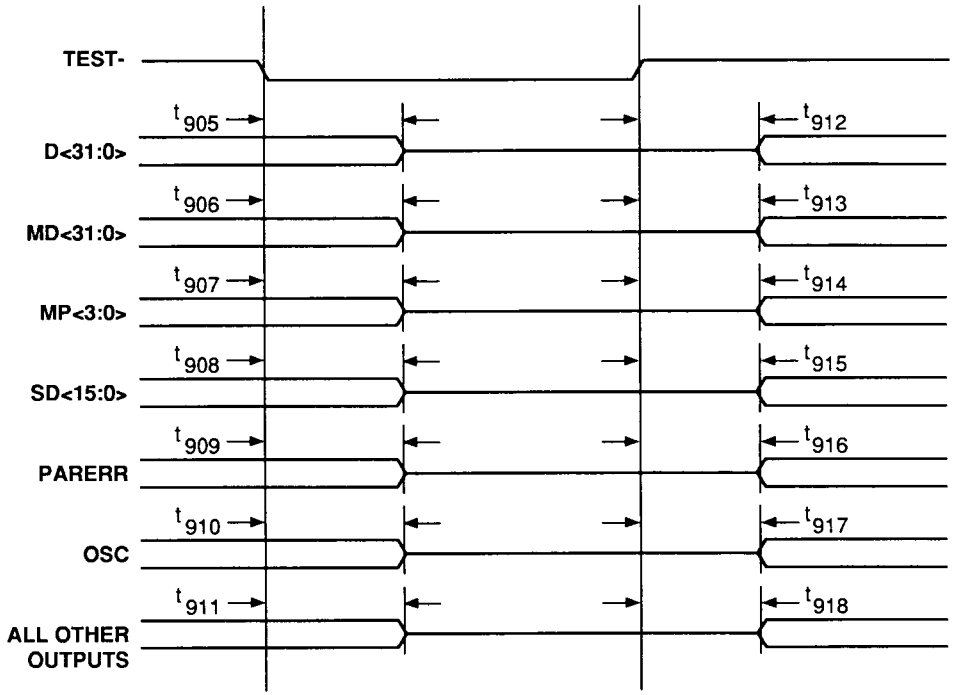
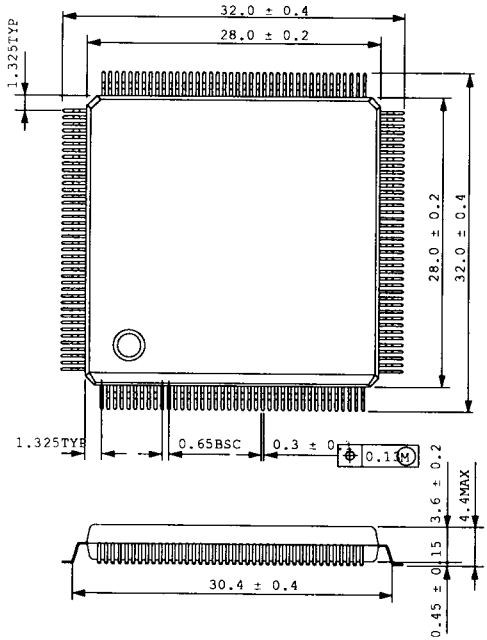
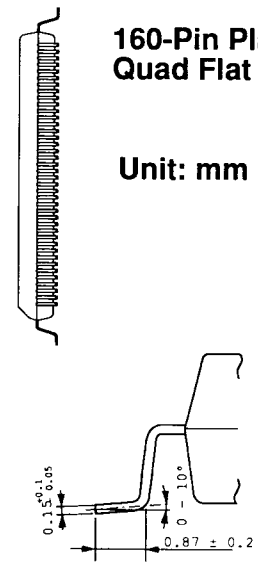


Figure 10-9B. Test Mode

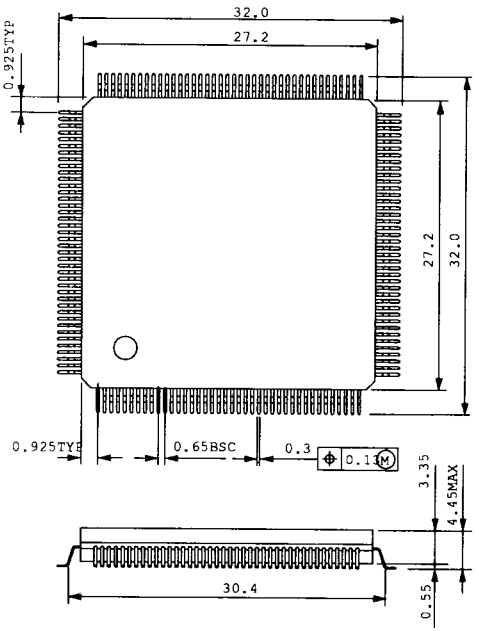
11. e88C312 MECHANICAL INFORMATION

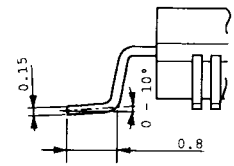




160-Pin Plastic Quad Flat Package

Unit: mm





160-Pin Ceramic Quad Flat Package

Unit: mm

Figure 11-1. e88C312: 160-Pin Quad Flat Package

11.1 e88C312 Pin Lists

11.1.1 Numerical

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VDD	41	VSS	81	VDD	121	VSS
2	D1	42	VSS	82	MP0	122	VSS
3	D0	43	SD0	83	MD31	123	D31
4	RESET4	44	SD1	84	MD30	124	D30
5	DBAM4	45	SD2	85	MD29	125	D29
6	DBAM3	46	SD3	86	MD28	126	D28
7	DBAM2	47	SD4	87	MD27	127	D27
8	DBAM1	48	SD5	88	MD26	128	D26
9	DBAM0	49	SD6	89	MD25	129	D25
10	HLDA1	50	VSS	90	VSS	130	VSS
11	DLE	51	VDD	91	MD24	131	VDD
12	WDLE	52	SD7	92	MD23	132	D24
13	XBHE-	53	SD8	93	MD22	133	D23
14	XA1	54	SD9	94	MD21	134	D22
15	XA0	55	SD10	95	MD20	135	D21
16	REF-	56	SD11	96	MD19	136	D20
17	AEN1-	57	SD12	97	MD18	137	D19
18	FRSTADS	58	SD13	98	MD17	138	D18
19	VSS	59	SD14	99	VSS	139	D17
20	VDD	60	SD15	100	VDD	140	D16
21	VSS	61	VSS	101	VSS	141	VSS
22	ERR387-	62	OSC	102	MD16	142	D15
23	PRQ387	63	OSC119	103	MD15	143	D14
24	BZ387-	64	CX2	104	MD14	144	D13
25	RST387	65	CX1	105	MD13	145	D12
26	WTPRES-	66	VDD	106	MD12	146	VDD
27	WTINTR	67	SDIR1	107	MD11	147	D11
28	TEST-	68	SDIR0	108	MD10	148	D10
29	ERR386-	69	RTCAS	109	MD9	149	D9
30	BZ386-	70	VSS	110	MD8	150	VSS
31	PRQ386	71	PARERR	111	VSS	151	D8
32	IRQ13	72	CASB3-	112	MD7	152	D7
33	BDIR	73	CASB2-	113	MD6	153	D6
34	CS8042-	74	CASB1-	114	MD5	154	VDD
35	PARCS-	75	CASB0-	115	MD4	155	D5
36	SERCS1-	76	MP3	116	MD3	156	D4
37	SERCS2-	77	MP2	117	MD2	157	D3
38	PGCS0-	78	MP1	118	MD1	158	D2
39	PGCS1-	79	VSS	119	MD0	159	VSS
40	VDD	80	VSS	120	VDD	160	VSS

11.1.2 Alphabetical

Name	Pin	Name	Pin	Name	Pin	Name	Pin
AEN1-	17	D7	152	MD4	115	SERCS1-	36
BDIR	33	D8	151	MD5	114	SERCS2-	37
BZ386-	30	D9	149	MD6	113	TEST-	28
BZ387-	24	DBAM0	9	MD7	112	VDD	1
CASB0-	75	DBAM1	8	MD8	110	VDD	20
CASB1-	74	DBAM2	7	MD9	109	VDD	40
CASB2-	73	DBAM3	6	MP0	82	VDD	51
CASB3-	72	DBAM4	5	MP1	78	VDD	66
CS8042-	34	DLE	11	MP2	77	VDD	81
CX1	65	ERR386-	29	MP3	76	VDD	100
CX2	64	ERR387-	22	OSC	62	VDD	120
D0	3	FRSTADS	18	OSC119	63	VDD	131
D1	2	HLDA1	10	PARCS-	35	VDD	146
D10	148	IRQ13	32	PARERR	71	VDD	154
D11	147	MD0	119	PGCS0-	38	VSS	19
D12	145	MD1	118	PGCS1-	39	VSS	21
D13	144	MD10	108	PRQ386	31	VSS	41
D14	143	MD11	107	PRQ387	23	VSS	42
D15	142	MD12	106	REF-	16	VSS	50
D16	140	MD13	105	RESET4	4	VSS	61
D17	139	MD14	104	RST387	25	VSS	70
D18	138	MD15	103	RTCAS-	69	VSS	79
D19	137	MD16	102	SD0	43	VSS	80
D2	158	MD17	98	SD1	44	VSS	90
D20	136	MD18	97	SD10	55	VSS	99
D21	135	MD19	96	SD11	56	VSS	101
D22	134	MD2	117	SD12	57	VSS	111
D23	133	MD20	95	SD13	58	VSS	121
D24	132	MD21	94	SD14	59	VSS	122
D25	129	MD22	93	SD15	60	VSS	130
D26	128	MD23	92	SD2	45	VSS	141
D27	127	MD24	91	SD3	46	VSS	150
D28	126	MD25	89	SD4	47	VSS	159
D29	125	MD26	88	SD5	48	VSS	160
D3	157	MD27	87	SD6	49	WDLE	12
D30	124	MD28	86	SD7	52	WTINTR	27
D31	123	MD29	85	SD8	53	WTPRES-	26
D4	156	MD3	116	SD9	54	XA0	15
D5	155	MD30	84	SDIR0	68	XA1	14
D6	153	MD31	83	SDIR1	67	XBHE-	13

Index

Items starting with numbers

A

B

C

D

E

F

M

N

O

P

R

S

T

V

W

X