CHEETAH ET6000
SINGLE CHIP 486 NON CACHE SOLUTION

* **100% IBM PC/AT Compatible 1-Chip AT Solution**
* **Designed to work at 16, 20, 25, 33 and 50MHz on a 486SX/DX based system**
* **Fast Burst Mode Memory Manager-Burst Read and 0WS Write**
* **One blocks of non-cacheable memory regions**
* **Up to 64MB DRAM support with Page Mode**
* **Mixing DRAM configurations - 256K, 1M and 4M devices**
* **Single ROM BIOS**
* **Shadow RAM option**
* **Software Programmable DRAM Wait States**
* **Fast Reset and Gate A20 to Optimize OS/2**
* **Asynchronous AT Bus Clock Generation**
* **Support Intel 80487SX and Weitek 4167 Coprocessor without external PALs**
* **Concurrent Refresh and AT Refresh Option**
* **Hardware and Software Turbo Clock Switching**
* **Local Bus support**
* **Less than 10 components plus memory to implement an unique 486 system**
* **1.0 Micron Low Power, High Speed CMOS Technology**
* **160 Pin PQFP package**

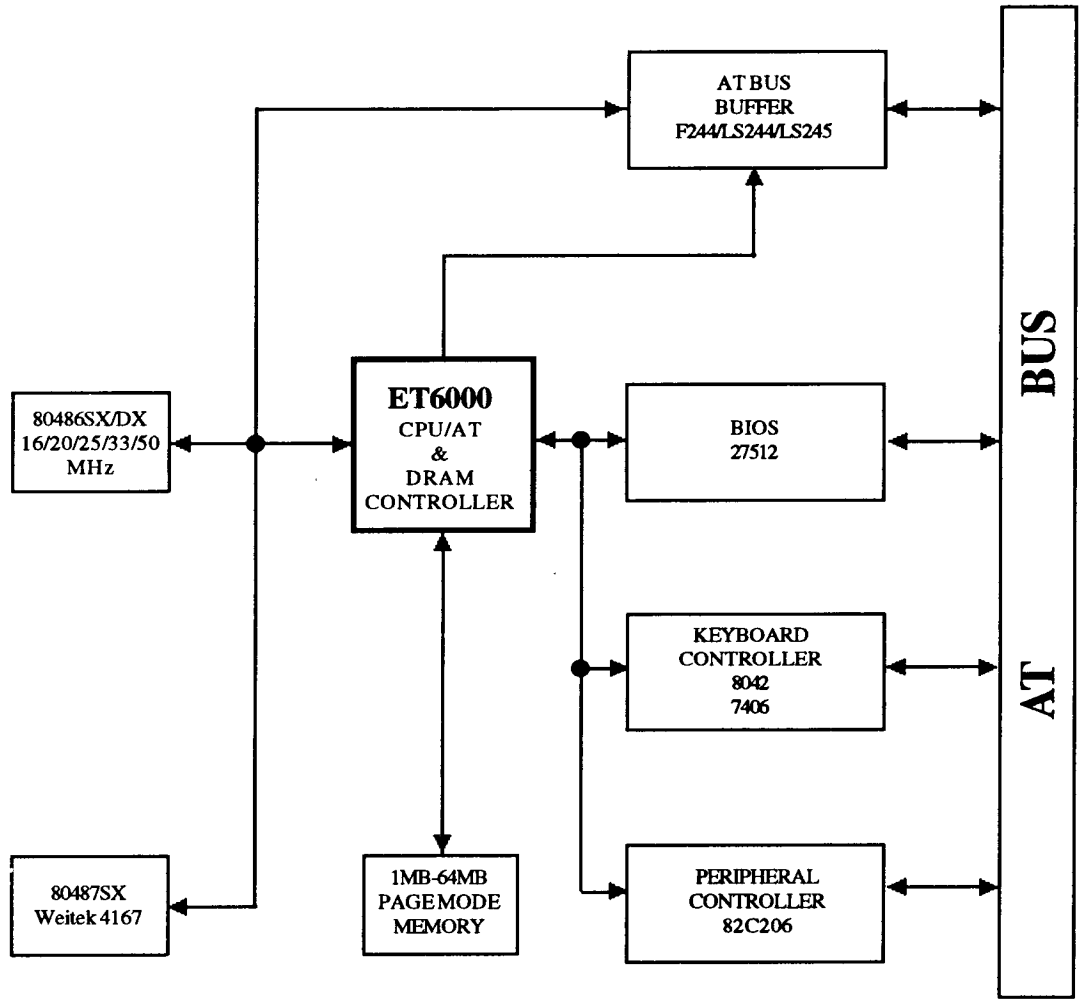
The CHEETAH single chip provides high integration and a low cost solution for a 16, 20, 25, 33, and 50MHz 486/AT based system design. The CHEETAH combined with 82C206 or compatible peripheral controller offers a 100% PC/AT compatible system using less than 10 components plus memory devices. The CHEETAH is available in the 160-pin Plastic Quad Flat-pack package. The 1.0u high speed, low power CMOS Technology allows for substantial stability when running at 25, 33, and 50MHz.

The CHEETAH includes 486 CPU control, AT Bus Control, Page Mode DRAM Control, Asynchronous AT Bus Clock Generation, data bus conversion logic which performs the conversion necessary between the 8 and 16-bit data paths, and Coprocessor Interface Logic to support Intel 487SX and Weitek 4167.

The Cheetah ET6000 is a highly integrated single chip AT optimized specifically for 486 CPUs. The emphasis of this chip is to reduce the cost requirements of 486 applications, without compromising performance. Fast bursting can be achieved with 80ns DRAMs.

The system cost is also minimized by allowing the use of slow DRAMs. The Burst Mode DRAM control is implemented to enhance system performance.

The Cheetah is designed to be 100% compatible with the IBM PC/AT. With its optimized Burst and DRAM design, enhanced features like Shadow RAM BIOS, and Concurrent Refresh; a high performance/low cost 486/AT can be implemented.



Cheetah 486 System Block Diagram

ET6000 SINGLE CHIP NON CACHE SOLUTION

1.0 Overview

The CHEETAH provides an efficient cost/performance ratio as a high rate of integration in a 486 based, IBM PC/AT compatible system. It is implemented using 1.0u CMOS Technology and can run at 16MHz, 20MHz, 25MHz, 33MHz and 50MHz of CPU system clock

The ET6000 contains the Memory Controller, AT Bus Controller, CPU Controller, Data Buffer Circuitry. The Burst DRAM Controllers are the main factors affecting the performance/cost ratio of the system.

The ET6000 interfaces directly with the 80486 and implements the state machines required for controlling all bus accesses.

The ET6000 performs all of the data buffering functions required for a 486 based PC/AT compatible personal computer system. The chip routes the data to and from the CPU Data Bus (CD Bus), the MAXD Bus and the ISA Bus (SD Bus) under CPU control.

2.0 Functional Description

The ET6000 has the following function modules:

* **Reset and Shutdown Logic**
* **CPU and AT Bus Control**
* **Master, DMA and Refresh Arbitration Logic**
* **Port B Register and NMI Logic**
* **OS/2 Optimization Logic (Port 92)**
* **DRAM Controller Logic**
* **DMA and Master Access DRAM Logic**
* **Concurrent Refresh**
* **Shadow RAM**
* **Bus Interface between CD, MAXD and SD Buses**
* **Parity Generation and Checking Logic**
* **Numerical Coprocessor Interface Logic**
* **14.318MHz and Counter Divided by 12**

2.1 Reset and Shutdown

The system contains four different resets: RESET1 is derived from the power-good signal at the power supply. Some power supplies have glitches on this signal, therefore, a de-dounce circuit is required before tying it to the RESET1 pin. RESET1 will generate both RESET3 (CPU Reset) and RESET4 (System Reset) for power-on initialization. This can only happen at system power-on. RESET2 is generated from the Cheetah ; it triggers RESET3 to reset the CPU either to perform a shutdown or to activate a software reset. It can also be generated by programming the internal register. RESET3 is activated for power-on, shutdown and for changing the CPU from protect mode back to real mode. RESET4 is activated when the entire system is reset.

2.2 Clock Generation

The ET6000 uses a single oscillator to generate the CPU clock. The oscillator input should be the same speed of the CPU. Depending upon the external crystal 14.318MHz frequency, the AT Bus Clock is divided by 2 as 7.1MHz. The AT Bus Clock can be changed by adding other external oscillator.

2.3 CPU and AT Bus Control

The CPU starts a cycle by asserting ADS- if the M/IO-, D/C- and W/R- signals plus address code turn out to be a internal local memory, LOCRAM- will assert LOW and the memory cycle begins. Otherwise, an AT Bus cycle will begin. ROM cycle is considered to be an AT Bus cycle because it is fixed at 8MHz and does not vary in relation to the CPU's speed. Therefore, a 200 nano-second access time ROM will be sufficient. Shadow RAM is supported to increase the performance. Since the CPU is running at its maximum speed, and the AT Bus is running at 8MHz, synchronization is required. DRAM does not need this handshaking because it is running at the same frequency as the CPU, thus, every-thing is synchronized. For the AT Bus cycle, ALE is where the AT Bus starts and the synchronized CPU ready is where it ends. This synchronization overhead can be significant when the AT Bus cycle is continu-ously accessed. The ET6000 synchronizes ALE with an option by switching the phase of the AT clock, not the signal itself, therefore, increasing the speed.

2.4 Master, DMA and Refresh

The Master Device uses the same pin as DMA for bus arbitration, and Refresh operates from a different pin so that it is easy to identify. The Master Device or DMA can be identified by the signals AEN8- and AEN16-. When either one is asserted LOW, it is a DMA cycle. The ET6000 supports both AT and Concurrent Refresh. No hold signal is sent back to the CPU in Concurrent Refresh. The AT Bus needs the full time to refresh as DRAMs do not need as much time. The ET6000 keeps track of when CPU to start its next instruction parallel to AT Bus Refresh. If the CPU needs to access the AT Bus, it must wait until refresh is completed.

2.5 Port B and NMI

A parity error detected will cause ET6000 to generate NMI to the CPU. NMI can also be generated through software. The ET6000 provides access to the Port B register defined for a PC/AT. The chart below illustrates bit definition:

Bit Definition Chart

Address	Bits	Function	Description
61H	7	Read Only	System Memory Parity Check
	6	Read Only	IO Channel Check
	5	Read Only	Timer 2 Output
	4	Read Only	Refresh Detection
	3	Read/Write	0: Enable IO Channel Check 1: Disable IO Channel Check
	2	Read/Write	0: Enable System Memory Parity Check 1: Disable System Memory Parity Check
	1	Read/Write	Speaker Data
	0	Read/Write	Timer 2 Gate

2.6 OS/2 Optimization

When running OS/2, 8742 needs to be programmed to activate the signal GATE A20 before entering Protected Mode. When it returns from the Protected Mode, some types of software use RESET2 by programming 8742 again. The Keyboard controller is a very slow device, thus, the system is slowed down dramatically. ET6000 supports the fast Gate A20 and Reset keyboard emulation and port 92 to help speed up performance.

2.7 DRAM Control Logic

2.7.1 Introduction

The DRAM Control Logic is designed and optimized for the 486 CPU. The ET6000 features an optimized DRAM memory controller, offering the highest performance for i486 CPU-based systems, while still retaining flexibility to allow the user to tailor the system to meet his/her needs.

Many memory configurations are available with the ET6000. These configurations are accomplished through use of the programmable register set. Slower DRAM devices can be accommodated through configuring the RAS# and CAS# access clocks. The number of clocks from assertion of RAS# to assertion of CAS# can be set to either 1.0 or 1.5 CPU T-states, while the number of clocks for CAS# access time can be either 1.0, 1.5, or 2.0 T-states. In addition, the RAS# precharge time Trp is programmable to either two or three clocks. The DRAM Controller supports up to 4 banks of DRAM with size up to 64MByte and three types of DRAM are supported: 256K, 1M and 4M.

TABLE A

Bank 0	Bank 1	Bank 2	Bank3	Total Memory Size	Page Size
256K	NONE	NONE	NONE	1M	2K
256K	256K	NONE	NONE	2M	4K
256K	256K	256K	NONE	3M	6K
256K	256K	256K	256K	4M	8K
1M	256K	NONE	NONE	5M	6K
256K	256K	1M	NONE	6M	8K
256K	256K	256K	1M	7M	10K
1M	1M	NONE	NONE	8M	8K
1M	1M	256K	NONE	9M	10K
256K	256K	1M	1M	10M	12K
1M	1M	1M	NONE	12M	12K
1M	1M	1M	256K	13M	14K
1M	1M	1M	1M	16M	16K
1M	4M	NONE	NONE	20M	12K
1M	1M	4M	NONE	24M	16K
1M	1M	1M	4M	28M	20K
4M	4M	NONE	NONE	32M	16K
4M	4M	1M	NONE	36M	20K
256K	1M	4M	4M	37M	22K
1M	1M	4M	4M	40M	24K
4M	4M	4M	NONE	48M	24K
256K	4M	4M	4M	49M	26K
1M	4M	4M	4M	52M	28K
4M	4M	4M	4M	64M	32K

Table A : Partial Possible DRAM Configuration

2.7.2 DRAM Sizes/Bank Configuration

For system design flexibility, the ET6000 can support either 256K, 1M, or 4M DRAM's. The amount of DRAM installed, and the size is indicated to the ET6000 by the use of register bits. Bits 3 and 2 at the index register 16H are used to indicate installed banks of DRAM, while bits 1 and 0 at the same register indicate the size of the DRAM's. From the settings of these bits, the CHEETAH internally calculates the bank address mappings and the top of physical memory. The DRAM Banks have to be filled in the following order: Bank0 -> Bank1 -> Bank2 -> Bank3. Possible DRAM bank configurations are shown Table A on page 5.

2.7.3 DRAM Speed and Wait State

In order to work with different types of DRAM speed, ET6000 supports wait state for memory read cycle as well as memory write cycle. For read cycle, a configuration of 0 to 3 wait state is available: R1WT, R2WT, R3WT. For write cycle, the ET6000 supports: W0WT, W1WT. (See Table B below.)

The ET6000 has Burst Mode Memory Manager support 3-2-2-2, 4-3-3-3, 5-4-4-4 DRAM burst cycles to enhance system speed.

2.7.4 Row and Column Address

Table C, below, illustrates row/column address for different types of DRAM. For easy debugging, all row and column addresses are continuous, no scramble is needed.

2.8 DMA and Master Access DRAM Logic

The DMA Master can access the local DRAM through ET6000. When HLDA1 and MEMR/MEMW become active, a memory read/write cycle will be performed. To guarantee cache coherence, the SRAM data will be updated when a memory write hit occurs.

2.9 Concurrent Refresh

In order to alleviate refresh penalty, ET6000 supports "Concurrent Refresh" in addition to normal PC Refresh. Traditional PC Refresh will send a HOLD to stop the CPU, Then, after receiving HLDA from the CPU, refresh will begin. Concurrent Refresh can execute the refresh cycle concurrently with the CPU as long as there is no DRAM conflict. (i.e. we enhance performance by allowing refresh to work on the DRAM and the CPU to work on the Cache RAM at the same time.) To quiet refresh noise on the Motherboard, all RAS are staggered during refresh cycle.

CPU SPEED	DRAM SPEED	DRAM WAIT STATE
486-20MHz	80NS (CMOS)	(W0WS, R0WS)
486-25MHz	80NS (CMOS)	(W0WS, R1WS)
486-33MHz	80NS (CMOS)	(W0WS, R1WS)
486-50MHz	80NS (CMOS)	(W1WS, R2WS)

Table B: Wait States / DRAM Speeds for 486 systems

DRAM Configuration	Row Address	Column Address
256K Page Mode	(A19-A11)	(A10-A2)
1M Page Mode	(A21-A12)	(A11-A2)
4M Page Mode	(A23-A13)	(A12-A2)

Table C : Row / Column Address for Different Types of DRAM

2.10 Shadow RAM

For those BIOS Call Intensive Application Softwares, it is not efficient to run BIOS Call in low speed ROM. Moving all ROM contents to a high speed DRAM will largely improve the performance of a BIOS Call intensive program.

ET6000 allows all Motherboard ROM and Adapter Card ROM to be shadowed on the Motherboard DRAM as long as they are resident in (C0000-CFFFF), (D0000-DFFFF), (E0000-EFFFF), or (F0000-FFFFF) range. If the Adapter ROM is on the Motherboard, it can still be shadowed.

2.11 Bus Interface Between CD, MAXD and SD Bus

The ET6000 Data Buffer provides interface between three distinct buses: the CD Bus, MAXD Bus and the SD Bus. The CD Bus (CD<15:0>) is the CPU Data Bus. The Memory Data Bus connects to the 32-bit wide local DRAM. The MAXD Bus (MD<15:0>) are Memory Address Bus and 16-bit bus for on board I/O devices which use the MD bus. Off board I/O devices would situate on the SD bus (SD<15:0>).

The data conversion can be done on either an 8-bit, 16-bit wide bus. The bus size 16(BS16-) feature is supported allowing the 486 to acknowledge the external 16-bit data buses. The 486 will make adjustments for correct transfer of the upper bytes.

2.12 Parity Generation and Checking Logic

The ET6000 generates byte-wise even Memory Parity Bits for both the CPU and DMA/Master Write to the local DRAM. The Memory Parity Bits (MP<3:0>) are strobed into the DRAM along with the write data, thus, they are directly connected to the DRAM.

During a local DRAM read cycle, the data and even parity bits are read from the DRAM onto the CD Bus and the MP Bus, respectively. The data is latched internally during the parity checking period. The byte-wise parity errors are gated with byte enable bits (BH0#, BE3#) to generate the latched parity error which would be asserted one system clock later, at the end of the read operation.

As soon as the latch parity error is asserted, it will stay active until cleared by another local DRAM read cycle that does not encounter parity error.

2.13 Numerical Coprocessor Interface Logic

The ET6000 Data Buffer supports the floating point errors handled with the i486 microprocessor.

The trailing edge of FERR- will trigger flip-flop to generate the IRQ signal which will be ORed with WTINTR and become interrupt level 13 (IRQ13-). After FERR- is assereted, the interrupt service routine handles the error and then clears the interrupt by executing a dummy write to I/O port F0h. The IGNNE- signal is also activated by this. It allows non-control instructions to be executed prior to the time the FERR- signal is reset by the i486. This is implemented for AT compatibility.

2.13 14.318MHz and Divided by 12 Counter

The ET6000 Data Buffer also provides the logic to generate a 14.318MHz OSC signal and a divided by 12 OSC119 signal which are used on the system board.

3.0 Configuration Registers

The ET6000 has internal registers used for system configuration and internal control. These areas are accessed through IO Ports 22H and 23H. Each access to an internal register is accomplished by first, writing its index into Port 22H. This index is then used to gate the appropriate internal register and the control data is accessed through Port 23H.

There are eighteen configuration registers in ET6000. The definitions of these registers are as follows:

TABLE D

System Configuration Register

Index	Bits	Values and Functions	Default
10H	0	RAM at A0000H to BFFFFH 0: AT Bus Cycle 1: Local Bus Cycle	0
	1	Wait for HALT after KBDRST 0: Do not wait for HALT 1: Wait for HALT	0
	2	Fast Reset Delay 0: Do not use delay 1: Wait for 2us delay	0
	3	Slow refresh at 95us 0: Disable slow refresh 1: Enable slow refresh	0
	4	Refresh Selection 0: AT Type Refresh 1: concurrent Refresh	0
	5	Reserved	
	7:6	00: Turbo / Non-turbo 01: Local device supported 10: Suspend mode 11: Not allowed	00

TABLE E

CACHE Configuration and Non-Cacheable Block Size Register

Index	Bits	Values and Functions	Default
11H	3:0	Reserved	
	4	0: 2 Bank DRAM 1: 4 Bank DRAM	0
	7:5	Non-Cacheable Block Size 000: Disabled 001: 512KB 010: 1MB 011: 2MB 100: 4MB 101: 8MB 110: 16MB 111: 32MB	000

TABLE F

Non-Cacheable Block Address Register

Index	Bits	Values and Functions	Default
12H	0	Reserved	0
	7:1	Non-Cacheable Address A25 to A19	0

TABLE G

DRAM Bank and Type Configuration Register

Index	Bits	Values and Functions	Default
13H	1:0	Bank0 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	01
	3:2	Bank1 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00
	5:4	Bank2 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00
	7:6	Bank3 DRAM Type 00: None 01: 256K 10: 1M 11: 4M	00

TABLE H

DRAM Configuration Register

Index	Bits	Values and Functions	Default
14H	0	Write Cycle Wait States 0: 0WS 1: 1WS	1
	2:1	Read Cycle Wait States 00: 0WS 01: 1WS 10: 2WS 11: 3WS	01
	3	RAS precharge time 0: 1.5 SYSCLK (not for 33MHz and 50MHz) 1: 2.5 SYSCLK	1
	4	RAS to CAS time 0: 1 SYSCLK (not for R0WS) 1: 2 SYSCLK	1
	5	0: Disable ROMCS at memory range C0000-DFFFF 1: Enable ROMCS at memory range C0000-DFFFF (NOTE: if C0000-DFFFF is enabled for ROMCS, then memory address cannot be SHADOWED)	0
	6	0: Enable on-board memory range 512K-640K 1: Disable on-board memory range 512K-640K	0
	7	0: Enable on-board memory range 15M-16M 1: Disable on-board memory range 15M-16M	0

TABLE I

Shadow RAM Configuration Register

Index	Bits	Values and Functions	Default
15H	0	RAM at C0000H-CFFFFH 0: Read/Writ 1: Read Only	0
	1	Access ROM/RAM at C0000H-CFFFFH 0: Accessed on-board ROM, ie AT bus cycle 1: Access Shaow RAM C0000H-CFFFFH enabled	0
	2	RAM AT D0000H-DFFFFH 0: Read/Writ 1: Read Only	0
	3	Access ROM/RAM at D0000H-DFFFFH 0: Accessed on-board ROM, ie AT bus cycle 1: Access Shaow RAM D0000H-DFFFFH enabled	0
	4	RAM AT E0000H-EFFFFH 0: Read/Writ 1: Read Only	0
	5	Access ROM/RAM at E0000H-EFFFFH 0: Accessed on-board ROM, ie AT bus cycle 1: Access Shaow RAM E0000H-EFFFFH enabled	0
	6	Access ROM/RAM at F0000H-FFFFFH (System BIOS ROM) 0: Read from ROM, Write to RAM 1: Read from Shadow RAM, Write will be protected (will not be written into RAM)	0
	7	Shadow RAM at C0000H-FFFFFH 0: Non Cacheable 1: Cacheable and Cache write protected	0

ET6000 Pin Description

Pin No.	Pin Type	Symbol	Description
Clocks			
41	I	CLKIN	Oscillator input. The frequency should be the same as the CPU's clock.
42	I	EXACLK	AT BUS CLOCK input from crystal.
39	I	CX1	14.318MHz input from crystal.
40	O	CX2	14.318MHz output to crystal.
37	O	OSC119	14.318MHz divided by 12 clock output
13	O	BUSCLK	8MHz AT BUS CLOCK.
Reset Contrl			
9	I	PWRGD	Power On Reset.
156	O	RESET3	CPU Reset. Assereted by either power on initializing the CPU or bringing the CPU back to real mode from the protected mode.
43	O	RESET4	System Reset. Assereted during Power On to reset the whole system.
CPU Control			
141	I	ADS-	An input from the CPU indicates address and cycle definitions are valid. It is an active low.
154	I	MIO-	CPU Status. A high means this is a memory cycle and low indicates an IO cycle.
148	I	WR-	CPU Status. A high means this is a write cycle and a low indicates a read cycle.
155	I	DC-	CPU status. A HIGH means it is a data access cycle, and a Low indicates code access.
145	I/O	RDYN-	This pin generates the CPU READY signal to alert the CPU that the cycle has finished with the exception of the coprocessor cycle. The MATH co-processor will generate its own CPU ready, thus, READY- acts as an input in this case.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
CPU Control (Continued)			
153, 152 151, 149	I/O	BE<3:0>-	INPUT BYTE ENABLE signals from the CPU. They become output signals at the DMA cycles to reflect XA0, SBHE-.
147	I	PHLDA	When active, it indicates the processor has released the bus in response to HOLD request. This signal is connected to the processor HLDA signal.
81	O	NMI	Non-Maskable Interrupt to the CPU.
158	O	HOLD	An active HIGH used to request the CPU to relinquish the bus to DMA, Master or Refresh cycle.
116-121,	I	A<7:2>	CPU Address.
103-105,	I	A<19:17>	
18		CAS3-/A25	
97-99,	I	A<24:22>	
101	I	A21	
96	I	A31	
106-112,	I/O	A<16:10>	CPU Address. Output signals during DMA and MASTER MODE.
114-115	I/O	A<9:8>	
102	I/O	A20	
Cache Control			
157	O	KEN-	Active low signal to indicate that the current cycle is cacheable.
122	O	BRDY-	Active low signal. Burst Ready to 486
142	I	BLAST-	BLAST- input from 486. Indicates that the burst cycle is complete after the next BRDY- is returned. Active low.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
DRAM Control			
160	O	DWROMCS-	Dual functional pin. It is data write enable for DRAM write cycle and ROM chip select for ROM cycle.
22	O	CAS0-	Column Address Strobe for DRAM bank 0.
21	O	CAS1-	Column Address Strobe for DRAM bank 1.
19	O	CAS2-	Column Address Strobe for DRAM bank 2. By combining with BE<3:0> each byte can be controlled individually
18	O	CAS3-	Column Address Strobe for DRAM bank 3. By combining with BE<3:0> each byte can be controlled individually
23-24, 21 22	O	RAS<1:0>- CAS1-/RAS3- CAS0-/RAS2-	Row Address Strobe 0 to 3 corresponding to bank 0 to 3. It should be buffered before tying to the DRAMs. These are active low signals.
138-140, 124-129, 131-132	I/O	MAXD<10:8> MAXD<7:2> MAXD<1:0>	DRAM Memory Address. They should be buffered before tying to the DRAMs and also used as refresh address output during REF cycle.
Data Bus			
61-69, 71-80, 82-25, 87-95	I/O	CD<31:23> CD<22:13> CD<12:9> CD<8:0>	Regular Mode: Connect to the CPU Data Bus. CD<15:0> would be driven during CPU read and DMA write memory cycle Bypass Mode: Connect to CPU Data and DRAM Data Bus. CD<15:0> will pass through transparent latch to parity generation and checking logic.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Data Bus (Continued)			
5-2	I/O	MP<3:0>	Memory Parity Bit 0 to 3. Output for CPU or DMA write to memory, and input for CPU or DMA read from memory. EVEN parity bit is generated on all write data cycles. This information must be driven back into MP<3:0> with the same timing as read data to insure the correct parity check. MP3 refers to Byte3 PARITY, MP2 refers to Byte2 Parity ans so on.
133-140, 124-129, 131-132	I/O I/O I/O	MAXD<15:8> MAXD<7:2> MAXD<1:0>	ISA Data Bus Bits <15:0> and memory address bus
AT Control			
35	O	L1MCS-	Low 1 Meg Chip Select to generate SMEMR- and SMEMW- for the AT Bus command which is an indication that it is within the first 1 Meg address range. It is an active low signal.
29	I/O	XBHE-	Peripheral Byte High Enable. An active LOW signal which indicates that the data is on the upper byte. It is an output during the CPU and DMA cycle and an input during the master CYCLE.
59-58, 26	I/O	XA<1:0> A20M	These signals are latched at address outputs during CPU cycles and inputs during DMA or Master cycles.
8	O	BALE	Bus Address Latch Enable. The trailing edge latches the valid address for the AT Slot.
55	I/O	MEMR-	AT Bus Memory Read. It is an output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
AT Control (Continued)			
54	I/O	MEMW-	AT Bus Memory Write. An output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.
56	I/O	IOR-	AT Bus IO Read. It is an output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.
57	I/O	IOW-	AT Bus IO Write. It is an output if the CPU is controlling the bus and an input if the DMA is in control. An active LOW signal.
14	I	0WS-	Zero Wait State. When LOW, the AT Bus will terminate its current cycle without additional wait state.
11	I/O	CHRDY	IO Channel Ready. When LOW, the AT Bus will insert wait states until this signal returns to HIGH.
30	I	MCS16-	16 Bit Memory Chip Select. When LOW, it is a 16 bit memory transfer from the AT Slot. When HIGH, an 8 bit memory transfer
31	I	IOCS16-	16 Bit IO Chip Select. When LOW, it is a 16 bit IO transfer. When HIGH, an 8 bit memory transfer.
10	I	IOCHCK-	An AT Bus error condition will cause an NMI to be generated.
15	O	SDEN-	Slot Data Enable. Enables the buffer that drives the data bus onto the slot an back.
32	O	ACK-	An active LOW, tied to the C206 ACK - pin.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
AT Control (Continued)			
27	I	MISC	An active LOW signal indicating a local BUS cycle, not an AT cycle.
45	O	INTA-	Interrupt Acknowledge. Asserted for CPU to read the interrupt vector from the XD Bus.
28	O	SDIR0-	System Data Bus Direction for the low byte. The data is moved from SD Bus to MD Bus when SDIR0- is LOW. The data is moved from MD Bus to SD Bus when SDIR0- is HIGH
34	O	SDIR1-	System Data Bus Direction for the high byte. The data is moved from SD Bus to MD Bus when SDIR1- is LOW. The data is moved from MD Bus to SD Bus when SDIR1- is HIGH
144	O	BS16-	A bus size of 16 caused the CPU to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a singale cycle. BS16- is an active LOW.
6	O	SAON-	An active LOW signal indicating a LA BUS cycle.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Refresh			
12	I/O	REF-	An output to indicate a refresh cycle. For Master Mode, it is an input from the Master Device to indicate a refresh cycle.
DMA Control			
48	I	DMAHRQ	HOLD REQUEST from DMA or other Bus Master for bus control.
53	I	AEN8-	Address Enable for 8 bit DMA transfer. An active LOW signal.
52	I	AEN16-	Address Enable for 16 bit DMA transfer. An active LOW signal.
46	O	HLDAOUT-	Indicates that the CPU has relinquished the bus to other masters or DMA.
33	I	MASTER-	When LOW, it indicates that a bus master other than the CPU or DMA is owning the bus.
49	I	ADSTB8	Address Strobe for 8 bit DMA transfer.
51	I	ADSTB16	Address Strobe for 16 bit DMA transfer.
7	O	AEN	Address enable signal, drive AT Bus AEN directly.
144	O	BS16-	A bus size of 16 caused the CPU to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a singale cycle. BS16- is an active LOW.
Decodes			
16	O	8042CS-	8742 Keyboard Controller Chip Select. An active LOW signal.
47	O	RTCAS-	Real Time Clock Address Strobe. It should tie to the 82C206. The trailing edge latches the address onto the CA Bus.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Floating Point Interface			
146	I	FERR-	Tied to the 486 FERR- pin.
159	O	IGNNE-	Connected to the 486 IGNNE- pin.
145	I	RDYIN-	This pin generates the NPU READY signal to alert the NPU that the cycle has finished.
Miscellaneous			
44	I	TMOUT2	Output from the 8254 timer located inside the 82C206.
38	O	TMGATE	TIMER GATE 2 enables the counter two of the 8254. Used for tone generation for the speaker.
36	O	SPKOUT	Speaker data used to drive the speaker. Buffer required.
27	I	MISC	This pin will connect to a hardwired clock switching control signal, if it exists. If bit 2 of register 10 is programmed to 0 then a high on this signal will keep the system in high speed mode. Otherwise, the system will enter low speed mode if this pin is low. The system will stay in high speed mode and does not count on this signal at all if bit 2 of register 10 is programmed to 1. Tied to high if not used.

ET6000 Pin Description (Continued)

Pin No.	Pin Type	Symbol	Description
Power			
20, 60 100, 143	I	VDD	Power Supply
Ground			
1, 17 25, 50 70, 86 113, 130 150	I	VSS	Ground

4.0 ET6000 Pin Driving Definition

Pin Number	Pin Name	I/O Type	Driving
1	VSS	I	
2	MP0	I/O	6 ma
3	MP1	I/O	6 ma
4	MP2	I/O	6 ma
5	MP3	I/O	6 ma
6	SAON-	O	4 ma
7	AEN	O	12 ma
8	BALE	O	4 ma
9	PWRGD	I	
10	IOCHCK-	I	
11	CHRDY	I/O	6 ma
12	REF-	I/O	4 ma
13	BUSCLK	O	6 ma
14	0WS-	I	
15	SDEN-	O	4 ma
16	8042CS-	O	4 ma
17	VSS	I	
18	CAS3-	I/O	12 ma
19	CAS2-	O	12 ma
20	VDD	I	
21	CAS1-	O	12 ma
22	CAS0-	O	12 ma
23	RAS1-	O	12 ma
24	RAS0-	O	12 ma
25	VSS	I	
26	A20M	I/O	4 ma
27	MISC	I	
28	SDIR0-	O	4 ma

4.0 ET6000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
29	XBHE-	I/O	4 ma
30	MCS16-	I	
31	IOCS16-	I	
32	ACK-	O	4 ma
33	MASTER-	I	
34	SDIR1-	O	4 ma
35	L1MCS-	O	4 ma
36	SPKOUT	O	4 ma
37	OSC119	O	6 ma
38	TMGATE	O	4 ma
39	CX1	I	
40	CX2	I	
41	CLKIN	I	
42	EXACLK	I	
43	RESET4	O	4 ma
44	TMOUT2	I	
45	INTA-	O	4 ma
46	HLDAOUT	O	4 ma
47	RTCAS	O	4 ma
48	DMAHRQ	I	
49	ADSTB8	I	
50	VSS	I	
51	ADSTB16	I	
52	AEN16-	I	
53	AEN8-	I	
54	MEMW-	I/O	4 ma
55	MEMR-	I/O	4 ma
56	IOR-	I/O	4 ma

4.0 ET6000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
57	IOW-	I/O	4 ma
58	XA0	I/O	4 ma
59	XA1	I/O	4 ma
60	VDD	I	
61	CD31	I/O	4 ma
62	CD30	I/O	4 ma
63	CD29	I/O	4 ma
64	CD28	I/O	4 ma
65	CD27	I/O	4 ma
66	CD26	I/O	4 ma
67	CD25	I/O	4 ma
68	CD24	I/O	4 ma
69	CD23	I/O	4 ma
70	VSS	I	
71	CD22	I/O	4 ma
72	CD21	I/O	4 ma
73	CD20	I/O	4 ma
74	CD19	I/O	4 ma
75	CD18	I/O	4 ma
76	CD17	I/O	4 ma
77	CD16	I/O	4 ma
78	CD15	I/O	4 ma
79	CD14	I/O	4 ma
80	CD13	I/O	4 ma
81	NMI	O	4 ma
82	CD12	I/O	4 ma
83	CD11	I/O	4 ma
84	CD10	I/O	4 ma

4.0 ET6000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
85	CD9	I/O	4 ma
86	VSS	I	
87	CD8	I/O	4 ma
88	CD7	I/O	4 ma
89	CD6	I/O	4 ma
90	CD5	I/O	4 ma
91	CD4	I/O	4 ma
92	CD3	I/O	4 ma
93	CD2	I/O	4 ma
94	CD1	I/O	4 ma
95	CD0	I/O	4 ma
96	A31	I	
97	A24	I/O	4 ma
98	A23	I	
99	A22	I	
100	VDD	I	
101	A21	I	
102	A20	I	
103	A19	I	
104	A18	I	
105	A17	I	
106	A16	I/O	4 ma
107	A15	I/O	4 ma
108	A14	I/O	4 ma
109	A13	I/O	4 ma
110	A12	I/O	4 ma
111	A11	I/O	4 ma
112	A10	I/O	4 ma

4.0 ET6000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
113	VSS	I	
114	A9	I/O	4 ma
115	A8	I/O	4 ma
116	A7	I	
117	A6	I	
118	A5	I	
119	A4	I	
120	A3	I	
121	A2	I	
122	BRDY-	O	12 ma
123	RDY-	O	12 ma
124	MAXD7	I/O	6 ma
125	MAXD6	I/O	6 ma
126	MAXD5	I/O	6 ma
127	MAXD4	I/O	6 ma
128	MAXD3	I/O	6 ma
129	MAXD2	I/O	6 ma
130	VSS	I	
131	MAXD1	I/O	6 ma
132	MAXD0	I/O	6 ma
133	MAXD15	I/O	6 ma
134	MAXD14	I/O	6 ma
135	MAXD13	I/O	6 ma
136	MAXD12	I/O	6 ma
137	MAXD11	I/O	6 ma
138	MAXD10	I/O	6 ma
139	MAXD9	I/O	6 ma
140	MAXD8	I/O	6 ma

4.0 ET6000 Pin Driving Definition (Continued)

Pin Number	Pin Name	I/O Type	Driving
141	ADS-	O	4 ma
142	BLAST-	I	
143	VDD	I	
144	BS16-	O	4 ma
145	RDYIN-	I	
146	FERR-	O	
147	PHLDA	O	
148	WR-	O	4 ma
149	BE0-	O	4 ma
150	VSS	I	
151	BE1-	O	4 ma
152	BE2-	O	4 ma
153	BE3-	O	4 ma
154	MIO-	O	4 ma
155	DC-	O	4 ma
156	RESET3	O	12 ma
157	KEN-	O	12 ma
158	HOLD	O	4 ma
159	IGNNE-	O	4 ma
160	DWROMS-	O	6 ma

4.1 ET6000 Absolute Maximum Ragings

	Symbol	Min	Max	Units
Supply Voltage	VDD		7.0	V
Input Voltage	VIN	-0.5	5.5	V
Output Voltage	VOUT	-0.5	5.5	V
Operating Temperature	Top	-2.5	50	C
Storage Temperature	Tstg	-40	125	C

4.2 82C490SX Operating Condition

	Symbol	Min	Max	Units
Supply Voltage	VDD	4.75	5.25	V
Ambient Temperature	TA	0	50	C

4.3 ET6000 DC Characteristics

	Symbol	Min	Max	Units
Input Low Voltage	VIL			
TTL Level (All pins except PWRGD)			0.8	V
SHMT Level (PWRGD pin)			1.0	V
Input High Voltage	VIH			
TTL Level (All pins except PWRGD, TURBO- and CLK2IN)		2.0		V
CLK2IN Level		3.7		V
SHMT Level (PWRGD and TURBO- pins)		4.0		V
Output Low Voltage	VOL		0.45	V
Output High Voltage	VOH	2.4		V
Input Low Current AT VIN=VSS	IIL	-10	10	uA
Input High Current AT VIN=VDD	IIH	-10	10	uA
Tri-State Output OFF Current LOW	IOZL		-10	uA
Tri-State Output OFF Current HIGH	IOZH		10	uA
Output Leakage Current	IOH		TBD	
Output Short Circuit Current	IOS		TBD	
Power Supply Current	EDD			
@20MHz			150	mA
@25MHz			200	mA
@33MHz			230	mA
Input Capacitance	CIN		7	pF
Output or I/O Capacitance	COUT		10	pF

4.3 ET6000 AC Characteristics

(TA = 0 C to 70 C, VDD = 5V ± 5%)

4.3.1 Clock Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
CLK Period	T101	40		30		20		ns
CLK high time at 2.0v	T102	14		12		8		ns
CLK high time at 3.7v	T103	10		8		5		ns
CLK low time at 2.0v	T104	14		12		8		ns
CLK low time at 0.8v	T105	10		8		5		ns
CLK fall time (3.7v to 0.8v)	T106		5		4		2	ns
CLK rise time (0.8v to 3.7v)	T107		5		4		2	ns
BUSCLK Period	T108	80	240	61	182	40	120	ns
BUSCLK high time at 3.7v	T109	47		15		12		ns
BUSCLK low time at 0.8v	T110	47		15		12		ns
BUSCLK fall time (3.7v to 0.8v)	T111		8		6		5	ns
BUSCLK rise time (0.8v to 3.7v)	T112		8		6		5	ns

4.3.2 Reset Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
RESET3 active delay from CLK high	T113		13		10		7	ns
RESET3 inactive delay from CLK high	T114	3	13		10		7	ns
RESET3 Pulse Width	T115	40		40		40		CLK
RESET4 active delay from CLK high	T116		30		24		15	ns

Notes:

All AC timing parameters are specified under capacitive load of 85pF, unless stated otherwise.

(TA = 0 C to 70 C, VDD = 5V ± 5%)

4.3.2 Reset Timing (Continued)		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
RESET4 inactive delay from CLK high	T117		30		24		15	ns
RESET3 active delay from PWRGD active	T118	3		3		3		CLK
RESET4 Pulse Width	T119	40		40		40		CLK
RESET4 active delay drom PWRGD inactive	T120	2		2		2		CLK

4.3.3 AT Cycle Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
BALE active from BUSCLK low	T123	11		9		8		ns
BALE inactive from BUSCLK low	T124	11		9		8		ns
XA[1:0],A[16:0],XBHE- valid from BALE high	T125		7		5		4	ns
Command active from BUSCLK low	T126		8		6		5	ns
Command inactive from BUSCLK high	T127	3	8	2	6	2	5	ns
MCS16- setup to BALE low	T128	20		15		13		ns
MCS16- hold from BALE low	T129	13		10		9		ns
IOCS16- setup to BUSCLK low	T130	24		18		15		ns
IOCS16- hold from BUSCLK low	T131	13		10		9		ns
IOCHRDY setup to ICLK low	T132	7		5		4		ns
IOCHRDY hold from ICLK low	T133	7		5		4		ns

(TA = 0 C to 70 C, VDD = 5V ± 5%)

4.3.3 AT Cycle Timing (Continued)		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
0WS- setup to BUSCLK high	T134	14		11		9		ns
0WS- hold from BUSCLK high	T135	13		10		9		ns
SDEN- active from BUSCLK low	T138		13		10		9	ns
SDEN- inactive from SCLK	T139		30		24		20	ns
MEMR-; MEMW- active from BUSCLK high	T141		8		6		5	ns
0WS- setup to BUSCLK low	T142	18		14		12		ns
0WS- hold from BUSCLK low	T143	17		13		11		ns

4.3.4 Arbitration Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
SCLK low from CLK high	T144	3	9	2	7	2	5	ns
SCLK high from CLK low	T145	3	9	2	7	2	5	ns
HOLD active from SCLK low	T146		15		12		9	ns
HOLD inactive from SCLK low	T147	5	15	4	12	3	9	ns
HLDAOUT active from HLDA high	T148		30		24		20	ns
HLDAOUT inactive from HLDA low	T149		30		24		20	ns

(TA = 0 C to 70 C, VDD = 5V ± 5%)

4.3.5 Refresh Cycle Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
HOLD active from SCLK low	T150		15		12		9	ns
HOLD inactive from SCLK low	T151	5	15	4	12	3	9	ns
REF- active from HLDA high	T152		23		18		15	ns
REF- inactive from BUSCLK high	T153		19		15		13	ns
XA[10:0] valid from BUSCLK high	T154		15		12		10	ns
XA[10:0] invalid from BUSCLK high	T155		15		12		10	ns
MEMR- inactive from BUSCLK high	T156		9		7		6	ns
MEMR- inactive from BUSCLK high	T157		9		7		6	ns
IOCHRDY inactive from BUSCLK low	T158		8		6		5	ns
IOCHRDY active from BUSCLK low	T159		8		6		5	ns
RAS0- active from SCLK low	T160	9	28	7	22	6	18	ns
RAS0- inactive from SCLK low	T161	8	23	6	18	5	15	ns
MA[10:8] valid from SCLK high	T162		28		22		18	ns
MA[7:0] invalid from SCLK high	T163		23		18		15	ns
REF- active from SCLK high	T166		26		20		17	ns

(TA = 0 C to 70 C, VDD = 5V ± 5%)

4.3.6 Miscellaneous Cycle Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
NMI active from IOW- inactive	T167		30		24		20	ns
NMI- active from IOCHCK- low	T168		26		20		17	ns
NMI- active from LPAR- low	T169		26		20		17	ns
A20M active from IOW- inactive	T172		19		15		13	ns
8042CS- active from SA[15:0] valid	T173		30		25		21	ns
8042CS- inactive from SA[15:0] invalid	T174		30		25		21	ns
RTCAS active from IOW- active	T175		30		25		21	ns
RTCAS inactive from IOW- inactive	T176		30		25		21	ns
L1MCS- active from A31,A[25:0] valid	T179		28		22		20	ns
L1MCS- inactive from A31,A[25:0] invalid	T180		28		22		20	ns
BUSCLK high from ICLK high	T183	5	18	4	14	4	12	ns
BUSCLK low from ICLK high	T184	6	20	5	16	5	14	ns

(TA = 0 C to 70 C, VDD = 5V ± 5%)

4.3.7 ROM Cycle Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
DOROMCS- active from SCLK low	T185		28		22		18	ns
DOROMCS- inactive from SCLK low	T186		28		22		20	ns
XA0 valid from BALE high	T187		8		6		5	ns
XA0 invalid from BALE high	T188		15		12		10	ns
RDY- active from SCLK low	T189		19		15		12	ns
RDY- inactive from SCLK low	T190	6	19	5	15		12	ns

4.3.8 Memory Cycle Timing		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
SCLK high to BRDY- active delay	T201	5	26	5	21	5	15	ns
SCLK high to BRDY- inactive delay	T202	4	24	4	20	4	18	ns
ADS- low to KEN- active delay	T203	5	24	5	21	5	17	ns
SCLK low to CAS- active delay	T204	5	25	5	22	5	18	ns
SCLK high to CAS- inactive delay (Read)	T205	4	25	4	23	4	18	ns
ADS- low to column address valid delay	T206	5	20	5	18	5	15	ns
SCLK high to column address valid delay (Burst)	T207	4	20	4	18	4	15	ns
SCLK high to KEN- inactive delay	T208	5	24	5	20	5	18	ns
SCLK high to RAS- inactive delay	T209	5	30	5	25	5	19	ns
SCLK high to RAS- active delay	T210	5	32	5	27	5	18	ns
SCLK high to row address valid delay	T211	5	38	5	30	5	20	ns
SCLK low to column address valid delay	T212	5	38	5	30	5	20	ns

4.3.8 Memory Cycle Timing (Continued)		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
SCLK high to CAS- active delay (Read)	T213	5	25	5	22	5	18	ns
SCLK high to column address valid delay	T214	5	38	5	30	5	20	ns
SCLK high to RDY- active delay	T215	5	26	5	21	5	15	ns
SCLK high to RDY- inactive delay	T216	4	24	4	20	4	18	ns
SCLK low to CAS- inactive delay	T217	5	25	5	22	5	18	ns
SCLK high to DWROMCS- active delay	T218	5	23	5	20	5	16	ns
SCLK low to DWROMCS- inactive delay	T219	4	25	4	22	4	18	ns
SCLK high to CAS- active delay (Write)	T220	5	23	5	20	5	16	ns
SCLK high to CAS- inactive delay (Write)	T221	4	25	4	22	4	18	ns
SCLK low to DWROMCS- inactive delay	T222	4	25	4	22	4	18	ns

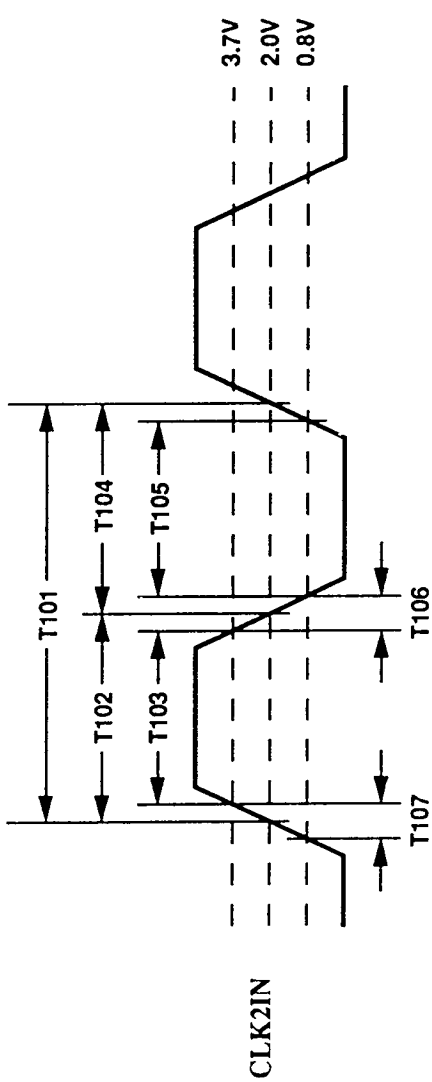
(TA = 0 C to 70 C, VDD = 5V ± 5%)

3.3.1 Oscillator and Timer Clock		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
OSC high delay from CX1 high	T307	12	31	10	28	9	26	ns
OSC low delay from CX1 low	T308	7	20	6	18	5	16	ns
OSC119 high delay from CX1 low	T309	8	23	7	20	6	19	ns
OSC119 low delay from CX1 low	T310	14	38	12	34	11	32	ns

3.3.2 CPU Write Local Memory		25MHz		33MHz		50MHz		
		Min	Max	Min	Max	Min	Max	Units
MP[3:0] valid from CD[31:0]	T311	5	17	4	14	4	9	ns
MP[3:0] hold time from CD[31:0]	T312	4	14	3	12	3	8	ns

3.3.12 Numerical Coprocessor Reset and Ready Timing		25MHz Min	25MHz Max	33MHz Min	33MHz Max	50MHz Min	50MHz Max	Units
READYO- setup time to CLK high	T364	4		3		3		ns
READYO- hold time from CLK high	T365	7		5		4		ns
READY- active from CLK high	T366	5	17	4	14	3	12	ns
READY- inactive from CLK high	T367	7	18	5	15	4	13	ns

3.3.13 Numerical Coprocessor Interface Timing		25MHz Min	25MHz Max	33MHz Min	33MHz Max	50MHz Min	50MHz Max	Units
IGNNE- active from 387FX- low	T368	5	17	4	14	3	12	ns
IGNNE- inactive from FERR- high	T369	4	12	3	10	3	9	ns
IRQ active from FERR- low	T370	5	17	4	14	3	13	ns
IRQ inactive from 387FX- low	T371	3	9	2	7	2	6	ns
IRQ active from WTINTR high	T372	4	12	3	10	3	8	ns
IRQ inactive from WTINTR low	T373	5	16	4	13	4	11	ns



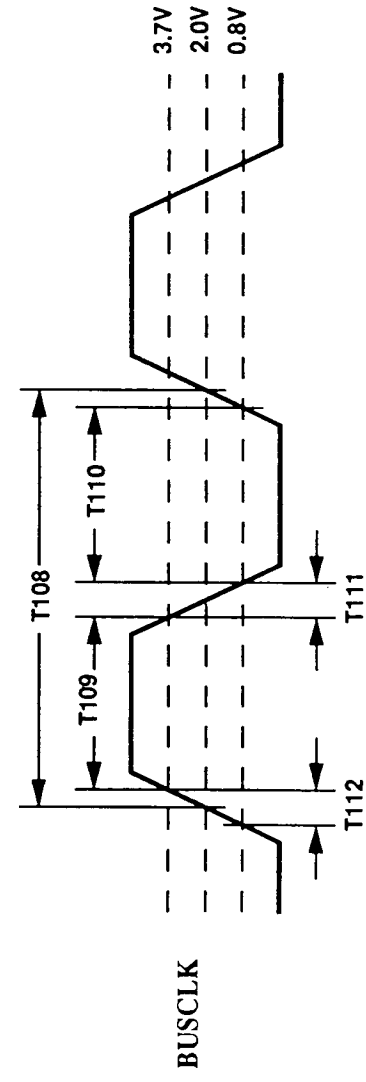


Fig. 4.3.1 Clock Timing

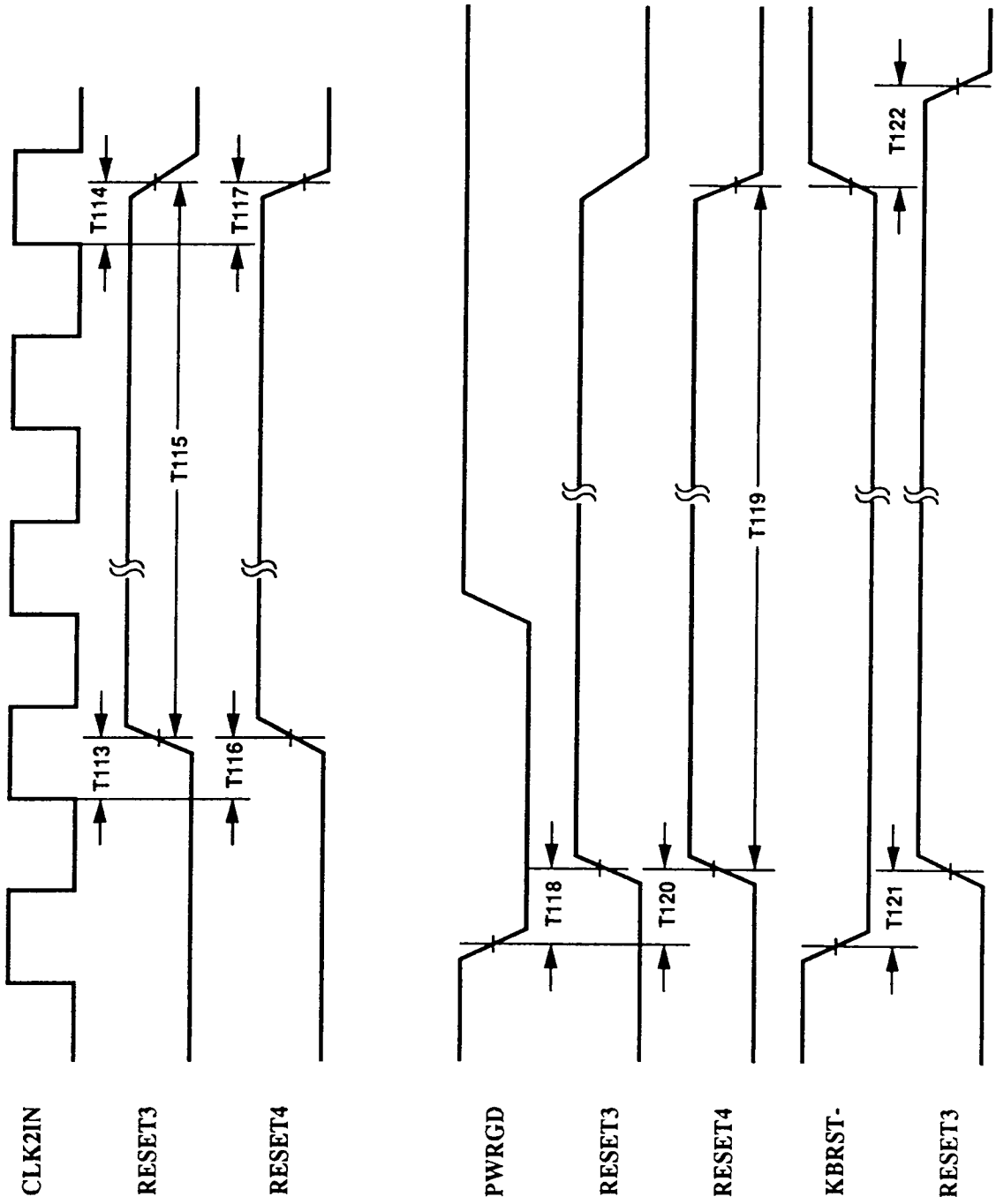


Fig. 4.3.2 Reset Timing

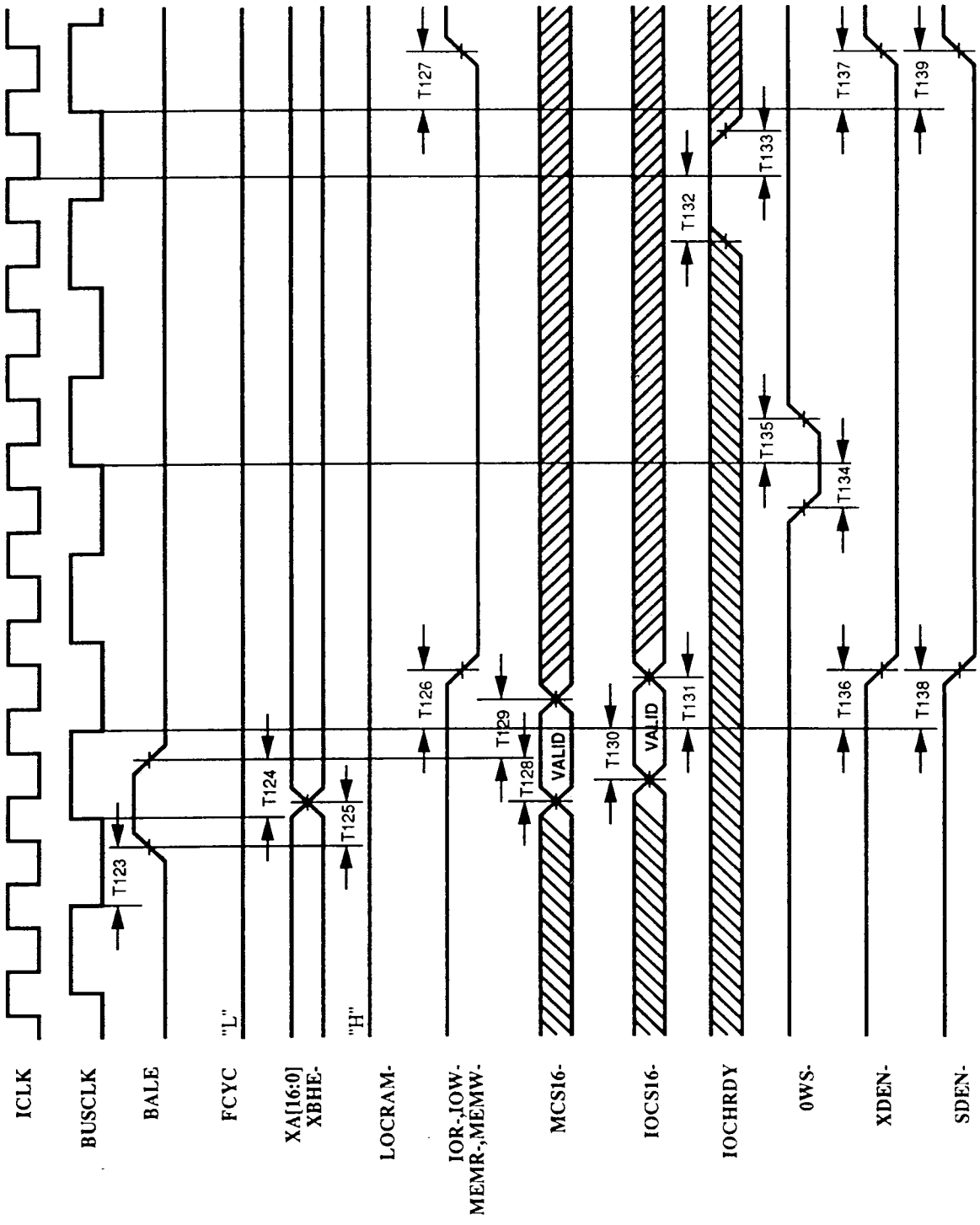


Fig. 4.3.3 8-Bit AT Cycle

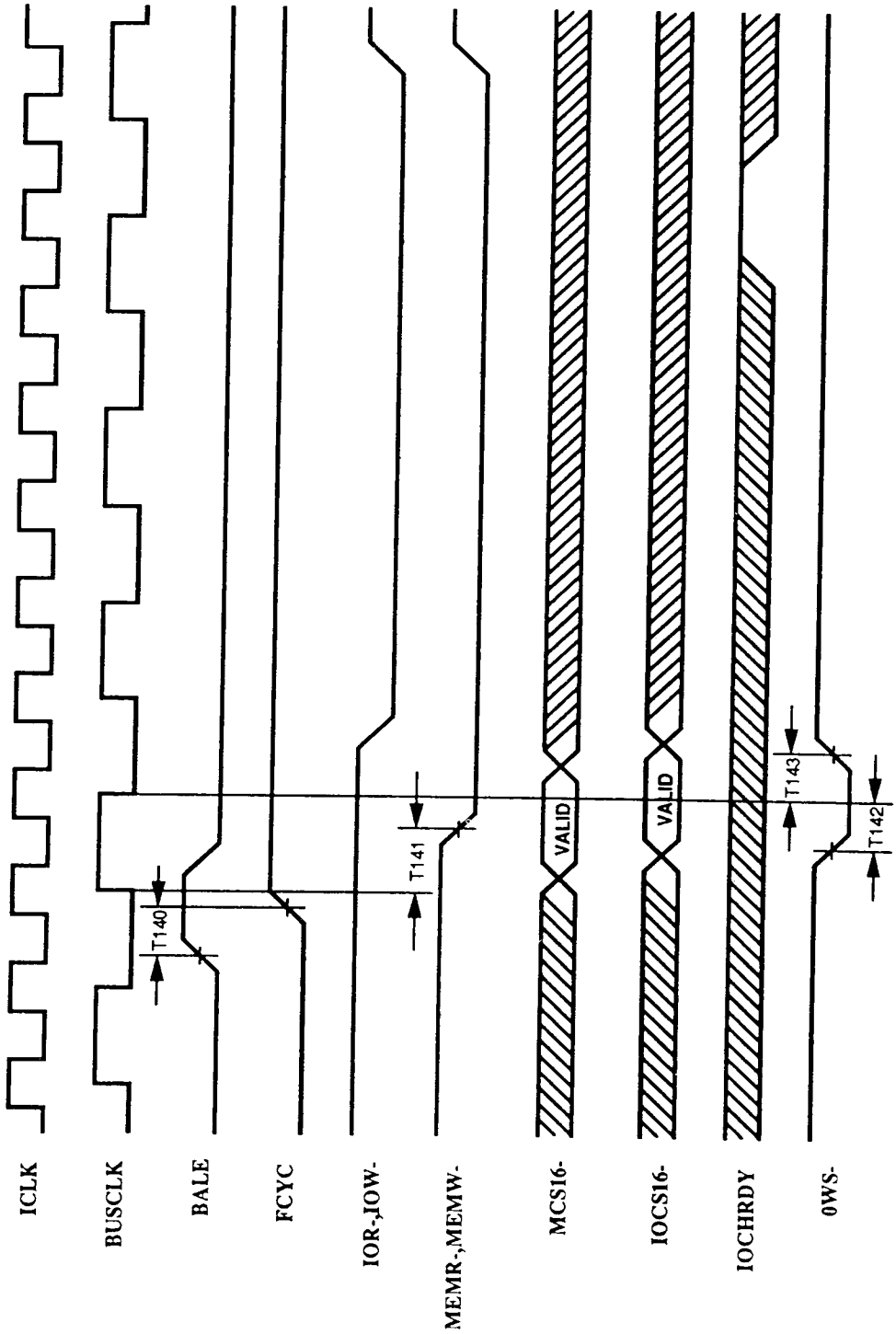


Fig. 4.3.4 16-Bit AT Cycle

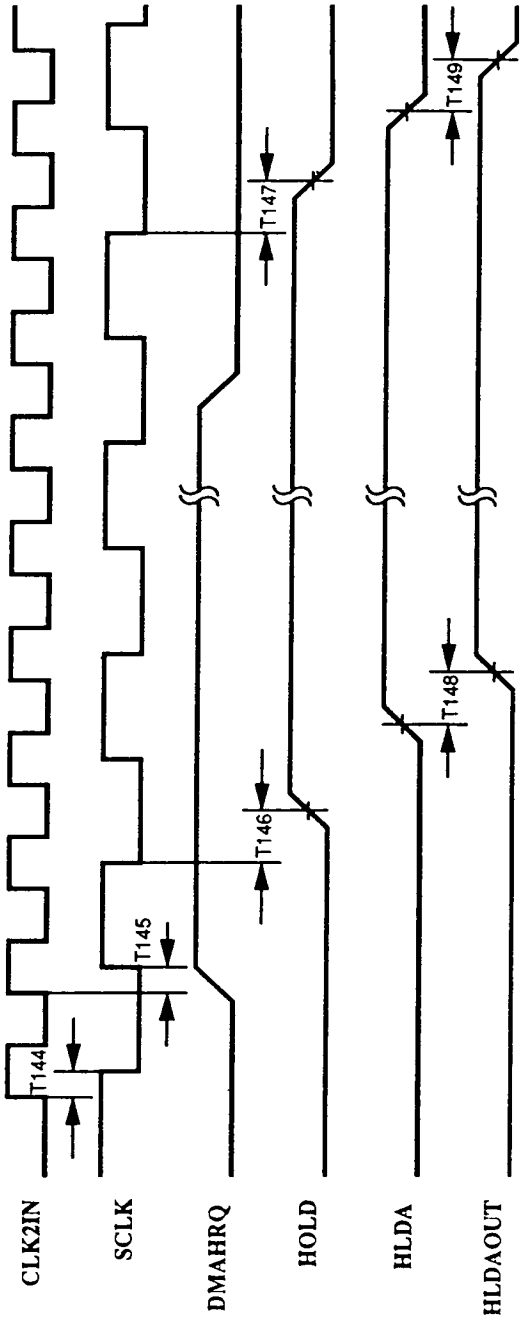


Fig. 4.3.5 DMA Arbitration

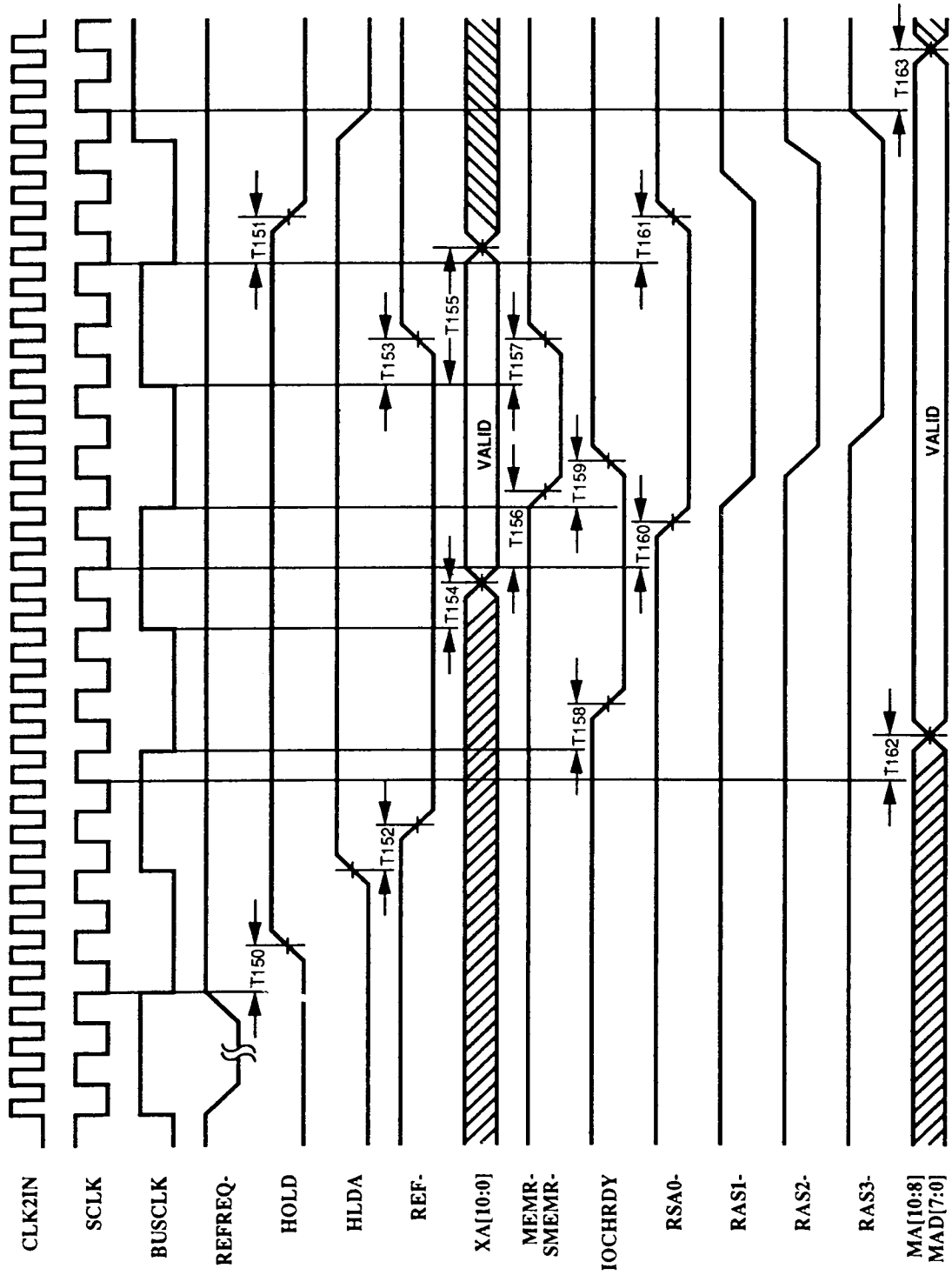


Fig. 4.3.6 AT Refresh Cycle

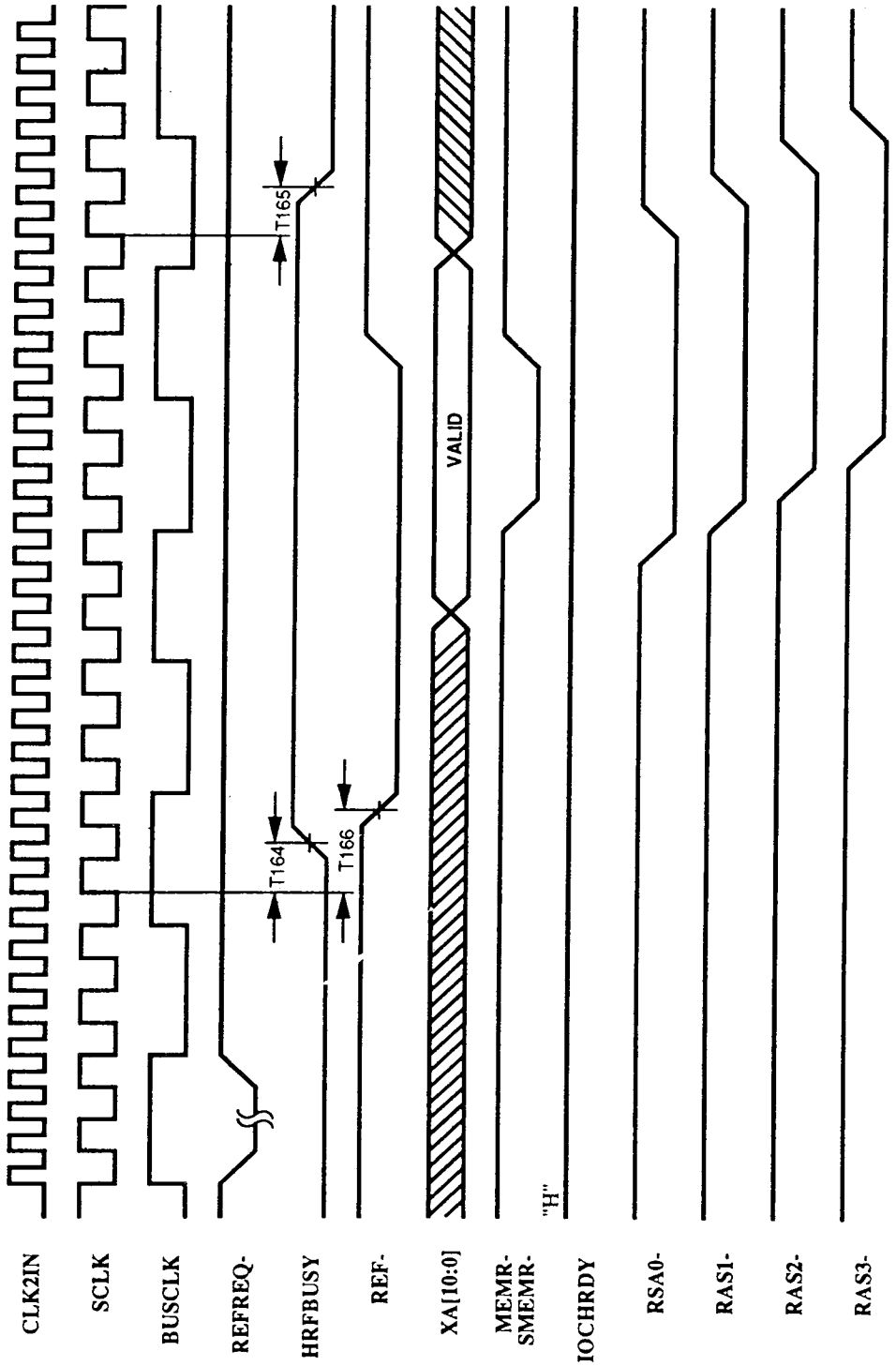


Fig. 4.3.7 Hidden Refresh Cycle

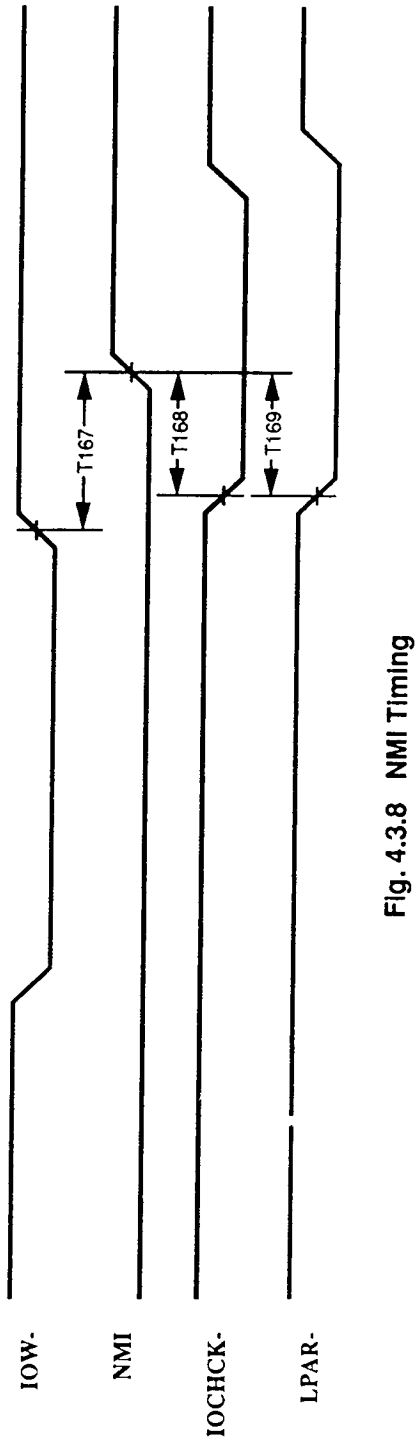


Fig. 4.3.8 NMI Timing

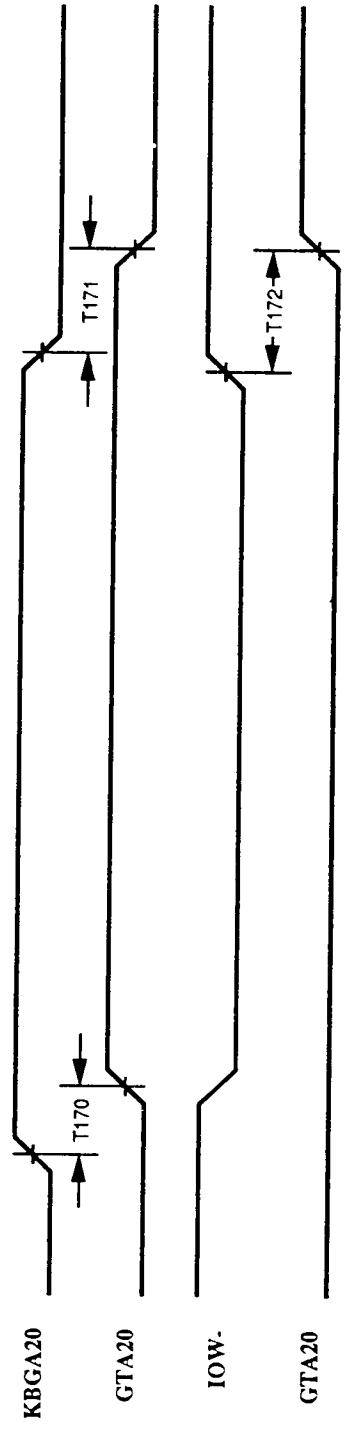


Fig. 4.3.9 GTA20 Timing

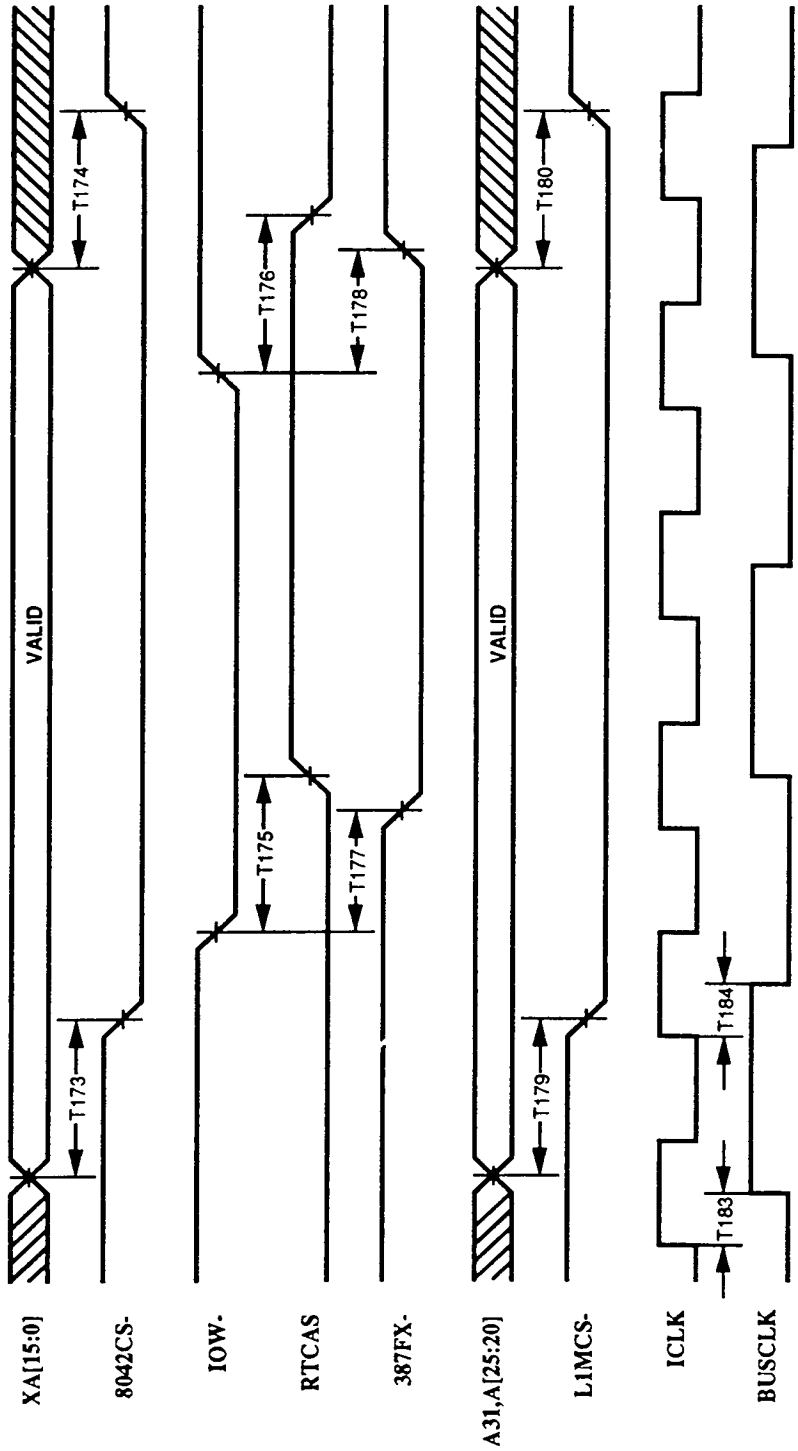


Fig. 4.3.10 Miscellaneous Timing

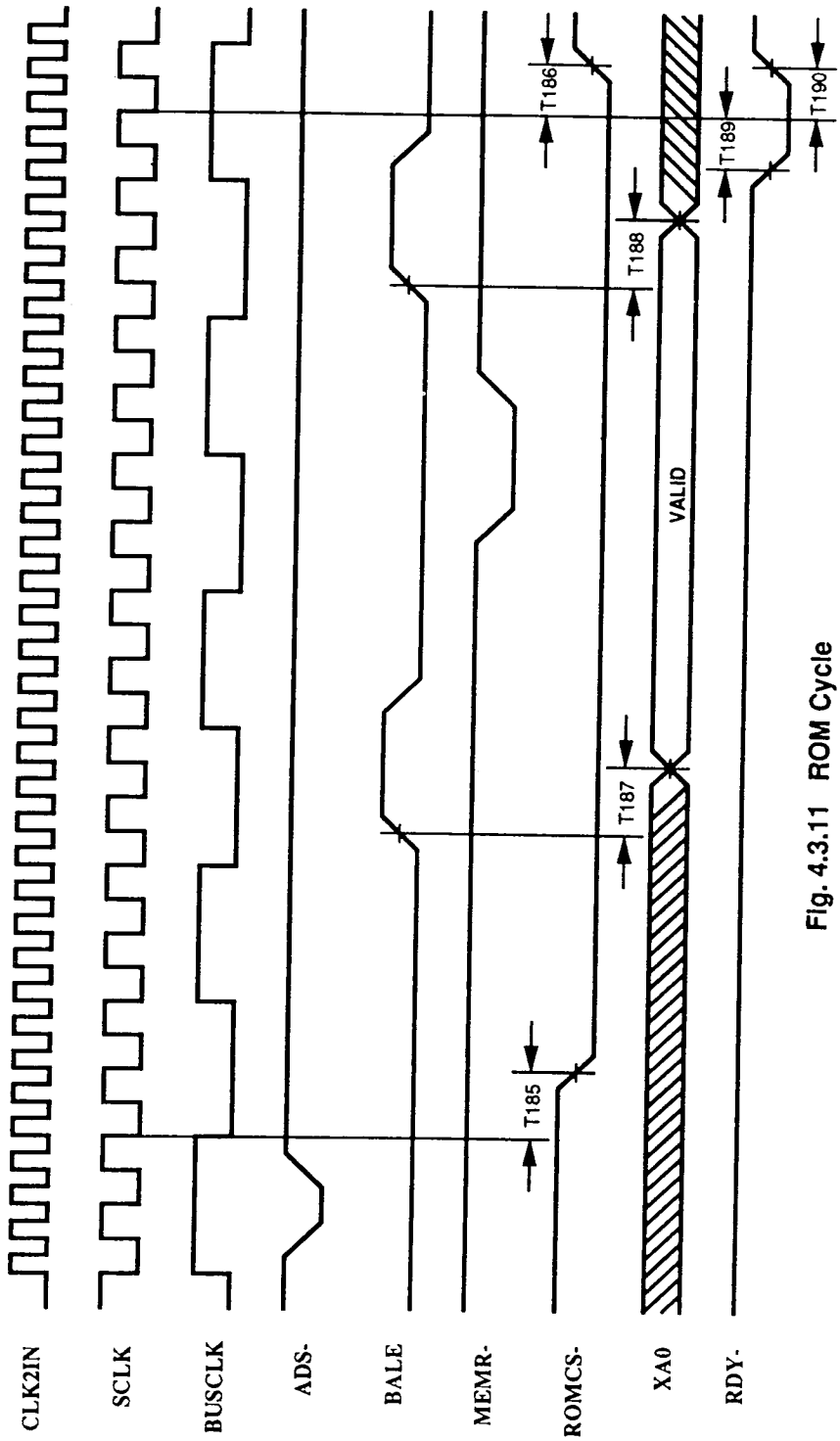
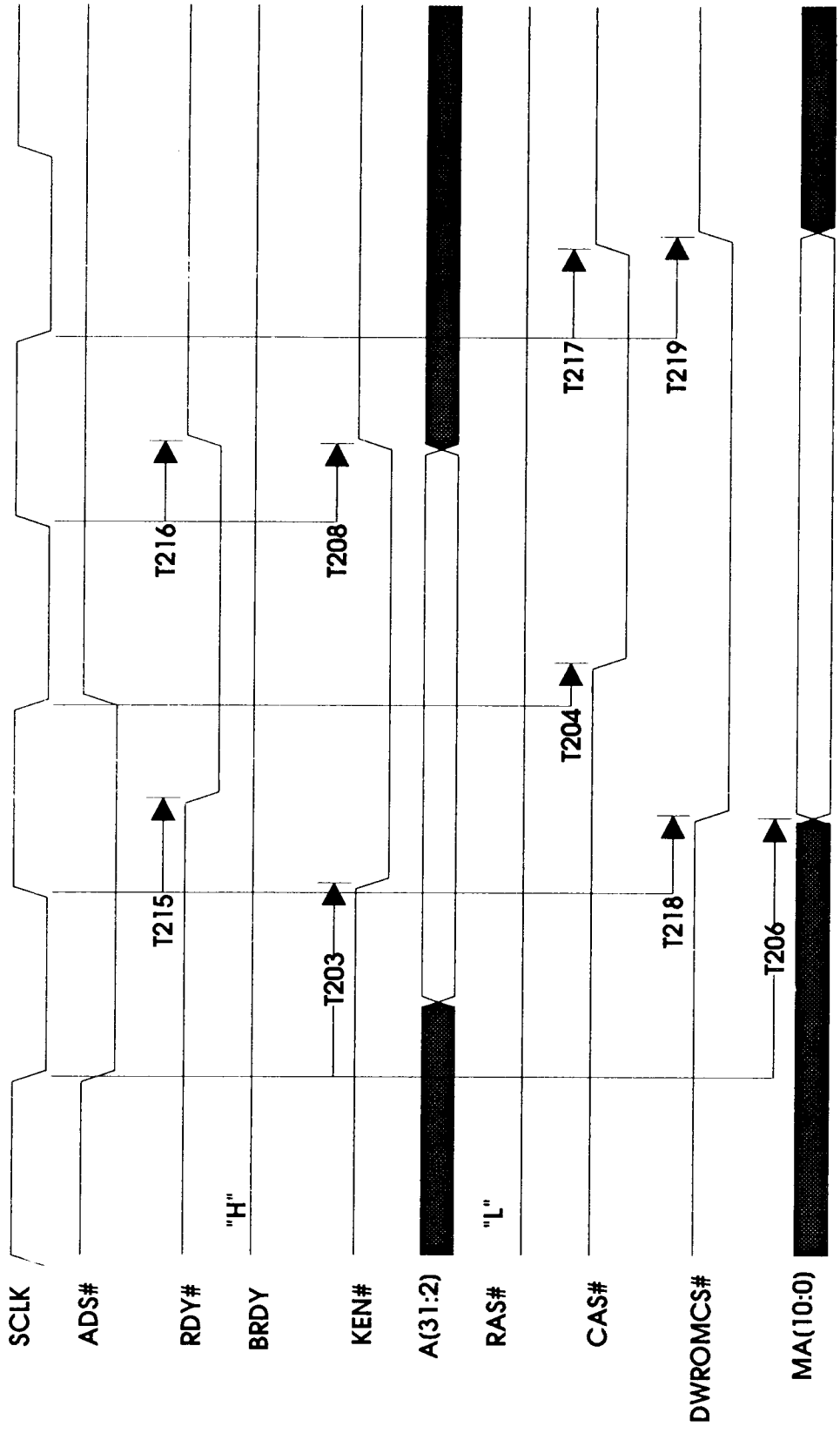
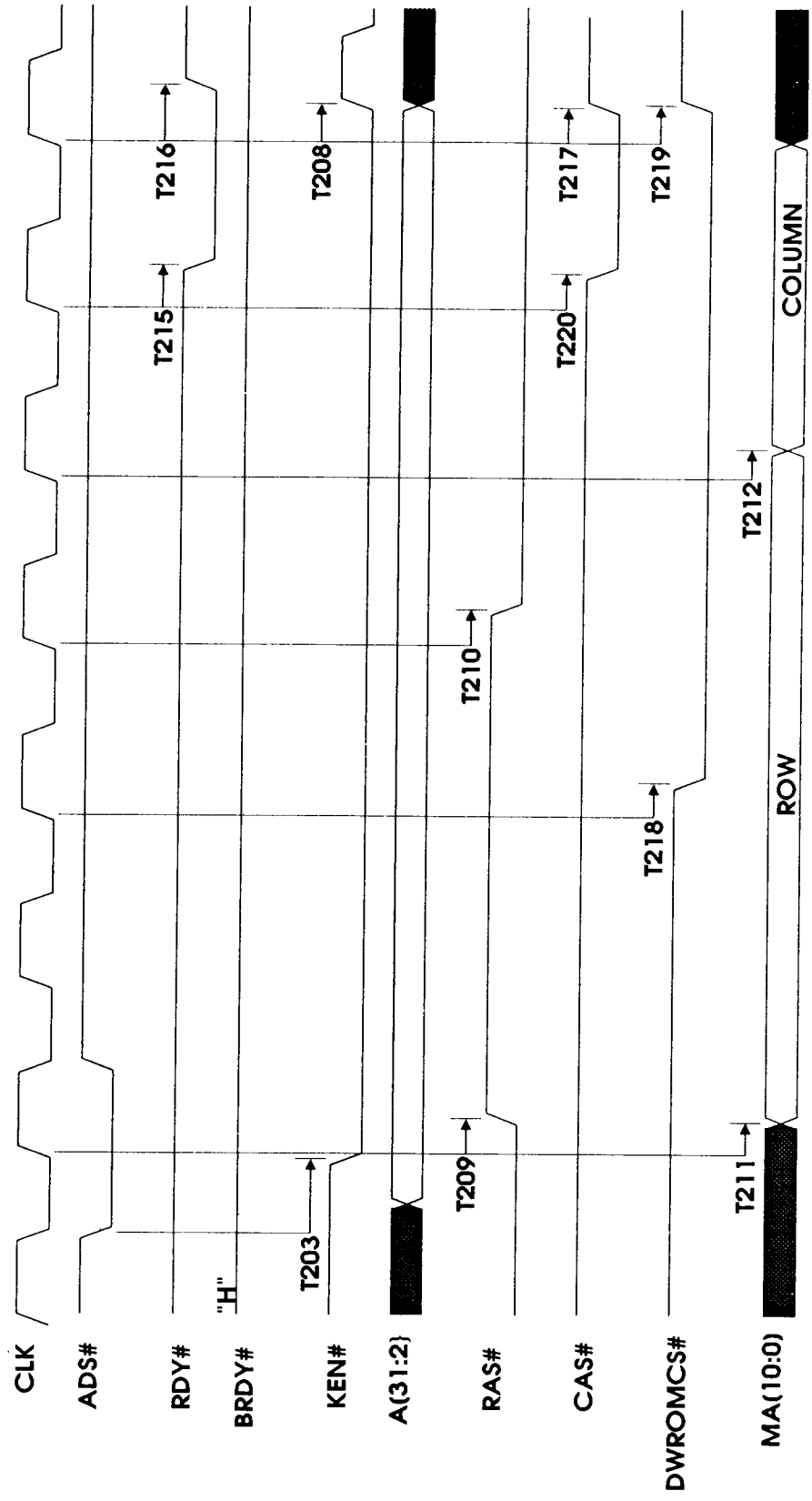


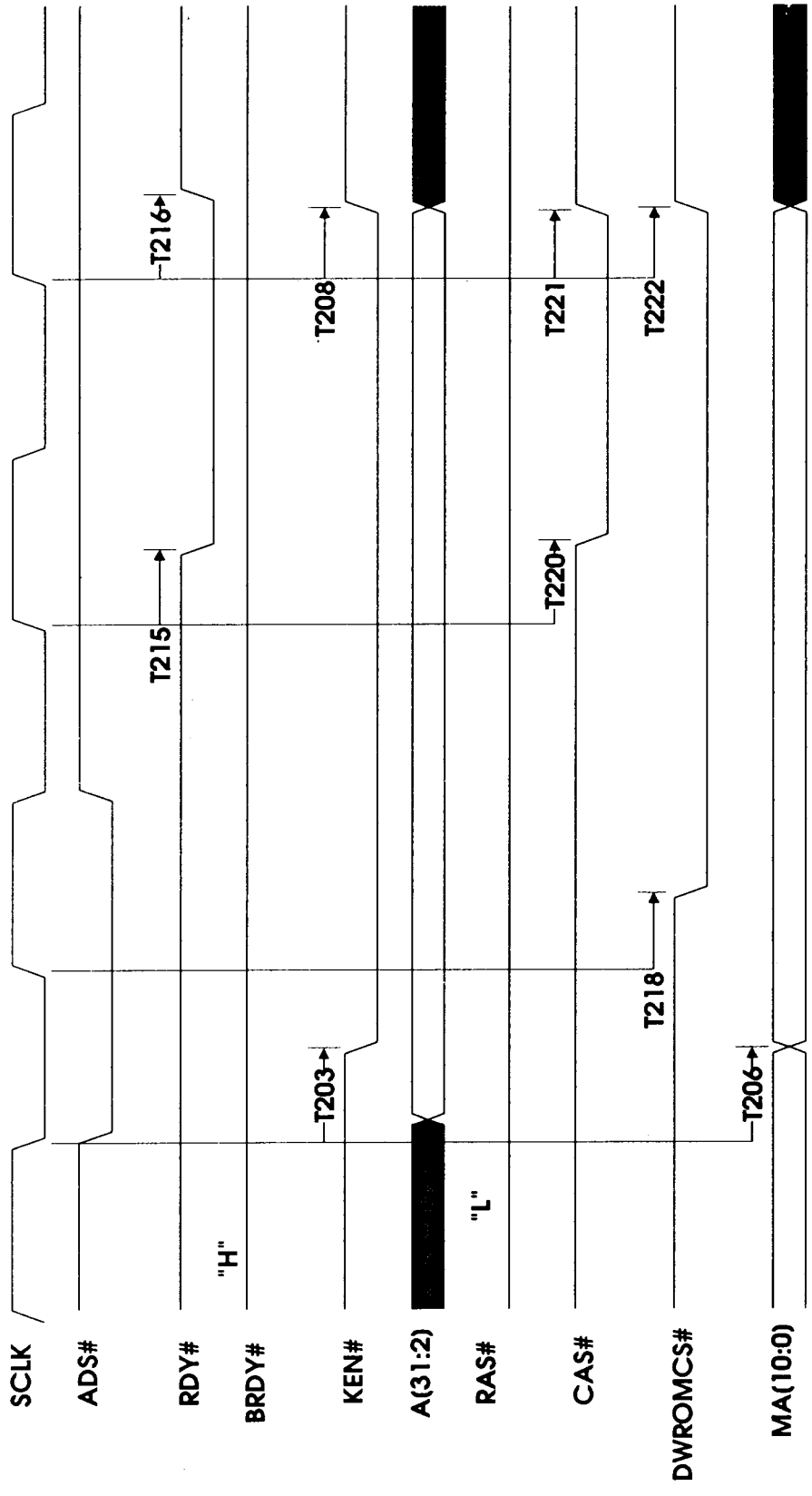
Fig. 4.3.11 ROM Cycle



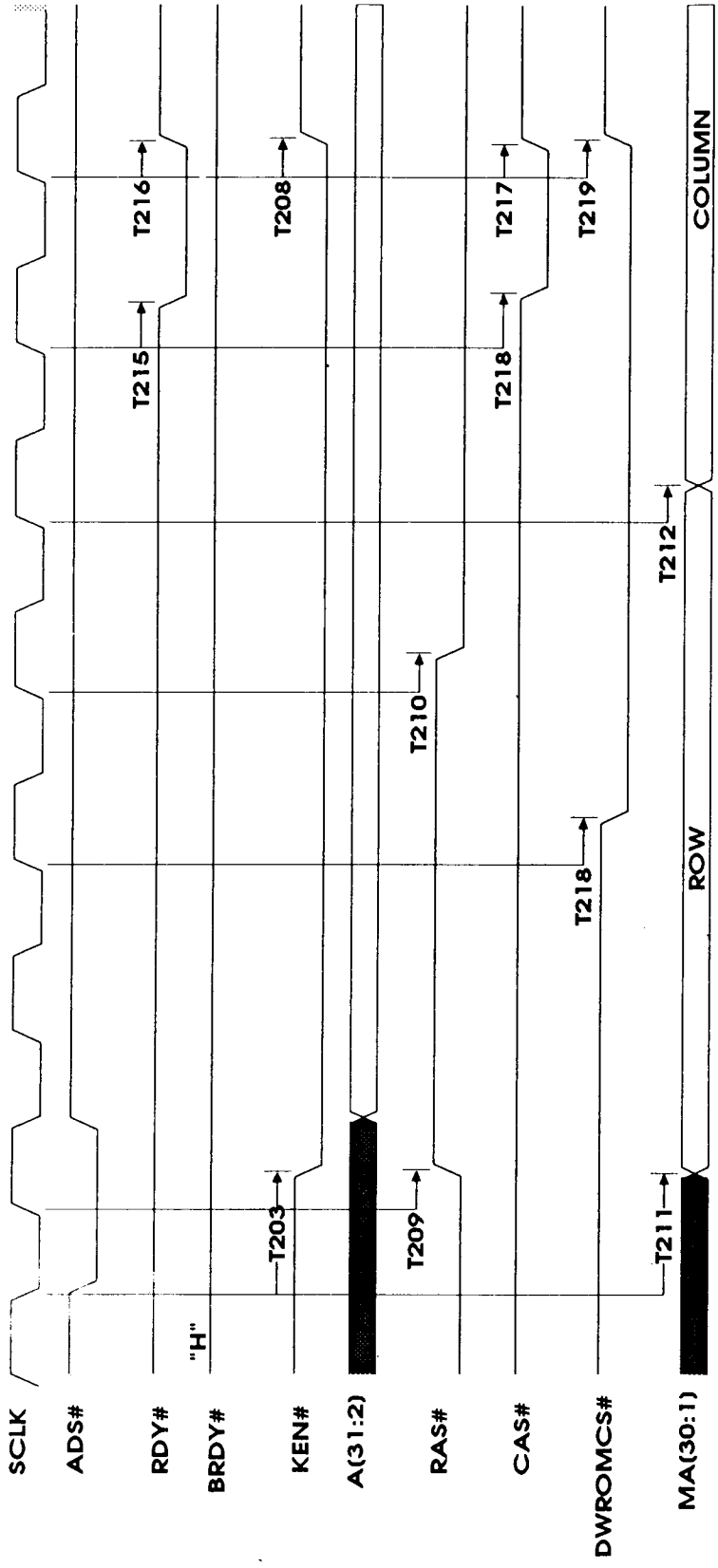
CPU Write DRAM, Write Wait State = 0
DRAM, Page Hit



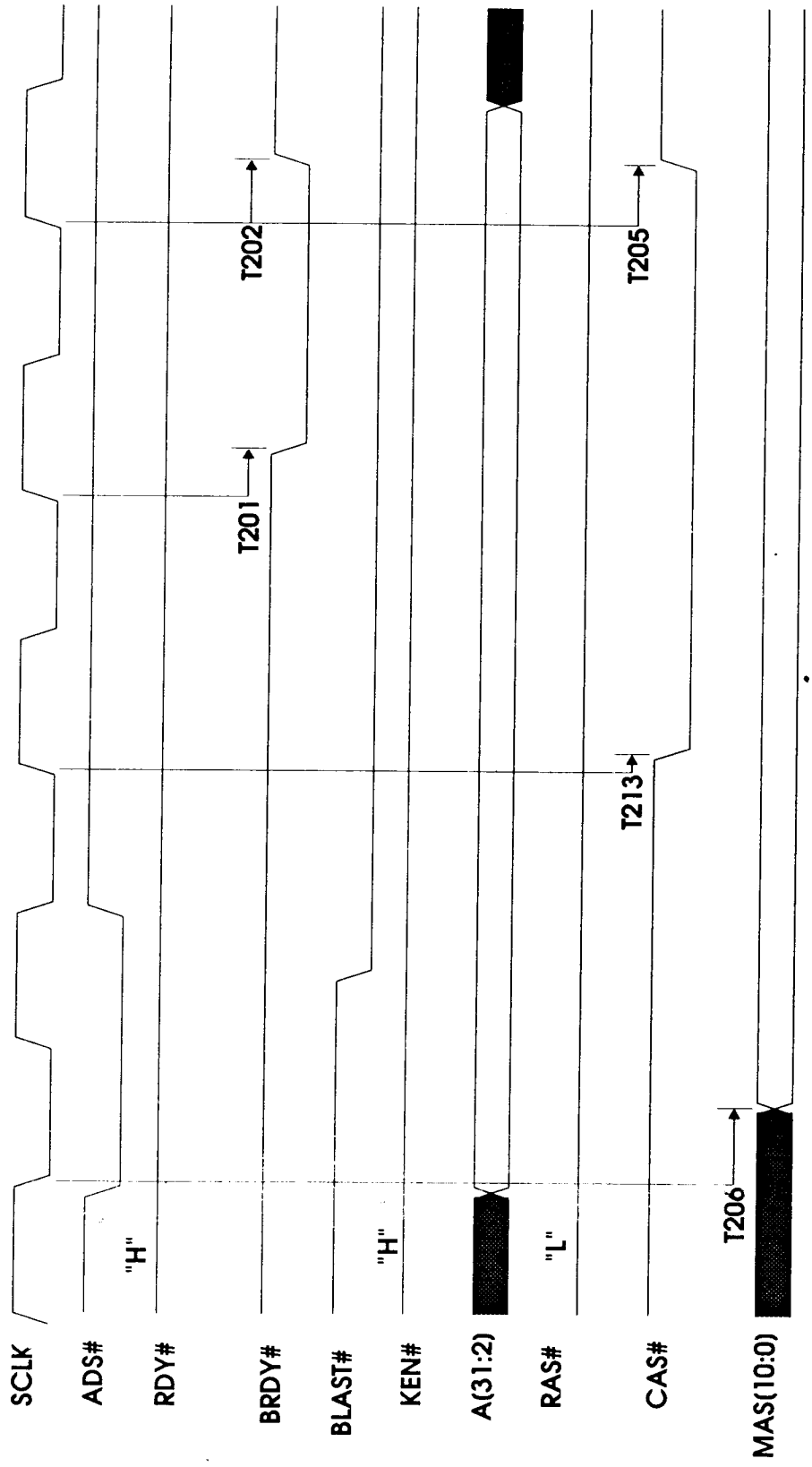
CPU Write DRAM, Write Wait State = 0
DRAM Page Miss



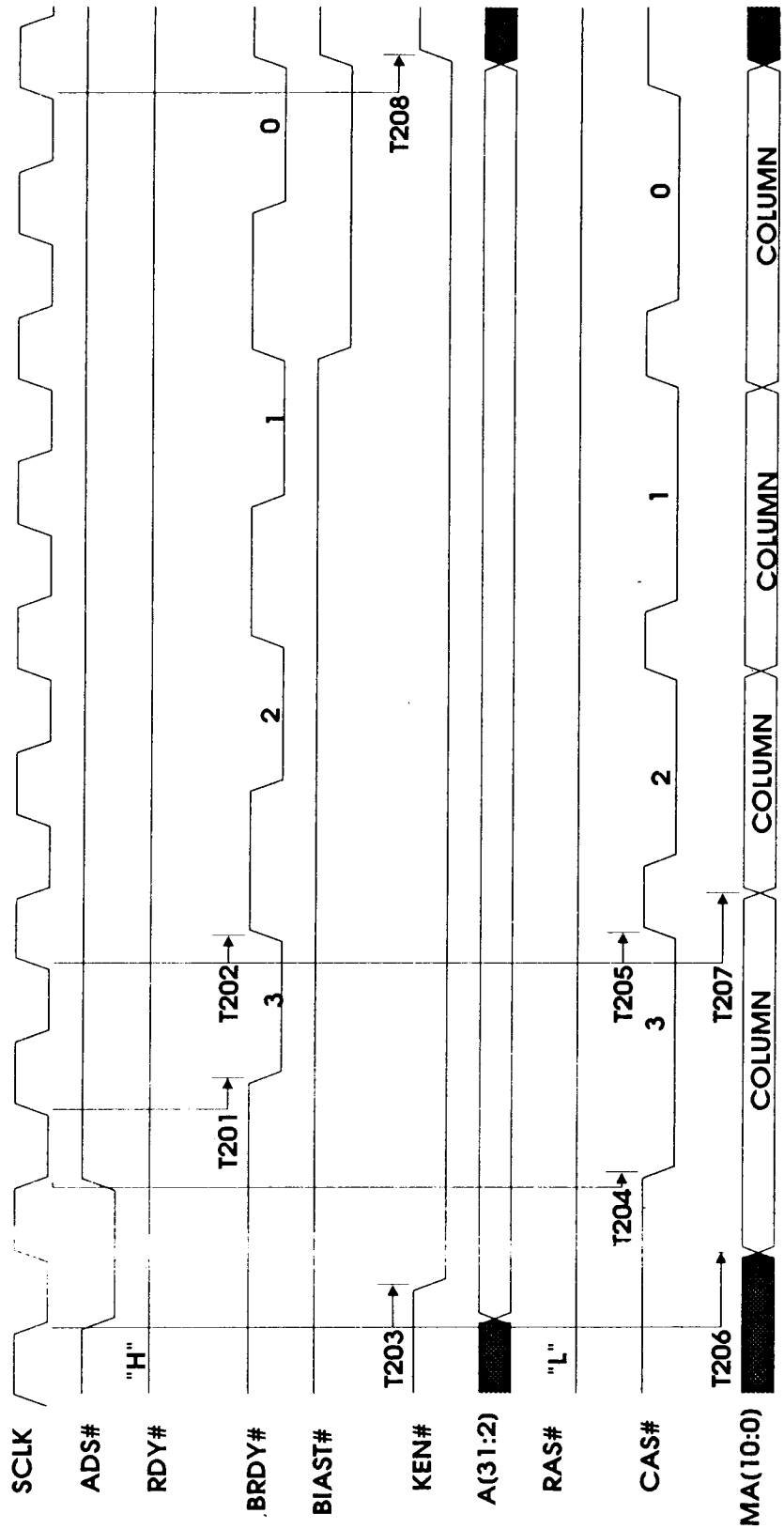
CPU Write DRAM, Write Wait State = 1
DRAM Page Hit



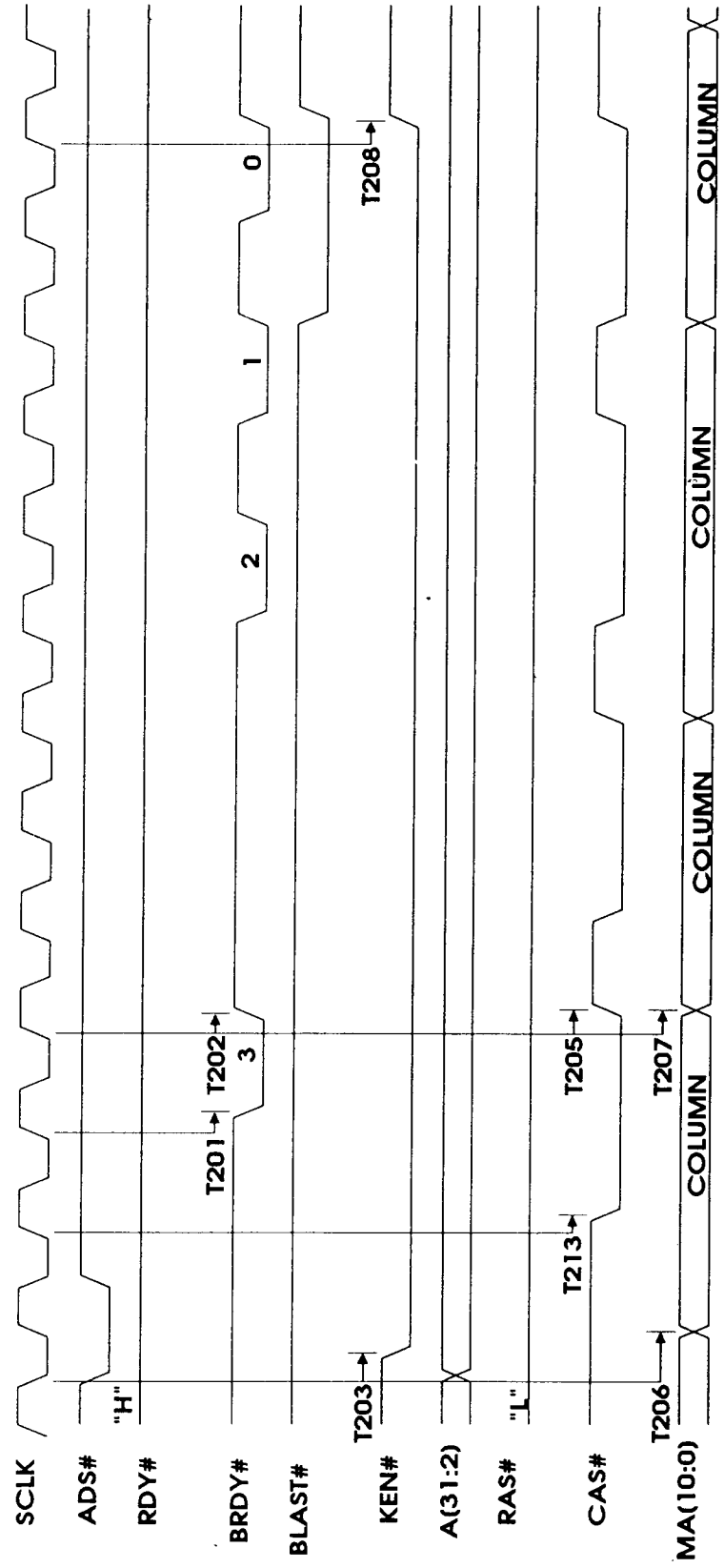
CPU Write DRAM, Write Wait State = 1
DRAM Page Miss



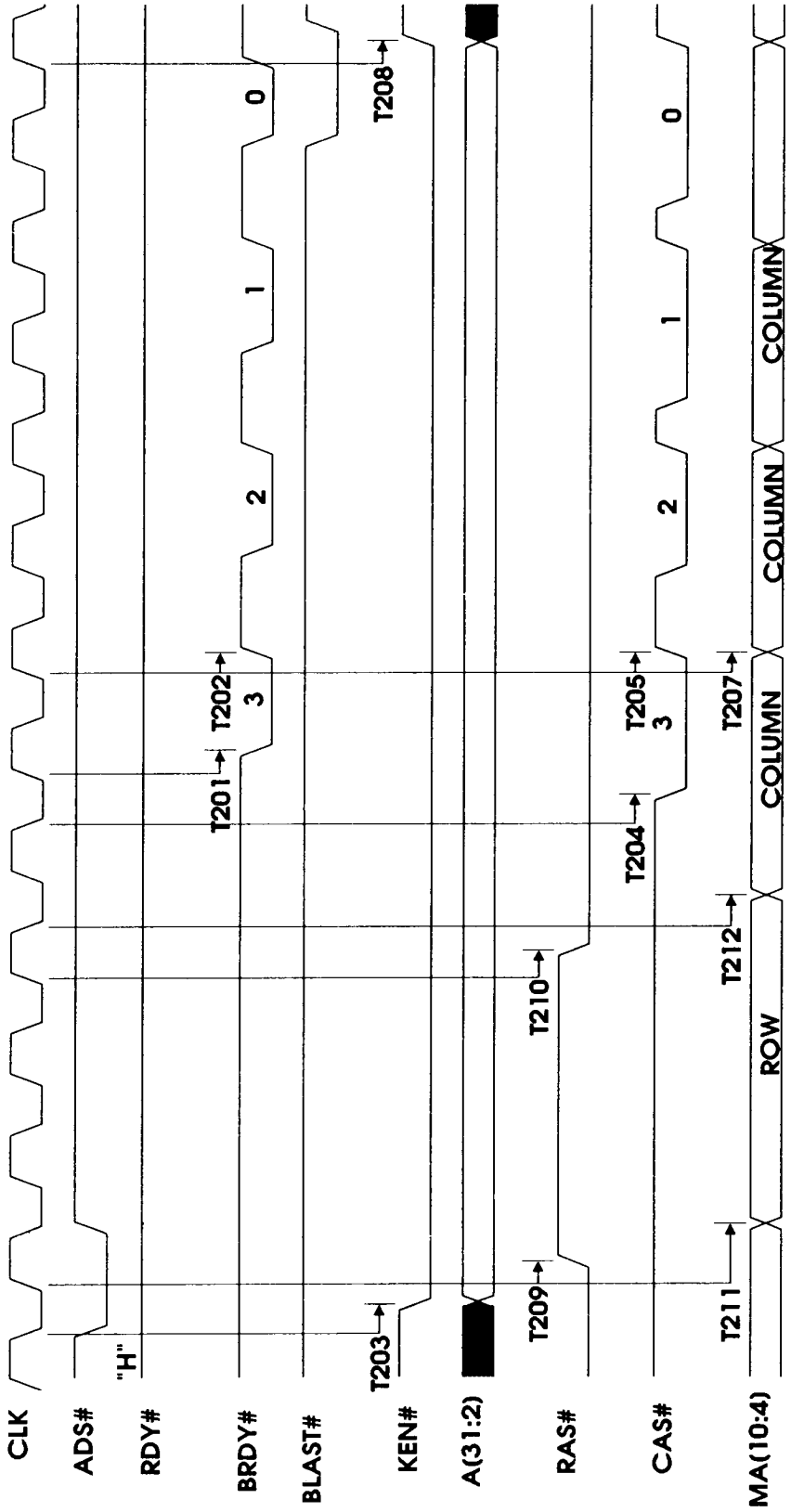
CPU Read DRAM, Noncacheable, Read Wait State = 1
DRAM, Page Hit



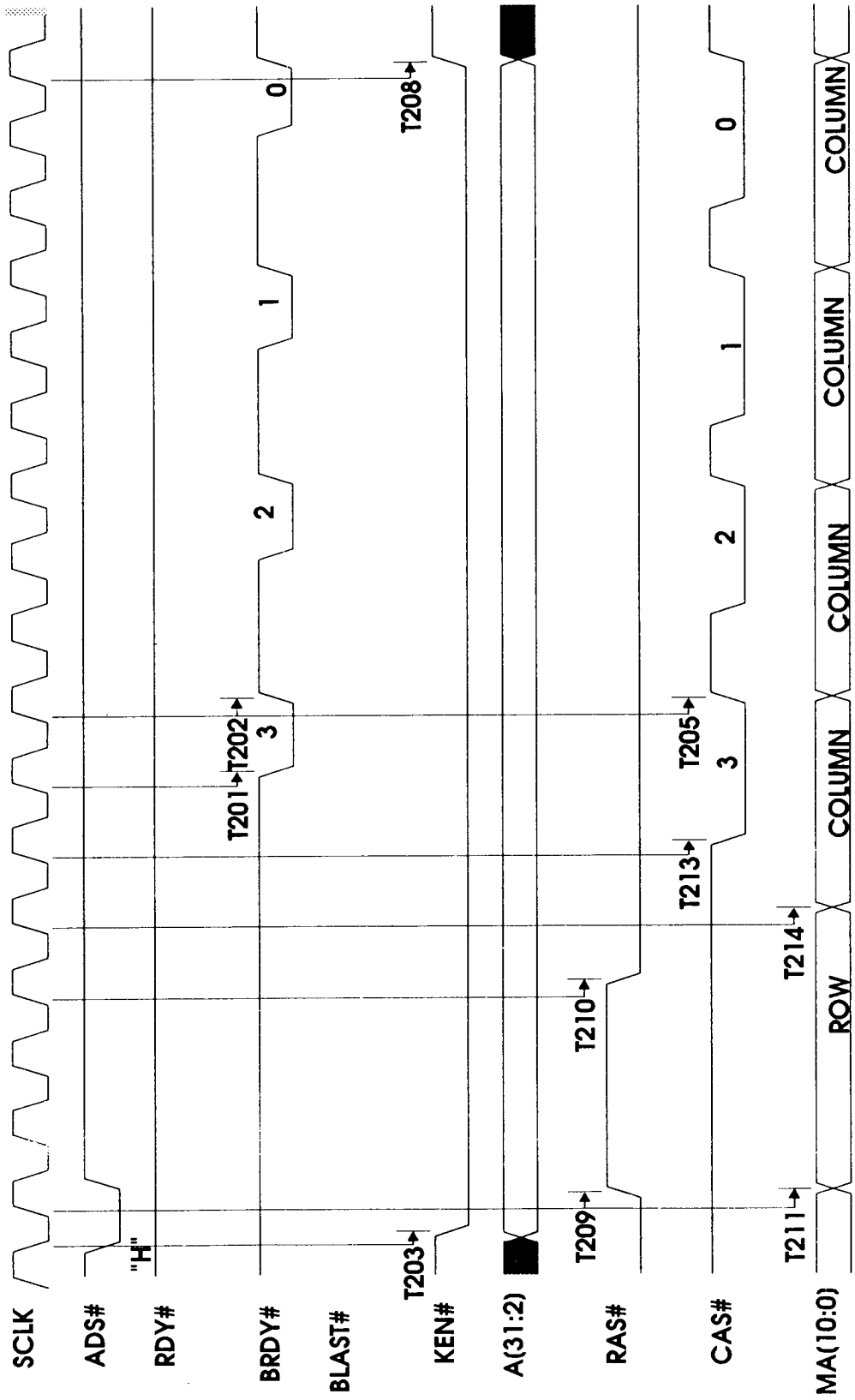
CPU Read DRAM, Read Wait State = 0, Burst 3-2-2-2
DRAM Page Hit



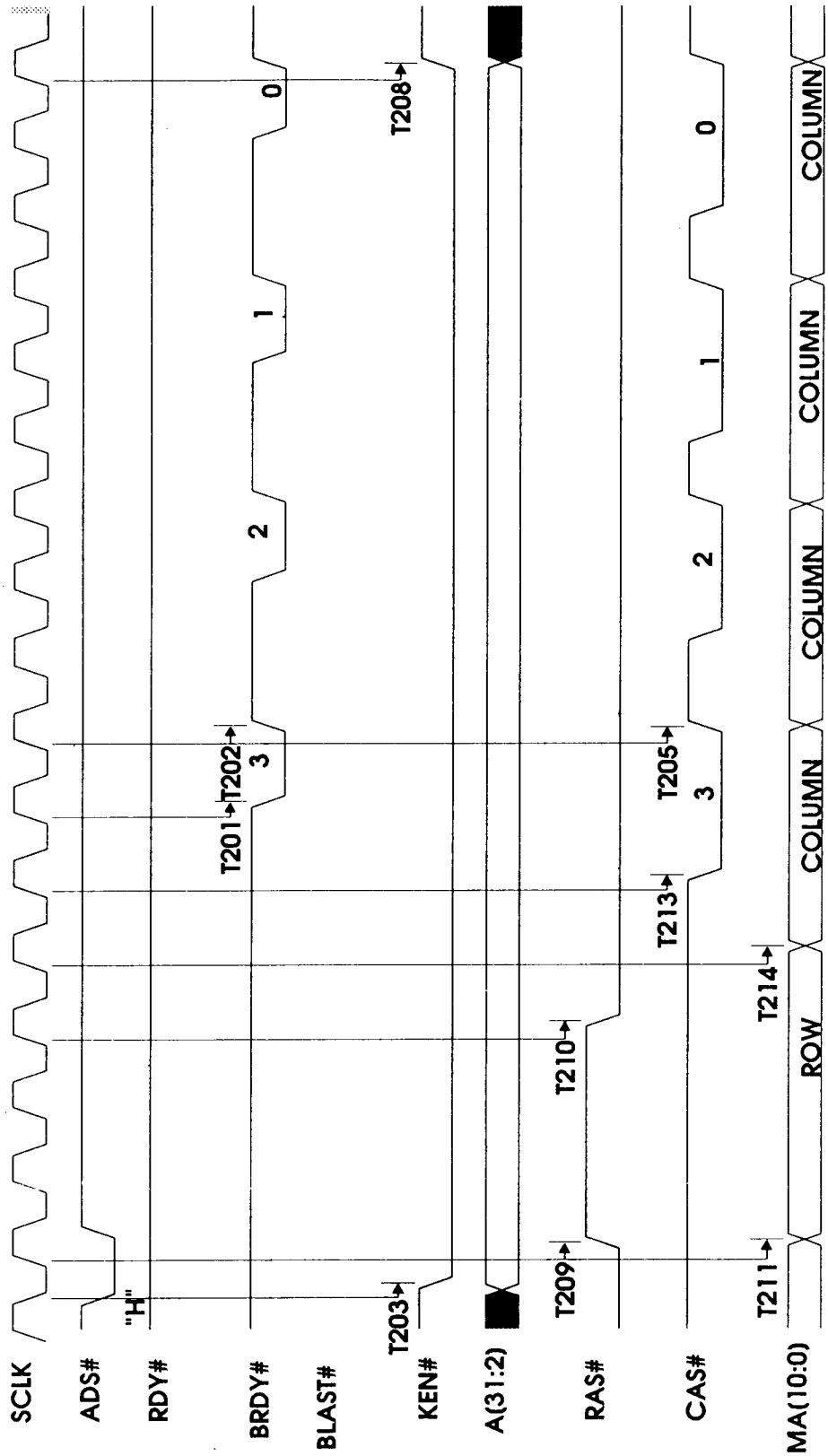
CPU Read DRAM, Read Wait State = 1, Burst 4-3-3-3
DRAM Page Hit



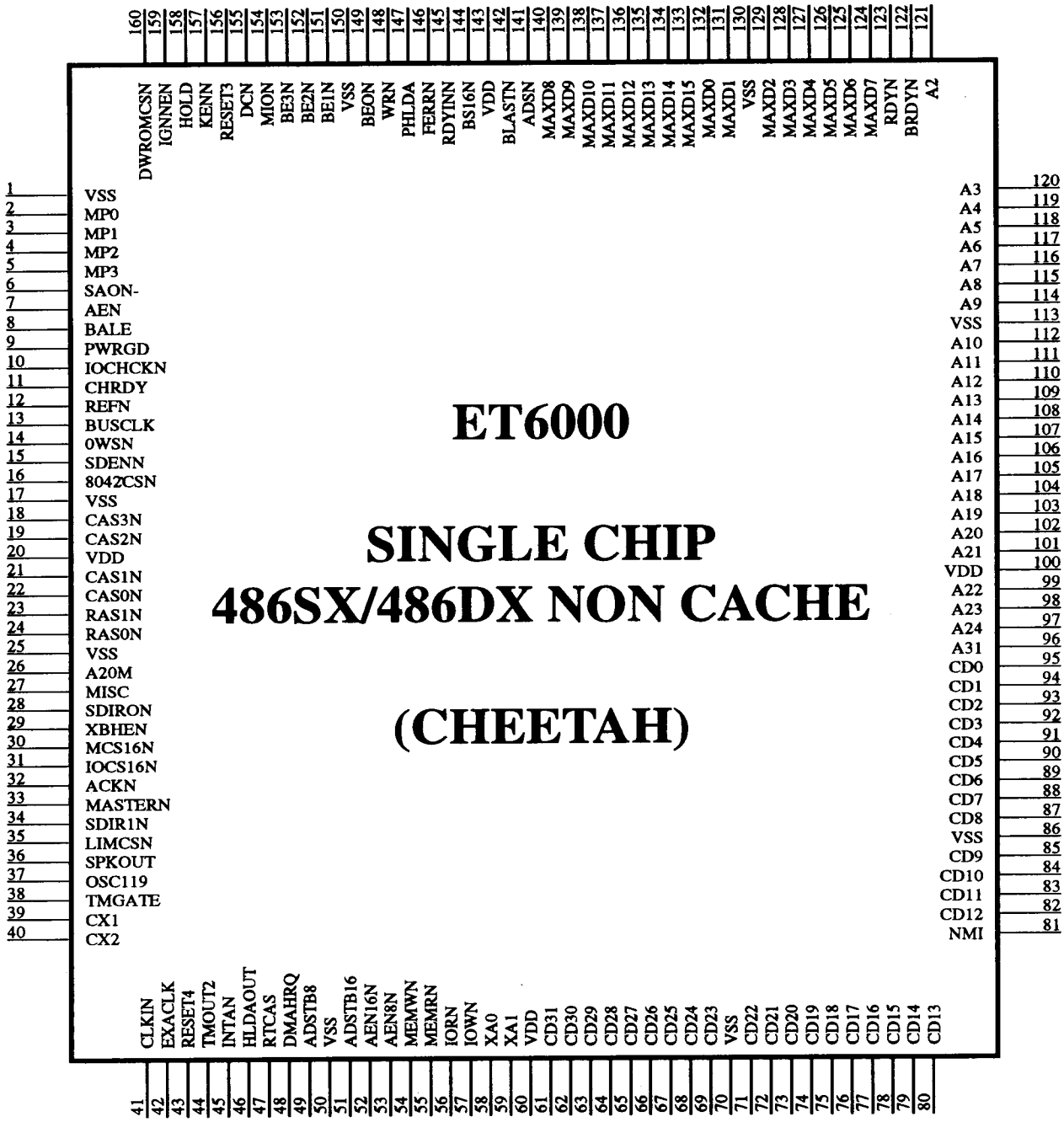
CPU Read DRAM, Read Wait State = 0, Burst 3-2-2-2
DRAM Page Miss



CPU Read DRAM, Read Wait State = 1, Burst 4-3-3-3
DRAM Page Miss

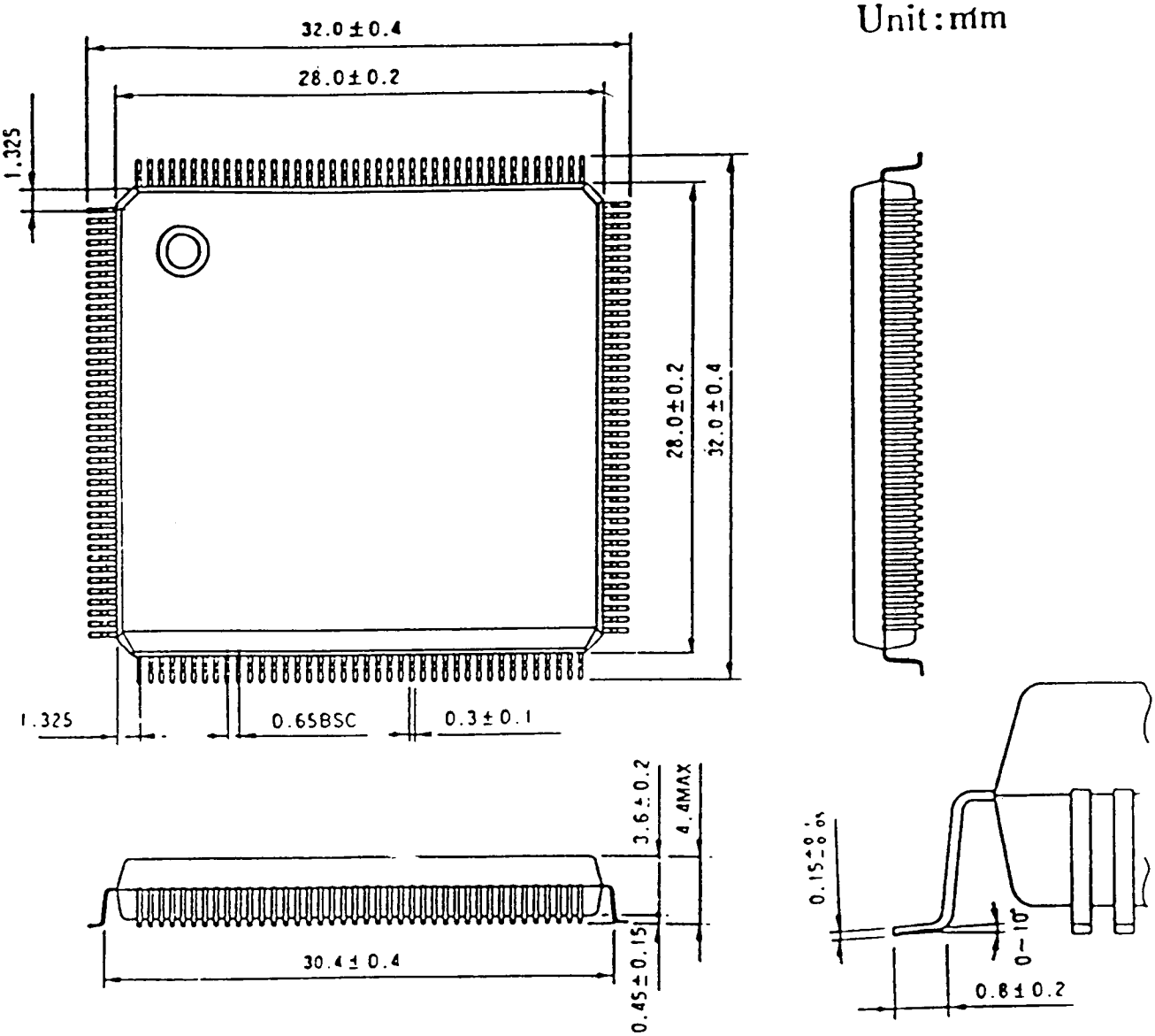


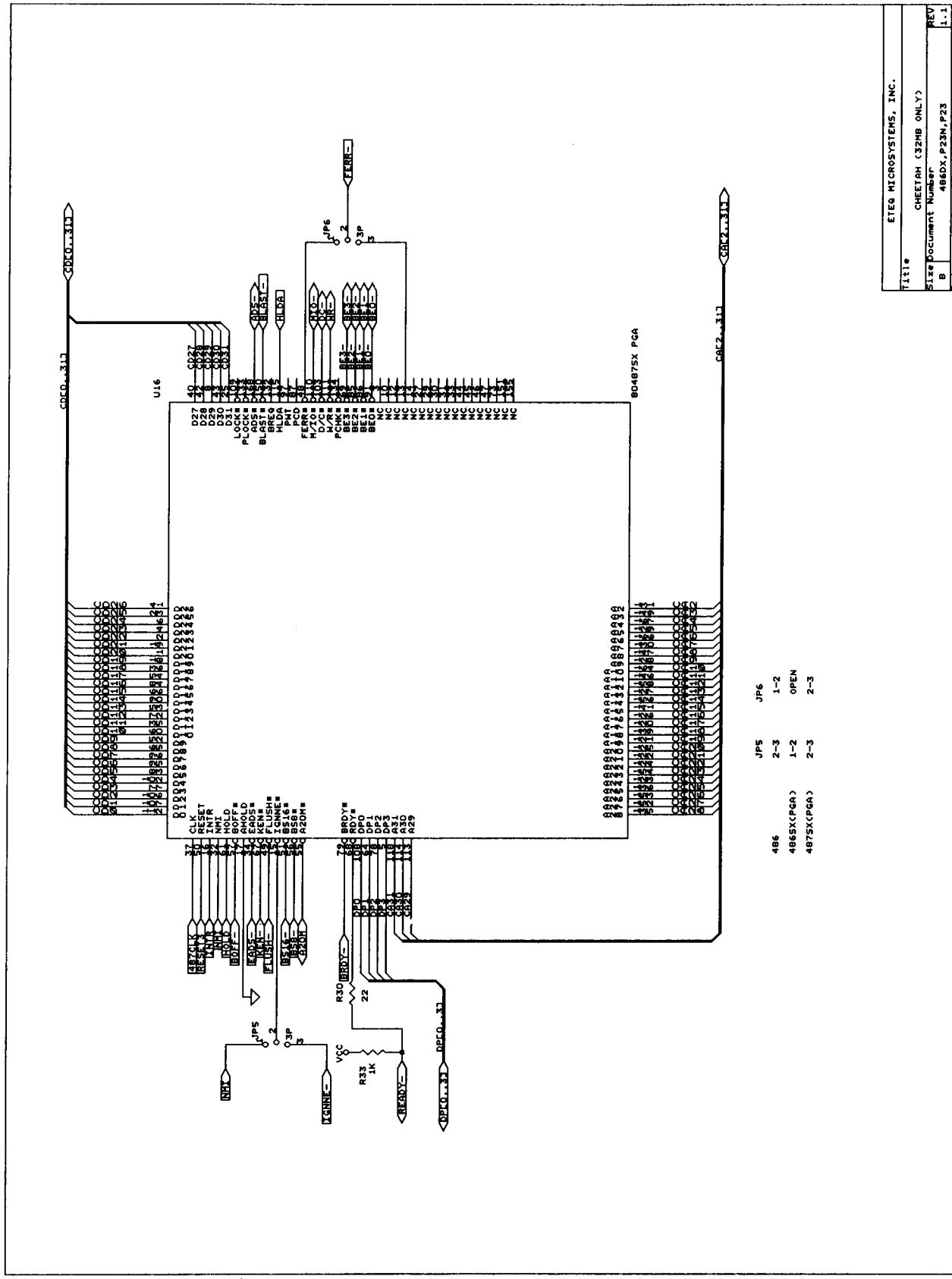
CPU Read DRAM, Noncacheable, Read Wait State = 0
DRAM, Page Hit

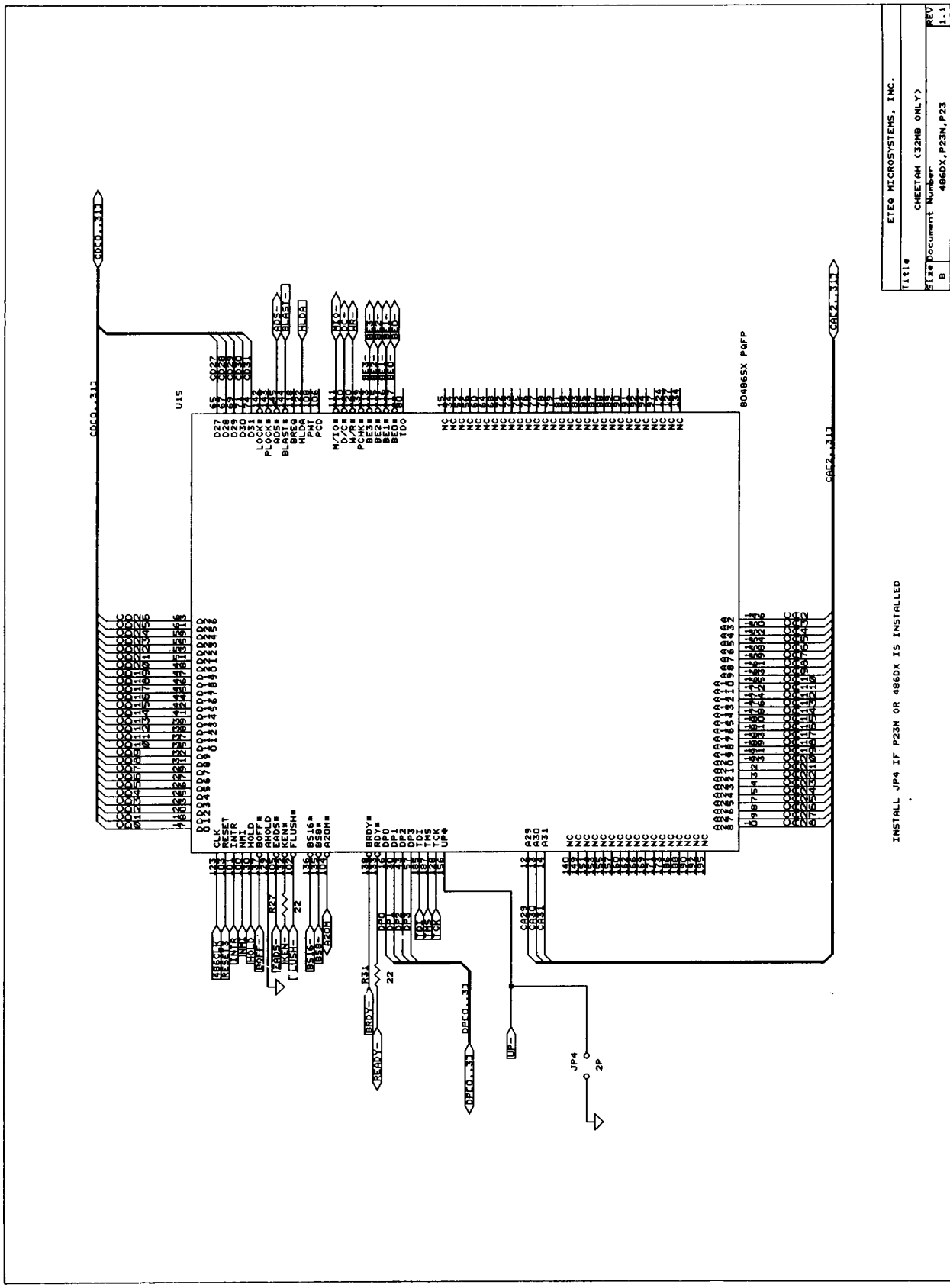


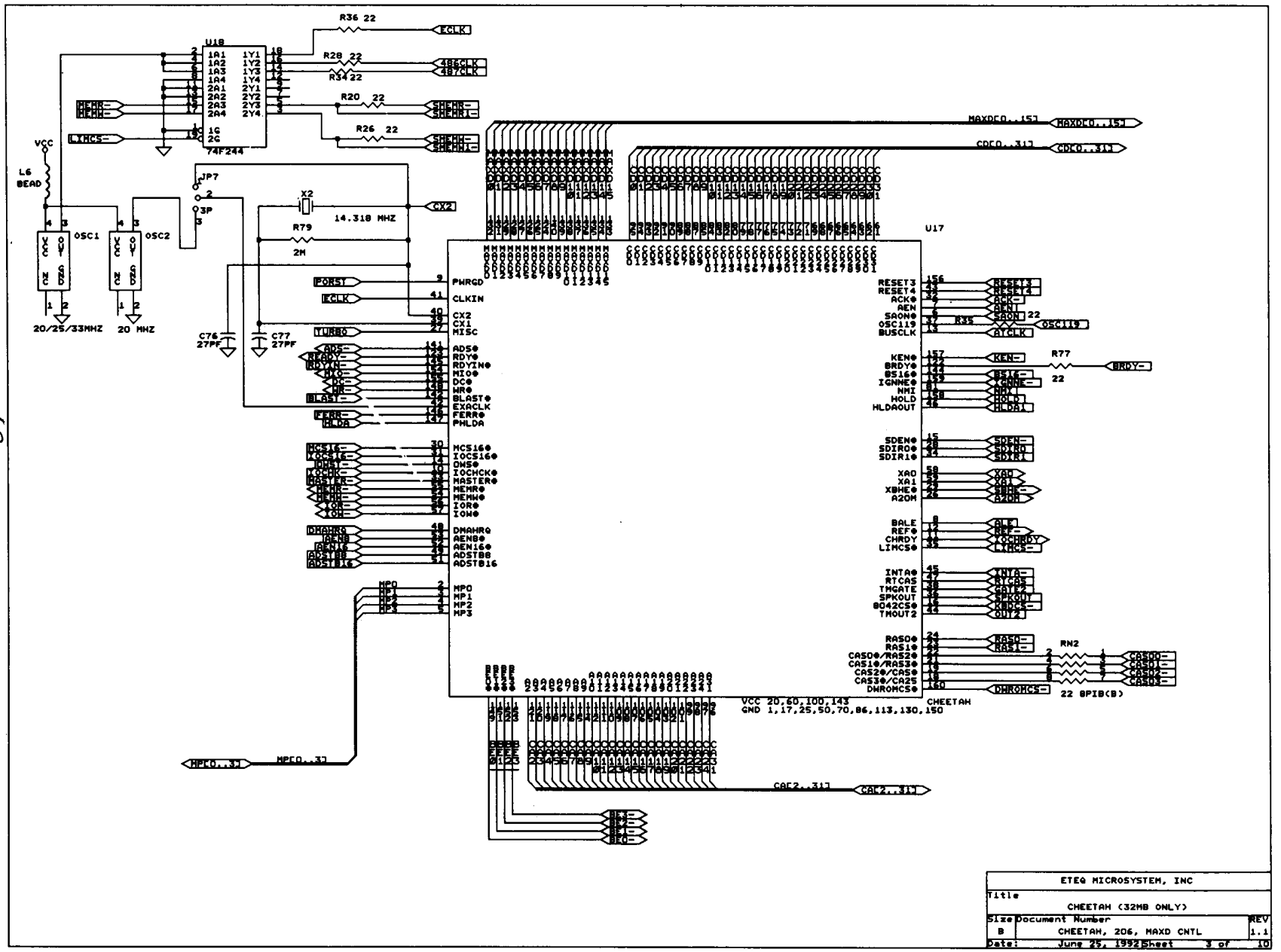
160-Pin Plastic Flat Package

Unit: mm









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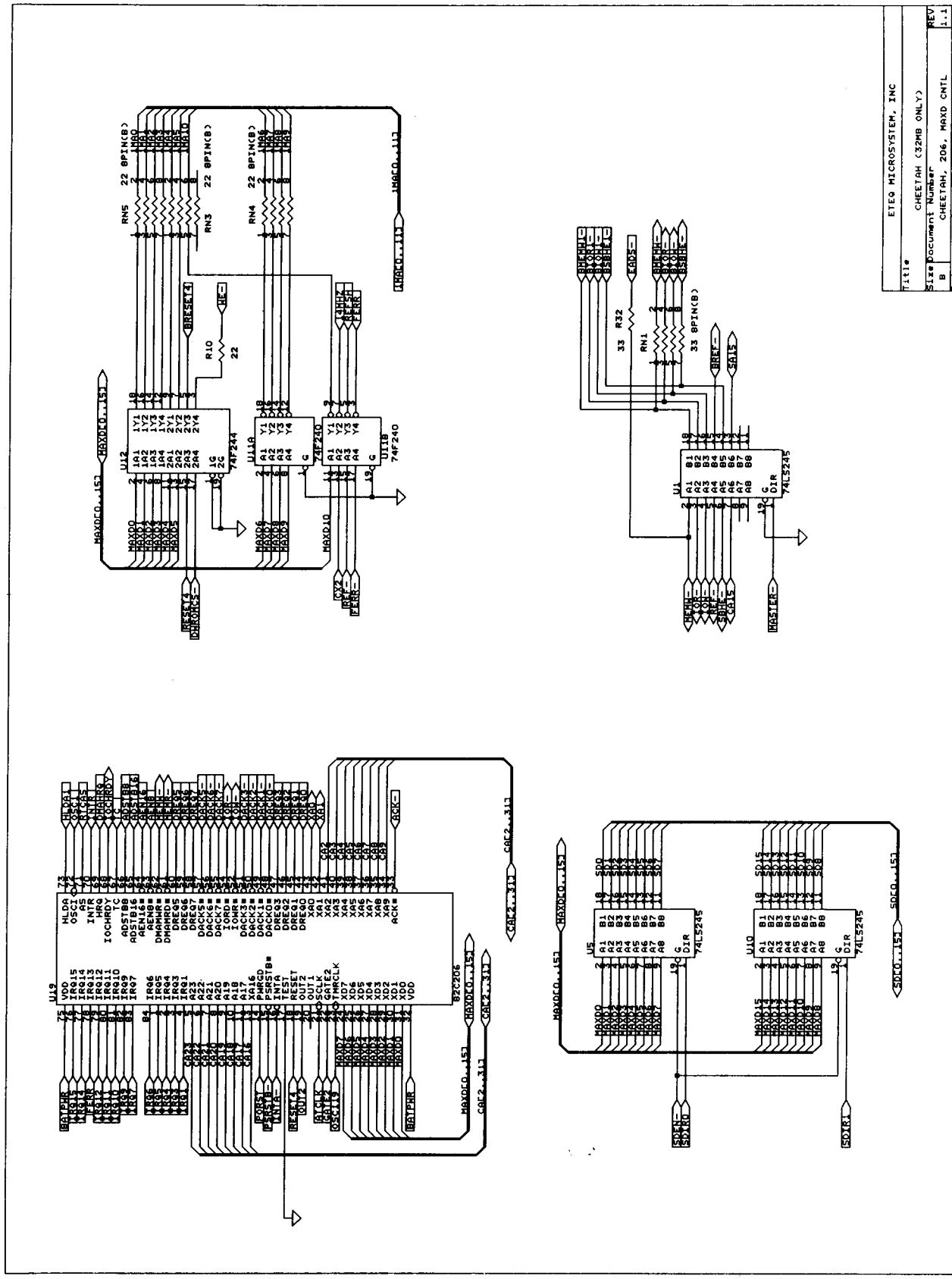

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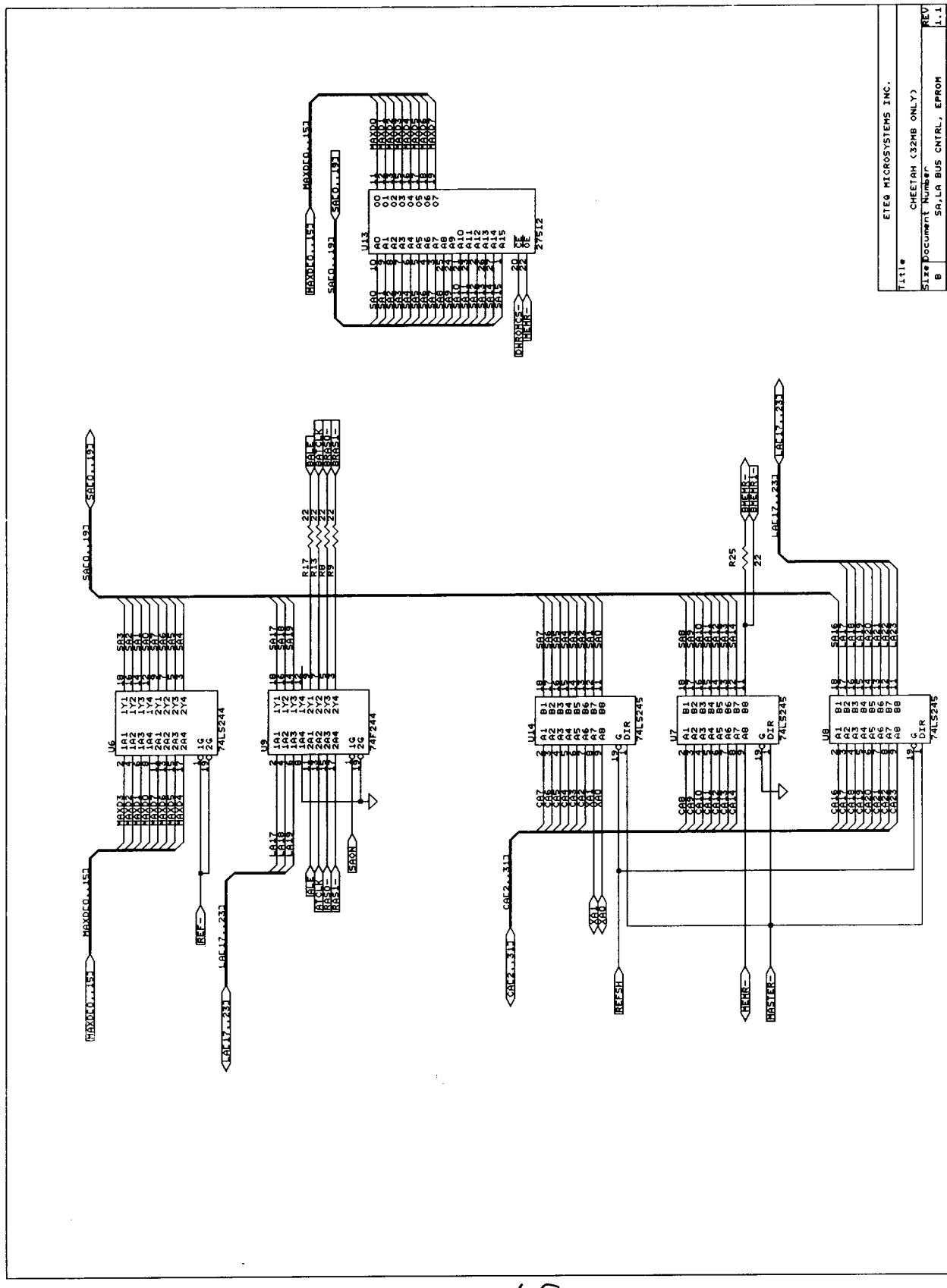

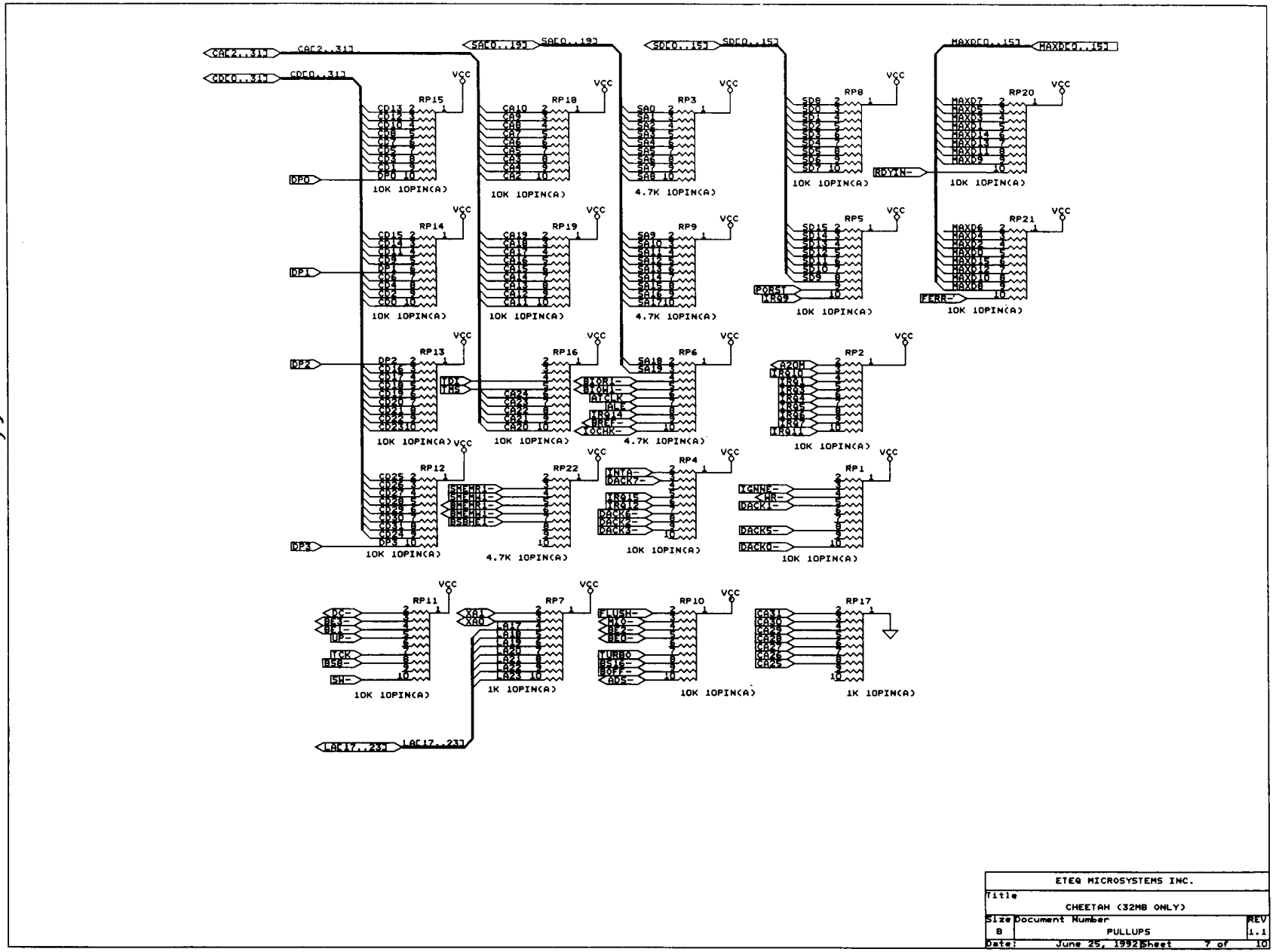

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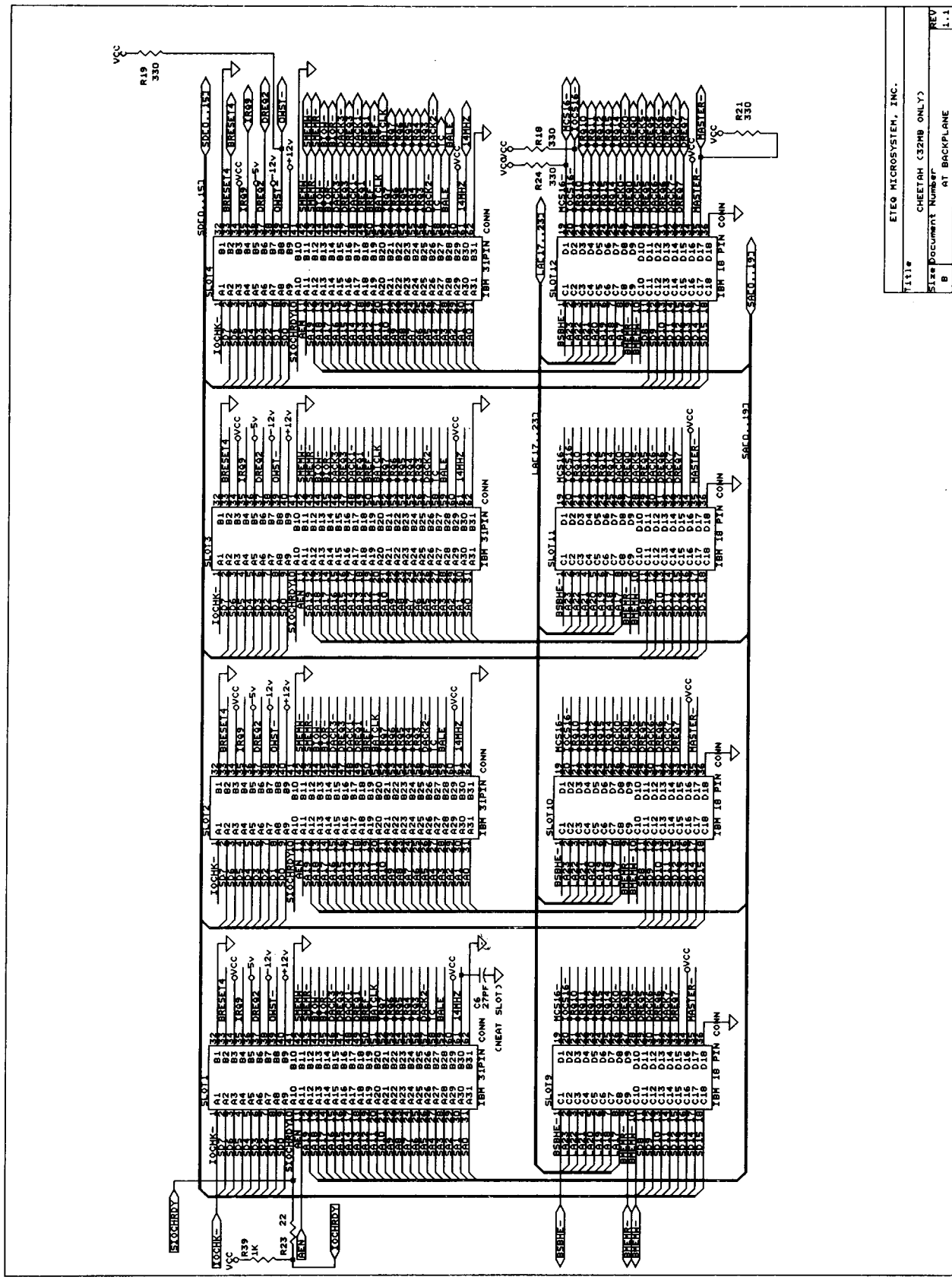

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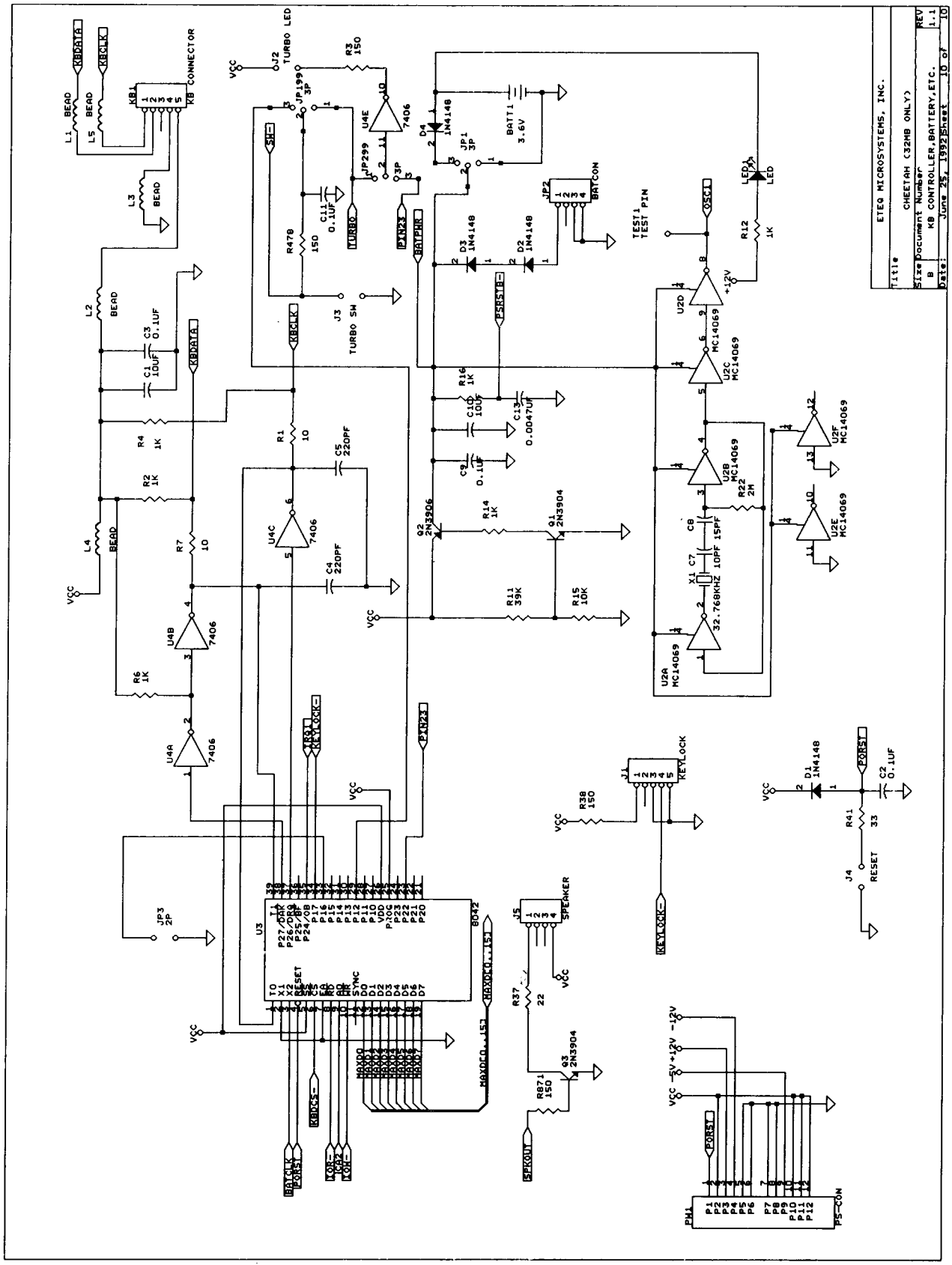

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