82C411

Flat Panel Color Palette/DAC

Data Sheet

May 1991

P R E L I M I N A R Y

CHIPS®

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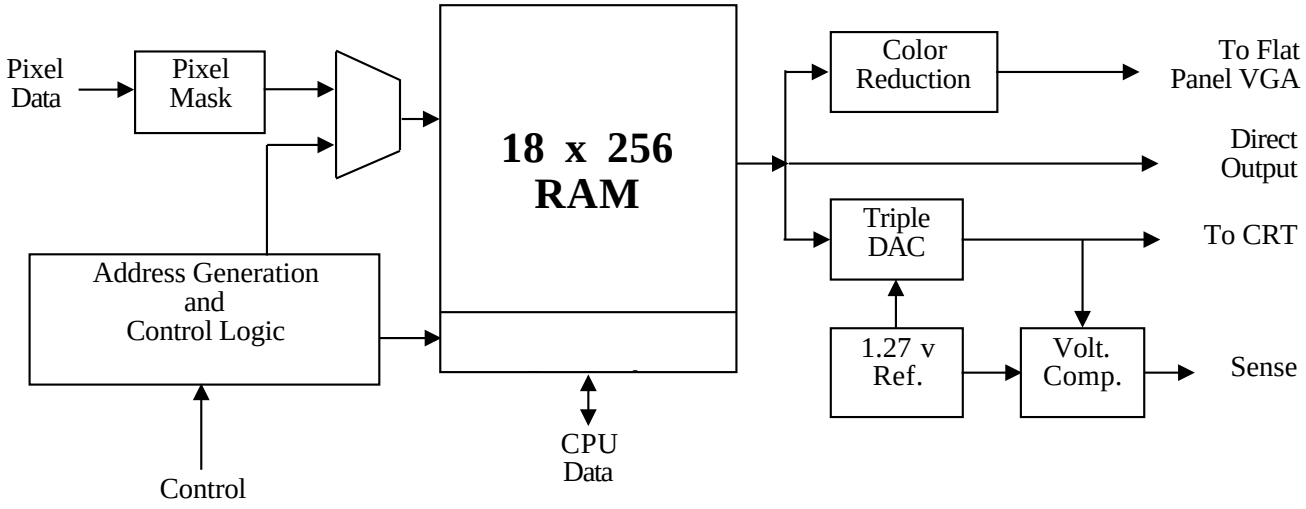
Publication No.: DS108
Stock No.: 010411-001
Revision No.: 0.8

82C411
Flat Panel Color Palette/DAC

- Full IBM VGA-compatibility
- Supports digital and analog CRT monitors and LCD, plasma, and electroluminescent flat panels
- Three RGB color to grayscale reduction techniques
- Direct connection to analog RGB color monitors
- Direct connection to Chips and Technologies Enhanced Flat Panel / CRT VGA Controllers
- Proven DOS and OS/2™ compatibility
- All CRT and Flat Panel palette functions are integrated into a single package
- 256 color support for color panels
- 64 gray levels for monochrome panels
- IBM VGA monochrome CRT compatibility on monochrome panels
- Power Down modes minimize power consumption
- No Sparkle during palette write operations



82C411 BLOCK DIAGRAM

Revision History

Revision	Date	By	Comment
0.0	3/151/90	MR	Created document.
0.1	3/90	MR	Minor update.
0.2	3/31/90	MR	Update functionality.
0.3	3/31/90	MR	Added electrical specs.
0.4	631/90	MR	Update pinout, package spec, electrical specs.
0.5	7/14/90	MR	Final update prior to Initial Release.
0.6	7/25/90	ST	Initial Release.
0.7	3/26/91	SV	Included pin list and updated timing diagrams.
0.8	4/26/91	SV	Update AC & DC specs and corrected various inaccuracies.

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Introduction

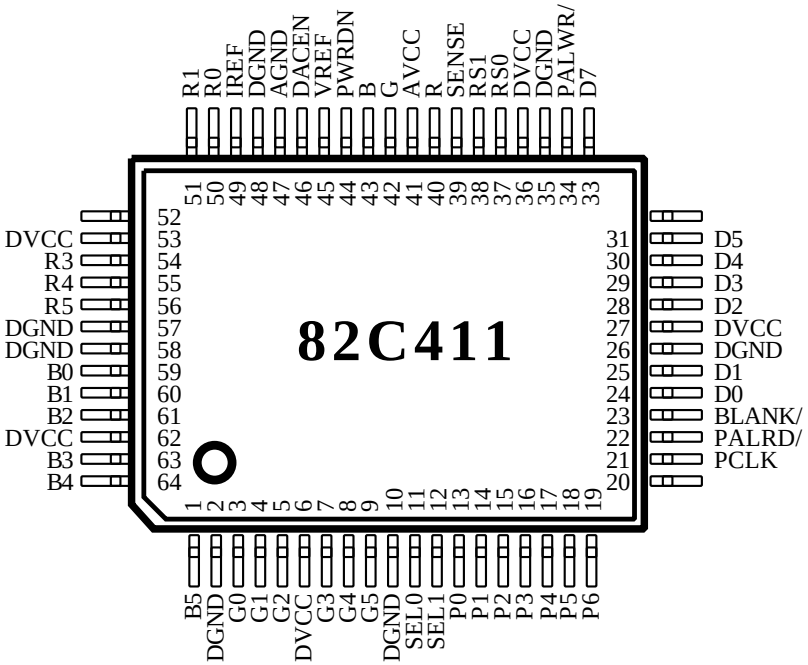
The 82C411 Flat Panel Palette supplies all of the functions of a VGA compatible RAMDAC, the 82C460 Flat Panel Color Palette, an LM339 voltage comparator and a current or voltage reference in a single CMOS package. In addition, features are provided to support power reduction as required in battery operated systems.

The 82C411 is designed to connect directly to Chips and Technologies Enhanced Flat Panel/CRT VGA Controllers and an analog CRT display. The 82C411 provides the analog output to drive a CRT as well as the color or grayscale data to the flat panel VGA controller. NTSC, equal weighting, and greengun-only are three reduction techniques supported on chip. In addition, the 82C411 can output all 18 bits of palette data directly. This may be used to drive digital CRTs or color panels. The flat panel controller uses the data to provide correct color or grayscale mapping on flat panel displays. The 82C411 and a flat panel VGA controller provide a two chip solution for a complete VGA Flat panel/CRT system.

The 82C411 provides two power saving features. Since the DAC outputs voltage reference and their support logic are required only when driving an analog CRT, they may be powered down when using the flat panel display. This portion of the chip is powered up only when the DACEN input is high.The second power down condition is the standby mode. When the PWRDN input is pulled high, all internal logic, references and outputs are turned off. Power is maintained only to the RAM core in order to retain the RAM data. No CPU accesses are allowed and the pixel clock may be stopped.

The 82C411 CPU and pixel interface are identical to that of an Inmos IMSG176 style RAMDAC. Since the DAC reference and LM339 voltage comparator are built into the 82C411, the system component count and complexity is greatly reduced.

As well as providing color or grayscale data for the flat panel controller, the 82C411 is designed to directly drive an analog CRT display. A single resistor is used to set the current level in the DACs. The 82C411 will directly drive a single or doubly terminated 75 ohm system. Only the termination resistor is required. No output series resistor is needed.


82C411
1 B5
2 DGND
3 G0
4 G1
5 G2
6 DVCC
7 G3
8 G4
9 G5
10 DGND
11 SEL0
12 SEL1
13 P0
14 P1
15 P2
16 P3
17 P4
18 P5
19 P6
20 PCLK
21 BLANK/
22 PALRD/
23 D0
24 D1
25 DGND
26 DVCC
27 D2
28 D3
29 D4
30 D5
31
33 D7
34 PALWR/
35 DGND
36 DVCC
37 RS0
38 RS1
39 SENSE
40 R
41 AVCC
42 G
43 B
44 PWRDN
45 VREF
46 DACEN
47 AGND
48 DGND
49 IREF
50 R0
51 R1
52
53 DVCC
54 R3
55 R4
56 R5
57 DGND
58 DGND
59 B0
60 B1
61 B2
62 DVCC
63 B3
64 B4

82C411 Pin List

Pin Name	Pin #
AGND	47
AVCC	41
B	43
B0	59
B1	60
B2	61
B3	63
B4	64
B5	1
BLANK/	23
D0	24
D1	25
D2	28
D3	29
D4	30
D5	31
D6	32
D7	33
DACEN	46
DGND	48
DGND	35
DGND	26

Pin Name	Pin #
DGND	10
DGND	2
DGND	58
DGND	57
DVCC	36
DVCC	27
DVCC	6
DVCC	62
DVCC	53
G	42
G0	3
G1	4
G2	5
G3	7
G4	8
G5	9
IREF	49
P0	13
P1	14
P2	15
P3	16

Pin Name	Pin #
P4	17
P5	18
P6	19
P7	20
PALRD/	22
PALWR/	34
PCLK	21
PWRDN	44
R	40
R0	50
R1	51
R2	52
R3	54
R4	55
R5	56
RS0	37
RS1	38
SEL0	11
SEL1	12
SENSE	39
VREF	45

82C411 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
21	PCLK	In	Both	PIXEL CLOCK. The rising edge controls the sampling of the values on the Pixel Address and Blank/ inputs. It controls progress of these values through the Color Palette pipeline to the outputs.
20	P7	In	Both	PIXEL ADDRESS. The byte wide value on these inputs is sampled and then masked by the Pixel Mask register and then used as the address into the Color Palette RAM.
19	P6	In	Both	
18	P5	In	Both	
17	P4	In	Both	
16	P3	In	Both	
15	P2	In	Both	
14	P1	In	Both	
13	P0	In	Both	
9	G5	Out	Both	GREEN DIGITAL OUTPUT. These pins provide the green data from the Color Palette RAM as addressed by the Pixel Address or the reduced data from the reduction logic. The output on these pins is selected by SEL[1:0].
8	G4	Out	Both	
7	G3	Out	Both	
5	G2	Out	Both	
4	G1	Out	Both	
3	G0	Out	Both	
1	B5	Out	Both	BLUE DIGITAL OUTPUT. These pins provide the blue data from the Color Palette RAM as addressed by the Pixel Address. The state of these outputs is controlled by SEL[1:0].
64	B4	Out	Both	
63	B3	Out	Both	
61	B2	Out	Both	
60	B1	Out	Both	
59	B0	Out	Both	
56	R5	Out	Both	RED DIGITAL OUTPUT. These pins provide the red data from the Color Palette RAM as addressed by the Pixel Address. The state of these outputs is controlled by SEL[1:0].
55	R4	Out	Both	
54	R3	Out	Both	
52	R2	Out	Both	
51	R1	Out	Both	
50	R0	Out	Both	
40	R	Out	Analog	RED, GREEN, BLUE ANALOG OUTPUTS. These signals are the outputs of the 6-bit DACs. Each of these outputs is capable of driving a doubly terminated 75 ohm coaxial cable.
42	G	Out	Analog	
43	B	Out	Analog	
23	BLANK/	In	Low	BLANKING CONTROL. A low on this input forces the analog outputs to the inactive state. (RGB=0 volts)

82C411 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
38 37	RS1 RS0	In In	Both Both	REGISTER SELECT 1 & 0. These two lines are sampled during the falling edges of the enable signals (PALWR/ or PALRD/) and select one of the three internal registers or the palette RAM. RS1 RS0 Register 0 0 Address Register (RAM Write Mode) 1 1 Address Register (RAM Read Mode) 0 1 Palette RAM 1 0 Pixel Mask Register
33 32 31 30 29 28 25 24	D7 D6 D5 D4 D3 D2 D1 D0	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	PALETTE DATA. These pins provide the read/write data to the internal registers. During the write cycle, the rising edge of PALWR/ latches the data into the selected register. During the read cycle, the register data is output on these pins when PALRD/ is active (low). When PALRD/ is inactive (high) the data lines are 3-stated.
34 22	PALWR/ PALRD/	In In	Low Low	PALETTE WRITE ENABLE and PALETTE READ ENABLE. These signals control the timing of read and write operations on the CPU interface. RS1:0 are latched on the falling edge of either of these signals during a CPU read or write. D7:0 are sampled on the rising edge of PALWR/ during an CPU write operation. PALWR/ and PALRD/ should not be asserted at the same time.
12 11	SEL1 SEL0	In In	Both Both	SELECT 1 & 0. These signals select the data output on the digital outputs (R[5:0], G[5:0] B[5:0]), the reduction algorithm and the input to output delay. The functions are: SEL1 SEL0 R[5:0] B[5:0] G[5:0] Delay (clocks) 0 0 Off Off NTSC Reduction 6 0 1 Off Off Equal Reduction 6 1 0 Off Off Green Data 6 1 1 Red Data Blue Data Green Data 4
39	SENSE	Out	Both	COMPARATOR SENSE OUTPUT. A low indicates that one or more of the RGB outputs is above the sense reference level (335 mV).

82C411 PIN DESCRIPTIONS

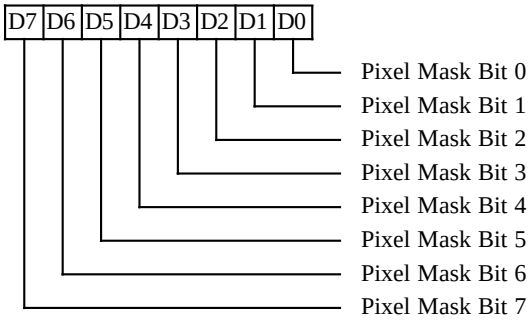
Pin #	Pin Name	Type	Active	Description
44	PWRDN	In	High	POWER DOWN. A high on this signal places the entire device in a low power mode. No input or output takes place and the input clock may be stopped. All internal registers are preserved.
45	VREF	In	Analog	VOLTAGE REFERENCE INPUT. This pin may be used to override the internal 1.27 v reference.
46	DACEN	In	High	DAC ENABLE. A high on this signal enables the voltage reference and the current outputs used in the DACs. When this input is low, the analog outputs and support logic are off.
49	IREF	Out	Analog	CURRENT REFERENCE SET. This pin is used to set the current level in the analog outputs. It is usually connected through a 220 ohm 1% resistor to ground.
6 27 36 53 62	DVCC	PWR		DIGITAL POWER SUPPLY. The digital and analog supplies are brought out separately to provide the highest noise immunity. A high frequency decoupling capacitor should be used between digital power and ground.
2 10 26 35 48 57 58	DGND	PWR		DIGITAL GROUND.
41	AVCC	PWR		ANALOG POWER SUPPLY. The analog power supply should be separated from the digital supply with a high frequency noise suppressing inductor. A high frequency decoupling capacitor should be used between analog power and ground.
47	AGND	PWR		ANALOG GROUND.

82C411 Color Palette Control Registers

Register Mnemonic	Register Name	RS 1:0	VGA Access	VGA I/O Address	Page
DACMASK	Pixel Mask Register	10	RW	3C6h	13
DACRX	Palette Read-Mode Index	11	W	3C7h	13
DACX	Palette Write-Mode Index	00	RW	3C8h	14
DACDATA	Palette Data Port	01	RW	3C9h	14

PIXEL MASK REGISTER (DACMASK)

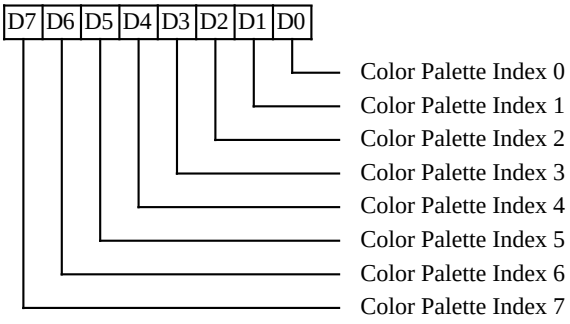
Read/Write at RS 1:0 = 10
Read/Write at VGA I/O Address 3C6h



The contents of this register are logically ANDed with the 8 bits of video data. Zero bits in this register cause the corresponding input to the color palette RAM address to be zero. For example, if this register is programmed with 7, only addresses 0-7 would be accessible; video data input bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette RAM.

READ-MODE INDEX REGISTER (DACRX)

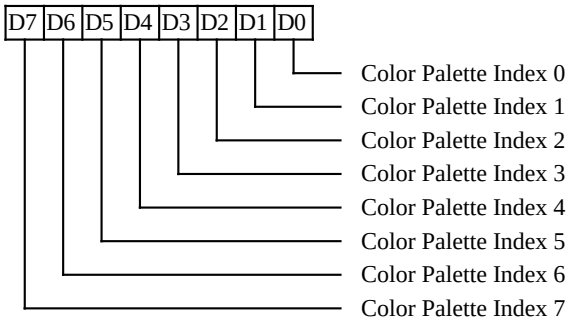
Read/Write RS 1:0 = 11
Write only at VGA I/O Address 3C7h



This register is used to set the address of the next read access. When this register is written, the RGB color values are read from the palette RAM and saved in an internal storage register. The palette address pointer is then incremented.

WRITE MODE INDEX REGISTER (DACX)

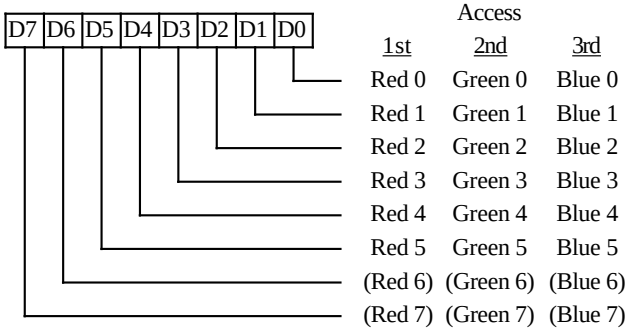
Read/Write at RS 1:0 = 00
Read/Write at VGA I/O Address 3C8h



This register is used to set the address of the next read access. When this register is written, the RGB sequencer is cleared and the address pointer is loaded with the value written to this register.

PALETTE DATA PORT (DACDATA 00-FF)

Read/Write at RS 1: 0 = 01
Read/Write at VGA I/O Address 3C9h



The index register is used to point to one of 256 data registers. Each data register is 18 bits in length (6 each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the appropriate index register, data values may be read from or written to the palette data port in sequence: first red, then green, then blue, then repeated for the next location if desired (the address pointer is incremented automatically).

PROGRAMMING THE COLOR PALETTE

The index may be read or written at either RS [1:0] = 10 or 01. When the index value is written to either port, it is written to both the index register and a 'save' register internal to the color palette chip. The save register (not the index register) is used internally by the palette chip to point at the current data register. When the index value is written to the read mode index, it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to the write mode index, the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) the data port is completed, the save and index registers are both automatically incremented. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment internal RGB sequence counter.

REDUCTION TECHNIQUES

Three reduction algorithms are provided to reduce the 18 bit RGB data to 6 bits. Reduced data is output on G[5:0] when SEL1=0. The output data is delayed six clocks from the input pixel address to reduced data output when reduction is selected. The reduction algorithms are as follows:

NTSC: This is the industry standard technique for reducing RGB color information to gray levels. The weighting is 5/16R +9/16G +1/8B. The data is reduced with 9 bits of precision and the 6 most significant bits are output. This technique is selected when SEL0=0.

EQUAL: In this technique the RGB values are equally weighted. The reduction is 5/16R +3/8G +5/16B. This technique is selected when SEL0 = 1.

GREEN ONLY: When SEL1=1, the green output pins, G[5:0] contain the green palette data. On monochrome flat panels, this provides a display identical to the IBM monochrome monitor. When SEL[1:0] = 10, the data is delayed six clocks from the pixel input to the data output.

When SEL[1:0] = 11, the data is delayed four clocks from the input pixel address and all 18 digital outputs are enabled.

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82C411 Electrical Specifications

82C411 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
P_D	Power Dissipation	–	1	W
V_{CC}	Supply Voltage	–0.5	7	V
V_I	Input Voltage	–0.5	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	V_{CC}+0.5	V
T_A	Operating Temperature (Ambient)	0	70	° C
T_{STG}	Storage Temperature	-55	150	° C
I_{OD}	Digital Output Current	-20	20	mA
I_{OA}	Analog Output Current	–	45	mA

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C411 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.5	5.5	V
T_A	Ambient Temperature	0	70	° C
T_C	Case Temperature	0	85	° C

82C411 DC CHARACTERISTICS (Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0	–	V_{CC}+0.5	V
V_{IL}	Input Low Voltage		–0.5	–	0.8	V
V_{REF}	Reference Voltage		–	1.27	–	V
I_{IN}	Digital Input Current		–10	+10	+10	uA
I_{OZ}	Digital Output Current (High Impedance)		–20	–	+20	uA
V_{OH}	Output High Voltage	I_{OH} = 4 mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA	–	–	0.4	V
I_{CC0}	Standby Supply Current	PWRDN=1	–	–	2	mA
I_{CC1}	Power Supply Current	DACEN=1	–	–	175	mA
I_{CC2}	Power Supply Current	DACEN=0	–	42	130	mA
C	Capacitance, Input or Output		–	10	20	pF

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

82C411 THERMAL CHARACTERISTICS (Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Min	Typ	Max	Units
JA	Thermal Resistance	–	63	–	° C/W

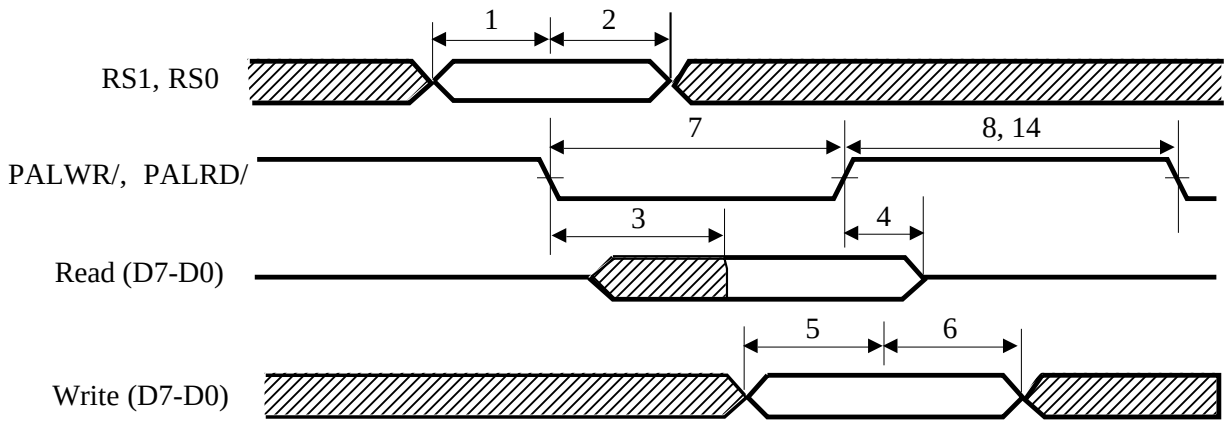
82C411 DAC CHARACTERISTICS (Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_O	Output Voltage	Io ≤ 10 mA	1.5	–	–	V
I_O	Output Current	Vo ≤ 1 V	21	–	–	mA
	Full Scale Error		–	–	±5	%
	DAC to DAC Correlation		±2.0	1.27	–	%
	DAC Linearity		.5	–	–	LSB
	Full Scale Setting Time		–	–	28	nS
	Rise Time	10% to 90%	–	–	6	nS
	Glitch Energy		–	–	200	pVsec
	Comparator Sensitivity		–	50	–	mV

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

82C411 AC TIMING CHARACTERISTICS - CPU INTERFACE

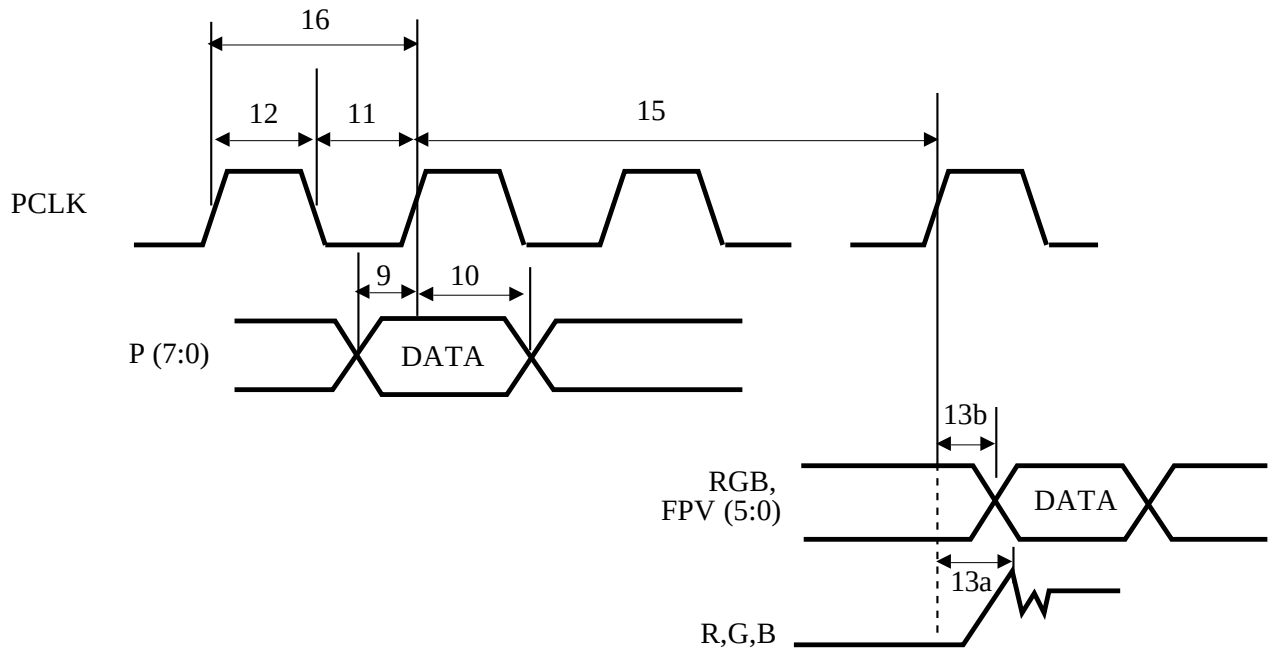
Symbol	Parameter	Min(ns)	Max(ns)
1	RS0, RS1 Setup Time	10	–
2	RS0, RS1, Hold Time	10	–
3	PALRD/ to Data Valid	–	45
4	PALRD/ Negated to Data Bus 3-Stated	5	–
5	Write Data Setup Time	10	–
6	Write Data Hold Time	10	–
7	PALWR/ or PALRD/ Low Pulse Width	50	–
8	PALRD/ High to PALRD/ or PALWR/ Low	8*PCLK	–
14	PALWR/ High to PALRD/ or PALWR/ Low	4*PCLK	–



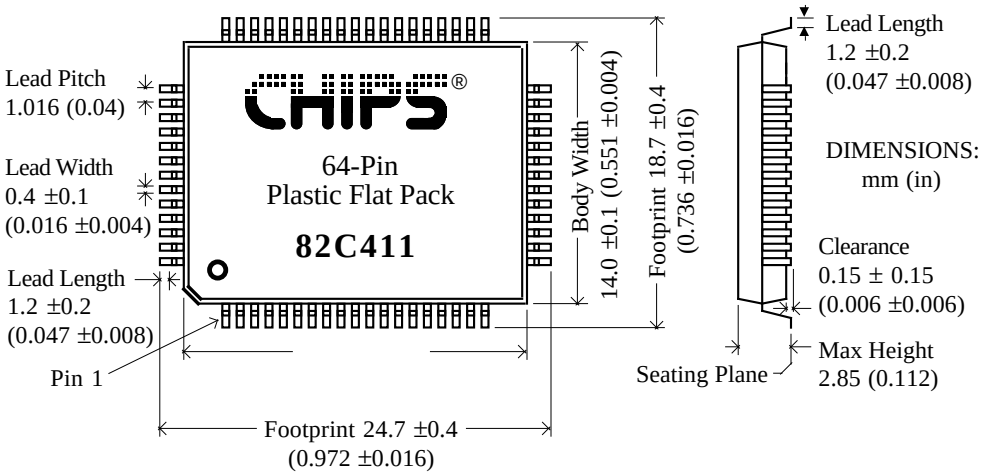
CPU Interface Timing

82C411 AC TIMING CHARACTERISTICS - Pixel I/O

Symbol	Parameter	Notes	Min(ns)	Max(ns)
9	Pixel Setup Time		4	–
10	Pixel Hold Time		4	–
16	Clock Cycle Time	40MHz	25	–
11	Clock Pulse Width Low Time		10	–
12	Clock Pulse Width High Time		10	–
13a	PCLK to Valid Analog Output		–	30
13b	PCLK to Valid Digital Output (load) = 10pf		5	21
–	Skew between any analog output on the same device		–	2
15a	Pixel in to analog output			3*PCLK
15b	Pixel in to digital output	SEL1:=0x or 10	6*PCLK	6*PCLK
15c	Pixel in to digital output	SEL1:0=11	4*PCLK	4*PCLK
	Analog output to Sense output delay		–	1000



Pixel I/O Timing


Lead Pitch
1.016 (0.04)
Lead Width
0.4 ±0.1
(0.016 ±0.004)
Lead Length
1.2 ±0.2
(0.047 ±0.008)
Pin 1
64-Pin
Plastic Flat Pack
82C411
Body Width
14.0 ±0.1 (0.551 ±0.004)
Footprint 18.7 ±0.4
(0.736 ±0.016)
Footprint 24.7 ±0.4
(0.972 ±0.016)
Lead Length
1.2 ±0.2
(0.047 ±0.008)
DIMENSIONS:
mm (in)
Clearance
0.15 ± 0.15
(0.006 ±0.006)
Max Height
2.85 (0.112)
Seating Plane