82C765 FLOPPY DISK CONTROLLER

- **Fully μPD765A and IBM-BIOS compatible**
- **Integrates all PC/XT, PC/AT, and most PS/2 Logic**
  - **—On chip 24 MHz Crystal Oscillator**
  - **—DMA enable logic**
  - **—IBM compatible address decode of A0-A2**
  - **—12 mA μP bus interface buffers**
  - **—40 mA floppy drive interface buffers**
  - **—Data rate and drive control registers**
- **Precision analog data separator**
  - **—Self-calibrating PLL and delay line**
  - **—Automatically chooses one of three filters**
  - **—Intelligent read algorithm**
- **Two pin programmable precompensation modes**
- **Other enhancements**
  - **—Up to 1 Mb/s data rate**
  - **—Implied seek up to 4000 tracks**
  - **—IBM or ISO formatting**
- **Low power CMOS, with power down mode**

This controller is a full featured floppy disk controller that is software compatible with the μPD765A, but also includes many additional hardware and software enhancements. These enhancements include additional logic specifically required for an IBM® PC, PC/XT, PC/AT, or PS/2 design.

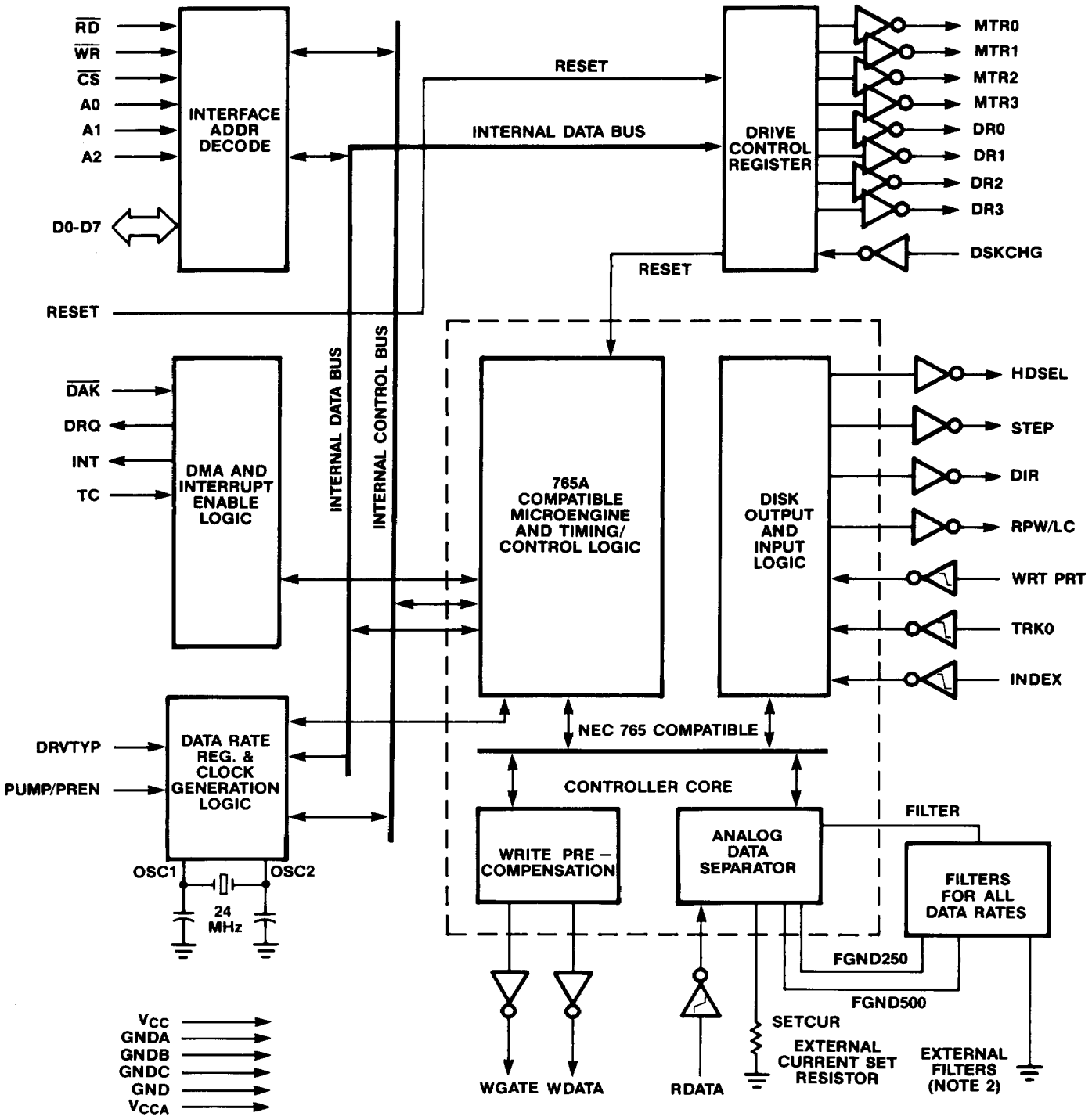
This controller incorporates a precision analog data separator, that includes a self-trimming delay line and VCO. Up to three external filters are switched automatically depending on the data rate selected. This provides optimal performance at the standard PC data rates of 250/300 kb/s, and 500 kb/s. It also enables optimum performance at 1 Mb/s (MFM). These features combine to provide the lowest possible PLL bandwidth, with the greatest lock range, and hence the widest window margin.

This controller includes write precompensation circuitry. A shift register is used to provide a fixed 125 ns early-late precompensation for all tracks at 500k/300k/250 kb/s (83 ns for 1 MB/s), or a precompensation value that scales with the data rate, 83 ns/125 ns/208 ns/250 ns for data rates of 1.0M/500k/300k/250 kb/s respectively.

Specifically to support the PC-AT and PC-XT design, the Floppy Disk Controller 82C765 includes address decode for the A0-A2 address lines, the motor/drive select register, data rate register for selecting 250/300/500 kb/s, Disk Changed status, dual speed spindle motor control, low write current and DMA/interrupt sharing logic. The controller also supports direct connection to the μP bus via internal 12 mA buffers. The controller also can be connected directly to the disk drive via internal open drain high drive outputs, and Schmitt inputs.

In addition to this logic the 82C765 includes many features to ease design of higher performance drives and future controller upgrades. These include 1.0 Mb/s data rate, extended track range to 4096, Implied seeking, working Scan Commands, motor control timing, both standard IBM formats as well as Sony 3.5" (ISO) formats, and other enhancements.

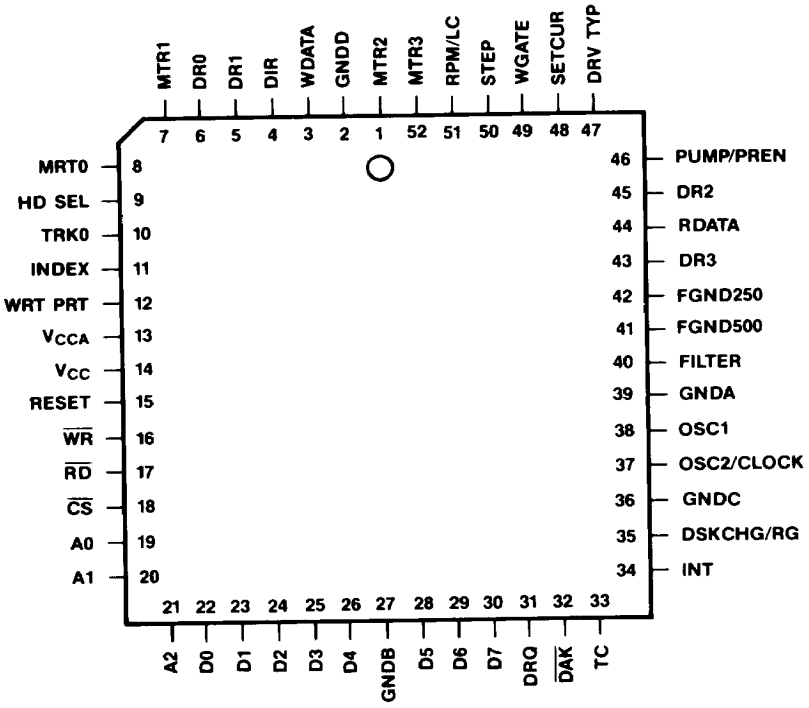
This device is available in a 52 pin Plastic Chip Carrier, and in a 48 pin Dual-In-Line package.



NOTE 1: THE MTR2, MTR3, DR2, AND DR3 ARE NOT AVAILABLE ON THE 48-PIN DIP.
NOTE 2: SEE FIGURE 4 FOR FILTER DESCRIPTION.
NOTE 3: TOTAL TRANSISTOR COUNT IS 29,700 (APPROX).

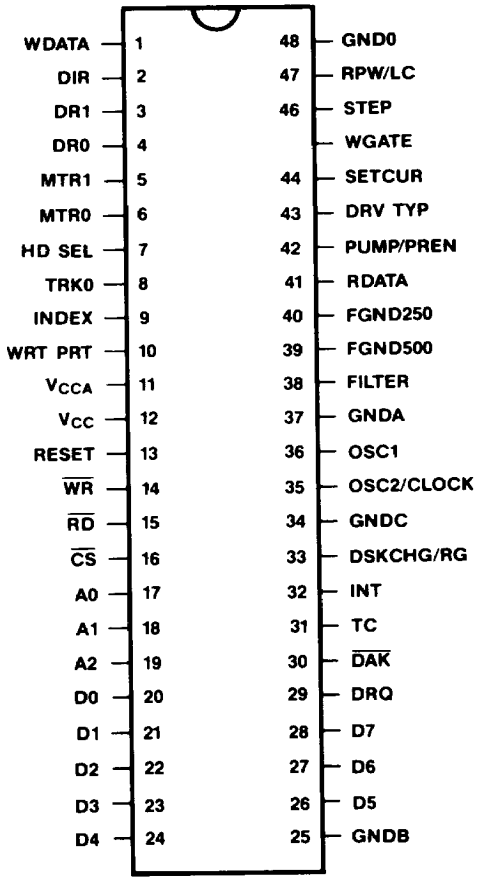
Figure 1. 82C765 Functional Block Diagram

Plastic Leaded Chip Carrier



TOP VIEW

Dual-In-Line Package



TOP VIEW

Connection Diagrams