# 82C5059 SINGLE CHIP PC-AT DISK CONTROLLER

## Memory Controller Features

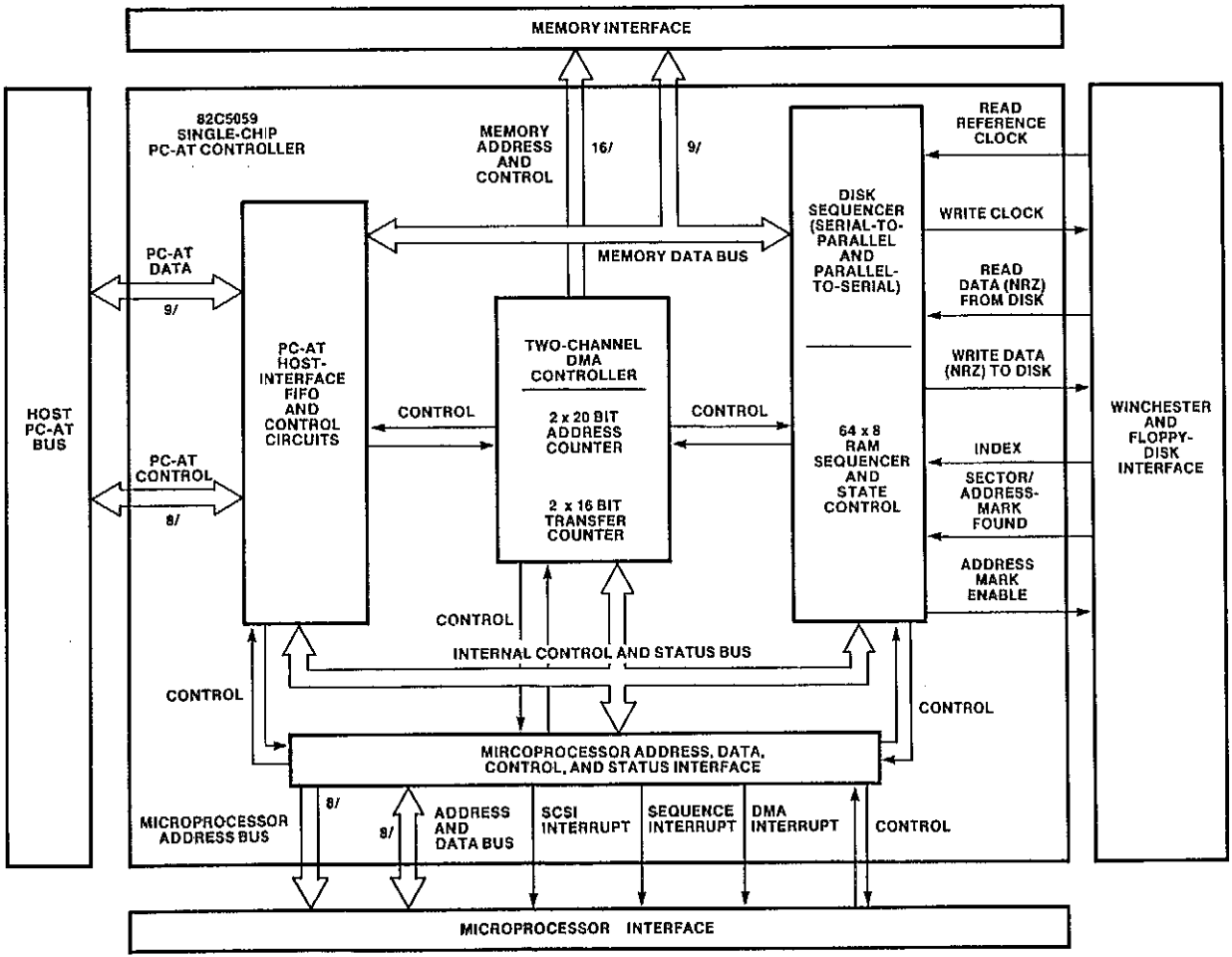
- Two Independent DMA Channels
- 13 Megabyte Device Bandwidth at 40MHz Clock
- 20-bit Address and 16-Bit Transfer Count Registers For Each Channel
- Holding Registers for Addresses Counts for Non-Contiguous Memory Transfers
- Bus Access Resolved on Channel Priority Basis
- Programmable:
  - — Interrupt Polarity
  - — Auto-Count Re-Initialization
  - — Memory Access Cycle Timing (2 To 5 Clock Cycles)
- Buffer Memory Address for 64K SRAM (2 Memory Chip Enables for 32K x 8 SRAM)
- DRAM Support For Up To 1 Megabyte

## Programmable Data Sequencer Features

- High Level Instruction Set
- Supports up to 20MHz Serial Bit Rate (NRZ)
- Programmable Disk Format
- NRZ Serial Disk Interface
- Direct Interface to ESDI Type Drives
- Multi-Sector Transfer Capability with Automatic Sector Increment
- Programmable Automatic ID Retries
- ESDI ID Sync Timeout Programmable
- ESDI Write Gate to AM ENABLE Programmable
- Format Track With Data From Buffer
- Programmable Write Gate Disable for Embedded Servo
- 32, 48, 56 Bit ECC Polynomial

## AT Interface Features

- Direct Interface to AT-Compatible Systems, Including 40-Pin Bus Interface
- High Current Drivers for Host Interface
- Schmidt Trigger Inputs Form Host Interface
- Configurable Primary or Secondary Address
- 2 Word FIFO
- Automatic BUSY, INTRQ and ECC Mode
- Flexible Interrupt Capability
- Advanced 1.5$\mu$ CMOS, Low Power Techonology
- 100-Pin Quad Flat Pack Packaging


MEMORY INTERFACE
82C5059
SINGLE-CHIP
PC-AT CONTROLLER
MEMORY
ADDRESS
AND
CONTROL
16/
9/
READ
REFERENCE
CLOCK
WRITE CLOCK
READ
DATA (NRZ)
FROM DISK
WRITE DATA
(NRZ) TO DISK
INDEX
SECTOR/
ADDRESS-
MARK
FOUND
ADDRESS
MARK
ENABLE
DISK
SEQUENCER
(SERIAL-TO-
PARALLEL
AND
PARALLEL-
TO-SERIAL)
64 x 8
RAM
SEQUENCER
AND
STATE
CONTROL
MEMORY DATA BUS
PC-AT
DATA
9/
PC-AT
CONTROL
8/
PC-AT
HOST-
INTERFACE
FIFO
AND
CONTROL
CIRCUITS
TWO-CHANNEL
DMA
CONTROLLER
2 x 20 BIT
ADDRESS
COUNTER
2 x 16 BIT
TRANSFER
COUNTER
CONTROL
CONTROL
CONTROL
INTERNAL CONTROL AND STATUS BUS
CONTROL
CONTROL
MIRCOPROCESSOR ADDRESS, DATA,
CONTROL, AND STATUS INTERFACE
HOST
PC-AT
BUS
WINCHESTER
AND
FLOPPY-
DISK
INTERFACE
MICROPROCESSOR
ADDRESS BUS
8/
8/
ADDRESS
AND
DATA BUS
SCSI
INTERRUPT
SEQUENCE
INTERRUPT
DMA
INTERRUPT
CONTROL
MICROPROCESSOR INTERFACE

## Introduction

The 82C5059 Single Chip PC-AT Controller is a CMOS LSI Applications Specific Integrated Circuit (ASIC) designed to be the primary component in a high-performance intelligent PC-AT Winchester disk controller system. The 82C5059 single chip controller provides three essential functions in a disk controller system: it manages the flow of data for a serial peripheral, it controls access to the external RAM buffer memory that is required for such transfers and it directly interfaces to a PC-AT type system bus. The 82C5059 is designed to be used with a microprocessor having either a Z8- or 8051-type bus structure.

The 82C5059 consists of three functional sections:

1. A DMA controller
2. A data sequencer
3. A PC-AT interface controller

The 82C5059 incorporates a dual-bus architecture, providing separate ports for microprocessor and memory buffer operations. With the goal of achieving the highest possible performance, this dual-bus structure is used so that disk data transfers can occur simultaneously with microprocessor operations.

In the DMA controller, Channel 0 is used for moving blocks of data between the data sequencer and the external buffer, while Channel 1 is used for moving blocks of data between the PC-AT host interface and the buffer. When the data sequencer is not using Channel 0, this channel can also be used to allow the microprocessor to access the RAM buffer. DMA controller operation is programmed by writing the DMA controller registers, while operation may be monitored by reading the DMA controller registers.

The programmable data sequencer provides format control, error detection, and serial/parallel (SERDES) conversion functions normally associated with disk controllers. It is designed to be used with NRZ (Non-Return to Zero) interfaces such as those used in the ESDI (Enhanced Small Device Interface) or any of the CHIPS family of encode/decode VCO devices. Flexible operation of the sequencer is made possible by write registers that program its operation, while read registers allow the firmware to monitor operation. In addition, complete flexibility in disk formatting is permitted by a 64-byte on-device format RAM, which is accessed through three of the data sequencer write registers (WR25, WR30 & WR31).

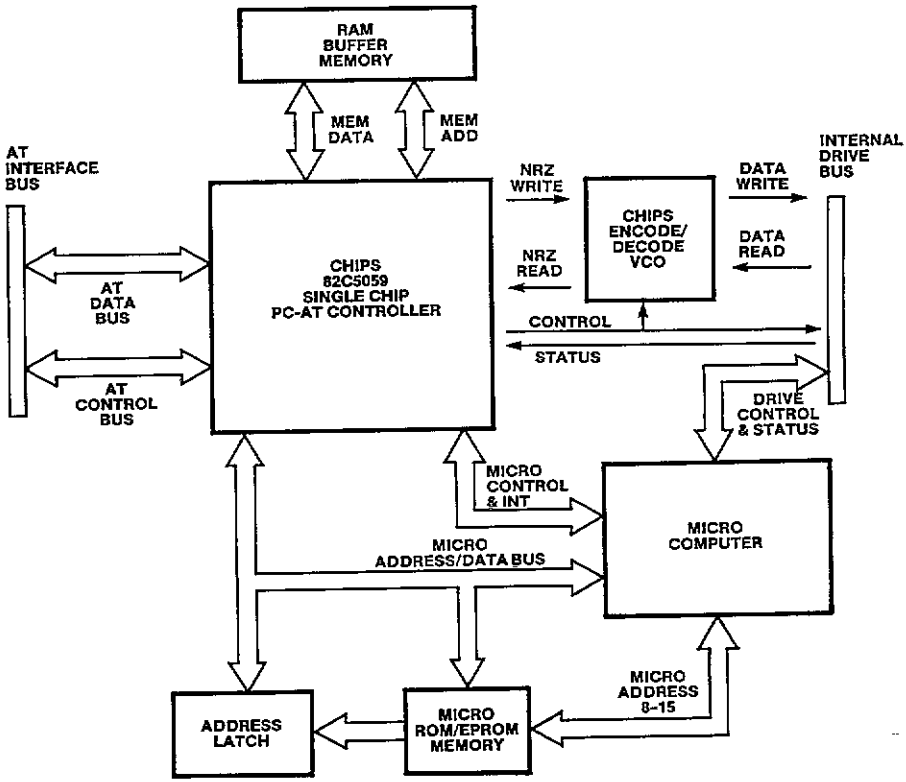
In addition to an external RAM buffer, a byte-oriented microprocessor such as the Z8 or 8051, with its associated memory, the 82C5059 may be connected with the CHIPS 10C5070 Encode/Decode/PLL for MFM encoding/decoding up to 5 Mbits/second, or the 10C5027 Encode/Decode/PLL for RLL 2,7 encoding/decoding up to 10 Mbits/second thus providing a complete controller solution for an embedded PC-AT interfacing disk drive.

### Ordering Information

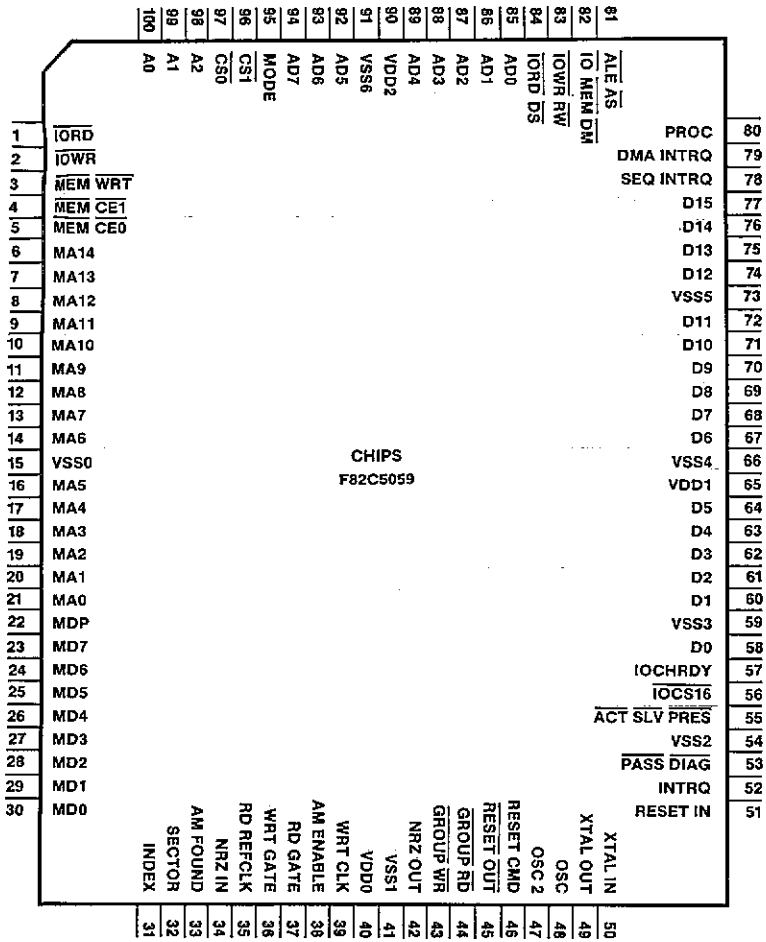
The 82C5059 can be ordered using the following part number:

F82C5059 (100-Pin QFP)

Evaluation samples are available now. Production orders accepted with standard leadtimes.




**F82C5059 Typical System Configuration**


CHIPS
F82C5059
1 IORD
2 IOWR
3 MEM WRT
4 MEM CE1
5 MEM CE0
6 MA14
7 MA13
8 MA12
9 MA11
10 MA10
11 MA9
12 MA8
13 MA7
14 MA6
15 VSS0
16 MA5
17 MA4
18 MA3
19 MA2
20 MA1
21 MA0
22 MDP
23 MD7
24 MD6
25 MD5
26 MD4
27 MD3
28 MD2
29 MD1
30 MD0
31 INDEX
32 SECTOR
33 AM FOUND
34 NRZ IN
35 RD REFCLK
36 WRT GATE
37 RD GATE
38 AM ENABLE
39 WRT CLK
40 VDD0
41 VSS1
42 NRZ OUT
43 GROUP WR
44 GROUP RD
45 RESET OUT
46 RESET CMD
47 OSC 2
48 OSC
49 XTAL OUT
50 XTAL IN
51 RESET IN
52 INTRQ
53 PASS DIAG
54 VSS2
55 ACT SLV PRES
56 IOCS16
57 IOCHRDY
58 D0
59 VSS3
60 D1
61 D2
62 D3
63 D4
64 D5
65 VDD1
66 VSS4
67 D6
68 D7
69 D8
70 D9
71 D10
72 D11
73 VSS5
74 D12
75 D13
76 D14
77 D15
78 SEQ INTRQ
79 DMA INTRQ
80 PROC
81 ALE AS
82 IO MEM DM
83 IOWR RW
84 IORD DS
85 AD0
86 AD1
87 AD2
88 AD3
89 AD4
90 VDD2
91 VSS6
92 AD5
93 AD6
94 AD7
95 MODE
96 CS1
97 CS0
98 A2
99 A1
100 A0

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Chips and Technologies, Inc.
3050 Zanker Road, San Jose, CA 95134 408-434-0600 telex 272929 CHIPS UR

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