82C460

Flat Panel Color Palette

Data Sheet

August 1990

P R E L I M I N A R Y

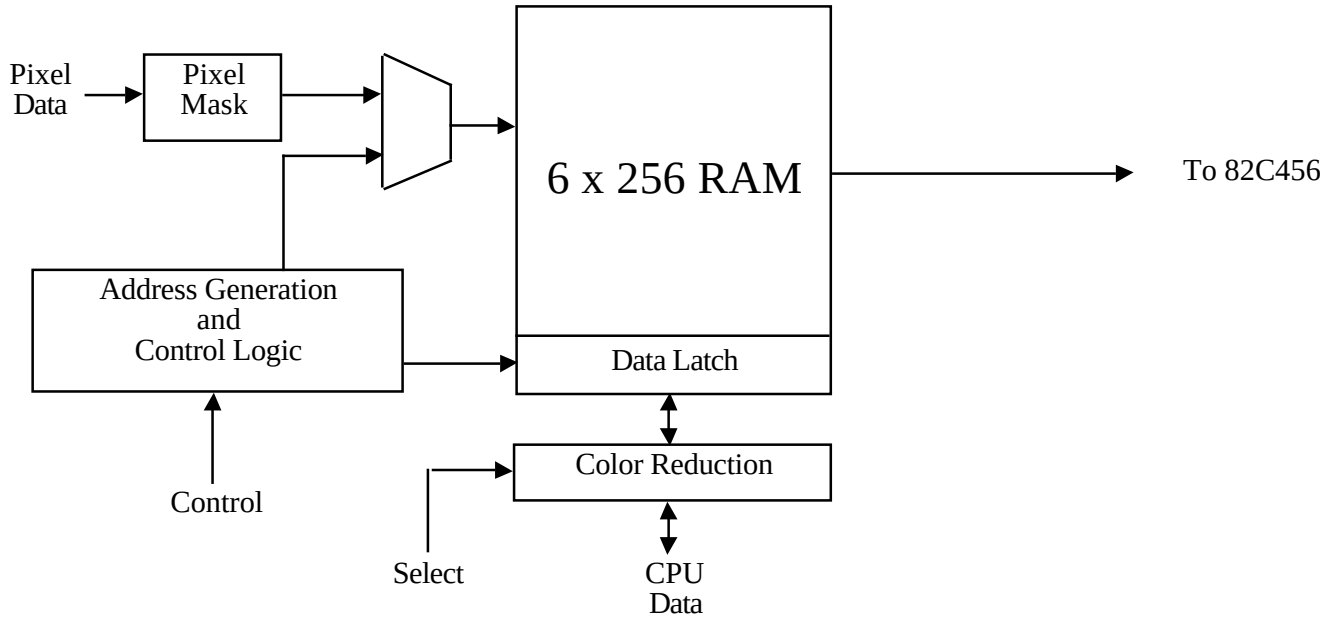
CHIPS®

Chips and Technologies, Inc.
3050 Zanker Road
San Jose, California 95134
Phone: 408-434-0600
Telex: 272929 CHIPS UR
FAX: 408-434-6452

Publication No.: DS85
Stock No.: 010460-001
Revision No.: 0.07

82C460
Flat Panel Color Palette

- Flat Panel Digital Palette
- Provides full VGA compatibility on flat panels
- Direct connection to Chips & Technologies 82C456 Enhanced Flat Panel/CRT VGA controller
- Three RGB to Grayscale reduction techniques
- 64 Gray levels for monochrome panels
- 64 Colors for color panels
- All Flat Panel palette functions integrated in a single package
- Supports LCD, Plasma, and Electro Luminescent flat panels



82C460 BLOCK DIAGRAM

Revision History

Revision	Date	By	Comment
0.04	7/6/90	ST	Extracted 82C460 Data Sheet from 82C456/460 Data Sheet Rev. 0.03.
0.05	7/6/90	SV	Revised Block Diagram.
0.06	7/17/90	MR	Grammatical and Formatting Changes.
0.07	7/24/90	ST	Initial Release.

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Introduction

The 82C460 Flat Panel Palette is designed to provide the external color palette data to the 82C456 for processing and display on the flat panel. The CPU interface is identical to that of an Inmos IMSG176 style RAMDAC. The 82C460 is used in parallel with the standard RAMDAC. All CPU address and data information is monitored by the 82C460.

The palette read and write signals pass through the 82C460 allowing selective reading and writing of the two palettes. Separate write enables are provided for each palette. A single read select is provided to determine which palette is read by the CPU.

During CPU writes to the external color palette, the 82C460 latches the color data as it is written to the color palette. After the blue data is written to the storage latch, the 82C460 reduces the data to 6 bits (64 color or gray levels) and then writes it to the palette RAM.

During display, the pixel input data is used as an address to the palette RAM. The RAM data is then output for processing by the 82C456.

Reduction Techniques

Four reduction algorithms are provided to reduce the 18 bit RGB data to 6 bits. The reduction algorithms are as follows:

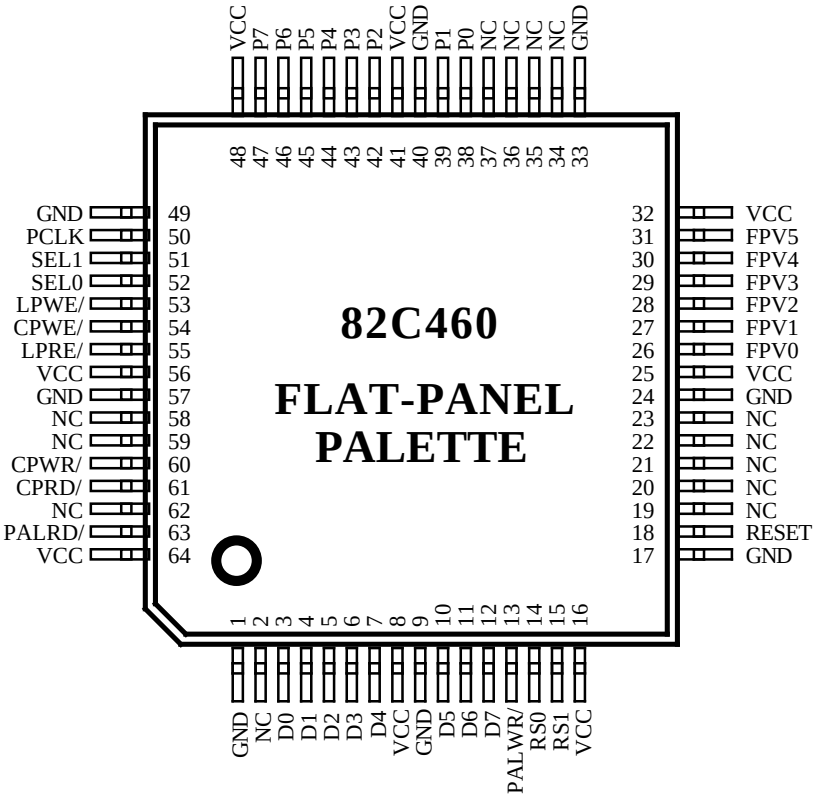
NTSC: This is the industry standard technique for reducing RGB color information to gray levels. The weighting is 5/16R +9/16G +1/8B. The data is reduced in a two stage adder and the 6 most significant bits are stored. This technique is selected when the select bits are both 0 (SEL1:0=00) .

EQUAL: In this technique the RGB values are equally weighted. The reduction is 5/16R +3/8G +5/16B. This technique is used when SEL1:0 = 01

GREEN only: This reduction type stores only the green (G) value. This produces the same display as an IBM monochrome CRT. This is used when SEL1:0 = 10.

COLOR: When SEL1:0 = 11, the two most significant bits of each color are stored without modification. This is used for displaying 64 colors on RGB color panels.

82C460 Pinouts



82C460 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
50	PCLK	In	Both	PIXEL CLOCK. The rising edge samples and latches the Pixel Address inputs. It controls progress of the data through the four stage pipeline to the Flat Panel Palette to the outputs.
47	P7	In	Both	PIXEL DATA. The input address to the Flat Panel Palette RAM.
46	P6	In	Both	
45	P5	In	Both	
44	P4	In	Both	
43	P3	In	Both	
42	P2	In	Both	
39	P1	In	Both	
38	P0	In	Both	
31	FPV5	Out	Both	FLAT PANEL VIDEO. The outputs of the Flat Panel Palette RAM as addressed by the Pixel Address.
30	FPV4	Out	Both	
29	FPV3	Out	Both	
28	FPV2	Out	Both	
27	FPV1	Out	Both	
26	FPV0	Out	Both	
13	PALWR/	In	Low	PALETTE WRITE ENABLE. This signal is used for CPU writes to the external color palette. RS 1:0 are latched on the falling edge and D7:0 on the rising edge during an CPU write operation.
63	PALRD/	In	Low	PALETTE READ ENABLE. This signal is used for CPU reads from the external color palette. RS 1:0 are latched on the falling edge. The data is presented when this signal is low.
15	RS1	In	Both	REGISTER SELECT 1 & 0. These two lines are sampled during the falling edges of the enable signals (PALWR/ or PALRD/) and select one of the three internal registers.
14	RS0	In	Both	

RS1	RS0	REGISTER
0	0	Address Register (RAM Write Mode)
1	1	Address Register (RAM Read Mode)
0	1	Palette RAM
1	0	Pixel Mask Register

82C460 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
12 11 10 7 6 5 4 3	D7 D6 D5 D4 D3 D2 D1 D0	I/O I/O I/O I/O I/O I/O I/O I/O	Both Both Both Both Both Both Both Both	PALETTE DATA. Read/write data to the internal registers. During the write cycle, the rising edge of PALWR/ latches the data into the selected register. When PALRD/ is inactive (high) the data I/O lines will be 3-stated.
51 52	SEL1 SEL0	In In	Both Both	SELECT 1 & 0. These signals select the algorithm used to reduce the RGB data before it is stored in the Flat Panel Palette RAM. The four algorithms are: **SEL1 SEL0 — RAM Data Mode** 0 0 — NTSC Weighting 0 1 — Equivalent 1 0 — GREEN only 1 1 — Color
53	FPWE/	In	Low	FLAT PANEL PALETTE WRITE ENABLE. This signal, when low, allows writes to occur to the Flat Panel Palette RAM.
54	CPWE/	In	Low	COLOR PALETTE WRITE ENABLE. This signal, when low, allows the CPWR/ output to go active (low) during palette write cycles (PALWR/ low)
55	FPRE/	In	Low	FLAT PANEL PALETTE READ ENABLE. This signal, when low, selects reads to occur from the Flat Panel Palette. If the signal is low, the CPRD/ is not active and read cycles are handled by the 82C460. When high, the 82C460 does not arrive data on the data outputs and the CPRD/ signal will be active for palette read cycles.
61	CPRD/	Out	Low	COLOR PALETTE READ. This signal is active during palette read cycles if the FPRE/ pin is high.
60	CPWR/	Out	Low	COLOR PALETTE WRITE. This signal is active during palette write cycles if the CPWE/ pin is low.

82C460 PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
18	RESET	In	High	RESET. The RESET signal should be brought high after power is applied.
8 16 25 37 41 48 56 64	VCC	In	-	POWER
1 9 17 24 33 40 49 57	GND	In	-	GROUND
2 19 20 21 22 23 34 35 36 37 58 59 62	NC	-	-	NO CONNECTION. These pins are reserved for future expansion. They should be left floating.

82C460 Electrical Specifications

82C460 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Dissipation	P_D	--	500	mW
Supply Voltage	V_{CC}	-0.5	7.0	V
Input Voltage	V_I	-0.5	V_{CC}+0.5	V
Output Voltage	V_O	-0.5	V_{CC}+0.5	V
Operating Temperature (Ambient)	T_{OP}	-25	85	° C
Storage Temperature	T_{STG}	-55	150	° C
Output Current	I_0	-20	20	mA

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C460 Normal Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	℃
Case Temperature	T_C	0	85	℃

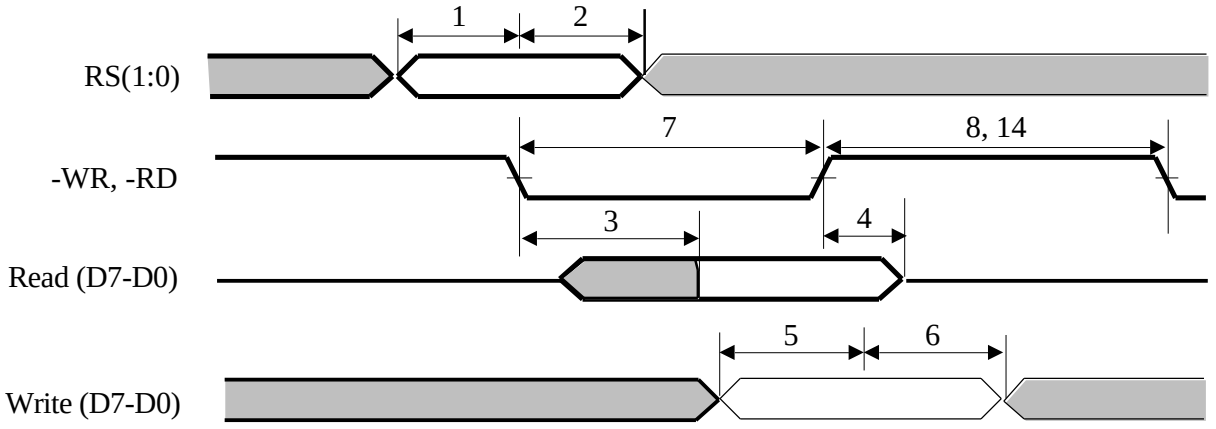
82C460 DC Characteristics (Under Normal Operating Conditions Unless Noted Otherwise)

Parameter	Notes	Symbol	Min	Typ	Max	Units
Power Supply Current		I_{CC}	--	20	--	mA
Input Leakage Current		I_{IL}	–10	--	+10	uA
Output Leakage Current	(High Impedance)	I_{OZ}	–10	--	+10	uA
Input Low Voltage		V_{IL}	--	--	Vcc * 0.3	V
Input High Voltage		V_{IH}	Vcc * 0.7	--	--	V
Output Low Voltage	I_{OL} = - 4mA	V_{OL}	--	--	0.4	V
Output High Voltage	I_{OH} = 4mA	V_{OH}	Vcc-0.6	--	--	V
Capacitance, Input or Output		C	--	10	20	pF

Note: Electrical specifications contained herein are preliminary and subject to change without notice.

82C460 AC Timing Characteristics - CPU Interface

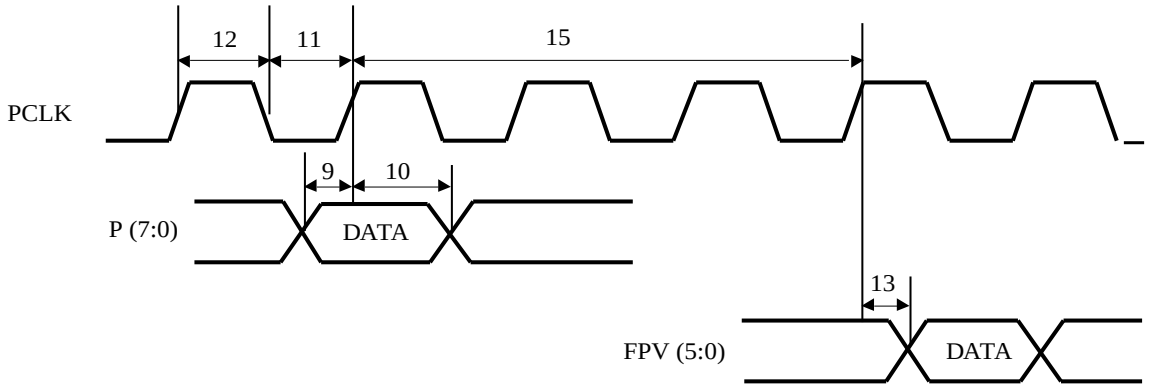
Parameter	Symbol	Min(ns)	Max(ns)
RS0, RSI Setup Time	1	10	--
RS0, RSI, Hold Time	2	10	--
PALRD/ to Data Valid	3	--	45
PALRD/ Negated to Data Bus 3-Stated	4	5	--
Write Data Setup Time	5	10	--
Write Data Hold Time	6	10	--
PALRD/, PALWR/ Pulse Width Low	7	50	--
PALRD/ Pulse Width High	8	4 * PCLK	--
PALWR/ Pulse Width High	14	5 * PCLK	--



82C460 CPU Timing

82C460 AC Timing Characteristics - Output Timing

Parameter	Symbol	Min(ns)	Max(ns)
Pixel Setup Time	9	4	--
Pixel Hold Time	10	4	--
Clock Pulse Width Low Time	11	16	--
Clock Pulse Width High Time	12	16	--
PCLK to Valid FPV-out	13	5	21
P-in to FPV-out delay	15	4*PCLK	4*PCLK



82C460 Output Timing

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82C460 Mechanical Specifications