



82C456A



Enhanced Flat Panel/CRT
VGA Controller

Data Sheet Addendum

P R E L I M I N A R Y



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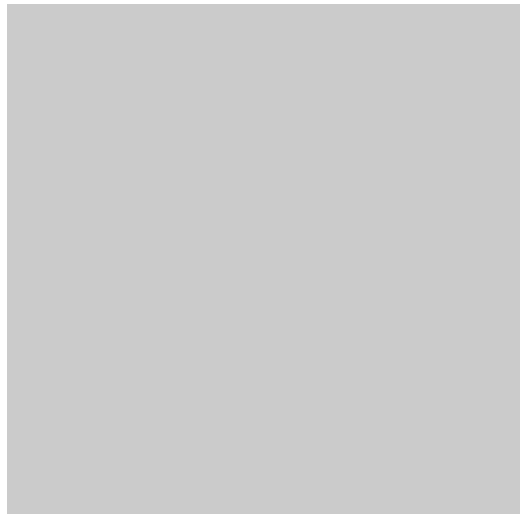
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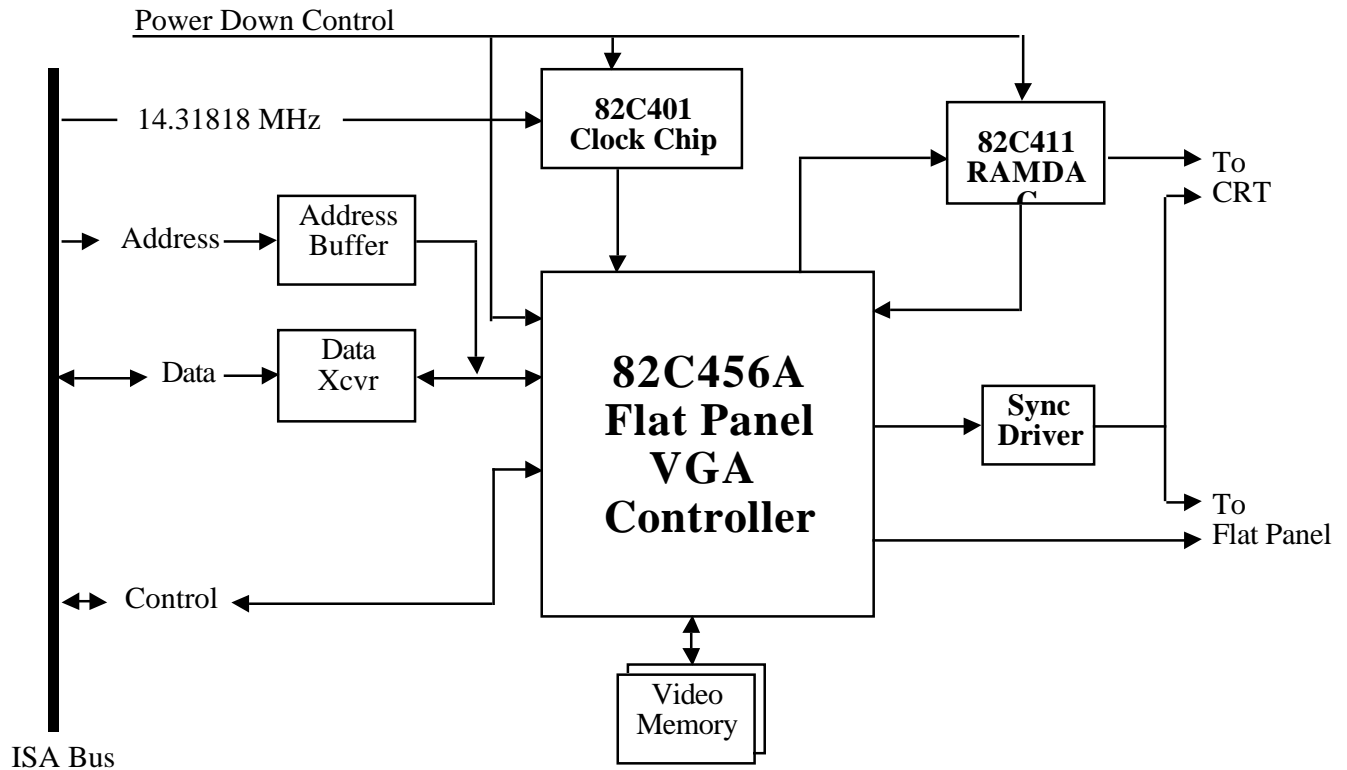
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82C456A Enhanced Flat Panel / CRT VGA Controller

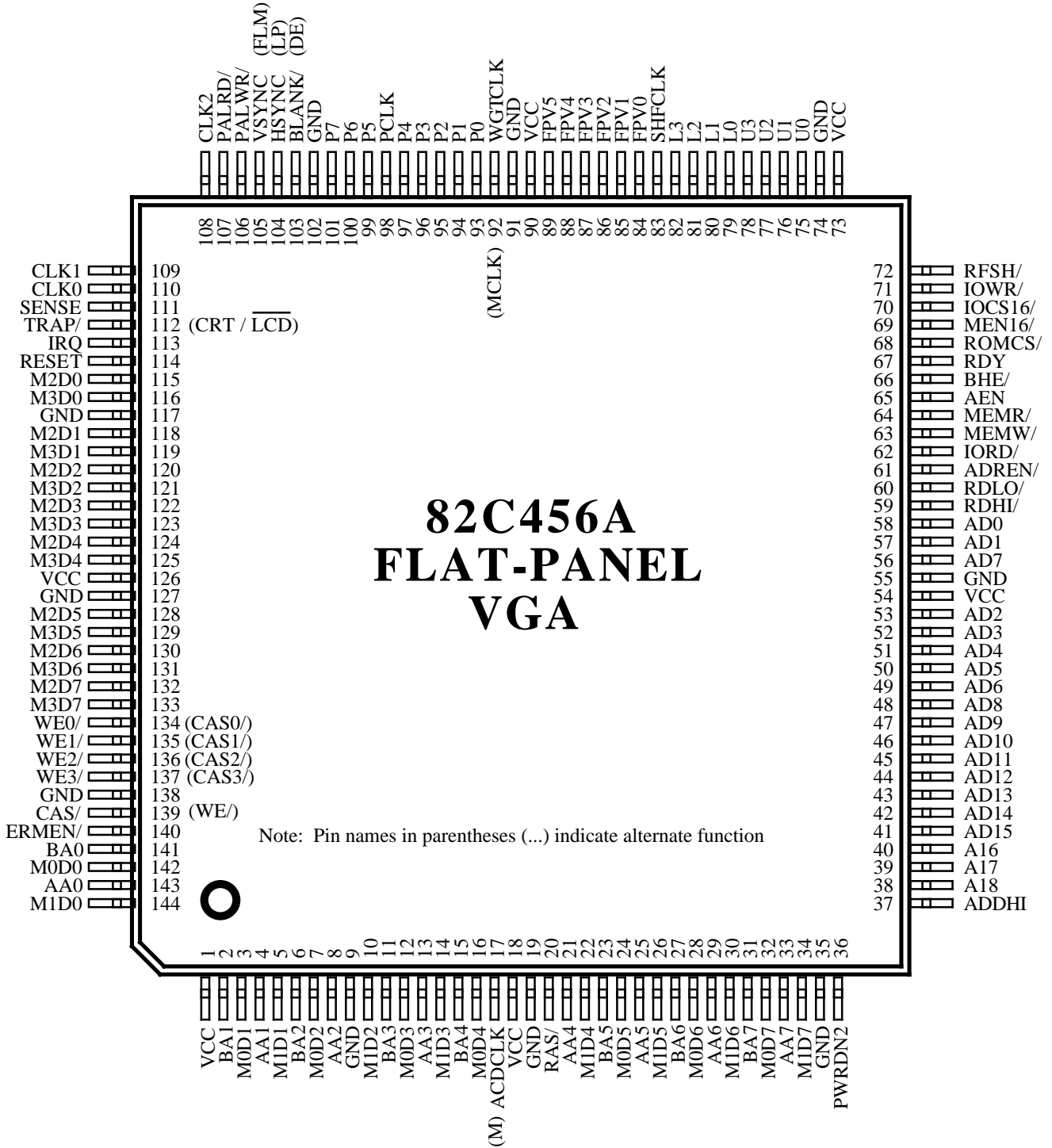
- Minimal component, low power VGA LCD flat panel controller
- Supports analog and digital CRT monitors and LCD, Plasma, and Electro Luminescent panels
- Up to 64 gray levels on monochrome panels
- Direct Support for 64K x 16 DRAMs
- RGB color to grayscale reduction techniques
Drives color panels with 64 colors
- SMARTMAP™ intelligent color to grayscale conversion
- Flicker-Free 64 gray scales on Fast response "mouse quick" FSTN LCD panels
- Text enhancement feature improves contrast on flat panel displays
- Programmable vertical compensation techniques increase usable display area
- IBM VGA monochrome CRT compatibility on monochrome panels
- Advanced SLEEP mode minimizes power consumption
- Proven DOS and OS/2™ compatibility
- Full backwards compatibility with IBM EGA, CGA, MDA and Hercules graphics standards

The 82C456A is pin compatible with and a direct drop-in replacement for the 82C456. All features, functionality, register descriptions, and application schematics for the 82C456A can be found in the 82C456 data sheet. This document is an addendum to the 82C456 data sheet in that it lists and describes all additional features of the 82C456A.



82C456A System Block Diagram

82C456A Pinouts



82C456A Pin List

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
ACDCLK (M)	17	FPV3	87	M3D3	123
A16	40	FPV4	88	M3D4	125
A17	39	FPV5	89	M3D5	129
A18	38	GND	9	M3D6	131
AA0	143	GND	19	M3D7	133
AA1	4	GND	35	MEMR/	64
AA2	8	GND	55	MEMW/	63
AA3	13	GND	74	MEN16/	69
AA4	21	GND	91	P0	93
AA5	25	GND	102	P1	94
AA6	29	GND	117	P2	95
AA7	33	GND	127	P3	96
AD0	58	GND	138	P4	97
AD1	57	HSYNC (LP)	104	P5	99
AD10	46	IOCS16/	70	P6	100
AD11	45	IORD/	62	P7	101
AD12	44	IOWR/	71	PALRD/	107
AD13	43	IRQ	113	PALWR/	106
AD14	42	L0	79	PCLK	98
AD15	41	L1	80	PWRDN2	36
AD2	53	L2	81	RAS/	20
AD3	52	L3	82	RDHI/	59
AD4	51	M0D0	142	RDLO/	60
AD5	50	M0D1	3	RDY	67
AD6	49	M0D2	7	RESET	114
AD7	56	M0D3	12	RFSH/	72
AD8	48	M0D4	16	ROMCS	68
AD9	47	M0D5	24	SHFCLK	83
ADDHI	37	M0D6	28	SENSE	111
ADREN/	61	M0D7	32	TRAP/	112
AEN	65	M1D0	144	U0	75
BA0	141	M1D1	5	U1	76
BA1	2	M1D2	10	U2	77
BA2	6	M1D3	14	U3	78
BA3	11	M1D4	22	VCC	1
BA4	15	M1D5	26	VCC	18
BA5	23	M1D6	30	VCC	54
BA6	27	M1D7	34	VCC	73
BA7	31	M2D0	115	VCC	90
BHE/	66	M2D1	118	VCC	126
BLANK/ (DE)	103	M2D2	120	VSYSN (FLM)	105
CAS/ (WE/)	139	M2D3	122	WE0/ (CAS0/)	134
CLK0	110	M2D4	124	WE1/ (CAS1/)	135
CLK1	109	M2D5	128	WE2/ (CAS2/)	136
CLK2	108	M2D6	130	WE3/ (CAS3/)	137
ERMEN/	140	M2D7	132	WGTCCLK (MCLK)	92
FPV0	84	M3D0	116		
FPV1	85	M3D1	119		
FPV2	86	M3D2	121		

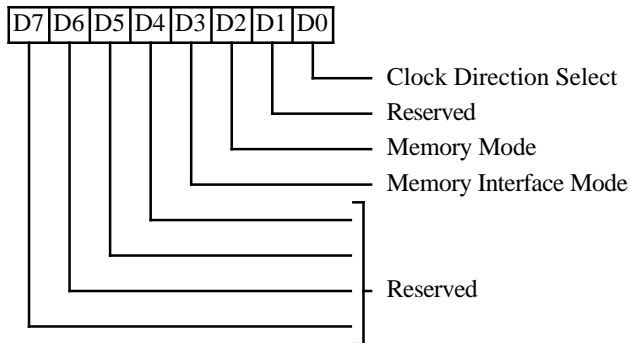
82C456A Extension Registers

The following pages describe the extended register bit definitions which are different for the 82C456A from the 82C456. The text in bold letters highlights the new bit definitions for the 82C456A.

MEMORY MODE REGISTER (XR04)

Read/Write at I/O Address 3B7h/3D7h

Index 04h



3 Memory Interface Mode

- 0 64K x 4 memory configuration
- 1 64K x 16 memory configuration

7-4 Reserved (0)

0 Clock Direction Select

- 0 CLK [2:0] are all inputs
- 1 CLK1 and CLK2 are general purpose outputs controlled by MISC output register bits 2 and 3. Pin 92 serves as the MCLK input. CLK0 is the dot clock input.

This bit may be set for compatibility with certain clock synthesizer chips (Note that use of the CHIPS 82C401 chip does not require setting this bit).

1 Reserved (0)

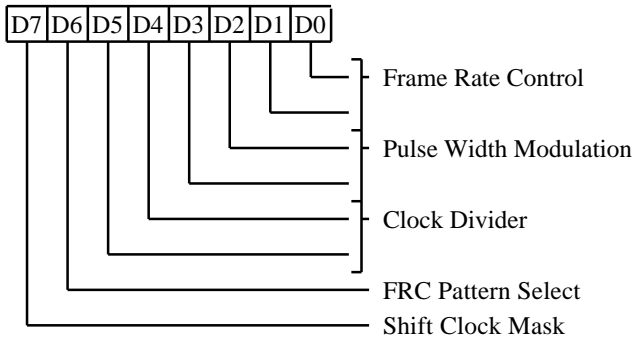
2 Memory Mode

- 0 Select VGA compatible memory mode (default on reset).
- 1 Select extended "Quad Mode". In this mode, display memory is mapped to the CPU address space as 4 pages of 64 Kbytes each (or 2 pages of 128 Kbytes each). The paging is controlled through the CPU Paging register (XR0B).

PANEL FORMAT REGISTER (XR50)

Read/Write at I/O Address 3B7h/3D7h

Index 50h



This register is effective only in flat panel mode as defined in bits 2-3 of XR51.

1-0 Frame Rate Control (FRC). These bits specify the gray levels simulated by the 82C456A on a frame by frame basis. This technique is used on flat panels that do not support gray levels internally, such as LCD panels.

- 00 No grayscale simulated for monochrome, 8 colors for color displays.
- 01 4 levels simulated for color panels only. (64 colors are displayed.)
- 10 64 gray levels simulated for monochrome panels only.
- 11 Reserved.

3-2 Pulse Width Modulation (PWM). This technique is used on flat panels that support internal gray levels such as most plasma panels.

- 00 No gray levels.
- 01 4 levels of colors supported by the panel. Effective only with color panels. (64 colors are displayed.)
- 10 16 gray levels supported by the panel. Effective with monochrome panels only.
- 11 Reserved (0)

5-4 Clock Divide (CD). These bits specify the frequency ratio between the dot clock (CLK0, CLK1, CLK2) and the SHFCLK signal.

- 00 Shift clock frequency = dot clock frequency. This setting is used to output one pixel per clock with flat panel displays.
- 01 Shift clock frequency = dot clock frequency/2. This setting is used to output two pixels per clock with flat panel displays.
- 10 Shift clock frequency = dot clock frequency/4. This setting is used to output four pixels per clock with flat panel displays.
- 11 Shift clock frequency = dot clock frequency/8. This setting is used to output eight pixels per clock with flat panel displays.

6 FRC Control Bit

- 0 31 x 15 FRC Matrix Size
- 1 32 x 16 FRC Matrix Size

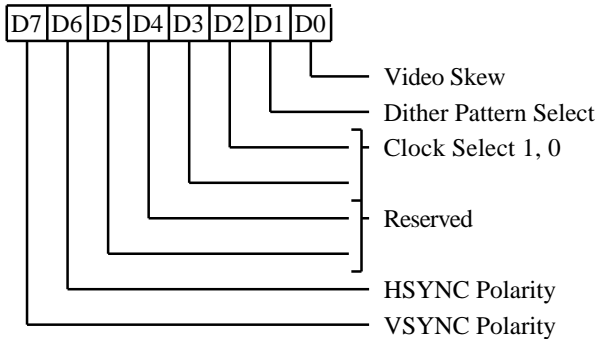
It is recommended that this bit be set to '1'.

7 Shift Clock Mask (SM).

- 0 Enable the SHIFT CLOCK to toggle outside the Display Enable interval.
- 1 Cause the Shift Clock to stop (low) outside the Display Enable interval.

ALTERNATE MISCELLANEOUS OUTPUT REGISTER (XR54)

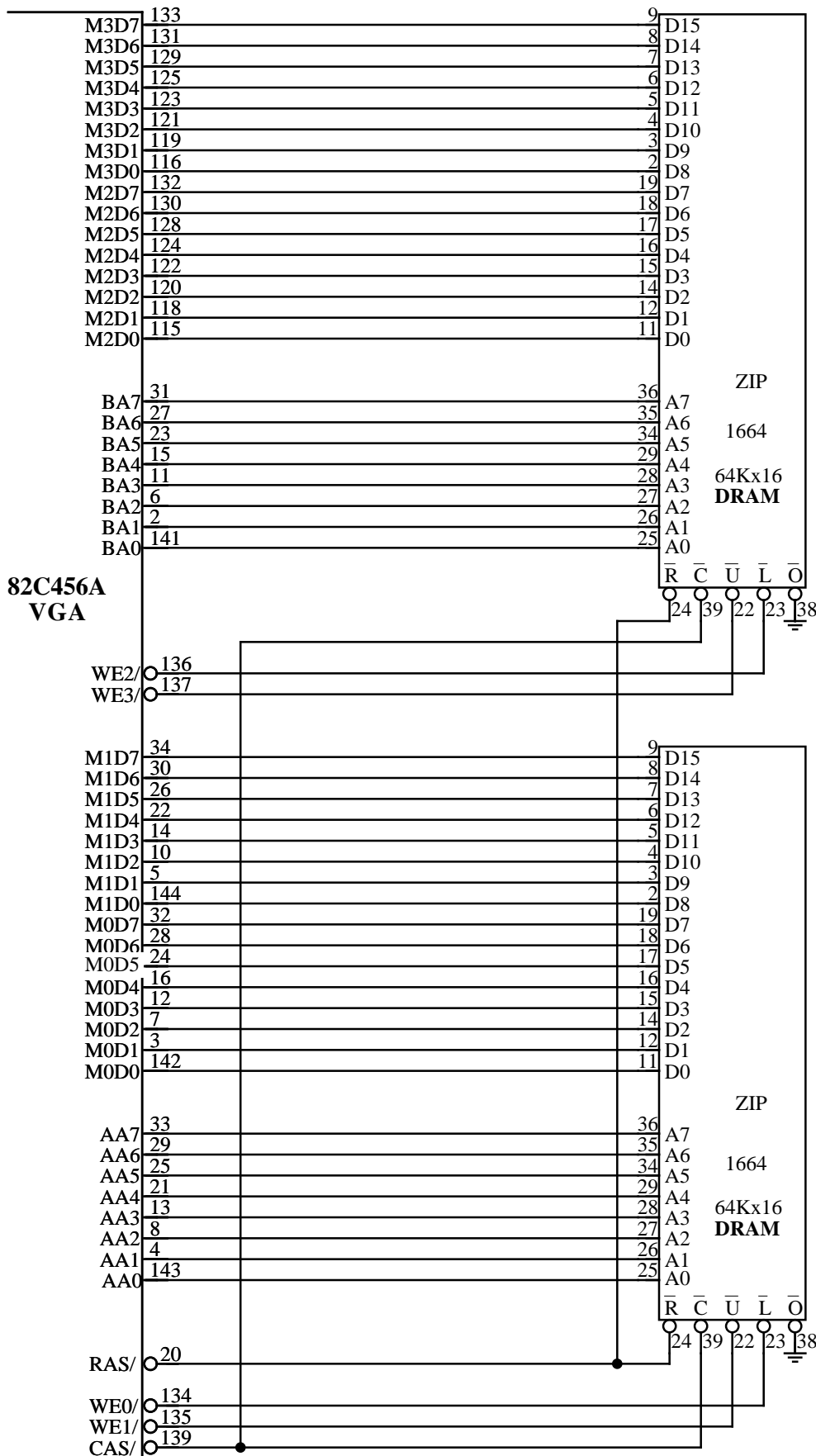
Read/Write at I/O Address 3B7h/3D7h
Index 54h



This register is used in Flat Panel modes.

- 0** Panel Video Skew
 - 0 No Panel Video data delay
 - 1 Video data delayed 1 clock cycle
 - 1** **FRC Pattern Select**
 - 0** Select Pattern A
 - 1** Select Pattern B

It is recommended that this bit be set to '1'.
 - 3-2** Clock Select Bits. These bits select the flat panel dot clock source as follows:
 - 00 Select CLK0
 - 01 Select CLK1
 - 10 Select CLK2
 - 11 Reserved
 - 5-4** Reserved (0)
 - 6** Hsync Polarity (0 = pos, 1 = neg)
 - 7** Vsync Polarity (0 = pos, 1 = neg)
- (The polarity of the Blank pin is controlled through the Video Interface Register.)



**82C456A
Display Memory
Circuit
64Kx16 DRAMs**

82C456A Mechanical Specifications

