82C456A

Enhanced Flat Panel/CRT
VGA Controller

Data Sheet Addendum

P R E L I M I N A R Y

CHIPS®

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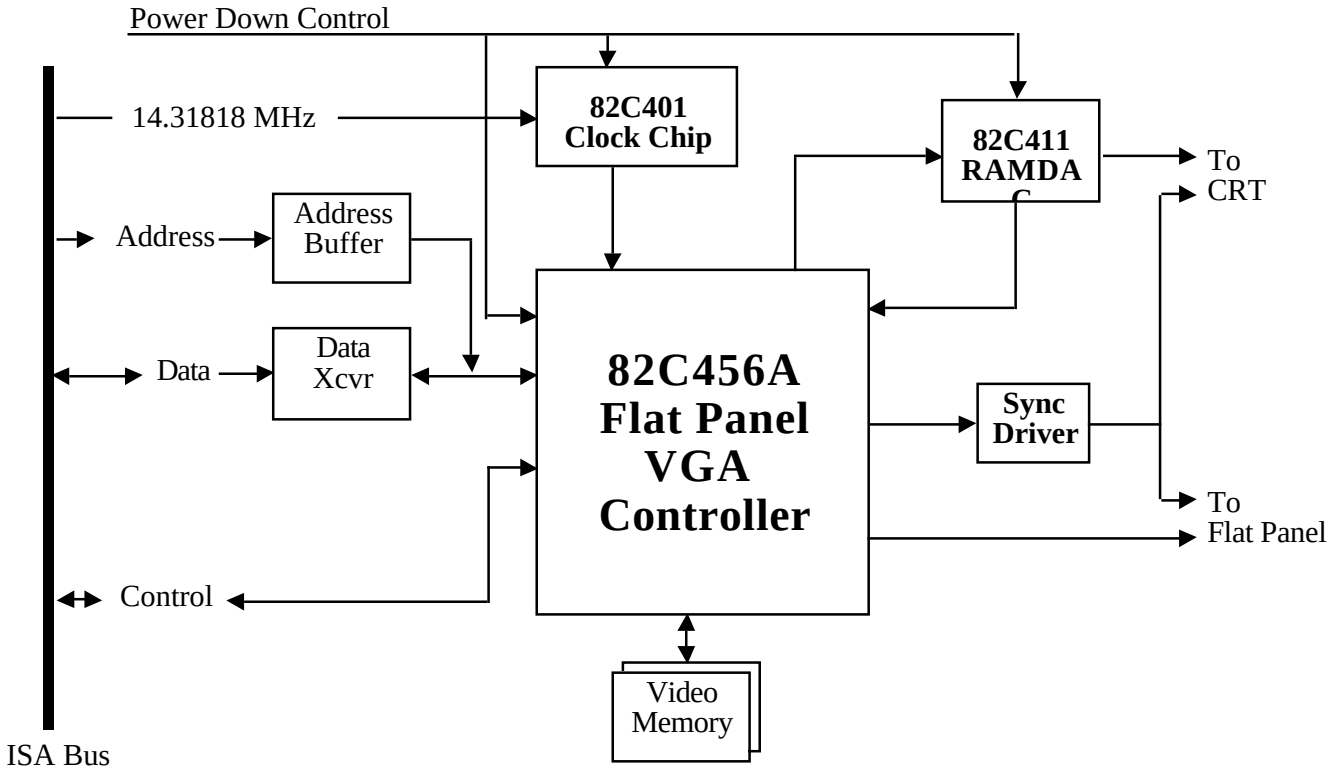
82C456A
Enhanced Flat Panel / CRT
VGA Controller

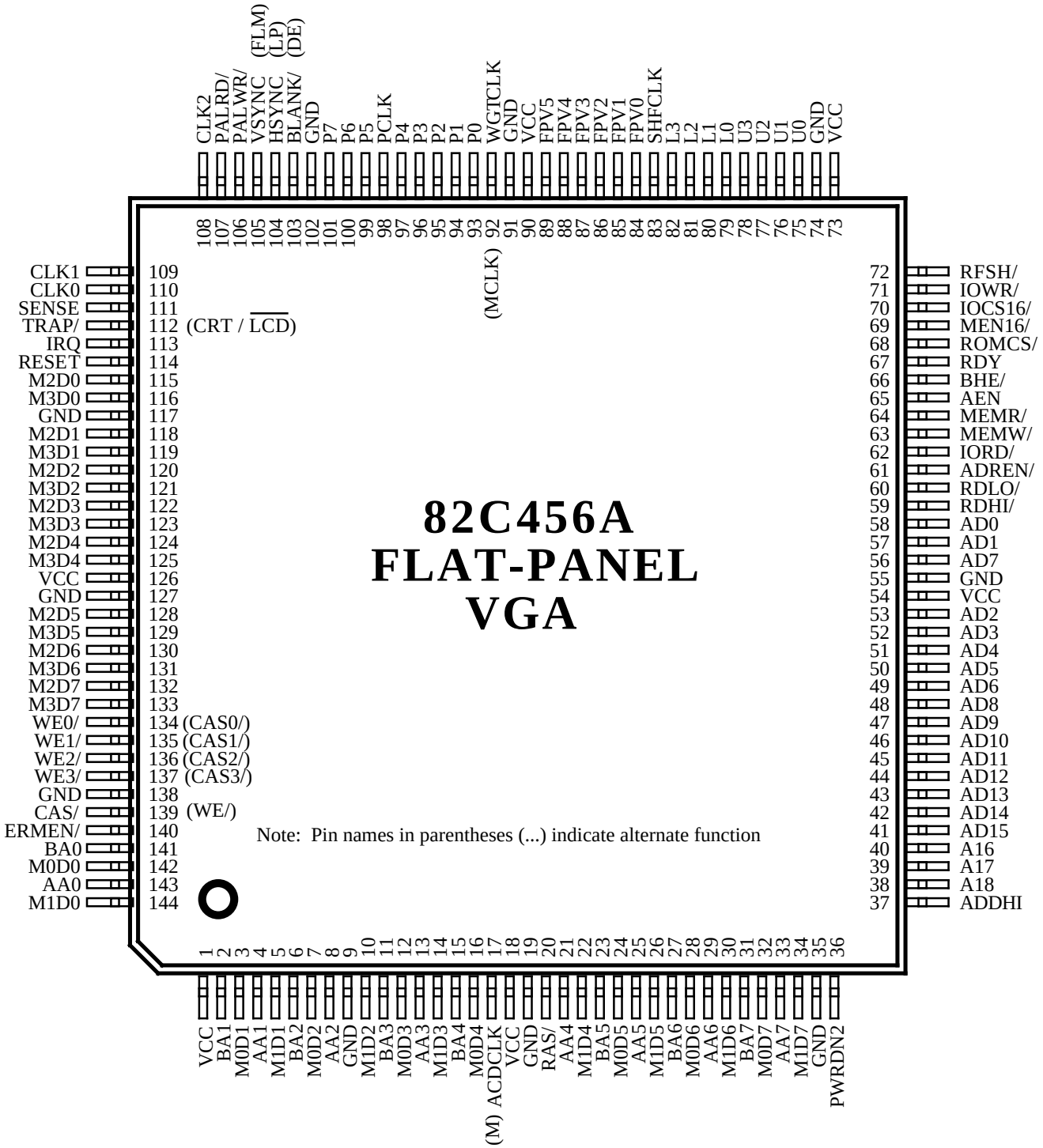
- Minimal component, low power VGA LCD flat panel controller
- Supports analog and digital CRT monitors and LCD, Plasma, and Electro Luminescent panels
- Up to 64 gray levels on monochrome panels
- Direct Support for 64K x 16 DRAMs
- RGB color to grayscale reduction techniques Drives color panels with 64 colors
- SMARTMAP™ intelligent color to grayscale conversion
- Flicker-Free 64 gray scales on Fast response "mouse quick" FSTN LCD panels
- Text enhancement feature improves contrast on flat panel displays
- Programmable vertical compensation techniques increase usable display area
- IBM VGA monochrome CRT compatibility on monochrome panels
- Advanced SLEEP mode minimizes power consumption
- Proven DOS and OS/2™ compatibility
- Full backwards compatibility with IBM EGA, CGA, MDA and Hercules graphics standards

The 82C456A is pin compatible with and a direct drop-in replacement for the 82C456. All features, functionality, register descriptions, and application schematics for the 82C456A can be found in the 82C456 data sheet. This document is an addendum to the 82C456 data sheet in that it lists and describes all additional features of the 82C456A.



82C456A System Block Diagram

82C456A Pinouts



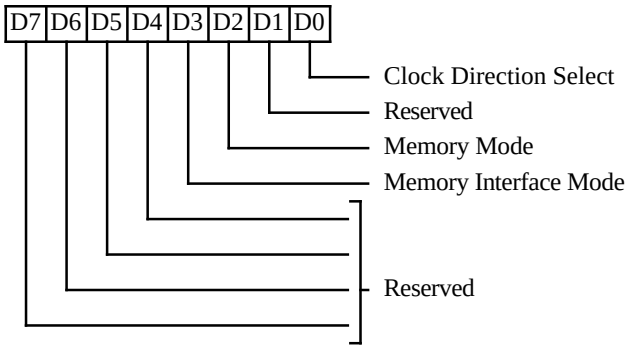
82C456A Pin List

Pin Name	Pin #
ACDCLK (M)	17
A16	40
A17	39
A18	38
AA0	143
AA1	4
AA2	8
AA3	13
AA4	21
AA5	25
AA6	29
AA7	33
AD0	58
AD1	57
AD10	46
AD11	45
AD12	44
AD13	43
AD14	42
AD15	41
AD2	53
AD3	52
AD4	51
AD5	50
AD6	49
AD7	56
AD8	48
AD9	47
ADDHI	37
ADREN/	61
AEN	65
BA0	141
BA1	2
BA2	6
BA3	11
BA4	15
BA5	23
BA6	27
BA7	31
BHE/	66
BLANK/ (DE)	103
CAS/ (WE/)	139
CLK0	110
CLK1	109
CLK2	108
ERMEN/	140
FPV0	84
FPV1	85
FPV2	86
FPV3	87
FPV4	88
FPV5	89
GND	9
GND	19
GND	35
GND	55
GND	74
GND	91
GND	102
GND	117
GND	127
GND	138
HSYNC (LP)	104
IOCS16/	70
IORD/	62
IOWR/	71
IRQ	113
L0	79
L1	80
L2	81
L3	82
M0D0	142
M0D1	3
M0D2	7
M0D3	12
M0D4	16
M0D5	24
M0D6	28
M0D7	32
M1D0	144
M1D1	5
M1D2	10
M1D3	14
M1D4	22
M1D5	26
M1D6	30
M1D7	34
M2D0	115
M2D1	118
M2D2	120
M2D3	122
M2D4	124
M2D5	128
M2D6	130
M2D7	132
M3D0	116
M3D1	119
M3D2	121
M3D3	123
M3D4	125
M3D5	129
M3D6	131
M3D7	133
MEMR/	64
MEMW/	63
MEN16/	69
P0	93
P1	94
P2	95
P3	96
P4	97
P5	99
P6	100
P7	101
PALRD/	107
PALWR/	106
PCLK	98
PWRDN2	36
RAS/	20
RDHI/	59
RDLO/	60
RDY	67
RESET	114
RFSH/	72
ROMCS	68
SHFCLK	83
SENSE	111
TRAP/	112
U0	75
U1	76
U2	77
U3	78
VCC	1
VCC	18
VCC	54
VCC	73
VCC	90
VCC	126
VSYNC (FLM)	105
WE0/ (CAS0/)	134
WE1/ (CAS1/)	135
WE2/ (CAS2/)	136
WE3/ (CAS3/)	137
WGTCLK (MCLK)	92

82C456A Extension Registers

The following pages describe the extended register bit definitions which are different for the 82C456A from the 82C456. The text in bold letters highlights the new bit definitions for the 82C456A.

MEMORY MODE REGISTER (XR04)
Read/Write at I/O Address 3B7h/3D7h
Index 04h



0 Clock Direction Select

0 CLK [2:0] are all inputs
1 CLK1 and CLK2 are general purpose outputs controlled by MISC output register bits 2 and 3. Pin 92 serves as the MCLK input. CLK0 is the dot clock input.

This bit may be set for compatibility with certain clock synthesizer chips (Note that use of the CHIPS 82C401 chip does not require setting this bit).

1 Reserved (0)

2 Memory Mode

0 Select VGA compatible memory mode (default on reset).

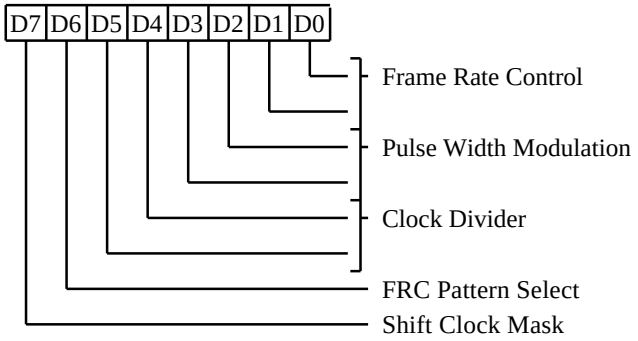
1 Select extended "Quad Mode". In this mode, display memory is mapped to the CPU address space as 4 pages of 64 Kbytes each (or 2 pages of 128 Kbytes each). The paging is controlled through the CPU Paging register (XR0B).

3 Memory Interface Mode

0 64K x 4 memory configuration
1 64K x 16 memory configuration

7-4 Reserved (0)

PANEL FORMAT REGISTER (XR50)
Read/Write at I/O Address 3B7h/3D7h
Index 50h



This register is effective only in flat panel mode as defined in bits 2-3 of XR51.

1-0 Frame Rate Control (FRC). These bits specify the gray levels simulated by the 82C456A on a frame by frame basis. This technique is used on flat panels that do not support gray levels internally, such as LCD panels.

00 No grayscale simulated for monochrome, 8 colors for color displays.

01 4 levels simulated for color panels only. (64 colors are displayed.)

10 64 gray levels simulated for monochrome panels only.

11 Reserved.

3-2 Pulse Width Modulation (PWM). This technique is used on flat panels that support internal gray levels such as most plasma panels.

00 No gray levels.

01 4 levels of colors supported by the panel. Effective only with color panels. (64 colors are displayed.)

10 16 gray levels supported by the panel. Effective with monochrome panels only.

11 Reserved (0)

5-4 Clock Divide (CD). These bits specify the frequency ratio between the dot clock (CLK0, CLK1, CLK2) and the SHFCLK signal.

00 Shift clock frequency = dot clock frequency. This setting is used to output one pixel per clock with flat panel displays.

01 Shift clock frequency = dot clock frequency/2. This setting is used to output two pixels per clock with flat panel displays.

10 Shift clock frequency = dot clock frequency/4. This setting is used to output four pixels per clock with flat panel displays.

11 Shift clock frequency = dot clock frequency/8. This setting is used to output eight pixels per clock with flat panel displays.

6 FRC Control Bit

0 31 x 15 FRC Matrix Size
1 32 x 16 FRC Matrix Size

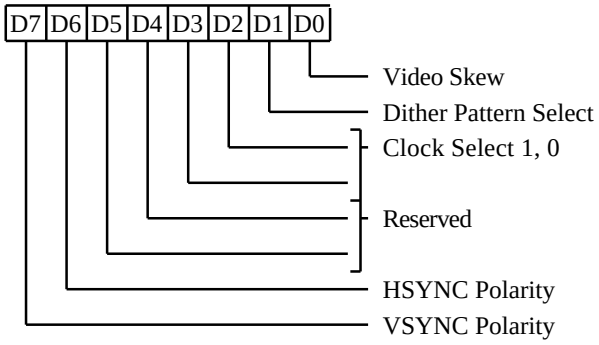
It is recommended that this bit be set to '1'.

7 Shift Clock Mask (SM).

0 Enable the SHIFT CLOCK to toggle outside the Display Enable interval.

1 Cause the Shift Clock to stop (low) outside the Display Enable interval.

ALTERNATE MISCELLANEOUS OUTPUT REGISTER (XR54)
Read/Write at I/O Address 3B7h/3D7h
Index 54h



This register is used in Flat Panel modes.

0 Panel Video Skew

0 No Panel Video data delay
1 Video data delayed 1 clock cycle

1 **FRC Pattern Select**

0 Select Pattern A
1 Select Pattern B

It is recommended that this bit be set to '1'.

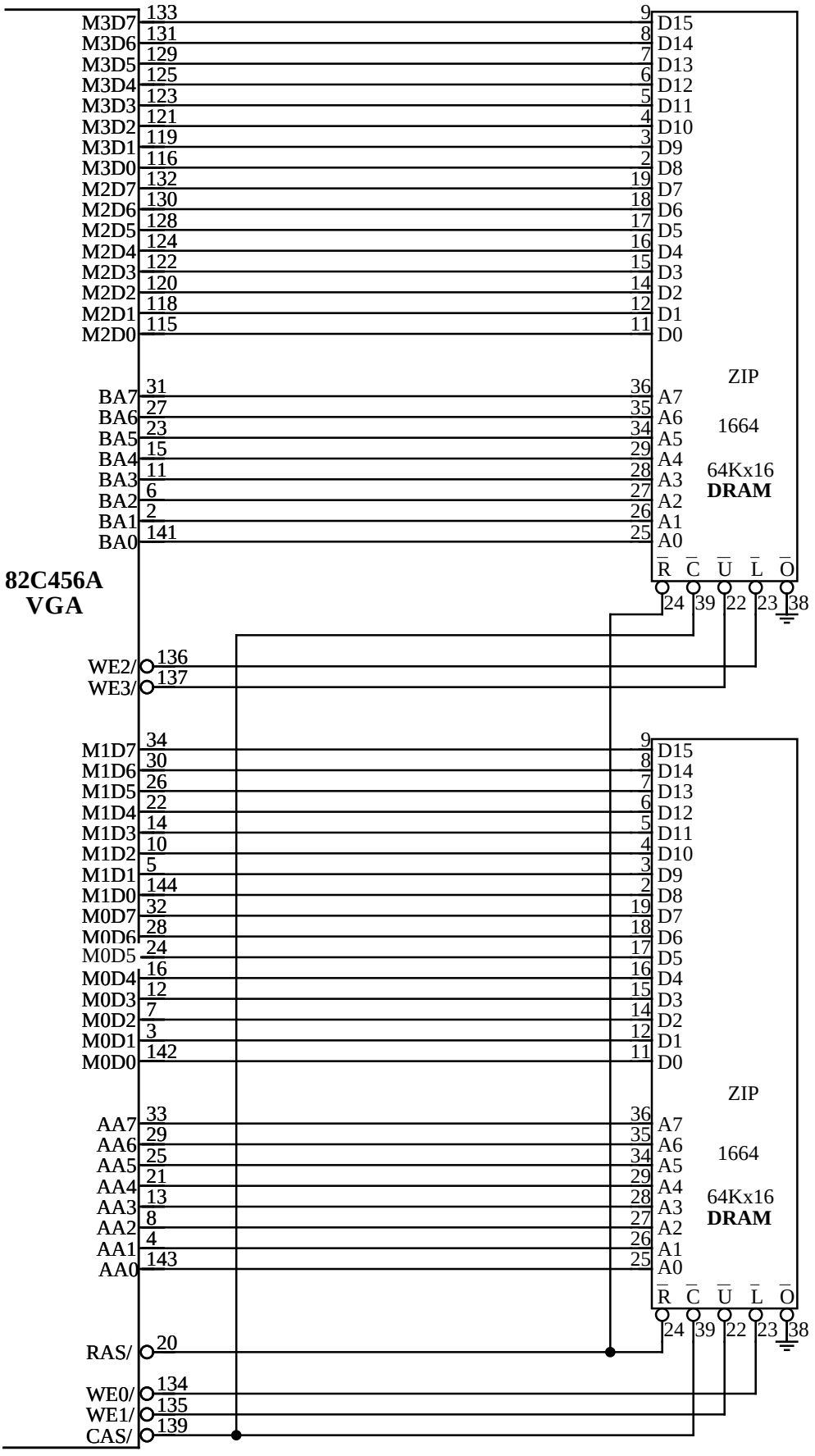
3-2 Clock Select Bits. These bits select the flat panel dot clock source as follows:

00 Select CLK0
01 Select CLK1
10 Select CLK2
11 Reserved

5-4 Reserved (0)

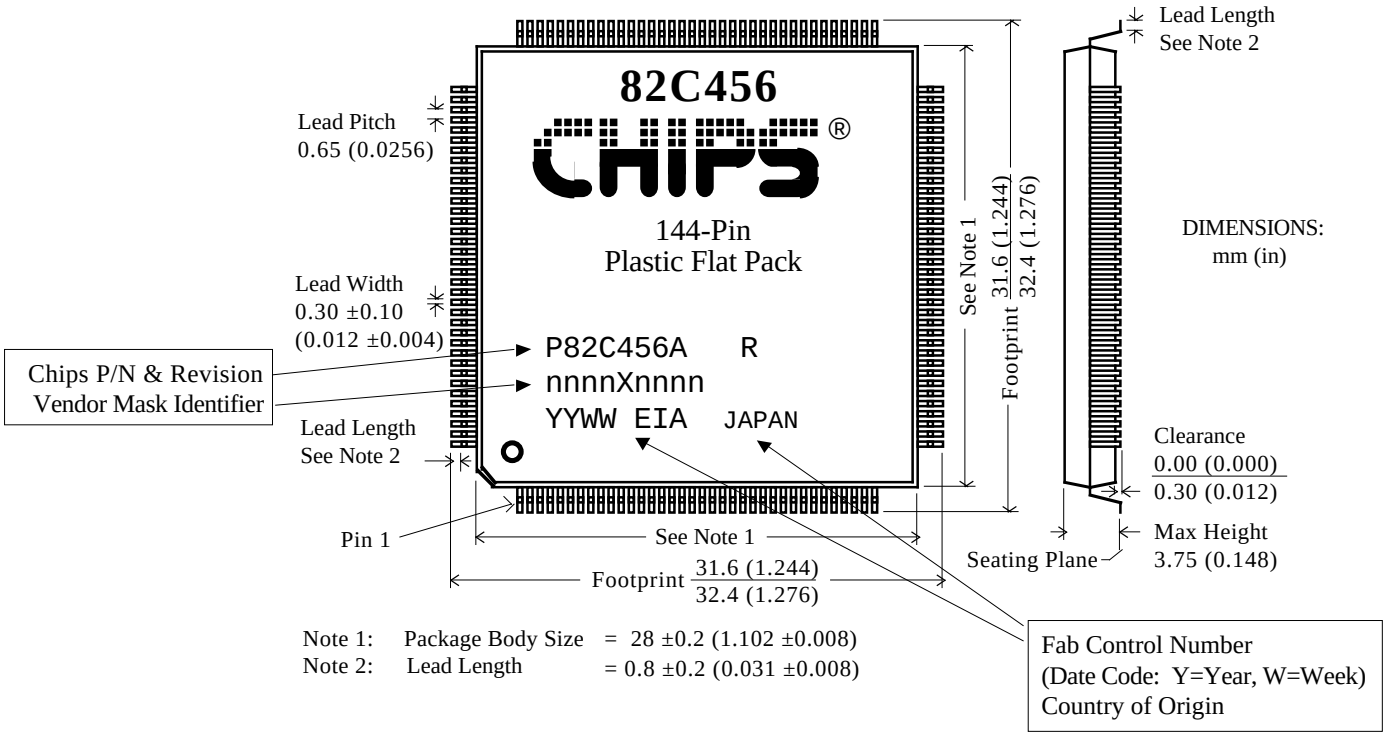
6 Hsync Polarity (0 = pos, 1 = neg)
7 Vsync Polarity (0 = pos, 1 = neg)

(The polarity of the Blank pin is controlled through the Video Interface Register.)



82C456A Display Memory Circuit 64Kx16 DRAMs

82C456A Mechanical Specifications



Note 1: Package Body Size = 28 ±0.2 (1.102 ±0.008)
Note 2: Lead Length = 0.8 ±0.2 (0.031 ±0.008)