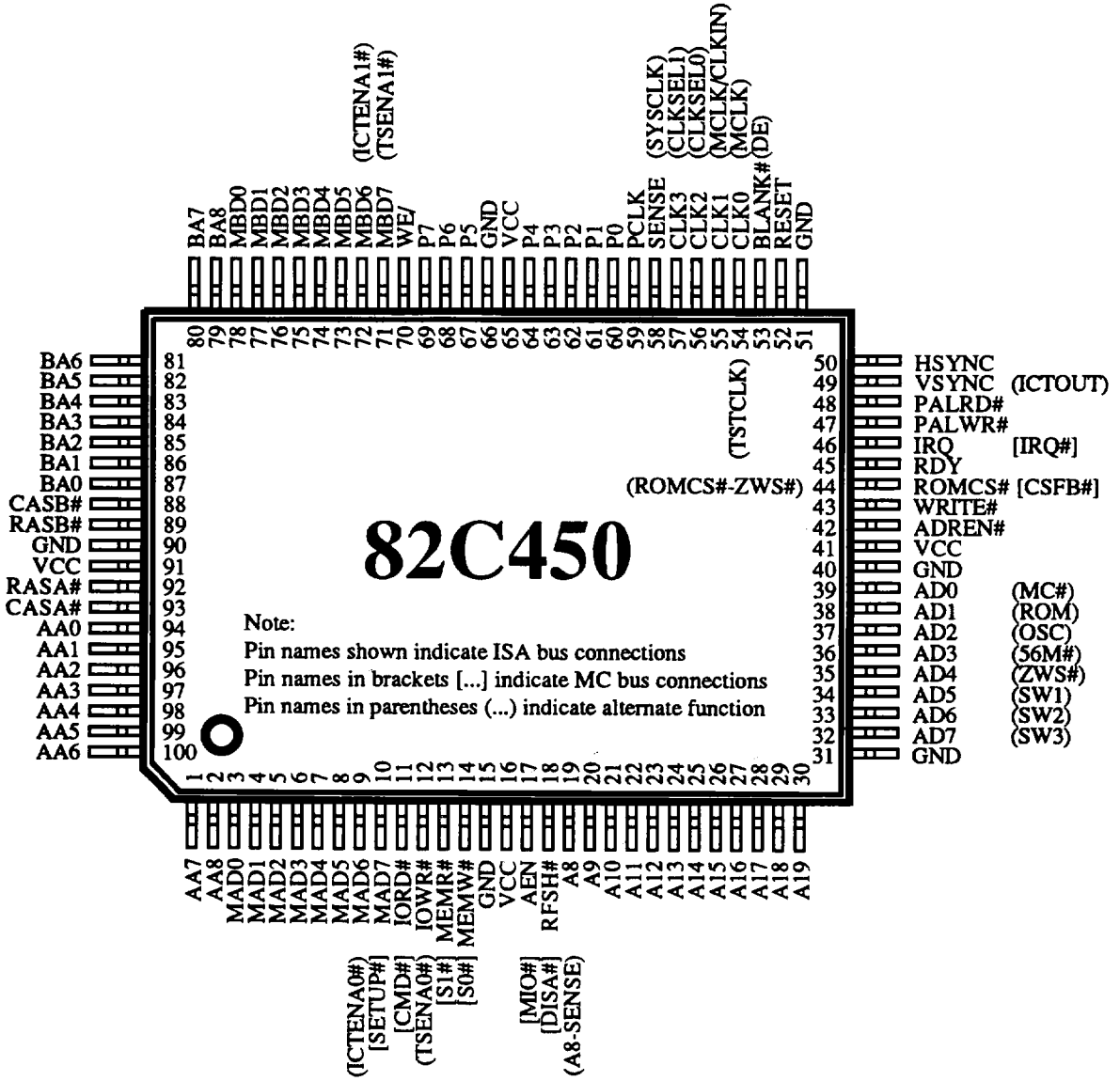
Pinouts


82C450
Note:
Pin names shown indicate ISA bus connections
Pin names in brackets [...] indicate MC bus connections
Pin names in parentheses (...) indicate alternate function
1 AA7
2 AA8
3 MAD0
4 MAD1
5 MAD2
6 MAD3
7 MAD4
8 MAD5
9 MAD6 (ICTENA0#) [SETUP#]
10 MAD7 [CMD#]
11 IORD# (TSENA0#)
12 IOWR# [S1#]
13 MEMR# [S0#]
14 MEMW#
15 GND
16 VCC
17 AEN [MIO#]
18 RFSH# [DISA#]
19 A8 (A8-SENSE)
20 A9
21 A10
22 A11
23 A12
24 A13
25 A14
26 A15
27 A16
28 A17
29 A18
30 A19
31 GND
32 AD7 (SW3)
33 AD6 (SW2)
34 AD5 (SW1)
35 AD4 (ZWS#)
36 AD3 (56M#)
37 AD2 (OSC)
38 AD1 (ROM)
39 AD0 (MC#)
40 GND
41 VCC
42 ADREN#
43 WRITE#
44 ROMCS# [CSFB#]
45 RDY
46 IRQ [IRQ#]
47 PALWR#
48 PALRD#
49 VSYNC (ICTOUT)
50 HSYNC
51 GND
52 RESET
53 BLANK# (DE)
54 CLK0 (MCLK)
55 CLK1 (MCLK/CLKIN)
56 CLK2 (CLKSEL0)
57 CLK3 (CLKSEL1)
58 SENSE (SYSCLK)
59 PCLK
60 P0
61 P1
62 P2
63 P3
64 P4
65 VCC
66 GND
67 P5
68 P6
69 P7
70 WE/
71 MBD7
72 MBD6 (TSENA1#)
73 MBD5 (ICTENA1#)
74 MBD4
75 MBD3
76 MBD2
77 MBD1
78 MBD0
79 BA8
80 BA7
81 BA6
82 BA5
83 BA4
84 BA3
85 BA2
86 BA1
87 BA0
88 CASB#
89 RASB#
90 GND
91 VCC
92 RASA#
93 CASA#
94 AA0
95 AA1
96 AA2
97 AA3
98 AA4
99 AA5
100 AA6
(TSTCLK)
(ROMCS#-ZWS#)

Pin List

Pin Name	Pin #
A8 (A8 - SENSE)	19
A9	20
A10	21
A11	22
A12	23
A13	24
A14	25
A15	26
A16	27
A17	28
A18	29
A19	30
AA0	94
AA1	95
AA2	96
AA3	97
AA4	98
AA5	99
AA6	100
AA7	1
AA8	2
AD0 (MC#)	39
AD1 (ROM)	38
AD2 (OSC)	37
AD3 (56M#)	36
AD4 (ZWS#)	35
AD5 (SW1)	34
AD6 (SW2)	33
AD7 (SW3)	32
ADREN#	31
AEN [MIO#]	17
BA0	87
BA1	86
BA2	85
BA3	84
BA4	83
BA5	82
BA6	81
BA7	80
BA8	79
BLANK# (DE)	53
CASA#	93
CASB#	88
CLK0 (MCLK)	54
CLK1 (MCLK/CLKIN)	55

Pin Name	Pin #
CLK2 (CLKSEL0)	56
CLK3 (CLKSEL1)	57
GND	15
GND	31
GND	40
GND	51
GND	66
GND	90
HSYNC	50
IORD# [CMD#]	11
IOWR# [SETUP#]	12
IRQ [IRQ#]	45
MAD0	3
MAD1	4
MAD2	5
MAD3	6
MAD4	7
MAD5	8
MAD6 (ICTENA0#)	9
MAD7 (TSENA0#)	10
MBD0	78
MBD1	77
MBD2	76
MBD3	75
MBD4	74
MBD5	73
MBD6 (ICTENA1#)	72
MBD7 (TSENA1#)	71
MEMR# [S1#]	13
MEMW# [S0#]	14
P0	60
P1	61
P2	62
P3	63
P4	64
P5	67
P6	68
P7	69
PALRD#	48
PALWR#	47
PCLK	59
RASA#	92
RASB#	89

Pin Name	Pin #
RDY	45
RESET	52
RFSH# [DISA#]	18
ROMCS# [CSFB#]	44
ROMCS# (ROMCS#-ZWS#)	44
SENSE (SYSCLK)	58
VCC	16
VCC	41
VCC	65
VCC	91
VSYNC	49
WE#	70
WRITE#	43

(56M#) See AD3
(A8 - SENSE) See AD0
(CLKSEL0) See CLK2
(CLKSEL1) See CLK3
(DE) See BLANK#
(ICTENA0#) See MAD6
(ICTENA1#) See MBD6
(MC#) See AD0
(MCLK) See CLK0
(MCLK/CLKIN) See CLK1
(OSC) See AD2
(ROM) See AD1
(ROMCS#-ZWS#) See ROMCS#
(SW1) See AD5
(SW2) See AD6
(SW3) See AD7
(SYSCLK) See SENSE
(TSENA0#) See MAD7
(TSENA1#) See MBD7
(ZWS#) See AD4

[MIO#] See AEN
[CMD#] See IORD#
[SETUP#] See IOWR#
[S1#] See MEMR#
[S0#] See MEMW#
[DISA#] See RFSH#
[CSFB#] See ROMCS#
[IRQ#] See IRQ

PIN DESCRIPTIONS

System Bus Interface

Pin #	Pin Name		Type	Active	Description
30	A19		In	High	System Upper Address Bus
29	A18		In	High	
28	A17		In	High	
27	A16		In	High	
26	A15		In	High	
25	A14		In	High	
24	A13		In	High	
23	A12		In	High	
22	A11		In	High	
21	A10		In	High	
20	A9		In	High	
19	A8	(A8 - SENSE)	In	High	A8 or A8 multiplexed with SENSE The definition of this pin changes for ZWS configuration. When CFG4 (pin 35) is high, the pin is A8. When CFG4 is low (ZWS configuration), the pin is A8 multiplexed with SENSE: when ADREN is low, the pin is A8; when ADREN is high, the pin is the SENSE input from the DAC output comparators (bit 4 of Input Status Register 0). See also extension register XR1F (Virtual Switch Register).
32	AD7	(CFG7)	I/O	High	System Address/Data Bus and Configuration Inputs. AD0-7 are sampled on the falling edge of RESET and latched into XR01. MC# determines whether the bus interface is EISA/ISA (1) or Micro Channel (0). ROM high enables decode of the BIOS ROM address space (C0000-C7FFF). OSC determines whether CLK2-3 are direct oscillator inputs (1) or outputs for a clock generator chip (0). 56M# determines whether memory timing comes from 50.350 MHz on CLK0 (1) or 56.644 MHz on CLK1 (0). ZWS# determines whether the pin definition will support the ZWS feature (0) or not (1). AD5-7 have no hardware configuration function.
33	AD6	(CFG6)	I/O	High	
34	AD5	(CFG5)	I/O	High	
35	AD4	(ZWS#)	I/O	High	
36	AD3	(MCS)	I/O	High	
37	AD2	(OSC)	I/O	High	
38	AD1	(ROM)	I/O	High	
39	AD0	(MC#)	I/O	High	
42	ADREN#		Out	Low	Address buffer enable (forced low during RESET)
43	WRITE#		Out	Low	Data transceiver direction (forced high during RESET)

ADREN#	WRITE#	Function
0	0	Normal (address input) state
0	1	Reset (AD bus undriven)
1	0	Data write to VGA chip
1	1	Data read from VGA chip

Note: Pin names in brackets [...] indicate Micro Channel bus functionality if different from EISA/ISA (PC/AT)

PIN DESCRIPTIONS **System Bus Interface (continued)**

Pin #	Pin Name		Type	Active	Description
44	ROMCS#	[CSFB#] (ROMCS# - ZWS#)	Out	Low	ROM Chip Select or ROM Chip Select multiplexed with ZWS# (EISA/ISA bus) or Card Select Feedback (Micro Channel bus). The definition of this pin changes for ZWS configurations. When CFG4 is high, the pin is ROMCS#. When CFG4 is low (ZWS configuration), the pin is ROM Chip Select multiplexed with ZWS#. The BIOS ROM is qualified with both ROMCS# and MEMR# and will therefore only be enabled for memory reads. The bus ZWS# signal should be qualified with the 82C450 ZWS# and MEMW# so that it is only asserted for memory writes.
58	SENSE	(SYSCLK)	In	Both	System Clock or Sense. The definition of this pin changes for ZWS configuration. When CFG4 is high, the pin is the SENSE input from the DAC output comparators (bit 4 of Input Status Register 0). When CFG4 is low (ZWS configuration), the pin is SYSCLK. SYSCLK is used to synchronize the output of the ZWS# signal.
45	RDY		Out	High	Ready. Driven low to indicate that current cycle should be extended with wait states. Driven high at end of cycle to indicate 'ready' then 3-stated.
46	IRQ	[IRQ#]	Out	Both	Frame Interrupt Output. Interrupt polarity is programmable. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller. (EISA/ISA-Bus interrupts are active high, Micro Channel bus interrupts are active low). See also XR14 bit–7.
52	RESET		In	High	Reset. Connect directly to the bus reset signal.

Note: Pin names in brackets [...] indicate Micro Channel bus functionality if different from EISA/ISA (PC/AT)

PIN DESCRIPTIONS

System Bus Interface (continued)

Pin #	Pin Name		Type	Active	Description
17	AEN	[MIO#]	In	Both	In EISA/ISA interface, defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (latched internally). In Micro Channel interface, indicates memory or I/O cycle: 1 = memory, 0 = I/O.
18	RFSH#	[DISA#]	In	Low	This pin is an active low signal indicating Refresh cycle. When this pin is low, the memory is not accessible.
11	IORD#	[CMD#]	In	Low	In EISA/ISA interface, indicates I/O Read Cycle. In Micro Channel interface, indicates beginning of a command part of a bus cycle. Driven off CMD# on Micro Channel, VGACMD# on CHIPS/250.
12	IOWR#	[SETUP#]	In	Low	In EISA/ISA interface, indicates I/O Write Cycle. In Micro Channel interface, indicates that the configuration register at 100-107 should be enabled. All other memory and I/O functions are disabled.
13	MEMR#	[S1#]	In	Low	In EISA/ISA interface, indicates Memory Read cycle. In Micro Channel interface, indicates Status 1.
14	MEMW#	[S0#]	In	Low	In EISA/ISA interface, indicates Memory Write cycle. In Micro Channel interface, indicates Status 0. S1# S0# Operation 0 0 Undefined 0 1 Read 1 0 Write 1 1 Undefined
48	PALRD#		Out	Low	Connected to the Read input of the Palette DAC (G176, BT471, or compatible). Asserted when the 82C450 is enabled and an I/O Read occurs from addresses 3C6h, 3C8h, or 3C9h. (The 82C450 responds directly for accesses to 3C7h).
47	PALWR#		Out	Low	Connected to the Write input of the Palette DAC (G176, BT471, or compatible). Asserted when the 82C450 is enabled and an I/O Write occurs to addresses 3C6-3C9h.

Note: Pin names in brackets [...] indicate Micro Channel bus functionality if different from EISA/ISA (PC/AT)

PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name		Type	Active	Description
2	AA8		Out	High	DRAM address bus for planes 0-1
1	AA7		Out	High	
100	AA6		Out	High	
99	AA5		Out	High	
98	AA4		Out	High	
97	AA3		Out	High	
96	AA2		Out	High	
95	AA1		Out	High	
94	AA0		Out	High	
79	BA8		Out	High	DRAM address bus for planes 2-3
80	BA7		Out	High	
81	BA6		Out	High	
82	BA5		Out	High	
83	BA4		Out	High	
84	BA3		Out	High	
85	BA2		Out	High	
86	BA1		Out	High	
87	BA0		Out	High	
10	MAD7	(TSENA0#)	I/O	High	DRAM data bus for planes 0-1 (MAD4-7 are not connected in 2-DRAM configurations). See note below for TSENA0# and ICTENA0#.
9	MAD6	(ICTENA0#)	I/O	High	
8	MAD5		I/O	High	
7	MAD4		I/O	High	
6	MAD3		I/O	High	
5	MAD2		I/O	High	
4	MAD1		I/O	High	
3	MAD0		I/O	High	
71	MBD7	(TSENA1#)	I/O	High	DRAM data bus for planes 2-3 (MBD4-7 are not connected in 2-DRAM configurations). See note below for TSENA1# and ICTENA1#.
72	MBD6	(ICTENA1#)	I/O	High	
73	MBD5		I/O	High	
74	MBD4		I/O	High	
75	MBD3		I/O	High	
76	MBD2		I/O	High	
77	MBD1		I/O	High	
78	MBD0		I/O	High	
70	WE#		Out	Low	Write enable for all memory banks/planes
92	RASA#		Out	Low	Row address strobe for memory planes 0-1
89	RASB#		Out	Low	Row address strobe for memory planes 2-3
93	CASA#		Out	Low	Column address strobe for memory planes 0-1
88	CASB#		Out	Low	Column address strobe for memory planes 2-3

If ICTENA0# and ICTENA1# are low with RESET high,a rising edge on CLK0 will put the chip into 'In Circuit Test' mode. See Functional Description. If TSENA0# and TSENA1# are low with RESET high, arising edge on CLK0 will 3-state all pins. A CLK0 rising edge without the enabling conditions exits 3-state.

PIN DESCRIPTIONS

Video Interface

Pin #	Pin Name		Type	Active	Description
69	P7		Out	High	8-bit video output
68	P6		Out	High	
67	P5		Out	High	
64	P4		Out	High	
63	P3		Out	High	
62	P2		Out	High	
61	P1		Out	High	
60	P0		Out	High	
59	PCLK		Out	High	Video Pixel Clock. Video data is synchronized to this clock.
50	HSYNC		Out	Both	Horizontal sync for CRT (polarity is programmable)
49	VSYNC		Out	Both	Vertical sync for CRT (polarity is programmable)
53	BLANK#	(DE)	Out	Both	Blanking signal for external palette DAC (polarity is programmable: see XR28 bit-0). May also be redefined as Display Enable (see XR28 bit-1).

PIN DESCRIPTIONS

Clock, Power, and Ground

Pin #	Pin Name		Type	Active	Description
54	CLK0	(MCLK)	In	High	If internal clock selection is enabled (default), CLK0, CLK1, CLK2, and CLK3 are inputs. One of the four is selected as the input dotclock per Misc Output Register (3C2h) bits 2 and 3. Memory clock may be selected from either CLK0 or CLK1 (see pin AD3 and configuration register XR01); if CLK0 is selected as MCLK, 50.35 MHz is used (CLK1 is 28.322); if CLK1 is selected as MCLK, 56.644 MHz is used (CLK0 is 25.175). If external clock selection is enabled (see pin AD2 and configuration register XR01), CLKIN becomes the input dotclock for all pixel clock frequencies and CLK2-3 become clock select outputs driven by Misc Output Register (3C2h) bits 2 and 3. In this mode, the CLK0 pin is always used for memory timing (MCLK).
55	CLK1	(MCLK/CLKIN)	In	High	
56	CLK2	(CLKSEL0)	I/O	High	
57	CLK3	(CLKSEL1)	I/O	High	
16	VCC		VCC	--	Power
41	VCC		VCC	--	
65	VCC		VCC	--	
91	VCC		VCC	--	
15	GND		GND	--	Ground
31	GND		GND	--	
40	GND		GND	--	
51	GND		GND	--	
66	GND		GND	--	
90	GND		GND	--	