82C426
CGA LCD/CRT CONTROLLER

- **Single chip 100% IBM CGA compatible LCD/CRT controller**
- **Very low power 100 pin CMOS device**
- **Supports all CGA modes**
- **Sleep Mode**
- **Built-in CPU Interface**
- **Supports AT&T 400-Line Graphics Mode**
- **Ideal for laptop computers**
- **A CGA controller can be implemented using only three chips including display memory**
- **Drives multiple monochrome and color panel types**
- **Supports two fonts**
- **Intelligent memory arbitration**

The 82C426 CGA LCD(Liquid Crystal Display)/CRT controller is a display controller for flat panel displays and CRT monitors. It is ideal for portable and laptop class IBM-compatible computers. The device is designed to drive the following types of panels:

- Single panel, single drive 4-bit parallel
- Dual panel, single drive 4-bit parallel
- Dual panel, dual drive 2x4-bit parallel
- Single panel, single drive 4x3-bit color
- Single panel, single drive 1x4-bit color

The 82C426 also supports CGA compatible CRTs. The device is fully compatible with applications designed for the IBM Color Graphics Adapter.

Figure 1 depicts a graphic subsystem using the 82C426.

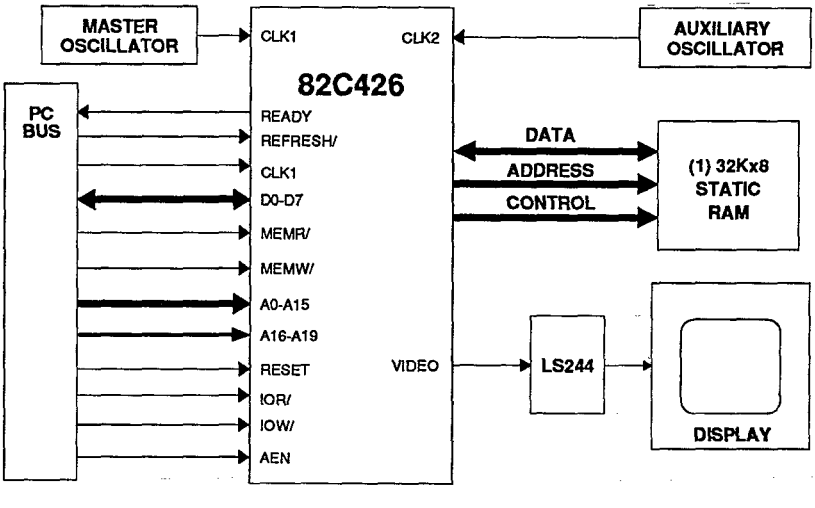
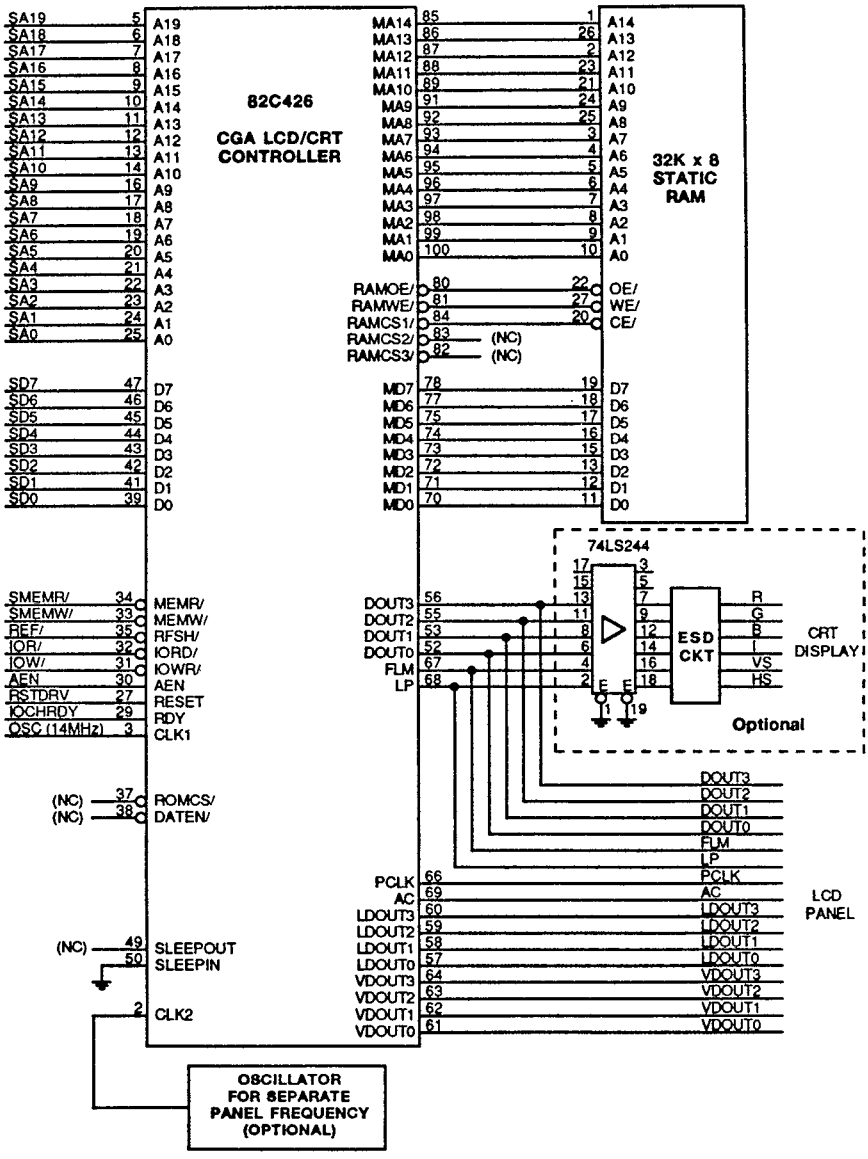
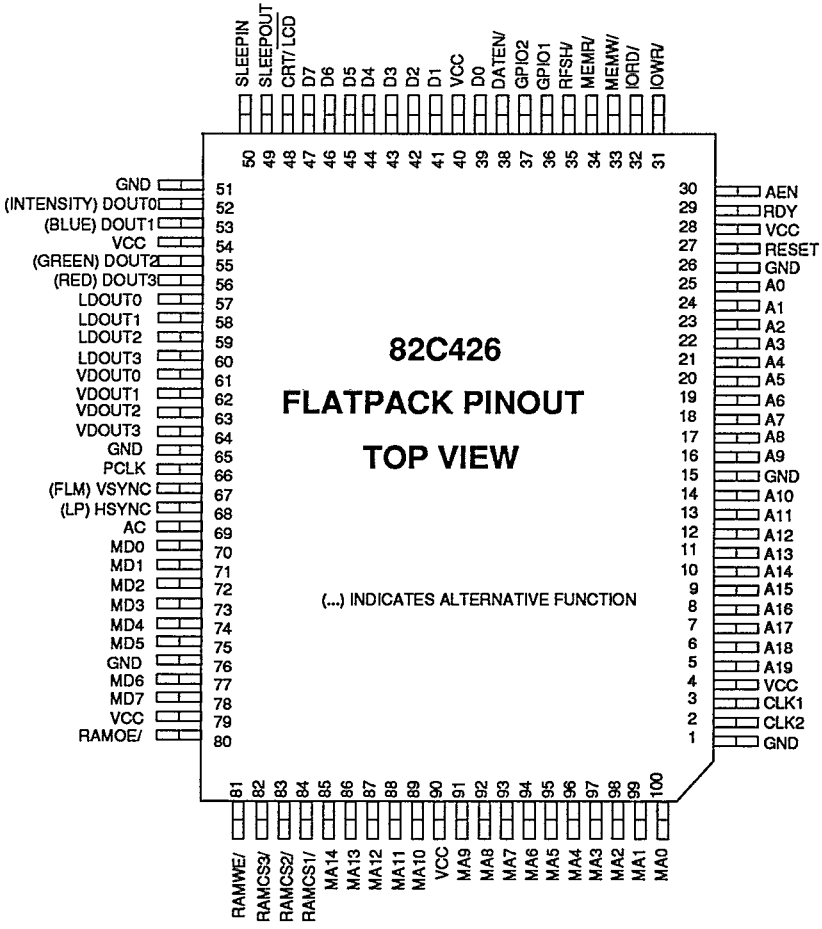


Figure 1: 82C426 Typical System Block Diagram

Table of Contents



82C426 MINIMUM SYSTEM SCHEMATIC


82C426
FLATPACK PINOUT
TOP VIEW
(...) INDICATES ALTERNATIVE FUNCTION
1 GND
2 CLK2
3 CLK1
4 VCC
5 A19
6 A18
7 A17
8 A16
9 A15
10 A14
11 A13
12 A12
13 A11
14 A10
15 GND
16 A9
17 A8
18 A7
19 A6
20 A5
21 A4
22 A3
23 A2
24 A1
25 A0
26 GND
27 RESET
28 VCC
29 RDY
30 AEN
31 IOWR/
32 IORD/
33 MEMW/
34 MEMR/
35 RFSH/
36 GPIO1
37 GPIO2
38 DATEN/
39 D0
40 VCC
41 D1
42 D2
43 D3
44 D4
45 D5
46 D6
47 D7
48 CRT/ LCD
49 SLEEPOUT
50 SLEEPIN
51 GND
52 (INTENSITY) DOUT0
53 (BLUE) DOUT1
54 VCC
55 (GREEN) DOUT2
56 (RED) DOUT3
57 LDOUT0
58 LDOUT1
59 LDOUT2
60 LDOUT3
61 VDOUT0
62 VDOUT1
63 VDOUT2
64 VDOUT3
65 GND
66 PCLK
67 (FLM) VSYNC
68 (LP) HSYNC
69 AC
70 MD0
71 MD1
72 MD2
73 MD3
74 MD4
75 MD5
76 GND
77 MD6
78 MD7
79 VCC
80 RAMOE/
81 RAMWE/
82 RAMCS3/
83 RAMCS2/
84 RAMCS1/
85 MA14
86 MA13
87 MA12
88 MA11
89 MA10
90 VCC
91 MA9
92 MA8
93 MA7
94 MA6
95 MA5
96 MA4
97 MA3
98 MA2
99 MA1
100 MA0

PIN DIAGRAM

82C426 PIN DESCRIPTION

Flatpack Pin No.	Name	Type	Active	Description
25	A0	In	High	Host computer system Address Bus.
24	A1	In	High	
23	A2	In	High	
22	A3	In	High	
21	A4	In	High	
20	A5	In	High	
19	A6	In	High	
18	A7	In	High	
17	A8	In	High	
16	A9	In	High	
14	A10	In	High	
13	A11	In	High	
12	A12	In	High	
11	A13	In	High	
10	A14	In	High	
9	A15	In	High	
8	A16	In	High	
7	A17	In	High	
6	A18	In	High	
5	A19	In	High	
39	D0	I/O	High	Host computer system Data Bus.
41	D1	I/O	High	
42	D2	I/O	High	
43	D3	I/O	High	
44	D4	I/O	High	
45	D5	I/O	High	
46	D6	I/O	High	
47	D7	I/O	High	
30	AEN	In	High	Address Enable. A high level indicates that a DMA operation is in progress. When low, the host CPU has control of address and command lines.
33	MEMW/	In	Low	Memory Write. This input must be low when the CPU writes to display/font memory.
34	MEMR/	In	Low	Memory Read. This input must be low when the CPU reads display/font memory.

Flatpack Pin No.	Name	Type	Active	Description
31	IOWR/	In	Low	I/O Write. This input must be low when the CPU writes 82C426 internal registers.
32	IORD/	In	Low	I/O Read. This input must be low when the CPU reads 82C426 internal registers.
29	RDY	Out	High	This normally-high pin (READY) is pulled low (not READY) when the 82C426 needs to extend the current CPU bus cycle. Upon completion of this bus cycle, the 82C426 drives this output high for one dot clock. When not active, this pin is 3-stated.
35	RFSH/	In	Low	System Memory Refresh. High for non-refresh cycles.
27	RESET	In	High	Reset signal. Reset must be active for a minimum of 4 input clock cycles (4Tc).
3	CLK1	In		Master Clock Input.
2	CLK2	In		Auxiliary Clock Input.
70	MD0	I/O		Display and font RAM Data Bus.
71	MD1	I/O		
72	MD2	I/O		
73	MD3	I/O		
74	MD4	I/O		
75	MD5	I/O		
77	MD6	I/O		
78	MD7	I/O		
100	MA0	Out		Display and font RAM Address Bus.
99	MA1	Out		
98	MA2	Out		
97	MA3	Out		
96	MA4	Out		
95	MA5	Out		
94	MA6	Out		
93	MA7	Out		
92	MA8	Out		
91	MA9	Out		
89	MA10	Out		
88	MA11	Out		
87	MA12	Out		
86	MA13	Out		
85	MA14	Out		

Flatpack Pin No.	Name	Type	Active	Description
84	RAMCS1/	Out	Low	Chip Select for Display RAM 1.
83	RAMCS2/	Out	Low	Chip Select for Display RAM 2.
82	RAMCS3/	Out	Low	Chip Select for Font RAM.
81	RAMWE/	Out	Low	Display and font RAM Write Enable.
80	RAMOE/	Out	Low	Display and font RAM Output Enable.
38	DATEN/	Out	Low	Indicates a valid access to Memory or I/O address space, excluding the ROM address space.
68	HSYNC or LP	Out	High	Hsync for CRT display. Latch Pulse (LP) for LCD display.
67	VSYNC or FLM	Out	High	Vsync for CRT/First Line Marker (FLM) for LCD.
69	AC	Out	High	LCD cell bias polarity.
66	PCLK	Out	High	Pixel Clock Output.
52	DOUT0 or INTENSITY	Out	High	Intensity signal for CRT/ Bit D0 of LCD Monochrome Data (Upper Panel in Dual-Panel Systems)/ Bit D0 of the Red Interface in 12-bit Color LCD Systems/ Unused in 3-bit Color LCD Systems.
53	DOUT1 or BLUE	Out	High	Blue signal for CRT/ D1 of LCD Monochrome Data (Upper Panel in Dual-Panel Systems)/ Bit D1 of the Red Interface in 12-bit Color LCD Systems/ Blue signal for 3-bit Color LCD Systems.
55	DOUT2 or GREEN	Out	High	Green signal for CRT/ D2 of LCD Monochrome Data (Upper Panel in Dual-Panel Systems)/ Bit D2 of the Red Interface in 12-bit Color LCD Systems/ Green signal for 3-bit Color LCD Systems.
56	DOUT3 or RED	Out	High	Red signal for CRT/ D3 of LCD Monochrome Data (Upper Panel in Dual-Panel Systems)/ Bit D3 of the Red Interface in 12-bit Color LCD Systems/ Red signal for 3-bit Color LCD Systems.

Flatpack Pin No.	Name	Type	Active	Description
57	LDOUT0	Out	High	Lower Panel Display Interface for Dual LCD Panels/Green Interface for Color LCD Panels/Unused in CRT and 3-bit LCD Systems.
58	LDOUT1	Out	High	
59	LDOUT2	Out	High	
60	LDOUT3	Out	High	
61	VDOUT0	Out	High	Blue Display Interface for Color LCD Panels/Unused in CRT and Monochrome LCD Systems.
62	VDOUT1	Out	High	
63	VDOUT2	Out	High	
64	VDOUT3	Out	High	
50	SLEEPIN	In	High	Sleep Input. High level invokes sleep mode.
49	SLEEPOUT	Out	High	Sleep Output. Indicates, when high, that the controller is in the sleep state.
36	GPIO1	I/O	High	General-Purpose I/O 1. This pin reflects the value of bit D0 of Register RD5, or the state of Display Enable, or may be configured as a software-readable input.
37	GPIO2	I/O	High	General-Purpose I/O 2. This pin reflects the value of bit D4 of Register RD5, or the state of ROMCS/, or may be configured as a software-readable input. ROMCS/ is low on a valid memory read of any address in the C0000:C7FFFh range.
48	CRT/$\overline{\text{LCD}}$	Out	Both	The CRT/$\overline{\text{LCD}}$ output is used to select the current display type. This pin reflects the state of bit D3 of register RDF. It is high for CRT mode, low for LCD mode.
4	VCC	+5V		Power Pins.
28	VCC			
40	VCC			
54	VCC			
79	VCC			
90	VCC			
1	GND	GND		Ground.
15	GND			
26	GND			
51	GND			
65	GND			
76	GND			

FUNCTIONAL DESCRIPTION

Operating Modes

The 82C426 supports all CGA modes: 80 by 25 character text, 40 by 25 character text, 640 by 200 two color graphics and 320 by 200 four color graphics. 640 by 400 two color graphics and 320 by 400 four color graphics modes (AT&T mode) are also supported for 400-line panels. The mode is selected by writing to the control registers. CGA compatible registers are used to invoke the CGA modes; extension registers control the additional modes. The display buffer memory begins at address B8000h for all modes; its length depends on the RAM configuration chosen. The 82C426 is an extension of the 82C425 and is upward compatible with both the IBM CGA and the 82C425. Specific panel sizes are needed to maintain register-level CGA compatibility, though the controller is flexible and other sizes of panels can be driven for non-CGA compatible applications. Display size is generally limited by the range of possible register values and frame buffer memory size.

Text Modes

80 x 25 Text Mode

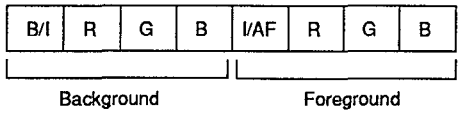
This mode is compatible with applications developed for CGA 80 column text mode. Each character on the screen is represented by two consecutive bytes in the display buffer. Bytes at even addresses contain the character code; the following odd byte contains the display attributes for that character. One screen occupies 4000 bytes of screen buffer memory. Text is normally displayed as an 8 by 8 pixel character cell, though characters as high as 16 scan lines can be displayed. Fonts are stored in and accessed from an external static RAM or ROM. Either the default system font (loaded by the BIOS during initialization) or an optional user-defined font may be used.

40 x 25 Text Mode

This mode is compatible with 40 column CGA applications. Display buffer memory has the same format as 80 column mode, though only 2000 bytes are used per screen. The same font(s) are used as with 80 column mode; each pixel is doubled in the horizontal direction to yield a character cell which is 16 pixels wide and normally 8 pixels high.

Text Mode Attribute Processing

Odd bytes in the display buffer contain the character attributes. These attributes are interpreted in the same manner for both text modes and for both CRT displays and LCD panels. The attribute byte has a foreground and background nibble:



The upper four bits define the background color of the character cell. If bit 5 of the Mode Control register (I/O Address 3D8h) is zero, then bit 7 represents the intensity bit of the background color, otherwise bit 7 controls character blink.

The lower four bits define the foreground color. If bit 6 of the Function Control register (RDF) is zero then bit 3 represents the intensity bit of the foreground color, otherwise bit 3 controls alternate font selection. I/AF can be used to select either of the two RAM-resident character sets on a character by character basis, allowing characters from both fonts to be shown on the screen simultaneously.

When driving a CRT or color panel, the 82C426 displays the colors exactly as an IBM CGA board does. For monochrome panels, the processing of the attributes is identical, but the resulting colors are translated to gray levels; translation to eight or four levels can be chosen.

The mapping technique for monochrome panels is based on weighting the R, G, B, I bits such that R is the most significant bit and I the least. Different colors can map to the same gray level because there are fewer gray levels than pos-

sible colors. To insure a minimum contrast between the foreground and background level, a second translation called SMARTMAP can be invoked by setting the extension registers.

SMARTMAP™

The SMARTMAP scheme compares and adjusts the foreground and background gray values on a character by character basis to produce adequate display contrast on monochrome LCD panels. The minimum contrast level is determined by a value programmed in the Threshold register (RDA). The contrast enhancement value used to adjust the foreground and background values is stored in the Shift Parameter register (RDB). If the adjusted values exceed the maximum allowed values, the Saturation bit (D4 in RDA) determines if the output is limited to the saturation point or allowed to wrap around. SMARTMAP is enabled by programming a non-zero value in the Threshold register (RDA).

If the Blink attribute is enabled, the background intensity bit (AT7) is taken as zero before the SMARTMAP algorithm is applied. If the Alternate Font Select Function is enabled, the foreground color intensity bit (AT3) is taken as zero before applying the SMARTMAP algorithm. Smartmap affects only text modes for monochrome LCD panels; it has no effect on graphics modes or color panels. Optimal threshold and shift parameter values depend on the particular LCD panel used.

Display Buffer and Font Storage

Display Buffer

The display buffer appears to the CPU as an array in memory, beginning at B8000h, and is used for both text and graphics. Registers RC and RD contain the offset into this area where the displayed characters or graphics data begin. This array can be 16 Kbytes to 32 Kbytes long, depending on the RAM configuration. CGA compatible modes require 16 Kbytes; extension modes can require a larger buffer.

Fonts

Fonts for the text modes are held in either RAM or ROM. Font memory is accessed by the CPU by mapping it in or out of the display buffer address space with bit 1 of the Function Control register (RDF).

Two different fonts can be stored in the font memory. Each font is a set of 256 characters, 8 dots wide and up to 16 dots high; the Maximum Scan register (R9) controls the character height. Each font requires a maximum of 4 Kbytes (16x256) of font memory. When the font area is swapped into the display buffer area (RDF, D1), the first font begins at B8000h; the second font is at B9000h. Figure 2 shows the organization of the font data. Characters are stored in as-

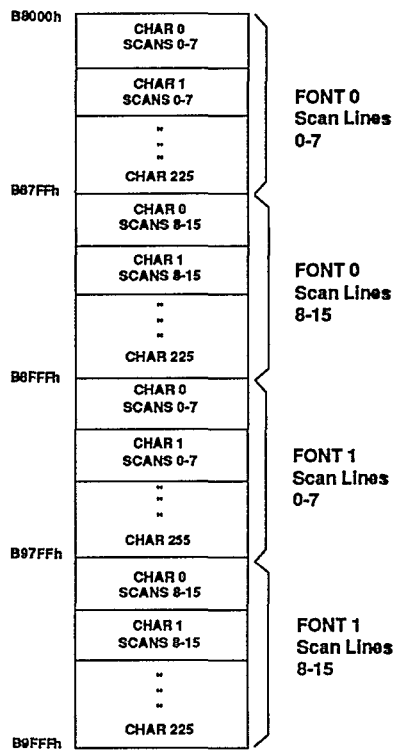


Figure 2: Font RAM Organization

cending order beginning with character code 0. Scanlines 8 through 15 (if needed) are stored at addresses 2 Kbytes above scans 0 through 7.

Font 0:

Scan Lines 0-7:

(char. code x 8) + scan line

Scan Lines 8-15:

2048 + (char. code x 8) + (scan line - 8)

Font 1:

Scan Lines 0-7:

4096 + (char. code x 8) + scan line

Scan Lines 8-15:

6144 + (char. code x 8) + (scan line - 8)

A 4K RAM or ROM can be used for applications requiring only one font or two 8 by 8 fonts by not using address line MA12. One 8 by 8 font can be stored in a single 2K memory; MA12 and MA11 are not connected in this case.

Character Blink and Cursor

Default character blink and cursor functions are identical to the IBM CGA board. The cursor can be turned off by programming the Cursor Start Scan register (RA) to a value greater than the character height. The cursor blink rate is twice that of the character blink rate; they can be altered from the default rates by bits D7-D4 of the Vertical Sync Width/Blink Control register (RDD). It is sometimes desirable to lower the character and cursor blink rate for LCD panels because the persistence of the image is longer than that of a CRT.

Text on 400-line Panels

Text can be displayed on a 400-line panel while maintaining complete CGA compatibility. A 16-line font such as the one used by the IBM EGA board is loaded at initialization. The fact that 16 line characters are being displayed is transparent to the CGA software because the standard register values are used, ensuring compatibility. The details of implementing this scheme are discussed in the description of the Panel Configuration Register (RD8).

Graphics Modes

The 82C426 supports both CGA-compatible graphics modes as well as AT&T graphics mode. CGA graphics applications software will run without modification for both CRT and LCD displays. For 400-line panels, the 200-line CGA graphics modes can be mapped onto the display by double scanning the image, maintaining complete compatibility, in addition to the true 640 by 400 AT&T graphics mode.

640 x 200 Two Color Mode

Each pixel is represented by one bit in memory. The memory organization of the pixels is shown in Figure 3 below:

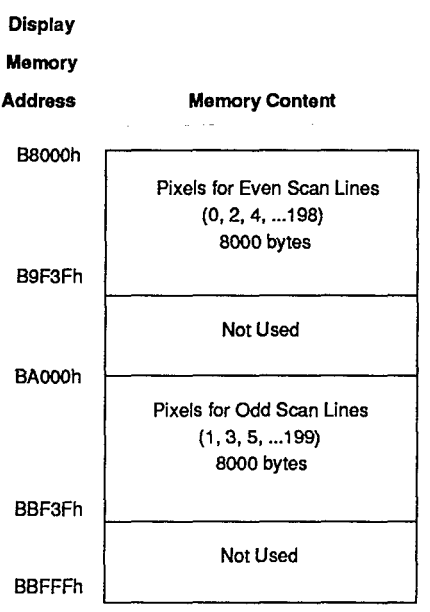
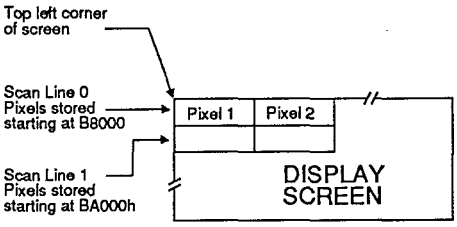


Figure 3: Memory Organization for CGA Compatible Graphics Modes

The highest order bit in a byte is displayed on the screen first as shown in Figure 4. Odd and even scan lines are stored in separate 8 Kbyte blocks of display memory. No gray level algorithm is used for LCD panels in this mode.



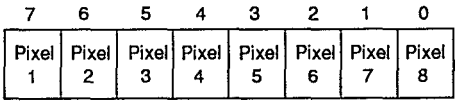


Figure 4: Pixel Storage and Display for 640 x 200 Graphics Mode

320 x 200 Four Color Graphics Mode

In this mode, each pixel is represented by two bits, C0 and C1. Figure 5 shows how they appear on the screen:

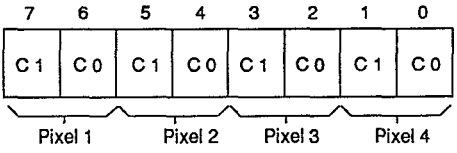


Figure 5: Pixel Storage and Display for 320 x 200 Graphics Mode

Even scan lines (0,2,4,...198) are stored starting at hex address B8000h; odd scan lines are stored starting at BA000h. Each two-bit pixel can be displayed as any one of 4 different colors.

When a CGA compatible CRT display is used, operation is identical to the IBM CGA. When an LCD panel is used, the 320 x 200 4 color (2 bits/pixel) mode is displayed on a 640 pixel panel by mapping each pixel in memory to 2 pixels on the panel. This is shown in Figure 7.

400-line (AT & T) Graphics Modes

True 400-line graphics mode can be used. It is an extension of the CGA modes. Representation of the pixel data in each byte is identical to the CGA two-color and four-color modes, though twice as much frame buffer memory is required to hold the image (32000 bytes). In these modes, the scan lines are separated into four areas instead of two, as shown in Figure 6.

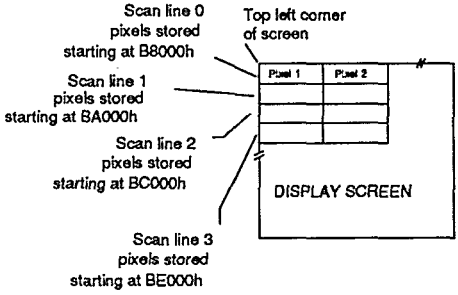


Figure 6: Memory Organization for 400-Line Graphics Modes

Memory Configurations

The 82C426 can be programmed for different memory configurations with register RD8. In standard CGA modes 16000 bytes are needed for frame buffer memory. 32000 bytes of frame buffer are needed for the true 400-line graphics

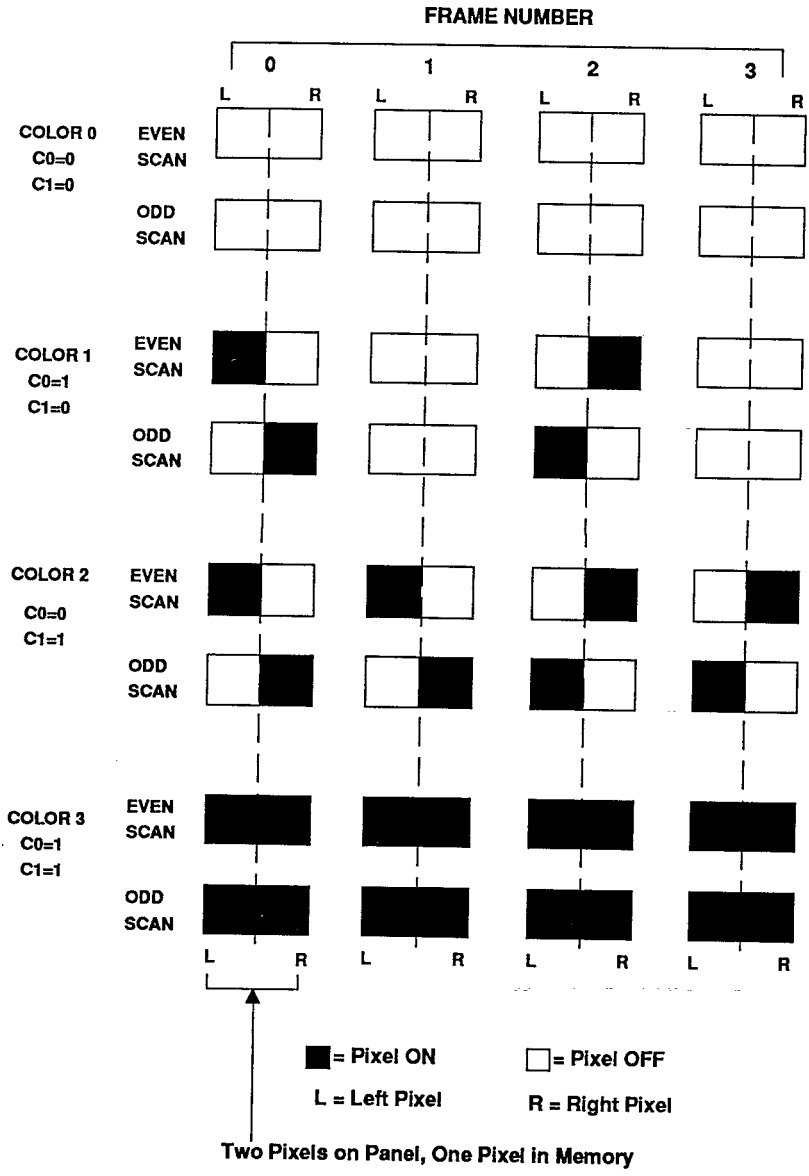


Figure 7: 320 Pixel/Line 4-Level Gray Scale Scheme Displayed on 640 Pixel/Line Panel

modes. An 8 Kbyte area is required for font storage

In the single 32K RAM configuration, the RAMCS1/ signal selects the RAM. In text mode, the upper quarter of the RAM holds the font. The lower three-quarters can be used as frame buffer. In graphics mode, the entire RAM is available as frame buffer, but the font will be overwritten if more than the first 24 Kbytes is used. This will not affect standard CGA modes since they use only 16K.

In the 32K and 8K RAM configuration, the font is contained in the 8K RAM/ROM (selected by RAMCS3/). The entire 32K RAM can be used as frame buffer and is selected by RAMCS1/.

The three-8K RAM configuration uses two RAMs for the frame buffer. RAMCS1/ selects the RAM that holds the first half of the frame buffer; RAMCS2/ selects the other. RAMCS3/ selects the font RAM/ROM.

In the 16K and 8K RAM configuration, the entire 16K RAM can be used as frame buffer and is selected by RAMCS1/. The font is contained in the 8K RAM/ROM (selected by RAMCS3/).

Frame buffer accesses are executed in two clock cycles. In text modes, three accesses are made per character time; the remaining time is available to the CPU. The ASCII character value is fetched, then the attribute value, then the font is read. In graphics modes, two bytes of graphics data are read per character time.

Displays Supported

The 82C426 supports both CGA compatible CRTs and liquid crystal displays. Only one display may be active at a time, because the timing for CRTs and LCD panels are different. The current mode is indicated by the CRT/LCD output pin. The CRT and LCD panel may require different clocks, so two clock inputs are provided (CLK1 and CLK2); bit D5 of the Timing Control register (RDE) determines which clock input is used. A programmable divider is used for generating the character and pixel clock from the selected clock input. Bits D6 and D7 of register RDE control the divider. SRAM timing is based on the clock input that is selected and is independent of the programmable divider.

CRT Displays

The 82C426 can be used with any IBM CGA compatible CRT as well as variable frequency CRTs that are compatible with CGA video signals. Four bits of video data and vertical and horizontal sync signals are supplied by the 82C426 to the CRT display; these use TTL levels.

Liquid Crystal Displays

The 82C426 supports several types of displays:

Single panel, single drive 4-bit parallel

Dual panel, single drive 4-bit parallel

Dual panel, dual drive 2 x 4-bit parallel

Single panel, single drive 4 x 3-bit color

Single panel, single drive 1 x 4-bit color

Display type mode is independent of panel resolution. Interface timing for the panels is shown in Figure 8. The FLM (first line marker) signal indicates the first line of data of each frame. Only the alternate FLM timing is shown in the figure (RD8, bit D3 = 1). When RD8 bit D3 = 0, FLM rises at least one character time before the rising edge of the LP (latch pulse) of the first line of data. It falls at least one character clock after the rising edge of LP. LP is active during the last pixel or nibble of pixels of each line. In single panel mode, the number of LPs exactly equals the number of lines displayed on the panel. DOUT3 is the left most pixel when using the 4 or 8 bit wide interfaces. PCLK is continuous; there is no horizontal or vertical blank time.

The AC signal controls the polarity of the bias of the cells in the panel, so that none of the pixel cells is subjected to a non-zero average DC bias. If such a bias exists, vertical lines (ghosting) appear and the panel may be damaged. The AC control register (RD9) determines the period of the AC clock. The value programmed in bits D0-D4 of this register should be a high, odd number since there are an even number of lines

in the panel. Each panel has a different optimal value, which can be determined experimentally.

CPU Interface

In all CGA modes, I/O addresses are mapped to the 3Dx block of CPU I/O space. Display and font buffer memory is located at B8000h-BFFFFh. The arbitration technique utilized does not limit CPU accesses to horizontal or vertical retrace periods. The 82C426 interleaves CPU accesses with screen refresh accesses, ensuring rapid CPU transfers to/from display memory without screen "snow". It uses the PC bus RDY line to add wait states to the bus cycle if a screen refresh is occurring. The CPU will typically wait for a period of one to four character clocks (depending on the speed of the CPU).

Using the 82C426 for Non-CGA Applications

The 82C426 supports a wide range of panel sizes. For completely IBM compatible applications, particular panel sizes, frame buffer organization and controller register values are required. For designs that do not require compatibility, the panel sizes supported are limited by the values to which the controller register can be programmed and the memory storage of the frame buffer. The 82C426 is also a minimal, flexible solution for CRT applications. The 82C426 can also be interfaced to other types of CPUs; in this case, AEN should be tied low and RFSH/ should be tied high.

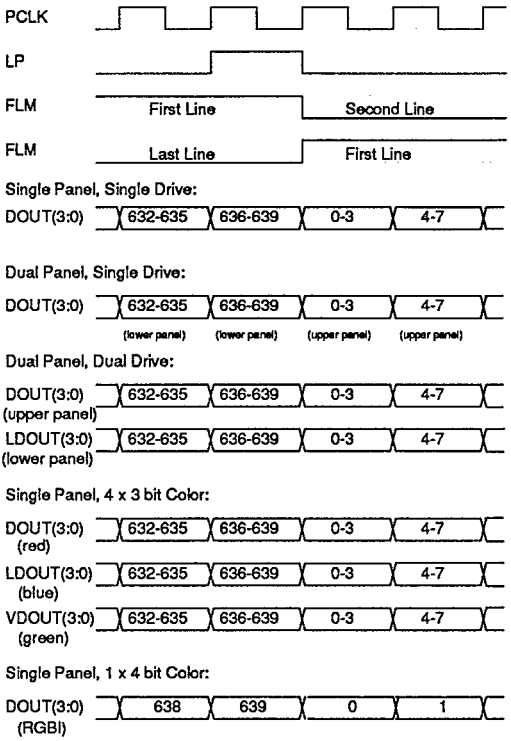


Figure 8: Timing for LCD Panels

82C426 REGISTERS

The 82C426 contains registers which define and control a raster-scan CRT display or LCD. Most of these registers are accessed with a two step process that uses two byte addresses in the CPU I/O space. First, a pointer to the desired register is written into the address register (I/O address 3D4h). Then the data register is read or written (I/O address 3D5h). Unless otherwise specified, the default contents of all registers are undefined on power-up. Registers RD3-RDF are extension registers.

Register Mnemonic	Register Name	Address Pointer	PC I/O Address
——	Address Register	—	3D4h
R0	Horizontal Total	00	3D5h
R1	Horizontal Displayed	01	3D5h
R2	Horizontal Sync Position	02	3D5h
R3	Ignored	03	3D5h
R4	Vertical Total	04	3D5h
R5	Vertical Total Adjust	05	3D5h
R6	Vertical Displayed Register	06	3D5h
R7	Vertical Sync Position	07	3D5h
R8	Ignored	08	3D5h
R9	Maximum Scans/Row	09	3D5h
RA	Cursor Start Scan	0Ah	3D5h
RB	Cursor End Scan	0Bh	3D5h
RC	Start Address High	0Ch	3D5h
RD	Start Address Low	0Dh	3D5h
RE	Cursor Address High	0Eh	3D5h
RF	Cursor Address Low	0Fh	3D5h
R10	Light Pen High	10h	3D5h
R11	Light Pen Low	11h	3D5h
RD3	Gray-level Control #1	D3h	3D5h
RD4	Gray-level Control #2	D4h	3D5h
RD5	General-Purpose	D5h	3D5h
RD6	Sleep	D6h	3D5h
RD7	Panel Size	D7h	3D5h
RD8	Panel Configuration	D8h	3D5h
RD9	AC Control	D9h	3D5h
RDA	Threshold	DAh	3D5h
RDB	Shift Parameter	DBh	3D5h
RDC	Horizontal Sync Width	DCh	3D5h
RDD	Vertical Sync Width	DDh	3D5h

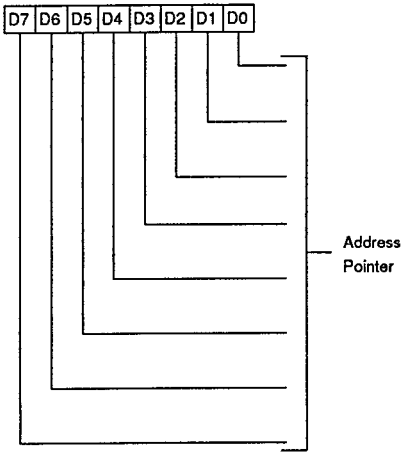
82C426 Registers
(Continued)

Register Mnemonic	Register Name	Address Pointer	PC I/O Address
RDE	Timing Control	DEh	3D5h
RDF	Function Control	DFh	3D5h
——	Mode Control	——	3D8h
——	Color Select	——	3D9h
——	Input Status	——	3DAh
——	Light Pen Clear	——	3DBh
——	Light Pen Set	——	3DCh
——	AT&T Mode	——	3DEh

Register Descriptions

ADDRESS REGISTER

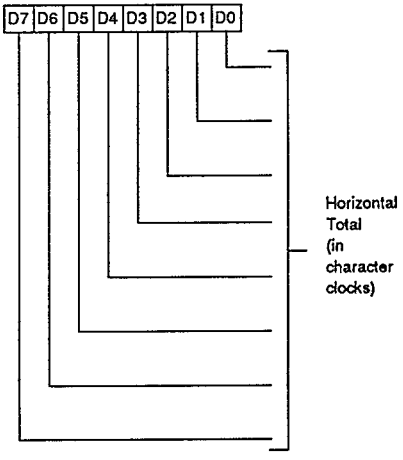
Read-Write Register
I/O Address: 3D4h



The Address Register is an 8-bit register. When loaded with a binary value(pointer), it points to the data register to be accessed.

HORIZONTAL TOTAL REGISTER (R0)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 00h

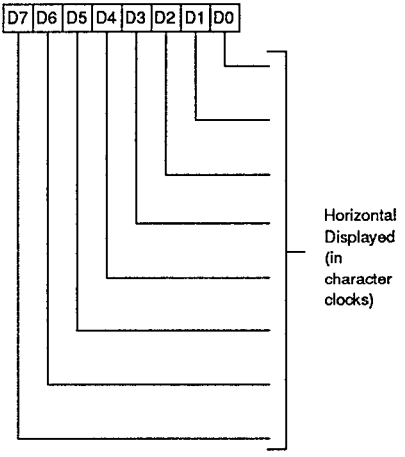


The Horizontal Total Register defines the number of characters in a horizontal scan line, including the retrace time. As such, it defines the horizontal sweep rate. The value programmed in this register is one less than the total character clocks in a horizontal scan line.

This register is ignored when an LCD display is used.

HORIZONTAL DISPLAYED REGISTER (R1)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 01h

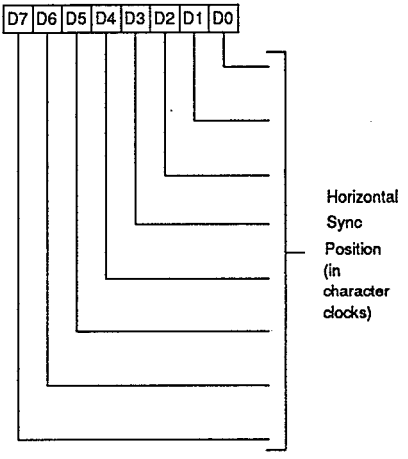


This 8-bit register determines the number of characters displayed per line, not including retrace time.

This register is used with both the CRT and LCD displays.

HORIZONTAL SYNC POSITION REGISTER (R2)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 02h

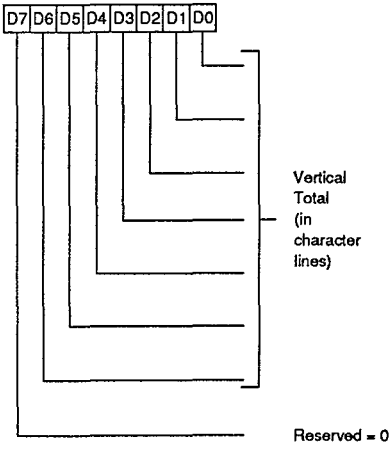


The Horizontal Sync Position Register controls the position of the horizontal sync pulse. The value programmed corresponds to the character location of the start of the horizontal sync pulse; characters are numbered from zero. When the programmed value is increased, the display on the CRT is shifted to the left. When the value is decreased, the display is shifted to the right.

This register is ignored when an LCD display is used.

VERTICAL TOTAL REGISTER (R4)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 04h

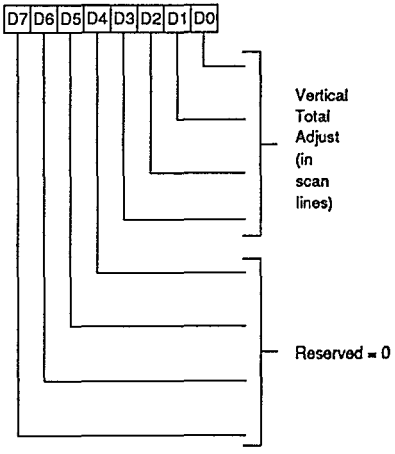


The Vertical Total Register and Vertical Total Adjust Register together determine the number of scan lines per frame. The value in the Vertical Total Register represents character row times while that in the Vertical Total Adjust register represents scan lines. The value programmed in this register is one less than the number of character rows per frame.

This register is ignored when an LCD display is used.

VERTICAL TOTAL ADJUST REGISTER (R5)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 05h

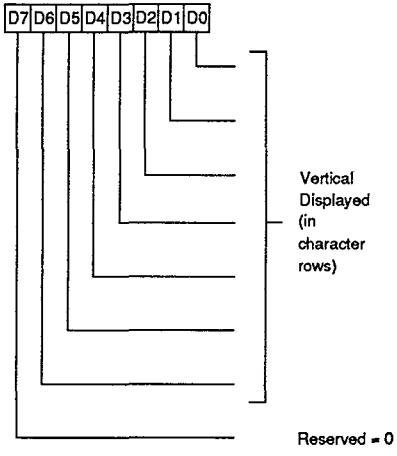


This 4-bit register defines the number of scan lines to be added to the Vertical Total Register content to determine the frame rate.

This register is ignored when an LCD display is used.

VERTICAL DISPLAYED REGISTER (R6)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 06h

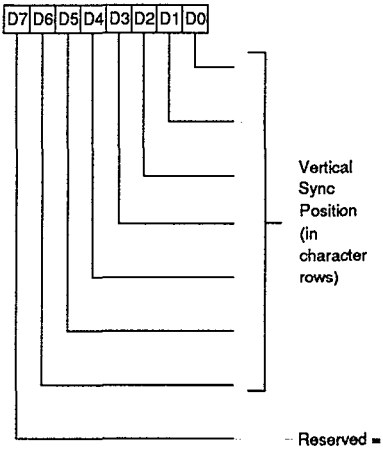


This 7-bit register specifies the number of displayed character rows per frame. This register is programmed in character row times.

This register is used with both CRT and LCD displays.

VERTICAL SYNC POSITION REGISTER (R7)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 07h

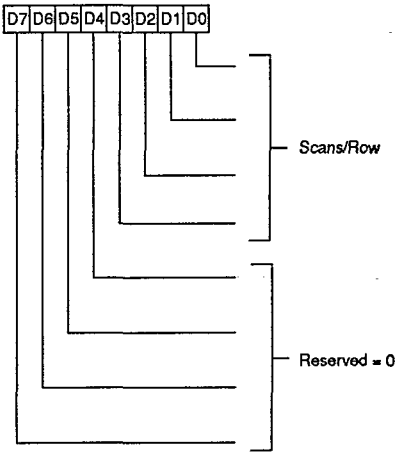


This 7-bit register defines the position of VSYNC and is programmed in terms of character row times. The programmed value corresponds to the character row at which the vertical sync pulse occurs; rows are numbered from 0. When the programmed value is increased the display on the CRT is shifted up; when decreased it is shifted down.

This register is ignored when an LCD display is used.

MAXIMUM SCAN LINE REGISTER (R9)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 09h

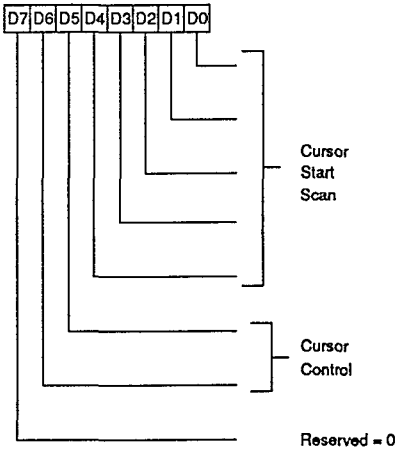


This 4-bit register determines the number of scan lines per character row. The row address counter is controlled by this register. The programmed value is one less than the number of scan lines/row.

This register is used with both CRT and LCD displays.

CURSOR START REGISTER (RA)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 0Ah



Bits D0-D4 specify the scan line (starting from 0) within a character row where the rectangular cursor block begins. The programmed value is the scan line at which the cursor starts.

Bits D6 and D5 control display of the Text Cursor as follows:

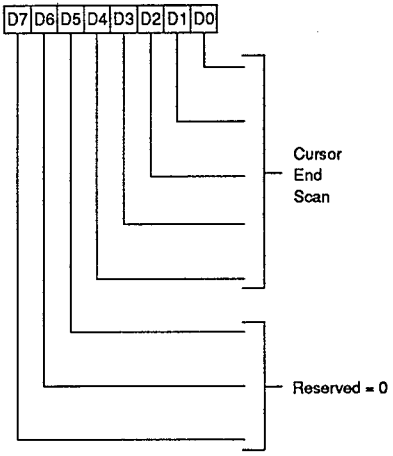
D6	D5	Cursor Attributes
0	0	Cursor is blinked at the blink rate
0	1	Cursor is turned off
1	0	Cursor is blinked at the blink rate
1	1	Cursor is blinked at half the blink rate

The Blink Rate is defined by the Vertical Sync Width/Blink control register (RDD). The default blink rate is 1/16 of the frame rate (blink on for 8 frames, off for 8 frames).

This register is used with both CRT and LCD displays.

CURSOR END REGISTER (RB)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 0Bh

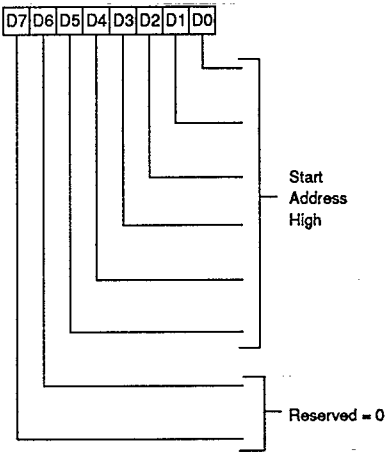


Bits D0-D4 specify the scan line (starting from 0) within a character row where the rectangular cursor block ends. The programmed value is one less than the scan line at which the cursor ends. If cursor start is greater than the cursor end, then a split cursor is displayed. If cursor start is beyond the character field, then no cursor is displayed.

This register is used with both CRT and LCD displays.

START ADDRESS HIGH REGISTER (RC)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 0Ch

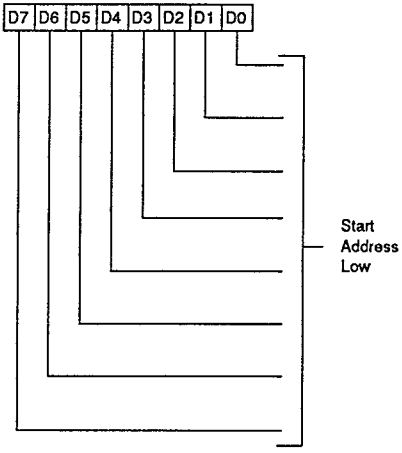


The Start Address is a 14-bit value which specifies the word address in the display buffer at which screen refresh starts. This display buffer address is mapped to the upper left corner of the screen. The Start Address High Register contains the 6 high-order bits of this address, while the Start Address Low Register specifies the 8 low-order bits. The most significant bit of the Start Address High register is read/write and does not affect the screen refresh start address.

This register is used with both CRT and LCD displays.

START ADDRESS LOW REGISTER (RD)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 0Dh

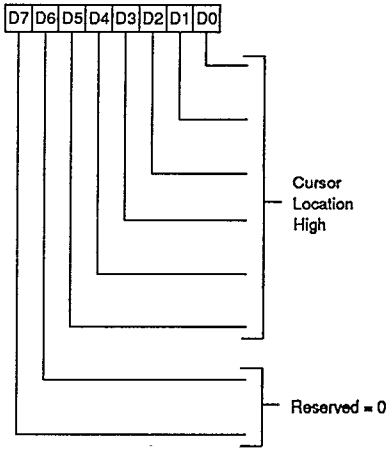


These 8 bits are the low order bits of the 14-bit word address in display memory at which screen refresh starts. This display buffer address is mapped to the upper left corner of the screen. The Start Address High register contains the 6 high-order bits of this address.

This register is used with both CRT and LCD displays.

CURSOR LOCATION HIGH REGISTER (RE)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 0Eh

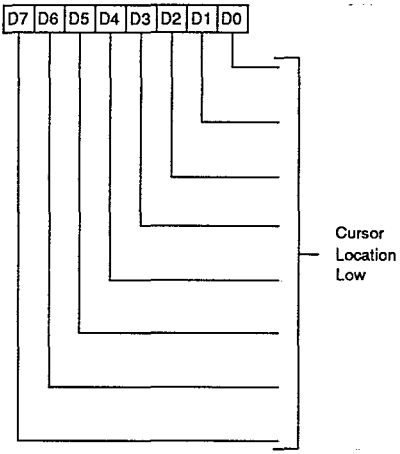


The Cursor Location address is a 14-bit value. The 6 high-order bits are programmed in the Cursor Location High Register. The 8 low-order bits are programmed in the Cursor Location Low Register. This 14-bit word address defines the display memory word address for the character which has the cursor superimposed on it. The most significant bit of the Cursor Location High register is read/write and does not affect the cursor address.

This register is used with both CRT and LCD displays.

CURSOR LOCATION LOW REGISTER (RF)

Read-Write Register
I/O Address: 3D5h
Address Pointer: 0Fh

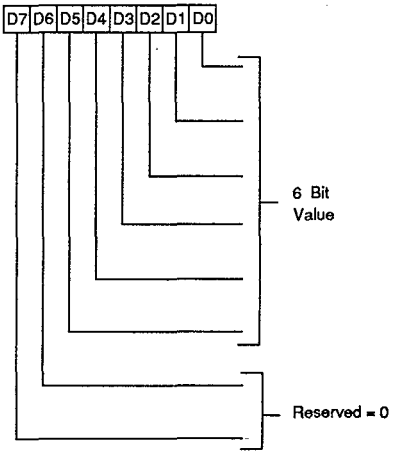


These 8 bits are the low order bits of the 14-bit Cursor Location address. The upper 6 bits are programmed in the Cursor Location High register. Together these 14 bits specify the display memory word address at which the cursor is located.

This register is used with both CRT and LCD displays.

LIGHT PEN HIGH REGISTER (R10)

Read Only Register
I/O Address: 3D5h
Address Pointer: 10h

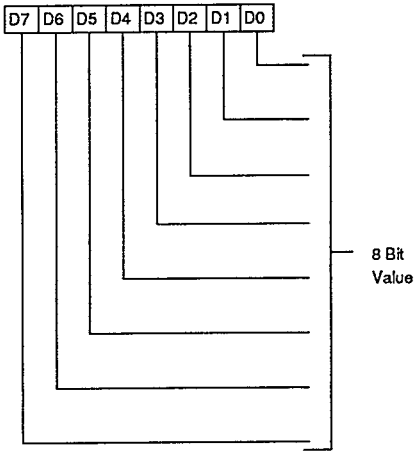


This register returns the upper 6 bits of the address latched by the light pen strobe. The active edge of the light pen strobe is generated by reading or writing the Set Light Pen register (address 3DCh); the other edge is generated by reading or writing the Clear Light Pen register (address 3DBh).

This register is used with both CRT and LCD displays.

LIGHT PEN LOW REGISTER (R11)

Read Only Register
I/O Address: 3D5h
Address Pointer: 11h

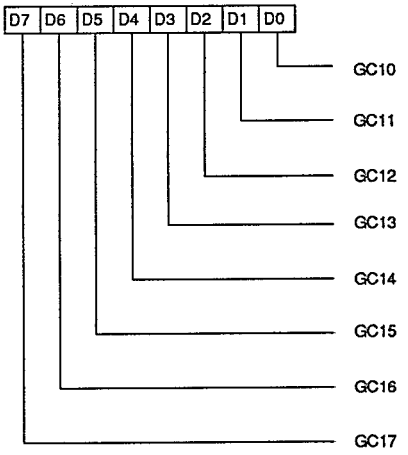


This register returns the lower 8 bits of the address latched by the light pen strobe. It is included for CGA software compatibility. The active edge of the light pen strobe is generated by reading or writing the Set Light Pen register (address 3DCh); the other edge is generated by reading or writing the Clear Light Pen register (address 3DBh).

This register is used with both CRT and LCD displays.

GRAY-LEVEL CONTROL REGISTER #1 (RD3)

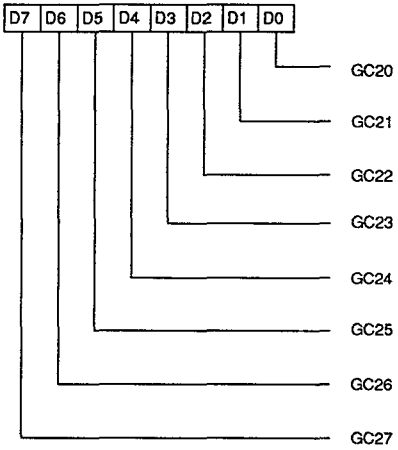
Read Write Register
I/O Address: 3D5h
Address Pointer: D3h



This register, along with RD4, is used to control parameters of the monochrome alternate gray-level algorithm. The recommended value is 43h, though other values may be used. Bit GC13 should be zero. Optimal value can depend on panel type.

GRAY-LEVEL CONTROL REGISTER #2 (RD4)

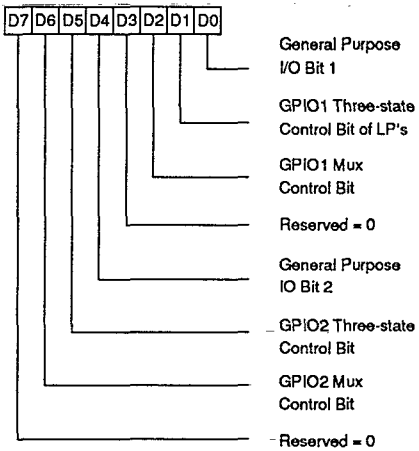
Read Write Register
I/O Address: 3D5h
Address Pointer: D4h



This register, along with RD3, is used to control parameters of the monochrome alternate gray-level algorithm. The recommended value is E6h, though other values may be used. Bits GC23 and GC27 should be zero. Optimal value can depend on panel type.

GENERAL-PURPOSE REGISTER (RD5)

Read Write Register
I/O Address: 3D5h
Address Pointer: D5h



The 82C426 supports two General-Purpose I/O pins which may be configured to have several functions. Each pin may be an output which reflects the state of either ROMCS/ or Display Enable (the default configuration); it may be an output which reflects the state of the corresponding software-writeable I/O bit; or it may be an input pin whose state may be read back as the software-readable I/O bit. This register is cleared to 0 upon reset.

D0: General-Purpose I/O 1 Bit

This bit may be written and read by the CPU. Its value may be reflected directly on the GPIO1 pin, or it may be used to read the state of the GPIO1 pin when the pin is configured as an input. It is cleared to 0 on RESET.

D1: General-Purpose I/O 1 Three-State Control Bit

This bit is used to control the function of the General-Purpose I/O1 Pin. When it is 0, the GPIO1 pin is

configured as an output pin. When it is a 1, the GPIO1 pin is three-stated and may be driven as an input from an external source. It is cleared to 0 on RESET.

D2: General-Purpose I/O 1 Mux Control Bit

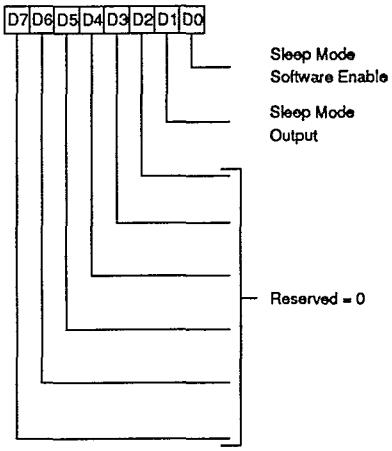
This bit controls the output function of the GPIO1 pin. When the bit is programmed to 0, the GPIO1 pin outputs the value of Display Enable. When the bit is programmed to a 1, the GPIO1 pin outputs the value of the GPIO1 Output Bit RD5,D0. Note that the GPIO1 pin is only driven if Bit 1 is set to 0. It is cleared to 0 on RESET.

D4-D6: General-Purpose I/O 2 Bits

These bits control the function of the GPIO2 pin, and are directly analogous to the I/O1 bits in D0:2 of this register. The only difference is that instead of Display Enable, GPIO2 outputs ROMCS/ in its primary output mode. This is an active low signal that indicates a valid memory read from any address in the range C0000h:C7FFFh.

SLEEP REGISTER (RD6)

Read Write Register
I/O Address: 3D5h
Address Pointer: D6h



D0: Sleep Mode Software Enable

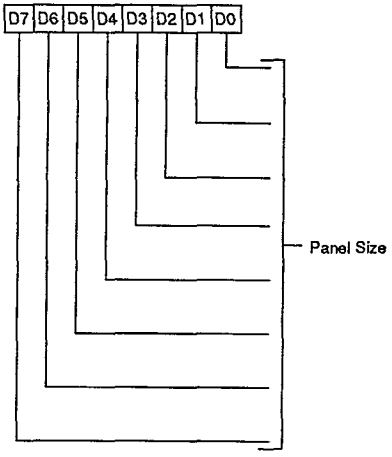
This bit invokes Sleep Mode. If a 1 is written to this bit, the 82C426 enters Sleep Mode after completing the current display fetch. There is no response to memory accesses by the CPU while in Sleep Mode, although all I/O registers remain accessible. The SLEEP Output pin is driven high. If a 0 is written to this bit, normal operation resumes, provided the Sleep Input pin is low. SLEEPIN, pin 50, can also be used to enter Sleep Mode.

D1: Sleep Mode Output

This read-only bit reflects the state of the SLEEP output pin, which is 1 if the 82C426 is in Sleep Mode, or if the Video Enable bit is cleared to zero.

PANEL SIZE REGISTER (RD7)

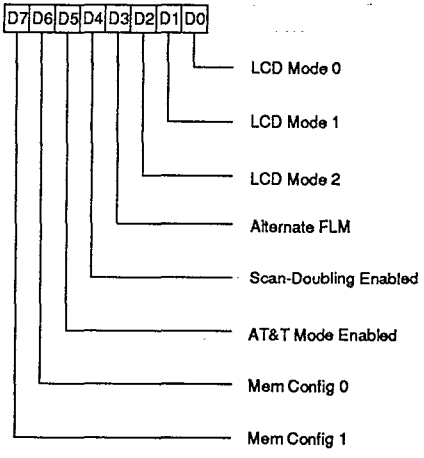
Read Write Register
I/O Address: 3D5h
Address Pointer: D7h



This 8-bit register defines the size of the upper panel in dual-panel systems. The size is defined in terms of scan-lines. The number programmed is one less than the number of scan-lines in the upper panel. Thus, for example, the maximum dual-panel display supported is a 512-line panel, consisting of two 256-line panels; in this case the programmed value would be FFh (255). This register is not cleared on reset, and is ignored in CRT Mode.

PANEL CONFIGURATION REGISTER (RD8)

Read Write Register
I/O Address: 3D5h
Address Pointer: D8h



D0-D2: LCD Mode

These bits select the LCD panel and drive type required. These bits are ignored in CRT Mode. The encoding is as follows:

D2	D1	D0	Panel Type
0	0	0	Single-Panel, Single-Drive
0	0	1	Dual-Panel, Single-Drive
0	1	0	Dual-Panel, Dual-Drive
0	1	1	Single-Panel, 12-bit Color
1	0	0	Single-Panel, 4-bit Color

On Reset these bits default to '000' - single-panel, single drive mode. Values other than those shown above are reserved.

Single Panel, Single Drive:

In this mode, operation is identical to the 82C425. Data is fetched sequentially from memory, and out-

put via the four-bit DOUT3:0 interface, four pixels at a time.

Dual Panel, Single Drive:

The data is output via the four-bit DOUT3:0 interface, four pixels at a time. Two scan-lines are output: first the upper panel scan line, then the lower panel scan line. LP is active during the last nibble of the lower panel data.

Dual Panel, Dual Drive:

Display data is output simultaneously to the upper and lower panel. Data for the upper panel is output on DOUT3:0; data to the lower panel is output on LOUT3:0. Four pixels are output at a time on each of the two interfaces.

Single Panel, 12-bit Color:

Three parallel display outputs are used for the Red, Green, and Blue components of each of the 4 pixels that are output at a time. The RGB components are output on DOUT3:0, LDOUT3:0, and VDOUT3:0 respectively. The Intensity bit in memory is ignored.

Single Panel, 4-bit Color:

One pixel is output per PCLK edge. The RGB components are output on DOUT3, DOUT2 and DOUT1 respectively, and the Intensity component is output on DOUT0.

D3: Alternate FLM

When this bit is 0, the FLM (First Line Marker) signal is generated in the same manner as the 82C425. It rises before the LP of the first line of data and falls after it. When this bit is 1, an alternate FLM time is generated. FLM rises as the last LP of the frame falls, and falls with the falling edge of the first LP of the frame.

D4-5: Scan-Doubling Enable, AT&T Mode Enable

D5	D4	Description
0	0	Normal Operation
0	1	Scan Doubling
1	X	AT&T Mode Enabled

These two bits along with the AT&T Control Bit in the AT&T Register (3DE) control support of extended resolution displays.

On Reset, these bits default to '00', normal operation. Each scan-line is displayed once only per screen refresh time.

If Bit 4 is set to 1 and Bit 5 to 0, Scan Doubling Mode is entered. In text modes, the text fonts are displayed at twice the height programmed into R9. For CGA-compatible text modes, an 8x16 EGA font is loaded. In graphics modes, the display is scan-doubled, each scan line being displayed twice. The display can therefore be toggled between 16-scan line font text mode and 200-line scan-doubled graphics mode in a CGA-compatible manner.

When D5=1, the AT&T Mode register (3DE) becomes accessible. It is otherwise invisible. The resolution now depends on the state of the AT&T Control Bit in the AT&T Register (3DE,D0). D4 is ignored if D5=1. If D5=1 and D0 of the AT&T Mode Register is 0, then the display is the same as when bit 4=1. If D5=1 and D0 of the AT&T Mode Register is 1, then graphics data is displayed at twice the screen height programmed into the CGA-compatible registers. Scan lines are not doubled. Text modes are still displayed when bit 4=1.

D6-7: Memory Configuration

D7	D6	Description
0	0	Default - 3 8Kx8 SRAMs or 2 8Kx8 SRAMs and 1 8Kx8 ROM
0	1	Single Mem - 1 32Kx8 SRAM
1	0	Dual Mem - 1 16Kx8, 1 8Kx8 SRAM/ROM
1	1	Dual Mem - 1 32Kx8, 1 8Kx8 SRAM/ROM

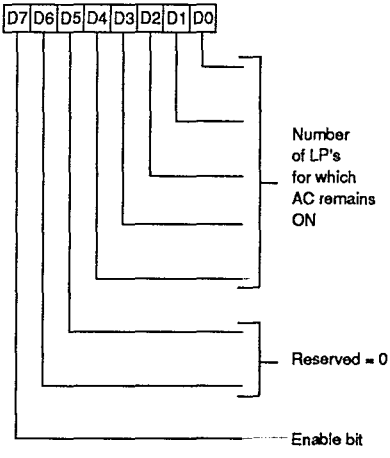
The Memory Configuration bits control how the 82C426 controls the external memory in the system.

On Reset the Memory Configuration Mode defaults to 00.

These configurations are explained in the Functional Description section.

AC CONTROL REGISTER (RD9)

Read-Write Register
I/O Address : 3D5
Address Pointer : D9h



D0-D4:

The value programmed into this register is one less than the number of Latch Pulses for LCD Displays which the AC signal is on and off (50% duty cycle).

D5-D6: Reserved

D7: Enable programmable AC

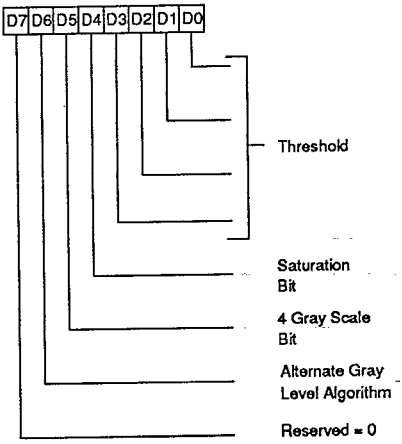
When this bit is 1, it enables the programmable AC signal generation. When this bit is 0, the AC signal remains ON for one frame and OFF for the next.

On reset, this bit is 0.

Gray Scale Registers

THRESHOLD REGISTER(RDA)

Read-Write Register
I/O Address: 3D5h
Address Pointer: DAh



D0-D3: Threshold Value

These bits define a threshold used to determine when to apply foreground and background shift values. SMARTMAP applies the shift when the difference between foreground and background colors does not exceed this threshold value.

D4: Saturation Bit

When D4 = 1, the shift in foreground and background colors done by SMARTMAP will be limited to the saturation points, i.e. overflow will cause the full scale output and underflow will generate a zero output.

When D4 = 0, the mapping of colors will be done with modulo-16 arithmetic.

D5: Gray Scale Bit

When D5 = 0, eight gray scales are selected for text modes. When D5 = 1, four gray scale mode is selected

D6: Alternate Gray-level Algorithm

In monchrome panel modes:

When equal to 0, the gray-level algorithm is the same as the 82C425. When set to 1, an alternate improved gray-level algorithm is used. The alternate algorithm is controlled by RD3 and RD4.

In color panel modes:

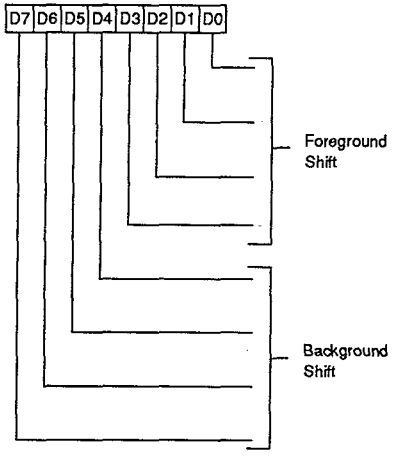
When equal to 0, no gray-level algorithm is used. When set to 1, a gray-level algorithm is applied to obtain 3 levels each of red, green and blue. This method generates the full set of colors displayed by the IBM CGA monitor.

D7: Reserved

Optimal value is dependent on panel type. On reset, this register contains 00h. This register has no effect in CRT mode.

SHIFT PARAMETER REGISTER(RDB)

Read-Write Register
I/O Address: 3D5h
Address Pointer: DBh



These shift values are used as part of SMARTMAP to increase contrast between foreground and background colors in gray scale text modes.

D0-D3: Foreground Shift
These four bits define the amount of shift for foreground colors in the text gray scale scheme.

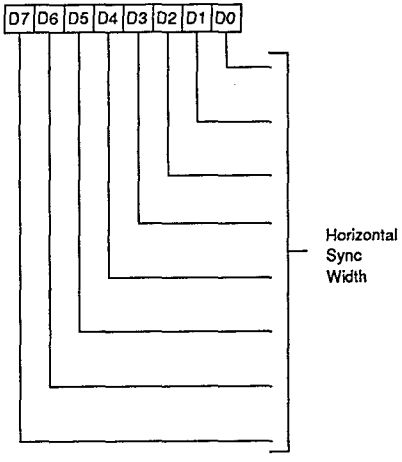
D4-D7: Background Shift
These bits define the background color shift.

Optimal value is dependent on panel type. On reset, this register contains 00h. This register has no effect in CRT mode.

Miscellaneous Registers

HORIZONTAL SYNC WIDTH REGISTER (RDC)

Read-Write Register
I/O Address: 3D5h
Address Pointer: DCh

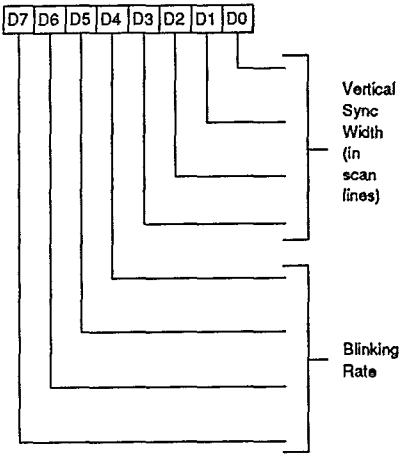


This register defines the width of the HSYNC pulse in terms of dot clocks. On power up this register defaults to a value of 40h, which is compatible to IBM's CGA when the dot clock has a frequency of 14.318 MHz.

This register is ignored when a LCD display is used.

VERTICAL SYNC WIDTH /BLINK CONTROL REGISTER (RDD)

Read-Write Register
I/O Address: 3D5h
Address Pointer: DDh



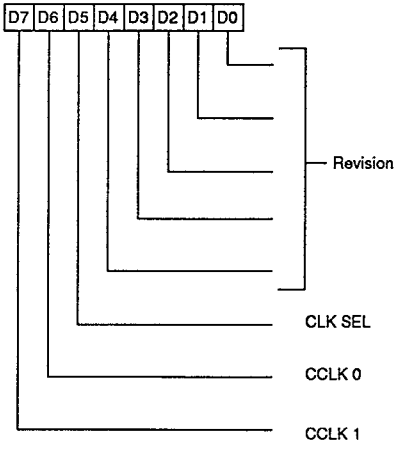
The lower 4 bits of this register define the width of VSYNC in terms of scan lines. On power up these bits default to a value of 2, which is compatible to IBM's CGA. The actual number of scan lines is one more than the value programmed in this register.

The upper 4 bits define the blinking rate of characters. The cursor blink rate is double the character blink rate. If the programmed value is N, the character will be on for N+1 frames and off for N+1 frames; the cursor will be on for (N+1)/2 frames and off for (N+1)/2 frames. The default value for blinking rate is 7.

This register is ignored when a LCD display is used.

TIMING CONTROL REGISTER(RDE)

Read-Write Register
I/O Address: 3D5h
Address Pointer: DEh



D0-D3: Revision
These bits indicate the silicon revision.

D5: Clk Select
This bit selects which clock input will be used by the controller as the master clock source. A 0 in this bit selects CLK1 while a 1 selects the CLK2.

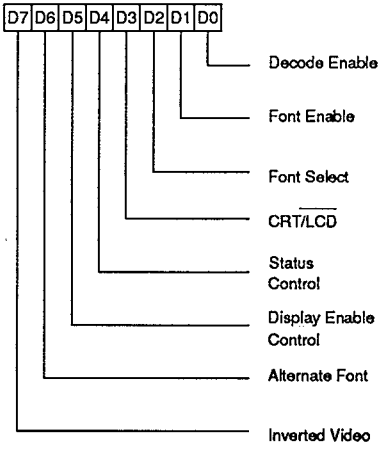
D6-D7: CCLK DIV 0-1
These bits determine the length of the panel shift clock in units of master clock cycles. These bits control the frequency of the pixel clock and panel shift clock as follows:

CCLK1	CCLK0	Pixel Frequency (CRT)	PCLK (LCD)
0	0	CLKIN/1	CLKIN/4
0	1	CLKIN/2	CLKIN/8
1	0	CLKIN/3	CLKIN/12
1	1	CLKIN/4	CLKIN/16

In CRT mode, the panel shift clock is not used. On reset, this register contains 00h.

FUNCTION CONTROL REGISTER(RDF)

Read-Write Register
I/O Address : 3D5h
Address Pointer: DFh



D0: Decode Enable
This bit controls the display buffer and I/O address decoding logic, and determines whether the device will respond to CPU memory and I/O accesses. When D0 = 0, the 82C426 does not respond to any reads by the host CPU to the display buffer or I/O addresses 3Dx. This bit should be set to 1 to enable CPU I/O and memory accesses. It is initialized to 0 at reset, at which time it is write-only. After it is set to 1, it can be read.

D1: **Font Enable**
This bit controls access to the font RAM. When set to '1', the font RAM can be accessed by the CPU as the first 8 Kbytes of the display buffer address space (B8000h-B9FFFh). When this bit is '0', access to the font RAM is disabled. This bit is initialized to '0' at reset.

D2: **Font Select**
This bit controls the selection of one of the two fonts resident in the font RAM. When '0', the font resident in low memory(B8000h) is selected. When '1', the upper memory(B9000h) font is selected.

D3: **CRT/$\overline{\text{LCD}}$**
When D3 = '1', a CRT display is selected. When D3 = '0', an LCD is selected.

D4: **Status Control**
For CRT: This bit is ignored for CRT displays.
For LCD: This bit affects the behavior of the Display Enable (3DA,DO) and Vertical Sync (3DA,D3) bits. When cleared (0), the Display Enable bit toggles every sixteen character clocks and the Vertical sync bit is active during the first scan line.
When set (1), the Display Enable and Vertical Sync bits behave differently. The Display Enable bit is active during the first 16 characters of each line and during all scan lines of rows 22 through the end of the panel in text modes (or row 85 through the end of the panel in graphics modes). The Vertical Sync bit is active during all scan lines of row 24 in text modes or rows 93 through 96 (inclusive) in graphics modes.

D5: **Enable Control**
For CRT: This bit is ignored for CRT displays.
For LCD: This bit affects the behavior of the Enable Video bit (3D8,D3). When cleared (0), the Enable Video bit behaves as in CRT mode. When set (1), disabling of the video data stream by clearing Enable Video is delayed until Display Enable is inactive. This prevents changes to the Enable Video bit from disturbing the LCD panel during active video display.

D6: **Alternate Font**
When D6 = 1, the Alternate Font is selected by text attribute bit AT3. When D6 = 0, attribute bit AT3 is the foreground intensity bit.

D7: **Inverted Video**
When D7 = 0, the video outputs are normal (positive true) TTL levels. When D7 = 1, the video outputs are inverted.

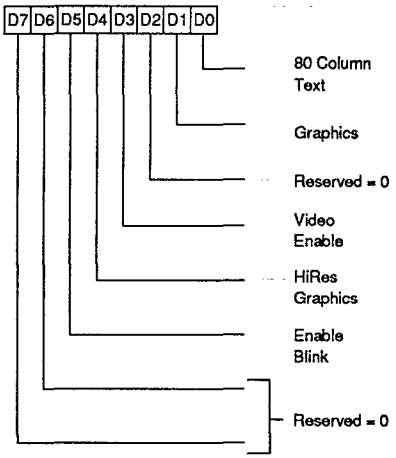
On reset, this register contains 00h.

Other CGA Registers

The 82C426 contains additional registers which are used in the CGA. These registers are described below.

MODE CONTROL REGISTER

Read - Write Register
I/O Address: 3D8h



Bits D0, D1, and D4 select a CGA submode. Submodes are defined by the following table (bit combinations not listed are illegal):

D4	D1	D0	Submode
1	1	0	640 x 200 Graphics
0	1	0	320 x 200 Graphics
0	0	1	80 x 25 Text
0	0	0	40 x 25 Text

D3: **Enable Video**

For CRT: When D3 = '1', video is enabled; when D3 = '0', video is disabled.

For LCD: Behavior of this bit depends on the Enable Control bit (RDF, D5). When the Enable Control bit is cleared, this bit behaves the same as for a CRT. When the Enable Control bit is set, the effect of clearing this bit (disabling video) is delayed until the Display Enable bit is inactive. This prevents changes to the Enable Video bit from disturbing the LCD panel during active video display.

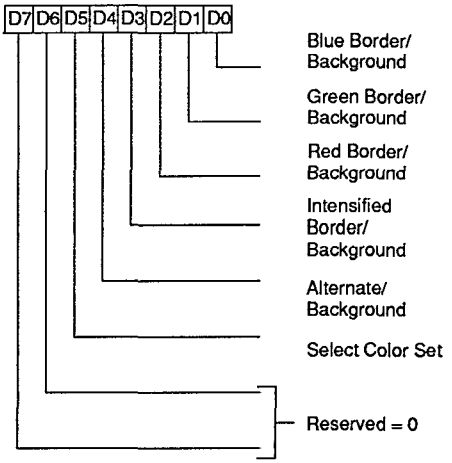
D5: **Enable Blink**

When D5 = '1', blinking is controlled by text attribute bit AT7. When '0', AT7 selects background intensity.

On reset, this register contains 00h.

CGA COLOR SELECT REGISTER

Read/Write Register
I/O Address: 3D9h



D0: Blue Border/Background

Selects blue border in 40x25 CGA text mode. Selects blue background in CGA 320x200 graphics mode. Selects blue foreground in CGA 640x200 graphics mode.

D1: Green Border/Background

Selects green border in 40x25 CGA text mode. Selects green background in CGA 320x200 graphics mode. Selects green foreground in CGA 640x200 graphics mode.

D2: Red Border/Background

Selects red border in 40x25 CGA text mode. Selects red background in CGA 320x200 graphics mode. Selects red foreground in CGA 640x200 graphics mode.

D3: Intensified Border/Background

Selects Intensified border in 40x25 CGA text mode. Selects Intensified background in CGA 320x200 graphics mode. Selects Intensified foreground in CGA 640x200 graphics mode.

D4: Alternate/Background

Selects alternate intensified colors in CGA graphics mode. Selects background colors in CGA text modes.

D5: Select Color Set

Selects foreground colors in CGA 320x200 graphics mode. The colors are generated as follows:

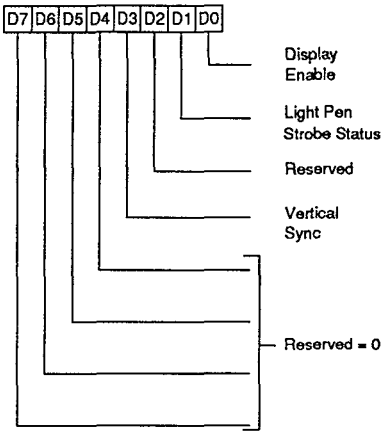
D5	Pixel Bit 1	Pixel Bit 0	Foreground Color
0	0	0	Background (D0-D3)
0	0	1	Green
0	1	0	Red
0	1	1	Brown
1	0	0	Background (D0-D3)
1	0	1	Cyan
1	1	0	Magenta
1	1	1	White

D6-D7: Reserved

On reset, this register contains 00h. This register is used with both CRT and LCD displays.

INPUT STATUS REGISTER

Read Only Register
I/O Address: 3DAh



Bits D0 and D3 have different meaning depending on the type of display selected.

D0: Display Enable

For CRT: A '1' indicates that the raster is in the retrace period.

For LCD: The behavior of this bit depends on the Status Control bit (RDF, D4). When the Status Control bit is cleared (0), the Display Enable bit toggles every sixteen character clocks. When the Status Control bit is set (1), the Display Enable bit is active during the first 16 characters of each line and during all scan lines of rows 22 through the end of the panel in text modes (or row 85 through the end of the panel in graphics modes).

D1: Light Pen Strobe

A '1' indicates that the Light Pen strobe has been set.

D3: Vertical Sync

For CRT: A '1' indicates that Vsync is active.

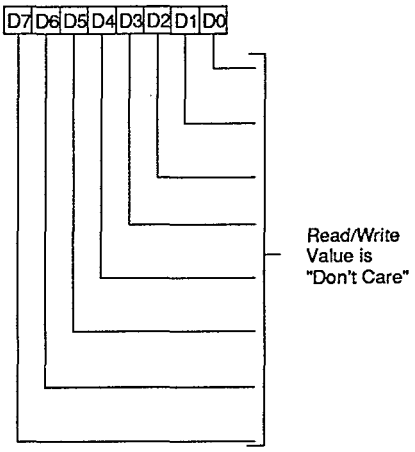
For LCD: The behavior of this bit depends on the Status Control bit (RDF, D4). When the Status Control bit is cleared (0), the Vertical Sync bit is active during the first scan line. When the Status Control bit is set (1), the Vertical Sync bit is active during all scan lines of row 24 in text modes or rows 93 through 96 (inclusive) in graphics modes.

D4-D7: Reserved

This register is used with both CRT and LCD displays.

CLEAR LIGHT PEN REGISTER

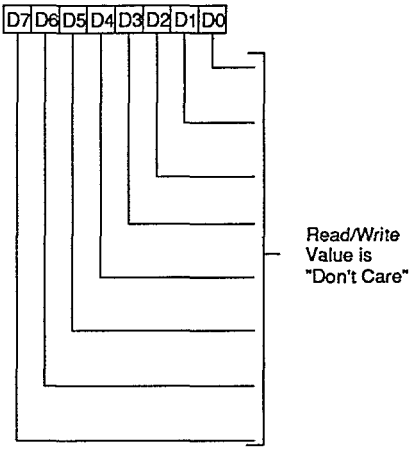
Read-Write Register
I/O Address: 3DBh



Reading or writing this register clears the strobe to the light pen latch. It may be cleared before or after the value is read from the Light Pen registers (R10h, R11h).

SET LIGHT PEN REGISTER

Read-Write Register
I/O Address: 3DCh

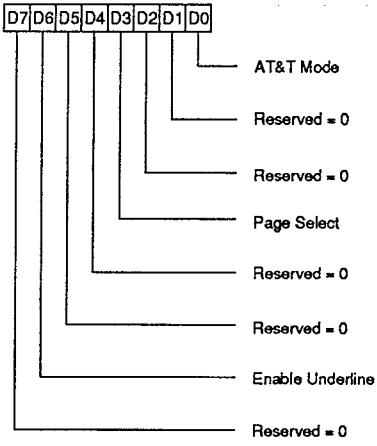


Reading or writing this register sets the light pen strobe, latching the current display memory address. This display memory address may be subsequently read through the Light Pen registers R10h and R11h. The Light Pen strobe must be explicitly reset by reading or writing the Clear Light Pen register (3DBh).

AT&T Mode Register

AT&T MODE REGISTER

Read - Write Register
I/O Address: 3DEh



This register is used to support AT&T 400-line M20 mode graphics. It is hidden if D5 of RD8 is not set.

D0: **AT&T Mode**

The AT&T Mode bit is enabled by the AT&T Enable bit in the Panel Configuration Register (RD8,D5). If D5 of RD8 is 0, the AT&T Mode Bit (3DE,D0) is ignored. If RD8,D5 is 1, the AT&T Mode Bit determines the extended resolution mode.

If the AT&T Bit is enabled, and the AT&T Mode Bit is 0, extended resolution Mode 1 is selected. In this mode, text data is displayed at 16-scan line resolution, and graphics data is displayed at 200-scan line double-scanned resolution. If the AT&T Bit is enabled and the AT&T Mode Bit is 1, then extended resolution mode 2 is selected. In this mode, text data is still displayed at 16-scan line resolution, but graphics data is displayed at true 400-scan line resolution, with 400 unique scan lines of data. On Reset this bit defaults to 0.

D3: **Page Select**

This bit selects between the upper and lower 16 Kbyte of memory. This bit is only significant in a 32 Kbyte memory configuration. In other configurations this bit has no effect. When D0 = 0, Display Memory starting at B8000h is used. When D0 = 1, Display Memory starting at BC000h is used. This bit is used in text modes and in 200-scan line graphics modes (whether scan doubled or not). The bit is not factored into the Text Cursor placement or the Light Pen latch. This bit is independent of the AT&T enable bit. It has no effect on CPU access of the memory. On Reset this bit defaults to 0.

D6: **Enable Underline**

This bit enables the MDA underline attribute (AT0) to display a foreground underline on the last scan line of the text character cell. When D6 = 0 (default), AT0 selects blue foreground. When D6 = 1, AT0 selects foreground color underline. This bit is not qualified by the AT&T enable bit. If the character on which the underline is set is also blinked, the underline blinks with the character.

D7: **Reserved**

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}		7.0	V
Input Voltage	Vi	-0.5	V_{DD}+0.5	V
Output Voltage	Vo	-0.5	V_{DD}+0.5	V
Operating Temperature	Top	-25	85	°C
Storage Temperature	Tstg	-40	125	°C

82C426 Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{DD}	4.5	5.5	V
Ambient Temperature	T_A	0	70	°C

82C426 DC Characteristics

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}		0.8	V
Input High Voltage (all pins except MD15:0)	V_{IH}	2.0		V
Input High Voltage (MD15:0)	V_{IH}	3.5		V
Output Low Voltage	V_{OL}		0.45	V
Output High Voltage	V_{OH}	2.4		V
Output Low Current (all pins except D0-D7, RDY, PCLK, HSYNC, VSYNC, AC, CRT/LCD)	I_{OL}		+4	mA
Output Low Current (D0-D7, RDY, PCLK, HSYNC, VSYNC, AC, CRT/LCD)	I_{OL}		+8	mA

82C426 DC Characteristics, *Continued*

Parameter	Symbol	Min	Max	Units
Output High Current (all pins except D0-D7, RDY, PCLK, HSYNC, VSYNC, AC, CRT/LCD)	I_{OH}		-4	mA
Output High Current (D0-D7, RDY, PCLK, HSYNC, VSYNC, AC, CRT/LCD)	I_{OH}		-8	mA
Input Leakage Current	I_{IL}	-100	+100	µA
Power Supply Current @ 14.3 MHz CLK, 0°C	$I_{CC\ ACTIVE}$		TBD	mA
Power Supply Current @ Clocks Stopped	I_{CC}		TBD	µA
Output High Impedance Leakage 0.45 <VPIN <VDD	I_{OZ}	-100	+100	µA

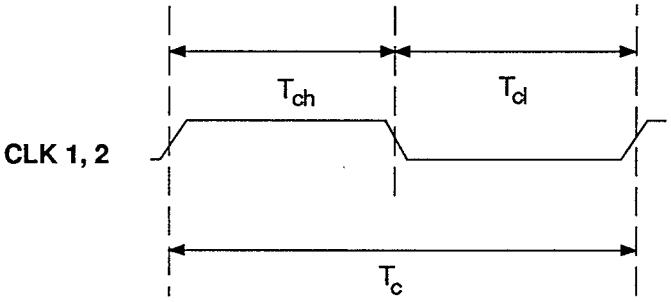
82C426 AC Timing Characteristics

(TA = 0°C - 70°C, VDD = 5V±10%)

Clock Timing

Parameter	Symbol	Min(ns)	Max(ns)
CLK1,2 Period	Tc	33	
CLK1,2 High time	Tch	16	
CLK1,2 Low time	Tcl	16	

CLKIN TIMING

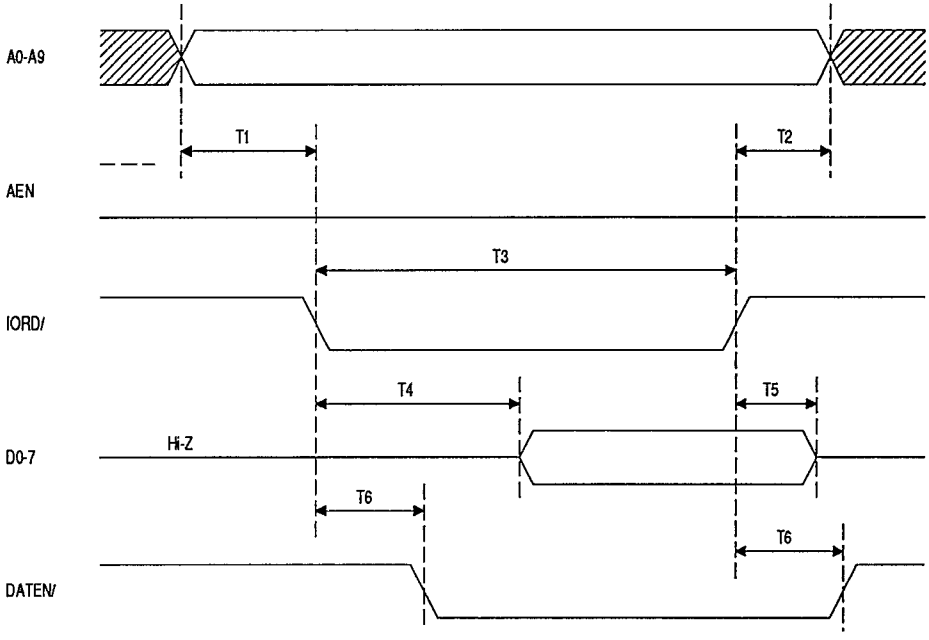


I/O BUS TIMING

I/O Read Cycle Timing

Parameter	Symbol	Min(ns)	Max(ns)
Address setup to IORD/ (I/O Read)	T1	25	
Address hold from IORD/ (I/O Read)	T2	0	
IORD/ Pulse Width	T3	100	
Valid data delay from IORD/	T4		40
Data Three-State from IORD/	T5		25
DATEN/ from IORD/	T6		25

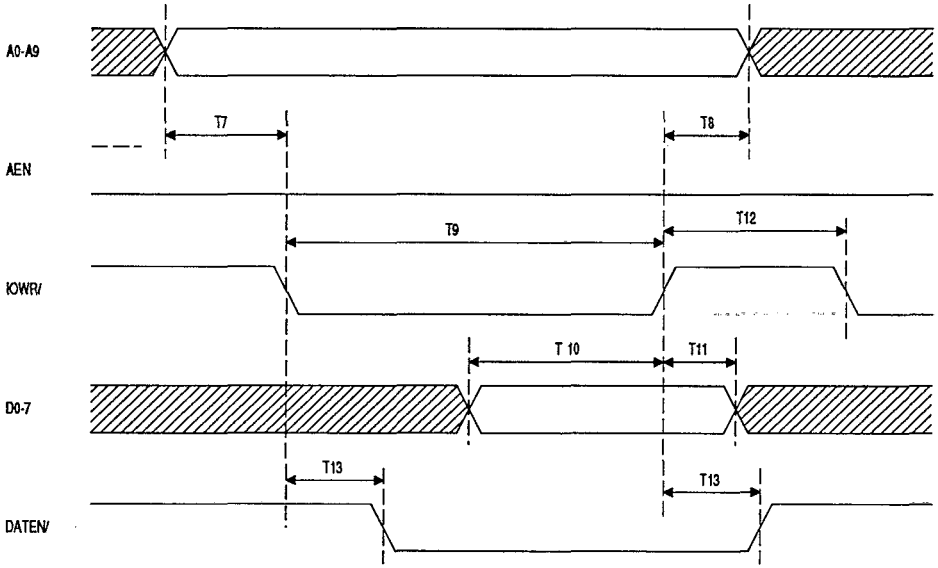
I/O READ CYCLE



I/O Write Cycle Timing

Parameter	Symbol	Min(ns)	Max(ns)
Address setup to IOWR/ (I/O Write)	T7	25	
Address hold from IOWR/ (I/O Write)	T8	0	
IOWR/ Pulse Width	T9	100	
Data Setup to IOWR/	T10	40	
Data Hold from IOWR/	T11	0	
Write Recovery Time	T12	60	
DATEN/ from IOWR/	T13		25

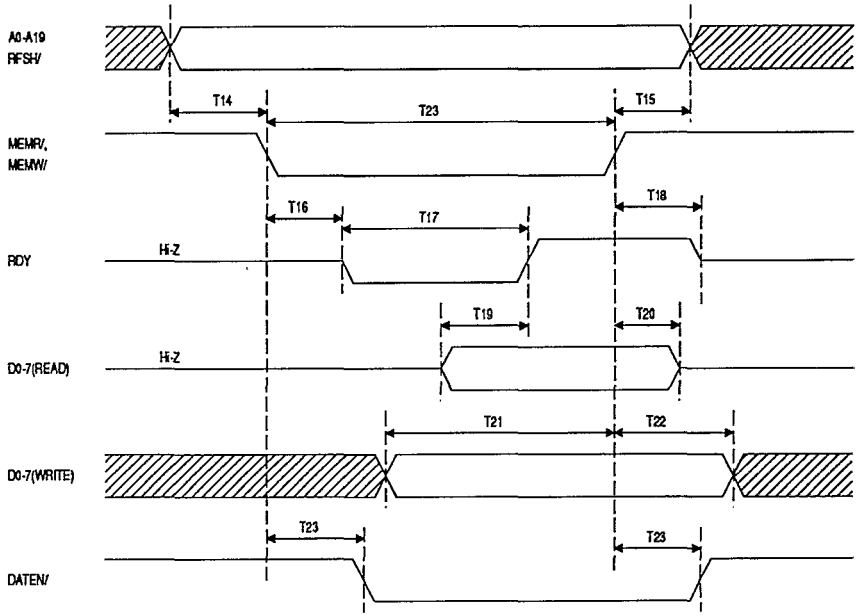
I/O WRITE CYCLE



Memory Read/Write Cycle Timing

Parameter	Symbol	Min(ns)	Max(ns)
Memory Address setup to MEMR/, MEMW/	T14	25	
Memory Address hold from MEMR/, MEMW/	T15	0	
MEMR/, MEMW/ to RDY Low delay	T16		25
RDY Width	T17	4Tc	12Tc
RDY Inactive Delay	T18		25
Memory Read Data setup to RDY	T19	0	
Memory Read Data hold from MEMR/	T20	5	30
Memory Write Data setup to MEMW/	T21	2Tc	
Memory Write Data hold from MEMW/	T22	0	
MEMR/, MEMW/ Pulse Width	T23	100	
DATEN from MEMW/ or MEMR/	T24		25

CPU MEMORY READ/WRITE CYCLE



LCD Video Timing

Parameter	Symbol	Min(ns)	Max(ns)
DOUT Delay	T25	-20	20
LP Delay (1)	T26	-20	20
LP to AC Delay	T27	-20	20

		Typ
FLM Setup Time (3)	T28	Tchar
FLM Hold Time	T29	Tchar

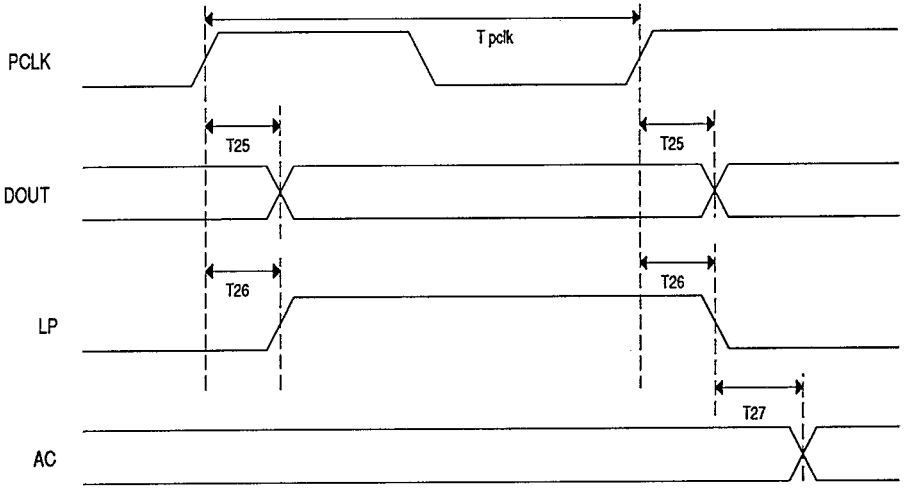
Notes:

1. LP is active only during output of the last video data for each scan line.
2. Tpclk = (4, 8, 12 or 16)x Tc, as programmed by the character clock divider field in the Timing Control Register (RDE).
3. The period of Tchar varies with the type of mode selected as follows:

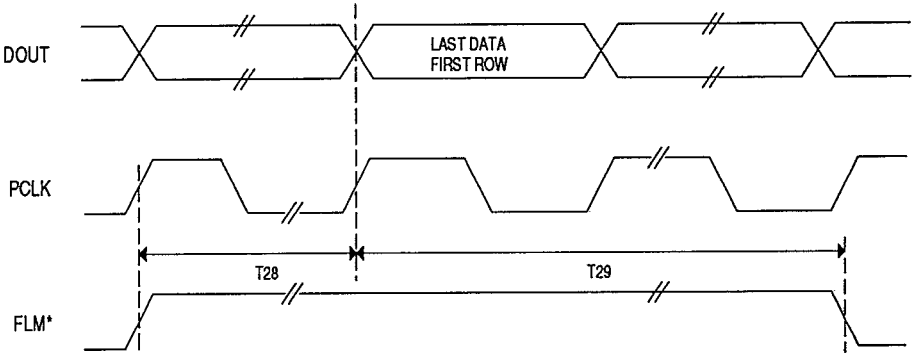
Period of the Character Clock in Each Mode

Mode	80 Column Text	40 Column Text	640 Wide Graphics	320 wide Graphics
Tchar	2 Tpclk	4 Tpclk	2 Tpclk	4 Tpclk

LCD VIDEO TIMING



FLM DETAIL



***NOTE:** FLM timing for RD8, D3=0 is shown.

SRAM Interface Timing

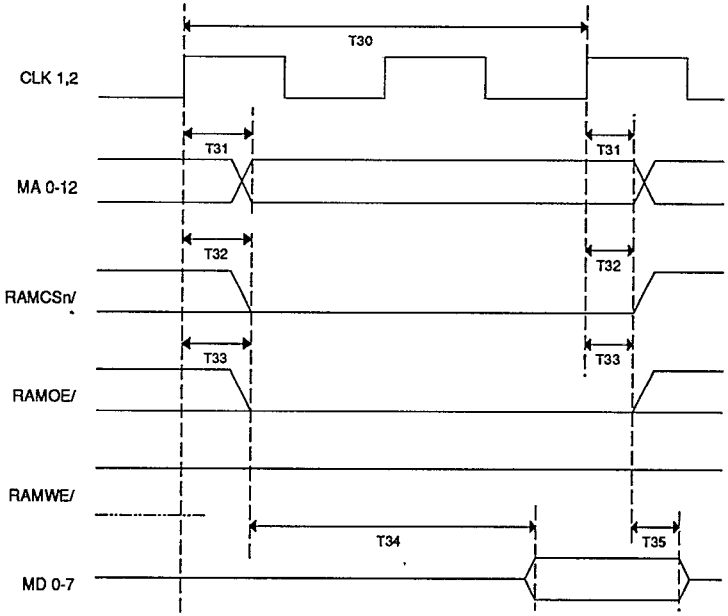
Parameter	Symbol	Min(ns)	Max(ns)
Read/Write Cycle Time	T30	2Tc[1]	2Tc[1]
Address Delay Time	T31	10	25
Chip Select Delay Time	T32	10	25
Output Enable Delay Time	T33	10	25
Read Data Setup Time	T34		2Tc - 15[1]
Read Data Hold Time	T35		0
Write Enable Active Delay Time	T36		25
Write Enable Inactive Delay Time	T37		25
Write Data Valid Delay	T38		30
Write Data Valid Hold Time	T39	0	

Notes:

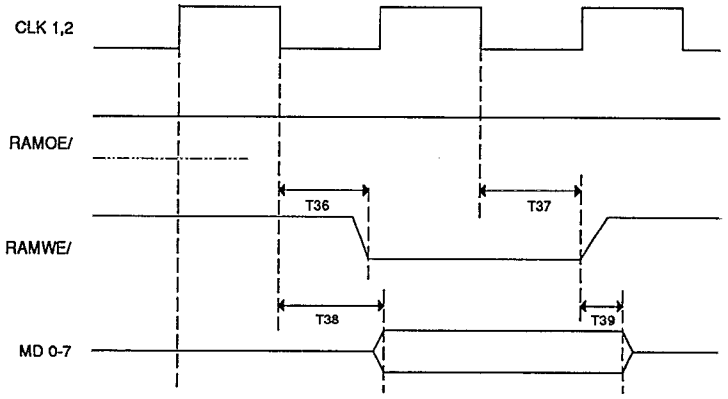
1. Static RAM with an access time of (2Tc-15ns) is required.

SRAM INTERFACE TIMING

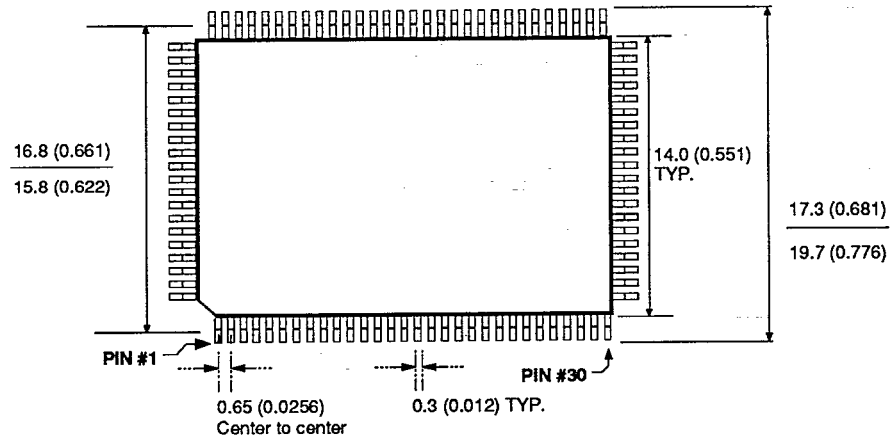
Memory Read Cycle

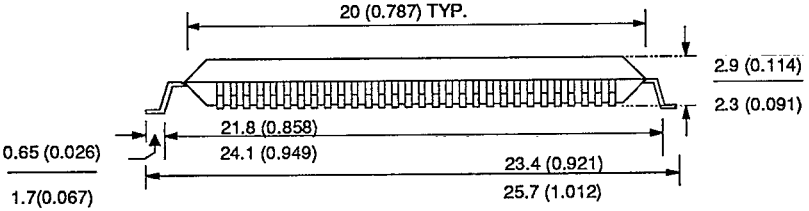


Memory Write Cycle



82C426 FLATPACK
Mechanical Dimensions





All dimensions in millimeters (inches)

Chips and Technologies, Incorporated
3050 Zanker Road, San Jose, CA 95134 408-434-0600 Telex 272929 CHIP UR