F87000

Multi-Mode
Peripheral Chip

Data Sheet

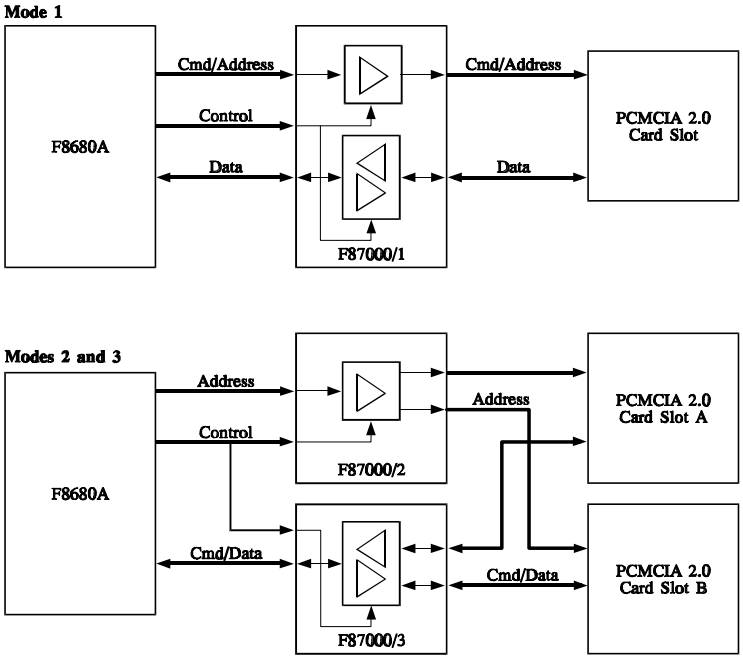
November 1993

P R E L I M I N A R Y

CHIPS®

F87000 Multi-Mode Peripheral Chip

- Fully static design substantially reduces power consumption when compared to discrete TTL designs, allowing direct battery drive.
- 3.3V or 5V operation provides flexibility for system design and allows dynamic 3.3/5V switching of system voltage to further reduce power consumption.
- Each F8700 device can be strapped to configure one of three buffer modes or a multi-function mode, reducing parts inventory requirements.
- High integration means each F8700 mode replaces at least seven discrete TTL devices.
- Full isolation of PCMCIA memory and I/O cards is supported to allow safe insertion and removal of cards, both "hot" and "cold."
- PCMCIA buffer modes are completely PCMCIA 2.0-compatible.
- For single PCMCIA card support, Mode 1 buffers 20 address lines and 5 control lines. Because of the quiet bus design of PC/CHIPm the upper address lines can be connected directly to the PCMCIA card slot in a single card system for full 64MB support.
- For dual PCMCIA card support, Modes 2 and 3 together buffer all necessary address and control lines for independent 64MB support of each card.
- Between PCMCIA cycles, the F87000 sets PCMCIA buses and control lines to a low-power state to consume only a fraction of the power used in a standard TTL buffer design.
- Multi-function mode (Mode 4) provides keyboard scanning, a parallel interface, and IDE interface, a configuration latch, and a 1.8MHz UART clock generation circuit.
- Keyboard scan interface in the multi-function mode requires only a single external resister pack and provides an interrupt to the system on key depression. The interface can be used instead as general-purpose 16-bit output and 8-bit input ports.
- Parallel interface in the multi-functional mode allows high-speed, PS/2-compatible bidirectional communication with other systems.
- Configuration latch can be used to control seven external devices plus the UART clock divider. An additional decode line accommodates an external latch for eight more device control lines.



System Diagram

Revision History

Revision	Date	By	Comment
0.1	7/6/93	PD	Internal Review—Rough Draft
0.2	8/6/93	PD	Internal Review—Added product overview write-up and made additional author's changes.
03	9/4/93	ST	Internal Review—Added Pin 41, 39, and 99 descriptions; Modified Electrical Timing Section
1.0	11/23/93	ST	Initial Release

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Introduction

The F87000 Multi-Mode Peripheral Chip is a companion to the F8680A PC/CHIP single-chip PC. By strapping pins to select the desired mode, the F87000 device becomes one of four integrated peripheral chips that extend the functionality of PC/CHIP.

Chips and Technologies, Inc. has designed the F87000 chip specifically for use with the F8680A microchip to accomodate portable computing devices and embedded control applications where integration, conservation of board space, and power consumption are critical.

In PCMCIA card implementations, card buffering and isolation is recommended for design robustness, especially in rugged use environments. The buffering ensures that the PCMCIA card receives a strong clean signal, while the isolation provides both the protection for "hot card insertion" and is hardwired for turning off power to a card. Hardware isolation, supported with Power Management SuperState code, minimizes the system's power consumption. PCMCIA card slots that are not properly buffered and isolated run a high risk of a system crash/failure if the cards are inserted/ removed while the slot is powered.

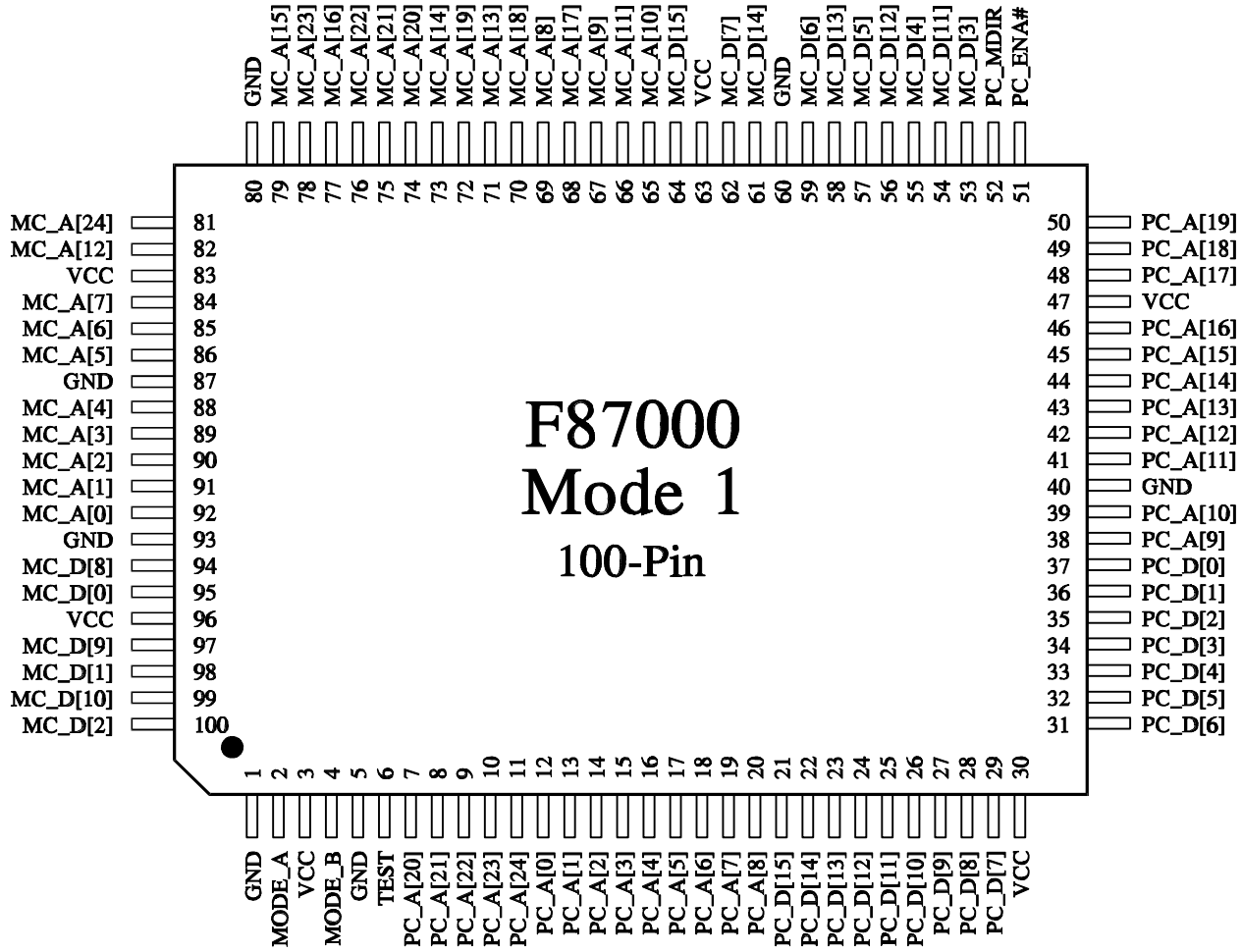
The PC/CHIP F87000 is designed to be used in four modes.

- Mode 1—Single PCMCIA card buffering support provides:
  - 20-bit address buffer.
  - 16-bit bidirectional data buffer.
  - Buffering for five control signals.
- Modes 2 and 3—Dual PCMCIA card buffering support provides:
  - Individual address buffering (64MB each).
  - Individual data bus buffering.
  - Two OR gates.
- Mode 4—Multifunctional mode provides:
  - Keyboard circuitry interfacing to a 16 x 8 keyboard matrix.
  - Clock divider conversion of 14.31818MHz to 1.8432MHz output (divide by 7.77).
  - Parallel printer port.
  - IDE interface.
  - 7-bit configuration ports plus external select for port expansion.

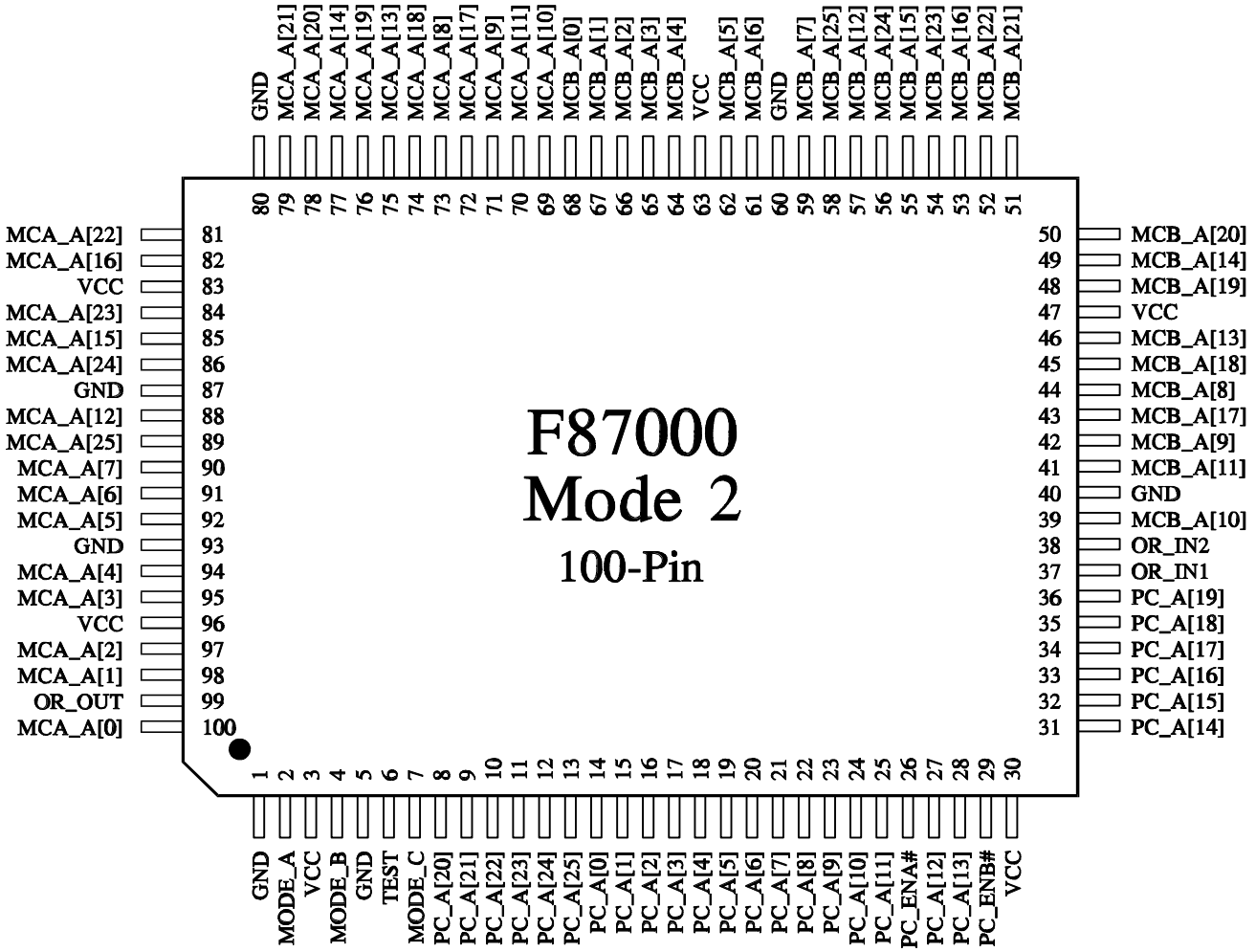
Pinouts

The F87000 is designed for four modes of operation. The pinout diagrams for each mode is shown below and on the following pages. Following the diagrams are the alphabetical lists of the pins per mode (Pin List).

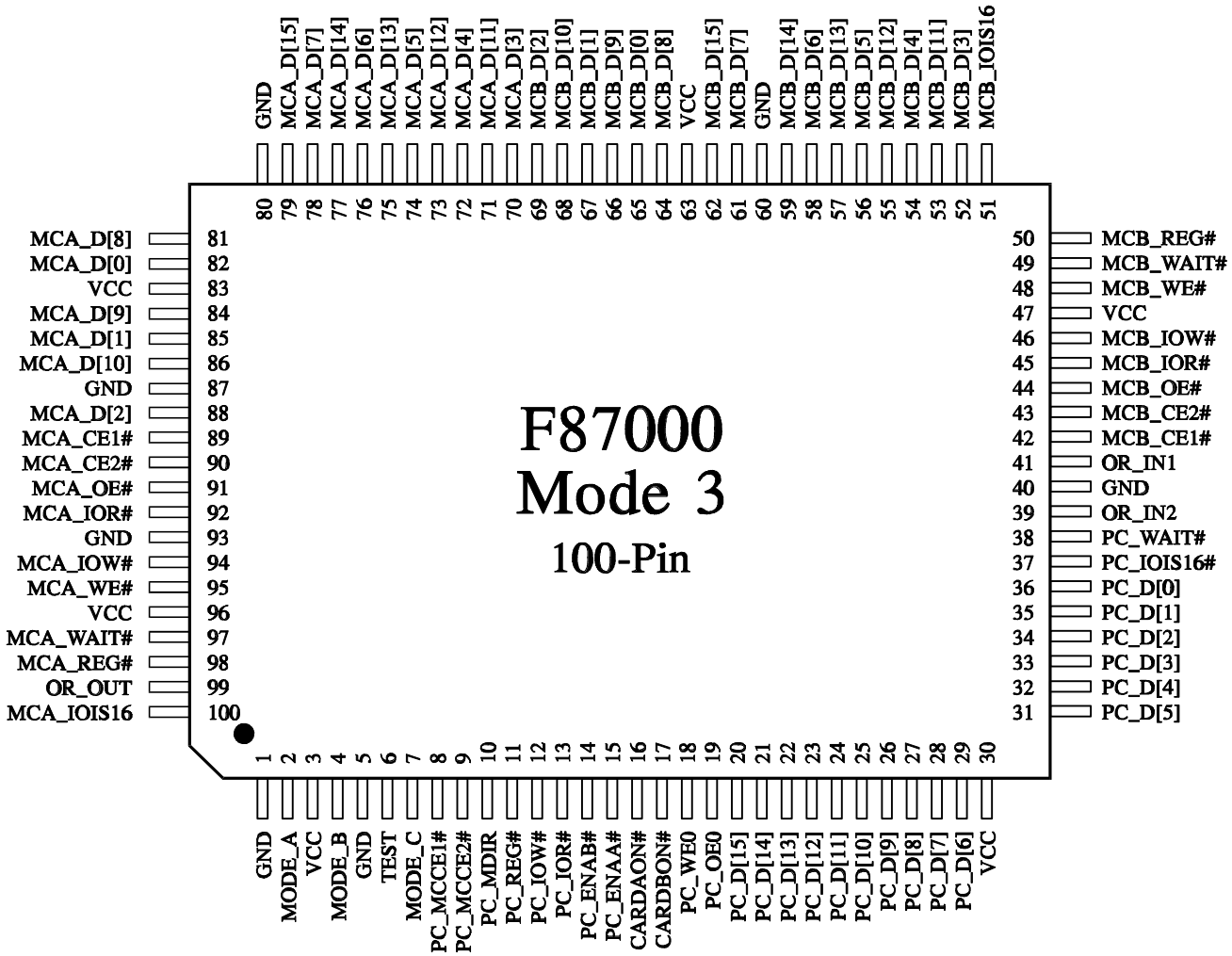
The detailed description of the pins follow the pin list.



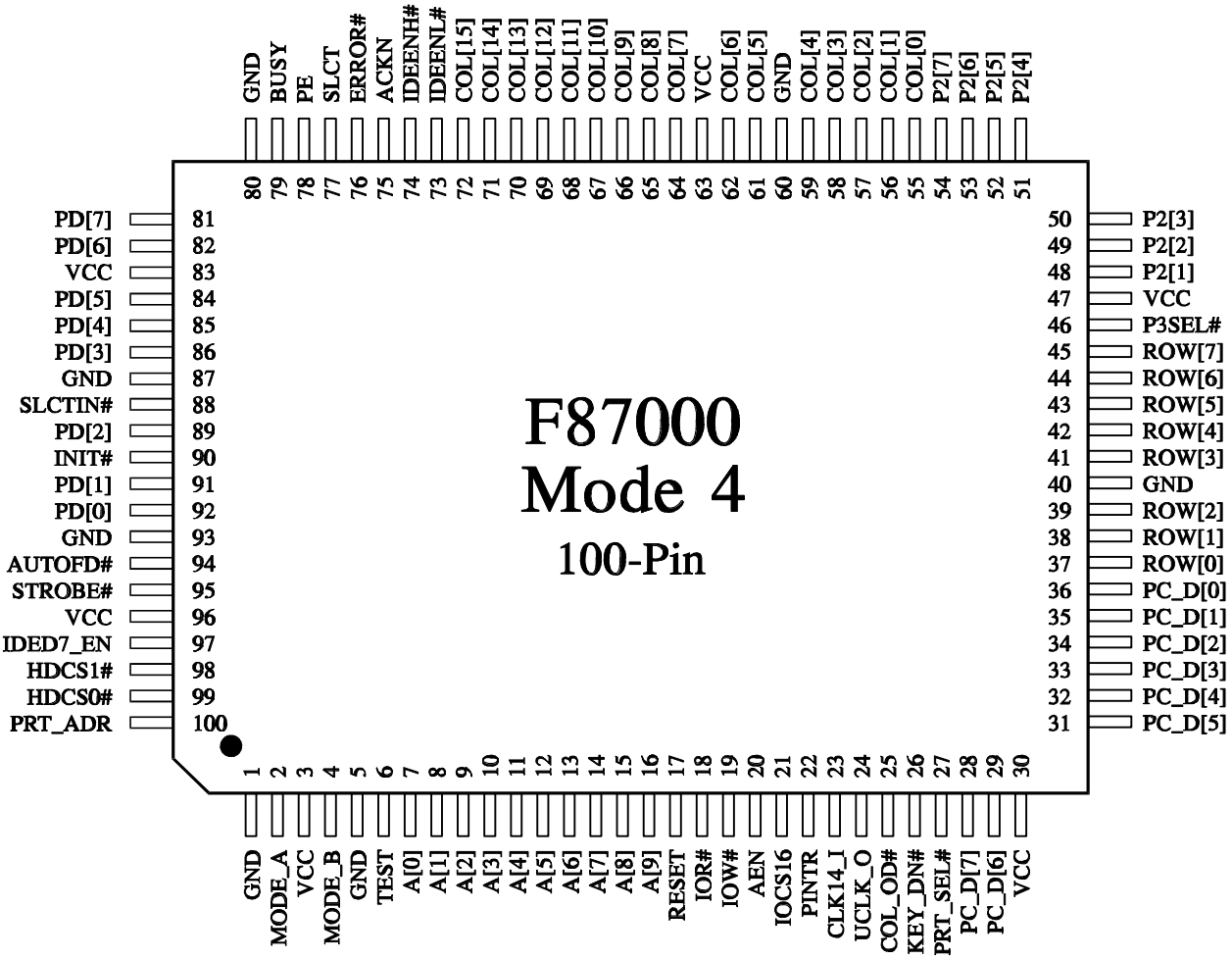
F87000 Pinout, Mode 1—Top View



F87000 Pinout, Mode 2—Top View



F87000 Pinout, Mode 3—Top View



F87000 Pinout, Mode 4—Top View

PIN LIST—MODE 1

Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)
GND	1	G	—	—	MC_D[2]	100	I/O	—	4	PC_A[18]	49	I	TTL	—
GND	5	G	—	—	MC_D[3]	53	I/O	TTL	4	PC_A[19]	50	I	TTL	—
GND	40	G	—	—	MC_D[4]	55	I/O	TTL	4	PC_A[20]	7	I	SHCMOS	—
GND	60	G	—	—	MC_D[5]	57	I/O	TTL	4	PC_A[21]	8	I	SHCMOS	—
GND	80	G	—	—	MC_D[6]	59	I/O	TTL	4	PC_A[22]	9	I	SHCMOS	—
GND	87	G	—	—	MC_D[7]	62	I/O	TTL	4	PC_A[23]	10	I	SHCMOS	—
GND	93	G	—	—	MC_D[8]	94	I/O	—	12	PC_A[24]	11	I	SHCMOS	—
MC_A[0]	92	O	—	12	MC_D[9]	97	I/O	—	12	PC_D[0]	37	I/O	SHCMOS	4
MC_A[1]	91	O	—	12	MC_D[10]	99	1/0	—	12	PC_D[1]	36	I/O	SHCMOS	4
MC_A[2]	90	O	—	12	MC_D[11]	54	I/O	TTL	4	PC_D[2]	35	I/O	SHCMOS	4
MC_A[3]	89	O	—	12	MC_D[12]	56	I/O	TTL	4	PC_D[3]	34	I/O	SHCMOS	4
MC_A[4]	88	O	—	12	MC_D[13]	58	I/O	TTL	4	PC_D[4]	33	I/O	SHCMOS	4
MC_A[5]	86	O	—	12	MC_D[14]	61	I/O	TTL	4	PC_D[5]	32	I/O	SHCMOS	4
MC_A[6]	85	O	—	12	MC_D[15]	64	I/O	TTL	4	PC_D[6]	31	I/O	SHCMOS	4
MC_A[7]	84	O	—	12	MODE_A	2	I	SHCMOS	—	PC_D[7]	29	I/O	SHCMOS	4
MC_A[8]	69	O	—	4	MODE_B	4	I	SHCMOS	—	PC_D[8]	28	I/O	SHCMOS	4
MC_A[9]	67	O	—	4	PC_A[0]	12	I	SHCMOS	—	PC_D[9]	27	I/O	SHCMOS	4
MC_A[10]	65	O	—	4	PC_A[1]	13	I	SHCMOS	—	PC_D[10]	26	I/O	SHCMOS	4
MC_A[11]	66	O	—	4	PC_A[2]	14	I	SHCMOS	—	PC_D[11]	25	I/O	SHCMOS	4
MC_A[12]	82	O	—	12	PC_A[3]	15	I	SHCMOS	—	PC_D[12]	24	I/O	SHCMOS	4
MC_A[13]	71	O	—	4	PC_A[4]	16	I	SHCMOS	—	PC_D[13]	23	I/O	SHCMOS	4
MC_A[14]	73	O	—	4	PC_A[5]	17	I	SHCMOS	—	PC_D[14]	22	I/O	SHCMOS	4
MC_A[15]	79	O	—	4	PC_A[6]	18	I	SHCMOS	—	PC_D[15]	21	I/O	SHCMOS	4
MC_A[16]	77	O	—	4	PC_A[7]	19	I	SHCMOS	—	PC_ENA#	51	I	TTL	—
MC_A[17]	68	O	—	4	PC_A[8]	20	I	SHCMOS	—	PC_MDIR	52	I	TTL	—
MC_A[18]	70	O	—	4	PC_A[9]	38	I	SHCMOS	—	TEST	6	IP	SHCMOS	—
MC_A[19]	72	O	—	4	PC_A[10]	39	I	TTL	—	VCC	3	P	—	—
MC_A[20]	74	O	—	4	PC_A[11]	41	I	TTL	—	VCC	30	P	—	—
MC_A[21]	75	O	—	4	PC_A[12]	42	I	TTL	—	VCC	47	P	—	—
MC_A[22]	76	O	—	4	PC_A[13]	43	I	TTL	—	VCC	63	P	—	—
MC_A[23]	78	O	—	4	PC_A[14]	44	I	TTL	—	VCC	83	P	—	—
MC_A[24]	81	O	—	12	PC_A[15]	45	I	TTL	—	VCC	96	P	—	—
MC_D[0]	95	I/O	—	12	PC_A[16]	46	I	TTL	—					
MC_D[1]	98	I/O	—	12	PC_A[17]	48	I	TTL	—					

Notes:

All VCC pads must be externally connected to VCC supply.
All GND pads must be externally connected to ground.

I	Input pin
O	Output pin
I/O	Bidirectional pin
IUP	Input pin with internal pull-up resistor
OD	Open drain output
SHCMOS	CMOS Schmitt-trigger input

PIN LIST—MODE 2

Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)
GND	1	G	—	—	MCB_A[1]	67	O	—	4	PC_A[3]	17	I	SHCMOS	—
GND	5	G	—	—	MCB_A[2]	66	O	—	12	PC_A[4]	18	I	SHCMOS	—
GND	40	G	—	—	MCB_A[3]	65	O	—	12	PC_A[5]	19	I	SHCMOS	—
GND	60	G	—	—	MCB_A[4]	64	O	—	4	PC_A[6]	20	I	SHCMOS	—
GND	80	G	—	—	MCB_A[5]	62	O	—	4	PC_A[7]	21	I	SHCMOS	—
GND	87	G	—	—	MCB_A[6]	61	O	—	4	PC_A[8]	22	I	SHCMOS	—
GND	93	G	—	—	MCB_A[7]	59	O	—	4	PC_A[9]	23	I	SHCMOS	—
MCA_A[0]	100	O	—	4	MCB_A[8]	44	O	—	4	PC_A[10]	24	I	TTL	—
MCA_A[1]	98	O	—	12	MCB_A[9]	42	O	—	4	PC_A[11]	25	I	TTL	—
MCA_A[2]	97	O	—	12	MCB_A[10]	39	0	—	4	PC_A[12]	27	I	TTL	—
MCA_A[3]	95	O	—	12	MCB_A[11]	41	O	—	4	PC_A[13]	28	I	TTL	—
MCA_A[4]	94	O	—	12	MCB_A[12]	57	O	—	4	PC_A[14]	31	I	TTL	—
MCA_A[5]	92	O	—	12	MCB_A[13]	46	O	—	4	PC_A[15]	32	I	TTL	—
MCA_A[6]	91	O	—	12	MCB_A[14]	49	O	—	4	PC_A[16]	33	I	TTL	—
MCA_A[7]	90	O	—	12	MCB_A[15]	55	O	—	4	PC_A[17]	34	I	TTL	—
MCA_A[8]	73	O	—	4	MCB_A[16]	53	O	—	4	PC_A[18]	35	I	TTL	—
MCA_A[9]	71	O	—	4	MCB_A[17]	43	O	—	4	PC_A[19]	36	I	TTL	—
MCA_A[10]	69	O	—	4	MCB_A[18]	45	O	—	4	PC_A[20]	8	I	SHCMOS	—
MCA_A[11]	70	O	—	4	MCB_A[19]	48	O	—	4	PC_A[21]	9	I	SHCMOS	—
MCA_A[12]	88	O	—	12	MCB_A[20]	50	O	—	4	PC_A[22]	10	I	SHCMOS	—
MCA_A[13]	75	O	—	4	MCB_A[21]	51	O	—	4	PC_A[23]	11	I	SHCMOS	—
MCA_A[14]	77	O	—	4	MCB_A[22]	52	O	—	4	PC_A[24]	12	I	SHCMOS	—
MCA_A[15]	85	O	—	12	MCB_A[23]	54	O	—	4	PC_A[25]	13	I	SHCMOS	—
MCA_A[16]	82	O	—	12	MCB_A[24]	56	O	—	4	PC_ENA#	26	I	SHCMOS	—
MCA_A[17]	72	O	—	4	MCB_A[25]	58	O	—	4	PC_ENB#	29	I	SHCMOS	—
MCA_A[18]	74	O	—	4	MODE_A	2	I	SHCMOS	—	TEST	6	IP	SHCMOS	—
MCA_A[19]	76	O	—	4	MODE_B	4	I	SHCMOS	—	VCC	3	P	—	—
MCA_A[20]	78	O	—	4	MODE_C	7	I	SHCMOS	—	VCC	30	P	—	—
MCA_A[21]	79	O	—	4	OR_IN1	37	I	SHCMOS	—	VCC	47	P	—	—
MCA_A[22]	81	O	—	12	OR_IN2	38	I	SHCMOS	—	VCC	63	P	—	—
MCA_A[23]	84	O	—	12	OR_OUT	99	O	—	12	VCC	83	P	—	—
MCA_A[24]	86	O	—	12	PC_A[0]	14	I	SHCMOS	—	VCC	96	P	—	—
MCA_A[25]	89	O	—	12	PC_A[1]	15	I	SHCMOS	—					
MCB_A[0]	68	O	—	4	PC_A[2]	16	I	SHCMOS	—					

Notes:

All VCC pads must be externally connected to VCC supply.
All GND pads must be externally connected to ground.

I	Input pin
O	Output pin
I/O	Bidirectional pin
IUP	Input pin with internal pull-up resistor
OD	Open drain output
SHCMOS	CMOS Schmitt-trigger input

PIN LIST—MODE 3

Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)
GND	1	G	—	—	MCB_D[0]	65	I/O	TTL	4	PC_D[3]	33	I	SHCMOS	—
GND	5	G	—	—	MCB_D[1]	67	I/O	TTL	4	PC_D[4]	32	I	SHCMOS	—
GND	40	G	—	—	MCB_D[2]	69	I/O	TTL	4	PC_D[5]	31	I	SHCMOS	—
GND	60	G	—	—	MCB_D[3]	52	I/O	TTL	4	PC_D[6]	29	I	SHCMOS	—
GND	80	G	—	—	MCB_D[4]	54	I/O	TTL	4	PC_D[7]	28	I	SHCMOS	—
GND	87	G	—	—	MCB_D[5]	56	I/O	TTL	4	PC_D[8]	27	I	SHCMOS	—
GND	93	G	—	—	MCB_D[6]	58	I/O	TTL	4	PC_D[9]	26	I	SHCMOS	—
CARDAON#	16	I	SHCMOS	—	MCB_D[7]	61	I/O	TTL	4	PC_D[10]	25	I	TTL	—
CARDBON#	17	I	SHCMOS	—	MCB_D[8]	64	I/O	TTL	4	PC_D[11]	24	I	TTL	—
MCA_D[0]	82	I/O	TTL	12	MCB_D[9]	66	I/O	TTL	4	PC_D[12]	23	I	TTL	—
MCA_D[1]	85	I/O	TTL	12	MCB_D[10]	68	I/0	TTL	4	PC_D[13]	22	I	TTL	—
MCA_D[2]	88	I/O	TTL	12	MCB_D[11]	53	I/O	TTL	4	PC_D[14]	21	I	TTL	—
MCA_D[3]	70	I/O	TTL	4	MCB_D[12]	55	I/O	TTL	4	PC_D[15]	20	I	TTL	—
MCA_D[4]	72	I/O	TTL	4	MCB_D[13]	57	I/O	TTL	4	PC_ENA#	15	I	SHCMOS	—
MCA_D[5]	74	I/O	TTL	4	MCB_D[14]	59	I/O	TTL	4	PC_ENB#	14	I	SHCMOS	—
MCA_D[6]	76	I/O	TTL	4	MCB_D[15]	62	I/O	TTL	4	PC_IOIS16#	37	O	—	4
MCA_D[7]	78	I/O	TTL	4	MCB_CE1N	42	O	—	4	PC_IOR#	13	I	SHCMOS	—
MCA_D[8]	81	I/O	TTL	12	MCB_CE2N	43	O	—	4	PC_IOW#	12	I	SHCMOS	—
MCA_D[9]	84	I/O	TTL	12	MCB_IOIS16	51	I	TTL	—	PC_MCCE1	8	I	SHCMOS	
MCA_D[10]	86	I/O	TTL	12	MCB_IOR#	45	O	—	12	PC_MCCE2	9	I	SHCMOS	
MCA_D[11]	71	I/O	TTL	4	MCB_IOW#	46	O	—	12	PC_MDIR	10	I	SHCMOS	—
MCA_D[12]	73	I/O	TTL	4	MCB_OE#	44	O	—	4	PC_OE0	19	I	SHCMOS	—
MCA_D[13]	75	I/O	TTL	4	MCB_REG#	50	O	—	12	PC_REG#	11	I	SHCMOS	—
MCA_D[14]	77	I/O	TTL	4	MCB_WAIT#	49	I	TTL	—	PC_WAITI#	38	O	—	4
MCA_D[15]	79	I/O	TTL	4	MCB_WE#	48	O	—	12	PC_WE0	18	I	SHCMOS	—
MCA_CE1#	89	O	—	12	MODE_A	2	I	SHCMOS	—	TEST	6	IP	SHCMOS	—
MCA_CE2#	90	O	—	12	MODE_B	4	I	SHCMOS	—	VCC	3	P	—	—
MCA_IOIS16	100	I	TTL	—	MODE_C	7	I	SHCMOS	—	VCC	30	P	—	—
MCA_IOR#	92	O	—	12	OR_IN1	41	I	TTL	—	VCC	47	P	—	—
MCA_IOW#	94	O	—	12	OR_IN2	39	I	TTL	—	VCC	63	P	—	—
MCA_OE#	91	O	—	12	OR_OUT	99	O	—	12	VCC	83	P	—	—
MCA_REGN\#	98	O	—	12	PC_D[0]	36	I	SHCMOS	—	VCC	96	P	—	—
MCA_WAIT#	97	I	TTL	—	PC_D[1]	35	I	SHCMOS	—					
MCA_WE#	95	O	—	12	PC_D[2]	34	I	SHCMOS	—					

Notes:

All VCC pads must be externally connected to VCC supply.
All GND pads must be externally connected to ground.

I	Input pin
O	Output pin
I/O	Bidirectional pin
IUP	Input pin with internal pull-up resistor
OD	Open drain output
SHCMOS	CMOS Schmitt-trigger input

PIN LIST—MODE 4

Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)	Pin Name	Pin No.	Pad Type	Input Type	Drive (mA)
A[0]	7	I	SHCMOS	—	GND	5	G	—	—	PD[0]	92	O	TTL	12
A[1]	8	I	SHCMOS	—	GND	40	G	—	—	PD[1]	91	O	TTL	12
A[2]	9	I	SHCMOS	—	GND	60	G	—	—	PD[2]	89	O	TTL	12
A[3]	10	I	SHCMOS	—	GND	80	G	—	—	PD[3]	86	O	TTL	12
A[4]	11	I	SHCMOS	—	GND	87	G	—	—	PD[4]	85	O	TTL	12
A[5]	12	I	SHCMOS	—	GND	93	G	—	—	PD[5]	84	O	TTL	12
A[6]	13	I	SHCMOS	—	HDCS0#	99	O	—	12	PD[6]	82	O	TTL	12
A[7]	14	I	SHCMOS	—	HDCS1#	98	O	—	12	PD[7]	81	O	TTL	12
A[8]	15	I	SHCMOS	—	IDED7_EN	97	I/O	TTL	12	PE	78	I	TTL	—
A[9]	16	I	SHCMOS	—	IDEENH#	74	O	—	4	PINTR	22	O	—	4
ACKN	75	I	TTL	—	IDEENL#	73	O	—	4	PRT_ADR	100	I	TTL	—
AEN	20	I	SHCMOS	—	INIT#	90	OD	—	12	PRT_SEL#	27	I	SHCMOS	—
AUTOFD#	94	OD	TTL	12	IOCS16	21	I	SHCMOS	—	RESET	17	I	SHCMOS	—
BUSY	79	I	TTL	—	IOR#	18	I	SHCMOS	—	ROW[0]	37	I	SHCMOS	—
CLK14_I	23	I	SHCMOS	—	IOW#	19	I	SHCMOS	—	ROW[1]	38	I	SHCMOS	—
COL[0]	55	O	—	4	KEY_DN#	26	O	—	4	ROW[2]	39	I	TTL	—
COL[1]	56	O	—	4	MODE_A	2	I	SHCMOS	—	ROW[3]	41	I	TTL	—
COL[2]	57	O	—	4	MODE_B	4	I	SHCMOS	—	ROW[4]	42	I	TTL	—
COL[3]	58	O	—	4	P2[1]	48	O	—	4	ROW[5]	43	I	TTL	—
COL[4]	59	O	—	4	P2[2]	49	O	—	4	ROW[6]	44	I	TTL	—
COL[5]	61	O	—	4	P2[3]	50	O	—	4	ROW[7]	45	I	TTL	—
COL[6]	62	O	—	4	P2[4]	51	O	—	4	SLCT	77	I	TTL	—
COL[7]	64	O	—	4	P2[5]	52	O	—	4	SLCTIN#	88	OD	—	12
COL[8]	65	O	—	4	P2[6]	53	O	—	4	STROBE#	95	OD	TTL	12
COL[9]	66	O	—	4	P2[7]	54	O	—	4	TEST	6	IP	SHCMOS	—
COL[10]	67	O	—	4	P3SEL#	46	O	—	4	UCLK_O	24	O	—	4
COL[11]	68	O	—	4	PC_D[0]	36	I/O	SHCMOS	4	VCC	3	P	—	—
COL[12]	69	O	—	4	PC_D[1]	35	I/O	SHCMOS	4	VCC	30	P	—	—
COL[13]	70	O	—	4	PC_D[2]	34	I/O	SHCMOS	4	VCC	47	P	—	—
COL[14]	71	O	—	4	PC_D[3]	33	I/O	SHCMOS	4	VCC	63	P	—	—
COL[15]	72	O	—	4	PC_D[4]	32	I/O	SHCMOS	4	VCC	83	P	—	—
COL_OD#	25	I	SHCMOS	—	PC_D[5]	31	I/O	SHCMOS	4	VCC	96	P	—	—
ERROR#	76	I	TTL	—	PC_D[6]	29	I/O	SHCMOS	4					
GND	1	G	—	—	PC_D[7]	28	I/O	SHCMOS	4					

Notes:

All VCC pads must be externally connected to VCC supply.
All GND pads must be externally connected to ground.

I	Input pin
O	Output pin
I/O	Bidirectional pin
IUP	Input pin with internal pull-up resistor
OD	Open drain output
SHCMOS	CMOS Schmitt-trigger input

PIN DESCRIPTION

Mode 1

Pin Name	Pin No.	Type	Description
PC_A[0]	12	In	Address/Command inputs from PC/CHIP
PC_A[1]	13		
PC_A[2]	14		
PC_A[3]	15		
PC_A[4]	16		
PC_A[5]	17		
PC_A[6]	18		
PC_A[7]	19		
PC_A[8]	20		
PC_A[9]	38		
PC_A[10]	39		
PC_A[11]	41		
PC_A[12]	42		
PC_A[13]	43		
PC_A[14]	44		
PC_A[15]	45		
PC_A[16]	46		
PC_A[17]	48		
PC_A[18]	49		
PC_A[19]	50		
PC_A[20]	7		
PC_A[21]	8		
PC_A[22]	9		
PC_A[23]	10		
PC_A[24]	11		
MC_A[0]	92	Out	Address/Command outputs to memory card
MC_A[1]	91		
MC_A[2]	90		
MC_A[3]	89		
MC_A[4]	88		
MC_A[5]	86		
MC_A[6]	85		
MC_A[7]	84		
MC_A[8]	69		
MC_A[9]	67		
MC_A[10]	65		
MC_A[11]	66		
MC_A[12]	82		
MC_A[13]	71		
MC_A[14]	73		
MC_A[15]	79		
MC_A[16]	77		
MC_A[17]	68		
MC_A[18]	70		
MC_A[19]	72		
MC_A[20]	74		
MC_A[21]	75		
MC_A[22]	76		
MC_A[23]	78		
MC_A[24]	81		

PIN DESCRIPTION **Mode 1 (continued)**

Pin Name	Pin No.	Type	Description
PC_D[0]	37	Bidirectional	Data bus connected to PC/CHIP
PC_D[1]	36		
PC_D[2]	35		
PC_D[3]	34		
PC_D[4]	33		
PC_D[5]	32		
PC_D[6]	31		
PC_D[7]	29		
PC_D[8]	28		
PC_D[9]	27		
PC_D[10]	26		
PC_D[11]	25		
PC_D[12]	24		
PC_D[13]	23		
PC_D[14]	22		
PC_D[15]	21		
MC_D[0]	95	Bidirectional	Data bus connected to memory card
MC_D[1]	98		
MC_D[2]	100		
MC_D[3]	53		
MC_D[4]	55		
MC_D[5]	57		
MC_D[6]	59		
MC_D[7]	62		
MC_D[8]	94		
MC_D[9]	97		
MC_D[10]	99		
MC_D[11]	54		
MC_D[12]	56		
MC_D[13]	58		
MC_D[14]	61		
MC_D[15]	64		
PC_ENA#	51	In	Enable input driven by PC/CHIP
PC_MDIR	52	In	Direction control. Controls direction of data transfer between PC/CHIP and the memory card.

PIN DESCRIPTION — Mode 1 (continued)

Pin Name	Pin No.	Type	Description
TEST	6	IUP	Test input. Has internal pull-up resister. When low, chip enters test mode.*
MODE_A	2	In	Should be connected to GND
MODE_B	4	In	Should be connected to GND
GND	1, 5, 40, 60 80, 87, 93	Supply	Ground pins
VCC	3, 30, 47 63, 83, 96	Supply	Power supply pins

* The chip enters test mode when the test pin is lowered. In test mode, pin 7 becomes TEST_DATA, pin 8 becomes TEST_CLK, and pin 99 becomes TEST_OUT.

Data on the TEST_DATA input becomes latched internally on the first positive transition of TEST_CLK pin after test mode is entered. The value of this internal latch cannot be changed while the test pin remains low regar dless of any signal on the TEST_DATA and TEST_CLK pins.

Depending on the value programmed into the test latch, two different test modes can be selected:

If TEST_DATA was low, then all pins become tri-state including pin 99 (TEST_OUT).

If TEST_DATA was high, then all pins become input except for pin 99 (TEST_OUT). These pins form an XOR chain with the output on pin 99. This XOR chain does not include pin 6 (TEST).

PIN DESCRIPTION

Mode 2

Pin Name	Pin No.	Type	Description
PC_A[0]	14	In	Address inputs from PC/CHIP
PC_A[1]	15		
PC_A[2]	16		
PC_A[3]	17		
PC_A[4]	18		
PC_A[5]	19		
PC_A[6]	20		
PC_A[7]	21		
PC_A[8]	22		
PC_A[9]	23		
PC_A[10]	24		
PC_A[11]	25		
PC_A[12]	27		
PC_A[13]	28		
PC_A[14]	31		
PC_A[15]	32		
PC_A[16]	33		
PC_A[17]	34		
PC_A[18]	35		
PC_A[19]	36		
PC_A[20]	8		
PC_A[21]	9		
PC_A[22]	10		
PC_A[23]	11		
PC_A[24]	12		
PC_A[25]	13		
MCA_A[0]	100	Out	Address outputs to memory card A
MCA_A[1]	98		
MCA_A[2]	97		
MCA_A[3]	95		
MCA_A[4]	94		
MCA_A[5]	92		
MCA_A[6]	91		
MCA_A[7]	90		
MCA_A[8]	73		
MCA_A[9]	71		
MCA_A[10]	69		
MCA_A[11]	70		
MCA_A[12]	88		
MCA_A[13]	75		
MCA_A[14]	77		
MCA_A[15]	85		
MCA_A[16]	82		
MCA_A[17]	72		
MCA_A[18]	74		
MCA_A[19]	76		
MCA_A[20]	78		
MCA_A[21]	79		
MCA_A[22]	81		
MCA_A[23]	84		
MCA_A[24]	86		
MCA_A[25]	89		

PIN DESCRIPTION **Mode 2 (continued)**

Pin Name	Pin No.	Type	Description
MCB_A[0]	68	Out	Address outputs to memory card B
MCB_A[1]	67		
MCB_A[2]	66		
MCB_A[3]	65		
MCB_A[4]	64		
MCB_A[5]	62		
MCB_A[6]	61		
MCB_A[7]	59		
MCB_A[8]	44		
MCB_A[9]	42		
MCB_A[10]	39		
MCB_A[11]	41		
MCB_A[12]	57		
MCB_A[13]	46		
MCB_A[14]	49		
MCB_A[15]	55		
MCB_A[16]	53		
MCB_A[17]	43		
MCB_A[18]	45		
MCB_A[19]	48		
MCB_A[20]	50		
MCB_A[21]	51		
MCB_A[22]	52		
MCB_A[23]	54		
MCB_A[24]	56		
MCB_A[25]	58		
PC_ENAA#	26	In	Address enable input for card A, active low
PC_ENAB#	29	In	Address enable input for card B, active low
OR_IN1	37	In	Input to or gate
OR_IN2	38	In	Input to or gate
OR_OUT	99	Out	Output of or gate
TEST	6	IUP	Test input. Has internal pull-up resister. When low, chip enters test mode.*

PIN DESCRIPTION

Mode 2 (continued)

Pin Name	Pin No.	Type	Description
MODE_A	2	In	Should be connected to GND
MODE_B	4	In	Should be connected to VDD
MODE_C	7	In	Should be connected to GND
GND	1, 5, 40, 60 80, 87, 93	Supply	Ground pins
VCC	3, 30, 47 63, 83, 96	Supply	Power supply pins

* The chip enters test mode when the test pin is lowered. In test mode, pin 7 becomes TEST_DATA, pin 8 becomes TEST_CLK, and pin 99 becomes TEST_OUT.

  Data on the TEST_DATA input becomes latched internally on the first positive transition of TEST_CLK pin after test mode is entered. The value of this internal latch can not be changed while the test pin remains low regardless of any signal on the TEST_DATA and TEST_CLK pins.

  Depending on the value programmed into the test latch, two different test modes can be selected.

  If TEST_DATA was low, then all pins become tri-state including pin 99 (TEST_OUT).

  If TEST_DATA was high, then all pins become input except for pin 99 (TEST_OUT). These pins form an XOR chain in which its output is pin 99. This XOR chain does not include pin 6 (TEST).

PIN DESCRIPTION

Mode 3

Pin Name	Pin No.	Type	Description
PC_D[0]	36	Bidirectional	Data bus. Connects to the PC/CHIP data bus
PC_D[1]	35		
PC_D[2]	34		
PC_D[3]	33		
PC_D[4]	32		
PC_D[5]	31		
PC_D[6]	29		
PC_D[7]	28		
PC_D[8]	27		
PC_D[9]	26		
PC_D[10]	25		
PC_D[11]	24		
PC_D[12]	23		
PC_D[13]	22		
PC_D[14]	21		
PC_D[15]	20		
MCA_D[0]	82	Bidirectional	Data bus. Connects to memory card A
MCA_D[1]	85		
MCA_D[2]	88		
MCA_D[3]	70		
MCA_D[4]	72		
MCA_D[5]	74		
MCA_D[6]	76		
MCA_D[7]	78		
MCA_D[8]	81		
MCA_D[9]	84		
MCA_D[10]	86		
MCA_D[11]	71		
MCA_D[12]	73		
MCA_D[13]	75		
MCA_D[14]	77		
MCA_D[15]	79		
MCB_D[0]	65	Bidirectional	Data bus. Connects to memory card B
MCB_D[1]	67		
MCB_D[2]	69		
MCB_D[3]	52		
MCB_D[4]	54		
MCB_D[5]	56		
MCB_D[6]	58		
MCB_D[7]	61		
MCB_D[8]	64		
MCB_D[9]	66		
MCB_D[10]	68		
MCB_D[11]	53		
MCB_D[12]	55		
MCB_D[13]	57		
MCB_D[14]	59		
MCB_D[15]	62		

PIN DESCRIPTION **Mode 3 (continued)**

Pin Name	Pin No.	Type	Description
PC_IOW#	12	In	Connects to IOW# output of PC/CHIP
PC_IOR#	13	In	Connects to IOR# output of PC/CHIP
PC_OE0#	19	In	Connects to OE0 output of PC/CHIP
PC_REG#	11	In	Connects to REG# output of PC/CHIP
PC_WE0#	18	In	Connects to WE0 output of PC/CHIP
MCA_IOW#	94	Out	Connects to IOW# input of card A
MCA_IOR#	92	Out	Connects to IOR# input of card A
MCA_WE#	95	Out	Connects to WE# input of card A
MCA_OE#	91	Out	Connects to OE3 input of card A
MCA_REG#	98	Out	Connects to REG# input of card A
MCB_IOW#	46	Out	Connects to IOW# input of card B
MCB_IOR#	45	Out	Connects to IOR# input of card B
MCB_WE#	48	Out	Connects to WE# input of card B
MCB_OE#	44	Out	Connects to OE# input of card B
MCB_REG#	50	Out	Connects to REG# input of card B
PC_IOIS16#	37	Out	Connects to IOCS16# input of PC/CHIP
PC_WAIT#	38	Out	Connects to WAIT# input of PC/CHIP
MCA_IOIS16#	100	Out	Connects to IOIS16# output of card A
MCA_WAIT#	97	In	Connects to WAIT# output of card A
MCB_IOIS16#	51	In	Connects to IOIS16# output of card B
MCB_WAIT#	49	In	Connects to WAIT# output of card B
PC_MCCE1#	8	In	Connects to MCCE1# output of PC/CHIP
PC_MCCE2#	9	In	Connects to MCCE2# output of PC/CHIP
MCA_CE1#	89	Out	Connects to CE1# input of card A
MCA_CE2#	90	Out	Connects to CE2# input of card A
MCB_CE1#	42	Out	Connects to CE1# input of card B
MCB_CE2#	43	Out	Connects to CE2# input of card B
PC_ENAA#	15	In	Connects to ENAA# output of PC/CHIP. Enables card A signals
PC_ENAB#	14	In	Connects to ENAB# output of PC/CHIP. Enables card B signals

PIN DESCRIPTION — Mode 3 (continued)

Pin Name	Pin No.	Type	Description
CARDAON#	16	In	Controlled by PC/CHIP. When low along with PC_ENAA#, MCA_CE1# and MCA_CE2# may be activated.
CARDBON#	17	In	Controlled by PC/CHIP. When low along with PC_ENAB#, MCB_CE1#, and MCB_CE2# may be activated.
PC_MDIR	10	In	Connects to the PC/CHIP MDIR output. Controls the direction of the data transfer between PC/CHIP and memory cards.
OR_IN1	41	In	Input to OR gate
OR_IN2	39	In	Input to OR gate
OR_OUT	99	Out	Output of OR gate
TEST	6	IUP	Test input. Has internal pull-up resister. When low, chip enters test mode.*
MODE_A	2	In	Should be connected to GND
MODE_B	4	In	Should be connected to VDD
MODE_C	7	In	Should be connected to VCC
GND	1, 5, 40, 60 80, 87, 93	Supply	Ground pins
VCC	3, 30, 47 63, 83, 96	Supply	Power supply pins

* The chip enters test mode when the test pin is lowered. In test mode, pin 7 becomes TEST_DATA, pin 8 becomes TEST_CLK, and pin 99 becomes TEST_OUT.

Data on the TEST_DATA input becomes latched internally on the first positive transition of TEST_CLK pin after test mode is entered. The value of this internal latch can not be changed while the test pin remains low regardless of any signal on the TEST_DATA and TEST_CLK pins.

Depending on the value programmed into the test latch, two different test modes can be selected.

If TEST_DATA was low, then all pins become tri-state including pin 99 (TEST_OUT).

If TEST_DATA was high, then all pins become input except for pin 99 (TEST_OUT). These pins form an XOR chain in which its output is pin 99. This XOR chain does not include pin 6 (TEST).

PIN DESCRIPTION

Mode 4

Pin Name	Pin No.	Type	Description
PC_D[0]	36	Bidirectional	Data bus. Connects to the PC/CHIP data bus.
PC_D[1]	35		
PC_D[2]	34		
PC_D[3]	33		
PC_D[4]	32		
PC_D[5]	31		
PC_D[6]	29		
PC_D[7]	28		
A[0]	7	In	Address bus. Connects to the PC/CHIP address bus.
A[1]	8		
A[2]	9		
A[3]	10		
A[4]	11		
A[5]	12		
A[6]	13		
A[7]	14		
A[8]	15		
A[9]	16		
PRT_SEL#	27	In	Selects internal ports. Normally is driven by one of the PC/CHIP PS pins.
PRT_ADR	100	In	When low allows PRT_SELN to select the internal ports. When high the address of internal ports will be 37C-37F.
AEN	20	In	Address enable input. Connects to the PC/CHIP AEN output.
IOCS16#	21	In	IOCS16 output from hard disk.
IOR#	18	In	Connects to IOR# output of the PC/CHIP.
IOW#	19	In	Connects to IOW# output of PC/CHIP.
PINTR	22	Out	Parallel port interrupt request.
RESET	17	In	When high, sets the internal ports P0, P1, and P3 to high.
KEY_DN#	26	Out	Goes low when any of ROW inputs are low.
COL[0]	55	Out	Connects to keyboard matrix columns.
COL[1]	56		
COL[2]	57		
COL[3]	58		
COL[4]	59		
COL[5]	61		
COL[6]	62		
COL[7]	64		
COL[8]	65		
COL[9]	66		
COL[10]	67		
COL[11]	68		
COL[12]	69		
COL[13]	70		
COL[14]	71		
COL[15]	72		
COL_OD#	25	In	When low, it causes COL0-15 pins to be open drain outputs (when used as a key board). When high, it becomes a complementary output (when a general purpose output port is needed).

PIN DESCRIPTION

Mode 4 (continued)

Pin Name	Pin No.	Type	Description
ROW[0] ROW[1] ROW[2] ROW[3] ROW[4] ROW[5] ROW[6] ROW[7]	37 38 39 41 42 43 44 45	In	Connects to keyboard matrix rows. External pull-ups are required.
P2[1] P2[2] P2[3] P2[4] P2[5] P2[6] P2[7]	48 49 50 51 52 53 54	Out	Port 2 outputs. P2[0] is used internally to enable UART clock.
P3SEL#	46	Out	Decode for an external output port.
CLK14_I	23	In	14.31818MHz clock input
UCLK_O	24	Out	1.8432MHz clock out
IDED7_EN	97	Out	Enable for external IDED7 buffer.
HDCS0# HDCS1#	99 98	Out	Hard disk chip select.
IDEENH#	74	O	IDE high data buffer enable.
IDEENL#	73	O	IDE low data buffer enable.
PD[0] PD[1] PD[2] PD[3] PD[4] PD[5] PD[6] PD[7]	92 91 89 86 85 84 82 81	Bidirectional	Bidirectional data bus is used to transfer data between the CPU and printer port LPT2.
STROBE#	95	OD	Parallel port strobe.
SLCTIN#	88	OD	Selects printer when low.
INIT#	90	OD	When low it initializes the printer.
AUTOFD#	94	OD	When low printer adds one line feed after printing.
ACK#	75	In	Acknowledge input.
BUSY	79	In	Active high busy input.
PE	78	In	Active high paper end input.
SLCT	77	In	Active high device select input.
ERROR#	76	In	Error input.

PIN DESCRIPTION **Mode 4 (continued)**

Pin Name	Pin No.	Type	Description
TEST	6	IUP	Test input. Has internal pull-up resister. When low, chip enters test mode.*
MODE_A	2	In	Should be connected to VDD.
MODE_B	4	In	Should be connected to GND.
GND	1, 5, 40, 60 80, 87, 93	Supply	Ground pins.
VCC	3, 30, 47 63, 83, 96	Supply	Power supply pins.

* The chip enters into test mode when the test pin is lowered. In test mode, pin 7 becomes TEST_DATA, pin 8 becomes TEST_CLK, and pin 99 becomes TEST_OUT.

  Data on the TEST_DATA input becomes latched internally on the first positive transition of TEST_CLK pin after test mode is entered. The value of this internal latch can not be changed while the test pin remains low rega rdless of any signal on the TEST_DATA and TEST_CLK pins.

  Depending on the value programmed into the test latch, two different test modes can be selected.

  If TEST_DATA was low, then all pins become tri-state including pin 99 (TEST_OUT).

  If TEST_DATA was high, then all pins become input except for pin 99 (TEST_OUT). These pins form an XOR chain in which its output is pin 99. This XOR chain does not include pin 6 (TEST).

Registers

The address decocder consists of four outputs and one 8-bit input port in the F87000. They use pins IOR#, IOW#, and AEN to select these ports. The ports summary are listed in the table below.

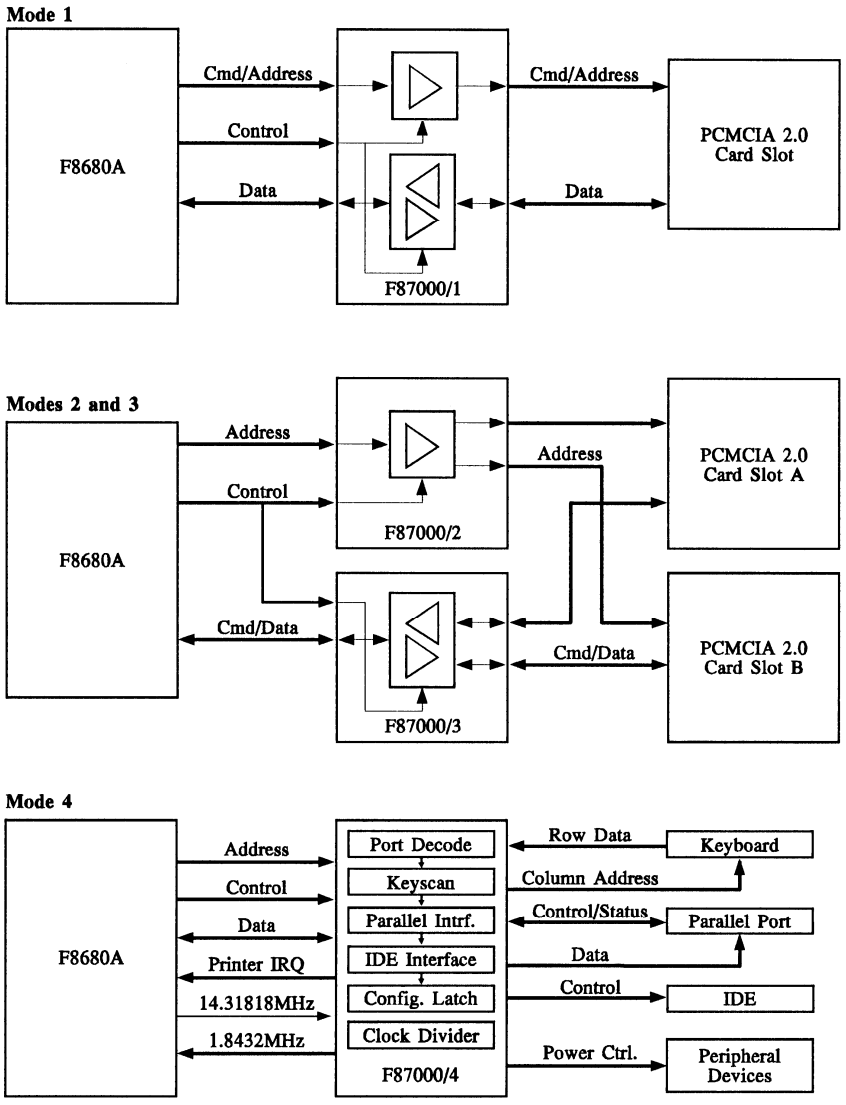
F87000 PORT SUMMARY

Port Address	Port Name	I/O Access	Description
378-37A	Parallel Port	LPT1	This is a bidirectional printer port.
37C	Port 0	Write	This is an output port that drives keyboard outputs COL7-0. A1-0 = 00. This register is set to 1sby RESET.
		Read	This is an input port that is driven by keyboard pins ROW7-0. A1-0 = 10.
37D	Port 1	Write	This is an output port that drives keyboard outputs COL15-8. A1-0 = 01. This register is set to 1s by RESET.
37E	Port 2	Write	This is an output port that drives pins P2[7-1]. Bit 0 of this port is used internally to enable the UART clock. When P2[0] is low UCLK is enabled; when P2[1] = 0, then UCLK output is low. A1-0 = 10. This register is set to 1s by RESET.
37F	Port 3	Write	This is an external output port. When this port is selected, P3SEL# output goes low.

Functional Description

Block diagrams of the F87000 Multi-Mode Perpheral chip for each of its four modes are shown in the figure below.

Any F87000 device can function in any of the four modes as selected by the mode pins strapped to ground (GND).



Functional Block Diagram

MODE 1

This mode is designed to provide the interface for 25-bit address bus and 16-bit data bus between PC/CHIP and memory card. The address pins are interchangeable with PCMCIA control input pins IOR#, IOW#, OE#, WE#, and REG#. Therefore, if the higher address pins are not needed to support the smaller PCMCIA cards, those address pins may be used to buffer the control signals to the PCMCIA cards. The address and data bus are driven low when the memory card is not in use to prevent floating at the memory card inputs and to enable power down of the memory card. See the address buffer and data buffer tables below for the function.

MODE 1 ADDRESS BUFFER

PC_ENAA#	Function
0	PC_A[24-0] → MC_A[24-0]
1	MC_A[24-0] → low

The data bus D[15-0] from the PC/CHIP are buffered before connecting to a PCMCIA card. Signal outputs to the card are forced low when the card is not in use to prevent floating the card's input.

MODE 1 DATA BUFFER

PC_MDIR	PC_ENAA#	Function
x	1	MC_D[15-0] = low PC_D[15-0] = tri-state
0	0	PC_D[15-0] → MC_D[15-0]
1	0	MC_D[15-0] → PC_D[15-0]

MODE 2

This mode is designed to provide the interface for a 26-bit address bus to two independently controlled memory cards. When a memory card is not in use, its address bus will be driven low to prevent floating of the memory card inputs and to enable power down of the memory card. See the address buffer tables below for the function.

MODE 2 ADDRESS BUFFER

PC_ENAA#	PC_ENAB#	Function
0	0	PC_A[25-0] → MCA_A[25-0] PC_A[25-0] → MCB_A[25-0]
0	1	PC_A[25-0] → MCA_A[25-0] MCB_A[25-0] = low
1	0	PC_A[25-0] → MCB_A[25-0] MCA_A[25-0] = low
1	1	MCA_A[25-0] = low MCB_A[25-0] = low

MODE 3

This mode is designed to provide the interface for 16-bit address and control signals bus between the PC/CHIP and two independently controlled memory cards. When a memory card is not in use, its data and control lines are driven low to prevent floating of the memory card inputs and to enable power down of the memory card. See the following four tables for the functions.

MODE 3 DATA BUFFER

PC_MDIR	PC_ENAA#	PC_ENAB#	Function
0	0	0	PC_D[15-0] → MCA_D[15-0] PC_D[15-0] → MCB_D[15-0]
0	0	1	PC_D[15-0] → MCA_D[15-0] MCB_D[15-0] = low
0	1	0	PC_D[15-0] → MCB_D[15-0] MCA_D[15-0] = low
x	1	1	MCA_D[15-0] = low MCB_D[15-0] = low PC_D[15-0] = tri-state
1	0	0	PC_D[15-0] = tri-state MCA_D = tri-state MCB_D = tri-state
1	0	1	MCA_D[15-0] → PC_D[15-0] MCB_D[15-0] = tri-state
1	1	0	MCB_D[15-0] → PC_D[15-0] MCA_D[15-0] = tri-state

MODE 3 BUFFER FOR CONTROL SIGNALS IOW#, IOR#, WE#, REG#, AND OE#

PC_ENAA#	PC_ENAB#	Function
0	0	PC_IOW# →MCA_IOW# PC_IOR#→MCA_IOR# PC_WE0# →MCA_WE# PC_OE0#→MCA_OE# PC_REG# →MCA_REG# PC_IOW# →MCB_IOW# PC_IOR# →MCB_IOR# PC_WE0# →MCB_WE# PC_OE0# →MCB_OE# PC_REG# →MCB_REG#
0	1	PC_IOW# →MCA_IOW# PC_IOR#→MCA_IOR# PC_WE0# →MCA_WE# PC_OE0# →MCA_OE# PC_REG# →MCA_REG# MCB_IOW# = low MCB_IOR# = low MCB_WE# = low MCB_OE# = low MCB_REG# = low
1	0	PC_IOW# →MCB_IOW# PC_IOR# →MCB_IOR# PC_WE# →MCB_WE# PC_OE# →MCB_OE# PC_REG# →MCB_REG# MCA_IOW# - low MCA_IOR# = low MCA_WE# = low MCA_OE# = low MCA_REG# = low
1	1	MCB_IOW# = low MCB_IOR# = low MCB_WE# = low MCB_OE# = low MCB_REG# = low MCA_IOW# = low MCA_IOR# = low MCA_WE# = low MCA_OE# = low MCA_REG# = low

MODE 3 MULTIPLEXER FOR INPUTS WAIT# AND IOIS16#

PC_ENAA#	PC_ENAB#	Function
0	0	PC_ IOIS16# = high PC_WAIT# = high
0	1	MCA_IOIS16# → PC_IOIS16# MCA_WAIT# → PC_WAIT#
1	0	MCB_IOIS16# → PC_IOIS16# MCB_WAIT# → PC_WAIT#
1	1	PC_IOIS16# = high PC_WAIT# = high

MODE 3 BUFFER FOR CONTROL SIGNALS CE1# AND CE2#

CARDAON#	CARDBON#	PC_ENAA#	PC_ENAB#	Function
0	0	0	0	MCA_CE1# = high MCA_CE2# = high MCB_CE1# = high MCB_CE2# = high
0	0	0	1	PC_MCCE1# → MCA_CE1# PC_MCCE2# → MCA_CE2# MCB_CE1# = high MCB_CE2# = high
0	0	1	0	PC_MCCE1# → MCB_CE1# PC_MCCE2# → MCB_CE2# MCA_CE1# = high MCA_CE2# = high
0	0	1	1	MCA_CE1# = high MCA_CE2# = high MCB_CE1# = high MCB_CE2# = high
0	1	0	x	MCB_CE1# = tri-state MCB_CE2# = tri-state PC_MCCE1# → MCA_CE1# PC_MCCE2# → MCA_CE2#
0	1	1	x	MCA_CE1# = high MCA_CE2# = high MCB_CE1# = tri-state MCB_CE2# = tri-state
1	0	x	0	MCA_CE1# = tri-state MCA_CE2# = tri-state PC_MCCE1# → MCB_CE1# PC_MCCE2# → MCB_CE2B#
1	0	x	1	MCA_CE1# = tri-state MCA_CE2# = tri-state MCB_CE1# = high MCB_CE2# = high
1	1	x	x	MCA_CE1# = tri-state MCA_CE2# = tri-state MCB_CE1# = tri-state MCB_CE2# = tri-state

MODE 4

This mode is designed to provide a keyboard scanning, a parallel printer port, programmable output ports, an IDE interface, 1.8MHz clock circuitry, and a 7-bit configuration port plus an external select for port expansion. (For the summary of the port addresses see the section entitled *Registers*.)

Address Decoder

There are four outputs and one 8-bit input port in the F87000. The address decoder uses pins IOR#, IOW#, and AEN to select these ports.

Keyboard Scanning Circuitry

The keyboard scan logic consists of 16 open drain outputs (COL[15-0]) that is connected to the keyboard columns and 8 inputs (ROW[7-0]) that is connected to the keyboard rows. External pull-up resistors must be connected to these inputs. The data on the COL pins is driven by ports 0 and 1. The ROW pins are read by the PC/CHIP through port 2. An 8-input AND gate (output = KEY_DN#) signals the PC/CHIP when any key is pressed. The key scan is idle until there is activity on the keyboard.

Parallel Port

See the section entitled *Registers* section for the port address summary.

Electrical Specifications

The tables in this section describes the operating environment and signal timing of the F87000.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	-0.3 to +7.0	V
V_{IN}/V_{OUT}	Input/output voltage	-0.3 to V_{DD} +0.3	V
I_{IN}	DC input current	±10	mA
T_{STG}	Storage temperature	Plastic: -40 to 125	C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. The function al operation should be restricted to the recommended operating conditions. See the next table.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage	Commercial: 4.75 to 5.25	V
V_{IN}/V_{OUT}	Input/output voltage	0 to V_{DD}	V
T_{OPR}	Operating temperature	Commercial: 0 to 70	C

DC CHARACTERISTICS
V_{DD}= 4.75 to 5.25V, T_A = 0 to 70° C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{IH}	Input high current	$V_{IN} = V_{DD}$	—	—	5	µA
I_{IL}	Input low current	$V_{IN}=V_{SS}$, Normal $V_{IN}=V_{SS}$, Pull-up	 75	 150	5 247	µA
V_{IH} V_T+	Input high voltage	TTL Schmitt	2.0 2.7	 3.0	 3.3	V
V_{IL} V_T-	Input low voltage	TTL Schmitt	 1.7	 2.0	0.8 2.3	V
V_{OH}	Output high voltage	I_{OH} = - 4mA, (4mA outputs) I_{OH} = -12mA, (12mA outputs)*	2.4	—	—	V
V_{OL}	Output low voltage	I_{OL} = 4mA, (4mA outputs) I_{OL} = 12mA, (12mA outputs)*	—	—	0.4	V
I_{OZ}	Tri-state output leakage current	$V_{OUT} = V_{DD}$ or V_{SS}	—	—	5	µA
I_{CC}	Stand-by current	Inputs static, outputs floating	—	—	10	µA
I_{DD}	Functional current	—	—	—	10	mA

* Pins 81, 82, 84-86,88-92, 94, 95, and 97-99 are 12mA outputs when they are in output mode. All o ther outputs are 4mA.

All Characteristics of the F87000 are strictly the result of combinational delays. Therefore, no uni forms are included to indicate timing relationships. Please refer to the F8680A Data Sheet for details on PCM CIA, Memory, and I/O timing.

AC CHARACTERISTICS —MODE 1
V_{DD} = 4.75 to 5.25V, T_A = 0 to 70° C, C_L = 75pF

Symbol	Parameter	Min.	Max.	Unit
T11	PC_A to MC_A	4	19	ns
T13	PC_D to MC_D	4	19	ns
T15	MC_D to PC_D	5	19	ns
T16	PC_ENAA# inactive to MC_A, low	4	20	ns
T17	PC_ENAA# active to MC_A active	4	21	ns
T18	PC_ENAA# inactive to PC_D tri-state	5	20	ns
T19	PC_ENAA# active to PC_D active	5	31	ns
T112	PC_ENAA# inactive to MC_D low	4	20	ns
T113	PC_ENAA# active to MC_D active	4	21	ns

AC CHARACTERISTICS —MODE 2
V_{DD} = 4.75 to 5.25V, T_A = 0 to 70° C, C_L = 75pF

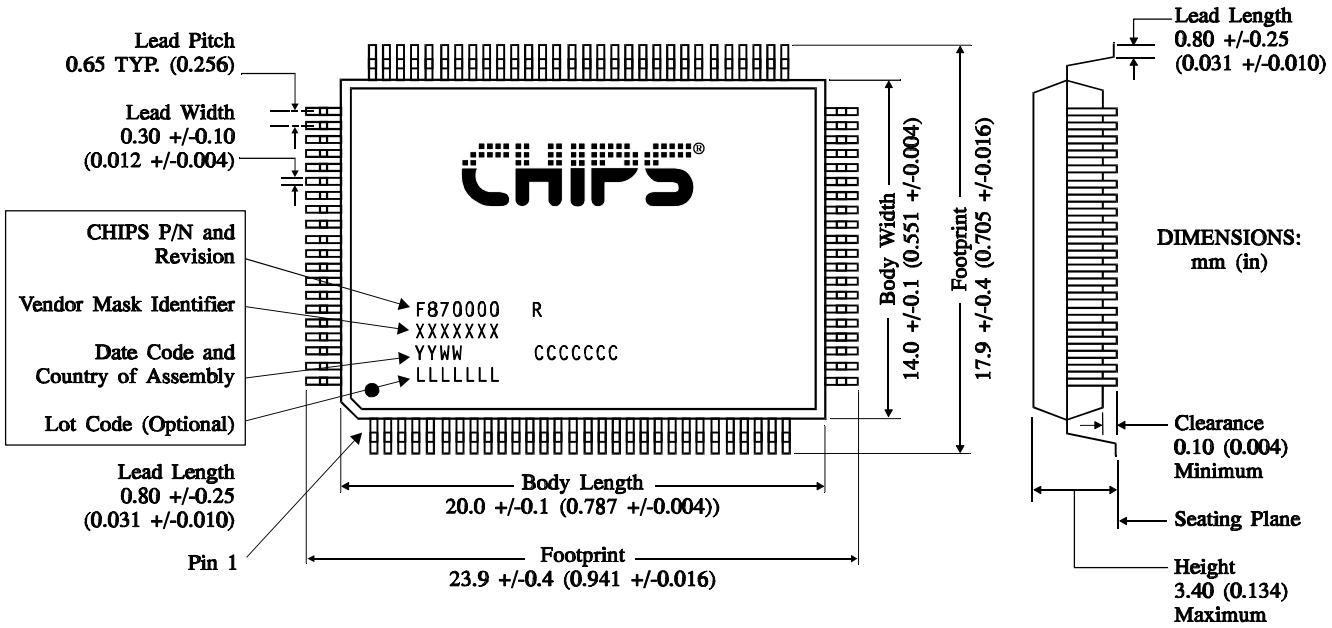
Symbol	Parameter	Min.	Max.	Unit
T21	PC_A to MC_A	4	20	ns
T22	PC_ENAA#/PC_ENAB# inactive to MC_A low T_{PHL}	4	21	ns
T23	PC_ENAA#/PC_ENAB# active to MC_A active T_{PLH}	4	21	ns
T24	OR_OUT	4	15	ns

AC CHARACTERISTICS —MODE 3
V_{DD} = 4.75 to 5.25V, T_A = 0 to 70° C, CL= 75pF

Symbol	Parameter	Min.	Max.	Unit
T30	PC_D to MC_D	4	20	ns
T32	PC_ENAA#/PC_ENAB# inactive to MC_D low	4	22	ns
T33	PC_ENAA#/PC_ENAB# active to MC_D active	5	22	ns
T35	MCA_D to PC_D	5	20	ns
T37	MCB_D to PC_D	5	19	ns
T38	PC_ENAA# inactive to PC_D tri-state	5	22	ns
T39	PC_ENAA# active to PC_D active	6	34	ns
T302	PC_ENAB# inactive to PC_D tri-state	5	22	ns
T303	PC_ENAB# active to PC_D active	9	33	ns
T312	PC_(IOW#, IOR#, WE#, OE#, REG#) to MCA_(IOW#, IOR#, WE#, OE#, REG#)	4	15	ns
T313	PC_(IOW#, IOR#, WE#, OE#, REG#) to MCB_(IOW#, IOR#, WE#, OE#, REG#)	5	20	ns
T316	PC_ENAA# inactive to MCA_(IOW#, IOR#, WE#, OE#, REG#) low	4	16	ns
T317	PC_ENAB# inactive to MCB_(IOW#, IOR#, WE#, OE#, REG#) low	5	21	ns
T318	PC_ENAA# active to MCA_(IOW#, IOR#, WE#, OE#, REG#) high	4	16	ns
T319	PC_ENAB# low to MCB_(IOW#, IOR#, WE#, OE#, REG#) high	6	22	ns
T321	MC_A(IOIS16#,WAIT#) to PC_(IOIS16#, WAIT#)	5	20	ns
T322	PC_ENAA# inactive to PC_(IOIS16#, WAIT#) inactive	6	21	ns
T323	PC_ENAA# active to PC_(IOIS16#, WAIT#) active	6	21	ns
T325	MC_B(IOIS16#,WAIT#) to PC_(IOIS16#, WAIT#)	5	20	ns
T326	PC_ENAB# inactive to PC_(IOIS16#, WAIT#) inactive	6	21	ns
T327	PC_ENAB# active to PC_(IOIS16#, WAIT#) active	6	22	ns
T328	PC_MCCE1/2# to MCA_CE1/2#	4	15	ns
T330	PC_ENAA# inactive to MCA_CE1/2# inactive	5	17	ns
T331	PC_ENAA# active to MCA_CE1/2# active	5	17	ns
T332	CARDAON# inactive to MCA_CE1/2# tri-state	3	13	ns
T333	CARDAON# active to MCA_CE1/2# active	3	13	ns
T336	PC_MCCE1/2# to MCB_CE1/2#	5	19	ns
T338	PC_ENAB# inactive to MCB_CE1/2# inactive	6	21	ns
T339	PC_ENAB# active to MCB_CE1/2# active	6	21	ns
T340	CARDBON# inactive to MCB_CE1/2# tri-state	5	17	ns
T341	CARDBON# low to MCB_CE1/2# low	5	17	ns

Mechanical Specifications

The F87000 is available in a 100-pin PQFP (Plastic Quad Flat Package). The dimensions are shown below.



100-Pin PQFP Package

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