T-52-33-05

CS8285
PEAKsx CHIPSet

Features

- Close-coupled design with SCATsx
- 16KB/32KB Direct-Mapped and two-way set associative cache
- Integrated internal tag RAM and comparators
- Caches AT I/O channel memory as well as system DRAM
- Interfaces to 80386sx
- Latches and buffers for all address lines to/from the AT expansion bus at 24mA
- Buffers commands to/from the expansion bus at 24mA
- 120 pin QFP

The PEAKsx CHIPSet supports high performance 80386sx cache system designs. The highly integrated solution has all the necessary logic needed to complement a 25MHz 386sx motherboard solution with only two VLSI devices. The CHIPSet consists of the low-cost 82C836 Single Chip AT (SCATsx) and the highly integrated 82C835 cache controller. This high level of integration and unified cache allows designers to take full advantage of the 386sx performance at 25MHz.

Figure 1-8. PEAKsx Block Diagram