CS8281 NEATsx™ DATA BOOK

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CS8281 NEATsx Data Book

* 100% IBM PC AT- and OS/2-compatible
* Optimized for use in 16MHz to 20MHz AT-compatible, laptop-compatible, and CMOS industrial control systems
* Supports 80386sx operation with 0.5 to 0.7 waits states at 16MHz with 100ns DRAMs and at 20MHz with 80ns DRAMs
* Supports single bank page mode as well as 2-way and 4-way page interleaved mode with a page interleaved memory controller
* Supports EMS 3.2 (and 4.0 with an external memory mapper) with an integrated Lotus-Intel-Microsoft Expanded Memory Specification (LIM EMS) memory controller
* Contains separate CPU and AT bus clocks
* Uses software configurable command delays, wait states, and memory organization
* Shadows BIOS to improve system performance
* Requires only 24 components plus memory for creation of a 386sx-based system board
* Available as four CMOS 84-pin PLCC or 100-pin PFP components

The CS8281 NEATsx CHIPSet, which is composed of four VSLI devices, is a high-performance, 100%-compatible, enhanced implementation of the control logic used in the IBM PC AT. The flexible architecture of the NEATsx CHIPSet allows it to be used as the basis for any 386sx-compatible system.

The CS8281 NEATsx CHIPSet provides a complete 386sx PC/AT compatible system, requiring only 24 logic components plus memory devices.

The CS8281 NEATsx CHIPSet consists of the 82C811 CPU/bus controller, the 82C812 page/interleave and EMS memory controller, the 82C215 data/address buffer, and the 82C206 integrated peripherals controller (IPC).

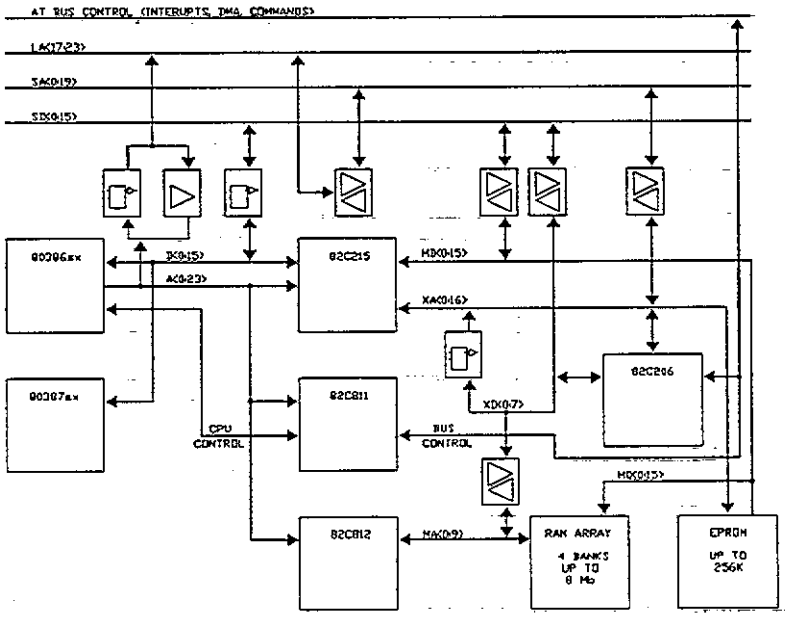

Figure 1 CS8281 Block Diagram

The NEATsx CHIPSet supports a local CPU bus, a 16-bit system memory bus, and the AT buses as shown in the NEATsx system block diagram. The 82C811 provides synchronization and control signals for all buses. The 82C811 also provides an independent AT bus clock and allows for dynamic selection between the processor clock and a user-selectable AT bus clock. Because command delays and wait states are configured by software, peripheral boards are provided with maximum flexibility.

The 82C812 page/interleave and EMS memory controller provides an interleaved memory subsystem design with page mode operation. It supports up to 8MB of DRAM with combinations of 256Kb and 1Mb DRAMs. The processor can operate at 16 MHz with 0.7 wait state memory accesses, using 100 nsec DRAMs. This is possible through a page interleaved memory scheme. A RAM shadowing feature allows faster execution of EPROM stored BIOS code by downloading and executing code from RAM. In a DOS environment, memory above 1MB can be used as EMS memory.

The 82C215 data/address buffer provides buffering and latching between the local CPU address bus and the peripheral address bus. It also provides buffering between the local CPU data bus and the memory data bus. Parity bit generation and error detection logic resides in the 82C215.

The 82C206 integrated peripherals controller is an integral part of the NEATsx CHIPSet. It is described in the 82C206 data book.

System Overview

The CS8281 NEATsx CHIPSet is designed for use in 12-16 MHz 80386 based systems and provides complete support for the IBM PC AT bus. Four buses are supported by the CS8281 NEATsx CHIPSet: the CPU local bus (A and D); the system memory bus (MA and MD); the I/O channel bus (SA and SD); and the X bus (XA and XD). The system memory bus provides an interface between the CPU and the DRAMs and EPROMs controlled by the 82C812. The I/O channel bus refers to the bus supporting the AT-compatible bus adapters which can be either 8- or 16-bit devices. The X bus is the peripheral bus to which the 82C206 IPC and other peripherals are attached in an IBM PC AT.

MANUAL CONVENTIONS

The following conventions are used throughout this document to refer to the configuration and diagnostics registers internal to the 82C811 and 82C812:

* REGnH denotes the internal register of index *n* in hexadecimal notation.
* REGnH<x:y> denotes the bit field from bit *x* to bit *y* with index *n* in hexadecimal notation.

The following two methods are used to indicate an active low signal:

* a bar over the signal name
* an asterisk following the signal name

The following symbols are used to indicate the rising and falling edges of signals:

* ↑ - is a rising edge
* ↓ - is a falling edge

The following terms are used throughout the document:

* MB = megabyte
* Mb = megabit
* KB = kilobyte
* Kb = kilobit

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LIST OF FIGURES

1.0 82C811 Bus Controller

2.0 82C812 Page/Interleave and EMS Memory Controller

1 82C811 Bus Controller

1.1 Features

* Clock generation with software speed selection
* Optional independent AT bus clock
* CPU interface and bus control
* Programmable command delays and wait state generation
* Port B register
* Port B register and NMI logic
* DMA and refresh logic
* Numeric processor interface logic
* Configuration registers

1.2 Functional Description

The 82C811 Bus Controller consists of the following functional subsystems as illustrated in Figure 1.1.

* Reset and shutdown logic
* Clock generation and selection logic
* CPU state machine, AT bus state machine, and bus arbitration logic
* Action Codes generation logic

1.2.1 Reset and Shutdown Logic

Two reset inputs, RESET1* and RESET2* are provided on the 82C811 bus controller. RESET1* is usually connected to the power good signal from the power supply. When RESET1* is active, the 82C811 issues RESET3 and RESET4 for a system reset. Both RESET3 and RESET4 are synchronized with PROCCLK. RESET3 is active for a minimum of 64 PROCCLK cycles, and RESET4 is active as long as RESET1* is active. RESET2* is generated by an 8042 (or 8742) keyboard controller when a warm reset is used. RESET2* activates only RESET3, and this in turn resets the 80386sx CPU. RESET3 is also activated by the 82C811 when a shutdown condition is detected in the CPU. Additionally, a fast reset option is provided in the 82C811 to generate a warm reset without the delays normally associated with the keyboard controller. RESET4 is used to reset the AT bus, the 82C206 IPC, the 8042

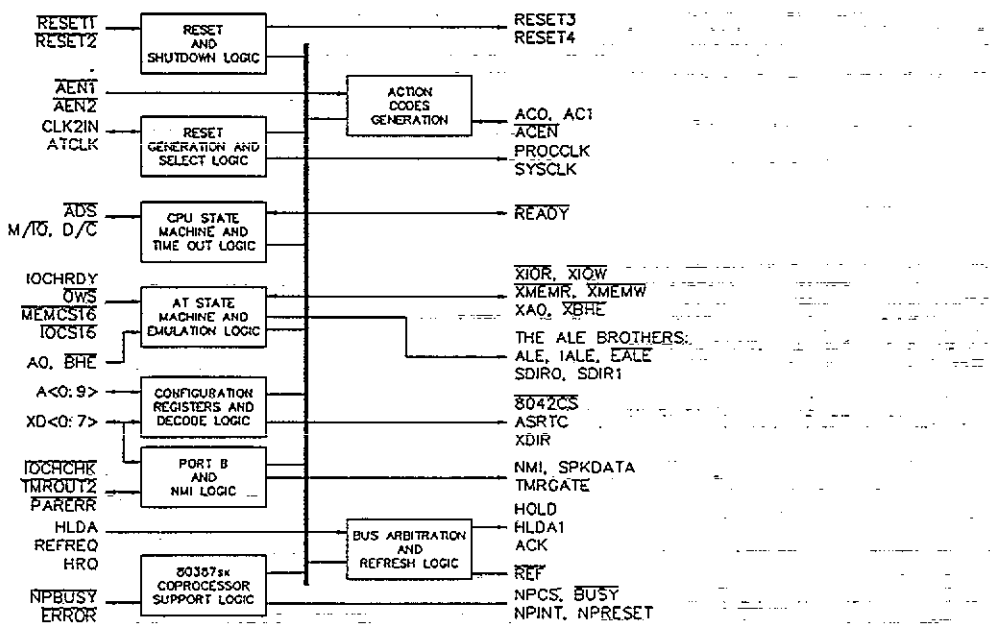


Figure 1.1 82C811 Block Diagram

keyboard controller, and the 82C812 memory controller. RESET3 and RESET4 meet the setup and hold timing requirements of the 80386sx CPU.

1.2.2 Clock Generation and Selection Logic

The 82C811 provides a flexible clock selection scheme as shown in Figure 1.2. The 82C811 has two input clocks, CLK2IN and ATCLK. CLK2IN, which is used generally for the processor clock, is driven by a crystal oscillator. ATCLK, which used for the AT bus clock, may be derived from a crystal or crystal oscillator.

The 82C811 generates the processor clock, PROCCLK, by selecting either the CLK2IN input or the internal bus clock, BCLK. PROCCLK is used internally to drive the CPU state machine as well as driving the 80386sx and 82C812. BCLK, the internal AT bus state machine clock may be generated from one of three sources. A multiple (either $^1/_2$ or $^1/_3$) of CLK2IN may be selected as the source for BCLK. Alternately, ATCLK may be selected as the source. ATCLK is used generally as the source for BCLK when the frequency of CLK2IN is too high or too low. SYSCLK is provided as an AT bus clock. It operates at one half the frequency of BCLK.

When CLK2IN is selected as the source for BCLK, the 82C811 operates in synchronous mode. If ATCLK is used, the 82C811 operates in asynchronous mode. Since an asynchronous AT bus state machine must be synchronized with a CPU state machine at the beginning and end of each cycle, synchronous modes yield slightly higher performance from the AT bus than an asynchronous mode at the same frequency. This performance difference only applies to AT bus cycles and is not apparent to the user.

The BCLK select bits at register RA2 (bits 0 and 1) cannot be modified while register RA0, bit 4 is set to one (PROCCLK = BLCK). This bit must be set to zero (PROCCLK = CLK2IN) while writing to bits zero and one of RA2.

The following clock selections are possible with the 82C811:

* Synchronous Modes
  - PROCCLK = CLK2IN
    BCLK = CLK2IN/2
  - PROCCLK = CLK2IN
    BCLK = CLK2IN/3
  - PROCCLK = BCL
    BCLK = CLK2IN/2
  - PROCCLK = BCLK
    BCLK = CLK2IN/3
  - PROCCLK = BCLK
    BCLK = ATCLK
* Asynchronous Mode
  - PROCCLK = CLK2IN
    BCLK = ATCLK

In most cases, CLK2IN is selected as the source for the processor clock. Other selections for PROCCLK are used when CPU speed must be controlled for compatibility with CPU speed dependent software.

The clock switching circuitry in the 82C811 insures that during clock switching, PROCCLK does not glitch and is not inactive for longer than necessary. No PROCCLK phases are shorter than those of the fastest input clock, and PROCCLK does not remain inactive for more than two periods of the slower clock.

1.3 82C811 Common Operating Modes

This section describes the three most common modes of operation. They are,

* Normal mode
* One-third mode
* External mode

1.3.1 Normal Mode

This mode is enabled by default (without writing to the internal registers of the 82C811). When in normal mode, the following statements are true:

* PROCCLK = CLK2IN
* BCLK = CLK2IN/2
* SYSCLK = CLK2IN/4

Since the CPU state machine clock and the AT bus state machine clock are derived from CLK2IN, this is a synchronous mode. ALE and commands XMEMR*, MEMW*, XIOR*, and XIOW* are issued only for AT bus cycles and not for local cycles. If activated by default, I/O cycles have one command delay, 8-bit AT memory cycles have four wait states, and 16-bit AT memory cycles have one wait state.

Figure 1.2 shows a normal mode AT bus cycle. The cycle starts with IALE being generated at references (1) and (2). AF16* is sampled in the high state at reference (3). Control is then transferred to the AT bus state machine. ALE is generated (4) and is followed by the command (6) after a programmed number of command delays (5). After the wait states occur, the command goes inactive (7) and READY* is generated (8).

1.3.2 One-Third Mode

This is a synchronous mode similar to normal mode with the exception that BCLK is one-third of the processor clock frequency instead of one-half.

* PROCCLK = CLK2IN
* BCLK = CLK2IN/3
* SYSCLK = CLK2IN/6

One-third mode allows operation without an ATCLK crystal at CPU frequencies up to 25 MHz. At 25 MHz, the bus frequency is 8.33 MHz, slightly above the 8 MHz standard.

1.3.3 External Mode

This is an asynchronous mode that is enabled when ATCLK is selected as the source for BCLK. The following clock selections are required in this mode:

* PROCCLK = CLK2IN
* BCLK = ATCLK
* SYSCLK = ATCLK/2

Figure 1.3 shows an external mode cycle. At the start of the cycle, IALE is generated (1) and AF16* is sampled in the inactive (high) state (2). ALE is generated on the first falling edge of SYSCLK (3). After a programmed number of command delays occur, in this

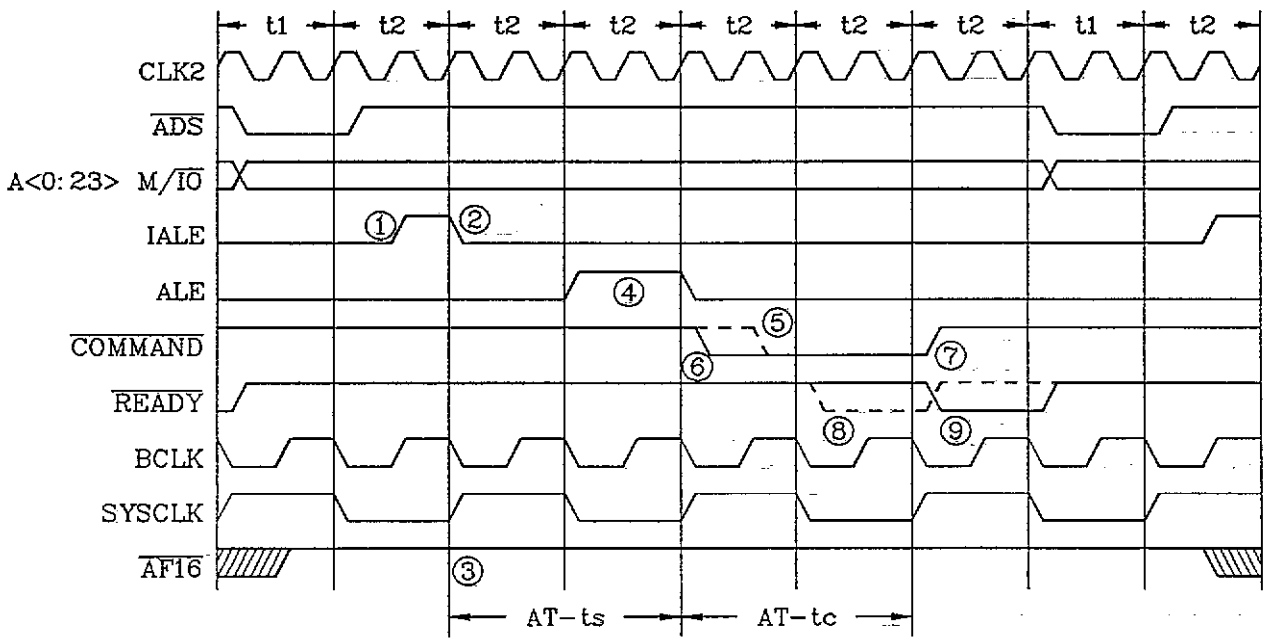


Figure 1.2 Normal Mode AT Bus Cycle

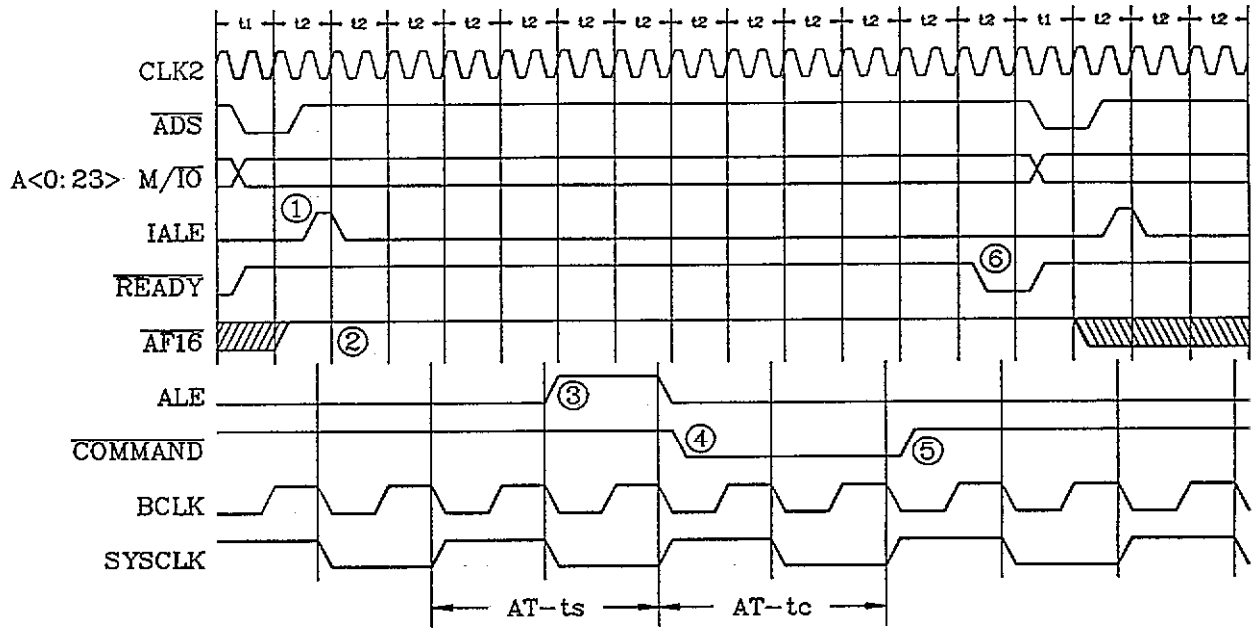


Figure 1.3 External Mode AT Bus Cycle

case zero, the appropriate command is activated (4). After a second series of programmed wait states, the command is deactivated (5). At the beginning of the next processor cycle, READY* is generated to end the cycle (6).

1.4 CPU State Machine, Bus State Machine, and Bus Arbitration

In traditional AT-compatible designs, the bus clock and the CPU clock are the same. In the NEATsx, the CPU and bus do not need to share the same clock. This allows the CPU to run at high frequencies, while the bus runs at an AT-compatible 8 MHz. High-performance systems can be designed that are compatible with standard AT bus peripherals.

1.4.1 CPU State Machine

The CPU state machine monitors ADS*, M/IO*, W/R*, and D/C* from the 80386sx processor to determine a CPU cycle's type and starting point. The state machine generates IALE in response to a new cycle, and generates READY* at the end of an AT bus cycle.

A bus cycle is distinguished from a local cycle by the state of AF16* at the start of the cycle. If AF16* is active at the start of a memory cycle, the 82C811 does not begin an AT bus cycle, but does allow the memory controller to process the cycle. AF16* is only sampled for memory cycles. If AF16* is low at the start of an I/O or interrupt cycle, it is ignored. If the 82C811 is treating a cycle as a local memory cycle and READY* is not active after 128 clock cycles, the 82C811 generates READY*, sets a bus timeout flag in one of its internal registers, and generates an NMI if it is enabled.

1.4.2 AT Bus State Machine

The AT bus state machine starts a bus cycle when the CPU state machine detects that AF16* is inactive. The CPU state machine uses BCLK, which is two times the frequency of the AT system clock, SYSCLK. When ATCLK is selected as the source for BCLK,

the 82C811 performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C811 supports 8- and 16-bit transfers between the processor and 8- or 16-bit memory or I/O devices located on the AT bus. The action code outputs AC0, AC1, and ACEN* (action code enable) are used for bus sizing and 8- and 16-bit bus conversions by the 82C215. The action code outputs are discussed in section 1.6.

At the start of an AT bus cycle, ALE becomes active for one BCLK cycle. During memory cycles, MEMCS16* is sampled on the falling edge of ALE to determine the bus size. During I/O cycles, IOCS16* is sampled and must remain valid for the duration of the cycle. After a programmed number of command delays, the memory or I/O command becomes active. The command signals remain active until the programmed number of wait states are executed. At this point, IOCHRDY is sampled. If IOCHRDY is active, the command becomes inactive after the next SYSCLK cycle. If IOCHRDY is not active, one more wait state is executed and IOCHRDY is sampled again. This process continues indefinitely until IOCHRDY becomes active.

The number of command delays and wait states are programmable under software control. A command delay is a one BCLK delay between the end of ALE and the start of a command. Wait states are additional SYSCLK cycles added to the time a command is active. A command active for zero wait states would be one SYSCLK cycle long. Defaults for command delays and wait states are discussed in section 1.9.1.

1.4.3 Bus Arbitration

The 82C811 controls bus activity and provides arbitration between the CPU, DMA and bus master devices, and DRAM refresh logic. The 82C811 arbitrates between HRQ and REFREQ in a non-preemptive manner. After arbitration, HOLD becomes active. The CPU responds with HLDA, indicating that it has relinquished control. The 82C811 then activates REF* or HLDA1, depending on which device prevailed during arbitration. During a refresh cycle, the refresh logic has control of the bus until REF* becomes

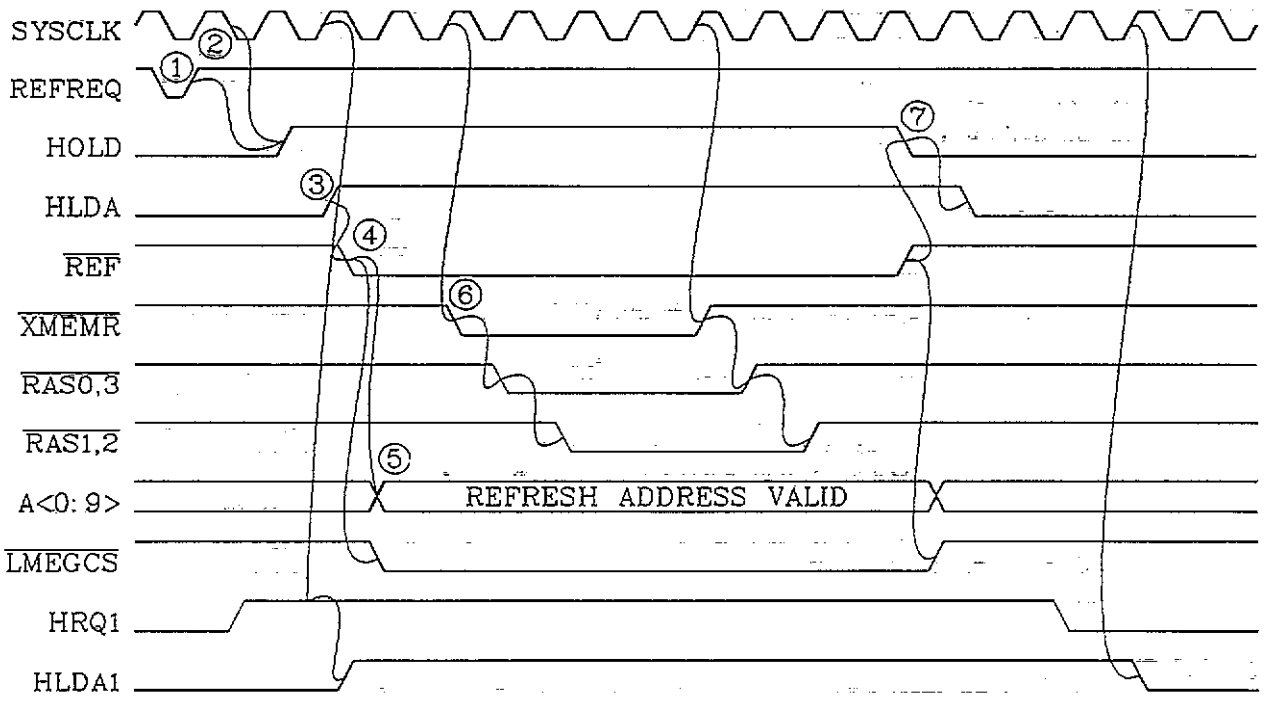


Figure 1.4 Refresh / DMA Cycle

inactive. The 82C811 activates XMEMR* during a refresh cycle after it has provided the refresh address on address lines A0-A9. During a DMA cycle, the DMA controller has control of the bus until HRQ becomes inactive. The 82C811 controls bus sizing and conversion with the action codes. ALE, EALE*, and ACEN* remain active throughout a DMA cycle.

Figure 1.4 shows a Refresh/DMA cycle. The rising edge of REFREQ (1) sets an internal flag in the 82C811. On the first rising edge of SYSCLK, a hold request to the CPU (HOLD) is activated (2). When the CPU finishes with its current activity and releases the bus, it activates hold acknowledge (HLDA) (3). The 82C811 then begins the refresh cycle by activating REF* (4). The 82C812 immediately returns all RAS* lines to their inactive state. After REF* is activated, the 82C811 places the refresh address on A0-A9 (5), and activates XMEMR* (6). After refresh is complete, XMEMR* and REF* are driven to inactive states. HOLD also returns to an inactive state, and the CPU regains control of the bus (7).

If a DMA device requests control of the bus, the 82C811 receives HRQ1 active. After a time during which the DMA is latent, the CPU relinquishes the bus to the requesting device by issuing HLDA1. HLDA1 is active as long as HRQ1 is active. Once the DMA device no longer asserts HRQ1, HLDA1 is no longer asserted by the 82C811 to return control to the processor.

1.5 Additional Hold Time

On the AT bus, certain peripherals require an extended data hold time after the command goes inactive. The 82C811 provides an option to delay READY* by one processor cycle, as shown in Figure 1.2, reference (9). This extends the data hold time on write cycles by two PROCCLK cycles.

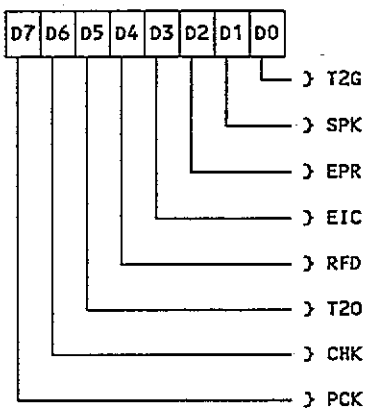
1.6 Action Codes Generation Logic

The AT state machine performs data conversion for CPU accesses to devices not on the CPU or memory bus. The AT bus conversions are performed for 16- to 8-bit read or write operations. 16-bit transfers to or from the CPU are broken into smaller 8-bit AT bus or peripheral bus reads or writes. Action codes are generated (shown in Table 1.2) to control the buffers in the 82C215. The action codes are in response to signals MEMCS16* and IOCS16*.

1.7 Port B and NMI Generation Logic

The 82C811 provides access to Port B defined for the PC/AT as shown in Table 1.1.

Table 1.1 Port B



Bits	R/W	Function
0		T2G - Timer 2 Gate (Speaker)
1		SPK - Speaker Data
2		ERP Enable System Memory Parity Check
3		EIC - Enable I/O Channel Check
4		RFD - Refresh Detect
5		T2O - Timer 2 Out
6		CHK - I/O Channel Check
7		PCK - System Memory Parity Check

The NMI circuitry latches and enables I/O and parity error conditions that generate non-maskable interrupts to the CPU if NMI is enabled. Reading Port B indicates the source of the error condition (CHK and PCK). NMI may be disabled by setting bit 7 of I/O port 70H to one. Setting this bit to zero enables NMI. Although bit 7 of port 70H is contained in the 82C811, port 70H is also used to access the real time clock, which is part of the 82C206.

Table 1.2 Action Codes

Action Codes Enable (ACEN) Generation

Operation	ACEN
DMA/MASTER	0
CPU (local)	1
CPU (AT bus)	0 for write 0 qualified by command for read and interrupt acknowledge cycles
REFRESH	1 qualified by REF

Action Codes for AT-Bus CPU Cycles

AC	Operation
00	16-bit write and 8-bit write (low byte)
01	16-bit read and 8-bit read (low byte)
10	8-bit write (high byte)
11	8-bit read (high byte)

Action Codes for DMA/MASTER Cycles

AC	Operation
00	MD bus tri-stated from the 82C215 for 16-bit and 8-bit (low byte) read/write operations
01	Reserved
10	High memory write MD0-7 to MD8-15
11	High memory read MD8-15 to MD0-7

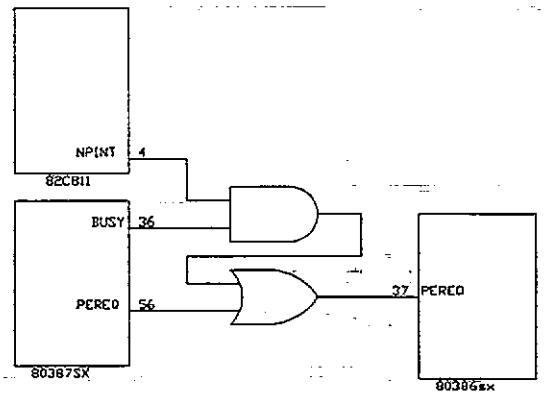


Figure 1.5
Additional Circuitry for Coprocessor

1.8 80387sx Numeric Processor Interface

The 82C811 allows a numeric coprocessor to be connected with a minimum of external logic. Two additional gates are required to force PEREQ to the 80386sx high when NPINT and NPBUSY* are high, as shown in Figure 1.5. These gates are added externally to reduce the pin count on the 82C811. The 82C811 determines if an 80387sx coprocessor is present in the system during power on. If one is detected, bit 7 of register RA2 is set to a one.

While executing a task, the 80387sx issues an NPBUSY* signal to the 82C811. During normal operation, this signal is passed out to the CPU as BUSY*. If during this busy period, a numeric coprocessor error occurs, the ERROR* input to the 82C811 becomes active. This results in the latching of the BUSY* output and assertion of NPINT. Both signals stay active until cleared by an I/O write cycle to address 0F0H or 0F1H. A system reset clears both NPINT and BUSY* latches in the 82C811. The 80387sx is reset through the NPRESET output. This output can be activated by a system reset or by performing a write operation to I/O port 0F1H.

1.9 Configuration Registers

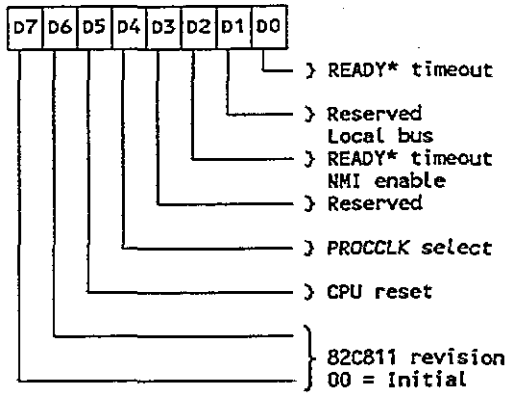
There are three bytes of configuration

registers in the 82C811: RA0, RA1, and RA2. An indexing scheme reduces the number of I/O ports required to access all the registers required for the NEAT CHIPset. Port 22H is used as an indexing register and Port 23H is used as the data register. The index value is placed in port 22H to access a particular register; the data read from or written to that register is located at port 23H. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same register data is being accessed again. All reserved bits are set to zero by default. When written to, the reserved bits must be set to zero, unless otherwise specified. The three registers are listed below.

Register Number	Register Name	Index
RA0	PROCCLK Select	60H
RA1	Command Delay	61H
RA2	Wait States	62H

Table 1.3 PROCCLK Select

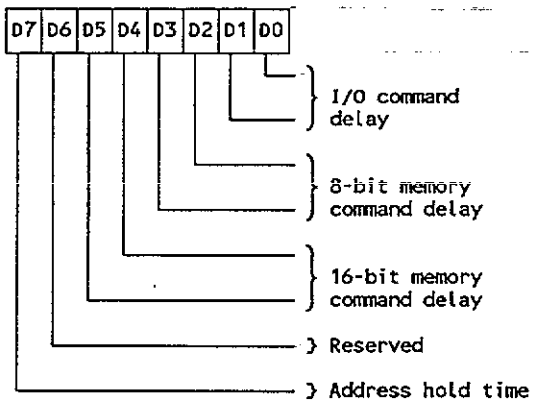
PROCCLK Select Register (RA0)
Index Register Port: 22H
Data Register Port: 23H
Index: 60H



Bits	Function
0	Local Bus READY* Timeout. A one indicates that READY* was not generated within 128 clock cycles after starting a local cycle.
1	Reserved*
2	Local Bus READY* Timeout NMI Enable. A one enables NMI generation and a zero disables it. The default is zero.
3	Reserved*
4	Processor Clock Select. A one selects PROCCLK = BCLK. A zero selects PROCCLK = CLK2IN. The default is zero.
5	Fast CPU Reset. This bit changing from zero to one generates a 16 cycle PROCCLK RESET3 pulse.
6,7	82C811 Revision Number. 00 is the initial release.

Table 1.4 Command Delay

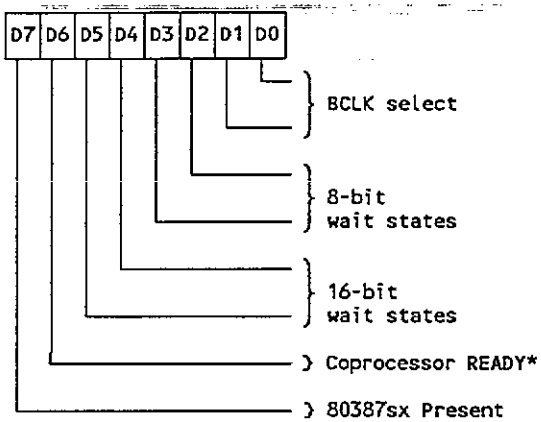
Command Delay Register (RA1)
Index Register Port: 22H
Data Register Port: 23H
Index: 61H



Bits	Function
0,1	AT bus I/O Cycle Command Delay. Specifies between 0 and 3 BCLK cycle command delays for AT cycles. Default is one. Delays are measured from ALE.
2,3	AT bus 8-bit Memory Command Delay. Specifies between 0 and 3 BCLK cycle command delays for 8-bit memory cycles. Default is one.
4,5	AT bus 16-bit Memory Command Delay. Specifies between 0 and 3 BCLK cycle command delays for 16-bit memory cycles. Default is zero.
6	Reserved. Default is one.
7	Address Hold Time Delay. A one enables extra address bus hold time. Default is zero.

Table 1.5 Wait States

Wait States Register (RA2)
Index Register Port: 22H
Data Register Port: 23H
Index: 62H



Bits	Function	
0-1	Bus Clock (BCLK) Select	
	1,0	BCLK Selection
	0 0	BCLK = CLK2IN/2 (Default)
	0 1	BCLK = CLK2IN/3
	1 0	BCLK = ATCLK
	1 1	Reserved
2-3	8-bit AT Cycle Wait States	
	3,2	Wait States
	0 0	2 Wait States
	0 1	3 Wait States
	1 0	4 Wait States
	1 1	5 Wait States (Default)
4-5	16-bit AT Cycle Wait States	
	5,4	Wait States
	0 0	0 Wait States
	0 1	1 Wait States
	1 0	2 Wait States
	1 1	3 Wait States (Default)
6	Coprocessor -READY. Set to one.	
7	80387sx Present (R/O). If set to one, the 82C811 has detected the presence of an 80387sx in the system.	

Table 1.6 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25°	85°	C
Storage Temperature	T_{STG}	-40°	125°	C

NOTE:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

Table 1.7 82C811 Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0°	70°	C

Table 1.8 82C811 DC Characteristics
(T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V
Output Low Voltage	V_{OL}	-	0.45	V
I_{OL} = 6mA (SYSCLK, RESET3, RESET4, ATCLK2, HOLD, BHE*, NMI, IALE, ALE, EALE*, HLDA1, 8042CS*, ASRTC*, XMEMR*, XMEMW*, XIOR*, XIOW*, -XBHE*, XAO, XD<0:7>, SPKDATA, INTA*, SDIR<0:1>, ACEN, AC<0:1>, BUSY*, NPINT, NPRESET, TMRGATE)				
I_{OL} = 12mA (PROCCLK, READY*)				
I_{OL} = 16mA (REF*)				
Output High Voltage	V_{OH}	2.4	-	V
I_{OH} = 6mA (SYSCLK, RESET3, RESET4, ATCLK2, HOLD, BHE*, NMI, IALE, ALE, EALE*, HLDA1, 8042CS*, ASRTC, XMEMR*, XMEMW*, XIOR*, XIOW*, XBHE*, XAO, XD<0:7>, SPKDATA, INTA*, SDIR<0:1>, ACEN, AC<0:1>, BUSY*, NPINT, NPRESET, TMRGATE)				
I_{OL} = 12mA (PROCCLK, READY*)				
I_{OL} = 16mA (REF*)				
Input Current $0<V_{IN}<V_{CC}$	I_{IL}	-	±10	uA
Power Supply Current @ 16MHz	I_{CC}	-	50	mA
@ 20MHz	I_{CC}	-	60	mA
Output High Impedance Leakage Current $0.45<V_{OUT}<V_{CC}$	I_{OZ1}		±10	uA
PROCCLK Output Low Voltage @ I_{OL} = 5mA	V_{OLC}	-	0.45	V
PROCCLK Output High Voltage @ I_{OH} = -1mA	V_{OHC}	4.0	-	V
Input Capacitance F_C = 1MHz (Note 1)	C_{IN}		10	pF
Output or I/O Capacitance F_C = 1MHz (Note 1)	C_{OUT}		12	pF
Output Leakage Current $0.45 \leq V_{OUT} \leq V_{CC}$	I_{LO}		±15	uA

NOTE 1:

Not tested

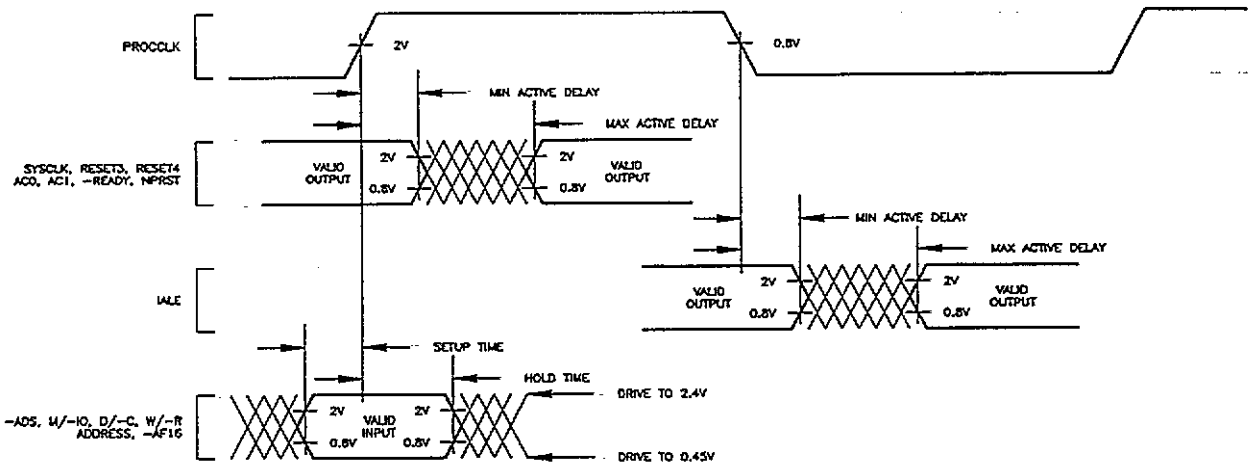


Figure 1.6 82C811 Setup, Hold and Active Delay Timings Relative to PROCCLK

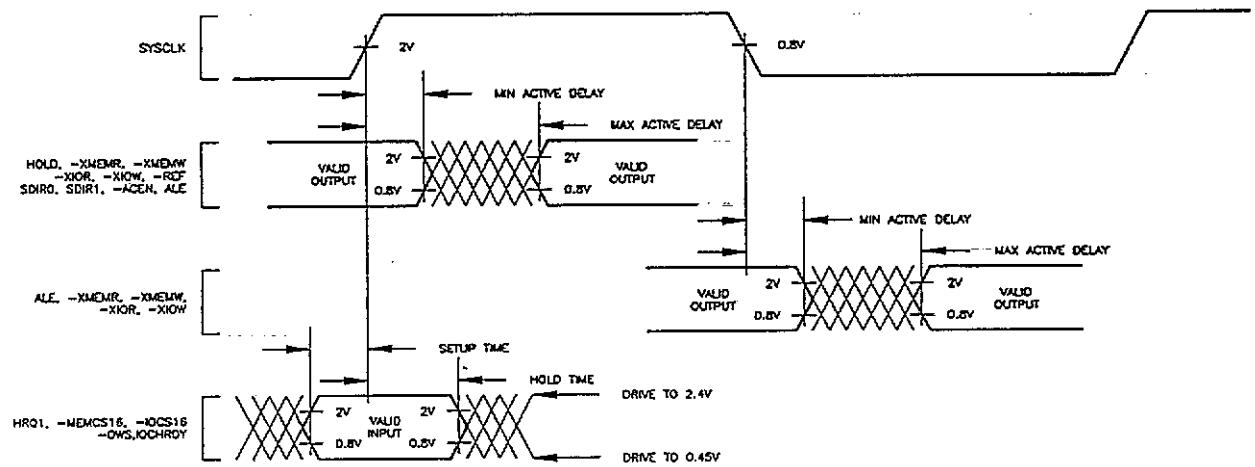


Figure 1.7 82C811 Setup, Hold and Active Delay Timings Relative to SYSCLK

Table 1.9 82C811-16, 82C812-20 AC Characteristics
(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; C_L = 75pF)
(Min and max values in nanoseconds.)

Symbol	Description	16 MHz		20 MHz	
		Minimum	Maximum	Minimum	Maximum
t1	ALE active delay from SYSCLK ↓	-10	10	-10	10
t2	ALE inactive delay from SYSCLK ↑	-10	12	-10	12
t3	Command active delay from SYSCLK	-10	16	-10	16
t4	Command inactive delay from SYSCLK	-10	12	-10	12
t5	EALE* active delay from SYSCLK ↓	0	35	0	30
t6	MEMCS16* setup time to SYSCLK ↑	10	-	10	-
t7	MEMCS16* hold time to SYSCLK ↑	4	-	4	-
t8	IOCS16* setup time to SYSCLK ↓	10	-	10	-
t9	IOCS16* hold time to SYSCLK ↓	10	-	10	-
t10	OWS* setup time to SYSCLK ↑	9	-	9	-
t11	OWS* hold time to SYSCLK ↑	4	-	4	-
t12	IOCHRDY setup time to SYSCLK ↑	11	-	11	-
t13	IOCHRDY hold time to SYSCLK ↑	4	-	4	-
t14	IALE active delay from PROCCLK ↓	1	15	1	12
t15	IALE inactive delay from PROCCLK ↓	1	15	1	12
t16	AF16* setup time to PROCCLK ↑	15	-	15	-
t17	AF16* hold time to PROCCLK ↑	11	-	11	-
t18	READY* input setup time to PROCCLK ↑	25	-	20	-
t19	READY* input hold time to PROCCLK ↑	10	-	10	-
t20	RESET3 active delay from PROCCLK ↑	0	17	0	15
t21	RESET3 inactive delay from PROCCLK ↑	4	17	4	12
t22	RESET4 active delay from PROCCLK ↑	3	17	0	15
t23	RESET4 inactive delay from PROCCLK ↑	4	17	4	12
t24	SDIR1-0 active delay from SYSCLK ↓	0	40	0	40
t25	SDIR1-0 inactive delay from SYSCLK ↑	1	21	1	20
t26	ACEN* active delay from SYSCLK ↓	0	30	0	30
t27	ACEN* inactive delay from SYSCLK ↑	0	21	0	20
t32	ACO active delay from PROCCLK ↑	5	35	5	35
t33	ACO inactive delay from PROCCLK ↑	5	35	5	35
t34	AC1 active delay from PROCCLK ↑	5	35	5	35
t35	AC1 active delay from PROCCLK ↑	5	35	5	35
t38	HOLD active delay from SYSCLK ↓	-10	50	-10	50
t39	HOLD inactive delay from SYSCLK ↑	-10	50	-10	50
t40	REF* delay from HLDA	0	50	0	50
t43	REF* inactive delay from SYSCLK ↑	0	25	0	25
t44	XMEMR* active from SYSCLK ↑	-10	16	-10	16
t45	XMEMR* inactive from SYSCLK ↑	-10	12	-10	12
t46	HRQ1 setup to SYSCLK ↑	10	-	10	-
t47	HRQ1 hold time to SYSCLK ↑	4	-	4	
t49	HLDA1 active delay from HLDA ↑	0	40	0	40

Table 1.9 82C811-16, 82C812-20 AC Characteristics (continued)
(T_A = 0°C to 70°C; V_{CC} = 5V ±5%)
(Min and max values in nanoseconds.)

Symbol	Description	16 MHz Minimum	16 MHz Maximum	20 MHz Minimum	20 MHz Maximum
t51	HLDA1 inactive delay from HLDA ↓	0	40	0	40
t54	NPINT delay from NPBUSY*, ERROR* low	0	36	0	36
t55	NPINT inactive delay from ERROR* ↑	0	36	0	36
t57	ERROR* hold time with respect to NPBUSY* ↑	0	-	0	-
t58	ERROR* setup time to NPBUSY* ↑	3	-	3	-
t60	BUSY* active delay from NPBUSY* ↓	0	18	8	14
t61	BUSY* inactive delay from NPBUSY* ↑	0	23	8	23
t62	BUSY* delay from IOW*	-10	20	-10	20
t63	NPRST active delay from PROCCLK	-10	27	-10	27
t64	NPRST inactive delay from PROCCLK	-10	27	-10	27
t65	READY inactive delay from PROCCLK ↑	6	25	6	25
t66	Address setup to PROCCLK ↑	19	-	19	-
t67	Address hold from PROCCLK ↑	17	-	17	-
t68	CLK2IN ↑ to PROCCLK ↓ delay	0	16	0	16
t69	CLK2IN ↓ to PROCCLK ↑ delay	0	16	0	16
t70	PROCCLK ↑ to SYSCLK ↑ normal mode delay	0	16	0	16
t71	PROCCLK ↑ to SYSCLK ↓ normal mode delay	0	16	0	16
t72	PROCCLK ↑ to SYSCLK ↑ one-third mode delay	0	16	0	16
t73	PROCCLK ↑ to SYSCLK ↓ one-third mode delay	0	16	0	16
t74	ATCLK ↓ to PROCCLK ↑ delay	0	16	0	16
t75	ATCLK ↑ to PROCCLK ↓ delay	0	16	0	16
t76	ATCLK ↓ to SYSCLK ↑ delay	0	32	0	32
t77	ATCLK ↓ to SYSCLK ↓ delay	0	32	0	32
t80	ADS setup to PROCCLK ↑	19	-	19	-
t81	ADS hold from PROCCLK ↑	6	-	6	-
t82	M/IO*, D/C*, W/R* setup to PROCCLK ↑	19	-	19	-
t83	M/IO*, D/C*, W/R* hold to PROCCLK ↑	9	-	9	-
t84	READY active delay from PROCCLK ↑	12	30	12	30

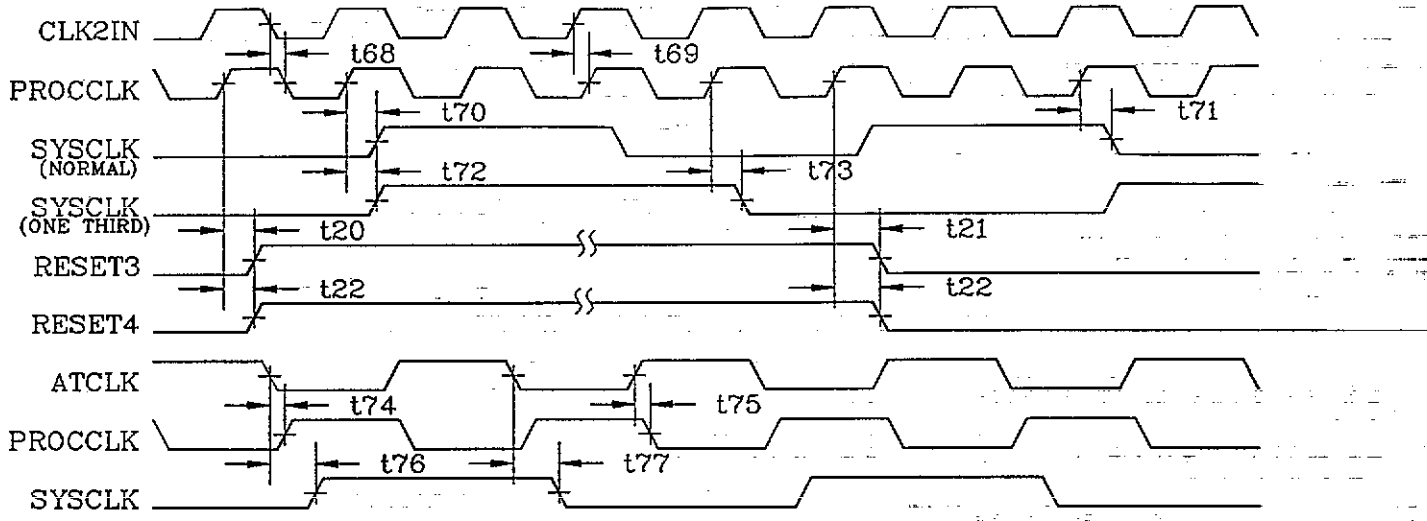


Figure 1.9 Clock/Reset Timing

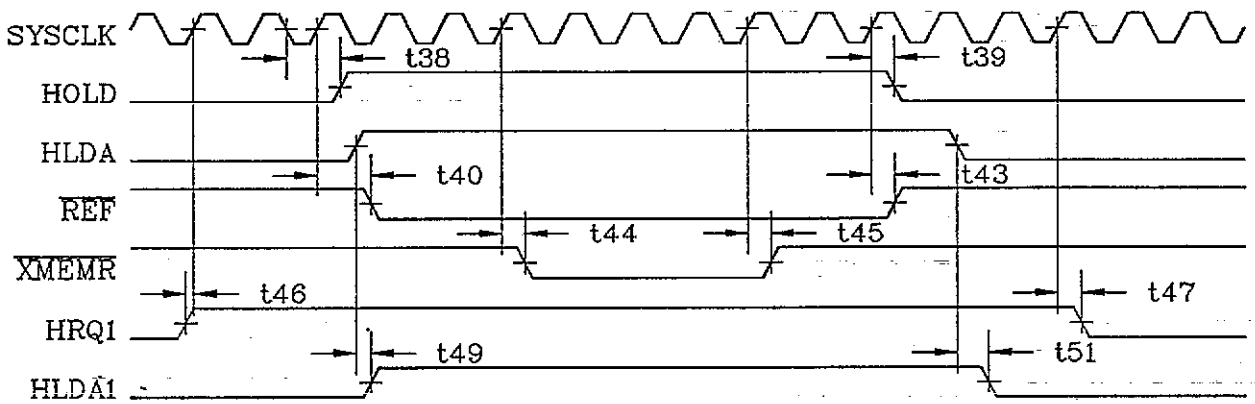


Figure 1.10 Refresh/DMA Timing

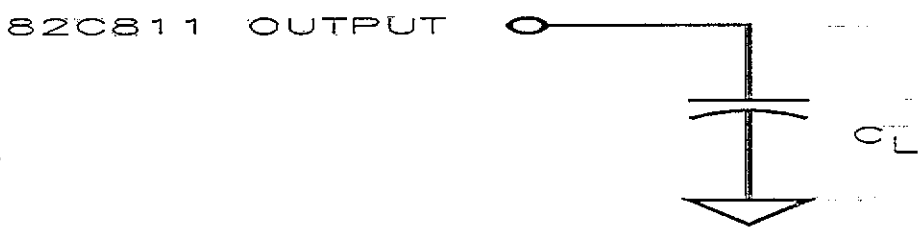


Figure 1.8 82C811 Test Load

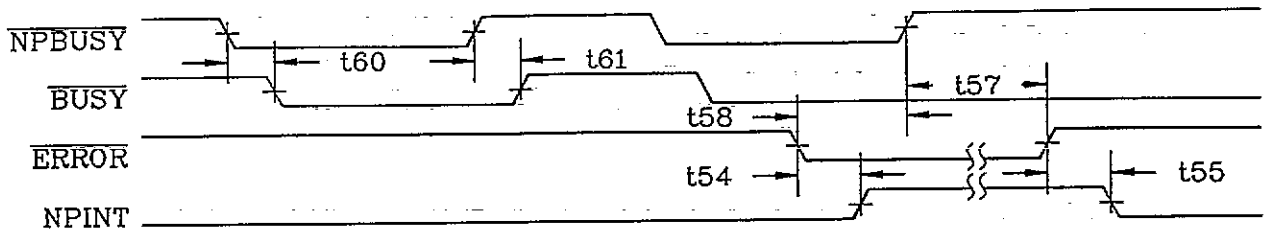


Figure 1.11 Coprocessor Timing

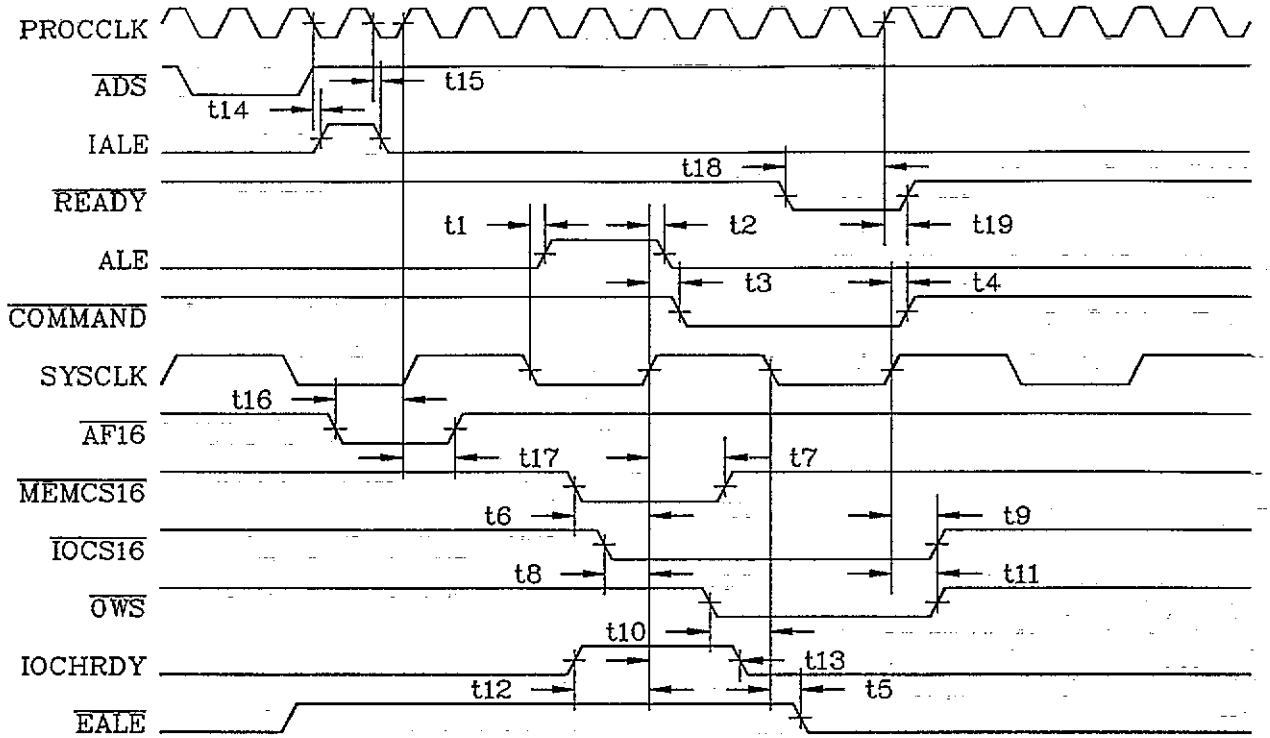


Figure 1.12 Bus Timing

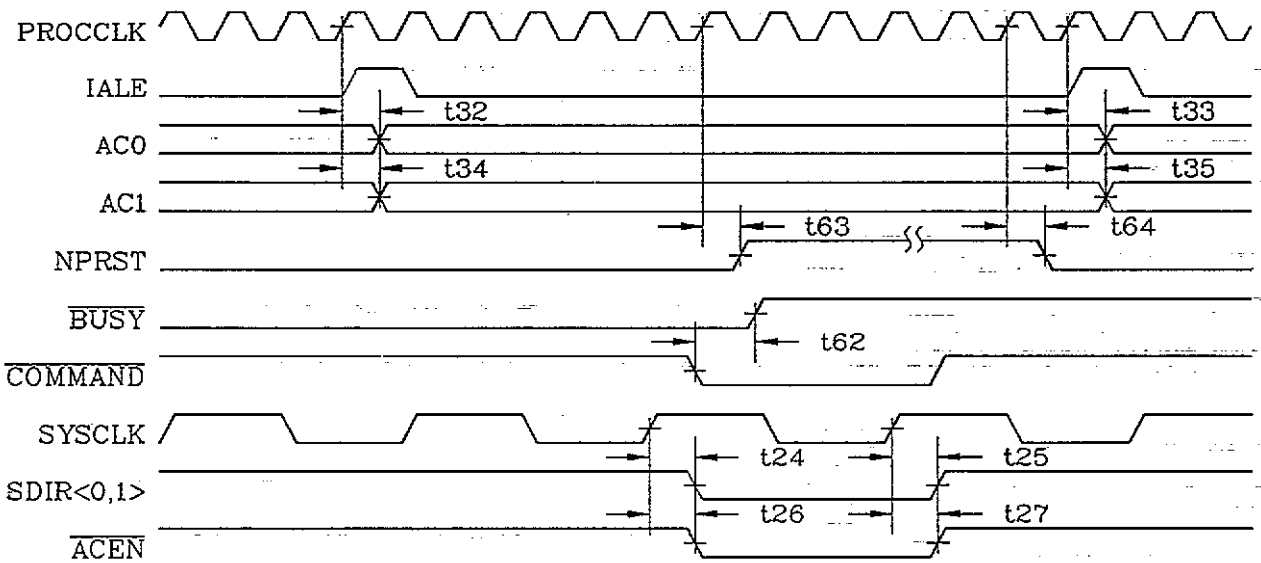


Figure 1.13 Control Timing

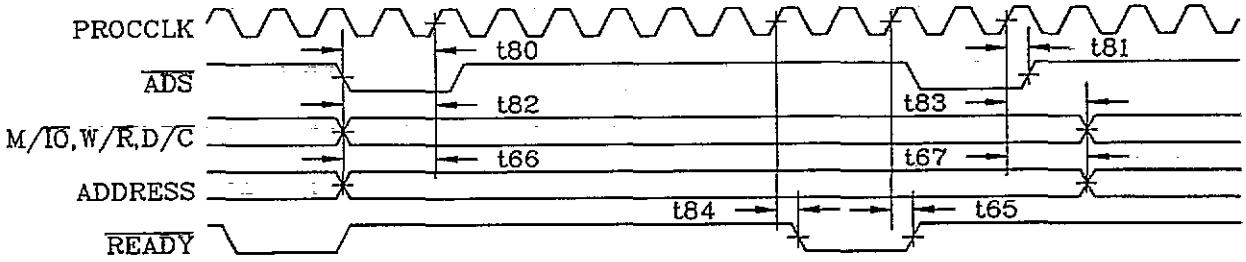


Figure 1.14 Miscellaneous Timing

Table 1.10 82C811 Pin Descriptions

Signal Type	Number	Name	I/O	Description
Clock	5	CLK2INI	I	Processor clock (PROCCLK) input from a crystal oscillator.
Clock	2	PROCCLK	O	PROCESSOR CLOCK output for the 80386sx and the 82C812. It is derived from CLK2IN. It can also be programmed to be derived from ATCLK. This pin has 12mA drive capability.
Clock	76	ATCLK1	I	Optional clock source for AT bus clock. ATCLK1 may be driven by a crystal oscillator or a crystal. This input is only used for external mode. If a clock source is not connected, ATCLK1 should be tied low.
Clock	81	ATCLK2	O	AT bus clock output. If a crystal is to be used as the clock source when the 82C811 is in external mode, The crystal should be connected between ATCLK1 and ATCLK2. A 10 ohm resistor should be used in series with ATCLK2. If an oscillator is used to drive ATCLK1, ATCLK2 should be left open. This pin has 6mA drive capability.
Clock	83	SYSCLK	O	AT bus clock output. SYSCLK is one half of the frequency of BCLK. It should be buffered before driving the bus. This pin has 6mA drive capability.
Control	13	RESET1*	I	RESET1 is an active low input generated by the "power good" signal of the power supply. When low, it activates RESET3 and RESET4.
Control	51	RESET2*	I	RESET2 is an active low input generated from the keyboard controller for a "warm reset". It forces a CPU reset by activating RESET3.
Control	38	RESET4	O	RESET4 is an active high output used to reset the AT bus, 82C206 IPC, 8042 keyboard controller, 82C812 memory controller. It is synchronized with the processor clock. This pin has 6mA drive capability.
Control	50	RESET3	O	RESET3 is an active high output to the 80386sx. It is active when RESET1* or RESET2* are active. It is also activated when a shut-down condition in the CPU is detected. This pin has 6mA drive capability.
CPU Interface	71	READY*	I/O	READY is an open collector output to the 80386sx CPU and 82C812 memory controller. This is an active low signal indicating the end of a cycle. For local memory and coprocessor cycles, READY is an input. READY should be pulled up externally with a 1k ohm resistor. This pin has 12mA drive capability.
CPU Interface	8	ADS*	I	ADDRESS STROBE input from 80386sx CPU. Indicates that CPU is starting a new cycle.
CPU Interface	79	D/C*	I	DATA/CONTROL input from CPU. High for data transfer cycles, low for control cycles such as HALT or code fetches.
CPU Interface	80	W/R*	I	WRITE/READ input from CPU. High for write cycles, low for read cycles.
CPU Interface	72	M/IO*	I	MEMORY INPUT/OUTPUT input from CPU. High for memory cycles, low for I/O cycles. A pull up resistor of 10K Ohms is required.

Table 1.10 82C811 Pin Descriptions (continued)

Signal Type	Number	Name	I/O	Description
CPU Interface	55	HOLD	O	CPU HOLD REQUEST active high output to the CPU. It is active during DMA, Master and Refresh cycles. This pin has 6mA drive capability.
CPU Interface	37	HLDA	I	HOLD ACKNOWLEDGE active high input from CPU. It is active when the CPU has relinquished control of the bus.
Address	49	BHE*	I/O	BYTE HIGH ENABLE is an active low signal indicating data transfer on the bits 8 - 15 of the data bus. It is an input for CPU cycles, and an output for DMA and Master cycles. A pull up resistor of 10K Ohms is required. This pin has 6mA drive capability.
CPU Interface	39	NMI	O	NON MASKABLE INTERRUPT is an active high output to the NMI pin of the CPU and is generated by the 82C811 to invoke a non-maskable interrupt. This pin has 6mA drive capability.
CPU Interface	41	IALE	O	INTERNAL ADDRESS LATCH ENABLE is an active high output used to latch addresses in the 82C215 at the start of CPU cycles. It is not issued for halt cycles. This pin has 6mA drive capability.
I/O Channel Interface	31	IOCHRDY	I	I/O CHANNEL READY is an asynchronous, active high input from the AT bus. It is driven low by devices on the AT bus to extend the current cycle. Wait states will be inserted as long as IOCHRDY is low. A 51 ohm series damping resistor at the AT bus connector is recommended to limit overshoot. A 1K ohm pull up resistor is required.
I/O Channel Interface	30	IOCHCK*	I	I/O CHANNEL CHECK is an active low input from the AT bus causing an NMI to be generated. A 10K Ohm pull up resistor is required.
I/O Channel Interface	11	PARERR*	I	PARITY ERROR is an active low input from the 82C215 which causes an NMI if enabled. It indicates a parity error in local memory.
I/O Channel Interface	44	ALE	O	ADDRESS LATCH ENABLE is an active high output to the AT bus. It controls the address latches driving the AT bus. This signal should be buffered to drive the AT bus. This pin has 6mA drive capability.
I/O Channel Interface	73	EALE*	O	EARLY ADDRESS LATCH ENABLE is an active low output used to latch the LA17-LA23 address lines. It allows address lines LA17-LA23 to change after the first bus Tc state. This pin has 6mA drive capability.
DMA Interface	40	HLDA1	O	HOLD ACKNOWLEDGE 1 is an active high output indicating that a bus cycle has been granted in response to HOLD REQUEST 1. This pin has 6mA drive capability.
DMA Interface	26	HRQ	I	HOLD REQUEST is an active high input from a DMA device or bus master. For a NEAT design, this pin should be connected to the HRQ pin of the 82C206.
DMA Interface	27	AEN1*	I	ADDRESS ENABLE 1 is an active low input from the 8 bit DMA controller.
DMA Interface	28	AEN2*	I	ADDRESS ENABLE 2 is an active low input from the 16 bit DMA controller.

Table 1.10 82C811 Pin Descriptions (continued)

Signal Type	Number	Name	I/O	Description
DMA Interface	48	ROMCS*	I	ROM CHIP SELECT is an active low input from the 82C812. It is used to disable parity checks for local ROM cycles.
Bus Inputs	12	MEMCS16*	I	MEMORY CHIP SELECT 16 is an active low input from the AT bus. It is pulled low by a 16 bit memory device to indicated it is capable of 16 bit transfers. A pull up resistor of 330 Ohms is required.
Bus Inputs	33	IOCS16*	I	I/O CHANNEL SELECT 16 is an active low input from the AT bus. It is pulled low by a 16 bit I/O device to indicated that the device is capable of 16 bit transfers A pull up resistor of 330 Ohms is required.
Bus Inputs	69	OWS*	I	ZERO WAIT STATES is an active low input from the AT bus. High speed devices on the AT bus may pull this line low to cause a zero wait state cycle. It requires a 330 Ohms pull up resistor.
Device Decode	35	8042CS*	O	8042 CHIP SELECT is an active low address decode for the keyboard controller chip select. This pin has 6mA drive capability.
Device Decode	82	ASRTC	O	Real Time Clock Address Strobe. This is an active high output generally connected to the AS pin of the 82C206. It is active during I/O writes to port 070H. This pin has 6mA drive capability.
Refresh	52	REFREQ	I	REFRESH REQUEST is an active high input initiating a DRAM refresh sequence. It is generally connected to the timer #1 output of the 82C206.
Refresh	58	REF*	I/O	REFRESH is an open drain, active low signal. It is driven low by the 82C811 to indicate that a refresh cycle is in progress, or may be driven low externally to initiate a refresh cycle. An external pull up of 620 Ohms is required. This pin has 16mA drive capability.
X-Bus Interface	9	XMEMR*	I/O	X BUS MEMORY READ is active (low) during AT bus memory read cycles. It is an output during CPU and refresh cycles and an input during DMA and master cycles. This pin has 6mA drive capability.
X-Bus Interface	10	XMEMW*	I/O	X BUS MEMORY WRITE is active (low) during AT bus memory write cycles. It is an output during CPU cycles and in input during DMA and master cycles. This pin has 6mA drive capability.
X-Bus Interface	70	XIOR*	I/O	X BUS I/O READ is active (low) during I/O read cycles. It is a output during CPU cycles and an input during DMA or master cycles. This pin has 6mA drive capability.
X-Bus Interface	56	XIOW*	I/O	X BUS I/O WRITE is active (low) during I/O write cycles. It is an input during master and DMA cycles and is an output during CPU cycles. This pin has 6mA drive capability.
X-Bus Interface	57	XBHE*	I/O	X BYTE HIGH ENABLE is driven low to indicate a data transfer on bits 8 - 15 of the data bus. It is an output for CPU and DMA cycles and an input for master cycles. A 4.7K Ohm pull-up resistor is required on this line. This pin has 6mA drive capability.

Table 1.10 82C811 Pin Descriptions (continued)

Signal Type	Number	Name	I/O	Description
X-Bus Interface	59-62	XD<7:4>	I/O	X DATA BUS bits <7:4> are used for communication with 82C811 internal registers. This pin has 6mA drive capability.
X-Bus Interface	68-65	XD<3:0>	I/O	X DATA BUS bits <3:0> are used for communication with 82C811 internal registers. This pin has 6mA drive capability. *(Note: These pins differ from NEAT.)*
X-Bus Interface	75	TMRGATE		TIMER GATE is an active high output generally connected to the GATE2 pin on the 82C206. When high, the 82C206 produces a square wave to drive the speaker. This pin has 6mA drive capability.
X-Bus Interface	53	TMROUT2	I	TIMER OUT 2 is an active high input from the 82C206 timer #2. The state of this line can be read from "Port B".
X-Bus Interface	77	SPKDATA	O	SPEAKER DATA is an output bit from "Port B". It is used for software control of the speaker. This pin has 6mA drive capability.
X-Bus Interface	54	INTA*	O	INTERRUPT ACKNOWLEDGE output is active (low) during interrupt acknowledge cycles. This pin has 6mA drive capability.
Buffer Control	34	SDIR0	O	S DATA BUS DIRECTION for bits 0 - 7. When low, the SD bus is driven onto the MD bus. When high, the MD bus is driven onto the SD bus. This pin has 6mA drive capability.
Buffer Control	36	SDIR1	O	S DATA BUS DIRECTION for bits 8 - 15. When low, the SD bus is driven onto the MD bus. When high, the MD bus is driven onto the SD bus. This pin has 6mA drive capability.
Buffer Control	47	ACEN*	O	ACTION CODE ENABLE is an active low output that validates the action code signals AC<1,0> that are used by the 82C215 address/data buffer. This pin has 6mA drive capability.
Buffer Control	46, 45	AC1, AC0	O	ACTION CODE is a two bit encoded output command for bus size control and byte assembly operations performed in the 82C215. This pin has 6mA drive capability.
Memory Control	78	AF16*	I	AF16 is an active low input indicating that the current cycle is a local bus cycle. A high indicates an AT bus cycle. A 10K Ohm pull up resistor is required.
Memory Control	14-16 18-21 25-23	A<9:7> A<6:3> A(2:0>	I/O	CPU address lines A9 - A0. These are inputs during CPU bus cycles and outputs during refresh cycles. This pin has 6mA drive capability.
Memory Control	29	XA0	I/O	ADDRESS line XA0 from the X bus. It is an output during CPU bus cycles and is an input for 8 bit DMA cycles. This pin has 6mA drive capability.
Coprocessor Interface	6	A23	O	ADDRESS LINE 23 input from CPU. High during I/O cycles for numeric processor. This pin has 6mA drive capability.

Table 1.10 82C811 Pin Descriptions (continued)

Signal Type	Number	Name	I/O	Description
Coprocessor Interface	7	BUSY*	O	BUSY is an active low output to the CPU indicating that the coprocessor is busy. A 4.7K Ohm pull up resistor is required. This pin has 6mA drive capability. This pin has 6mA drive capability.
Coprocessor Interface	74	NPBUSY*	I	NUMERIC PROCESSOR BUSY is an active low input from the coprocessor, indicating that it is currently executing a command. It is used to generate the BUSY signal to the CPU. A 4.7K Ohm pull up resistor is required.
Coprocessor Interface	32	ERROR*	I	ERROR is an active low input from the coprocessor indicating that an unmasked error condition exists. A 4.7K Ohm pull up resistor is required.
Coprocessor Interface	4	NPINT	O	NUMERIC PROCESSOR INTERRUPT is an active high output. It is an interrupt request generated in response to the ERROR* signal from the coprocessor. A 10K Ohm pull up resistor is required. This pin has 6mA drive capability.
Coprocessor Interface	3	NPRESET	O	NUMERIC PROCESSOR RESET is an active high reset to the 80387sx. It is active when RESET4 is active or when a write operation is made to Port 0F1H. In the later case, it is active for 64 PROCCLK cycles the period of the command. This pin has 6mA drive capability.
Power Supplies	42, 63, 84	V_{DD}	PWR	POWER SUPPLY
Power Supplies	1, 17, 22	V_{SS}	PWR	GROUND
Power Supplies	43, 64	V_{SS}	PWR	GROUND

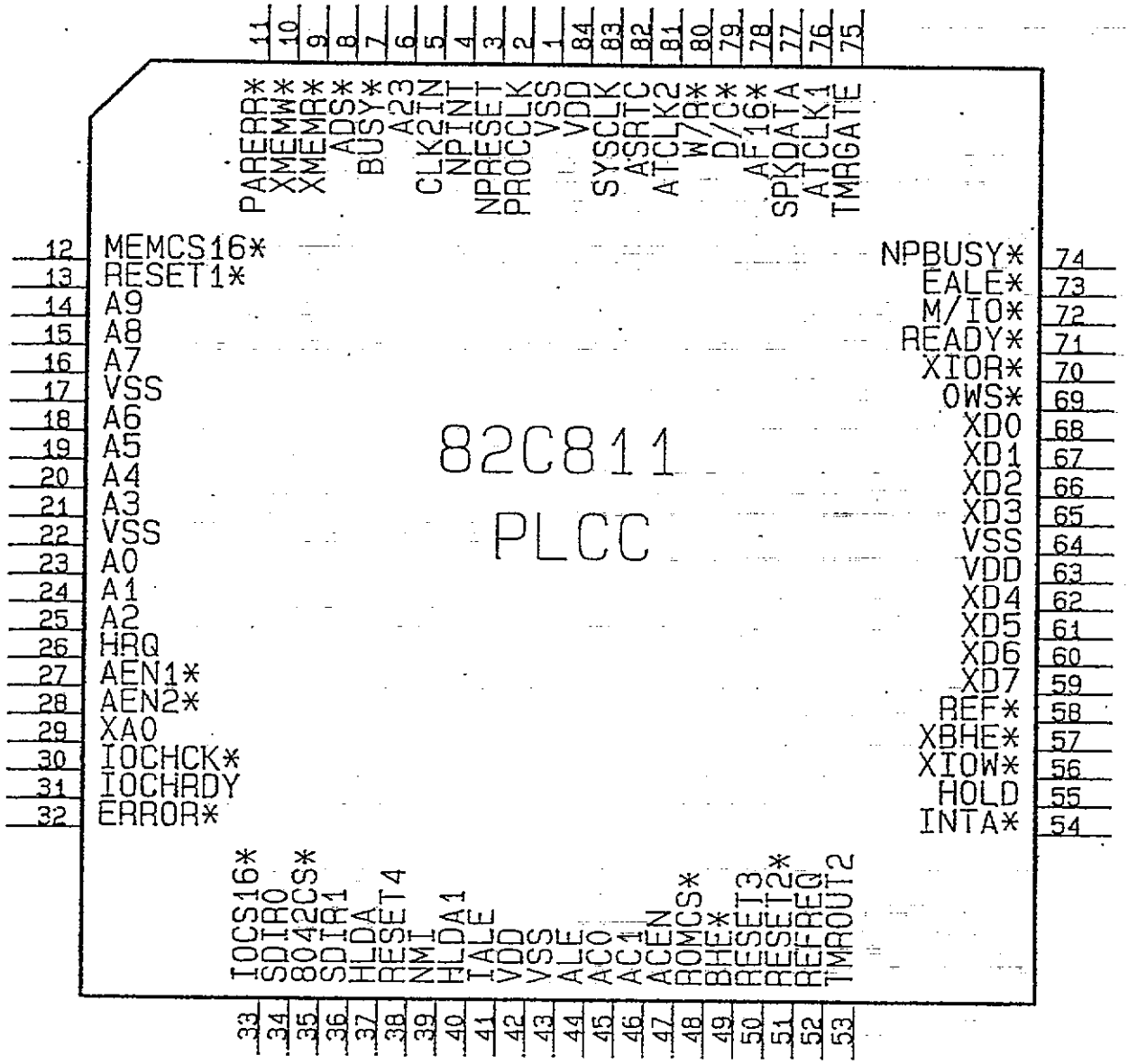
Table 1.11 82C811 Pin Numbers in Order by PFP Designation

PLCC	PFP	SIGNAL NAME	PLCC	PFP	SIGNAL NAME
11	1	PARERR*	53	51	TMROUT2
-	2	VDD	-	52	VDD
-	3	VSS	-	53	VSS
12	4	MEMCS16*	54	54	INTA*
13	5	RESET1*	55	55	HOLD
14	6	A9	56	56	XIOW*
15	7	A8	57	57	XBHE*
16	8	A7	58	58	REF*
17	9	VSS	59	59	XD7
18	10	A6	60	60	XD6
19	11	A5	61	61	XD5
20	12	A4	-	62	NOCONNECT
-	13	NOCONNECT	62	63	XD4
21	14	A3	63	64	VDD
22	15	VSS	-	65	NOCONNECT
-	16	NOCONNECT	64	66	VSS
23	17	A0	65	67	XD3
24	18	A1	66	68	XD2
25	19	A2	67	69	XD1
26	20	HRQ	68	70	XD0
27	21	AEN1*	69	71	OWS*
28	22	AEN2*	70	72	XIOR*
29	23	XA0	71	73	READY*
30	24	IOCHCK*	72	74	M/IO*
31	25	IOCHRDY	73	75	EALE*
32	26	ERROR*	74	76	NPBUSY*
-	27	VSS	-	77	VSS
-	28	VSS	-	78	VSS
33	29	IOCS16*	75	79	TMRGATE
34	30	SDIR0	76	80	ATCLK1
35	31	8042CS*	77	81	SPKDATA
36	32	SDIR1	78	82	AF16*
37	33	HLDA	79	83	D/C*
38	34	RESET4	80	84	W/R*
39	35	NMI	81	85	ATCLK2
40	36	HLDA1	82	86	ASRTC
41	37	IALE	83	87	SYSCLK
-	38	NOCONNECT	-	88	NOCONNECT
42	39	VDD	84	89	VDD
43	40	VSS	1	90	VSS
-	41	VDD	-	91	VDD
44	42	ALE	2	92	PROCCLK
45	43	AC0	3	93	NPRESET
46	44	AC1	4	94	NPINT
47	45	ACEN	5	95	CLK2IN
48	46	ROMCS*	6	96	A23
49	47	BHE*	7	97	BUSY*
50	48	RESET3	8	98	ADS*
51	49	RESET2*	9	99	XMEMR*
52	50	REFREQ	10	100	XMEMW*

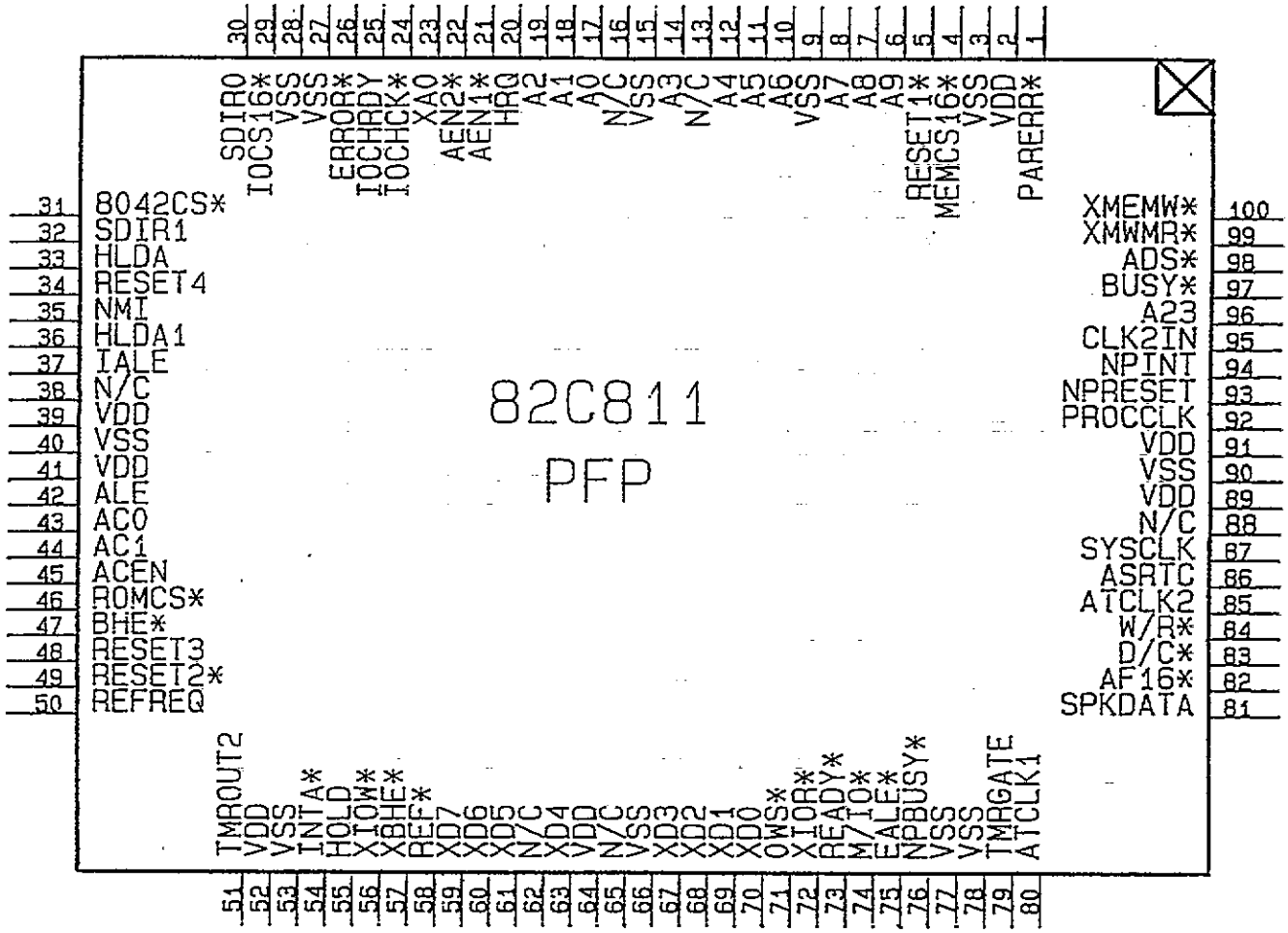
Table 1.12 82C811 Pin Numbers in Alphabetical Order

PLCC	PFP	SIGNAL NAME	PLCC	PFP	SIGNAL NAME
69	71	0WS*	3	93	NPRESET
35	31	8042CS*	11	1	PARERR*
23	17	A0	2	92	PROCCLK
24	18	A1	71	73	READY*
25	19	A2	58	58	REF*
21	14	A3	52	50	REFREQ
20	12	A4	13	5	RESET1*
19	11	A5	51	49	RESET2*
18	10	A6	50	48	RESET3
16	8	A7	38	34	RESET4
15	7	A8	48	46	ROMCS*
14	6	A9	34	30	SDIR0
6	96	A23	36	32	SDIR1
45	43	AC0	77	81	SPKDATA
46	44	AC1	83	87	SYSCLK
47	45	ACEN	75	79	TMRGATE
8	98	ADS*	53	51	TMROUT2
27	21	AEN1*	-	2	VDD
28	22	AEN2*	42	39	VDD
78	82	AF16*	-	41	VDD
44	42	ALE	-	52	VDD
82	86	ASRTC	63	64	VDD
76	80	ATCLK1	84	89	VDD
81	85	ATCLK2	-	91	VDD
49	47	BHE*	-	3	VSS
7	97	BUSY*	17	9	VSS
5	95	CLK2IN	22	15	VSS
79	83	D/C*	-	27	VSS
73	75	EALE*	-	28	VSS
32	26	ERROR*	43	40	VSS
37	33	HLDA	-	53	VSS
40	36	HLDA1	64	66	VSS
55	55	HOLD	-	77	VSS
26	20	HRQ	-	78	VSS
41	37	IALE	1	90	VSS
54	54	INTA*	80	84	W/R*
30	24	IOCHCK*	29	23	XA0
31	25	IOCHRDY	57	57	XBHE*
33	29	IOCS16*	68	70	XD0
72	74	M/IO*	67	69	XD1
12	4	MEMCS16*	66	68	XD2
39	35	NMI	65	67	XD3
-	13	NOCONNECT	62	63	XD4
-	16	NOCONNECT	61	61	XD5
-	38	NOCONNECT	60	60	XD6
-	62	NOCONNECT	59	59	XD7
-	65	NOCONNECT	70	72	XIOR*
-	88	NOCONNECT	56	56	XIOW*
74	76	NPBUSY*	9	99	XMEMR*
4	94	NPINT	10	100	XMEMW*

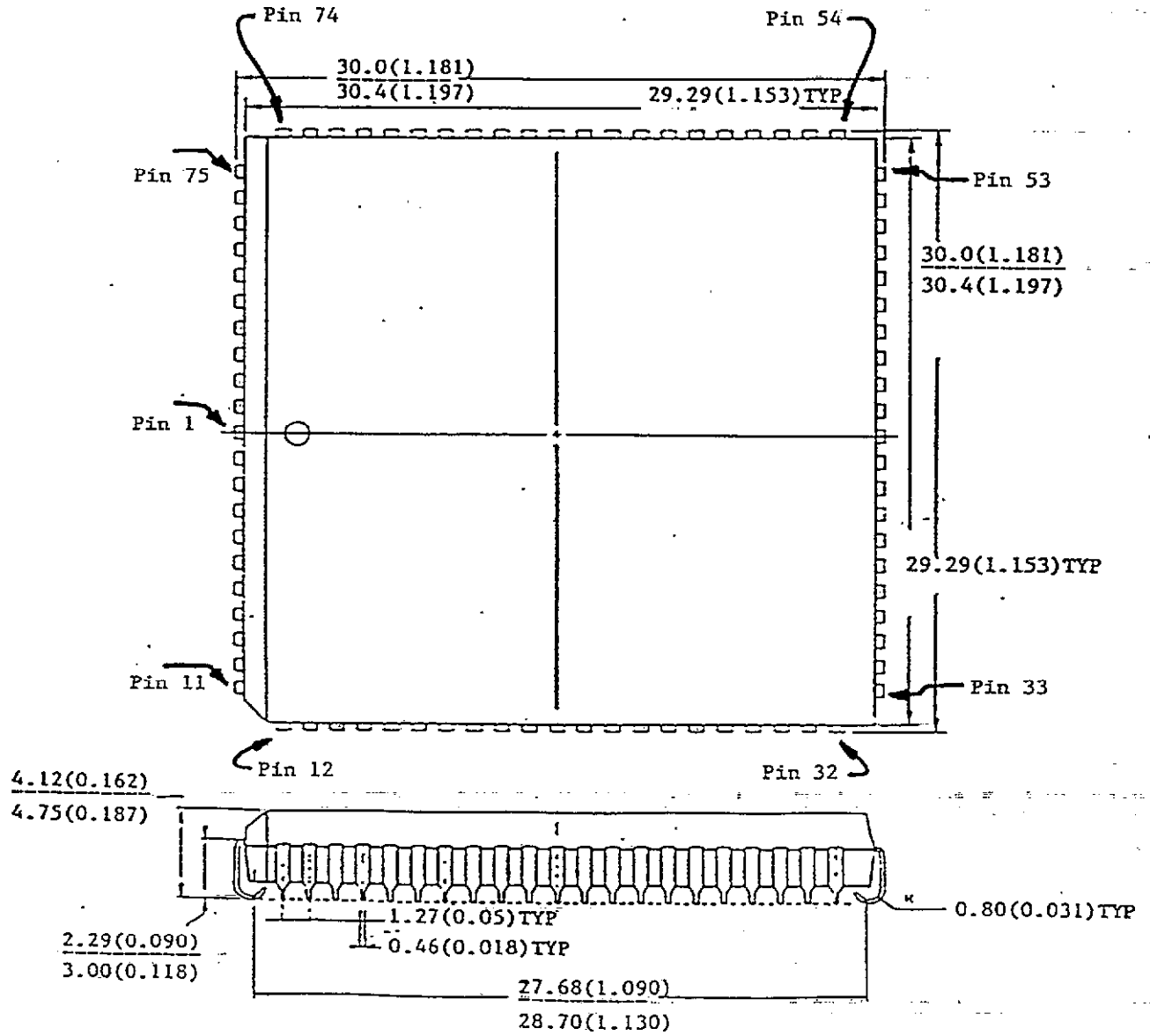
84-Pin Plastic Leaded Chip Carrier



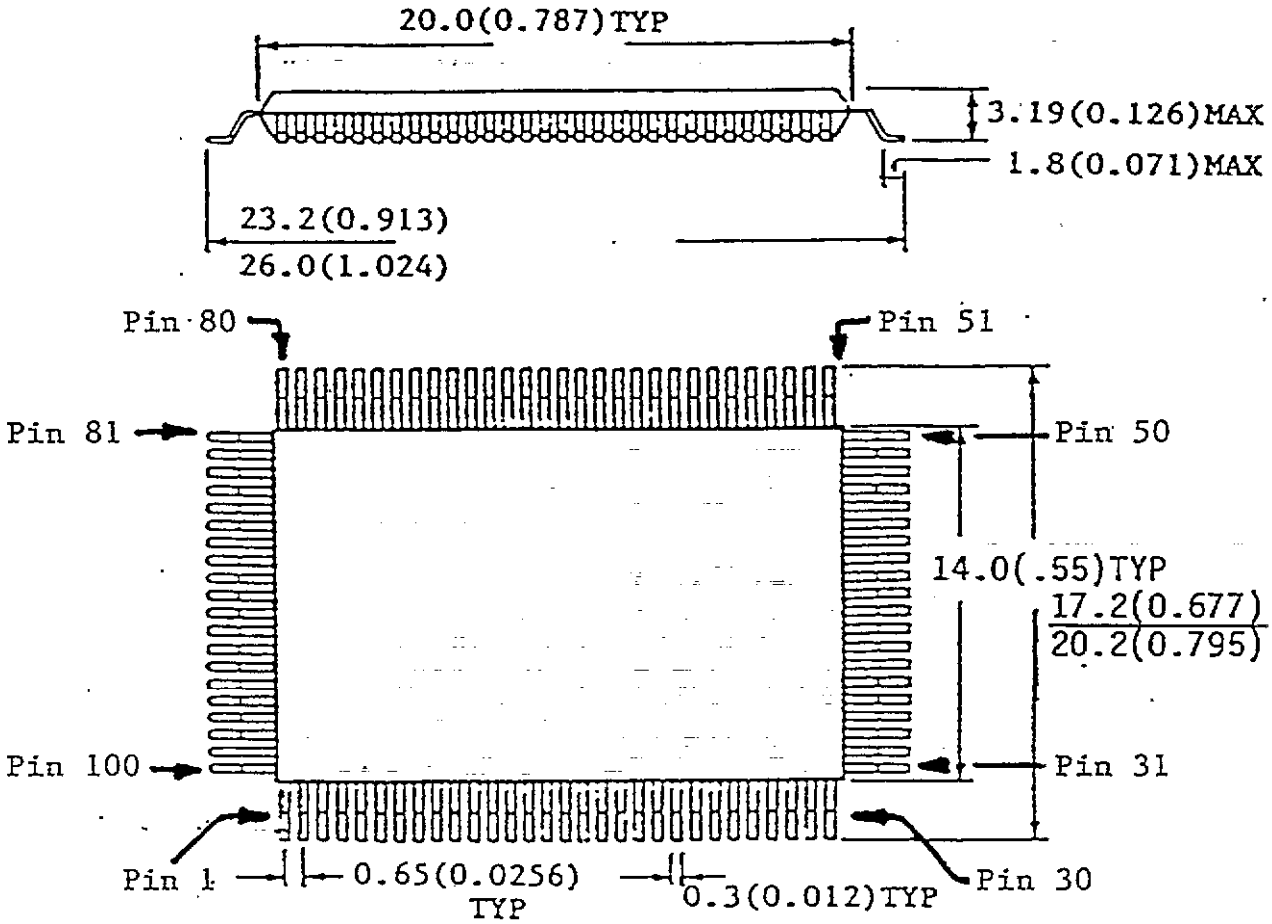
100-Pin Plastic Flat Package



84-Pin Plastic Leaded Chip Carrier



100-Pin Plastic Flat Package



2 82C812 Page/Interleave and EMS Memory Controller

2.1 Features

* Uses page mode access with interleaved memory banks to provide better performance than conventional DRAM accessing schemes
* Supports 100ns DRAMs at 16 MHz using page interleaved operation
* Supports up to 8MB of on-board memory
* Provides automatic remapping of RAM in the 640KB to 1MB area to the top of the 1MB address space
* Supports Lotus Intel Microsoft - Expanded Memory System (LIM-EMS) address translation logic
* Executes BIOS (Basic Input/Output System) faster through implementation of a shadow RAM feature
* Switches quickly between protected and real mode for optimum OS/2 use
* Reduces power supply noise through use of staggered refresh

2.2 Overview

The 82C812 utilizes page mode access DRAMs to perform the memory control functions in the NEATsx system. Various memory array configurations possible, and page/interleaved mode operation are discussed in this section. Figure 2.1 is a block diagram of the 82C812 chip.

2.2.1 Array Configuration

The 82C812 organizes memory as banks of 18-bit modules, consisting of sixteen bits of data and two bits of parity information. The sixteen bits of data are split into high and low order bytes, with one parity bit for each byte. This configuration can be implemented by using eighteen 1-bit wide DRAMs or by using four 4-bit wide DRAMs for data with two 1-bit wide DRAMs for parity. The minimum configuration can be a single bank of RAM operating in either non-page mode or single bank page mode. In order to implement the two-way interleaving scheme, the DRAMs within a pair of banks must be identical.

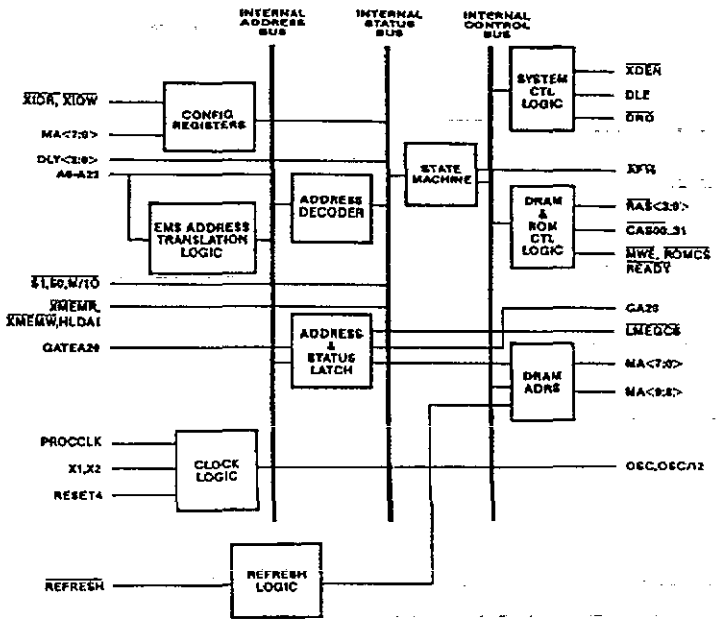


Figure 2.1 82C812 Block Diagram

However, each bank of DRAM pairs can be different from other pairs. For example, banks 0 and 1 may use 256K by 1 bit DRAMs while banks 2 and 3 may use 1M by 1 bit DRAMs. A typical system may be shipped with one or two banks of smaller DRAM types (for example, 256K by 1 bit DRAMs) and later upgraded with additional pairs of banks of larger DRAMs (for example, 1M by 1 bit DRAMs).

2.2.2 Modes of Operation

The 82C812 can operate in either non-page mode (traditional RAS - CAS mode) or a page-interleave scheme.

Non page mode timing is illustrated in Figure 2.2. In the beginning of a cycle, the first half of a multiplexed address is presented to the address pins on the RAM chips, and the Row Address Strobe (RAS*) is asserted. This begins the DRAM access by latching the address inside of the RAM chips and causes an internal row of data to be read from the memory cells and loaded into a temporary register. The address presented to the chips is then changed to the second half, which is the column portion of the address. The Column Address Strobe (CAS*) is then asserted, causing the RAM to enable its output buffers, and selecting the appropriate bit within its temporary register. At the end of the DRAM access, RAS* is returned to its inactive state. This causes the RAM to write the contents of its temporary register back into the original row of memory cells. RAS* must remain in its inactive state for approximately the same length of time as the minimum RAS* active time. This means that a complete cycle will take about twice as long as the RAM's access time. Non-page mode is useful at low CPU speeds, such as 12 Mhz with 80 nS DRAM's, where it can be used with zero wait states.

Page mode operation does not require RAS* to return to its inactive state between most accesses. RAS* must go inactive during refresh periods, on page misses (to latch the new row address) and after a RAS* time out period. (RAS time out is provided to insure the RAS* maximum pulse width specification is met.) After the initial assertion of RAS*, RAS* may remain low as long the row portion of the address is valid. This means that for all accesses within a row (page) boundary, RAS will remain active and the speed limitation will be the column access time of the RAM chips. The column access time (t_{cac}) is generally quite short compared to the row access time. The 82C812 takes advantage of this to provide zero wait state accesses for all accesses that fall within a page boundary. With 80 nS page mode DRAM's, the CPU may be operated at speeds up to 20 MHz with

Figure 2.2 82C812 Non-Page Mode Operation

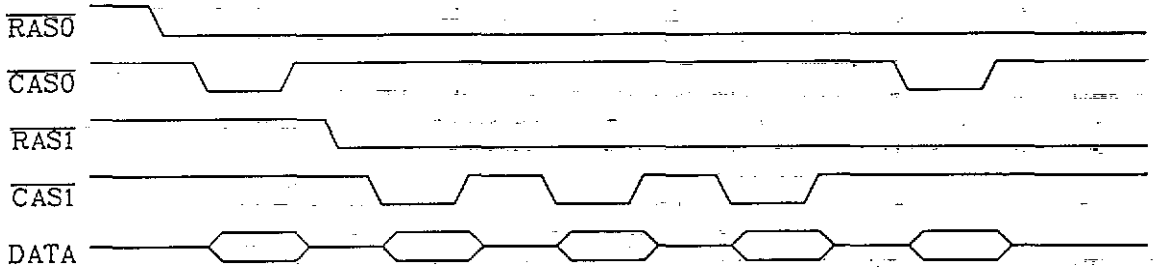


Figure 2.3 82C812 Page-Interleave Mode Operation

zero wait states. The page size for 256 K DRAM's is approximately 1 K bytes. To enlarge the page size, and therefore, the region of zero wait state accesses, the 82C812 will interleave it's DRAM accesses on a page boundary. If two adjacent banks of DRAM's have the same size, or, if all four banks are the same size, all accesses to the first page of memory will go to the first bank of DRAM's, accesses for the next page will go to the next bank, and so on. If the DRAM's are of differing sizes, the 82C812 will operate them in page mode only.

2.3 OS/2 Optimization

NEATsx architecture features OS/2 optimization through the use of the fast GATEA20 of the 82C812 in conjunction with the fast reset of the 82C811. OS/2 makes frequent DOS calls while operating in protected mode of the 80386sx. In order to service these DOS calls, the 80386sx has to switch quickly from protected to real mode. Typical AT-compatible architectures require that the processor issue two commands to the 8042 (or 8742) keyboard controller in order to reset the processor (to return to real address mode from protected mode) and to activate GATEA20.

Register RA0, bit 5 of the 82C811 resets the 80386sx processor, while register RB3, bit 1 of the 82C812 controls the gating of CPU address line A20. Since these functions are implemented in the hardware of the NEATsx CHIPSet rather than in the firmware of the 8042, they operate considerably faster. In an OS/2 environment, where the 80386sx switches out of protected mode frequently, this feature provides significant performance improvement.

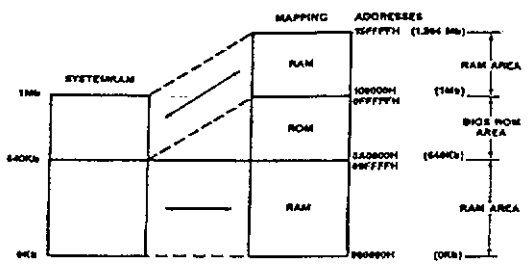


Figure 2.4 System RAM/ROM Mapping for 1Mb System RAM

2.4 Functional Description

Figure 2.1 is a block diagram of the 82C812 memory controller. It consists of the following sections:

* EPROM and DRAM control logic
* System control logic
* Memory mapping and refresh logic
* Oscillator clock generation logic
* Configuration registers

2.4.1 EPROM and DRAM Control Logic

The EPROM and DRAM control logic in the 82C812 is responsible for the generation of the RAS*, CAS*, and MWE* signals for DRAM accesses and the generation of ROMCS* for EPROM accesses. This section also generates READY* for the CPU upon completion of local memory operation. The appropriate number of wait states are inserted as programmed by software (or by default) in the wait state register of the 82C812. Figure 2.5 is a block diagram of the DRAM organization of the NEAT architecture. Note that each RAS* line drives each 256K X 18-bit bank (or 1M X 18-bit bank). The CAS* lines are used to drive individual bytes within each bank. MWE* is connected to each DRAM bank write enable input.

2.4.2 System Control Logic

This section of the 82C812 generates XDEN*, DLE, DRD*, and AF16* for system control. XDEN* is issued for I/O accesses to the internal registers of the 82C812. It is used to enable the XD0-7 lines onto the MA0-7 lines from an external buffer to access the internal registers of the 82C812. DLE and DRD* are generated to enable and control the direction of data between the CPU data bus and the memory data bus (MD bus). AF16* is issued by the 82C812 state machine. It is active for local memory accesses and meets the set up and hold times with respect to PROCCLK for the 82C811.

2.4.3 Memory Mapping and Refresh Logic

The 82C812 has an extensive set of memory mapping registers. These registers are discussed in section 2.3.5. In systems containing 1MB of RAM, the memory mapping logic is able to remap RAM that overlaps the EPROM area (640K-1M) to a range of addresses beginning at the 1MB boundary (see Figure 2.6). Software is then able to access the 1MB of system RAM from 0 to 640K and from 1M to 1.384M, while EPROM is addressed 640K to 1M.

2.4.4 Shadow RAM Feature

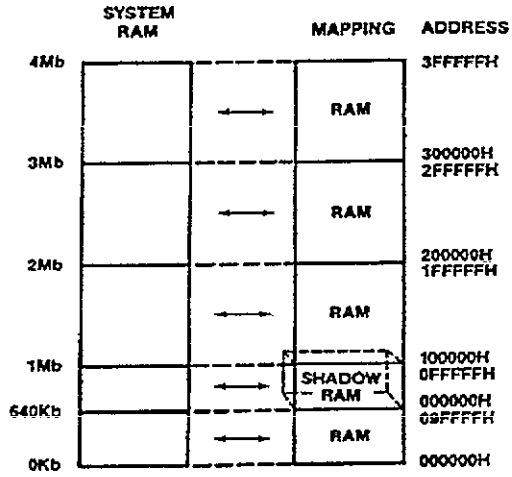


Figure 2.5 Ram Mapping With Shadow RAM (More Than 1Mb of RAM)

In order to enhance system performance, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The 82C812 provides a feature called shadow RAM that when enabled allows the BIOS code to be executed from system RAM resident at the same physical address as the BIOS EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-intensive applications. Performance improvements as high as 300% to 400% have been observed in shadow RAM benchmark tests. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and the RAM mapping register.

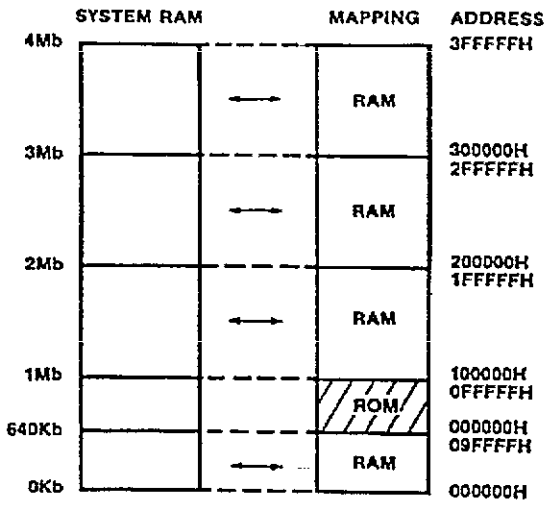


Figure 2.6 RAM/ROM Mapping Without Shadow RAM (More Than 1Mb of RAM)

If more than 1MB of system RAM exists and shadow RAM is not invoked, RAM is mapped as shown in Figure 2.7. Note that RAM in the range from 640K to 1M cannot be accessed. If the shadow RAM feature is invoked, RAM is mapped as shown in Figure 2.8 and the EPROM is remapped (shadowed) into RAM beginning at the 1MB boundary. In both cases, for accesses above the 1MB boundary, the BIOS switches the processor from real to protected mode.

2.4.5 EMS Address Translation Logic

The 82C812 provides mapping hardware that is compatible with the Expanded Memory Specification, version 3.2 (EMS 3.2). This allows a 64K block of addresses (C0000H-EFFFFH) to be used as a window (called a page frame) into a larger memory map. The page frame is divided into four 16K blocks (pages) that can be independently redirected to any area within the 82C812's memory map. (but not to locations on the AT bus). The EMS specification allows the processor to access to the vast amounts of memory while remaining in real address mode.

Memory used in conjunction with the EMS specification must be reserved as expanded memory and not be available as extended memory. The EMS memory size field in register RB11 (bits 5,6,7) is used for this purpose. It allows a section of extended

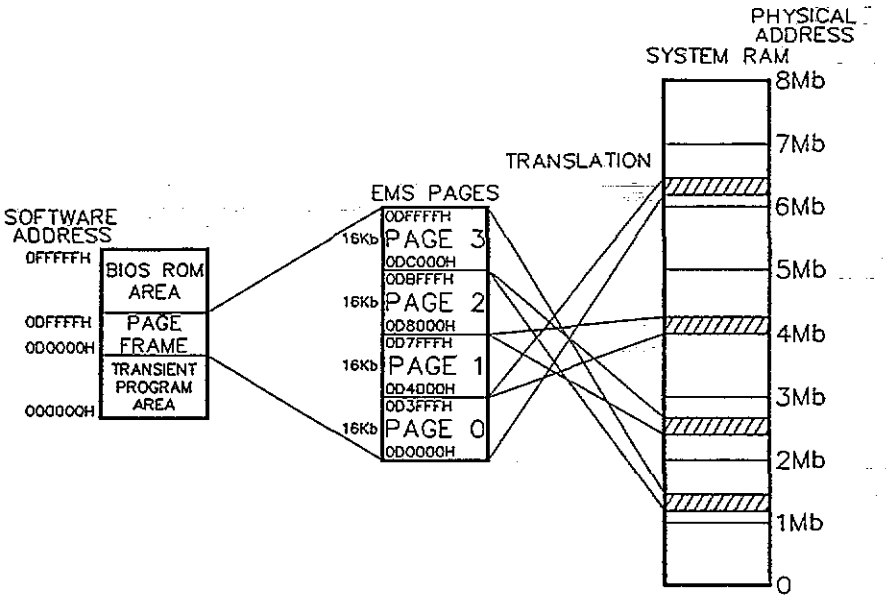


Figure 2.7 EMS Mapping

memory to be hidden from the system and prevents software from accessing the memory as both extended and expanded.

For example, if a system contains 4MB of RAM and the EMS memory size field is set to 2MB, the upper 2MB of memory will only be accessible as expanded memory. This leaves a balance of 1MB extended memory (part of which can be used for RAM shadowing) and 1MB conventional (or base) memory (memory at addresses below 1MB).

2.4.6 EMS 4.0 Support

The NEATsx CHIPSet provides full support for the Chips and Technologies 82C631 memory mapper–a device that enables a NEATsx system to support the new EMS 4.0 standard. Up to four 82C631 devices can be installed in a system and provide up to eight mapping register sets.

EMS 4.0 goes beyond the single 64K page frame allowed by EMS 3.2 and permits all the addresses between 0 and 1MB (00000H-FFFFFH) to be divided into sixty-four 16K pages. Multiple sets of mapping registers are also provided. The 82C631, when used in conjunction with EMS 4.0, allows operating systems such as Desqview or Microsoft Windows to swap entire application programs in and out of a system's memory map with a single I/O instruction. For further information, refer to the 82C631 data sheet.

2.4.7 Refresh Logic

During a refresh cycle, the 82C811 puts out the refresh address on the A0 - A9 address lines and asserts the REF* signal. The 82C812 uses these signals to generate the refresh address on the MA0 - MA9 address lines, the RAS* signals, and LMEGCS*. LMEGCS* is pulled low during refresh to allow MEMR* to be asserted on the AT bus. Figure 1.5 is a sequence diagram for a refresh cycle. Note that the 82C812 pulls RAS<1,2>* low, one delay unit after RAS<0,3>*. This technique of staggering the refresh reduces power supply noise generated during RAS* switching. Prior to a refresh, all RAS* lines are pulled high to ensure RAS* precharge. The RAS0* - RAS3*, RAS1* - RAS2* bundling is provided so that staggering is effective for all memory configurations between a two banks and four banks.

2.4.8 Memory Configurations

The NEATsx CHIPSet permits the use of 1M, 256K, and in one case, 64K DRAMs for system memory. Each memory bank can be implemented with eighteen 1-bit wide DRAMs or four 4-bit wide DRAMs with two 1-bit wide DRAMs. Possible configurations for on-board memory are provided in Table 2.1. Each bank is 16-bits wide with an additional two bits for parity.

Table 2.1 Memory Configurations

	DRAM Type				Total	EMS
	Bank 0	Bank 1	Bank 2	Bank 3	Memory	Range
1	0	0	0	0	disable	0
2	256KB	0	0	0	512KB	0
3	1MB	0	0	0	2MB	1MB to 2MB
4	256KB	64KB	0	0	640KB	0
5	256KB	256KB	0	0	1MB	1MB to 1.38MB
6	1MB	1MB	0	0	4MB	1MB to 4MB
7	256KB	256KB	0	0	1.5MB	1MB to 1.5MB
8	256KB	256KB	1MB	0	3MB	1MB to 3MB
9	1MB	1MB	1MB	0	6MB	1MB to 6MB
10	256KB	64KB	256KB	256KB	1.64MB	1MB to 1.64MB
11	256KB	256KB	256KB	256KB	2MB	1MB to 2MB
12	256KB	64KB	1MB	1MB	4.64MB	1MB to 4.64MB
13	256KB	256KB	1MB	1MB	5MB	1MB to 5MB
14	1MB	1MB	1MB	1MB	8MB	1MB to 7MB

Page/interleaving is possible only when similar pairs of DRAMs are installed. Table 2.1 indicates how page/interleaving is possible with combinations 5, 6, 10, 11, and 12.

2.5 Clock Generation Logic

The 82C812 has an oscillator circuit that uses a 14.31818 MHz crystal to generate the OSC and OSC/12 clocks. The 1.19381 MHz OSC/12 clock is used internally by a RAS time out counter for each RAM bank. In page mode operation, RAS* remains low until a page miss or refresh occurs. For many types of DRAM, 10 microseconds is the maximum time RAS* may be held low. RAS* time out counters will return RAS* to an inactive state after a time out of about 10 microseconds.

2.6 Configuration Registers

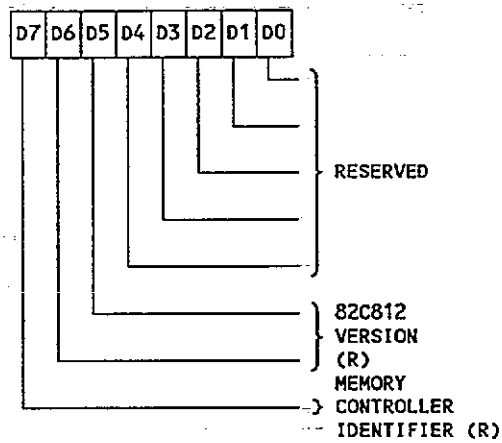
The 82C812 has twelve configuration and diagnostics registers, RB0 - RB11. These registers are accessed through I/O ports 22H and 23H, which are normally found in the interrupt controller module of the 82C206 IPC. An indexing scheme reduces the number of I/O addresses required to access all the registers needed to configure and control the memory controller. Port 22H is used as an index register that points to the required data value accessed through port 23H. A write of the index value for the required data is made to location 22H. The index value, after it is decoded, controls the multiplexers gating the appropriate register to the output bus. Every access to port 23H must be preceded by writing the index value to port 22H even if the same data register is being accessed again. All bits marked as reserved are set to zero by default; they must be maintained in this state during write operations, unless otherwise specified. Table 2.2 lists the registers.

Table 2.2 Configuration Registers

Register Number	Register Name	Index
RB0	Version	64H
RB1	Rom Configuration	65H
RB2	Memory Enable-1	66H
RB3	Memory Enable-2	67H
RB4	Memory Enable-3	68H
RB5	Memory Enable-4	69H
RB6	Bank 0/1 Enable	6AH
RB7	DRAM Configuration	6BH
RB8	Bank 2/3 Enable	6CH
RB9	EMS Base Address	6DH
RB10	EMS Address Extension	6EH
RB11	Miscellaneous	6FH

Table 2.3 Version Identification

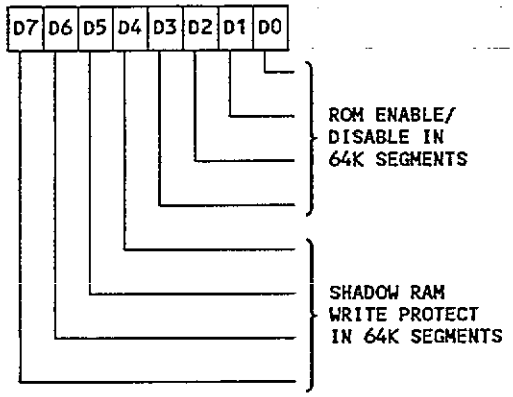
Version Register (RB0)
Index register port: 22H
Data register port: 23H
Index: 64H



Bits	Function
0-4	Reserved
5-6	82C812 revision number. 00 = initial release.
7	NEATsx memory controller identifier. 0 = 82C812

Table 2.4 ROM Configuration

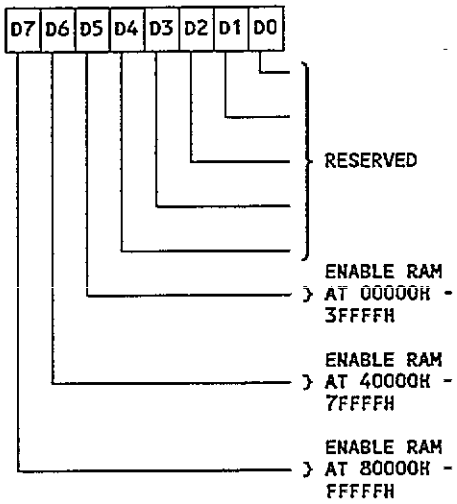
ROM Configuration Register (RB1)
Index Register Port: 22H
Data Register Port: 23H
Index: 65H



Bits	Function
0	ROM at F0000H-FFFFFH (BIOS). Default = 0 = ROM enabled. ROMCS* is generated.
1	ROM at E0000H-EFFFFH. Default = 1 = ROM disabled, shadow RAM enabled. ROMCS* is not generated unless bit is set to zero.
2	ROM at D0000H-DFFFFH. Default = 1 = ROM disabled, shadow RAM enabled. ROMCS* is not generated unless bit is set to zero.
3	ROM at C0000H-CFFFFH (EGA). Default = 1 = ROM disabled, shadow RAM enabled. ROMCS* is not generated unless bit is set to zero.
4	Shadow RAM at F0000H-FFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read Only (write protected).
5	Shadow RAM at E0000H-EFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read Only (write protected).
6	Shadow RAM at D0000H-DFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read Only (write protected).
7	Shadow RAM at C0000H-CFFFFH in Read/Write mode. 0 = Read/Write (default), 1 = Read Only (write protected).

Table 2.5 Memory Enable-1

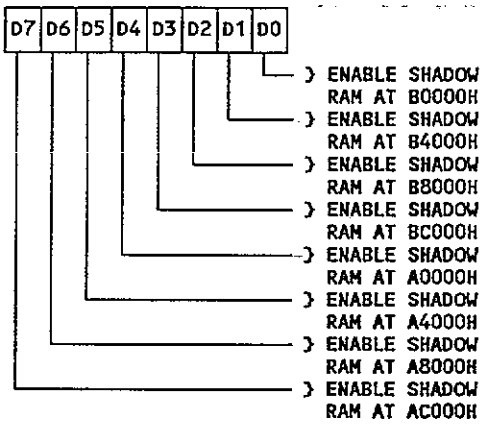
Memory Enable-1 Register (RB2)
Index Register Port: 22H
Data Register Port: 23H
Index: 66H



Bits	Function
0-4	Reserved.
5	Enable RAM at 00000H - 3FFFFH. Bits are read only. 1 = 82C812 does not respond to accesses in this range. 0 = Default. 82C812 does respond to accesses in this range.
6	Enable RAM at 40000H - 7FFFFH. Bits are read only. 1 = 82C812 does not respond to accesses in this range. 0 = Default. 82C812 does respond to accesses in this range.
7	Enable RAM at 80000H - FFFFFH. Bits are read/write. 0 = Default. 82C812 does not respond to accesses in this range. 1 = 82C812 does respond to accesses in this range.

Table 2.6 Memory Enable-2

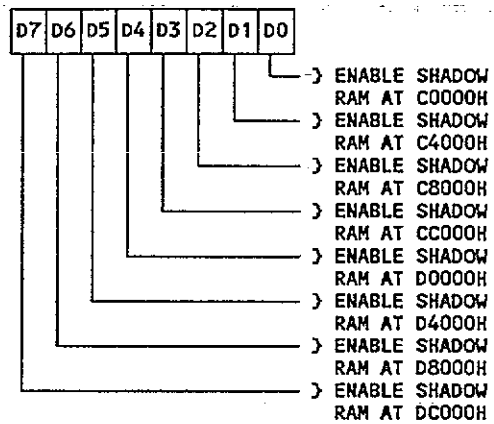
Memory Enable-2 Register (RB3)
Index Register Port: 22H
Data Register Port: 23H (R/W)
Index: 67H



Bits	Function
0	Enable Shadow RAM in B0000H-B3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in B4000H-B7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in B8000H-BBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in BC000H-BFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in A0000H-A3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in A4000H-A7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in A8000H-ABFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in AC000H-AFFFFH area. Disable = 0, Enable = 1.

Table 2.7 Memory Enable-3

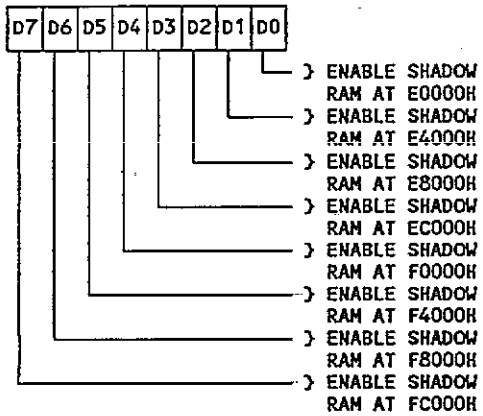
Memory Enable-3 Register (RB4)
Index Register Port: 22H
Data Register Port: 23H (R/W)
Index: 68H



Bits	Function
0	Enable Shadow RAM in C0000H-C3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in C4000H-C7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in C8000H-CBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in CC000H-CFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in D0000H-D3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in D4000H-D7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in D8000H-DBFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in DC000H-DFFFFH area. Disable = 0, Enable = 1.

Table 2.8 Memory Enable-4

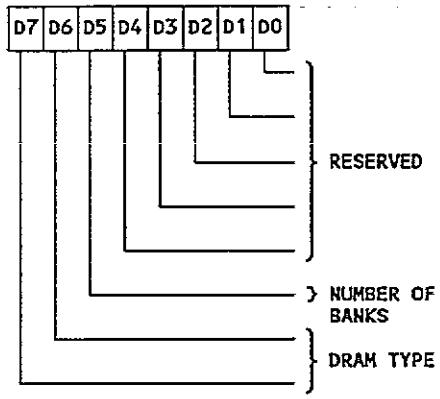
Memory Enable-4 Register (RB5)
Index Register Port: 22H
Data Register Port: 23H (R/W)
Index: 69H



Bits	Function
0	Enable Shadow RAM in E0000H-E3FFFH area. Disable = 0, Enable = 1.
1	Enable Shadow RAM in E4000H-E7FFFH area. Disable = 0, Enable = 1.
2	Enable Shadow RAM in E8000H-EBFFFH area. Disable = 0, Enable = 1.
3	Enable Shadow RAM in EC000H-EFFFFH area. Disable = 0, Enable = 1.
4	Enable Shadow RAM in F0000H-F3FFFH area. Disable = 0, Enable = 1.
5	Enable Shadow RAM in F4000H-F7FFFH area. Disable = 0, Enable = 1.
6	Enable Shadow RAM in F8000H-FBFFFH area. Disable = 0, Enable = 1.
7	Enable Shadow RAM in FC000H-FFFFFH area. Disable = 0, Enable = 1.

Table 2.9 Bank 0/1 Enable

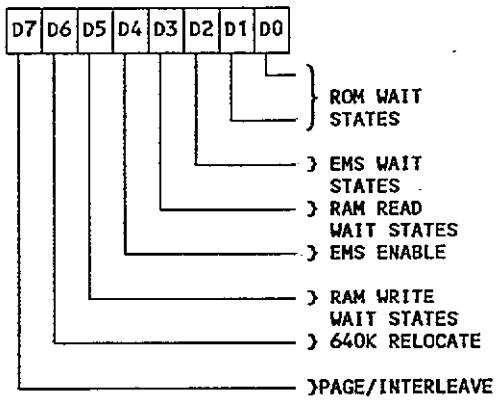
Bank 0/1 Enable Register (RB6)
Index Register Port: 22H
Data Register Port: 23H
Index: 6AH



Bits	Function	
0-4	Reserved	
5	Number of RAM banks used. 0 = one bank, non-interleaved mode (default). 1 = two banks.	
7-6	These bits contain the information for the DRAM types used on a system board. POST/BIOS should use the DRAM configuration data stored in the CMOS RAM of the 82C206 IPC.	
	7-6	DRAM types
	0 0	Disabled
	0 1	256K and 64K DRAMs used (for 640K combination only)
	1 0	256K DRAMs used (default)
	1 1	1M DRAMs used

Table 2.10 DRAM Configuration

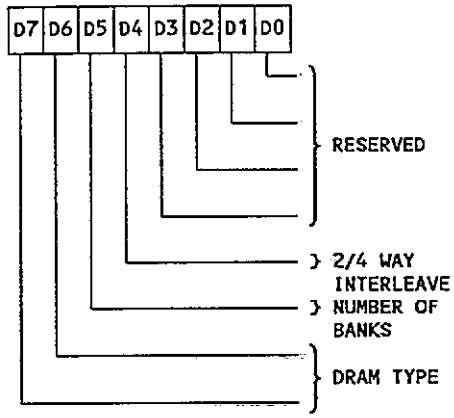
DRAM Configuration Register (RB7)
Index Register Port: 22H
Data Register Port: 23H (R/W)
Index: 6BH



Bits	Function
1,0	ROM access wait states control.
	1-0 Wait States: 0 0 = 0; 0 1 = 1; 1 0 = 2; 1 1 = 3 (Default)
2	EMS wait states 0 = 0 wait states (default) 1 = 1 wait state.
3	RAM read access wait states 0 = 0 wait states, 1 = 1 wait state.
4	EMS enable bit. If set to zero, EMS is disabled (default). If set to one, EMS is enabled.
5	RAM write access wait states. 0 = 0 wait states, 1 = 1 wait state.
6	640K to 1M RAM relocation bit. A one (default) relocates local RAM from 0A0000H-0FFFFFH to 100000H-11FFFFH, only if total local RAM is 1MB.
7	Page/Interleaved mode enable. A zero disables the page/interleaved mode, allowing usage of normal mode for the DRAMs (default). A one enables page/interleaved mode for the DRAMs.

Table 2.11 Bank 2/3 Enable

Bank 2/3 Enable Register (RB8)
Index Register Port: 22H
Data Register Port: 23H
Index: 6CH

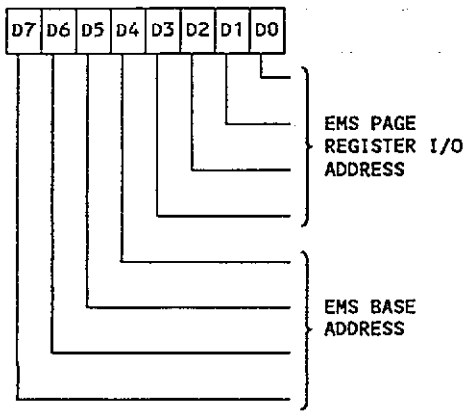


Bits	Function
0-3	Reserved.
4	0 = default; selects 2-way interleave. 1 = Selects 4-way interleave.
5	Number of local RAM banks used. 0 = one bank used, non-interleaved mode only (default). 1 = two banks used.
6-7	These bits indicate the local DRAM type as listed:

6-7	DRAM Type
0 0	None (default)
1 0	Reserved
0 1	256K
1 1	1M

Table 2.12 EMS Base Address

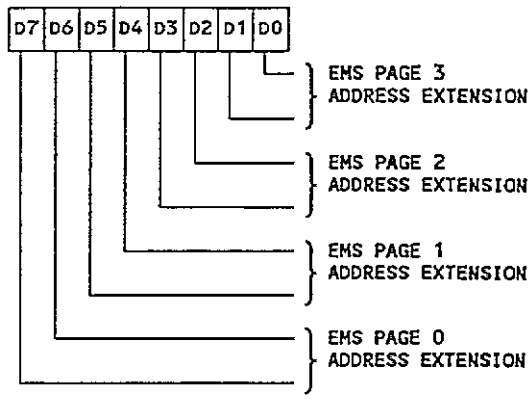
EMS Base Address Register (RB9)
Index Register Port: 22H
Data Register Port: 23H (R/W)
Index: 6DH



Bits	Function	
0-3	These bits are used for the EMS page register I/O base address. The bits are encoded as follows, with unused combinations being reserved:	
	3--0	I/O Base
	0000	208H 209H
	0001	218H/219H
	0101	258H/259H
	0110	268H/269H
	1010	2A8H/2A9H
	1011	2B8H/2B9H
	1110	2E8H/2E9H
7-4	These bits are used for selecting the expanded memory base addresses. They are encoded as follows, with all unused combinations being reserved:	
	7--4	EMS Base Addresses
	0000	C0000H, C4000H, C8000H, CC000H
	0001	C4000H, C8000H, CC000H, D0000H
	0010	C8000H, CC000H, D0000H, D4000H
	0011	CC000H, D0000H, D4000H, D8000H
	0100	D0000H, D4000H, D8000H, DC000H
	0101	D4000H, D8000H, DC000H, E0000H
	0110	D8000H, DC000H, E0000H, E4000H
	0111	DC000H, E0000H, E4000H, E8000H
	1000	E0000H, E4000H, E8000H, EC000H

Table 2.13 EMS Address Extension

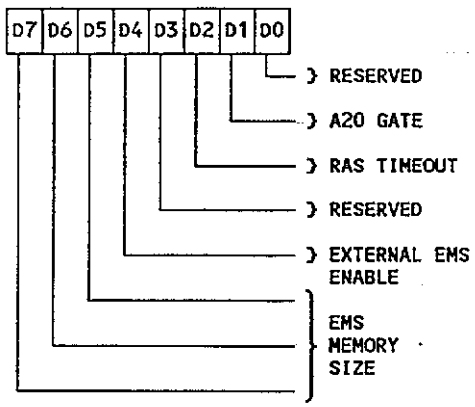
EMS Address Extension Register (RB10)
Index Register Port: 22H
Data Register Port: 23H
Index: 6EH



Bits	Function	
1-0	EMS Page 3 Address Extension Bits	
	1,0	Block of EMS Memory
	0 0	1MB to 2MB
	0 1	2MB to 4MB
	1 0	4MB to 6MB
	1 1	6MB to 8MB
3-2	EMS Page 2 Address Extension Bits	
	3,2	Block of EMS Memory
	0 0	1MB to 2MB
	0 1	2MB to 4MB
	1 0	4MB to 6MB
	1 1	6MB to 8MB
5,4	EMS Page 1 Address Extension Bits	
	5,4	Block of EMS Memory
	0 0	1MB to 2MB
	0 1	2MB to 4MB
	1 0	4MB to 6MB
	1 1	6MB to 8MB
7,6	EMS Page 0 Address Extension Bits	
	7,6	Block of EMS Memory
	0 0	1MB to 2MB
	0 1	2MB to 4MB
	1 0	4MB to 6MB
	1 1	6MB to 8MB

Table 2.14 Miscellaneous

Miscellaneous Register (RB11)
Index Register Port: 22H
Data Register Port: 23H
Index: 6FH



Bits	Function
0	Reserved
1	This bit is used for address line A20 control. It provides OS/2 optimization while switching between real and protected modes. The bit defaults to zero and enables CPUA20 onto A20. If set to one, it sets A20 = 0.
2	This bit is used to enable the RAS time-out counter for page mode operation. The counter is enabled if set to zero (default) and is disabled if set to one.
3	Reserved. Set to one.
4	External EMS Enable. 1 = External EMS enabled.
7-5	These bits are used to set the EMS memory space according to the following coding:

7-5	EMS Memory Size
000	1MB to 1.5MB (0.5MB)
001	1MB to 2MB (1MB)
010	1MB to 3MB (2MB)
011	1MB to 4MB (3MB)
100	1MB to 5MB (4MB)
101	1MB to 6MB (5MB)
110	1MB to 7MB (6MB)
111	1MB to 8MB (7MB)

Table 2.15 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	-	7.0	V
Input Voltage	V_I	-0.5	5.5	V
Output Voltage	V_O	-0.5	5.5	V
Operating Temperature	T_{OP}	-25°	85°	C
Storage Temperature	T_{STG}	-40°	125°	C

NOTE:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

Table 2.16 82C812 Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0°	70°	C

Table 2.17 82C812 DC Characteristics

Parameter	Symbol	Min	Max	Units
Input Low Voltage	V_{IL}	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V
Output Low Voltage	V_{OL}	-	0.45	V
I_{OL} = 4mA (MA<0:9>, GA20, X2, OSC/12, -ROMCS, RAS<0:3>, -MWE, DLE, -XDEN, -LMEGCS, DLYOUT, XDIR, OSC)				
I_{OL} = 8mA (-READY, -CAS<00:31>, -AF16)				
Output High Voltage	V_{OH}	2.4	-	V
I_{OH} = 4mA (MA<0:9>, GA20, X2, OSC/12, -ROMCS, RAS<0:3>, -MWE, DLE, -XDEN, -LMEGCS, DLYOUT, XDIR, OSC)				
I_{OH} = 8mA (-READY, -CAS<00:31>, -AF16)				
Input Current $0<V_{IN}<V_{CC}$	I_{IL}	-	±10	uA
Power Supply Current @ 16MHz	I_{CC}	-	50	mA
Output High Z Leakage Current $0.45<V_{OUT}<V_{CC}$	I_{OZ1}		±10	uA

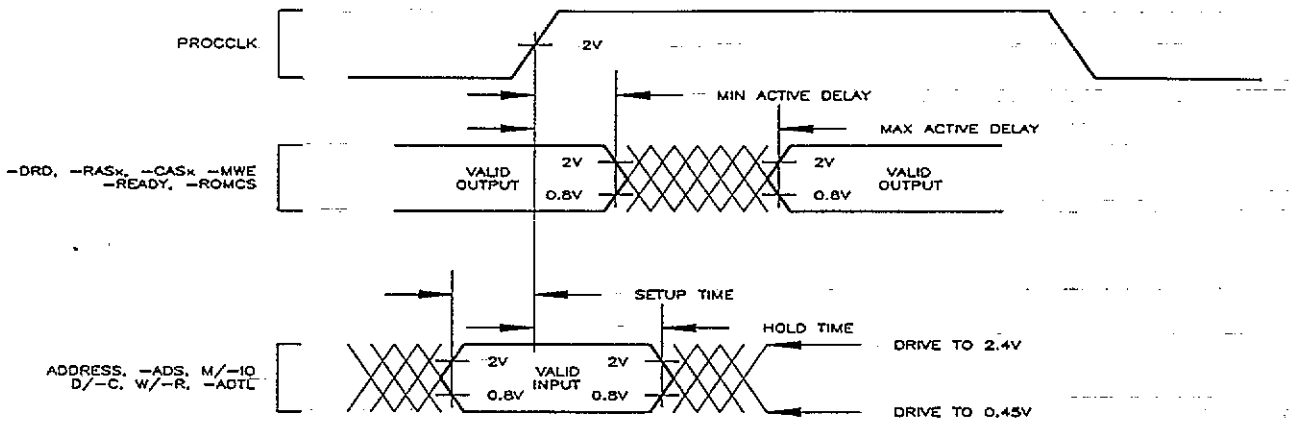


Figure 2.8 82C812 Setup, Hold and Active Delay Timings Relative to PROCCLK

Table 2.18 82C812-16, 82C812-20 AC Characteristics
(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; C_L = 75pF)
(Min and max values in nanoseconds.)

Symbol	Description	16 MHz Minimum	16 MHz Maximum	20 MHz Minimum	20 MHz Maximum
t1	RAS* active delay from PROCCLK ↑ (non-page)	0	16	0	16
t2	RAS* inactive delay from PROCCLK ↑ (non-page)	5	25	5	25
t3	DLYOUT active delay from RAS_i* active	-3	7	-3	7
t4	DLYOUT inactive delay from RAS_i* ↑	0	8	0	8
t5	Column address stable from DLY0 ↑	5	22	5	22
t6	Column address hold from DLY0 ↓	0	22	0	22
t7	CAS_i* active delay from DLY1 ↑	5	18	5	18
t8	CAS_i* inactive delay from DLY1 ↓	6	22	6	22
t11	READY* active delay from PROCCLK ↑	12	30	12	25
t12	READY* inactive delay from PROCCLK ↑	6	30	6	25
t13	DRD* active delay from PROCCLK ↑	10	19	10	19
t14	DRD* hold from DLE ↓	13	-	13	-
t15	DLE active delay from DLY1* ↓	0	30	0	22
t16	DLE inactive delay from PROCCLK ↑	0	25	0	20
t17	LMEGCS* active from PROCCLK ↑	0	31	0	25
t18	LMEGCS* inactive from PROCCLK ↑	0	31	0	25
t19	GA20* valid delay from CPU A20 valid	0	25	0	20
t20	GA20* invalid delay from CPU A20 invalid	0	25	0	20
t22	MWE* active delay from PROCCLK ↑	0	25	0	22
t23	MWE* inactive delay from PROCCLK ↑	0	20	0	18
t26	CAS_x* active delay from PROCCLK ↑	0	24	0	20
t27	CAS_x* inactive delay from PROCCLK ↑	0	21	0	21
t28	DRD* inactive delay from PROCCLK ↑	5	20	5	18
t29	CAS_x* inactive delay from DLE inactive	2	-	2	-
t30	RAS_x* active delay from PROCCLK ↑ (page mode)	8	24	8	16
t31	Row address setup time to RAS_x* ↓	8	-	8	-
t32	Row address hold time from PROCCLK ↑	6	25	6	20
t33	RAS_x* inactive delay from PROCCLK ↑ (page mode)	0	28	0	28
t34	RAS_i* precharge time (Interleaved Mode)		4xPROCCLK		4xPROCCLK
t35	ROMCS* active from PROCCLK ↑	0	30	0	25
t36	ROMCS* inactive from PROCCLK ↑	0	30	0	25
t37	DLE hold time from DRD*	0	25	0	22
t38	RAS_i* inactive from REF* active	0	32	0	32
t39	$RAS_{0,3}$* active from XMEMR* active	5	24	5	24
t40	$RAS_{0,3}$* inactive from XMEMR* inactive	5	20	5	20
t41	$RAS_{1,2}$* active from $RAS_{0,3}$* active	0	25	0	25

Table 2.18 82C812-16, 82C812-20 AC Characteristics (continued)
(T_A = 0°C to 70°C; V_{CC} = 5V ±5%; C_L = 75pF)
(Min and max values in nanoseconds.)

Symbol	Description	16 MHz		20 MHz	
		Minimum	Maximum	Minimum	Maximum
t42	$RAS_{1,2}$* inactive from $RAS_{0,3}$* inactive	11	30	11	30
t47	LMEGCS* delay from REF* ↓	5	30	5	30
t48	LMEGCS* delay from REF* ↑	10	30	10	30
t49	RAS_i* inactive from HLDA1 ↑	0	40	0	40
t50	RAS_i* active from command active	5	20	5	20
t51	RAS_i* inactive from command inactive	8	25	8	25
t54	Column address stable from DLY0 ↑	3	18	3	18
t55	CAS_i* active delay from DLY1 (XMEMW active)	5	25	5	25
t56	CAS_i* inactive delay from command inactive	9	22	9	22
t57	ADS setup to PROCCLK	19	-	19	-
t58	ADS hold from PROCCLK	6	-	6	-
t59	AF16 active delay	0	20	0	20
t60	ADTL setup to PROCCLK	19	-	19	-
t61	ADTL hold from PROCCLK	9	-	9	-
t62	READY setup to PROCCLK	19	-	19	-
t63	READY hold from PROCCLK	6	-	6	-
t64	M/IO*, D/C*, W/R* setup to PROCCLK	19	-	19	-
t65	M/IO*, D/C*, W/R* hold from PROCCLK	9	-	9	-
t66	Address setup to PROCCLK	19	-	19	-
t67	Address hold from PROCCLK	17	-	17	-

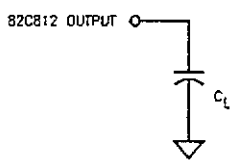


Figure 2.9 82C812 Test Load

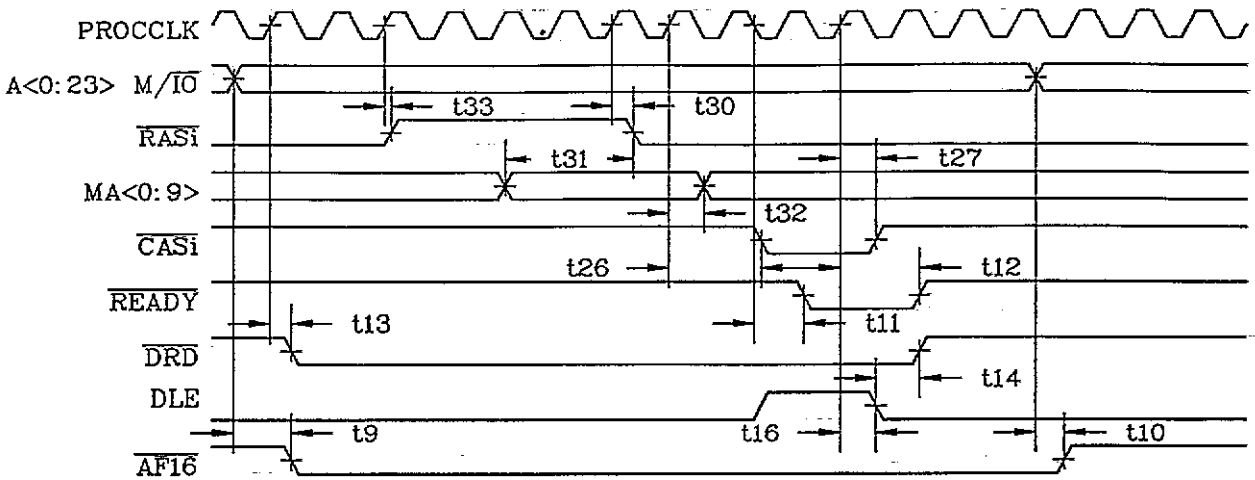


Figure 2.10 Page Mode Timing

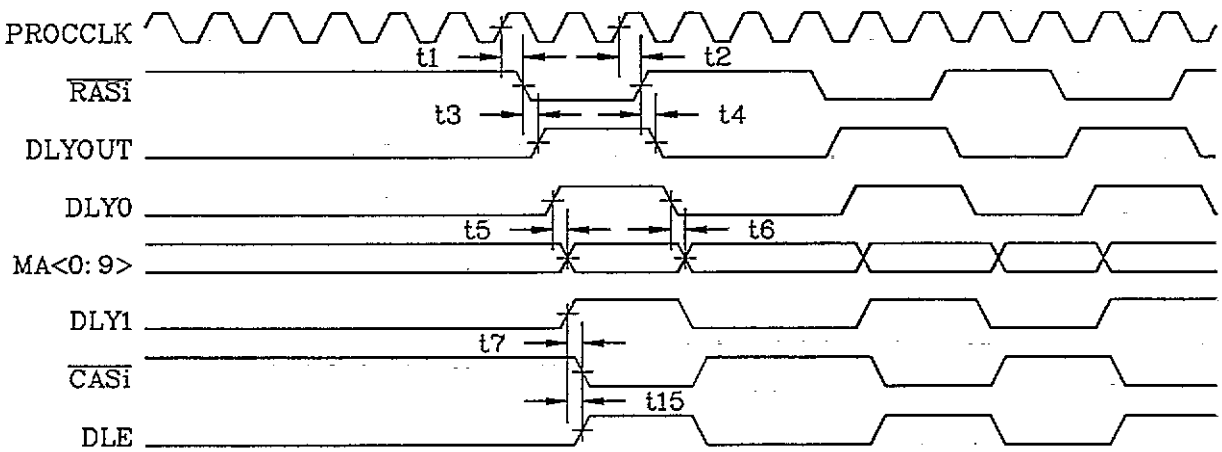


Figure 2.11 Non-Page Mode Timing

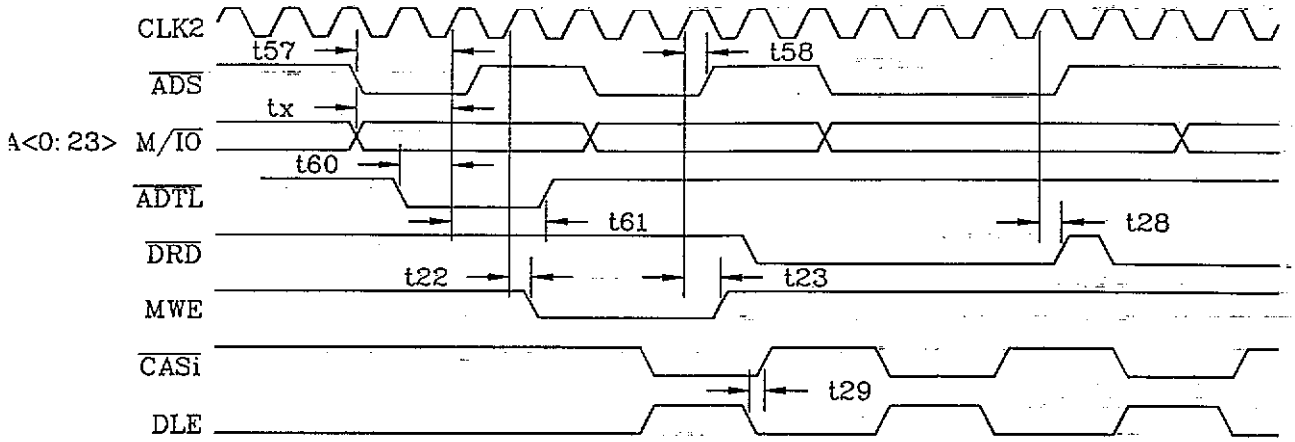


Figure 2.12 Miscellaneous Timing

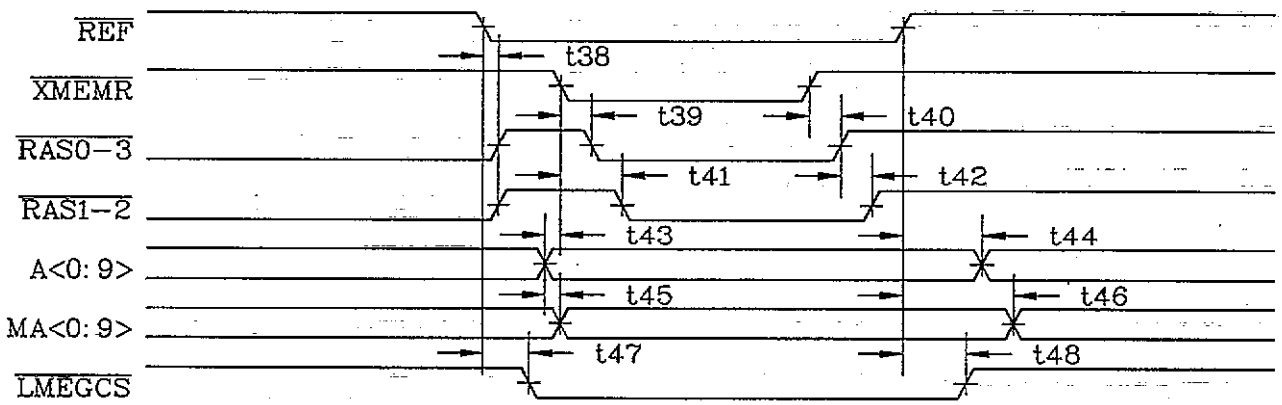


Figure 2.13 Refresh Timing

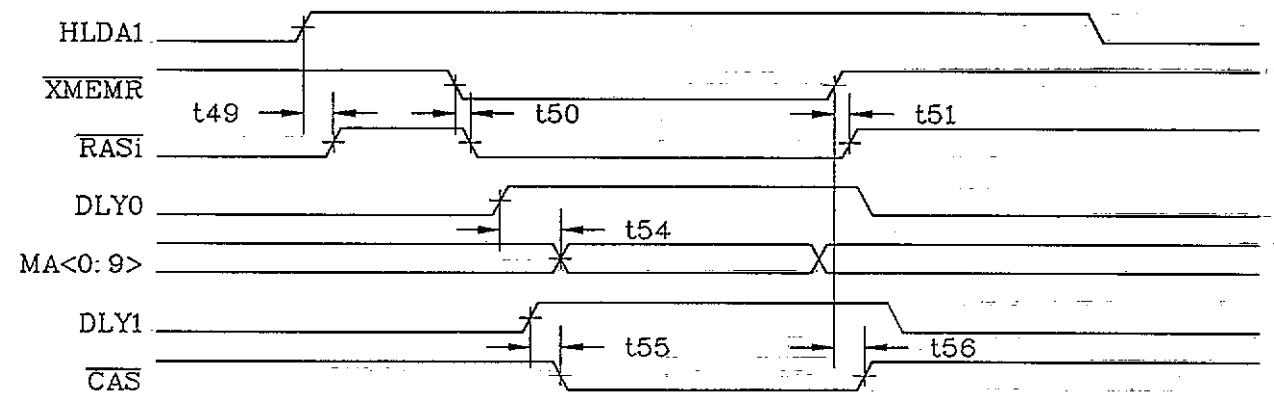


Figure 2.14 DMA Timing

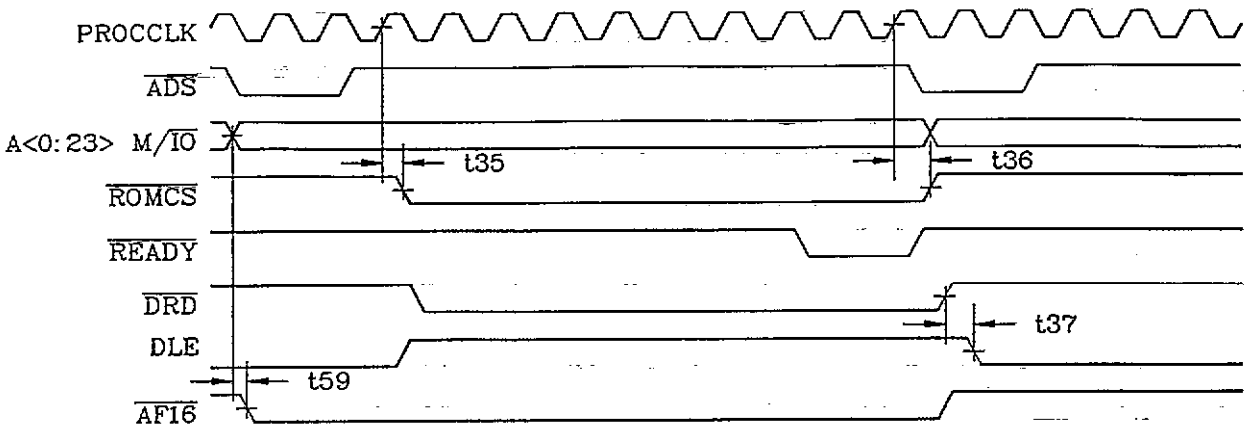


Figure 2.15 ROM Timing

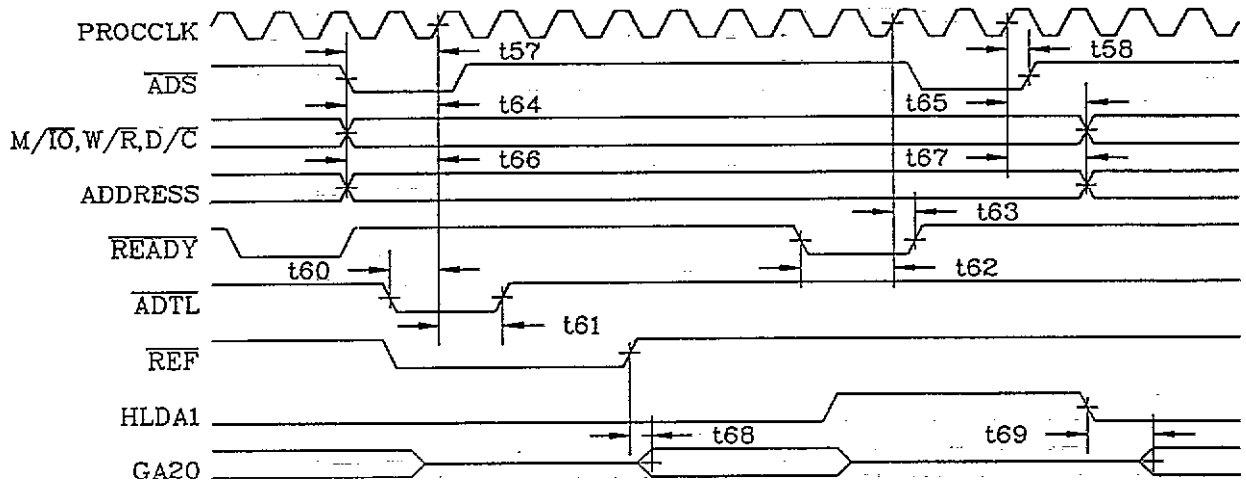


Figure 2.16 82C812 CPU Timing

Table 2.19 82C812 Pin Descriptions

Signal Type	Number	Name	I/O	Description
Clock	83	PROCCLK	I	PROCESSOR CLOCK input from the 82C211
Clock	23	X1	I	CRYSTAL 1 input from the 14.31818 MHz crystal.
Clock	24	X2	O	CRYSTAL 2 output to the 14.31818 MHz crystal. This pin has 4mA drive capability.
Clock/Control	18	OSC/ADTL	I/O	OSCILLATOR output / ADDRESS TRANSLATED input. If external EMS is not enabled, OSC/ADTL is a 14.313 MHz clock output for driving the OSC line on AT bus. If external EMS is enabled, this pin becomes an input for the ADTL line from the EMS mapper. This pin has 4mA drive capability.
Clock	21	OSC/12	O	OSCILLATOR divided by 12 is an 1.193 MHz clock output used to drive the TMRCLK pin of the 82C206. This pin has 4mA drive capability.
Control	12	RESET4	I	RESET 4 is the active high reset input from the 82C811. It resets the configuration registers to their default values. While RESET4 is active, RAS<0:3>, CAS<00:31>, OSC and OSC/12 remain inactive.
Control	20	REF*	I	REFRESH is an active low input for DRAM refresh control from the 82C811.
CPU Interface	63	ADS	I	ADDRESS STROBE input from 80386sx CPU. This active low signal indicates that the CPU is starting a cycle.
CPU Interface	65	W/R*	I	WRITE / READ input from 80386sx CPU. It indicates a write cycle if high and a read cycle if low.
CPU Interface	39	D/C*	I	DATA / CONTROL input from 80386sx CPU. Indicates data transfer operations when high, or control operations (code fetches, halt, etc.) when low.
CPU Interface	54	M/IO*	I	MEMORY I/O signal from the CPU. If high it indicates a memory cycle. If low, it indicates an I/O cycle.
Control	15	TEST	I	TEST input used for manufacturing. Must be tied to VSS for normal operation.
Control	38	XMEMR*	I	MEMORY READ input (active low) from AT bus.
Control	16	XMEMW*	I	MEMORY WRITE input (active low) from AT bus.
Control	19	HLDA1	I	HOLD ACKNOWLEDGE 1 is an active high input from the 82C211. It is used to generate RAS, CAS signals for DMA cycles, in response to a hold request.
ROM Interface	13	ROMCS*	O	ROM CHIP SELECT is an active low chip select output to the BIOS EPROM. It can be also connected to the output enable pin of the EPROM. This pin has 4mA drive capability.
Address	48, 74, 82	A0, A1, A2	I	ADDRESS lines from 80386sx CPU.
Address	40	A3	I	
Address	3-8	A<4:9>	I	
Address	46, 36	A10, A11	I	
Address	10, 11	A12, A13	I	
Address	47	A14	I	
Address	49-53	A<15:19>	I	
Address	55-58	A<20:23>	I	

Table 2.19 82C812 Pin Descriptions (continued)

Signal Type	Number	Name	I/O	Description
Address	34	BHE*	I	BYTE HIGH ENABLE is an active low input from the CPU for transfer of data on the upper byte.
Control	29	READY*	I/O	READY is the system ready signal to the CPU. It is output active low after requested memory or I/O data transfer is completed. It is an input when the current bus cycle is an AT bus cycle and is an output for local memory and I/O cycles. This pin has 8mA drive capability.
Control	59	AF16*	O	AF16 is an active low output asserted on local memory (EPROM or DRAM) cycles. It is high for all other cycles. This signal is sampled by the 82C211. This pin has 8mA drive capability.
DRAM Interface	77-80	RAS<3:0>	O	ROW ADDRESS STROBES 3 to 0 are active low outputs used to drive the DRAM RAS* pins. These signals may be used to drive the RAM chips without buffering. A 33 ohm series resistor is recommended. This pin has 4mA drive capability.
DRAM Interface	41	CAS00*	O	COLUMN ADDRESS STROBE - Bank 0, Low Byte
DRAM Interface	44	CAS01*	O	COLUMN ADDRESS STROBE - Bank 0, High Byte
DRAM Interface	14	CAS10*	O	COLUMN ADDRESS STROBE - Bank 1, Low Byte
DRAM Interface	2	CAS11*	O	COLUMN ADDRESS STROBE - Bank 1, High Byte
DRAM Interface	30	CAS20*	O	COLUMN ADDRESS STROBE - Bank 2, Low Byte
DRAM Interface	17	CAS21*	O	COLUMN ADDRESS STROBE - Bank 2, High Byte
DRAM Interface	35	CAS30*	O	COLUMN ADDRESS STROBE - Bank 3, Low Byte
DRAM Interface	9	CAS31*	O	COLUMN ADDRESS STROBE - Bank 3, High Byte These are active low outputs used to drive the DRAM CAS* pins. These signals may be used to drive the RAM chips without buffering. A 33 ohm series resistor is recommended. This pin has 8mA drive capability.
DRAM Interface	28	MWE*	O	MEMORY WRITE ENABLE is an active low output for DRAM write enable. A buffer and 33 ohm series resistor for every two banks of DRAM should be provided for this signal. This pin has 4mA drive capability.
DRAM Address	71-72	MA<8:9>	O	MULTIPLEXED DRAM ADDRESS lines MA<9:0>. Buffers and 33 ohm series resistors should be provided for every two banks of RAM. This pin has 4mA drive capability.
	66-70	MA<3:7>	I/O	
	60-62	MA<0:2>	I/O	
Control	45	DLE	O	DATA LATCH ENABLE is an active high output used to enable the local memory data buffer latch in the 82C215. This pin has 4mA drive capability.
Control	33	DRD*	O	DATA READ is an active low output used to transfer data from the memory bus to the local CPU bus in the 82C215. If high it sets the data path from the local CPU bus to the memory bus. This pin has 4mA drive capability.
DRAM Control	81	DLYOUT	O	DELAY LINE OUT is an active high output to the delay line for generating the DRAM control signals. This pin has 4mA drive capability.
DRAM Control	73	DLY0	I	DELAY INPUTS are active high inputs from the external delay line used to generate DRAM control signals.
DRAM Control	75	DLY1	I	
DRAM Control	76	DLY2	I	

Table 2.19 82C812 Pin Descriptions (continued)

Signal Type	Number	Name	I/O	Description
Miscellaneous	26	XDEN*	O	X DATA BUFFER ENABLE is an active low output used to control the external MA - XD bus buffer. This signal will be active during I/O operations to the internal registers of the 82C812. This pin has 4mA drive capability.
Miscellaneous	27	XDIR*	O	X BUS DIRECTION is used to control the direction of the buffers between the XD and SD buses. When XDIR* is low, the SD bus should be driven onto the XD bus. This pin has 4mA drive capability.
Address	31	GA20	I/O	ADDRESS line 20 is the gated A20 bit which is controlled by GATEA20. GA20 is an input during DMA and master cycles. This pin has 4mA drive capability.
Control	37	GATEA20	I	GATE A20 is an input from the 8042 keyboard controller used to force address line A20 to 0. When high, GA20 = CPU A20. When low, GA20 = 0.
Miscellaneous	25	LMEGCS*	O	LOW MEG CHIP SELECT is an address decode active when address lines A20 - A23 are low. It is used to enable the SMEMR* and SMEMW* signals on the AT bus for memory operations in the 00000H - OFFFFFH range. This pin has 4mA drive capability.
Power and Ground	32, 42, 84	V_{DD}	PWR	POWER SUPPLY.
Power and Ground	1, 22, 43,	V_{SS}	PWR	GROUND.
Power and Ground	64	V_{SS}		

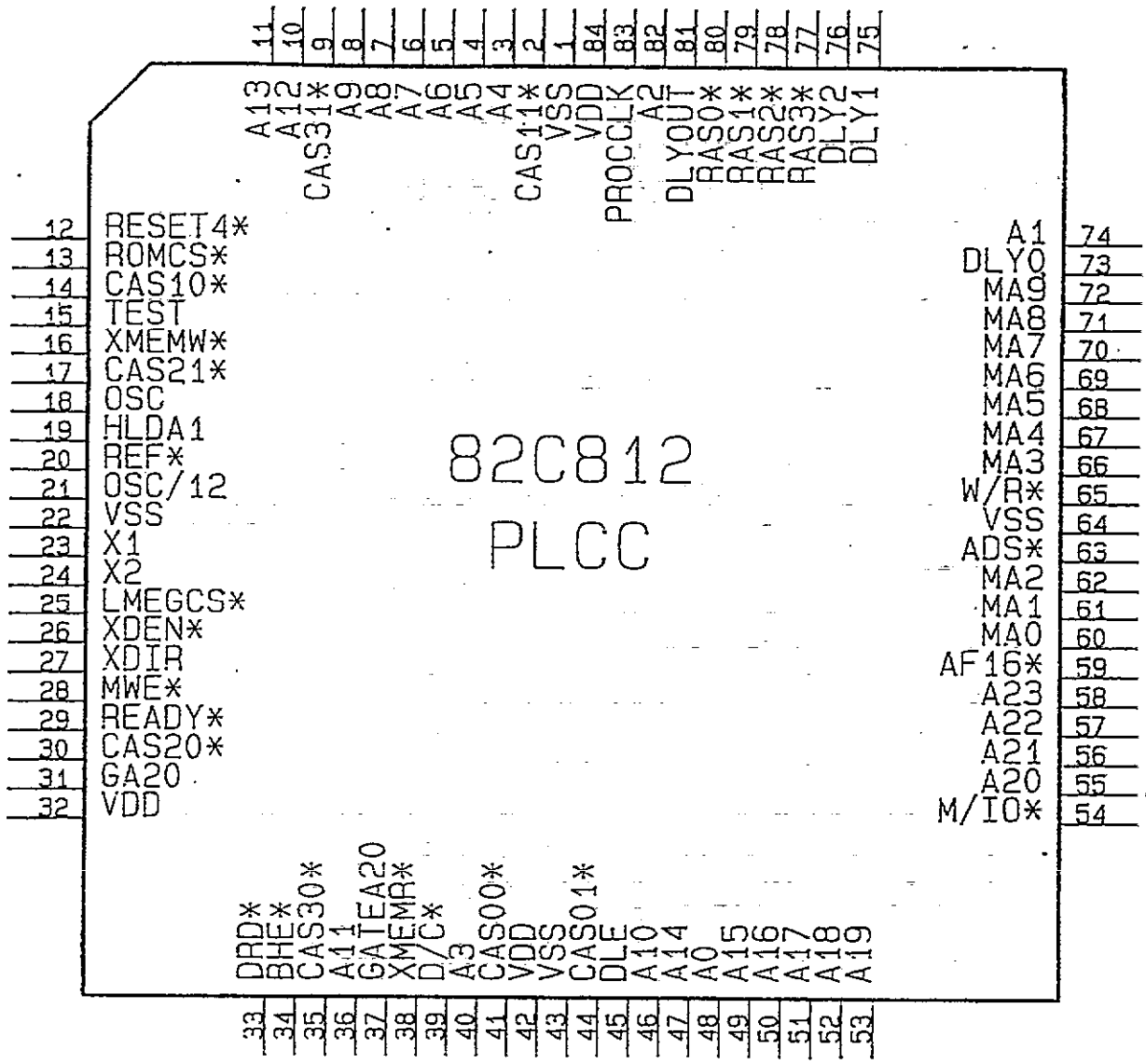
Table 2.20 82C812 Pin Numbers in Order by PFP Designation

PLCC	PFP	SIGNAL NAME	PLCC	PFP	SIGNAL NAME
10	1	A12	52	51	A18
11	2	A13	53	52	A19
12	3	RESET4*	-	53	NO CONNECT
13	4	ROMCS*	54	54	M/IO*
14	5	CAS10*	55	55	A20
-	6	NO CONNECT	56	56	A21
15	7	TEST	57	57	A22
16	8	XMEMW*	58	58	A23
-	9	NO CONNECT	-	59	NO CONNECT
17	10	CAS21*	59	60	AF16*
18	11	OSC	60	61	MA0
19	12	HLDA1	61	62	MA1
20	13	REF*	62	63	MA2
21	14	OSC/12	63	64	ADS*
22	15	VSS	-	65	NO CONNECT
-	16	NO CONNECT	64	66	VSS
23	17	X1	65	67	W/R*
24	18	X2	66	68	MA3
25	19	LMEGCS*	67	69	MA4
26	20	XDEN*	68	70	MA5
-	21	NO CONNECT	-	71	NO CONNECT
27	22	XDIR	69	72	MA6
28	23	MWE*	70	73	MA7
29	24	READY*	71	74	MA8
-	25	NO CONNECT	-	75	NO CONNECT
30	26	CAS20*	72	76	MA9
31	27	GA20	73	77	DLY0
32	28	VDD	74	78	A1
33	29	DRD*	75	79	DLY1
34	30	BHE*	76	80	DLY2
35	31	CAS30*	77	81	RAS3*
-	32	NO CONNECT	78	82	RAS2*
36	33	A11	-	83	NO CONNECT
37	34	GATEA20	79	84	RAS1*
38	35	XMEMR*	80	85	RAS0*
39	36	D/C*	81	86	DLYOUT
40	37	A3	82	87	A2
41	38	CAS00*	83	88	PROCCLK
-	39	NO CONNECT	-	89	NO CONNECT
43	40	VSS	1	90	VSS
42	41	VDD	84	91	VDD
44	42	CAS01*	2	92	CAS11*
45	43	DLE	3	93	A4
46	44	A10	4	94	A5
47	45	A14	5	95	A6
48	46	A0	6	96	A7
49	47	A15	7	97	A8
-	48	NO CONNECT	-	98	NO CONNECT
50	49	A16	8	99	A9
51	50	A17	9	100	CAS31*

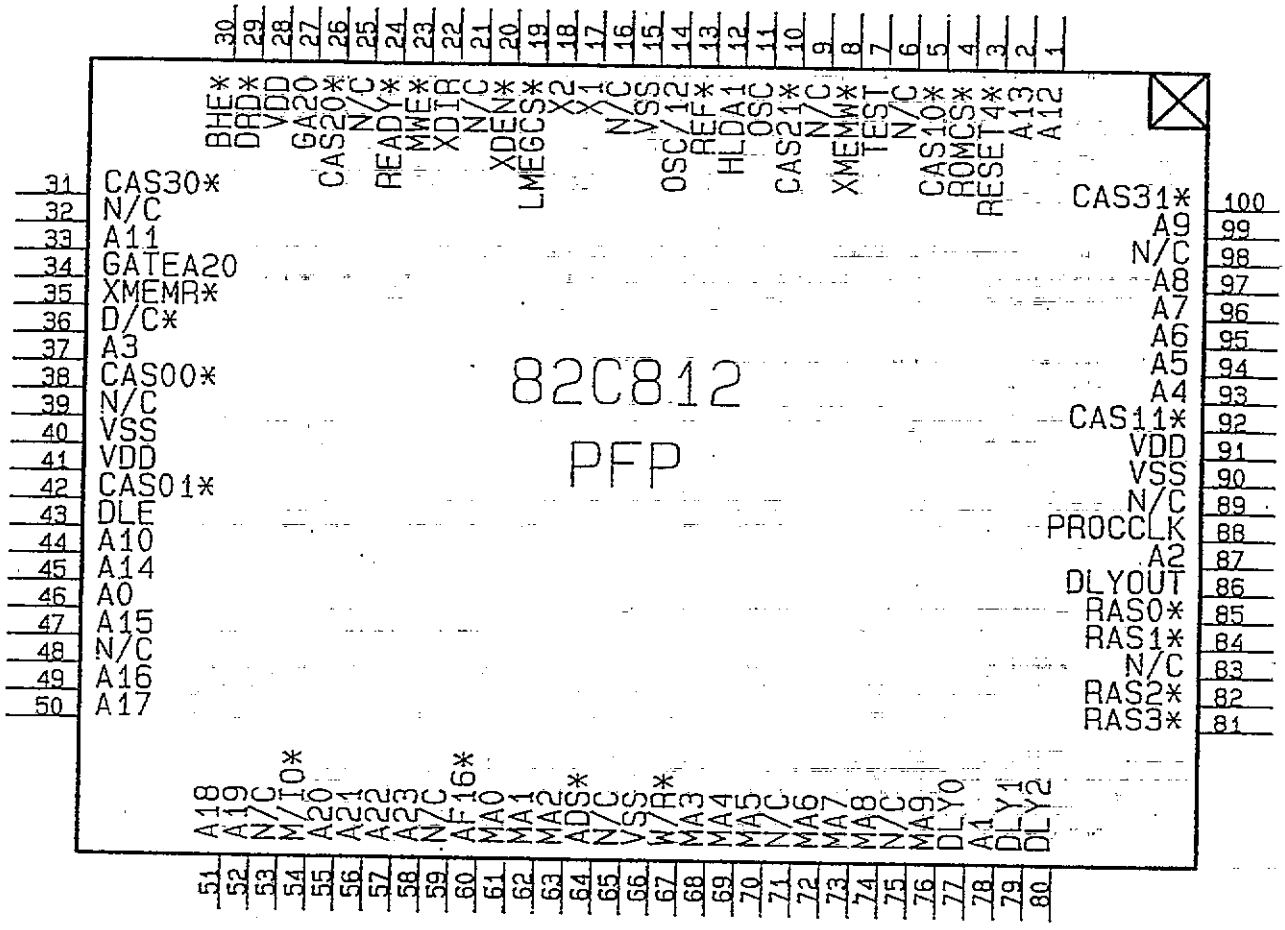
Table 2.21 82C812 Pins in Alphabetical Order

PLCC	PFP	SIGNAL NAME
48	46	A0
74	78	A1
82	87	A2
40	37	A3
3	93	A4
4	94	A5
5	95	A6
6	96	A7
7	97	A8
8	99	A9
46	44	A10
36	33	A11
10	1	A12
11	2	A13
47	45	A14
49	47	A15
50	49	A16
51	50	A17
52	51	A18
53	52	A19
55	55	A20
56	56	A21
57	57	A22
58	58	A23
63	64	ADS*
59	60	AF16*
34	30	BHE*
41	38	CAS00*
44	42	CAS01*
14	5	CAS10*
2	92	CAS11*
30	26	CAS20*
17	10	CAS21*
35	31	CAS30*
9	100	CAS31*
39	36	D/C*
45	43	DLE
73	77	DLY0
75	79	DLY1
76	80	DLY2
81	86	DLYOUT
33	29	DRD*
31	27	GA20
37	34	GATEA20
19	12	HLDA1
25	19	LMEGCS*
54	54	M/IO*
60	61	MA0
61	62	MA1
62	63	MA2
66	68	MA3
67	69	MA4
68	70	MA5
69	72	MA6
70	73	MA7
71	74	MA8
72	76	MA9
28	23	MWE*
-	6	NO CONNECT
-	9	NO CONNECT
-	16	NO CONNECT
-	21	NO CONNECT
-	25	NO CONNECT
-	32	NO CONNECT
-	39	NO CONNECT
-	48	NO CONNECT
-	53	NO CONNECT
-	59	NO CONNECT
-	65	NO CONNECT
-	71	NO CONNECT
-	75	NO CONNECT
-	83	NO CONNECT
-	89	NO CONNECT
-	98	NO CONNECT
18	11	OSC
21	14	OSC/12
83	88	PROCCLK
80	85	RAS0*
79	84	RAS1*
78	82	RAS2*
77	81	RAS3*
29	24	READY*
20	13	REF*
12	3	RESET4
13	4	ROMCS*
15	7	TEST
32	28	VDD
42	41	VDD
84	91	VDD
22	15	VSS
43	40	VSS
64	66	VSS
1	90	VSS
65	67	W/R*
23	17	X1
24	18	X2
26	20	XDEN*
27	22	XDIR
38	35	XMEMR*
16	8	XMEMW*

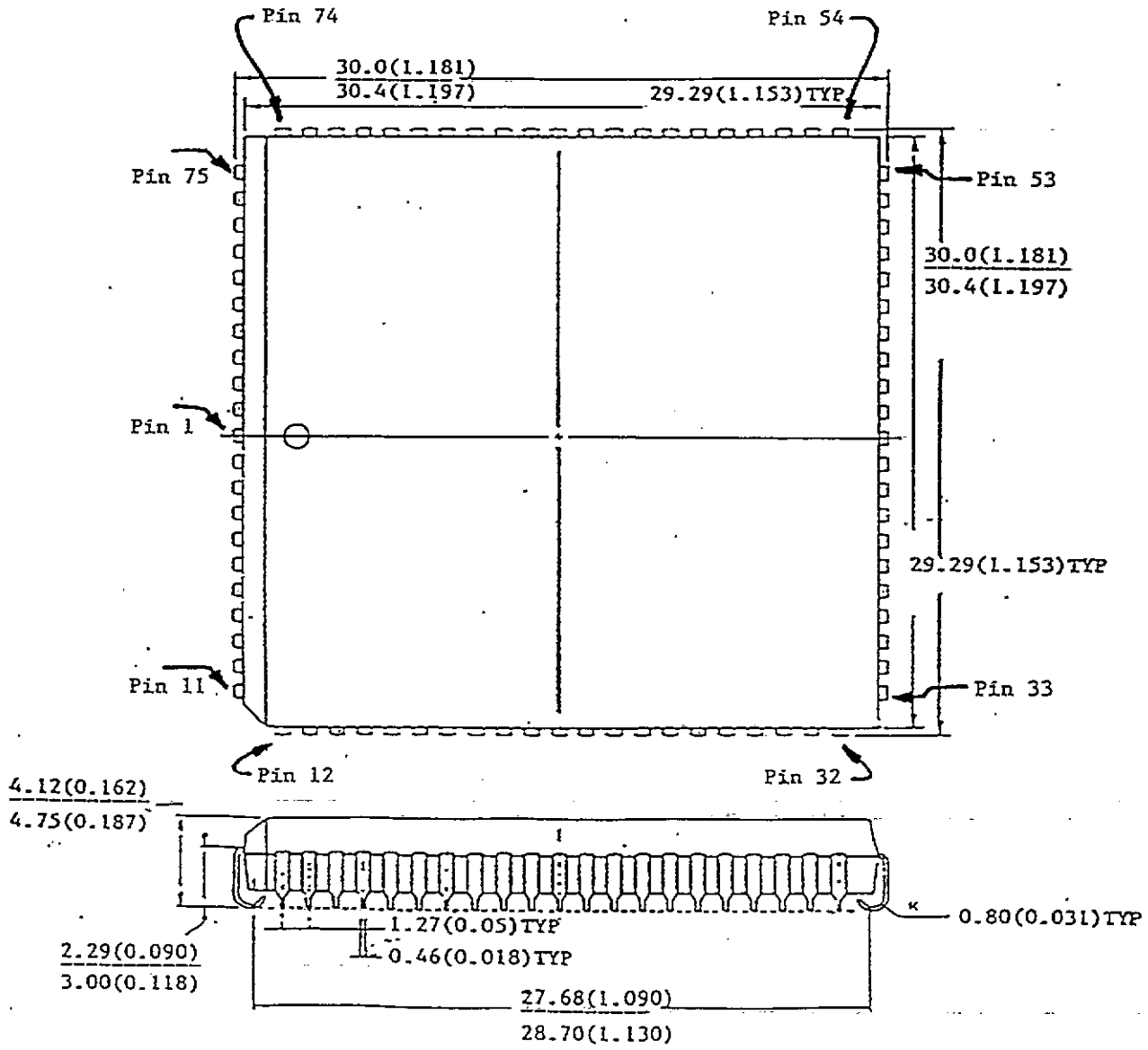
84-Pin Plastic Leaded Chip Carrier



100-Pin Plastic Flat Package



84-Pin Plastic Leaded Chip Carrier



100-Pin Plastic Flat Package