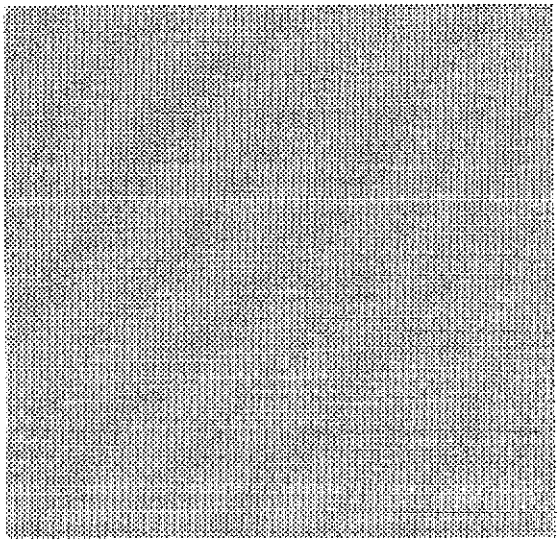
CS8233
PEAK/386 AT
CHIPSet



PEAK/386 AT

Data Book

December 1990

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- Supports 16, 20, 25 and 33 MHz 80386DX based Systems
- Independent clock to support correct AT bus timing
- Flexible architecture allows usage in any iAPX 386 design
- A complete 386/AT Cache based PC AT now requires only 19 IC's plus memory
- Integrates Cache Directory and CPU/Cache/DRAM Controller on a single chip to provide PEAK integration and PEAK performance
- Integrated CPU/Cache/DRAM Controller enhances 80386DX CPU and memory system performance
  - Averages to nearly zero wait state memory access
  - Zero wait state non-pipelined read hit access
  - Zero wait state non-pipelined write access
  - Buffered-write through DRAM update scheme to minimize write cycle penalty
  - Cache hit rate up to 99%
- Supports 32KB, 64KB, and 128KB two-way set associative cache organization
  - 32 byte line size
  - 4 byte sub-line size with associative valid bit
  - Supports blocks (of variable size - 4KB to 4M) of main memory as non-cacheable address space
  - Supports caching of data and code

- Tightly coupled 80386DX interface
  - Designed to interface directly with the 80386DX
  - Supports 16, 20, 25 and 33MHz operation
  - Integrated support for 80387DX a Weitek 3167 coprocessor
- Flexible memory architecture to support:
  - Memory configurations up to 128 MB
  - Programmable DRAM wait states
  - 256K, 1MB, and 4MB DRAMs in configurations of up to 4 blocks and 8 banks
  - Staggered RAS during refresh
  - Hidden refresh and burst refresh
  - 256K/512K/1M PROMs
- Supports shadowing of BIOS EPROMs

Introduction

The CS8233 PEAK/386 AT CHIPSet is a three chip VLSI implementation of most of the system logic required to implement a CACHE BASED iAPX 386DX based system. The CHIPSet is designed to offer a 100% PC AT compatible integrated solution. The flexible architecture of the CHIPSet allows it to be used in any iAPX386DX based system design, such as CAD/CAE workstations, office systems, industrial and financial transaction systems.The CS8233 PEAK/386 AT CHIPSet provides a complete CACHE BASED 386/AT system using only 19 components plus memory devices.The CS8233 PEAK/386 AT CHIPSet consists of one 82C311 CPU/Cache/DRAM Controller, one 82C315 Bus Controller, and one 82C316 Peripherals Controller.The CHIPSet supports a local CPU bus, a 32-bit system memory bus, and AT buses as shown in the system diagram. The 82C311, 82C315, and 82C316 are all available in 160 pin PFP package. Figure 1-1 shows the system block diagram.

The 82C311 CPU/Cache/DRAM Controller

The 82C311 provides the generation and synchronization of control signals for all buses. The 82C311 also supports an independent AT bus clock, and allows selection of different processor and AT bus clock speed.

The 82C311 contains a high performance and high integration Cache/DRAM controller designed to interface directly to the 80386DX microprocessor. By integrating Cache/DRAM control functions on-chip, simultaneous activation of cache and DRAM accesses minimize the cache miss cycle penalty.

The 82C311 Cache Controller supports a two-way set associative cache architecture and cache sizes of either 32KB, 64KB or 128KB. It implements a buffered-write through scheme and a Least Recently Used (LRU) replacement algorithm.

The 82C311 also has hardware support to allow the user to designate up to four blocks (of variable size from 4KB to 4MB) of main memory as non-cacheable address space. This feature is important for compatibility issues when operating in a multi-processing LAN environment, dual-port memory environment, and non-caching of video RAM. In addition, this feature eliminates the need to use very fast PALs externally to decode non-cacheable regions and gives the user much more flexibility.

82C315 Bus Controller

The 82C315 Bus Controller contains the data buffers used to interface between the local, system memory and AT data buses. In addition to having high current drive, they also perform the conversion necessary between the different sized data paths. The 82C315 also includes all the interface logic required to directly interface to the 80387DX and Weitek 3167 co-processors with no additional discrete logic required.

82C316 Peripheral Controller

The 82C316 Peripheral Controller contains the address buffers used to interface between all address buses and the addresses needed for proper data path conversion. In addition to integrating a variety of TTL/SSI interface logic, the 82C316 includes the equivalent of the 82C206 Integrated Peripheral Controller (IPC). The IPC section contains:

- Two (2) 82387 DMA controllers
- Two (2) 8259 interrupt controllers
- One (1) 8254 timer/counter
- One (1) MC146818 real time clock
- One (1) memory mapper

Manual Conventions

The following conventions are used throughout this document to refer to the configuration and diagnostics registers internal to the 82C811, 82C315, and 82C816:

- REGnH denotes the internal register of index n in hexadecimal notation.
- REGnH <x:y> denotes the bit field from bit *x* to bit *y* with index *n* in hexadecimal notation.
- (xxx) denotes default value after power on Reset. Where *xxx* are register bits.

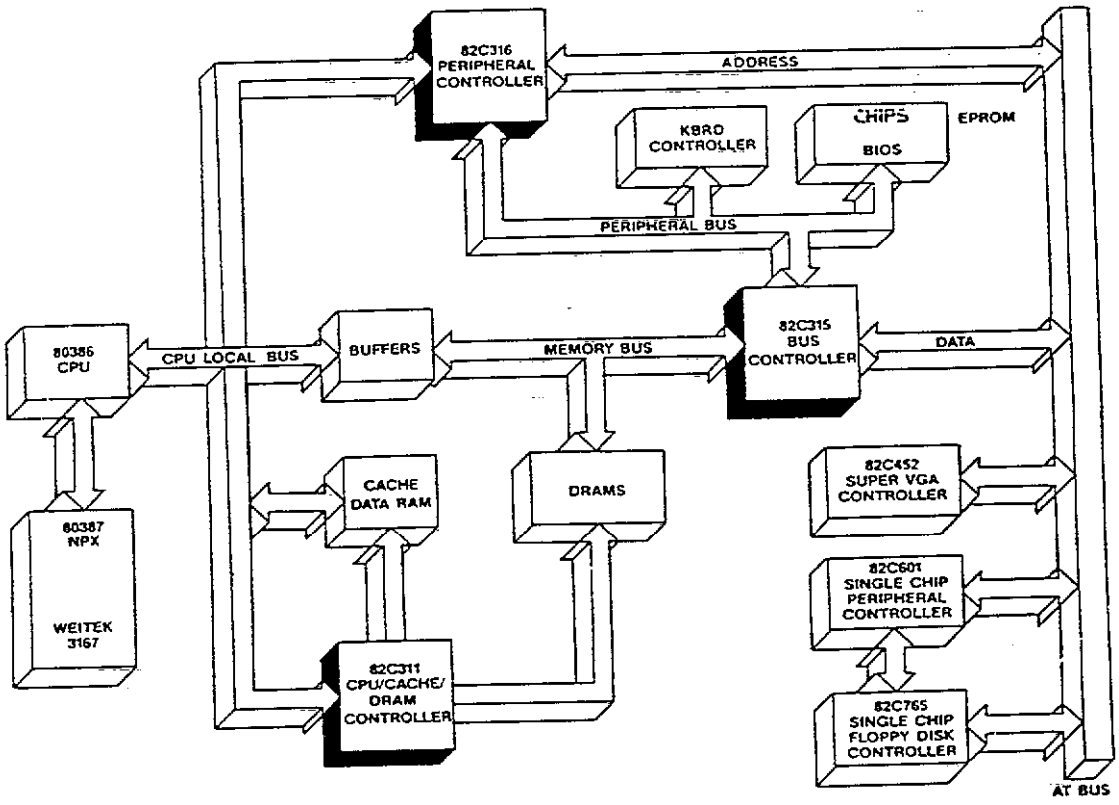
The following methods are used to indicate an active low signals:

- A dash after the signal name
- A bar over the signal name

The following terms are used throughout this document:

- MB = megabyte
- Mb = megabit
- KB = kilobyte
- Kb = kilobit
- ns = nano seconds

Figure 1-1. PEAK/386 System Block Diagram



Section 2

82C311 CPU/Cache/DRAM Controller

Features

The 82C311 provides most of the logic required to interface with the 80386DX processor. The 82C311 also implements state machines required to control the CPU, AT bus, DRAM, and the bus arbitration.

Functional Description

The 82C311 CPU/Cache/DRAM Controller consists of the following functional subsystems as illustrated in Figure 2-1.

- Reset and shutdown logic
- Clock selection logic
- Action code generation and data conversion logic
- State Machines for:
  - CPU
  - Local Memory
  - AT bus
  - Bus arbitration logic
- Memory Control logic for:
  - DRAM Access
  - Cache Memory Access
  - Refresh cycle
  - EPROM Access
  - Shadow RAM
- System control logic
- OS/2 Optimization
  - Fast RESET
  - Fast GATEA20
- 80387DX and Weitek interface logic
- Configuration registers

Reset and Shutdown Logic

Two reset inputs (RESET1- and RESET2-), and two reset outputs (RESET3 and RESET4) are provided on the 82C311. RESET1- is usually connected to the power good signal from the power supply. When RESET1- is active, the 82C311 issues RESET3 and RESET4 for a system reset. Both RESET3 and RESET4 are synchronized with CLK2. RESET3 is active for a minimum of 64 CLK2 cycles. RESET4 is active as long as RESET1- is active. RESET3 and RESET4 meet the setup and hold timing requirements of the 80386 processor.

RESET2- is generated by keyboard controller (8042 or 8742) when a warm reset is used. RESET2- activates only RESET3, and this in turn resets the 80386 CPU.

RESET3 is also activated by the 82C311 when a shutdown condition is detected in the CPU. After a shutdown condition is detected, RESET3 is asserted and is held high for at least 85 CLK2 cycles and then deasserted. An active RESET3 resulting from a shutdown is synchronized with respect to CLK2 to ensure proper CPU operation. RESET3 is also used to reset the coprocessor(80387 or Wietek).

Additionally, a fast reset option is provided in the 82C311 to generate a warm reset without the delays normally associated with the keyboard controller. RESET3 is asserted for at least 85 CLK2 cycles during the power on reset and warm reset.

RSTDRV is used to reset the AT bus. RSTDRV is generated by RESET4. RESET4 is used to reset the 82C316 peripheral controller, and the keyboard controller. It is synchronized with respect to CLK2 and is asserted as long as the power good signal is held low.

Clock Logic

The 82C311 has 3 clock inputs generated by the 82C315, CLK2, SCLK-, and BCLK. CLK2 is the same as the 80386 CPU clock and is used to drive the CPU state machine. SCLK- is the CLK2 divided by 2 and is internally synchronized by the 82C311 to be in phase with the internal states of the 80386 CPU. BCLK is used to drive the AT bus state machine clock and it is also used for the AT bus interface.

The 82C311 has 1 clock output, BUSCLK. It is used to drive the AT bus clock. BUSCLK is equal to BCLK divided by 2.

In traditional AT-compatible designs, the bus clock and the CPU clock are the same. In PEAK/386, it is not necessary for the CPU and the AT bus to share the same clock. The CPU and local memory state machines are typically driven by the CLK2, and the AT bus state machine runs off the BCLK. This allows the CPU to operate at much higher frequencies, while the AT bus runs at an AT-compatible 8 MHz speed. By allowing the different clock source for the CPU and the AT bus, high performance systems can be designed which are compatible with standard AT bus peripherals.

Figure 2-2 shows the phase relationship between the CLK2, SCLK and SCLK-. SCLK is 180 degrees out of phase with SCLK- and is used within the 82C311.

Figure 2-1. 82C311 Block Diagram

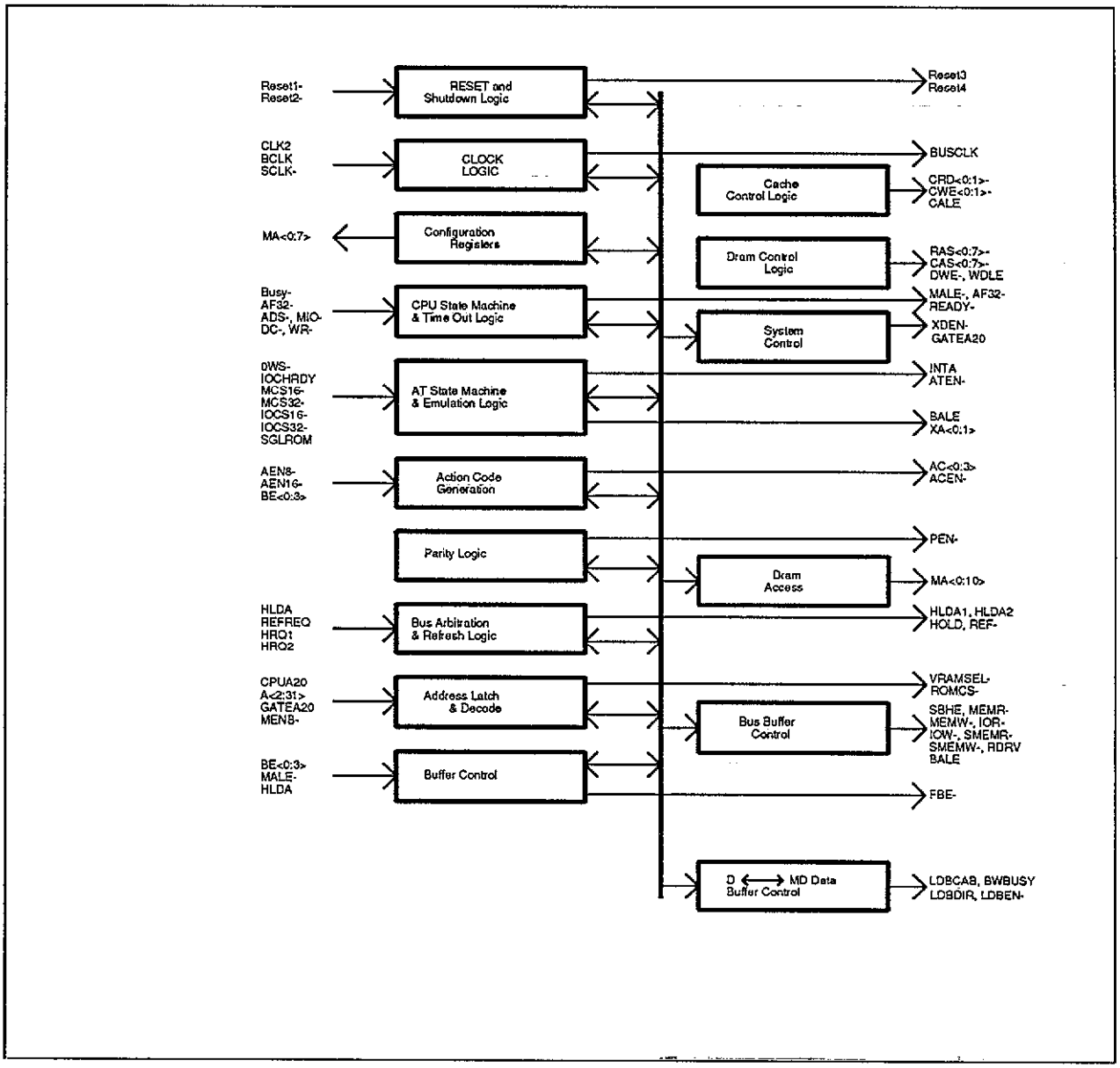
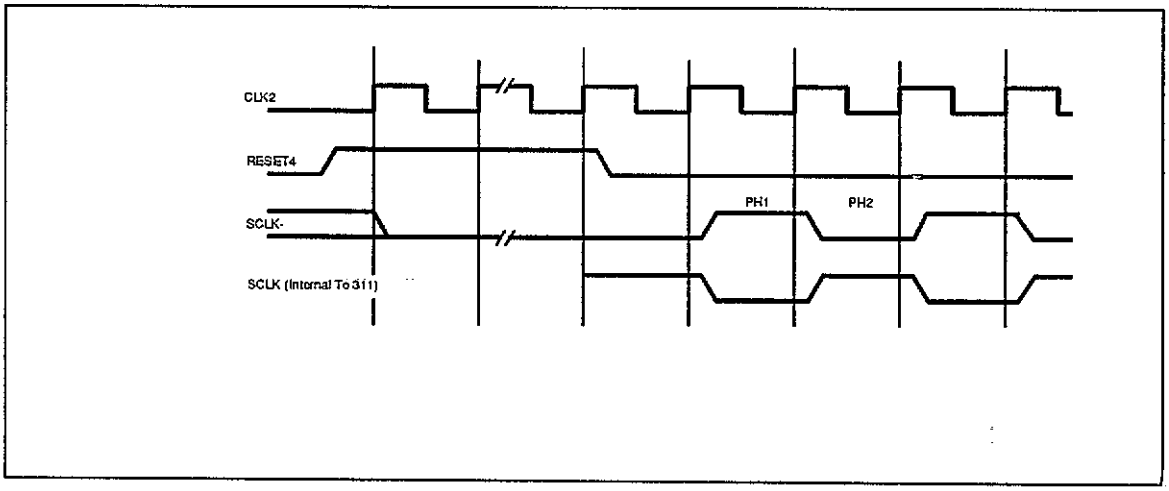


Figure 2-2. Clock Logic



CPU State Machine, Local Memory State Machine, AT Bus State Machine, and BUS Arbitration

The 82C311 contains several state machines to control all the accesses initiated from the CPU, DMA/Master or refresh request to the DRAM, cache memory, or the AT bus.

The CPU state machine and local memory state machine control all the accesses to the local bus (DRAM and cache memory); where the AT bus state machine controls the non-local buses. The CPU state machine and local memory state machine support only 32-bit transfers between the 80386 and the system memory. Because no bus conversions are required, the BS16- input of the 80386 is not used in a PEAK based system and should be pulled high to +5 V.

The AT bus state machine is responsible for all non-local bus accesses and controls the AT bus for proper bus conversions.

CPU State Machine

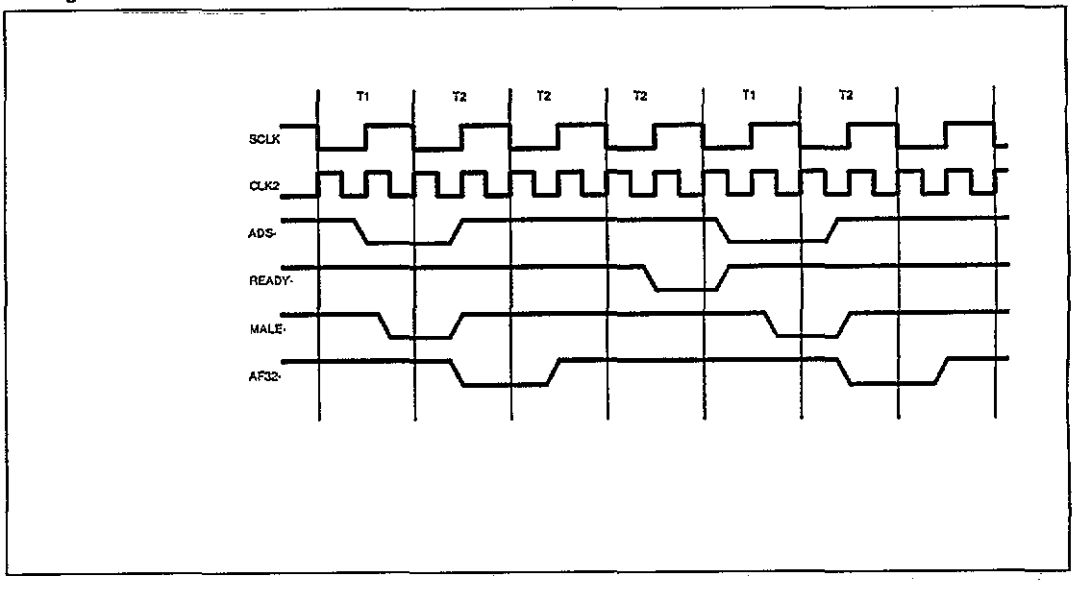
The interface to the 80386 processor requires proper interpretation of the status lines upon assertion of ADS- and generation of READY- upon completion of the requested operation. The 82C311 CPU state machine monitors ADS-, M/IO-, W/R-, and D/C- to determine the CPU's cycle type.

This state machine generates MALE- to indicate the start of a new CPU access cycle. MALE- is generated in response to ADS- being asserted by the CPU.

A local memory access is distinguished from a non-local memory access by assertion of the AF32- signal. The AF32- is generated internally by the 82C311. At end of T2, after generation of MALE-, the CPU state machine samples the AF32-. If AF32- is asserted, it is a local cycle and local bus state machine is activated. In response to MALE-, if AF32- is detected inactive, then the control is passed to the AT bus state machine. The CPU state machine generates READY- when the AT cycle has completed. Figure 2-3 shows the timing relationship for the MALE- and AF32- in respect to CLK2, ADS-, and READY-.

AF32- is an open collector signal and can be pulled low by external logic if a local cycle is required. For example, if there is a special device on board which

Figure 2-3. CPU State Machine



responds to an address range above 16 megabytes, the AF32- can be pulled low to accomodate that address range; so that 311 generates local cycle instead of AT cycle. The READY- should be generated by the special device at the end of the cycle. Refer to Index Reg<08> for more details.

Local Memory State Machine

When AF32- is asserted at start of the memory cycle, then the 82C311 starts its local memory state machine and does not allow the AT bus state machine to begin. The local memory state machine generates the corresponding RAS- and CAS-and other control signals. It can be programmed to insert wait states in units of SCLK (two CLK2) to extend the memory cycle such that slower DRAMs may be used to implement the memory sub-system.

At end of the cycle, the local memory state machine generates READY- to terminate the local cycle. If the 82C311 local memory state machine does not generate READY- after 128 clock cycles, then the 82C311 AT bus state machine optionally (if bit 2 of register 26 is set to 1)generates READY-, The 82C316 sets a bus time out flag in one of its internal registers, and generates NMI if it is enabled.

AT Bus state Machine

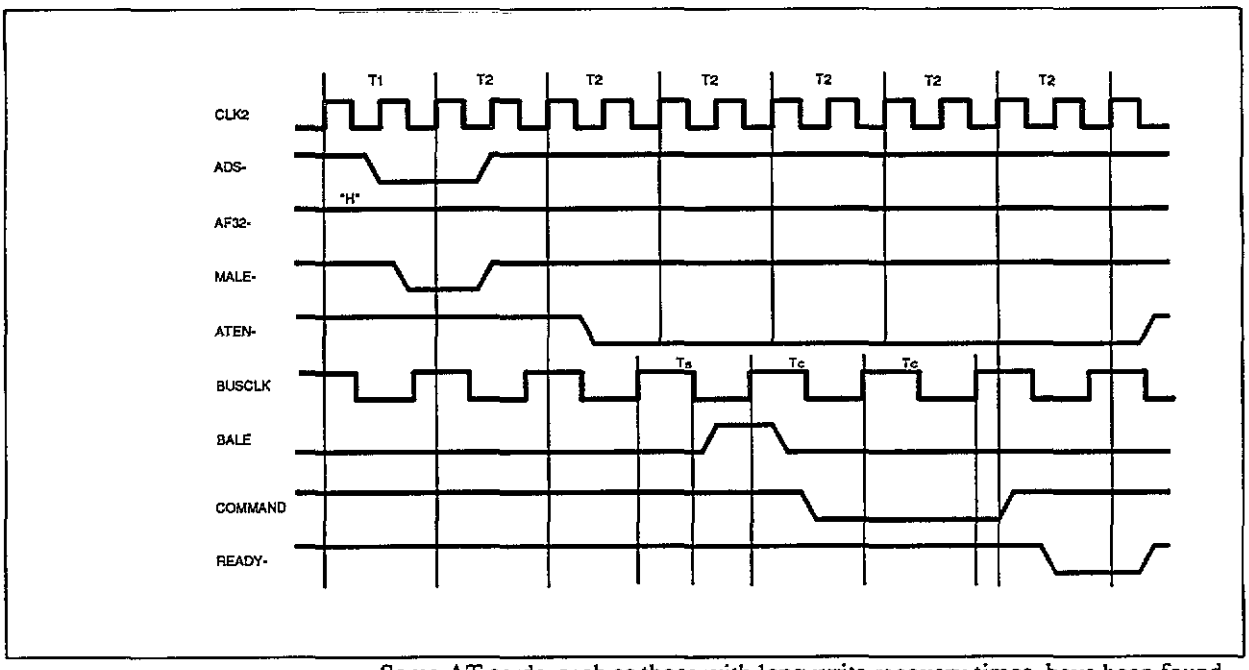
The AT bus state machine is activated when the AF32- is not active at the end of T2. The AT state machine is driven by BCLK, which is two times the frequency of the AT system clock, BUSCLK. The 82C311 performs the necessary synchronization of control and status signals between the AT bus and the processor. The 82C311 supports 8- , 16-, or 32-bit transfers between the processor and 8-, 16-, or 32-bit memory or I/O devices located on the AT bus.

An AT bus cycle is initiated by asserting the BALE signal and is terminated by asserting READY-. After a programmed number of delays, AT state machine then enters the command phase. The command signals for the memory or I/O remain active until the programmed number of wait states are executed. On the falling edge of the BCLK, IOCHRDY is sampled. If IOCHRDY is active, the command becomes inactive on the next rising edge of BUSCLK. If IOCHRDY is not active, the commands are extended for an additional cycle and IOCHRDY is sampled again. This process continues indefinitely until IOCHRDY becomes active.

The AT bus state machine has programmable registers(registers 05, 06) to provide additional wait states or delay the command (MEMR-, MEMW-, IOR- and IOW-) These controls provide more setup time for slow AT bus peripherals to maintain compatibility. These registers can be programmed to insert wait states(wait states are additional BUSCLK cycles added to the time a command is active) in units of BUSCLK and to delay the generation of IOR-, IOW-, MEMR-, MEMW- commands in one half units of BUSCLK (a command delay is one BCLK delay between end of BALE and start of command)within the selected wait states.

The 0WS- signal from AT bus is sampled in the middle of Tc (falling edge of BUSCLK) and if 0WS- is active the command is terminated at the end of Tc. Thus, a 0 wait state AT cycle consists of two BUSCLK cycles, Ts and Tc. The READY- to the CPU is generated by the 82C311 one or two CLK2 after the command is terminated. Figure 2-4 shows the timing diagrams for a one wait state AT bus cycle.

Figure 2-4. Bus Arbitration (REF)



Some AT cards, such as those with long write recovery times, have been found to perform better with "additional address hold time." *This is a programmable* option (programmable via Register 05H, bit 1) that delays the generation of READY to the CPU by 2 CLK2 (one CPU T state). This causes the current address to remain on the bus for one additional T state.

Action Codes Generation and Data Conversion Logic

The AT bus state machine provides controls to the 82C315 to perform data conversion for CPU accesses to devices not on the CPU or memory bus. The AT bus conversions are performed for 32-, 16-, and 8-bit read or write operations. 32-bit transfers to or from the CPU are broken into smaller 16- or 8-bit AT bus or peripheral bus reads or writes. When performing the data conversions, 4-bit action codes AC<0:3>, are generated to control the buffers in the 82C315 for the alignment of data paths and to control the direction between the D, MD, and SD data buses. The definitions for the action codes are given in the functional description of the 82C315. Byte addresses XA<0:1> are generated to drive the lower two bits of the AT address bus during AT cycles. -SBHE is generated when a high byte transfer is taking place.

During memory cycles, on the falling edge of BALE, MCS16- and MCS32- are sampled to determine the bus size conversion required. During I/O cycles, IOCS16- and IOCS32- are sampled on the falling edge of BALE and must remain valid for the duration of the cycle. If none of the above signals are asserted, 8-bit transfers are assumed and the request is converted into 2, 3, or 4 AT bus cycles; based on the CPU byte enable signals BE<0:3>-. When MCS16- for memory or IOCS16- for I/O is asserted, the AT bus state machine converts a 32-bit access into two 16-bit AT bus accesses.

The AT bus state machine also supports 32-bit transfers between the processor and the memory or I/O devices on the AT bus. MCS32- and IOCS32- inputs allow a device to request a 32-bit transfer. The AT bus has to be extended to 32-bit wide in order to utilize this feature (currently there is no AT bus

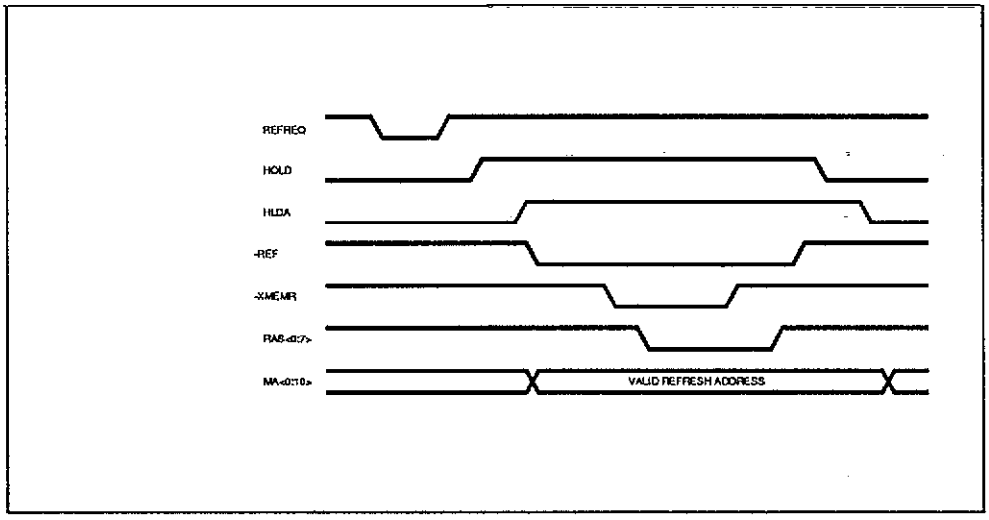
specification for 32 bit bus transfer). MCS32- and IOCS32- have priority over the MCS16- and IOCS16- signals.

A master cycle is a cycle where an AT card will take control of the bus (for example a disk controller). Before an AT bus master takes control, The CPU should program a DMA channel (the bus master uses this channel) in cascade mode. The bus master pulls DREQ- low and once the 82C316 provides the DACK- signal to the master, the master pulls MASTER- signal low. During master cycles, the MASTER- input is low to the 82C311, indicating that it is a master cycle. The 82C311 provides logic for master to access DRAM and on board I/O ports. the 82C315 does data path steering for master cycles. The 82C316 provides the address path via SA and A lines during master cycles. MASTER- should not be held for more than 15 micro seconds without requesting a REFRESH, or else data in the system memory may be lost due to lack of refresh cycles. The bus master pulls REF- low and the 82C316 generates the refresh address for the AT bus and the 82C311 generates MA<0:10> MEMR-, SMEMR- signals to refresh the memory on the AT bus and the local memory.

Bus Arbitration

The 82C311 controls bus activity and provides arbitration between the CPU, DMA, bus MASTER devices, local masters, and AT refresh logic. For any of these other devices to gain control of the system, the CPU must be put into hold. The 82C311 arbitrates between HRQ1, HRQ2, and REFREQ in a non-preemptive manner by generating HOLD request to the CPU. The CPU relinquishes the bus by issuing HLDA. The 82C311 responds by issuing

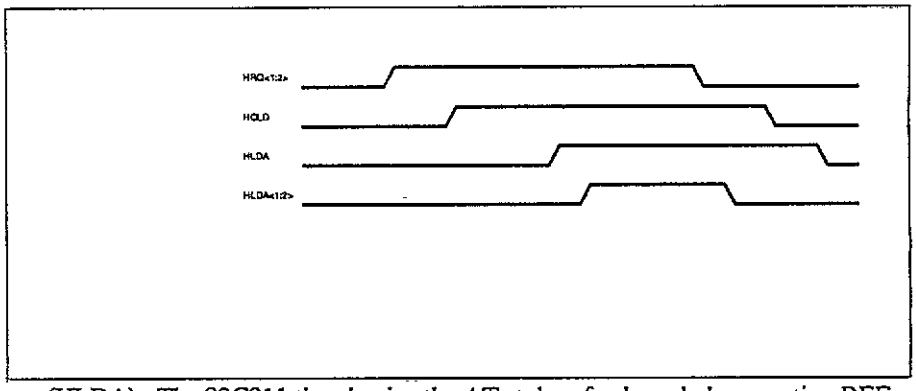
Figure 2-5. Refresh Cycle Arbitration



HLDA1, HLDA2, or REF- depending on which device prevailed during arbitration. During the AT style refresh cycles, the refresh logic has control of the bus until REF- goes inactive. During a DMA cycle, the DMA controller has control of the bus until HRQ becomes inactive. the 82C311 controls the bus sizing and conversion with the action codes.

Figure 2-5 shows an AT style refresh cycle arbitration. The rising edge of REFREQ sets an internal flag in the 82C311. On the first rising edge of BUSCLK, a HOLD request to the CPU is generated. When the CPU finishes with its current activity, it releases the BUS and activates hold acknowledge

Figure 2-6. DMA Arbitration



(HLDA). The 82C311 then begins the AT style refresh cycle by asserting REF-. There is no bus arbitration for hidden refresh as CPU is not put on hold.

Figure 2-6 shows a DMA cycle arbitration. If a DMA device requests control of the bus, it activates HRQ1 or HRQ2. The 82C311 receives HRQ1 or HRQ2 and issues a HOLD request to the CPU. After HOLD is active, the 82C311 issues an HLDA1 or HLDA2 and relinquishes the bus. Once the DMA device is no longer asserting the HRQ1 or HRQ2, the 82C311 desserts the HLDA1 or HLDA2 and returns the control to the CPU. HRQ2/HLDA2 are for local masters. The data buffers do not turn around, and the 82C311 does not generate byte enables from XA<0:1> and SBHE.

Memory Control logic

The 82C311 provides all the logic to interface to the DRAM and cache memories. It utilizes two way set associative cache organization of up to 128KB and conventional DRAM accesses of up to 128MB. It also contains the logic to perform refresh, DMA, access EPROMs, and shadow RAM.

DRAM Access

The 82C311 provides the control logic for generating RAS<0:7>-, CAS<0:7>-, MA<0:10> and DWE- to control the DRAM accesses. It also provides LDBCAB, BWBUSY, LDBDIR, and LDBEN- signals to control the direction of the data flow between the D and MD buses through a set of external 74F646 transceivers.

The 82C311 supports 256K, 1MB, and 4MB DRAMs in configuration of up to 4 blocks or 8 banks,thereby providing a maximum of 128MB of memory. Each block has 2 banks, every two banks within a block have their own configuration register (REG10 thru REG18) to allow usage of different type/speed of DRAM and to program their starting addresses. For example, Index Reg 10 determines the starting address for BLOCK0 (banks 0 and 1) and the type of DRAMs used. If 256K type DRAM is used, and the starting address is set to 0, then banks 0 and 1 will cover address ranges from 0 to 2MB. The starting address for block 1 (banks 2 and 3) then begins at 2MB. Register 11 is used to program wait states for BLOCK 0 and RAS precharge time for DRAMs in block 0. Register 11 is also used to program RAS pulse width during refresh for all eight banks. Parity generation and checking is also implemented in conjunction with the 82C315 data buffers.

The 82C311 controls the DRAM memory accesses from three sources:

- CPU
- DMA request
- Refresh request
- MASTER

These accesses are arbitrated based on the inputs HLDA1-, HLDA2, MASTER-, and REF-; and are handled by their own state machine.

The refresh state machine is in control whenever REF- is active. When HLDA<1:2> is active, the DMA state machine is in control. In all other cases, the CPU state machine is in control for valid DRAM memory accesses as defined by the memory map in the configuration registers. The arbitration is not preemptive, that is, the current active state machine always runs to completion prior to relinquishing the control of the system.

The CPU initiated accesses are decoded according to the memory map defined in the configuration registers. These accesses are conventional DRAM accesses; DRAM access begins by strobing in a valid row address with RAS- while CAS- remains high. Then, the addresses on MA<0:10> are changed from row addresses to column addresses and strobbed in by CAS-. This is the beginning of the DRAM cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the DRAM write enable pin and other control signals. The DRAM cycle is terminated when both RAS- and CAS- are returned to the high state. The 82C311 generates READY- to terminate the current CPU cycle. DWE- is connected to each DRAM write enable input.

During a DRAM write cycle, the parity bits (one parity bit for each byte) are generated by the 82C315 (if PEN input is low). These bits are written into DRAMs along with the data. During the DRAM read cycle, the data and parity bits are strobed into the 82C315 data buffer on the rising edge of CAS (generated by the 82C311 which is a combination of CAS signals for all banks). The 82C315 generates internal parity and compares with the parity read. If a parity error is present, LPAR- is generated by the 82C315, and 82C316 generates NMI to the CPU. The parity checking can be turned off by programming the index register 28 (bit 7) in the 82C311. When the parity checking is turned off, the parity enable signal (PEN-) is high from the 82C311 and parity checking logic is disabled inside the 82C315.

Posted Write Cycle

During a DRAM write cycle, the data is written into 74F646 buffer and the READY- is generated by the 82C311 at the end of the first T2; thus providing zero wait state write cycle. The actual write to the DRAM takes place subsequently. If the next cycle is a read hit cycle, the cache access is performed while main memory is being updated. This is the posted write cycle which increases the performance of the system. If a DRAM write cycle is already in progress, then the 82C311 does not perform another posted write cycle or read miss cycle, but waits until the current write cycle is completed. Therefore, if two consecutive DRAM write cycles are performed, the first cycle is zero wait state write cycle and the next DRAM write takes place after the first write is completed.

DMA accesses are initiated by asserting HLDA1 or HLDA2. The MEMR- and MEMW- determines if it is a read or write memory access. The bytes accessed are controlled internally with the BE<0:3> signals that are generated by the 82C311 based on XA0, XA1, and SBHE-. The DMA state machine makes one memory access per DMA bus cycle and does not attempt to pack or unpack data transfers to make full 32-bit transfers. The 82C311 supports both one wait state and zero wait state posted write cycles(This feature is not supported in revision B of the 82C311).

Cache Access

The 82C311 supports 32K, 64K, and 128K of cache memory organized in a two way set associative manner. All cache memory cycles: read hit, read miss, write hit, write miss are explained, in detail, in the section entitled *Cache Operation.* The 82C311 provides all the logic for generating CRD<0:1>-, CWE<0:1>-, and CALE signals to control the cache memory. For a detailed description of cache organization and structure, refer to the Cache section.

The cache memory doesn't have its own separate state machine to control its accesses. It is controlled by the CPU state machine during the read hit cycles and local memory state machine for all other cycles.

Refresh Cycle

The 82C311 provides the following refresh schemes:

- AT style refresh
- Burst refresh
- Hidden refresh

In an AT style refresh scheme, The 82C311 arbitrates the bus after receiving the REFREQ, and generates a HOLD request to the CPU. The CPU relinquishes the bus by issuing HLDA. The 82C311 responds by issuing REF- and starts the refresh cycle. After REF- is activated, the 82C311 places the refresh address on the MA<0:10> but and activates MEMR-. After refresh cycle is completed, REF- and MEMR- are driven to inactive states. HOLD is also returned to inactive state, and the CPU regains control of the bus. RAS-Only refresh is performed by strobing in a row address while CAS- remains high.

The Burst refresh allows multiple AT style refresh cycles per one refresh request (REFREQ) and ignores the next programmed number of incoming REFREQ; depending on its programmed state. The configuration register REG2B<1:2> controls the number of burst refresh cycles. The number of refresh cycles per REFREQ can be programmed to 4, 8, and 16. For example, when the 82C311 is programmed for burst of 8, it performs 8 refresh cycles per REFREQ and ignores the next 7 REFREQ. The advantage of performing burst over the single cycle refresh is in the refresh arbitration overhead required on every cycle. Thus burst refresh reduces the refresh overhead. The CPU stays on hold during the entire burst refresh cycle.

During the hidden refresh cycle, the 82C311 does not go through the bus arbitration, HOLD, and HLDA sequences. The hidden refresh is transparent to the CPU, allowing the CPU to continue operating from its cache memory. Therefore, hidden refresh and CPU cache hit cycles may occur concurrently. The CPU has to wait for all other accesses requiring the DRAM. All DMA and AT bus accesses are deferred until the completion of the on-going hidden refresh cycle.

Figure 2-7. Burst (of 4) Refresh Timing Diagram

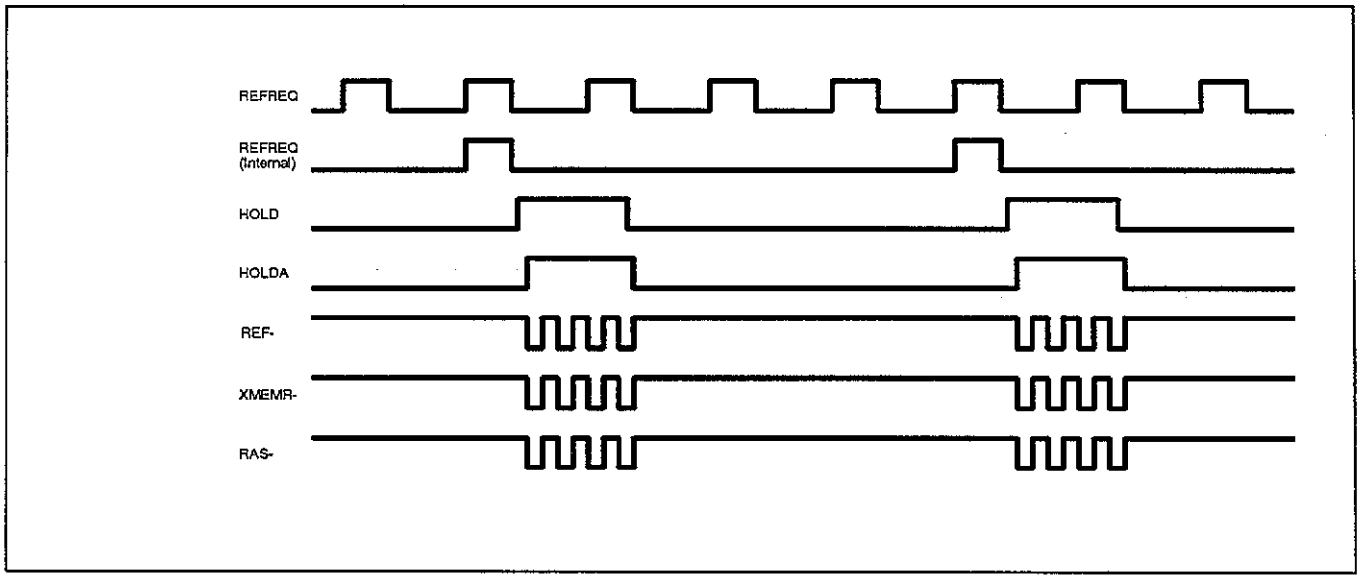


Figure 2-8. Hidden Refresh

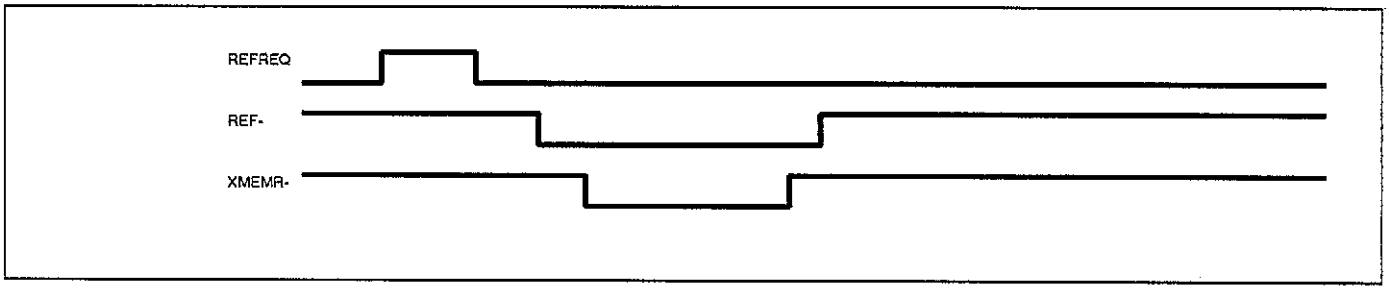


Figure 2-7 and 2-8 show the timing sequence for burst and hidden refresh cycles, respectively.

EPROM Control Logic

The 82C311 provides the control logic to generate the ROMCS- signal for EPROM accesses. The AT bus state machine generates the READY- for this cycle. ROMCS- is connected to the EPROM chip enable (CE-) input. ROMCS- is always generated for the address range:

1. FFFC0000H to FFFFFFFF.
2. 00FC0000H to 00FFFFFFH if index register 2C enables the ROM.
3. 000C0000H to 000FFFFF if index register 09 enables the ROM. The power up default has ROM Chipselect at the top 256K at 4Mb, top 64K at 16Mb, and top 64K at 1Mb.

Shadow RAM

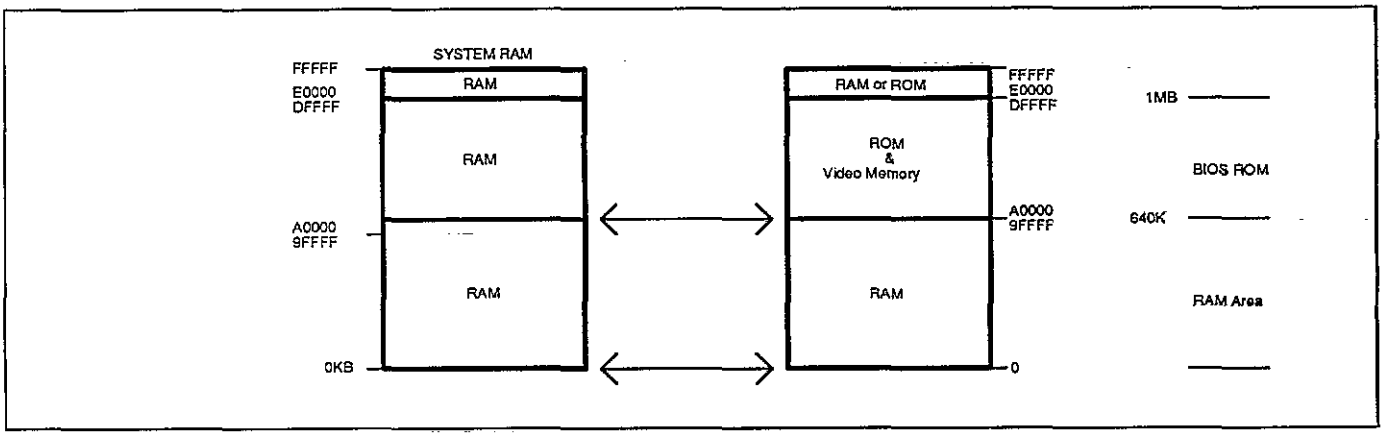
In order to enhance system performance, it is preferable to execute BIOS code through RAM rather than through slower EPROMs. The 82C311 provides a feature called shadow RAM that, when enabled, allows BIOS code to be executed from system RAM resident at the same physical address as the BIOS

EPROM. The software should transfer code stored in the BIOS EPROMs to the system RAM before enabling the shadow RAM feature. This feature significantly improves the performance in BIOS-intensive applications. Performance improvements as high as 300% to 400% have been observed in shadow RAM benchmark tests. The shadow RAM feature is invoked by enabling the corresponding bits in the ROM enable register and RAM mapping registers (REG9H, REG0EH, and REG0FH). Figure 2-9 shows the system memory with and without shadow.

Index registers 09 and 2C provide the option to disable writing to the RAM located in the BIOS area. Register 09 is used to enable or disable writing to the address range C0000H to FFFFFH. Each bit register disables or enables a 64K block of RAM. Similarly, register 1C provides the option to enable writing in the RAM area FC0000H to FFFFFFH.

Index register 0C through 0F provide the option to turn off the RAM on the system board from 512K to 1MB. These registers are enabled if bit 1 of register 8 is set to 1.

Figure 2-9. *Shadow RAM*



System Control Logic

The system control logic of the 82C311 generates the LDBEN-, LDBDIR-, XDEN-, and AF32- for system control. XDEN- is issued for I/O accesses to the internal configuration registers of the 82C311. It is used to enable the XD<0:7> onto the MA<0:7> address lines from an external buffer, for accessing the internal registers. LDBEN- and LDBDIR- are generated for enabling and controlling the 74F646 data buffers. AF32- is generated for local 32-bit memory accesses.

OS/2 Optimization

The PEAK/386 architecture features OS/2 optimization using fast reset and fast GATEA20 (FGA20). OS/2 makes frequent DOS calls while operating in protected mode of the 80386 CPU. In order to service these DOS calls, the CPU has to switch from protected to real mode quickly. Typical PC/AT architectures require the processor to issue two commands to the 8042 (or 8742) keyboard controller in order to reset the processor and to activate GATEA20. REG60<5> of the 82C311 is used to invoke a software reset and REG2B<6> is used to enable/disable the fast GATEA20. When fast GATEA20 is enabled, the 82C311 detects the I/O writes to keyboard controller port 60 and 64 and generates the GATEA20 internally. Therefore, the GATEA20 signal from the keyboard controller has to be connected through an open collector gate to the 82C311. When fast GATE20 is enabled using REG2B<6> the software should do I/O writes to port 60 and 64 to activate GATEA20. In the 82C311C the REG2F<5> is available to enable fast GATEA20 and writing to port 60 and 64 is not required when REG2F<5> is used. Hence,this is a faster way of implementing GATEA20. The REG2F<5> overrides REG2B<6> when the fast GATEA20 is enbaled in REG2F<5>. In order to disable fast GATEA20 in the 82C311C both REG2B<6> and REG2F<6> should be disabled.

80387DX and Weitek Interface

The 82C311, in conjunction with the 82C315 and 82C316, provides the logic necessary to interface with the 80387 and Weitek coprocessors.

The 82C311, during the 80387 cycle, generates an AF32- to set the current cycle into a non-AT cycle. The 82C316 generates the READY- at the end of the cycle.

If the Weitek WT3167 coprocessor is addressed and is not present, then the 82C311 generates READY- to terminate it. When the Weitek WT3167 is present and is addressed, the AF32- and READY- are generated by the coprocessor. The WT3167 memory address range is C0000000H to C1FFFFFFH. This address range is not accessible if the Weitek processor is not present. However, external logic present (on the motherboard) in this address range can force a local memory cycle by either pulling AF32- low or WTPRES- low. The external logic should generate ready.

During RESET1-, or power ON, the 80387 pulls the error signal low. The error signal is connected to the 82C315, latched by the falling edge of RESET4. If error is low, then bit 4 of Register 7 is set in the 82C315. The BIOS should read Register 7 and set bit 0 of Register 2B to 1.

Cache Functional Overview

The functional overview outlines the cache architecture and provides an insight into the operation of the 82C311 with 80386 interface. The 82C311 performs as an integrated CPU/Cache/DRAM memory controller in an 80386 based system. By maintaining the most frequently accessed code and data in high speed memory, it allows the 80386 processor to operate at its maximum rated frequency with near zero wait states.

The 82C311 cache controller portion is designed to be a cost effective solution for achieving the full performance of the 80386 based system. This is accomplished by maintaining the most frequently accessed code and data in high speed memory (cache memory) such that most memory requests can be satisfied from this memory. If the data resides in the cache memory (hit), the data is returned to the 80386/486 without wait states. If the data is not present in the cache memory (miss), then it is retrieved from the slower main memory with wait states.

Since the cache controller and the main memory controller are both integrated into a single device, cache memory access is performed in parallel with the main memory access. In case of a hit, main memory access cycle is terminated and the data is provided by the cache memory. In case of a miss, the main memory cycle is completed. Performing cache access and main memory access in parallel reduces the miss penalty.

During write operation, the data is held in a temporary buffer and the CPU is released so it can start a new cycle before the write cycle to main memory is completed. However, if another write cycle or a read miss cycle is performed, then additional wait states are inserted until the previous cycle is completed.

The effectiveness of the cache is determined predominantly by the size and organization of the cache, the hit and miss access times, and the dynamic behavior of the program. An efficient cache organization results in a high hit rate. The majority of the accesses are to cache and are completed without wait states. Very few accesses are to the main memory. Consequently, the average access time approaches that of the fast cache memory.

The 82C311 integrates the cache directory and the control logic required to support an external 32K/64K/128KB Cache and up to 4 blocks of 2 banks of DRAMs. The cache directory supports two way set-associative cache organization and maps 128MB of memory space. The minimum amount of local memory is 1MB if 256Kb memory devices are used (If 1Mb DRAMs are employed, the minimum amount of local memory is 4MB; and if 4Mb DRAMs are employed, the minimum amount of local memory is 16MB). A memory enable map is provided for memory residing within the 1MB memory address space. This mechanism can be used to prevent contention between the 1MB local memory and memory residing at predefined addresses on the AT expansion bus. For system memory above 1MB, memory can be installed in increments of 1MB.

All DRAM access and refresh control signals are presented by the 82C311 with programmable configuration for 256Kbx1, 256Kbx4, 1Mbx1, 1Mbx4, 4MbX1, and 4MbX4 devices. Every block can have different type/speed of memory devices and its starting address. Parity generation and checking is implemented in conjunction with the 82C315 data buffers.

The on-chip tag RAM directory can be accessed through the 8-bit peripheral data bus. The entire tag directory RAM can be written or read through I/O instructions for initialization or diagnostic purposes through REG21, REG22, REG23, and REG25. See the section titled *Cache Directory Testing* for more details.

Cache Concepts

Cache memory optimizes processor performance and enhances bus-bandwidth within cost, size, and power limitations. A cache reduces the average access time if it is organized such that it holds the most often requested code and data. The effectiveness of the cache is determined by the size, the physical organization, cache replacement algorithm and the behavior of the program. When a cache satisfies the processor access requirements, the overhead resulting from accessing the slower main memory is eliminated. The cache can operate at the speed of static memories while maintaining the economic advantages of a slower main memory storage.

Program Locality

Almost all programs exhibit some "locality of references." Programs usually access memory in the neighborhood of locations already accessed recently. Program locality makes cache systems possible. There are two aspects of locality:

- Temporal
- Spatial

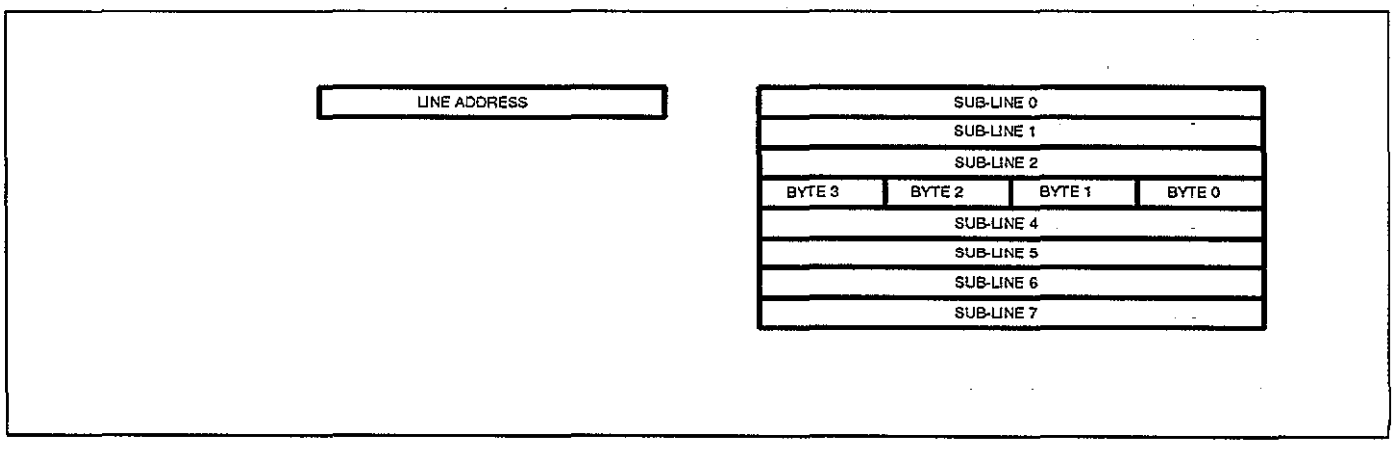
According to temporal locality, information used in the future will already be in use. This type of program behavior is exhibited by program loops in which the code and data are reused.

According to spatial locality, programs generally consist of a fairly small number of individually contiguous segments of memory. A cache memory buffers these contiguous segments, thereby increasing the probability that the requested code and data can be found in the cache.

Cache Size

The cache size is one of the most important parameters in terms of both cost and performance trade-offs. Cache miss rate reduces asymptomatically with the size of the cache. The increase in performance with an ever increasing cache size reaches a saturation point. Increasing the cache size beyond this point only increases the cost of the memory subsystem with minimal improvement in performance. The 82C311 supports 32K/64K/128K of cache memory.

Figure 2-10. *Line of a Cache*



Cache Organization

The basic characteristic of a cache is the fast access time. Therefore, very little or no time must be wasted when searching for words in the cache. For maximum efficiency, the cache is sub-divided into many smaller blocks of storage called "lines" that range in size from a single machine word (4 bytes in a 80386) to multiple words (32 to 64 bytes).

Each line has an address associated with it that must be stored and compared (using tag comparators) against the address of the memory request. These are kept as entries (one per line) in a directory (tag directory) to establish the correspondence between the data in the cache, and the particular fragment of main memory represented.

If the size of the lines are as small as possible, then the cache directory becomes large since there is a cache directory entry for each line in the cache. Doubling the size of a cache line, while holding the cache size fixed, reduces the size of the directory by a factor of two because two items (sub-lines) in the same line share the same directory entry. Figure 2-10 shows a typical implementation of a line of cache memory. This line is 16 sub-lines wide; where each sub-line is a double word (single addressable item of 80386). Address lines A2 thru A5 determine the desired sub-line within the line.

The 82C311 supports cache line size of 16 double words for 32K and 64KB of cache memory and 32 double words for 128KB cache memory.

The transformation of data from main memory to cache is referred to as the mapping process. Three mapping schemes are normally used:

- Fully associative
- Set associative
- Direct mapped

Fully Associative

Programs consist of various subroutines, stack areas and data variables located at different address locations. Therefore an efficient cache should be capable of holding several non- contiguous blocks of memory. A fully associative cache includes a tag comparator with each entry. A 16 block cache could hold 16 most often accessed blocks. As there is no relationship between the various blocks, it is necessary to maintain the entire address of the block. When the processor presents the address for the next instruction, the cache has to compare the addresses with each of the 16 addresses maintained in the cache. This would require 16 comparisons to determine if a match is found.

Few caches use this organization due to the complex circuitry required and the fact that the decrease in the miss rate achieved with the full associative algorithm is very small. Additionally, the number of comparisons required to determine if it is a hit or miss makes this mapping scheme unacceptably slow and expensive.

Direct Mapped Cache

In a direct mapped cache every memory block has only one possible location in cache. The lower order addresses presented by the processor are used as an index to select one of the entries in the tag directory. The most significant processor address bits are compared with the contents of the tag directory to determine if it is a hit or a miss access. Unlike the fully associative cache organization, only one address comparison is required to determine if the requested data is in the cache.

Direct mapping, while being the simplest to realize, has certain drawbacks. No two addresses with the same index can reside in the cache memory at the same time. If the code jumps back and forth between two address locations that have the same index, the cache controller must access the main memory frequently, as only one of the addressed location can exist in the cache.

Set Associative Cache

The set associative cache compromises between the direct mapped and the fully associative cache. In a set associative cache, the index selects several entries. In a two way set associative cache, two entries can have the same index or the same lower order address bits.

The set associative cache is more complex than the direct mapped cache. In the two way set associative cache, there are two locations for each index field. Two comparisons are required to determine if the requested data is in the cache. Additionally, the tag field is wider and requires larger SRAMs to store the tag information.

Now that two locations exist for each index field, the controller must decide which block to update. When a cache miss occurs and all the locations have been used up, the controller has to decide which location to overwrite. The most common replacement algorithms used are:

- Random Replacement
- First-in-first-out (FIFO)
- Least Recently Used (LRU)

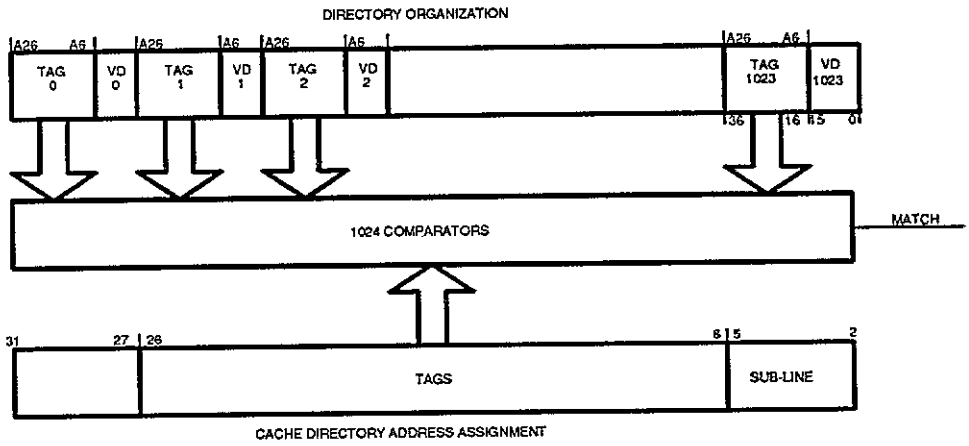
With the random replacement policy, the cache controller choses one tag data item for replacement at random. The FIFO procedure replaces the item that has been in the set the longest. The LRU algorithm selects for replacement the item that has been least recently used by the CPU. The LRU algorithm is the most efficient and can be implemented by adding a few extra bits in each line in the cache.

Cache Illustration

Consider a 64KB cache memory, with 16 Double-Word wide lines.

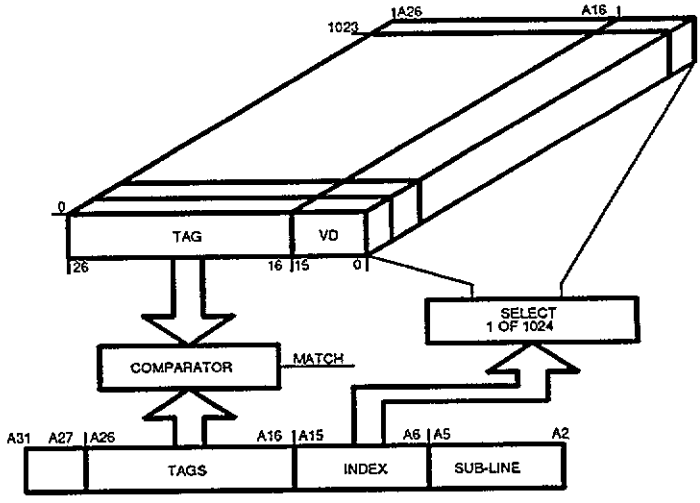
Figure 2-11 shows the implementation of this cache in a fully associative manner. Each tag entry is 21-bits wide and each validity field is 16-bits. To construct this cache, 64KB of cache memory, 1K X 21-bits wide (21Kb) for cache directory, 1K X 16-bits wide (16Kb) for validity field, and 1024 21-bit comparators are required. When the processor presents the address for the next instruction, address lines A6 thru A26 are compared with all 1024 entries of the cache directory to determine a match. A2 thru A5 select a sub-line within the line (one out of sixteen double word).

Figure 2-11. Fully Associative Cache Organization



CACHE SIZE = 64KB
CACHE LINE = 64 BYTES (16DW)
VALID BITS = 16 BITS (1 BIT PER DW)
TAGS SIZE = 21 BITS
FULLY ASSOCIATIVE
DIRECTORY SIZE = 1K X 37 BITS (37K BITS TOTAL)
NUMBER OF COMPARATORS = 1024 21-BIT COMPARATORS

Figure 2-12. Direct Mapped Cache Organization



CACHE SIZE = 64KB
CACHE LINE = 64 BYTES (16 DW)
VALID BITS = 16 BITS (1 BIT PER DW)
TAGS SIZE = 11 BITS
DIRECT MAPPED
DIRECTORY SIZE = 1 X 27 BITS X 1K(27K BITS TOTAL)
NUMBER OF COMPARATORS = 1 11-BIT COMPARATOR

Figure 2-13. Two-Way Set Associative Cache Organization

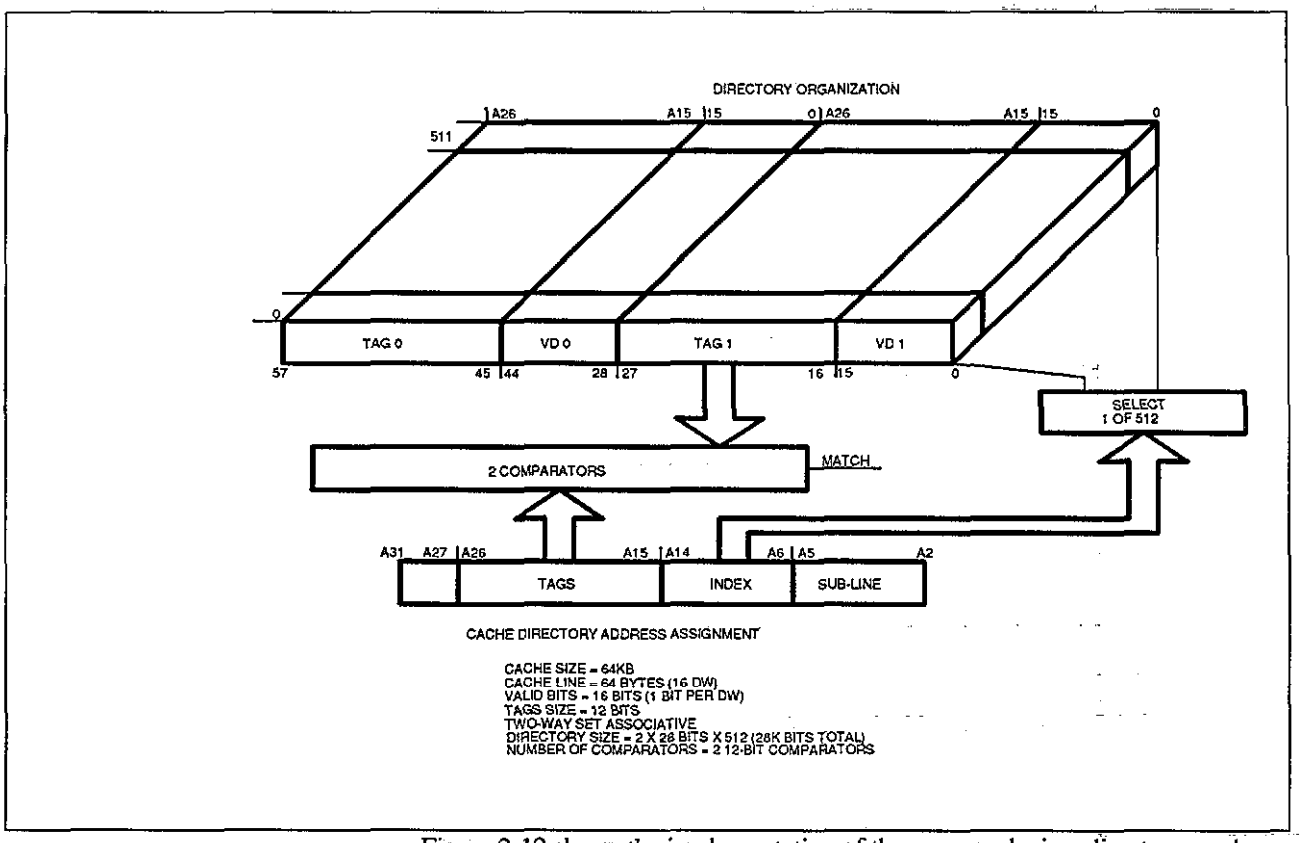


Figure 2-12 shows the implementation of the same cache in a direct mapped manner. Each tag entry is 11-bits wide and each validity field is 16-bits. To construct this cache, 64KB of cache memory, 1K X 11-bits wide (11Kb) for cache directory, 1K X 16-bits wide (16Kb) for validity field, and one 11-bit comparator is required. When the processor presents the address for the next instruction, address lines A6 thru A15 are used as an index to select one entry from the cache directory. The value contained in the tag directory is compared with A16 thru A26. If there is a match, then address line A2 through A5 selects the desired subline within the line and the data is retreived from the cache memory. If a miss is detected, then the data is obtained from the main memory.

Figure 2-13 shows the implementation of the same cache in a two-way set associative manner. Each tag entry is 12-bits wide and each validity field is 16-bits. To construct this cache, 64KB of cache memory, 2 X 512 X 12-bits wide (12Kb) for cache directory, 2 X 512 X 16-bits wide (16Kb) for validity field, and two 12-bits comparators are required. When the processor presents

Figure 2-14. Implementing the Cache

	NUMBER OF COMPARATORS	TOTAL TAG DIRECTORY MEMORY (IN BITS)
FULLY ASSOCIATED	1024 21-BIT	37K
TWO-WAY SET	2 12-BIT	28K
DIRECT MAPPED	1 11-BIT	27K

the address for the next instruction, address lines A6 thru A14 are used as an index to select one line from the cache directory which points to two entries. The values contained in the tag directory are compared with A15 thru A26 to determine a match. If there is a match in any of the two entries, a cache hit cycle occurs; otherwise, a miss cycle in performed.

Figure 2-14 shows the hardware required to implement the cache in three different manners. The amount of hardware required to implement the two-way set associative cache is very close to the direct mapped cache; however, there is a significant difference between the two-way set and fully associative cache. The additional hardware required to implement the fully associative cache does not compensate for the percentile gain in its hit rate.

Cache Updating

Cache maintains a copy of the most often used code of the main memory. The data in the cache should be identical to the main memory. When the cache memory is modified, the data in the main memory has to be updated as well. To meet this requirement, there are two basic approaches: write through and write back.

In a write through system, the controller copies the data into memory as well as the cache. This ensures the main memory and the cache contain the same data. The drawback with this type of implementation is each write cycle is treated as a write miss cycle, and the CPU has to wait for the slow memory to be updated.

Using a buffered write through algorithm, alleviates the problem. During the write operation, data is written into a temporary buffer. The CPU is released to begin a new cycle before the write cycle to the main memory is completed. If a write access is followed by a read hit cycle, the cache access is performed while the main memory is being updated. However, if a write cycle is followed by another write cycle or a read miss cycle, the processor has to wait for the completion of the previous cycle. The buffered write through is by far the most popular implementation.

In a write back system, the memory updates are not performed immediately. This method of implementation adds another bit called the altered bit. This bit is set if the cache is being written to with new data. This bit indicates that the cache data and the main memory data are different and the cache contains the most up-to-date information. When the cache is fully occupied, and a new data has to be brought into the cache, the altered bit is checked to see if the cache and the main memory contain the same data. If this bit is set, then the main memory is updated with the old data present in the cache, before over writing its contents.

This policy is more efficient as the number of accesses to main memory is minimized (main memory is not always updated). But the circuit complexity required to implement this policy defeats the minimal performance improvement.

The 82C311 supports a one stage buffered write through scheme to update the cache.

Cache Coherency

The buffered write through and the write back schemes ensure under normal operations, that the data present in the cache mirrors the data in the main memory. But, in a system environment, other bus masters and slave DMA devices access main memory and modify the contents. cache controllers that have a built in mechanism to update the corresponding cache contents are said to maintain coherency. Many schemes are used to maintain cache coherency, the easiest being to invalidate/flush the cache during DMA operation. This, though convenient, degrades the performance; as all subsequent memory accesses will be misses until the cache is filled with new data. The most popular method of maintaining cache coherency is by ensuring all accesses to the main memory go through the cache controller.

82C311 Cache Organization

The 82C311 supports 32K/64K/128K two way set associative cache organizations. The 82C311, depending upon the size of the cache, uses a configuration of two sets of 256 lines (for 32K) or 512 lines (64K or 128K). This allows two addresses with the same index to be resident in the cache concurrently. For a given cache size, the two way set associative organization yields a significantly better cache hit rate as compared to direct mapped cache. However the increase in hit rate for a four way set associative is not substantial enough to justify the additional complexity.

Two way set associative Cache architecture

Each entry in the 82C311 tag directory corresponds to 64 bytes (16 double words) for 32K and 64K cache memory and 128 bytes (32 double words) for 128K cache memory. It is further sub-divided into 16 sublines of four bytes (double word) each. This reduces the number of tag directory entries and, correspondingly, the tag directory size.

In a two way set associative organization, there are two banks of cache SRAMs and tag directory. For the 32K organization, each SRAM bank is 4K double words (4K X 32 bits = 16KB) and the tag directory consists of 256 entries. For the 64K organization, each SRAM bank is 8K double words (8K X 32 bits = 32KB), and the tag directory consist of 512 entries. Each entry in the tag directory represents 32 bytes of data. For the 128K organization, each SRAM bank is 16K double word (16K X 32 bits = 64KB) and the tag directory consists of 512 entries. Each entry in the tag directory represents 64 bytes of data.

Figure 2-15. *Address Assignment for 32Kb Cache Memory*

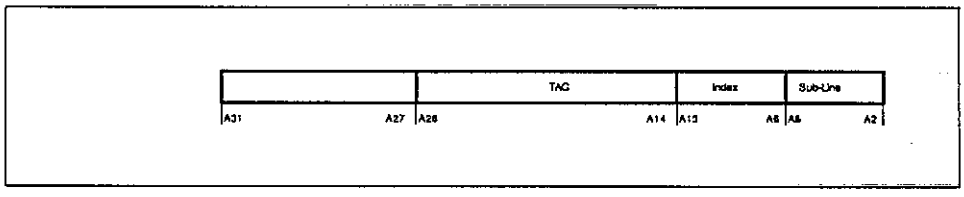


Figure 2-16. Address Assignment for 64Kb Cache Memory

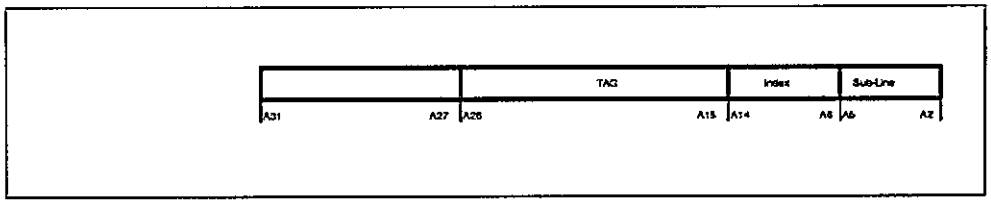
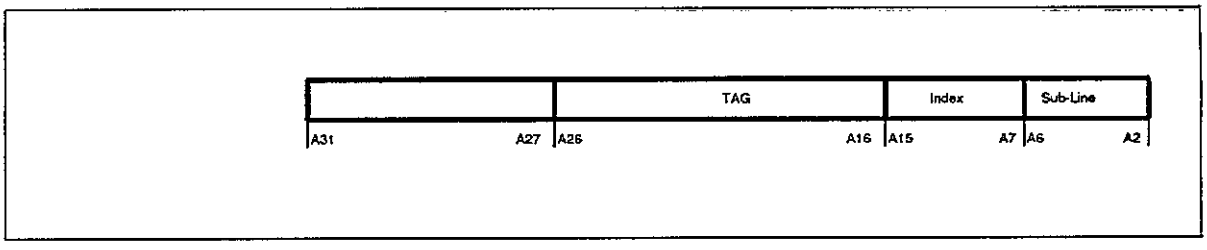


Figure 2-17. Address Assignment for 128Kb Cache Memory



Physical Address Field Assignment

The 80386 supports 32 address bits (30 address bits and four byte enables). While the 82C311 monitors all the 30 bits, it supports a maximum of 128MB of physical memory (A0 thru A26).

The physical address assignments for the 32KB, 64KB and 128KB cache memory are shown in Table 2-1, 2-2, and 2-3, respectively.

Figures 2-15, 2-16, and 2-17 illustrate the cache directory assignment for 32KB, 64K and 128K cache memory, respectively.

Table 2-1. Physical Address Assignment for 32Kb Cache Memory

Bits	Address Field
A<2:5>	Subline Index Selects the subline within a line. There are 16 sublines in a line and each subline can be individually validated/invalidated.
A<6:13>	Line Index Selects the correct line within the cache directory. The line index varies with the size of the cache RAM. For 32Kb, there are 8 address bits corresponding to 256 entries in the directory RAM.
A<14:26>	Address Tag These are the most significant 13 bits of the tag address stored in the tag directory. This address is compared against the tag selected by the line index to determine if the correct line is available in the cache.
A<27:31>	Highest Order Address Bits These bits have to be zero since the system memory has to be located below 128Mb.

Table 2-2. *Physical Address Assignment for 64Kb Cache Memory*

Bits	Address Field
A<2:5>	Subline Index Selects the subline within a line. There are 16 sublines in a line and each subline can be individually validated/invalidated.
A<6:14>	Line Index Selects the correct line within the cache directory. The line index varies with the size of the cache RAM. For 64Kb, there are 9 address bits corresponding to 512 entries in the directory RAM.
A<15:26>	Address Tag These are the most significant 12 bits of the tag address stored in the tag directory. This address is compared against the tag selected by the line index to determine if the correct line is available in the cache.
A<27:31>	Highest Order Address Bits These bits have to be zero since the system memory has to be located below 128Mb.

Table 2-3. *Physical Address Assignment for 128Kb Cache Memory*

Bits	Address Field
A<2:6>	Subline Index Selects the subline within a line. There are 32 sublines in a line and each subline can be individually validated/invalidated.
A<7:15>	Line Index Selects the correct line within the cache directory. The line index varies with the size of the cache RAM. For 128Kb, there are 9 address bits corresponding to 512 entries in the directory RAM.
A<16:26>	Address Tag These are the most significant 12 bits of the tag address stored in the tag directory. This address is compared against the tag selected by the line index to determine if the correct line is available in the cache.
A<27:31>	Highest Order Address Bits These bits have to be zero since the system memory has to be located below 128Mb.

Table 2-4. Cache Directory Organization

Bits	Entry Field	Description
0	LRU	Indicates which set was most recently used.
01:16	VD1	Valid bits for set 1.
17:29	TAG 1	A<14:26> address lines selected by index in set. A14 is ignored for 64Kb cache system. A14 and A15 are ignored for 128Kb cache system.
30:45	VDO	Valid bits for set 0.
46:58	TAG 0	A<14:26> address lines selected by index in set 0. A14 is ignored for 64Kb cache system. A14 and A15 are ignored for 128Kb cache system.

Cache Directory Organization

There are 59 bits per entry in the cache directory. The various fields within the entry are defined in Table 2-4.

Figures 2-18 and 2-19, and 2-20 illustrate the cache directory organization for 32K, 64K, and 128K cache memory, respectively. There are 59 bits per entry in the cache directory.

Figure 2-18. Directory Organization for 32Kb Cache Memory

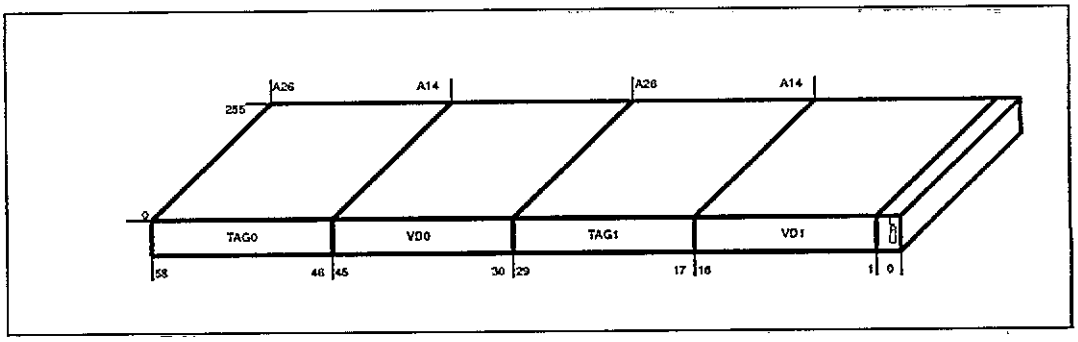


Figure 2-19. Directory Organization for 64Kb Cache Memory

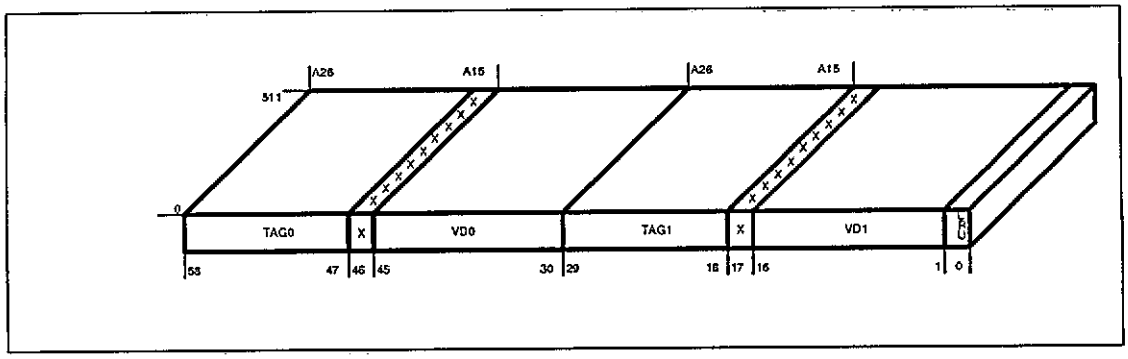
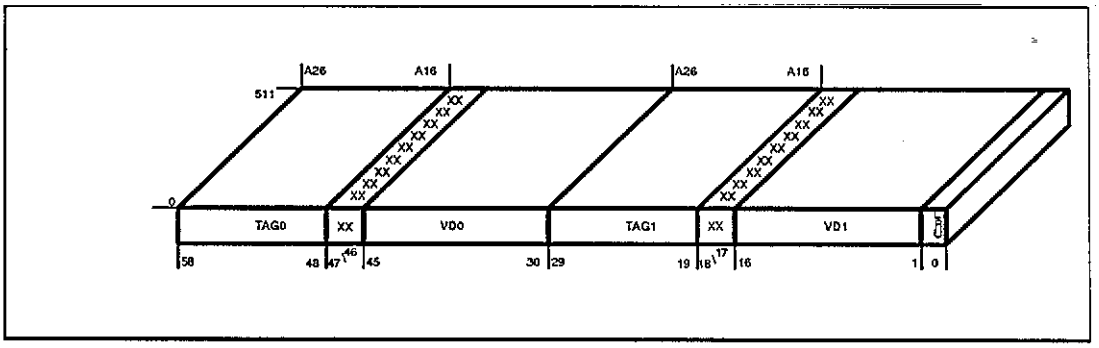


Figure 2-20. Directory Organization for 128Kb Cache Memory



32KB Cache Implementation

The cache data array is configured as two sets of 4096 double words (4K) each. It can be implemented using sixteen 4K by 4 SRAM. When the 82C311 is configured for 32KB of cache memory, it allocates a valid bit per double word and uses 256 entries of its cache directory.

Figures 2-21 and 2-22 illustrate the logical and physical cache organization for 32KB cache memory.

There are 59 bits per entry in the cache directory.

Figure 2-21. Logical Organization of 32Kb Cache Memory

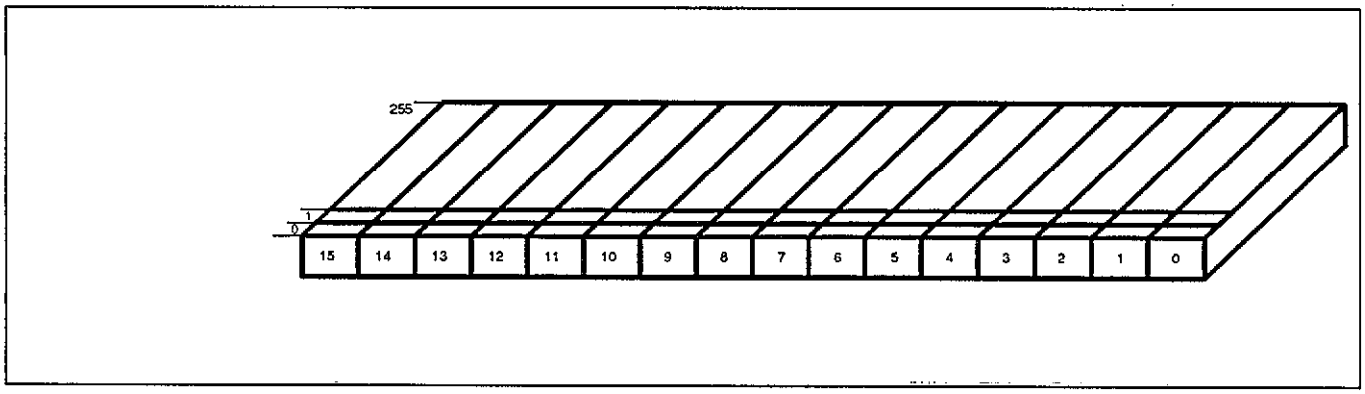


Figure 2-22. Physical Organization of 32Kb Cache Memory Using 4K x 4 SRAMs

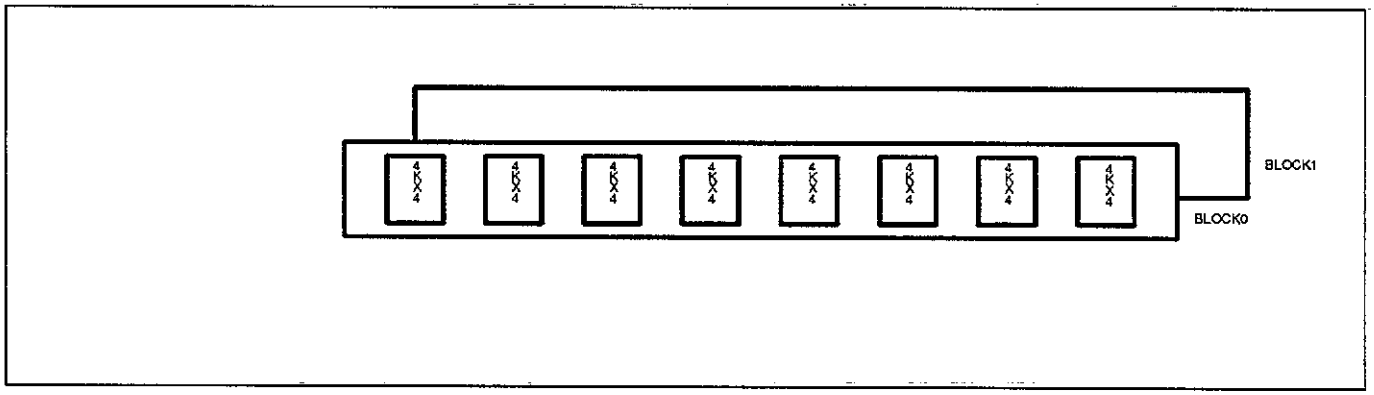


Figure 2-23. Logical Organization of 64Kb Cache Memory

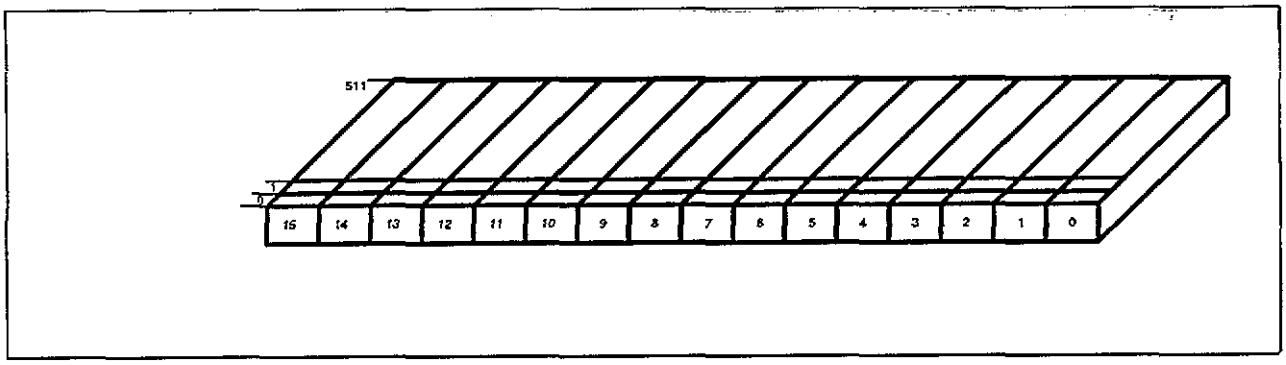
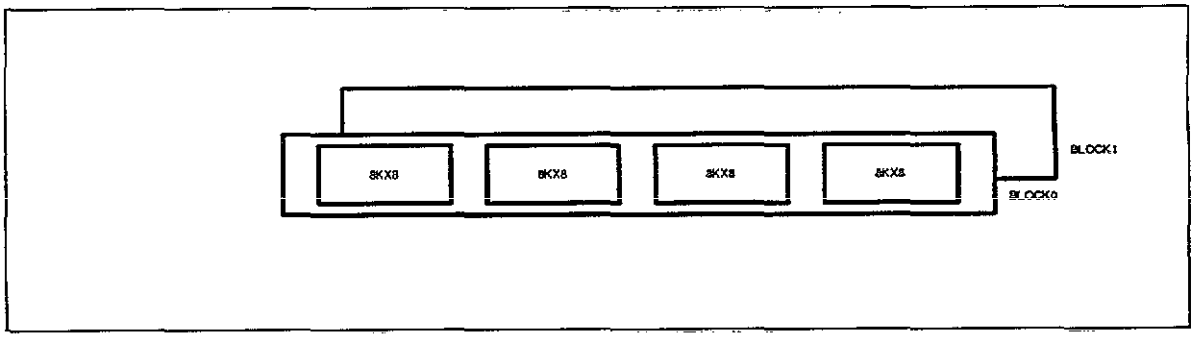


Figure 2-24. Physical Organization of 64Kb Cache Memory Using 8K x 8 SRAMs



64KB Cache Implementation

The cache data array for this size cache is configured as two sets of 8192 (8K) double words. A simple design could use eight 8K by 8 fast SRAMs, with 4 chips for each set. When the 82C311 is configured for 64KB of cache memory (REG24<5>), it allocates a valid bit per double word and uses all 512 entries of its cache directory.

Figures 2-23 and 2-24 illustrate the logical and physical cache organization for 64KB of cache memory.

128KB Cache Implementation

The data cache array for this size cache is configured as two sets of 16384 (16K) double words. Sixteen 8K by 8 SRAMs may be used to implement the cache memory. When the 82C311 is configured for 128KB of cache memory (REG24<4:5>), it allocates one valid bit per two double words and uses all 512 entries of its cache directory. The significant difference between implementing a 128KB cache versus 64KB is in the read miss cycle, all other cache cycles: read hit, write miss, and write hit, are the same.

During a read miss cycle, the 82C311 moves in data from the DRAM memory into the cache memory and sets a valid bit correspondingly. For 128KB cache memory, one valid bit is allocated to two double words; that is, for every read miss cycle, two double words must be moved into the cache memory prior to setting the corresponding valid bit. In order to move in two double words into the cache memory, two DRAM accesses must be completed prior to generating the READY- to the CPU to terminate the current cycle. During the first DRAM

Figure 2-25. *Logical Organization of 128Kb Cache Memory*

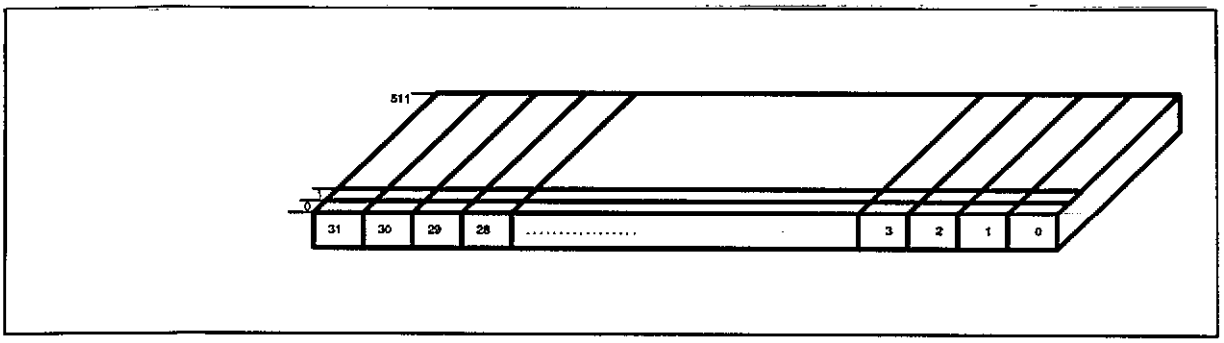
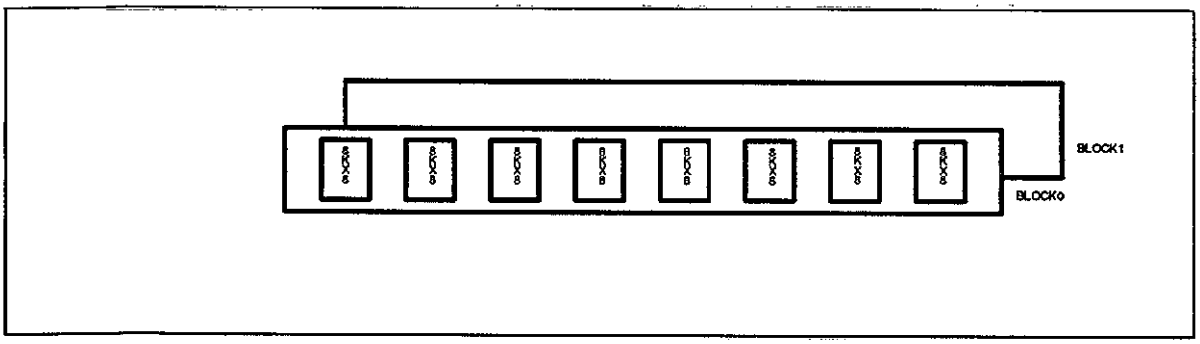


Figure 2-26. *Physical Organizaiton of 128Kb Cache Memory Using 8K x 8 SRAMs*



access, address line 2 (A2) is inverted inside the 82C311 and the inverted A2 is presented to the DRAM controller state machine. RAS and CAS are generated during the DRAM cycle. During the second DRAM access, the A2 is returned to its original state. RAS and CAS are again generated for second DRAM cycle, At end of the second DRAM access, the requested data is available on the bus and READY- is generated to terminate the read cycle. The 82C311 provides the signal BST128K to invert the A2 externally. The address line A2 should become exclusively OR'ed with the BST128K prior to getting connected to the SRAM address lines. Figures 2-25 and 2-26 illustrate the logical and physical cache organization for 128KB of cache memory.

The 82C311 has an option in 128K cache mode to access DRAM in page mode during a cache read miss cycle. In this mode only one RAS is generated for both DRAM cycles and two CAS signals are generated one for the first DRAM cycle and the second for the next DRAM cycle. The READY- is generated at the end of the second DRAM cycle. This increases the performance of the system. The page mode option can be turned on by programming bit 3 of register 2F to 1. The page mode option is not available on revision B of the 82C311.

Cache Operation

This section illustrates the following types of cache cycles:

- Read hit cycle
- Read miss cycle
- Write hit/miss cycle
- Direct SRAM access
- DMA cycle

Read Hit Operation

When a physical address is presented to the 82C311, it uses the line index field (A6 thru A14 in 64KB cache memory) to select a line from the cache directory. A line of a cache directory points to two tag entries, one from each set. The tags stored in these locations are simultaneously compared against the processor address lines. If a tag hit is detected and the corresponding valid bit for the selected subline is valid, then the corresponding data in the cache is forwarded to the processor, and the 32C311 drives the READY- signal low to terminate the read cycle.

The CRD- signal (CRD0- or CRD1-) is generated during the read hit cycle. The CRD- signal is connected to the output enable of SRAM. The Chipselect of SRAM is grounded. If the CRD- is programmed for Chip enable mode (bit 6 of Register 24 = 1), the CRD- is generated for write cycles also. The CRD- would then be used as Chip select for SRAMs. However it is always recommended to use CRD- as output enable (bit 6 of register 24 = 0) to SRAM.

However, if the current address matches the tag of both sets and both sets are valid, a cache error occurs. An error flag is set and no memory accesses are performed. This forces a READY to be generated by the 82C311.

Read Miss Operation

When a cache read miss occurs (the requested data is not in the cache memory), the main DRAM memory provides the data to the CPU. It also presents the same data to cache memory. A replacement algorithm which has the least amount of potential performance penalty is used. The least-recently-used (LRU) bit is an indication of which set should be replaced. A set which is not recently used, and therefore less likely to be used in the near future, is the set that should be replaced.

Write Hit Operation

When the CPU initiates a write cycle, a DRAM cycle also starts immediately independent of cache hit or miss result. If a cache hit happens in a write cycle, that is the corresponding data location in DRAM is also in cache memory, both DRAM and cache memory must be updated simultaneously. Therefore, SRAM and DRAM write cycle are initiated at the same time. SRAM cycle is much faster than DRAM cycle and additional wait states are required to complete the DRAM cycle. Instead of having the CPU wait for the completion of the DRAM cycle, a temporary register between CPU and the main memory temporarily holds the data for DRAM so the processor can continue. This is achived through the 74F646 buffers present between CPU data bus and memory data bus in the PEAK system.

If a cache miss occurs in a write cycle, no cache write operation occurs, only data in the main memory is updated.

If any of the cycles, immediately following the first write cycle requires another DRAM access while the main memory is still busy with the first write cycle, then additional wait states are asserted until the DRAM has completed the previous operation.

Direct DRAM Access

The CPU can bypass the cache to access the data in the DRAM directly. This is achieved by writing a 0 to bit 7 of index register 20. This feature is necessary during initial boot-up to check the integrity of the DRAM subsystem. In this mode, no SRAM cycle is done. Every memory cycle is a single RAS- followed by CAS access with user's option of 2 to 4 wait states.

DMA Operation

For local memory read cycles initiated by DMA or other masters on the bus, regardless of cache hit or miss, no SRAM is accessed. All memory read cycles are directed to main memory and the data buffer (82C315) receives data from the MD bus and drive the D and the SD busses.

For a local memory write cycle, the buffer's direction is from SD bus toward MD and D busses. Therefore, a cache miss causes the data to be written into the DRAM only and a cache hit writes the data into the DRAM and SRAM to maintain the coherency.

Functions Supported by BIOS Extension

The 82C311 provides diagnostic registers to allow the user to access the on-chip tag RAM directory through the 8-bit peripheral data bus. The entire tag directory RAM can be written or read from through I/O instructions for initialization or diagnostic purposes.

Cache Directory Testing

Entries within the cache directory may be read and written via the SRAM data port at Chipset Index Register 23h. The user may select which field within the cache directory is accessed by programming index registers 21h, 22h, and 25h. All entries within the cache directory are contained within the 82C311 chip, and are not dependent on the physical SRAM size.

The cache directory contains 512 cache lines in each cache set. For each cache line, there exists a 16-bit valid field, a 13-bit tag field, and a Least-Recently-Used (LRU) bit. The high bytes and low bytes of tag and valid fields must be accessed separately through Index Register 23h, and may be tested as separate entities. Tag fields only contain 5 bits within their high bytes, and the upper three bits always read back as 1's.

To access a field in the cache directory, use the following procedure:

1. The cache directory may be read while the cache is enabled, but not written. When writing to the cache directory, always disable the cache first.
2. Enable access to the cache directory by setting bit 7 in index register 21h. Also, set bit 6 when accessing a cache line number above 255. This bit, in conjunction with the 8 bits in index register 22h, form a 9-bit cache line number 00h to 1FFh (512 total cache lines). If accessing a tag field, specify the byte and set using bits 3, 4, and 5 within index register 21h. When accessing a valid or LRU field, these bits must be 0's.

3. Register 25h is used to select the byte and cache set when accessing a valid or LRU field. See the description of this register for the proper bit configuration. This register must be written with the value 00h when accessing a tag field.
4. Once index registers 21h and 25h have been programmed, write the lower 8 bits of the Cache Line Number to index register 22h.
5. After programming registers 21h, 22h, and 25h, the user may now access the data in the specified tag/valid/LRU field. This is done by reading/writing Chipset Index Register 23h. The user may continually to access the data in this field without reprogramming registers 21h, 22h, and 25h.

Line Invalidation

Any line in the cache directory can be selectively validated/invalidated through the configuration registers. The registers involved are REG21, REG22, REG23, and REG25.

Directory/Cache Purge

The directory purge can be done in the same way as line invalidation by IO cycles through REG21, REG22, REG23, and REG25. The I/O read cycles read the current values in the directory RAM, and the I/O write cycles load the desired values into the directory. The advantage of this mode of purging is that a program can non-destructively examine the contents of cache directory RAM.

To purge the cache data RAM, the cache has to be disabled by REG20<7> and the SRAM direct access bit REG20<4> should be turned ON. Then, the cache data RAM appears as part of the main memory in a 32K/64K/128KB block at an address specified by REG24<4:0> in the first 1MB.

Another way to flush the directory RAM is by using REG20<2>. If this bit is set to 0, then all following memory access act differently. The valid field of both sets of the particular line selected by the index field is reset to invalid (all 16 sublines/16 valid bits). To flush the entire TAG RAM, one pass through the entire line index field is required. The LRU field in this case is ignored.

Cache Directory Freeze

The 82C311 gives an option to freeze the cache directory. A cacahe read miss will not cause a tag RAM updtae and change of data in the cache RAM. Instead a normal DRAM cycle will be performed. A cache write hit will update the cache data RAM. This feature is useful for diagnostics purposes.

Cache Enable/Disable Sequence

After power-ON reset, the cache is disabled. Valid data can be loaded into DRAM without affecting the cache. All valid bits in cache directory should be disabled by executing I/O cycles. Then the cache can be enabled. As soon as the cache is enabled, the hit rate is set to zero since all valid bits are invalid and the cache data RAM is empty. As the program is executed, the cache data RAM is filled up gradually and the hit rate increases until an equilibrium point is reached.

To disable the cache, REG20<7> can be turned OFF again to become direct DRAM access mode only. Since the consistence between cache memory and

main memory is always maintained, the program can continue execution from main memory without intrusion.

SRAM Sizing

When Direct SRAM Access is enabled, (bit 4 of Register 20 = 1), no DRAM cycles are generated anywhere within the SRAM window. The size of the SRAM window is dependent on the size specified in index register 24h. If this size specified in register 24h is larger than the amount of SRAM physically present on the motherboard, the SRAM responds at multiple locations within the SRAM window. This feature may be used as an easy method of determining the physical SRAM size.

Examples:

1. While the cache controller is disabled, set the SRAM size to its maximum (128Kb). At the same time, establish the SRAM window space (assume 60000h to 7FFFFh). Index register 24h should be written with the value 16h.
2. Enable Direct SRAM Access (set bit 4 in index register 20h).
3. Initialize the entire 128Kb window to a known value (i.e., all zeros).
4. The SRAM used by cache set 0 begins at address 60000h, while the SRAM for set 1 begins at 70000h. Write a pattern to the first 16Kb of set 0 (60000h to 61fffh). Then scan the remainder of the set 0 address space for any appearance of the test pattern outside of the first 16Kb. If the pattern does not appear outside the first 16Kb, this indicates that set 0 contains 64Kb of cache. Repeat the procedure for set 1. Both sets must be of equal size. Add the total from set 0 and set 1 to obtain the total cache size.
5. If there is less than 64Kb of SRAM in set 0, then the 16Kb block repeats itself within the allocated 64Kb set 0 address space. If there are only 16Kb of SRAM in set 0 (total of 32Kb in the system), then the user will find that the pattern is repeated four times. If the pattern appears twice within the window, then there are 32Kb of SRAM in set 0, or a total of 64Kb in the system. Regardless of the total SRAM size, sets 0 and 1 must always have the same length.

   Example:

   Write a pattern to block 1, then read blocks 2 through 4 and check for the following conditions:

   - Block 1 = Block 2 = Block 3 = Block 4 ⟶ Set size is 16Kb
   - Block 1 = Block 3 and Block 2 = Block 4 ⟶ Set size of 32Kb
   - Pattern is in block 1 only ⟶ Set size is 64Kb

   Set 0 and Set 1 must be of equal length, and may be added together to determine the total cache size.

SRAM Testing

The Static RAM use by the cache controller may be tested by using the Direct SRAM Access feature of the PEAK/386 Chipset. This feature is enabled by setting bit 4 in Index Register 20h. Setting this bit maps SRAM over a portion of motherboard DRAM. Read and write cycles within this address space accesses the data within SRAM, and the DRAM is effectively disabled.

Before enabling Direct SRAM Access, make sure the cache is disabled (bit 7 in Register 20h must be 0). Also, it is important to make sure that the SRAM window is located at a non-intrusive location within the DRAM address space. This is accomplished via the SRAM Configuration Register (Index Register 24h). In Register 24h, set the SRAM size and the high 4 address bits of the SRAM Direct Access window.

Example:

If cache size is 64Kb, set bit 5 in register 24h. If the SRAM size is 128Kb, then set bit 4. If neither of these bits are set, the PEAK/386 Chipset defaults to a cache size of 32Kb.

In order to access 64Kb of SRAM in the address space 60000h to 6FFFFh, Index Register 24h should be written with the value 26h.

Once that address of the SRAM window has been established, Direct SRAM Access may be enabled by setting bit 4 in Index Register 20h. All memory accesses within the window affect the contests of SRAM, but not the contents of DRAM. The user may then perform pattern tests, address line tests, and other memory testing algorithms within the window for the purposes of testing SRAM. The user should also test for corruption of the underlying DRAM, as this should not occur and indicates a faulty part.

Cache Flush

Once the cache SRAM has been tested and its size determined, the cache must be flushed before it can be enabled. The PEAK Chipset provides a Cache Directory Flush feature in Chipset Register 20h. Cache Flushing is accomplished by clearing all valid bits in the cache directory. The following procedure is an efficient method of flushing and enabling the cache.

1. Set the cache size in Index Register 24h to 64Kb.
2. In Chipset Register 20h, enable the flush feature (bit 2 = 0), and enable the cache controller (bit 7 = 1). The Direct SRAM Access should also be disabled (bit 4 = 0).
3. Read any contiguous 32Kb block of memory. As each double-word of memory is read, the cache controller determines its cache line number within the tag directory and clear all valid bits, in both sets, correspondiing to that line.
4. Set the actual SRAM size in Chipset Register 24h.
5. Disable the Flush Feature by setting bit 2 in the Cache Control Register (Index 20h). The cache is now enabled and its operation will be transparent to any software executing on the system.

Non-Cacheable Regions

The PEAK/386 Chipset allows the software to declare four areas of memory as non-cacheable. Accesses to memory within this address space will go directly to DRAM, as though the cache controller were disabled. Any access outside these blocks is cached normally.

The Cache Controller within the PEAK/386 Chipset allows the user to declare any area of motherboard DRAM as being non-cacheable. This area must begin on any 4Kb boundary, and have a minimum length of 4Kb. Up to four non-cacheable regions may be declared. These non-cacheable blocks are

unrelated to the memory blocks declared in registers 10h through 18h. They may reside in any bank, and may even overlap. Declaring a non-cacheable block requires the user to program the following sets of registers:

Non-cacheable Block 0	Index Regs 30h, 31h, and 38h
Non-cacheable Block 1	Index Regs 32h, 33h, and 38h
Non-cacheable Block 2	Index Regs 34h, 35h, and 39h
Non-cacheable Block 3	Index Regs 36h, 37h, and 39h

The following procedure is recommended for establishing a non-cacheable block of memory:

1. Select the address at which the non-cacheable block is to start. Then clear bits 11 through 0 of this address. This gives the address of the 4Kb boundary on which the non-cacheable block must begin.
2. Write bits 15-12 of this address to the high 4 bits of index register 31h, 33h, 35h, or 37h; depending on which non-cacheable block is being programmed. The low 4 bits should be left as zeros for the time being. This leaves the non-cacheable block disabled until the user is finished programming the other registers.
3. Write bits 23-16 of the block's startiing address to index register 30h, 32h, 34h, or 36h.
4. Write bits 26-24 of the block address to register 38h or 39h. Be sure to preserve any bits relating to another non-cacheable block when performing this step.
5. Read back the register that was programmed in step 2. Now, set the low 4 bits to reflect the desired length of the non-cacheable region. See the description of these registers for the proper setting of these bits. Again, be sure to preserve the high 4 bits of this register. When the length has been set, no further cache cycles will be executed within the block.

The PEAK/386 Chipset only caches areas where there is motherboard DRAM present and enabled. Non-cacheable areas may reside anywhere within the 128 Mbyte address space supported by the PEAK Chipset. AT bus cycles are never cached, so the user need not use this feature for video RAM or memory which resides on AT adapter cards, unless these areas are shadowed in the DRAM.

Tristate feature

In this mode the outputs of the 82C311 can be tristated. This is useful in testing the system board. The 82C311 can be put into this mode by forcing MASTER-, HLDA, AEN16 low and TEST311 high.

82C311 Revisions

There are two 82C311 revisions identified as Revision B and Revision C. The 82C311 C supports both 25 and 33 Mhz, whereas the 82C311 B supports up to 25 Mhz. There are some feature differences between the 82C311 C and the 82C311 B. The differences between the 82C311B and the 82C311C are described at the end of the section.

Register Descriptions

Configuration Registers

There are 44 configuration and diagnostics registers in the 82C311. These are accessed through IO ports 22H and 23H normally found in the interrupt controller. An indexing scheme is used to reduce the number of I/O addresses required to access all registers needed to configure and control the CHIPSet. Each access (either read or write) to an internal register is done by first writing its index into port 22. This index then controls the multiplexers gating the appropriate register data accessible as port 23H. Every access to port 23H must be preceded by writing the index value to port 22H even if the same data port is being accessed again. The ( ) in the bit description of any bit indicates the default value after power up. **The registers mentioned here refer to the 82C311 Revsion C.**

CPU/Cache Controllers Internal Registers

This indicates the version of the 82C311 bits 7:6 indicates the version number.

Table 2-5. *Name: Version Register (READ ONLY)*

Index	Bits	Values and Functions
04H	7:6	Version number 10: Version number for 311C
	5:0	Reserved (000000)

Table 2-6. *Name: AT Bus Command Delay (READ/WRITE)*

Index	Bits	Values and Functions
05H	7:6	AT Bus 32 bit memory command delay. (00) : 0 BCLK delay. 01 : 1 BCLK delay. 10 : 2 BCLK delays. 11 : 3 BCLK delays.
	5:4	AT Bus 16 bit memory command delay. (00) : 0 BCLK delay. 01 : 1 BCLK delay. 10 : 2 BCLK delays. 11 : 3 BCLK delays.
	3:2	AT Bus 8 bit memory command delay. 00 : 0 BCLK delay. (01) : 1 BCLK delay. 10 : 2 BCLK delays. 11 : 3 BCLK delays.
	1:0	AT bus I/O cycle command delay. 00 : 0 BCLK delay. (01) : 1 BCLK delay. 10 : 2 BCLK delays. 11 : 3 BCLK delays.

Table 2-7. *Name: AT Bus Wait State Control (READ/WRITE)*

Index	Bits	Values and Functions
06H	7:6	32 bit AT Bus wait state. (00): 3 BUSCLK wait states. 01 : 2 BUSCLK wait states. 10 : 1 BUSCLK wait state. 11 : 0 BUSCLK wait states.
	5:4	16 bit AT Bus wait state (00): 3 BUSCLK wait states. 01 : 2 BUSCLK wait states. 10 : 1 BUSCLK wait state. 11 : 0 BUSCLK wait states.
	3:2	8 bit AT Bus wait state. (00): 5 BUSCLK wait states. 01 : 4 BUSCLK wait states. 10 : 3 BUSCLK wait state. 11 : 2 BUSCLK wait states.
	1	AT Bus address hold time. This feature is used if some AT cards require extra address hold time for relaible operation. This bit causes READY- to be generated 1 CPU wait state later then normal AT cycle. It keeps the data vaild longer for write cycles (0) : Disable extra address bus hold time. 1 : Enable extra address bus hold time of one CPU wait state
	0	Reserved

Table 2-8. *Name: Identification (READ/WRITE)*

Index	Bits	Values and Functions
08H	7:3	Reserved
	2	(0): AF32 will not be asserted for non local memory cycle. AT cycle is performed for address range not falling in the DRAM adddress area. 1 : If the address is more than 16MB and if no physical memory is configured then AF32 will be asserted. In this case no READY- is generated by the 82C311. There should be an external logic which identifies this address and generate READY to end the cycle. If READY- is not asserted by external logic then the 82C316 and the 82C311 generates READY- on time out if it is programmed(reg 26 bit 2 in the 82C316 and the 82C311) and also an NMI is generated by 82C316(see note).
	1	(0): Only 512K enabled. Ignore memory address configuration registers 0CH thru 0FH. When this bit is 0. 0: Normal configuration controlled by registers 0CH through 0FH.
	0	Reserved default = 1 (should be always 1)

Note: If AF32- can be pulled low by external logic for any address range, as AF32- is a bidirectional input, in which case READY_ should be generated by external logic.

Table 2-9. *Name: Low Boot Space RAM/ROM Configuration (READ/WRITE)*

Bits 7 to 4 disable writing to RAM located in the BIOS area in 64KB blocks. Bits 3 to 0 enable substitution of the BIOS ROM located below 1MB with RAM at the same location in 64KB blocks. This should be done after the BIOS code has been copied from the ROM and the RAM locations have been write protected using bits 7 to 4.

Index	Bits	Values and Functions
09H	7	64KB RAM type at 768K C0000-CFFFFH (EGA). (0) : 64KB of RAM at 768k is read/write . 1 : 64KB of RAM at 768k is read only.
	6	64KB RAM type at 832K D0000-DFFFFH . (0) : 64KB of RAM at 832k is read/write . 1 : 64KB of RAM at 832k is read only.
	5	64KB RAM type at 896K E0000-EFFFFH. (0) : 64KB of RAM at 896k is read/write . 1 : 64KB of RAM at 896k is read only.
	4	64KB RAM type at 960K F0000-FFFFFH (BIOS). (0) : 64KB of RAM at 960k is read/write . 1 : 64KB of RAM at 960k is read only.
	3	64KB ROM type at 768K C0000-CFFFFH (EGA). (0) : 64KB of ROM at 768k is disabled. 1 : 64KB of ROM at 768k is enabled. (0) : 64KB of ROM at 832k is enabled. 1 : 64KB of ROM at 832k is disabled.
	1	64KB ROM type at 896K E0000-EFFFFH. (0) : 64KB of ROM at 896k is enabled. 1 : 64KB of ROM at 896k is enabled.
	0	64KB ROM type at 960K F0000-FFFFFH (BIOS). (0) : 64KB of ROM at 960k is read/write . 1 : 64KB of RAM at 768k is read only.

Sequence of turning ON the shadow RAM for BIOS ROM:

1. Enable the ROM space in register 09H and make the RAM read/write-able.
2. Enable the corresponding local memory by using register 0FH.
3. Read the contents of the ROM and write it to the local memory. Since a memory write cycle will not generate ROMCS-, the data will be written into the DRAM.
4. Upon completion of the data transfer from the ROM to DRAM, program register 9 to disable the ROM and make the DRAM read only.

Sequence of turning ON the shadow RAM for EGA ROM:

1. Enable the ROM space in register 09H and make the RAM read/write-able.
2. Disable local memory located at 0C000H to 0CFFFH using register 0EH bits 4-7.
3. Read the contents of the EGA ROM into one of the CPU registers.
4. Enable the corresponding local memory located at 0C000H to 0CFFFH by using register 0EH bit 4-7.
5. Write the data from CPU register(where data was stored) into the memory. Since the memory located at 0C000H to 0CFFF is now enabled, the memory write cycle will be directed to the local memory system instead of the EGA memory.
6. Go back to step 2 until all the data are transfered from ROM into DRAM.
7. Upon completion of the data transfer from ROM to DRAM, program the register 9 to disable the ROM and make the DRAM read only.

Table 2-10. *Name: Memory Enable Map 080000-09FFFFH (READ/WRITE)*

Bit 0 enables the lowest and bit 7 enables the highest 16K block. For Example, bit 1 will control the 16KB block from 512K to 528K. This permits 16K blocks of memory to be disabled allowing ROMs, memory expansion schemes (EMS, EEMS or XMA) or memory mapped I/O devices to reside within the lower 1MB address space.

Index	Bits	Values and Functions
0CH	7:0	Enable bits for eight 16K blocks of memory. 0 : Address is on or controlled by the system board; 16K block enabled. (1): Address is on the I/O channel; 16k block disabled.

Table 2-11. *Name: Memory Enable Map 0A0000-0BFFFFH (READ/WRITE)*

Index	Bits	Values and Functions
0DH	7:0	Enable bits for eight 16K blocks of memory. 0 : Address is on or controlled by the system board; 16K block enabled. (1): Address is on the I/O channel; 16k block disabled.

Table 2-12. *Name: Memory Enable Map 0C0000-0DFFFFH (READ/WRITE)*

Index	Bits	Values and Functions
0EH	7:0	Enable bits for eight 16K blocks of memory. 0 : Address is on or controlled by the system board; 16K block enabled. (1): Address is on the I/O channel; 16k block disabled.

Table 2-13. *Name: Memory Enable Map 0E0000-0FFFFH(READ/WRITE)*

Index	Bits	Values and Functions
0FH	7:0	Enable bits for eight 16K blocks of memory. 0 : Address is on or controlled by the system board; 16K block enabled. (1): Address is on the I/O channel; 16k block disabled.

Table 2-14. *Name: Block 0 Type and Starting Address (READ/WRITE)*

This register defines the type of memory in block 0 and the starting address of the block. Since a block contains 2 banks the memory type defined applies to both the banks and starting address applies to the block.

Index	Bits	Values and Functions
10H	7:6	DRAM type in block 0. 00 : Block 0 disabled. (01): 256Kx1 or 256Kx4 DRAMs. 10 : 1Mx1 or 1Mx4 DRAMs. 11 : 4Mx1 or 4Mx4 DRAMs.
	5:0	Starting address 26:21 (000000).
		Disabled None
	256K	26:21 (2MB per pair of banks).
	1M	26:23 (8MB per pair of banks).
	4M	26:25 (32MB per pair of banks. A24:21 ignored in this register).
Default = 40H		

Table 2-15. *Name: Block 1 Type and Starting Address (READ/WRITE)*

This register defines the type of memory in block 1 and the starting address of the block.

Index	Bits	Values and Functions
12H	7:6	DRAM type in block 1.
		(00): Block 1 disabled.
		01 : 256Kx1 or 256Kx4 DRAMs.
		10 : 1Mx1 or 1Mx4 DRAMs.
		11 : 4Mx1 or 4Mx4 DRAMs.
	5:0	Starting address 26:21 (111111).
		Disabled None
	256K	26:21 (2MB per pair of banks).
	1M	26:23 (8MB per pair of banks).
	4M	26:25 (32MB per pair of banks. A24:21 ignored in this register).
Default = 3FH		

Table 2-16. *Name: Block 2 Type and Starting Address (READ/WRITE)*

This register defines the type of memory in block 2 and its starting address.

Index	Bits	Values and Functions
14H	7:6	DRAM type in block 2.
		(00): Block 2 disabled.
		01: 256Kx1 or 256Kx4 DRAMs.
		10 : 1Mx1 or 1Mx4 DRAMs.
		11: 4Mx1 or 4Mx4 DRAMs.
	5:0	Starting address 26:21 (000000).
	256K	26:21 (2MB per pair of banks).
	4M	26:25(32MB per pair of banks A24:21 ignored in this register)
Default = 3FH		

Table 2-17. *Name: Block 3 Type and Starting Address (READ/WRITE)*

This register defines the type of memory in block 3 and its starting address.

Index	Bits	Values and Functions
16H	7:6	DRAM type in block 3.
		(00): Block 3 disabled.
		01 : 256Kx1 or 256Kx4 DRAMs.
		10 : 1Mx1 or 1Mx4 DRAMs.
		11 : 4Mx1 or 4Mx4 DRAMs.
	5:0	Starting address 26:21 (111111).
		Disabled None
	256K	26:21 (2MB per pair of banks).
	1M	26:23 (8MB per pair of banks).
	4M	26:25 (32MB per pair of banks A24:A21 ignored in this register).
Default = 3FH		

Table 2-18. *Name: Block 0 RAM Timing and RAS- Pulse Width During Refresh of all Banks(READ/WRITE)*

This register defines wait states, RAS precharge, and RAS pulse for all banks.

Index	Bits	Values and Functions
11H	7:6	DRAM wait state.
		00 : 3 wait states.
		01 : 3 wait states.
		(10): 4 wait states.
		11 : 5 wait states
	5	Reserved. Default Value (0)
	4:3	RAS- precharge time.
		00 : 4CLK2 cycles.
		01 : 6CLK2 cycles.
		10 : 8CLK2 cycles.
		(11): 8CLK2 cycles.
	2:1	RAS- pulse width during refresh (for all banks).
		00 : 4 CLK2 cycles.
		01 : 5 CLK2 cycles.
		10 : 6 CLK2 cycles.
		(11): 7 CLK2 cycles.
	0	Reserved. Default Value (0)

Default = 9E

Table 2-19. *Name: Block 1 RAM Timing (READ/WRITE)*

This register defines wait states, RAS precharge for block 1.

Index	Bits	Values and Functions
13H	7:6	DRAM wait state.
		00 : 3 wait states.
		01 : 3 wait states.
		(10): 4 wait states.
		11 : 5 wait states
	5	Reserved. Default value (0)
	4:3	RAS- precharge time.
		00 : 4 CLK2 cycles.
		01 : 6 CLK2 cycles
		10 : 8 CLK2 cycles
		(11): 8 CLK2 cycles
	2:0	Reserved. Default value (0)

Default = 98H

Table 2-20. *Name: Block 2 RAM Timing (READ/WRITE)*

This register defines wait states, RAS precharge for block 2.

Index	Bits	Values and Functions
15H	7:6	DRAM wait state. 00 : 3 wait states. 01 : 3 wait states. (10): 4 wait states. 11 : 5 wait states.
	5	Reserved. Default value(0)
	4:3	RAS- precharge time. 00 : 4 CLK2 cycles. 01 : 6 CLK2 cycles 10 : 8 CLK2 cycles (11): 8 CLK2 cycles
	2:0	Reserved. Default Value(0)
Default = 98H		

Table 2-21. *Name: Type of Banks Filled in each Block (READ/WRITE)*

This register defines wait states, RAS precharge for block 3.

Index	Bits	Values and Functions
17H	7:6	DRAM wait state. 00 : 3 wait states. 01 : 3 wait states. (10): 4 wait states. 11 : 5 wait states
	5	Reserved. Default value(0)
	4:3	RAS- precharge time. 00 : 4CLK2 cycles. 01 : 6CLK2 cycles. 10 : 8CLK2 cycles. (11): 8CLK2 cycles.
	2:0	Reserved. Default value(111)
Default = 9FH		

Table 2-22. *Name: Type of Banks Filled in each Block (READ/WRITE)*

This register defines how many banks are present in a block. For example, if bit 3 = 0 only one bank i.e., bank 6 is present in block 3 and bank 7 is absent.

Index	Bits	Values and Functions
18H	7:4	Reserved. Default value(0)
	3	Block 3 Type. (0): One-Bank Filled. 1 : Two-Banks Filled.
	2	Block 2 Type. (0): One-Bank Filled. 1 : Two-Banks Filled.
	1	Block 1 Type. (0): One-Bank Filled. 1 : Two-Banks Filled.
	0	Block 0 Type. (0): One-Bank Filled. 1 : Two-Banks Filled.

Table 2-23. *Name: Cache Control (READ/WRITE)*

This register controls the cache operations, and is used for direct SRAM access, refresh type, and cache enable operations.

Index	Bits	Values and Functions
20H	7	Cache Enable bit. (0): Cache disabled. 1 : Cache enabled.
	6	Reserved. Default value(0)
	5	Enable Freeze cache directory bit. (0): Normal cache operation. 1 : Freeze cache directory. A cache read miss will not cause a tag RAM update and change of data in cache data RAM. Instead a normal DRAM read operation will be performed. A cache write hit will update the cache data RAM.
	4	Enable Direct SRAM access. (0): Normal cache operation. 1 : Access SRAM directly for 32 KB cache
	3	Refresh Type 0 : Hidden refresh. (1): AT-type refresh scheme is used in the system (with CPU being in HOLD state)
	2	Flush cache directory. 0 : Enable cache directory flush. When this bit is enabled (1): Normal cache operation.
	1	One Wait state for cache memory non-pipelined accesses. (0): One wait state SRAM access for non-pipelined cycles. 1 : Zero wait states for non-pipelined cycles.
	0	Reserved default value(1)
Default = 0D		

Table 2-24. *Name: Directory RAM Control I (READ/WRITE)*

This register, along with registers 22, 23, 25, is used for SRAM testing, tag RAM testing, and SRAM sizing.

Index	Bits	Values and Functions
21H	7	Enable Directory Access. 0: Disable cache directory access. (1) : Enable cache directory to be accessed through 8 bit peripheral data bus.
	6	T8 - Highest pointer bit to directory RAM. (0): The 1st 256 entries of directory RAM. 1 : The 2nd 256 entries of directory RAM.
	5	S2-Bit 2 of pointer to tag field.
	4	S1-Bit 1 of pointer to tag field.
	3	S0-Bit 0 of pointer to tag field. S2 S1 S0 Usage. (0)(0)(0): Disable access to tag field. 1 0 0 : Access set 0 high byte (A<22:26>). 1 0 1 : Access set 0 low byte (A<14:21>. 1 1 0 : Access set 1 high byte (A<22:26>). 1 1 1 : Access set 1 low byte (A<14:26>).
	2:0	Reserved Default value(000)
Default = 40		

Table 2-25. *Name: Directory RAM Control II(READ/WRITE)*

Index	Bits	Values and Functions
25H	7:5	Reserved Default value(000).
	4:3	Valid field of set 1 access. (00): Disable. 01 : Reserved. 10 : Enable access to Valid field of set 1 high byte. 11 : Enable access to Valid field of set 1 low byte
	2:1	Valid field of set 0 access. (00): Disable valid field access. 01 : Reserved. 10 : Enable access to Valid field of set 0 high byte. 11 : Enable access to Valid field of set 0 low byte
	0	LRU field access. (0): Disable LRU field access. 1 : Enable access to LRU field. To access the LRU field, use the XD0 bit, XD<1:7> are unspecified.
Default = 00		

Table 2-26. *Name: Low Bits of Directory Address Pointer(READ/WRITE)*

Index	Bits	Values and Functions
22H	7:0	Low order address bits for tag RAM directory. Together with REG21<6> they form a 9 bit address for 512 entries.

Default = FF

Table 2-27. *Name: Reference Location(READ/WRITE)*

Index	Bits	Values and Functions
23H	7:0	Used as a reference location to directory RAM access. In order to access the cache directory 1. Program REG21<7>=1 to enable directory access and setup the apropriate bits of register 7 for proper selection of field to be accessed. 2. Load register 22H with the intened line number to be accessed. 3. Following I/O read from register 23H will read the contents of the directory RAM. A I/O write to index register 23H will cause data to be written into the directory RAM.

Table 2-28. *Name: SRAM Configuration and Direct Access Address (READ/WRITE)*

This register is used to define the size of the cache and for direct SRAM accesses.

Index	Bits	Values and Functions
24H	7	Reserved Default value(0)
	6	*SRAM output enable control.* (0): CRD0# and CRD1# function as output enable. The CRD0(or 1) goes active for cache read hit cycles and these are connected to output enable of SRAMs. The SRAM chip enables should be coneected to ground. 1 : CRD0# and CRD1# function as chip select. The CRD0(or 1) is connected to chip enables of SRAM. The CRD signals go active for both read and write cycles.
	5	Amount of cache memory. (0): 32 KB data cache. 1 : 64 KB data cache.
	4	128KB cache option. (0): Disable 128KB cache option. 1 : Enable 128KB cache option.
	3:0	The highest 4 address bits for SRAM direct access. Default value(1111)

Table 2-29. *Name: Error Source/Address (MSBs)*

Index	Bits	Values and Functions
28H	7	Parity check enable(READ/WRITE). The PEN- signal will be active during local memory cycles. 0 Parity check is enabled (1) Parity check is disabled
	6	Cache error status bit (READ/WRITE). When this bit is read and if it is a 1, then a cache error has occured. To clear this bit, a zero should be written.
	2:0	Error address bits A26 to A24 (READ ONLY). The address bits A26 - A24 are stored in these bits on a parity error. LPAR- signal latches these addresses.

Table 2-30. *Name: Error Address (LSBs) (READ ONLY)*

Index	Bits	Values and Functions
29H	7:0	Error address bits A23 to A16. The address bits A23 - A16 are latched on parity error. LPAR- signal latches these address bits.

Table 2-31. *Name: Memory Enable Map 0-07FFFFH (READ /WRITE)*

Index	Bits	Values and Functions
2AH	7:1	Reserved.
	0	Enable/disable 0 to 512K on board memory (DRAM). This bit along with bit 1 of register 08 can disable all the memory between 0 to 1MB of on board memory. This bit should be set to 1. (0): Disable 0 to 512K on local memory. 1: enable 0 to 512K on local memory.
Default = 00		

Table 2-32. *Name: Miscellaneous Control (READ/WRITE)*

Index	Bits	Values and Functions
2BH	7	Memory Remapping. (0): Reserved
	6	Fast Gate A20 enable. This bit enables or disables the FAST GATEA20 of the 82C311. This bit when set provides performance improvement when the software(for example OS/2) switches between protected mode and real mode of 80386. The 82C311 identifies the I/O address 60 and 64 and generates GATEA20 internally. This feature can be overridden by register 2F bit 6. 0 : Disable Fast Gate A20. (1): Enable Fast Gate A20.
	5:3	Reserved.(000)
	2:1	AT Burst Refresh Control. (00): No Burst.(it is recommended to use NO BURST) 01 : Burst of 4. 10 : Burst of 8. 11 : Burst of 16.
	0	Coprocessor present. (0): Coprocessor does not exist. 1 : Coprocessor exists.
Note: Bit 0 of register 2BH reflects REG07 of 82C315 and the BIOS should set this bit accordingly. The status of this bit should remain unaltered after any WRITES to register 2BH.		

Table 2-33. *Name: Middle Boot Space RAM/ROM Configuration (READ /WRITE)*

This register is used to enable or disable the RAM in the area 15.768MB to 16MB. When the RAM is disabled, ROMCS- will be generated and a ROM can be present in that address range. When ROM is disbled, RAM is automaticaaly enabled. When RAM is enabled it can be write protected.

Index	Bits	Values and Functions
2CH	7	Type of 64KB RAM at 15.768MB.
		(0): 64KB of RAM at 15.768MB is R/W.
		1 : 64KB of RAM at 15.768MB is read only.
	6	Type of 64KB RAM at 15.832MB.
		(0): 64KB of RAM at 15.832MB is R/W.
		1 : 64KB of RAM at 15.832MB is read only.
	5	Type of 64KB RAM at 15.896MB.
		(0): 64KB of RAM at 15.896MB.is R/W.
		1 : 64KB of RAM at 15.896MB is read only.
	4	Type of 64KB RAM at 15.960MB.
		(0): 64KB of RAM at 15.960MB is R/W.
		1 : 64KB of RAM at 15.960MB is read only.
	3	Enable 64KB ROM at 15.768MB.
		(0): 64KB of ROM at 15.768MB is disabled.
		1 : 64KB of ROM at 15.768MB is enabled.
	2	Enable 64KB ROM at 15.832MB.
		(0): 64KB of ROM at 15.832MB is disabled.
		1 : 64KB of ROM at 15.832MB is enabled.
	1	Enable 64KB ROM at 15.896MB.
		(0): 64KB of ROM at 15.896MB is disabled.
		1 : 64KB of ROM at 15.896MB is enabled.
	0	Enable 64KB ROM at 15.960MB.
		0 : 64KB of ROM at 15.960MB is disabled.
		(1): 64KB of ROM at 15.960MB is enabled.

Table 2-34. *Name: Page Mode Posted Write Control*

This register is used to enable the page mode DRAM operation during a read miss cycle when 128K of cache is present. This is also used to enable FAST GATEA20 and control wait state for posted write cycle.

Index	Bits	Values and Functions
2FH	7:6	Reserved. should be 0
	5	(1) Enable FAST GATEA20. 0 Disable FASTGATEA20. This bit overrides the bit 6 of index register 2BH
	4	(0) Adds no extra wait states between back to back DRAM cycles 1 Adds one extra wait state between CAS- inactive and the following RAS- pulse. This bit is recommended to be set for the 82C311C
	3	(0) Page mode operation disabled for a read miss cycle for 128K cache operation. 1 Page mode enabled for a read miss cycle for 128K cache opeartion. In this mode RAS- remains active for two 32 bit memory read cycles during cache miss cycle. This feature allows use of page mode DRAMs and saves one wait state during cache read miss cycle.
	2	(0) Enables zero wait state posted write cycles 1 Adds one wait state for posted write cycles
	1	(0) Enables posted write cycles for DRAM. 1 Diasbales posted write cycles for DRAM.
	0	(0) Reserved

Default = 00

Table 2-35. *Name: Block 0 Non-Cacheable address A23 to A16 (READ/WRITE)*

Index	Bits	Values and Functions
30H	7:0	Block 0 Non-Cacheable address A23 to A16.

Table 2-36. *Name: Block 0 Non-Cacheable address A15 to A12 and Size (READ/WRITE)*

Index	Bits	Values and Functions
31H	7:4	Block 0 Non-Cacheable address A15 to A12.
	3:0	Non-Cacheable Size. (0000): Disabled. 0001 : 4 KB. 0010 : 8 KB. 0011 : 16 KB. 0100 : 32 KB. 0101 : 64 KB. 0110 : 128 KB. 0111 : 256 KB. 1000 : 512 KB. 1001 : 1 MB. 1010 : 2 MB. 1011 : 4 MB.

Table 2-37. *Name: Block 1 Non-Cacheable address A23 to A16 (READ/WRITE)*

Index	Bits	Values and Functions
32H	7:0	Block 1 Non-Cacheable address A23 to A16.

Table 2-38. *Name: Block 1 Non-Cacheable address A15 to A12 and Size (READ/WRITE)*

Index	Bits	Values and Functions
33H	7:4	Block 1 Non-Cacheable address A15 to A12.
	3:0	Non-Cacheable Size. (0000):Disabled. 0001 : 4 KB. 0010 : 8 KB. 0011 : 16 KB. 0100 : 32 KB. 0101 : 64 KB. 0110 : 128 KB. 0111 : 256 KB. 1000 : 512 KB. 1001 : 1 MB. 1010 : 2 MB. 1011 : 4 MB.

Table 2-39. *Name: Block 2 Non-Cacheable address A23 to A16 (READ/WRITE)*

Index	Bits	Values and Functions
34H	7:0	Block 2 Non-Cacheable address A23 to A16.

Table 2-40. *Name: Block 2 Non-Cacheable address A15 to A12 and Size (READ/WRITE)*

Index	Bits	Values and Functions
35H	7:4	Block 2 Non-Cacheable address A15 to A12.
	3:0	Non-Cacheable Size. (0000):Disabled. 0001 : 4 KB. 0010 : 8 KB. 0011 : 16 KB. 0100 : 32 KB. 0101 : 64 KB. 0110 : 128 KB. 0111 : 256 KB. 1000 : 512 KB. 1001 : 1 MB. 1010 : 2 MB. 1011 : 4 MB.

Table 2-41. *Name: Block 3 Non-Cacheable address A23 to A16 (READ/WRITE)*

Index	Bits	Values and Functions
36H	7:0	Block 3 Non-Cacheable address A23 to A16.

Table 2-42. *Name: Block 3 Non-Cacheable address A15 to A12 and Size (READ/WRITE)*

Index	Bits	Values and Functions
37H	7:4	Block 3 Non-Cacheable address A15 to A12.
	3:0	Non-Cacheable Size. (0000):Disabled. 0001 : 4 KB. 0010 : 8 KB. 0011 : 16 KB. 0100 : 32 KB. 0101 : 64 KB. 0110 : 128 KB. 0111 : 256 KB. 1000 : 512 KB. 1001 : 1 MB. 1010 : 2 MB. 1011 : 4 MB.

Table 2-43. *Name: Non-cacheable address A26 to A24 (READ/WRITE)*

Index	Bits	Values and Functions
38H	7:6	Reserved.
	5:3	Block 0 Non-Cacheable address A26 to A24.
	2:0	Block 1 Non-Cacheable address A26 to A24.

Table 2-44. *Name: Non-Cacheable address A26 to A24 (READ/WRITE)*

Index	Bits	Values and Functions
39H	7:6	Reserved.
	5:3	Block 2 Non-Cacheable address A26 to A24.
	2:0	Block 3 Non-Cacheable address A26 to A24.

Table 2-45. *Name: Fast Reset Control Register*

Index	Bits	Values and Functions
60H	7:6	Reserved.
	5	Alternate CPU reset. A low to high transition activates a CPU reset.
	4:0	Reserved.

Table 2-46. *Name: Time-out Register (WRITE ONLY)*

Index	Bits	Values and Functions
26H	7:3	Reserved.
	2	Enable READY time out. The READY- is generated by the 82C311 when an external device which pulls AF32- low fails to generate READY- to the CPU. This feature can be enabled or disabled. This is a write only bit. (0): READY time out disabled 1 : READY time out enabled
	1:0	Reserved.

Pin Descriptions

Pin #	Symbol	Type	Signal Description
78	CLK2	I	CLOCK 2 is a CMOS input for the memory controller and the 80386. It is derived from CLK2IN input of the 82C315. This clock can also be programmed in the 82C315 to be the same as BCLK. This pin is connected to CLK2 of 82C315.
79	BCLK	I	BCLK is a CMOS input clock signal from the 82C315 and is used for the AT Bus State Machine. It can be 1/2, 1/3, 1/4, or 1/5 of CLK2 in frequency or ATCLK1.
39	BUSCLK	O	BUS CLOCK is a clock output to the AT expansion BUS. This signal has a 4mA drive capability. It is one half of the AT bus state machine clock frequency BCLK.
84	SCLK-	I	SYSTEM CLOCK is from the 82C315 and is CLK2 divided by two and is an output generated as a reference to verify the phase relationship of the internal clock of the 80386. This is a CMOS input signal.
3	RESET1-	I	RESET 1 is an active low (schmitt-triggered) input which is generated by POWER GOOD for a cold reset. When low, it activates RESET3 and RESET. RESET1- is latched internally.
4	RESET2-	I	RESET 2 is an active low input which is generated from 8042 Keyboard Controller for a warm reset. It forces a CPU reset by activating the RESET3 signal.
122	RESET3	O	RESET 3 is an active high output signal which is used to reset the 80386 and the 80387 whenever RESET1- or RESET2- is active. It is also activated during CPU shutdown cycles. RESET3 will remain active for at least 78 CLK2 cycles. This signal has a 8mA drive capability.
123	RESET4	O	RESET 4 is an active high output which is used to reset the AT Bus, 8042, and 82C316. This signal has an 8mA drive capacility. RESET4 is synchronized with SCLK-.
9	READY-	I/O	READY is an active low bidirectional signal. It is an output after requested local memory or I/O data transfer is completed. It is an input when 82C316 generates ready for 387 cycles or time out ready for cycle termination or when Weitek coprocessor generates ready. As an output, this signal has an 8mA drive capability.
22	ADS-	I	ADDRESS STROBE is an active low input from the 80386 ADS- pin. ADS- indicates valid bus cycle definitions (ie. W/R-, D/C-, M/IO- and BE<0:3>-) and addresses (A2 to A31). A 10K pull-up resistor is recommended on this pin.

Pin #	Symbol	Type	Signal Description
21	WR-	I/O	WRITE/READ status is a bidirectional signal from the 80386 W/R- pin. As an input, during local memory or I/O cycles. WR- indicates a write bus cycle when high and a read bus cycle when low. As an output, this signal has a 1mA drive capability. During the DMA cycle, WR- is the same as MEMR- and has 4mA driving capability. A 10K pull-up resistor is recommended on this pin.
20	DC-	I	DATA/CONTROL is an input from the 80386 D/C- pin. DC- indicates a data cycle when high and a command cycle when low. A 10K pullup resistor is recommended on this pin.
19	M/IO	I	MEMORY/IO is an input from the 80386 M/IO-. Pin M/O- indicates a memory cycle when high and an I/O cycle when low. A 10K pullup resistor is recommended on this pin.
106	HOLD	O	HOLD request is an active high output to the 80386 HOLD pin. HOLD is used to request to the CPU to relinquish the use of the bus to another requesting master (HRQ1, HRO2, or REFREQ). This signal has a 4mA drive capability.
35	HLDA	I	HOLD ACKNOWLEDGE is an active high input from the 80386 HLDA pin. When high, HLDA indicates that the CPU has relinquished the system bus in response to an active HRQ1, HRQ2, or REFREQ signal to the 82C311.
8-5	BE<0:3>-	I/O	BYTE ENABLEs BE0- through BE3- are active low bidirectional signals. Indicating the status of the system 4 data bytes. BE3- controls the most significant byte while BE0- controls the least significant byte. These signals are inputs from the 80386 BE<0:3> pins during a CPU cycle. As outputs, BE<0:3>- are generated during DMA cycles based on the status signals XA0, XA1, and XBHE-. As an output, these signals have a 4mA drive capability.
25	0WS-	I	ZERO WAIT STATE is a schmitt-triggered active low input from the AT Bus, causing termination of the AT bus cycle. 16 or 32 bit memory or I/O cards residing on the AT expansion bus use this line to speed up accesses. This signal requires a 330 ohm pull-up resistor.
38	IO2XCS-	I	IO2X CHIP SELECT is a active low input signal from the 82C316 and is a I/O decode of addresses 022H OR 023H. It is used to access the internal indexed configuration registers of the PEAK 386/AT CHIPSet.
107	HLDA1	O	HOLD ACKNOWLEDGE 1 is an active high output signal to the 82C315 and 82C316 and indicates that the CPU has relinquished control of the system busses in response to HRQ1 (DMA or master cycle). This signal has a 2mA drive capability.

Pin #	Symbol	Type	Signal Description
34	REFREQ	I	REFRESH REQUEST is an active high input signal generated from the OUT1 pin of the 82C316 (OUT1 is generated by a 8254 compatible timer controller in the 82C316 in a PC/AT implementation). When active, REFREQ initiates a DRAM refresh sequence.
108	HLDA2	O	HOLD ACKNOWLEDGE 2 is an active high output signal and indicates that the CPU has relinquished control of the system busses in response to HRQ2. This signal has a 1mA drive capability.
83	HRQ1	I	HOLD REQUEST 1 is an active high input signal and it is used to indicate a DMA/Master is requesting the use of the bus. For an AT compatible architecture HRQ1 should be connected to the hold request signals HRQ from 82C316.
82	HRQ2	I	HOLD REQUEST 2 is an active high input signal and indicates a DMA/Master is requesting the system busses. This pin should be tied to ground if it is not used.
36	AEN8-	I	ADDRESS ENABLE for 8 bit DMA transfers is an active low input signal from one of the two DMA controllers. When active, AEN8- enables the address latches for 8 bit DMA transfers. It is inactive when the external bus master controls the system bus.
37	AEN16-	I	ADDRESS ENABLE for 16 bit DMA transfers is an active low input signal from one of the two DMA controllers. When active, AEN8- enables the address latches for 8 bit DMA transfers. It is inactive when external bus master controls the system bus.
42	MCS16-	I	MEMORY CYCLE SELECT 16 is an active low input signal from the AT bus. When active, MCS16- causes a 16 bit memory access on the I/O channel. When both MCS16- and MCS32- are not active then the current memory cycle is an 8 bit cycle. A 330 ohm pull-up resistor is recommended on this pin.
44	MCS32-	I	MEMORY CYCLE SELECT 32 is an active low input signal from the AT bus. When active, MCS32- causes a 32 bit memory access on the I/O channel. When both MCS16- and MCS32- are not active, then the current memory cycle is an 8 bit cycle. A 330 ohm pull-up resistor is recommended on this pin.
43	IOCS16-	I	I/O CYCLE SELECT 16 is an active low input signal from the AT bus. When active IOCS16- causes a 16 bit I/O access on the I/O Channel. IOCS16- and IOCS32- are not active then the current I/O cycle is a 8 bit cycle. A 330 ohm pull-up resistor is recommended on this pin.

Pin #	Symbol	Type	Signal Description
45	IOCS32-	I	I/O CYCLE SELECT 32 is an active low input signal from the AT bus. When active IOCS32- causes a 32 bit I/O access on the I/O Channel. IOCS16- and IOCS32- are both not active then the current I/O cycle is a 8 bit cycle. A 330 ohm pullup resistor is recommended on this pin.
152	REF-	I/O	REFRESH is a active low schmitt triggered bidirectional signal. As an input, REFRESH can be used to force a refresh cycle from an I/O master device. As an output, REFRESH initiates a refresh cycle for the DRAMs. A 620 ohm pull-up resistor is required on this pin. As an output, this signal has an 12mA drive capability.
94	BST128K	O	BST128K is used to control the A2 inversion in 128KB data cache mode. BST128K is EXclusive ORed with A2 to produce the lowest address bit for the cache memory. During a read miss cycle in 128K mode option, BST128K is at a high level during the first half of the cycle and will toggle low for the second half. BST128K is at a low level all other times. This signal has a 2mA drive capability.
153	LDBEN-	O	LOCAL DATA BUS ENABLE is an active low output to four octal bus transceiver and register components (646). When LDBEN- and LDBDIR are low then the current values on the DRAM data lines are transceived on to the CPU data lines. When LDBEN- is low, LDBDIR is high and BWBUSY is low; then the current blaues on the CPU data lines are transceived on to the DRAM data lines. When LDBEN- is low, LDBDIR is high and BWBUSY is high; then the values on the CPU data lines during the raised edge of LDBCAB are transceived on to the DRAM data lines. This signal has a 4mA drive capability.
154	LDBDIR	O	LOCAL DATA BUS DIRECTION controls the direction of the four octal bus transceiver and register components needed between the Local Data and the Memory Data Busses. When LDBEN- and LDBDIR are low then the current values on the DRAM data lines are transceived on to the CPU data lines. When LDBEN- is low, LDBDIR is high and BWBUSY is low then the current values on the CPU data lines are transceived on to the DRAM data lines. During buffered write cycles, when LDBEN- is low, LDBDIR is high and BWBUSY is high then the values on the CPU data lines during the rising edge of LDBCAB are transceived on to the DRAM data lines. This signal has a 4mA drive capability.
155	BWBUSY	O	BUFFER WRITE BUSY is an active high output signal to indicate that the main memory (local) is busy in a buffer write cycle. When LDBEN- is low, LDBDIR is high, and BWBUSY is high, then the values on the CPU data lines during the raised edge of LDBCAB are transceived on to the DRAM data lines. BWBUSY is also used in 82C315 to tri-state MD bus to avoid bus contention. This signal has a 4mA drive capability.

Pin #	Symbol	Type	Signal Description
156	LDBCAB	O	LOCAL DATA BUS CLOCK A to B is an active high output to four octal bus transceiver and register components (646) and one quad register. During the rising edge of LDBCAB the local data bit D0 to D31 are latched into the four octal bus transceivers and registers components. The latch byte enable LBE0- to LBE3- are also latch by the rising edge of LDBCAB. During the buffered write cycles, when LDBEN- is low, LDBDIR is high and BWBUSY is high, then the values latched by LDBCAB are transceived on to the DRAM data lines MD0 to MD31. This signal has a 4mA drive capability.
32, 33, 46-49 52-53,	MA<0:7>	I/O	MULTIPLEXED DATA/ADDRESS lines XDA0 to XDA7 are bidirectional signals used to interface to the System DRAM and the internal registers of the 82C311. During DRAM cycles, XDA<0:7> generate the lower address bits, MA<0:7> for the DRAM array. To access the internal registers for index and configuration values, XDA0 to XDA7 are required to be connected to the XD bus using a 74F245. IOW- controls the direction of the 74F245 and XDEN- enables the 74F245. These lines should be buffered and line terminated with 33 ohm resistors before driving the DRAM array. As outputs, these signals have an 8mA drive capability.
54, 55, 58	MA<8:10>	O	MULTIPLEXED ADDRESS lines MA8 to MA10 are output signals for the system DRAM memory. MA8, MA9 and MA10 should be connected to system DRAM address lines A8, A9 and A10 respectively. This output has a 8mA drive capability. These lines should be buffered and line terminated with 33 ohm resistors before driving the DRAM array.
24	IOCHRDY	I	IO CHANNEL READY is an schmitt-triggered active high input from the AT Bus. When low, IOCHRDY indicates a "not ready" condition and forces the insertion of wait states in I/O or memory accesses. When high, it allows the completion of the current I/O or memory access.
92	SDIR	O	SYSTEM BUS DIRECTION is an output signal to the 82C315 and controls the data bus direction between IO channel and memory data bus in the 82C315. When low, SDIR enables data transfer from the I/O channel to the MD bus. When high, it enables data transfer from the local bus to the I/O channel bus. This signal has a 2mA drive capability.
109	ACEN-	O	ACTION CODE ENABLE is an active low output to the 82C315 and validates ACTION CODES AC<0:3>. This signal has a 2mA drive capability.
110-113	AC<0:3>	O	ACTION CODEs are a four bit encoded command to the 82C315 and is used for data bus sizing and byte assembly operations. AC0 to AC3 are qualified by the ACEN signal. These signals have a 2mA drive capability.

Pin #	Symbol	Type	Signal Description
10	AF32-	I/O	AF32- is an active low bidirectional signal. As an output, AF32- indicates the current address is for local 32 bit memory on the system board. AF32- is used as an input when a Weitek 3167 coprocessor is present. A high indicates an AT bus cycle. AF32- requires a 10K ohm pull-up resistor. As an output, this signal has a 4mA drive capability.
96	MALE-	O	MEMORY ADDRESS LATCH ENABLE is an active low output signal to the 82C315 and 82C316 which indicates the start of a new CPU cycle. MALE- allows 82C316 to latch local addresses onto the SA bus during CPU AT cycles. MALE- is also used in 82C315 for parity generation and 387 interface circuits. This signal has a 4mA drive capability.
95	INTA-	O	INTERRUPT ACKNOWLEDGE is an active low output to the interrupt controller in the 82C316. This signal has a 2mA drive capability.
97	ATEN-	O	AT ENABLE is an active low output signal to the 82C315 and 82C316. When active, ATEN- indicates that the current CPU access is an AT bus cycle. This signal has a 4mA drive capability.
158-159	XA<00:01>	I/O	EXPANSION ADDRESS bits 0 and 1 are bidirectional signals and they are connected directly to the 82C316. XA00 is an output when the CPU is the bus master and input when 8-bit DMA is a bus master. XA01 is output when the CPU is the bus master and input when 8-bit or 16-bit DMA is a bus master. As an output, these signals have a 4mA drive capability.
151-134	A<2:19>	I	LOCAL ADDRESS bits A2 to A19 are input signals from the CPU and the 82C316.
116	A20	I/O	LOCAL ADDRESS bit 20 is a bidirectional signal. A20 is an output signal during CPU cycles and an input during DMA cycles. As an output, this signal has a 4mA drive capability.
129-124 118-117	A<24:31>	I	LOCAL ADDRESS bit 24 to 31 are input signals from the CPU.
98	XDEN-	O	XD BUS BUFFER ENABLE is an active low output and it is used to enable the buffer between the XD and MA<0:7> busses. XDEN- is asserted during I/O access cycles to locations 022H and 023H. This signal has a 2mA drive capability.
132-130	A<21:23>	I	Local address bits A21 to A23 are input signals from the CPU to the 82C316 (Peripheral).
101	ROMCS-	O	ROM CHIP SELECT is an active low signal. When active, ROMCS- enables the chip select inputs to the BIOS EPROMS and it also indicates to the 82C315 a BIOS read cycle and enables data to transceive from the XD bus onto the D bus. When ROMCS- is activated, it is recognized as a 16 bit memory operation and there is no need to pull MEMCS16- low during the ROM cycle. This signal has a 4mA drive capability.

Pin #	Symbol	Type	Signal Description
102	DRD-	O	DRAM READ DIRECTION is a active low output signal which is used by 82C315 to control the direction of data transfer from the SD bus to the MD bus. When low, DRD- enables data transfer from the MD bus to the SD bus. When high, the data transfer is from SD bus to the MD bus. This signal has a 2mA drive capability.
103	DWE-	O	DRAM WRITE ENABLE is active low output signal to the system DRAMs. This signal needs to be buffered and line terminated with a 33 ohm resistor. This signal has a 8mA drive capability.
59-62	RAS<0:3>-	O	ROW ADDRESS STROBES RAS0- to RAS3- are active low outputs to the system DRAMs. There is one RAS signal for each bank of memory on the motherboard. RAS0- is the strobe for bank 00. RAS1- is the strobe for bank 01. RAS2- is the strobe for bank 02. And RAS3- is the strobe for bank 03. These signals should be buffered and line terminated with 33 Ohm series resistors. These signals have a 6mA drive capability.
63-65, 68	RAS<4:7>-	O	ROW ADDRESS STROBES RAS4- to RAS7- are active low outputs to the system DRAMs. There is one RAS signal for each bank of memory on the motherboard. RAS4- is the strobe for bank 04. RAS5- is the strobe for bank 05. RAS6- is the strobe for bank 06. And RAS7- is the strobe for bank 07. These signals should be buffered and line terminated with 33 Ohms series resistors. These signal have a 6mA drive capability.
69	CAS-	O	COLUMN ADDRESS STROBE is an active low output signals which latches the DRAM data in the 82C315 data buffer. This signal has a 6mA drive capability.
70-73	CAS<0:3>-	O	COLUMN ADDRESS STROBES CAS0- to CAS3-are an active low output signal to the DRAMs for selecting the DRAMs of bank 0, 1, 2, 3. CAS0- to CAS3- must be externally ORed with the byte enables allowing for the selection of each byte of DRAM chips and the lines should be terminated with 33 ohm resistor. These signals have a 6mA drive capability.
74-77	CAS<4:7>-	O	COLUMN ADDRESS STROBES CAS4- to CAS7- are active low output signals to the DRAMs for selecting the DRAMs of bank 4, 5, 6, 7. CAS4- to CAS7- must be externally ORed with the byte enables allowing for the selection of each byte of DRAM chips and the lines should be terminated with 33 ohm resistors. These signals have a 6mA drive capability.
2	TEST311-	I	TEST PIN for the 82C311 is an active low input signal and should be pulled high with a 10K ohm resistor for proper operations of the 82C311.

Pin #	Symbol	Type	Signal Description
13	PEN-	O	PARITY ENABLE is an active low output signal which controls the overall parity enable circuity in the 82C315. This bit is controlled by REG28<7>. This signal has a 1mA drive capability.
119	MENB-	I	MEMORY ENABLE is an active low input signal. When active, MENB- validates the addresses on the local bus. This input can be used to disable the 82C311 from responding to predefined address locations via an external decode. This signal requires a 300 ohm pull-down resistor.
104	NA-	O	NEXT ADDRESS is an active low output signal to the 80386. NA- indicates to the CPU that the next cycle is to be a pipelined cycle. This signal has a 1mA drive capability. **This signal should not be connected to NA of 386 as the system should not be run in pipeline mode. This pin should not be used.**
88,89	CWE<0:1>-	O	CACHE WRITE ENABLE 0 and 1 are active low output signals to the SRAM's write enables in cache bank 0 and 1 respectively. These signals are active during read miss or write hit cycles. CWE<0:1>- should be ORed with byte enables LBE<0:3>- These signals have 8mA drive capability.
90, 91	CRD<0:1>-	O	CACHE READ 0 and 1 are active low output signals to the SRAM's output enables or the chip select pin of cache bank 0 and 1. During the read hit cycle, CRD0 or CRD1- are enabled to drive the requested data on to the D bus. Only one bank is selected at any given time. when the 82C311 is programmed in the Chip Select mode, CRD0- will become active during all cache memory accesses (read or write). In the output enable mode, CRD0- is active only during the read cycles. This signal has a 8mA drive capability.
93	CALE	O	CACHE ADDRESS LATCH ENABLE is an active high output signal for two octal latches. CALE is used to latch the SRAM addresses A2 to A15. When CALE is high, the latch is transparant and allows the 80386 addresses to flow through to the SRAM. On the high to low transition of CALE, the addresses are latched. This signal has a 6mA drive capability.
105	FBE-	O	FBE- is force byte enable signal from the 82C311. This signal is input to 82C315 and it is ORred with BE:3- inside 82C315 and used as LBE<3:0>. The FBE- signal goes active during a read miss cycle to update the all four bytes in the cache RAM.
23	MASTER-	I	MASTER is an active low input signal from an active device on the I/O channel (AT expansion bus). After MASTER- is forced low by an I/O device, the I/O CPU must wait for one system clock period before driving its address and data lines. MASTER- must not be held low for more than 15 microseconds, or else the data in the system memory may be lost due to lack of a refresh cycle. MASTER- must be pulled high with 10K ohm resistor.

Pin #	Symbol	Type	Signal Description
11	RSTDRV	O	RESET DRIVE is an active high output to the AT Bus. RSTDRV is used reset the I/O devices on the AT expansion bus. This signal has a 12mA drive capability.
27	MEMR-	I/O	MEMORY READ is an active low bidirectional signal directing memory to place valid data on the data bus. MEMR- is an output if the CPU is controlling the bus or an input if a DMA or external bus master is in control of the bus. As an output, this signal has a 12mA drive capability.
29	MEMW-	I/O	MEMORY WRITE is an active low bidirectional signal directing memory to accept data from the data bus. MEMW- is an output if the CPU is controlling the bus or an input if a DMA or external bus master is in control of the bus. As an output, this signal has a 12mA drive capability.
30	IOR-	I/O	I/O READ is an active low bidirectional signal instructing an I/O device to place data on the data bus. IOR- is an output if the CPU is controlling the bus or an input if a DMA controller is in control of the bus. As an output, this signal has a 12mA drive capability.
31	IOW-	I/O	I/O WRITE is an active low bidirectional signal instructing an I/O device to accept data from the data bus. IOW- is an output if the CPU is controlling the bus or an input if a DMA controller is in control of the bus. As an output, this signal has a 12mA drive capability.
12	BALE	O	BUFFERED ADDRESS LATCH ENABLE is an active high output to the AT expansion Bus. BALE indicates a valid address on the SA bus. It is used to hold the address during a AT bus cycle. This signal has a 12mA drive capability.
157	SBHE-	I/O	SYSTEM BUS HIGH ENABLE is an active low bidirectional signal to or from the AT expansion Bus. When active, SBHE- indicates when the high byte transfer is taking place. As an output, this signal has a 12mA drive capability.
16	SMEMR-	O	SYSTEM MEMORY READ is an active low output signal to the AT expansion Bus. When active, SMEMR- indicates that the lowest 1 megabyte memory space is being addressed for a read cycle. This signal has a 12mA drive capability.
17	SMEMW-	O	SYSTEM MEMORY WRITE is an active low output signal to the AT expansion Bus. When active, SMEMR- indiactes that the lowest 1 emgabyte memory space is being addressed by a write cycle. This signal has 12 ma drive capability.
28	LPAR-	I	LATCHED PARITY is an active low input from the 82C315. When active, LPAR- indicates a parity error during a local memory read cycle and causes an NMI to be generated. The failing address is latched by this signal within 82C311.
133	CPUA20	I/O	CPU ADDRESS bit 20 is from the 80386. This has 2ma drive capability.

Pin #	Symbol	Type	Signal Description
86	SGLROM	I	SIGNAL ROM is an active high input indicating an access to a 8 bit ROM accessory device. SGLROM should be tied low when not used.
115	FGA20	I/O	FAST GATE ADDRESS 20 is a open drain input/output signal used to control the gating of CPUA20. When FGA20 is low, 82C311 propagates CPUA20. When FGA20 is high the 82C311 forces A20 to be low regardless of CPUA20 state. FGA20 may be derived from the 8042 or 8742 keyboard controller. The signal may also be generated internal to the 82C311 when fast GATEA20 feature is enabled(REG2B). When the fast GATEA20 feature is enabled
114	WTPRES-	I	WEITEK PRESENT is an active low input indicating the presence of a WEITEK coprocessor. WTPRES- should be pulled high with a 10K ohm resistor when not used.
14	VRAMSEL-	O	VIDEO RAM SELECT is an active low output indicating the current cycle is a VRAM access. This signal will be active when addresses A31 to A20 are low, A19 to A17 are high, and A18 is low (A0000 to BFFFF). This signal has a 2mA drive capability.
87	HIT/MISS	O	When the signal is high, it indicates a hit cycle. When low, it indicates a miss cycle. It goes active on the first negative edge of CLK2 in T2 (for example, 1/2 CLK2 after T1) for 0 wait state, and for 1 wait state; the hit goes active at the middle of T2. The hit goes high at the end of the cycle on the rising edge of READY- signal. This has 2ma drive capability.
15	N/C		No connection.

Power and Grounds

Pin #	Symbol	Type	Signal	Description
18, 40, 50, 56, 66, 80 99, 120, 160	VCC	I	Vcc	Supply Voltage, 5V ± 5%
1, 26, 41 51, 57, 67, 81, 100, 121	VSS	I	Vss	Ground

82C311 Maximum Ratings and Operating Conditions

Table 2-47. Absolute Maximum Ratings

	Symbol	Min.	Max.	Units
Supply Voltage	Vcc		7.0	V
Input Voltage	V_I	-.5	5.5	V
Output Voltage	V_O	-.5	5.5	V
Operating Temperature	Top	-25	85	C
Storage Temperature	Tstg	-40	125	C

Note Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. Exceeding the absolute maximum ratings can cause permanent damage to the device.

Table 2-48. Operating Condition

	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A		70	C

DC Characteristics

	Symbol	Min.	Max.	Units
Input low voltage	V_{1L}			
TTL level (all pins except RESET1)			.8	V
SHMT level (RESET1, IOCHRDY, OWS)			1.0	V
CLK1, BCLK, SCLK (CMOS)			1.5V	
Input high voltage	V_{1H}			
TTL level (all pins except RESET1 and CLK2)		2.0		V
CLK2, SCLK, BCLK (CMOS)		3.5		V
SHMT level (RESET1, IOCHRDY, 0WS)		4.0		
Output low voltage	V_{OL}		0.4V	V
Output high voltage	V_{OH}			
All pins except FGA20		2.4		V
FGA20 pin has open drain driver				
Input LOW current @ Vo = Vss BCLK,,SCLK, RESET1, IOCHRDY, OWS	I_{IL}	-10	10	µA
All input and I/O pins except, BCLK,,SCLK, RESET1, IOCHRDY, OWS		-200	-10	µA
Input HIGH current @Vo = Vdd BCLK,,SCLK, RESET1, IOCHRDY, OWS	I_{IH}		10	
All input and I/O pins except, BCLK,,SCLK, RESET1, IOCHRDY, OWS		10	200	µA
3-state output OFF current LOW (no pull-up)	I_{OZL}		-10	µA
3-state output OFF current LOW (with pull-up)			-200	µA
3-state output OFF current HIGH (no pull-up)	I_{OZH}		10	µA
3-state output OFF current HIGH (with pull-up)			-10	µA
Output leakage current	I_{OH}			
Output short circuit current	I_{OS}			
Power supply current @ 25 MHz	I_{CC}		200	mA
Input capacitance	C_{IN}			
Output or I/O capacitance	C_{OUT}			

AC Characteristics

All timing parameters are specified under capacitive load of 50 pf and temperature of 70 degree C. All the units discussed in the following timing tables are in nanoseconds, unless otherwise specified. Also, the AC specifications mentioned in this document are subject to change.

Table 2-49. *Memory Cycle*

	Memory Cycle	33 MHz	
		Min.	Max.
t101	Operating frequency	8	33.33 MHz
t102	CLK2 period	15	
t103	CLK2 high time at 2V	6.25	
t104	CLK2 high time at Vcc-0.8V	4.5	
t105	CLK2 low time at 2V	6.25	
t106	CLK2 low time at 0.8V	4.5	
t107	CLK2 fall time (Vcc-0.8 to 0.8V)	4	
t108	CLK2 rise time (0.8V to Vcc-0.8V)	4	
t120	Address setup to CLK2 high	15	
t126	MALE- active from CLK2 high	0	25
t127	MALE- inactive from CLK2 low	0	25
t130	CRD<1:0>- active delay from CLK2 high 0WS read hit cycles	0	13
t131	CRD<1:0>- active delay from CLK2 low for all other cycles	0	20
t132	CRD<1:0>- active delay from CLK2 high (for 1 ws read hits)	0	28
t133	CRD<1:0>- inactive delay from CLK2 high	0	20
t134	READY- active delay from CLK2 low	4	14
t134a	READY- active delay from CLK2 high	4	22
t135	READY- inactive delay from CLK2 high	4	19
t136	CALE- high to low delay from CLK2 low	0	22
t137	CALE- high to low delay from CLK2 high	0	20
t138	CALE- inactive from CLK2 high	0	20
t142	RAS- active delay from CLK2 high	0	18
t143	RAS- inactive delay from CLK2 high	2	21
t145	Row address active to RAS active	7	
t147	Column address valid to CAS- active	7	
t150	CAS- active delay from CLK2 high	0	26
t151	CAS- incative delay from CLK2 high	5	26
t153	DRD- active delay from CLK2 high	0	40
t154	DRD- inactive delay from CLK2 high	0	25
t155	FBE- active delay from CLK2 low(0 ws)	0	25
t156	FBE- active delay from CLK2 high(1 ws)	0	25

Table 2-49. Memory Cycles (continued)

	Memory Cycle	33 MHz	
		Min.	Max.
t157	FBE- inactive delay from CLK2 low	0	25
t158	CWE- active delay from CLK2 low	0	15
t159	CWE- active delay from CLK2 high	0	25
t160	CWE- inactive delay from CLK2 high	0	9.5
t161	DWE- active delay from CLK2 high	0	26
t162	DWE- inactive delay from CLK2 high	0	40
t163	LDBCAB low to high delay from CLK2 high	0	20
t164	LDBCAB high to low delay from CLK2 high	0	25
t165	LDBDIR valid from CLK2 low	0	25
t166	Row address hold time from RAS active	15	
t167	BWBUSY active delay from CLK2 high	0	20
t167a	BWBUSY inactive delay from CLK2 high	0	30
t168	BST128K active delay from CLK2 high	0	30
t168a	BST128K inactive delay from CLK2 high	0	30

Table 2-50. DMA Cycle

	DMA Cycle	33 MHz		
		Min.	Typical	Max.
t170	Command setup time to CLK2 high	10		
t171	RAS- active delay from CLK2 high	0		20
t172	RAS- inactive delay from commands inactive	0		30
t173	Row address delay from address valid			20
t174	Row address hold time from CLK2 low	10		20
t175	Column address setup to CAS- active		1.5CLK2	
t176	Column address hold time from commands inactive	10		40
t177	CAS- active delay from RAS- active for DMA memory read cycle		3CLK2	
t178	CAS- active delay from RAS- active for DMA memory write cycle		4CLK2	
t179	CAS- active delay from CLK2 high	8		20
t180	CAS- inactive delay from commands inactive	8		20
t183	DRD- active delay from CLK2 high	5		30
t184	DRD- inactive delay from commands inactive	5		20
t185	AF32- active delay from command active	0		20
t186	AF32- inactive delay from command inactive	0		15
t187	DWE- active delay from CLK2 high	0		17
t188	DWE- inactive delay from commands inactive	0		17
t189	CRD- and CWE- active delay from CLK2 high	0		20
t190	CRD- and CWE- inactive delay from CLK2 high	10		25

Table 2-51. *ROM Cycle*

	ROM Cycle	33 MHz	
		Min.	Max.
t191	ROMCS- active delay from CLK2 high	0	28
t192	ROMCS- inactive delay from CLK2 high	0	25
t193	READY- input setup time to CLK2 high	15	
t194	READY- input hold time from CLK2 high	5	

Table 2-52. *AT Bus Access*

	AT Bus Access	33 MHz	
		Min.	Max.
t1100	ATEN- active from CLK2 high	0	22
t1101	ATEN- inactive from CLK2 high	0	22
t1102	BALE active from BUSCLK low	10	20
t1103	BALE inactive from BUSCLK high	10	20
t1104	Command active delay from BUSCLK low	10	20
t1105	Command inactive from BUSCLK high	10	20
t1106	ACEN- active delay from BUSCLK low (read)	10	20
t1107	ACEN- inactive delay from BUSCLK high	10	20
t1108	AC<3:0> active delay from BUSCLK low	10	20
t1110	IOCHRDY setup to BUSCLK low	10	
t1111	IOCHRDY hold from BUSCLK low	5	

Table 2-53. *AC Specification*

	AC Specification	33 MHz	
		Min.	Max.
t1112	MCS16-, IOCS16- setup to BUSCLK high	20	
t1114	MCS32-, IOCS32- setup from BUSCLK high	20	
t1116	Command active delay from BUSCLK high (Write or 0WS)	10	20
t1117	ACEN- active delay from BUSCLK high (Write)	10	25
t1118	ACEN- inactive delay from BUSCLK high (Write)	10	25
t1119	0WS- setup to BUSCLK low	20	
t1120	0WS- hold time from BUSCLK low	20	
t1123	XA<1:0>,SBHE- valid delay from BUSCLK low	0	18
t1124	XA<1:0>, SBHE invalid delay from BUSCLK low	0	18

Table 2-54. DMA Arbitration

DMA Arbitration		33 MHz	
		Min.	Max.
t1140	HRQn active setup to CLK2 high	15	
t1142	HOLD active delay from CLK2 high	2	25
t1144	HLDAn active delay from HLDA	0	19

Table 2-55. REFRESH Arbitration

REFRESH Arbitration		33 MHz	
		Min.	Max.
t1150	MEMR- delay from BUSCLK high	0	25

Table 2-56. RESET Timing

RESET Timing		33 MHz		
		Min.	Typical	Max.
t1170	RESET3 active delay from CLK2	0		25
t1171	RESET3 inactive delay from CLK2 high	2		10
t1172	RESET3 pulse width		78CLK2	
t1173	RESET4 active delay from CLK2 high	0		25
t1174	RESET4 inactive delay from CLK2 high	2		25
t1175	RESET4 active from RESET1- active		4CLK2	
t1176	RESET3 active from RESET1- inactive		2CLK2	

Table 2-57. Miscellaneous

Miscellaneous		33 MHz	
		Min.	Max.
t1185	BUSCLK low delay from BCLK high	0	22
t1186	BUSCLK high delay from BCLK high	0	22
t1187	BUSCLK high pulse width		140
t1188	BUSCLK low pulse width		140
t1189	BUSCLK rise time		6
t1190	BUSCLK low time		6

Table 2-58. *AC Specification*

AC Specification	33 MHz	
	Min.	Max.
t1191 FGA20 valid from IOW-		18
t1192 PEN valid from IOW- high		18
t1193 A20 delay from CPUA20	0	7

Table 2-59. *RESET Cycle*

REFRESH Cycle	33 MHz		
	Min.	Typical	Max.
t1200 RASi- active delay from CLK2 high	0		25
t1201 RASi- inactive delay from CLK2 high	0		25
t1202 RASi pulse width		4CLK2	
t1203 RAS(i+1) active delay RASi active		1CLK2	
t1204 REFERSH address setup time to RAS0		2CLK2	
t1205 REFERSH address hold from RAS		2CLK2	

Table 2-60. *I/O Cycle*

I/O Cycle	33 MHz	
	Min.	Max.
t1214 XDEN- active delay from XIOR- or XIOW-	15	26
t1215 XDEN- inactive delay from XIOR- or XIOW-	12	25
t1218 XDA output valid delay to XIOR-	0	30
t1219 XDA output hold time to XIOR-	0	30

Table 2-61. *LPAR Timing*

LPAR Timing	33 MHz	
	Min.	Max.
t1220 LPAR- input setup time to CAS-	10	

Note: The parameters t158 and t160 tracks so that the write pulse width for SRAM is met. The tracking requirement is t158-t160 should be greater than -2 and less than 5ns.

The New tracking parameters are:

1. t138 - t160 > 1ns
2. t158 - t160 < 5ns
3. t142 - t143 < 4ns

Table 2-62. Memory Cycle

	Memory Cycle	25 MHz	
		Min.	Max.
t101	Operating frequency	4	25MHz
t102	CLK2 period	20	125
t103	CLK2 high time at 2V	7	
t104	CLK2 high time at Vcc-0.8V	4	
t105	CLK2 low time at 2V	7	
t106	CLK2 low time at 0.8V	5	
t107	CLK2 fall time (Vcc-0.8 to 0.8V)	7	
t108	CLK2 rise time(0.8V to Vcc-0.8V)	7	
t120	Address setup to CLK2 high	18	
t126	MALE- active from CLK2 high	0	25
t127	MALE- inactive from CLK2 low	0	25
t130	CRD<1:0>- active delay from CLK2 high 0WS read hit cycles	0	17
t131	CRD<1:0>- active delay from CLK2 low for all other cycles	0	30
t132	CRD<1:0>- active delay from CLK2 high (for 1 ws read hits)	0	38
t133	CRD<1:0>- inactive delay from CLK2 high	0	20
t134	READY- active delay from CLK2 low	4	19
t134a	READY- active delay from CLK2 high	4	30
t135	READY- inactive delay from CLK2 high	4	19
t136	CALE- high to low delay from CLK2 low	0	25
t137	CALE- high to low delay from CLK2 high	0	25
t138	CALE- inactive from CLK2 high	0	25
t142	RAS- active delay from CLK2 high	0	30
t143	RAS- inactive delay from CLK2 high	2	24
t145	Row address active to RAS active	7	
t147	Column address valid to CAS- active	7	
t150	CAS- active delay from CLK2 high	0	37
t151	CAS- incative delay from CLK2 high	5	37
t153	DRD- active delay from CLK2 high	0	40
t154	DRD- inactive delay from CLK2 high	0	25
t155	FBE- active delay from CLK2 low (0 ws)	0	25
t156	FBE- active delay from CLK2 high (1 ws)	0	25
t157	FBE- inactive delay from CLK2 low	0	25
t158	CWE- active delay from CLK2 low	0	25
t159	CWE- active delay from CLK2 high	0	25
t160	CWE- inactive delay fromCLK2 high	0	14.5
t161	DWE- active delay from CLK2 high	0	26
t162	DWE- inactive delay from CLK2 high	0	40
t163	LDBCAB low to high delay from CLK2 high	0	30
t164	LDBCAB high to low delay from CLK2 high	0	25

Table 2-62. *Memory Cycle (continued)*

	Memory Cycle	25 MHz Min.	25 MHz Max.
t165	LDBDIR valid from CLK2 low	0	25
t166	Row address hold time from RAS active	15	
t167	BWBUSY active delay from CLK2 high	0	30
t167a	BWBUSY inactive delay from CLK2 high	0	30
t168	BST128K active delay from CLK2 high	0	30
t168a	BST128Kinactive delay from CLK2 high	0	30

Table 2-63. *DMA Cycle*

	DMA Cycle	25 MHz Min.	25 MHz Typical	25 MHz Max.
t170	Command setup time to CLK2 high	10		
t171	RAS- active delay from CLK2 high	0		20
t172	RAS- inactive delay from commands inactive	0		30
t173	Row address delay from address valid			20
t174	Row address hold time from CLK2 low	10		20
t175	Column address setup to CAS- active		1.5CLK2	
t176	Column address hold time from commands inactive	10		40
t177	CAS- active delay from RAS- active for DMA memory read cycle		3CLK2	
t178	CAS- active delay from RAS- active for DMA memory write cycle		4CLK2	
t179	CAS- active delay from CLK2 high	8		20
t180	CAS- inactive delay from commands inactive	8		20
t183	DRD- active delay from CLK2 high	5		30
t184	DRD- inactive delay from commands inactive	5		20
t185	AF32- active delay from command active	0		20
t186	AF32- inactive delay from command inactive	0		15
t187	DWE- active delay from CLK2 high	0		17
t188	DWE- inactive delay from commands inactive	0		17
t189	CRD- and CWE- active delay from CLK2 high	0		20
t190	CRD- and CWE- inactive delay from CLK2 high	10		25

Table 2-64. *ROM Cycle*

	ROM Cycle	25 MHz Min.	25 MHz Max.
t191	ROMCS- active delay from CLK2 high	0	28
t192	ROMCS- inactive delay from CLK2 high	0	25
t193	READY- input setup time to CLK2 high	15	
t194	READY- input hold time from CLK2 high	5	

Table 2-65. AT Bus Access

AT Bus Access		25 MHz	
		Min.	Max.
t1100	ATEN- active from CLK2 high	0	22
t1101	ATEN- inactive from CLK2 high	0	22
t1102	BALE active from BUSCLK low	10	20
t1103	BALE inactive from BUSCLK high	10	20
t1104	Command active delay from BUSCLK low	10	20
t1105	Command inactive from BUSCLK high	10	20
t1106	ACEN- active delay from BUSCLK low(read)	10	20
t1107	ACEN- inactive delay from BUSCLK high	10	20
t1108	AC:0 active delay from BUSCLK low	10	20
t1110	IOCHRDY setup to BUSCLK low	10	
t1111	IOCHRDY hold from BUSCLK low	5	
t1112	MCS16-,IOCS16- setup to BUSCLK high	20	
t1114	MCS32-,IOCS32- setup from BUSCLK high	20	
t1116	Command active delay from BUSCLK high (write or 0WS)	10	20
t1117	ACEN- active delay from BUSCLK high (write)	10	25
t1118	ACEN- inactive delay from BUSCLK high (Write)	10	25
t1119	0WS- setup to BUSCLK low	20	
t1120	0WS- hold time from BUSCLK low	20	
t1123	XA<1:0>,SBHE- valid delay from BUSCLK low	0	18
t1124	XA<1:0>,SBHE invalid delay from BUSCLK low	0	18

Table 2-66. DMA Arbitration

DMA Arbitration		25 MHz	
		Min.	Max.
1140	HRQn active setup to CLK2 high	15	
t1142	HOLD active delay from CLK2 high	2	25
t1144	HLDAn active delay from HLDA	0	19

Table 2-67. REFRESH Arbitration

REFRESH Arbitration		25 MHz	
		Min.	Max.
t1150	MEMR- delay from BUSCLK high	0	25

Table 2-68. *RESET Timing*

RESET Timing		25 MHz		
		Min.	Typical	Max.
t1170	RESET3 active delay from CLK2	0		25
t1171	RESET3 inactive delay from CLK2 high	2		15
t1172	RESET3 pulse width		78CLK2	
t1173	RESET4 active delay from CLK2 high	0		25
t1174	RESET4 inactive delay from CLK2 high	2		25
t1175	RESET4 active from RESET1- active		4CLK2	
t1176	RESET3 active from RESET1- inactive		2CLK2	

Table 2-69. *Miscellaneous*

Miscellaneous		25 MHz	
		Min.	Max.
t1185	BUSCLK low delay from BCLK high	0	22
t1186	BUSCLK high delay from BCLK high	0	22
t1187	BUSCLK high pulse width		140
t1188	BUSCLK low pulse width		140
t1189	BUSCLK rise time		6
t1190	BUSCLK low time		6
t1191	FGA20 valid from IOW-		18
t1192	PEN valid from IOW- high		18
t1193	A20 delay from CPUA20	0	7

Table 2-70. *REFRESH Cycle*

REFRESH Cycle		25 MHz		
		Min.	Typical	Max.
t1200	RASi- active delay from CLK2 high	0		25
t1201	RASi- inactive delay from CLK2 high	0		25
t1202	RASi pulse width		4CLK2	
t1203	RAS(i+1) active delay RASi active		1CLK2	
t1204	REFERSH address setup time to RAS0		2CLK2	
t1205	REFERSH address hold from RAS		2CLK2	

Table 2-71. *I/O Cycle*

I/O Cycle		25 MHz	
		Min.	Max.
t1214	XDEN- active delay from XIOR- or XIOW-	15	26
t1215	XDEN- inactive delay from XIOR- or XIOW-	12	25
t1218	XDA output valid delay to XIOR-	0	30
t1219	XDA output hold time to XIOR-	0	30

Table 2-72. LPAR Timing

LPAR Timing	25 MHz	
	Min.	Max.
t1220 LPAR- input setup time to CAS-	10	

Note: The parameters t158 and t160 tracks so that the write pulse width for SRAM is met. The tracking requirement is t158-t160 should be greater than -2 and less than 8ns.

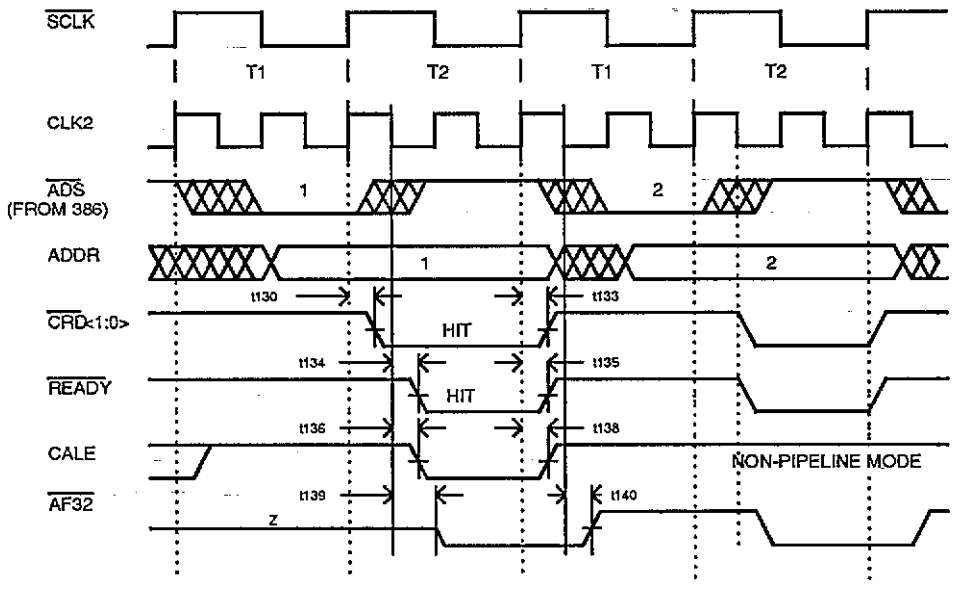
The New tracking parameters are:

1. t138 - t160 > 1ns
2. t158 - t160 < 8ns
3. t142 - t143 < 4ns

The AC specifications mentioned in this document are subject to change.

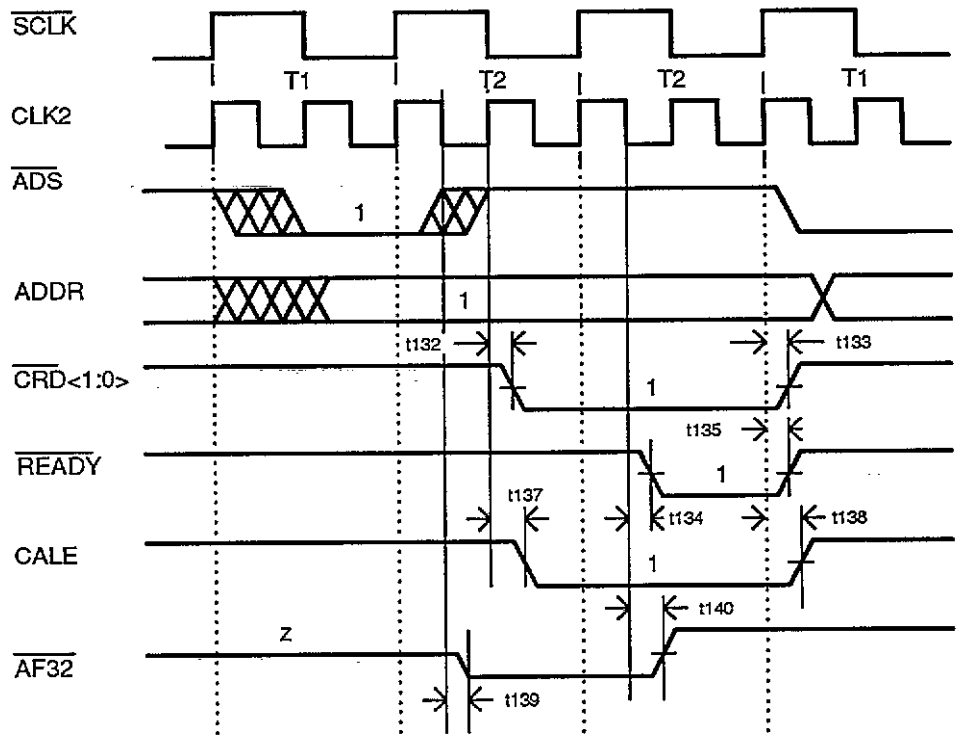
82C311C Timing Diagrams

Figure 2-27. *82C311C Read Hit Cycle 0WS SRAM*



READ HIT CYCLE, 0 WS SRAM, NON-PIPELINE MODE
82C311 REV. C

Figure 2-28. *82C311C Read Hit Cycle 1WS SRAM*



READ HIT CYCLE, 1 WS NON-PIPELINE CYCLE.
82C311 REV.C

Figure 2-29. *82C311C Read Miss Cycle 4WS DRAM, 0WS SRAM*

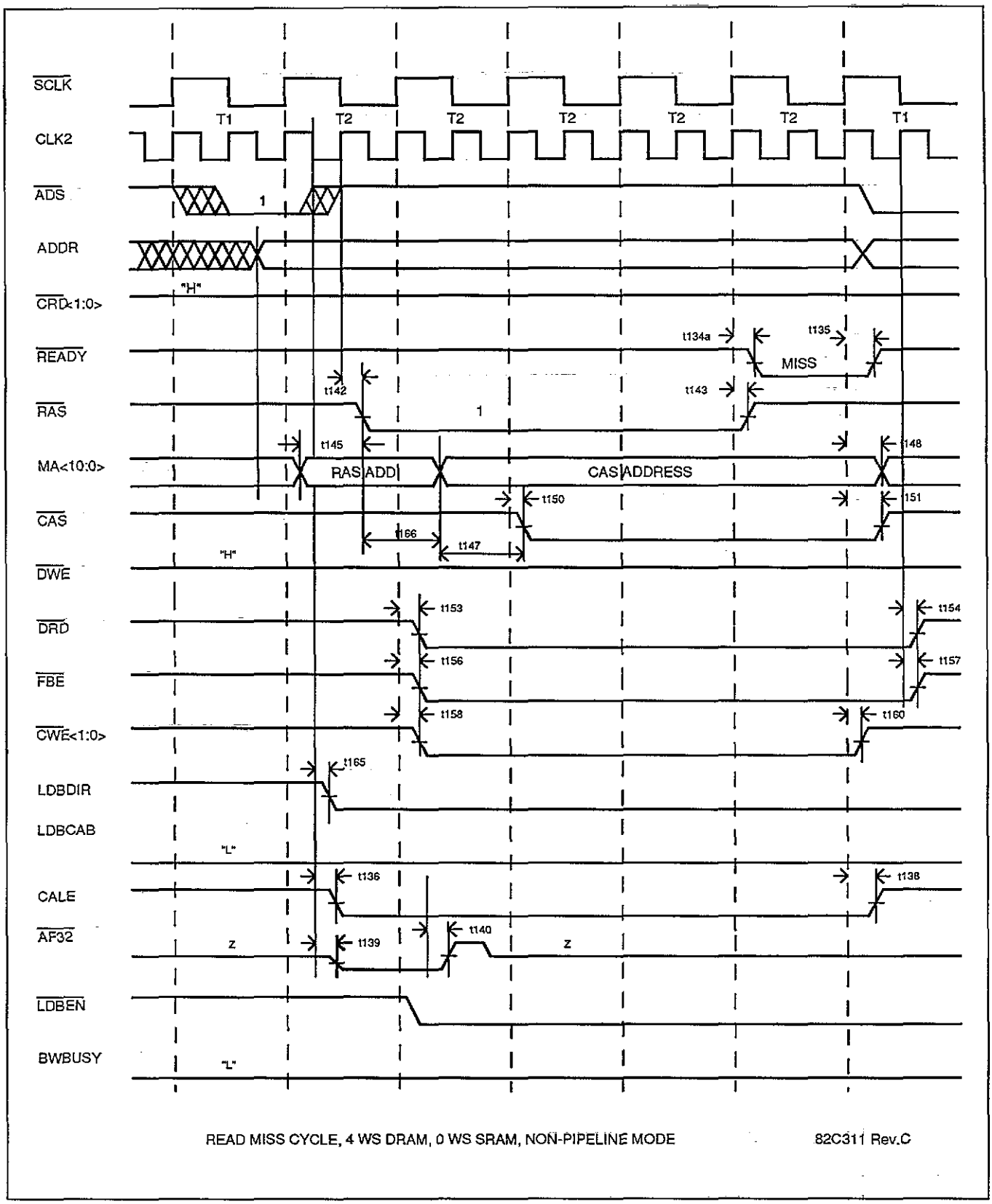


Figure 2-30. *82C311C Write Hit/Miss Cycle 4WS DRAM, 0WS SRAM*

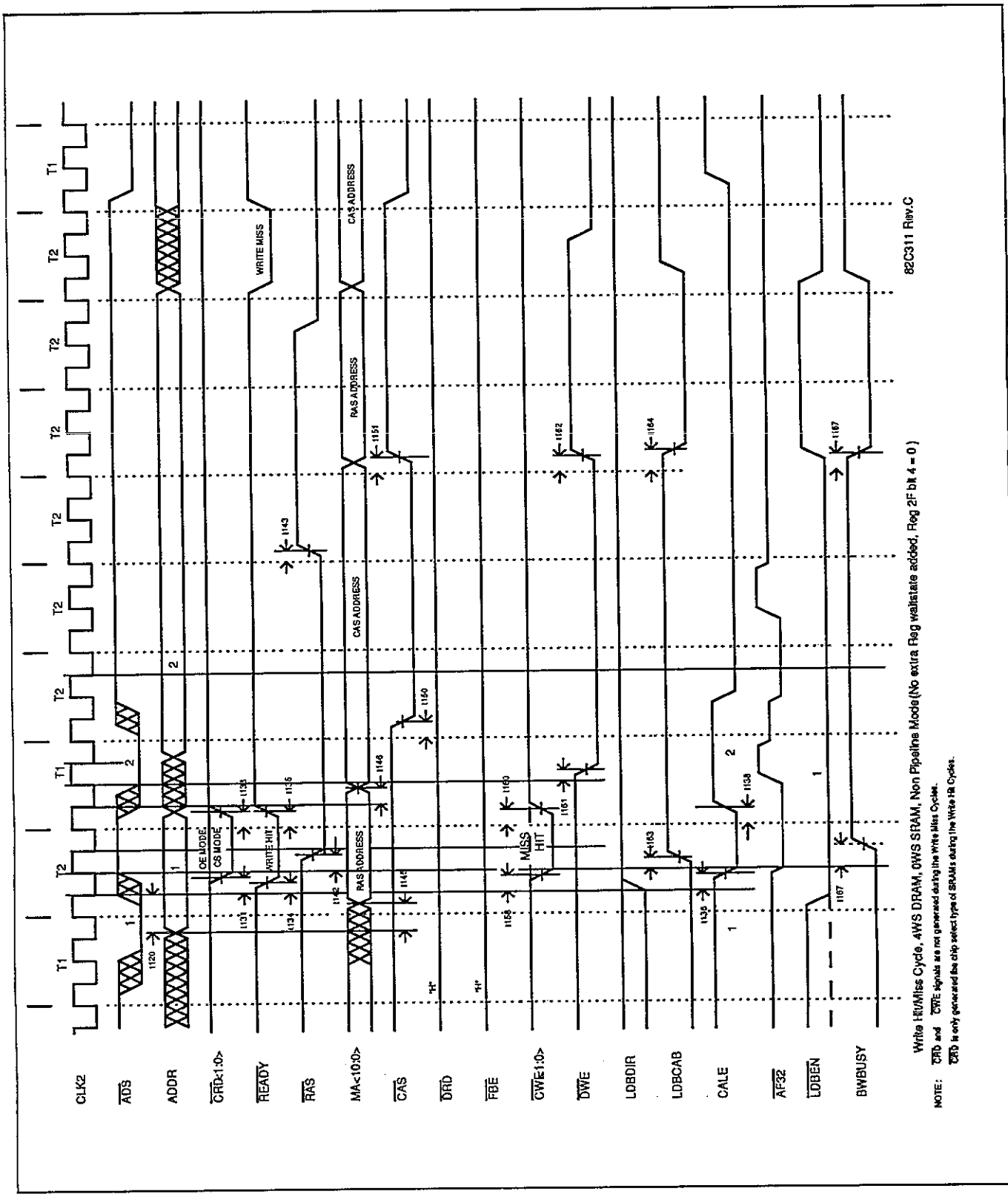


Figure 2-31. *82C311 128K Cache Read Miss Cycle*

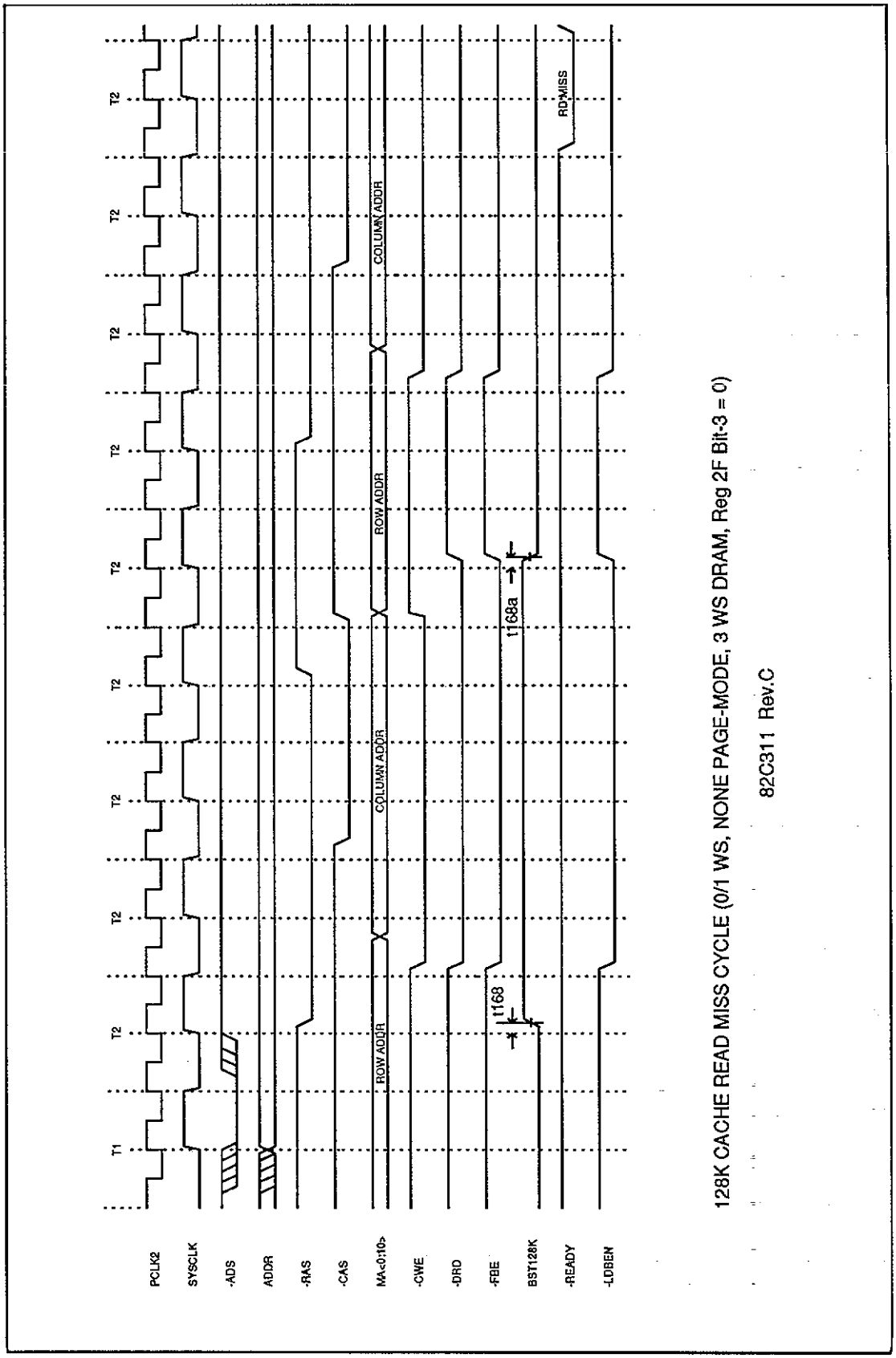


Figure 2-32. *82C311 CLK2 Timing Waveforms*

Clock 2 Waveforms

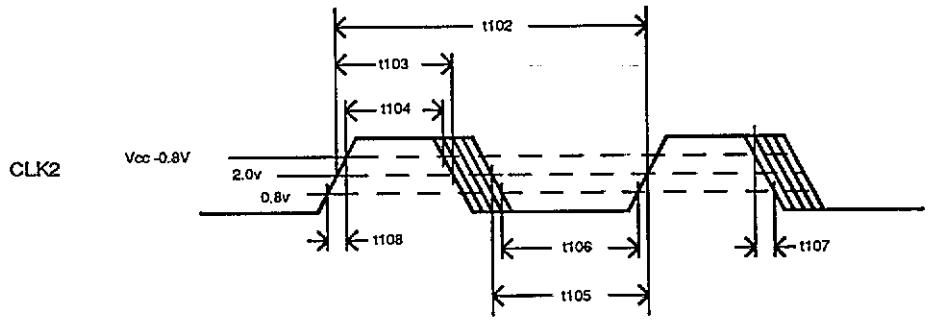
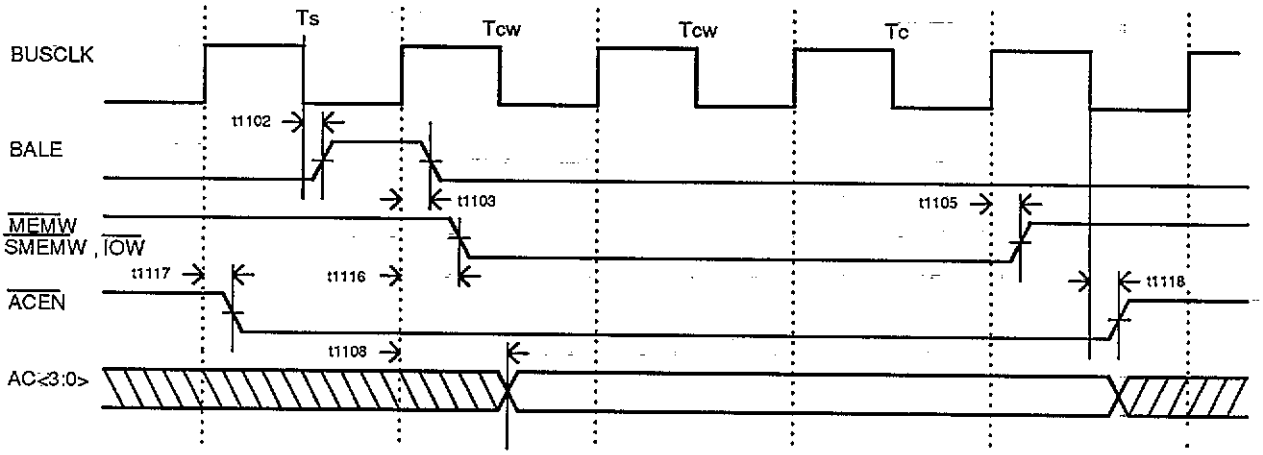
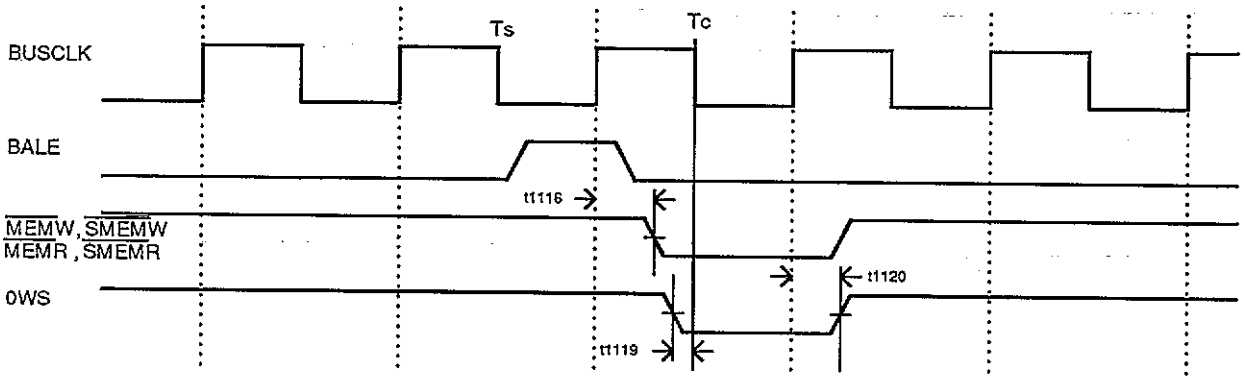


Figure 2-33. *82C311 AT Cycle (2 Wait States and 0 Wait State)*



AT Write Cycle (2 Wait States)



AT 0 Wait State Cycle

Figure 2-34. *82C311 AT Read Cycle*

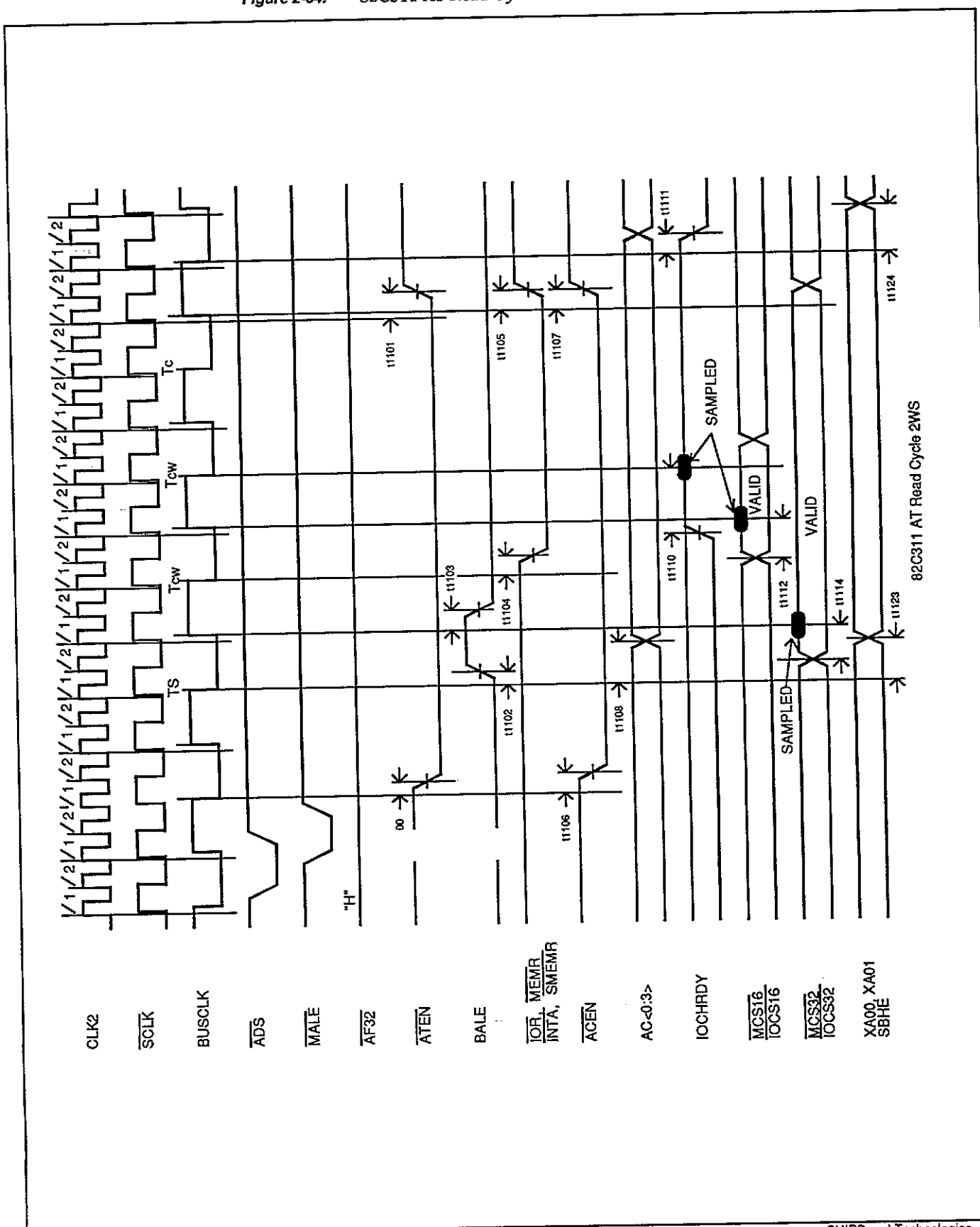
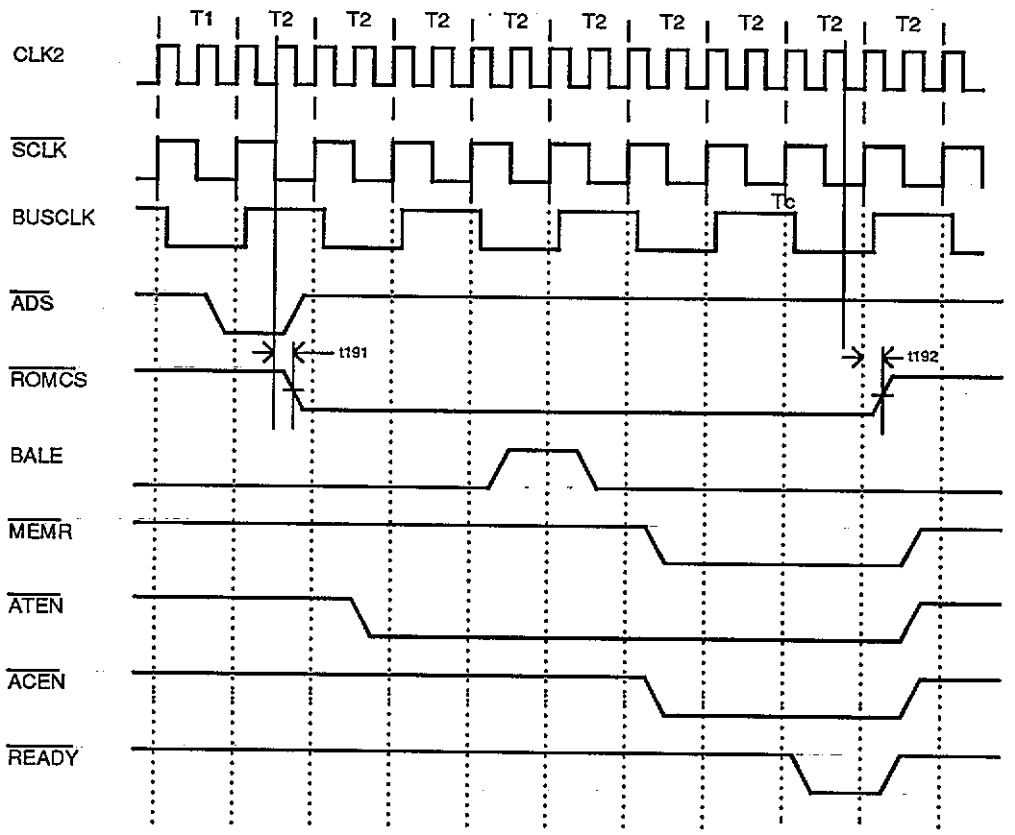


Figure 2-35. *82C311 ROM Read Cycle*



ROM READ CYCLE

Figure 2-36. *82C311 Resets*

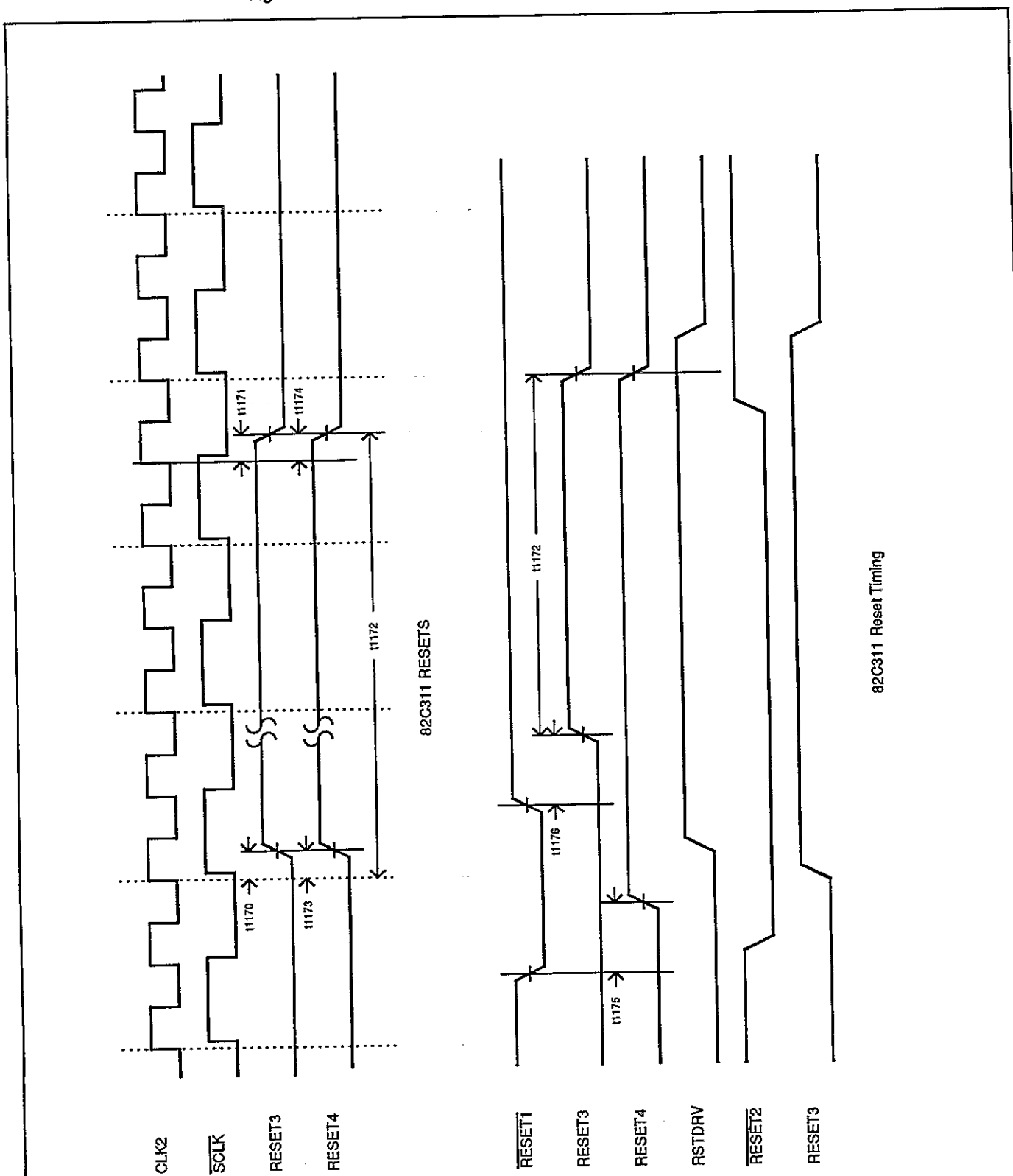
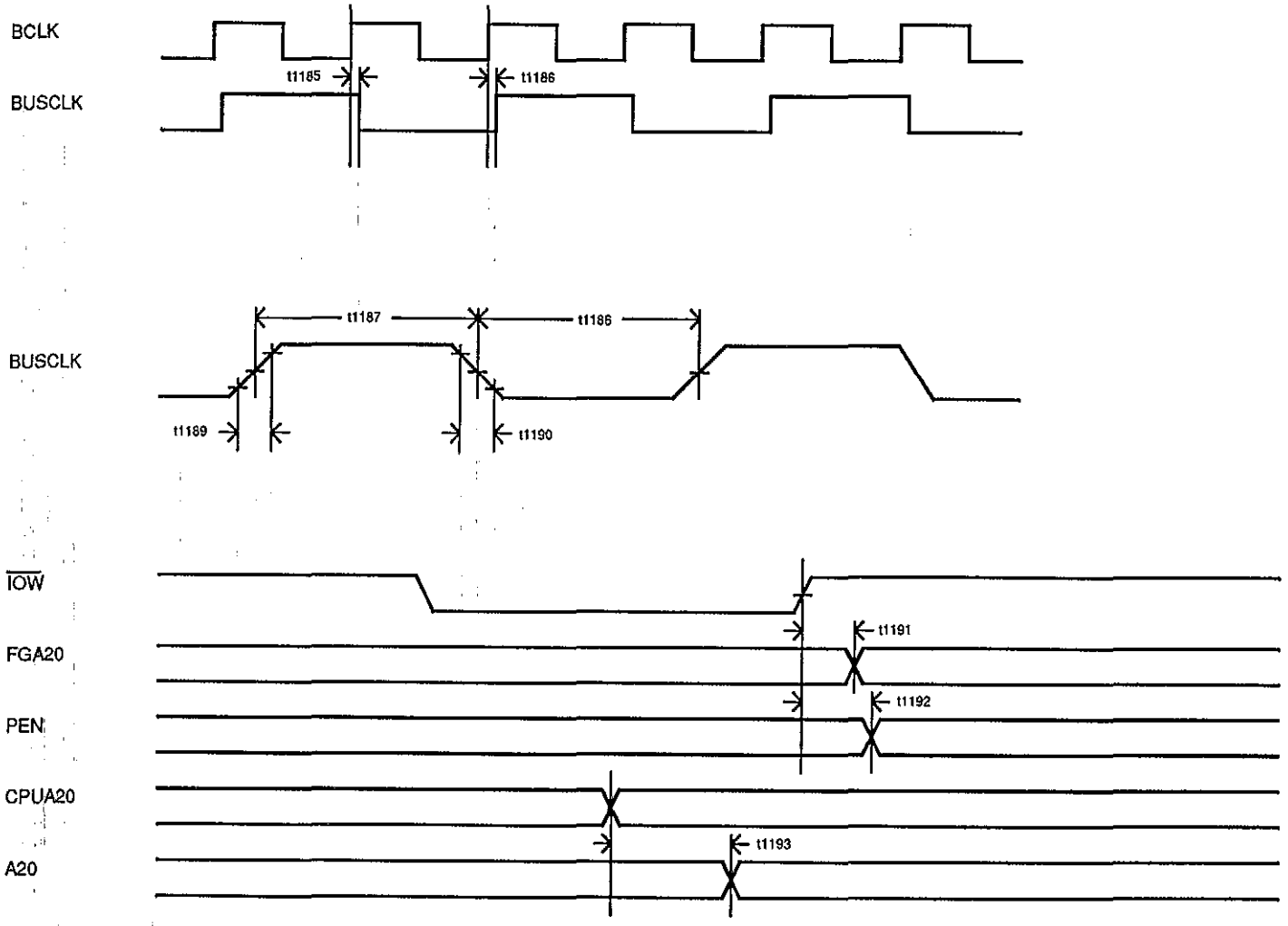


Figure 2-37. 82C311 Miscellaneous Timing



82C311 Misc Timing

Figure 2-38. *82C311 Refresh Cycle*

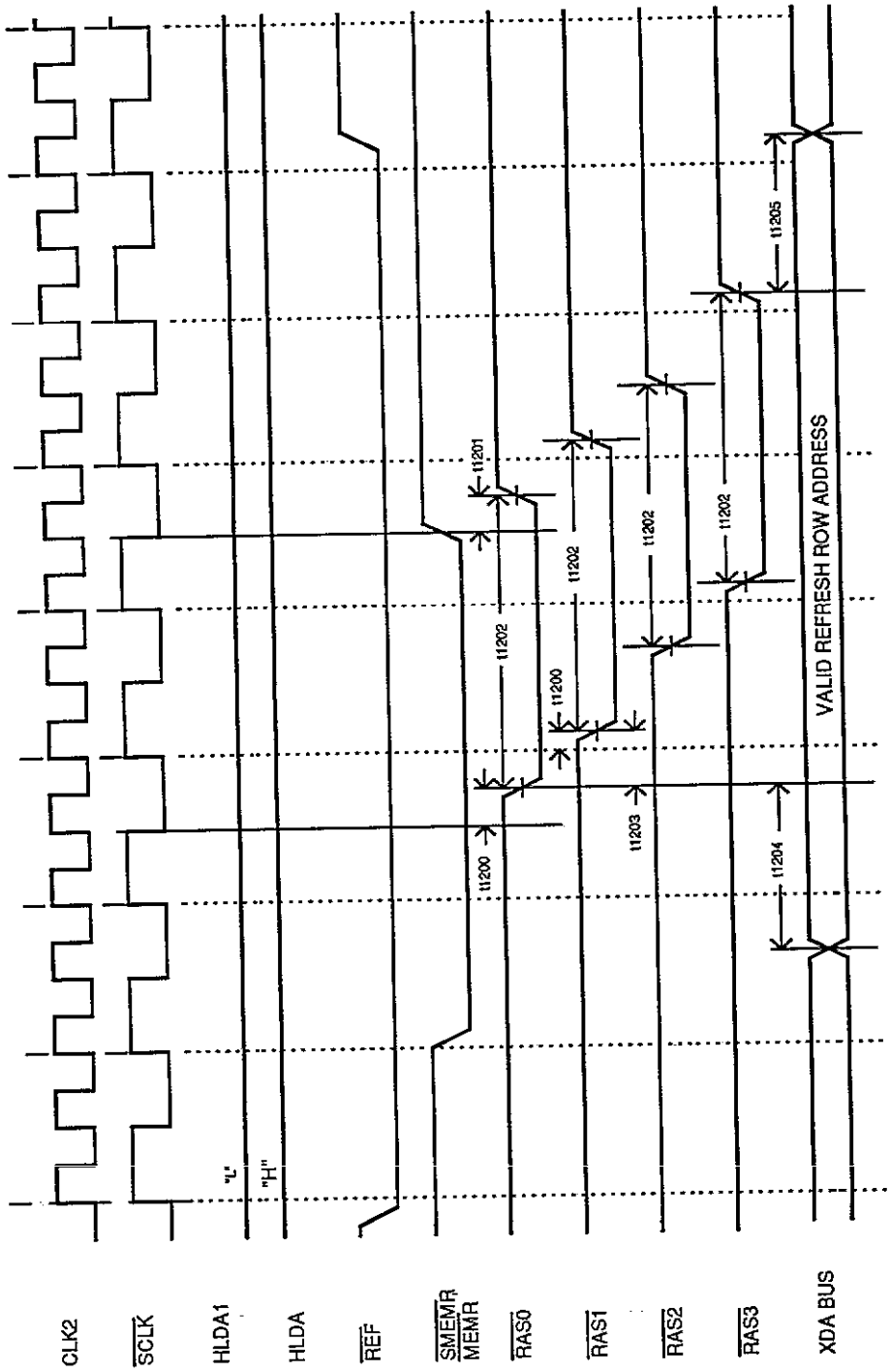


Figure 2-39. *82C311 Refresh Arbitration*

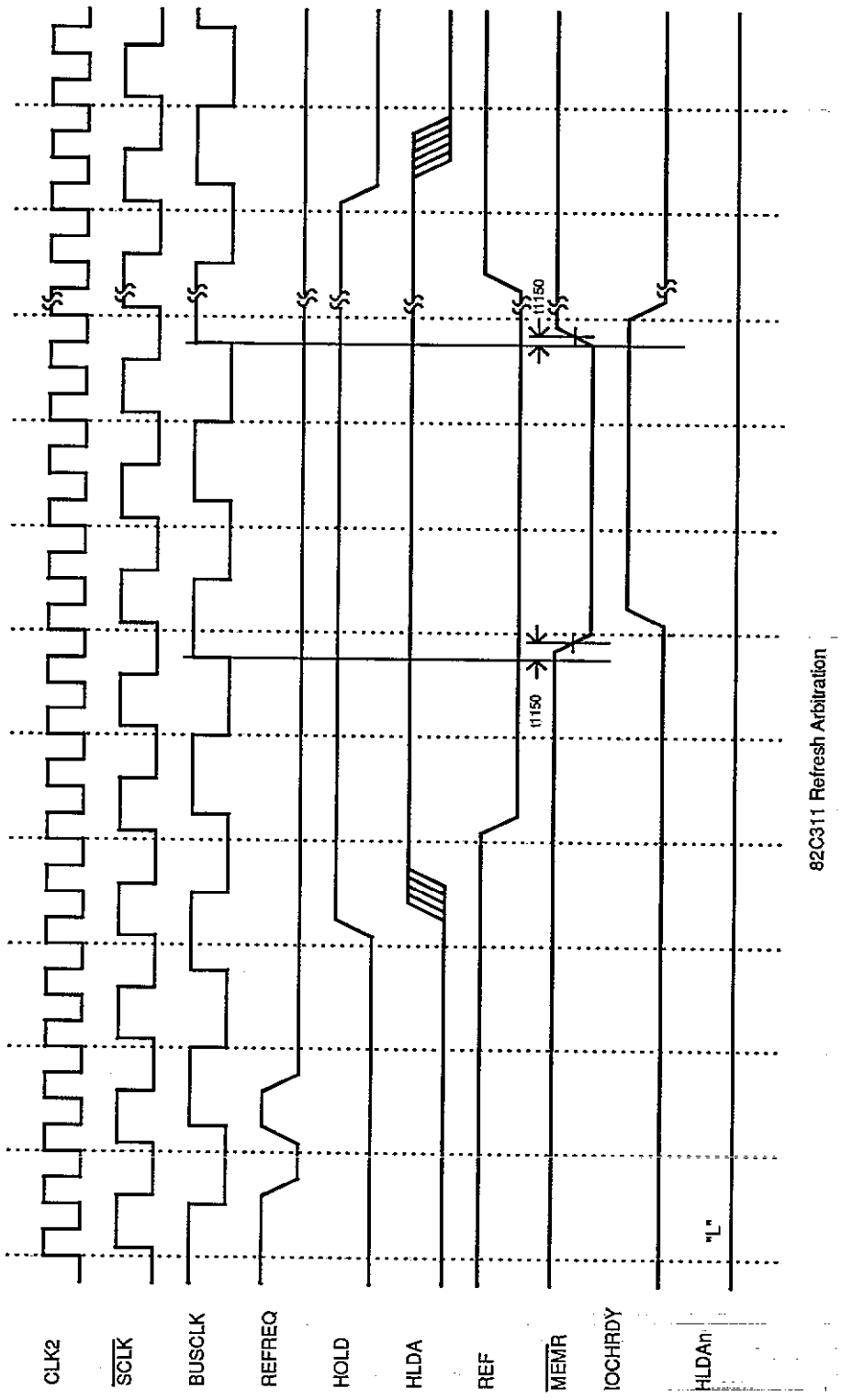
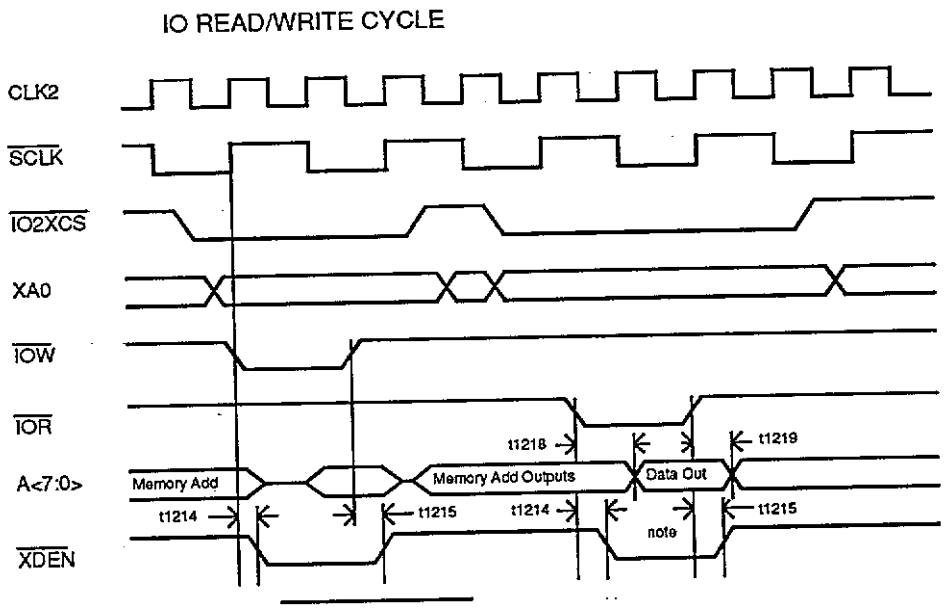
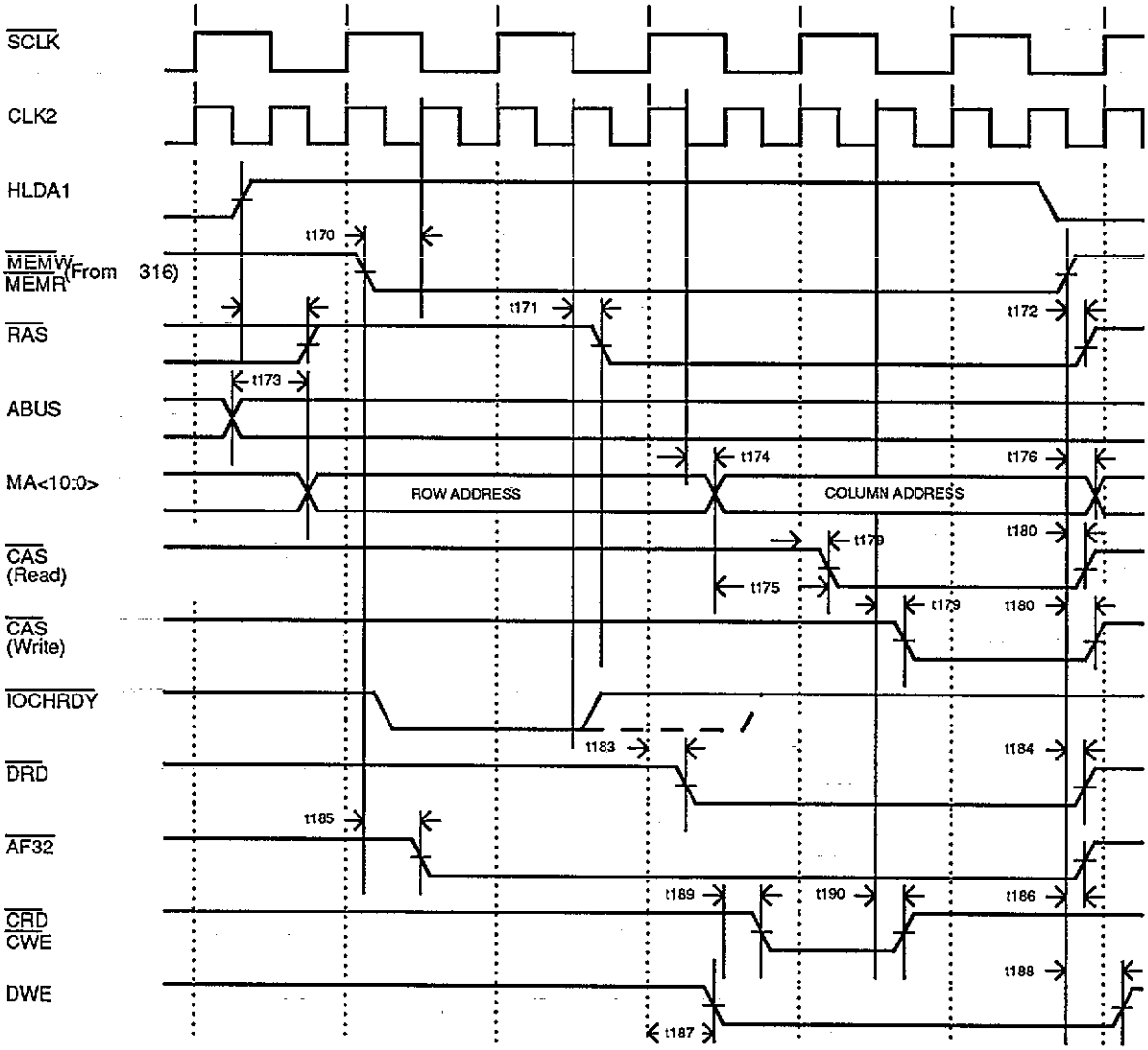


Figure 2-40. *82C311 I/O Read/Write Cycle*



Note No data output and XDEN is inactive if the index setup by the previous I/O 22 Write does not point to a valid I/O 23 register of the 82C311.

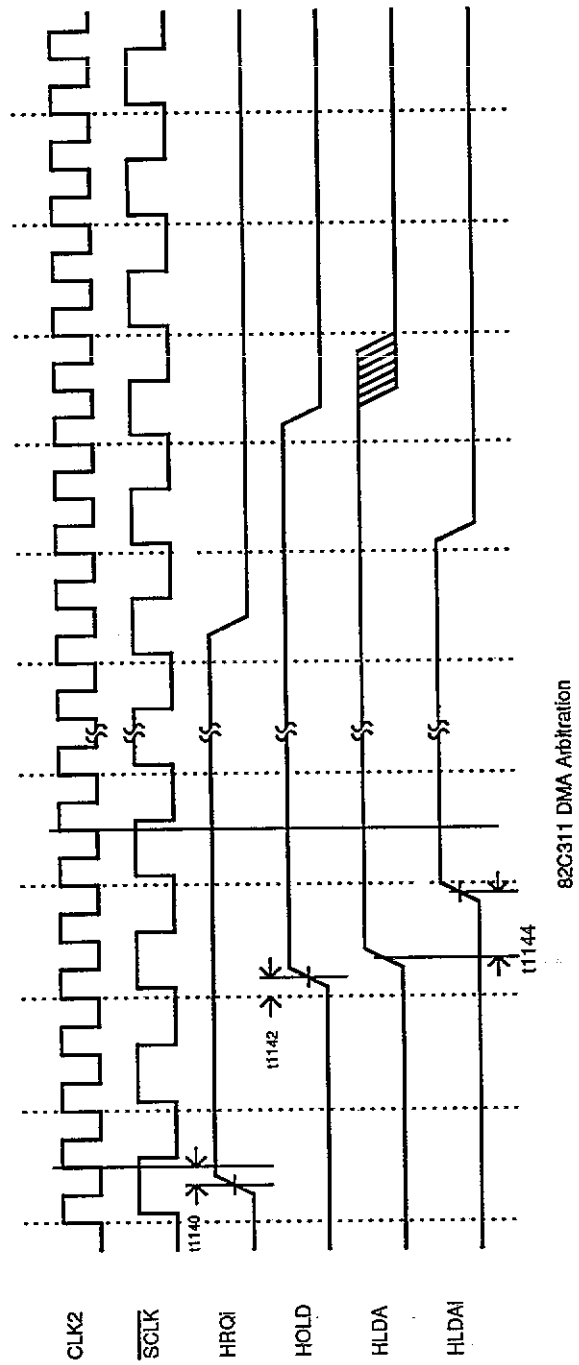
Figure 2-41. *82C311C DMA Cycle*



DMA Cycle 82C311 Rev.C

NOTE : $\overline{CRD}$ and $\overline{CWE}$ are generated during DMA Write Hit Cycles.
$\overline{CRD}$ is generated for chip select type SRAMs.
$\overline{AF32}$ is generated during DMA Cycle for 82C301 to generate the proper Action Code.

Figure 2-42. *82C311 DMA Arbitration*



82C311 Revision B

82C311 Revision B CPU/Cache/DRAM Controller is functionally identical to the 82C311 Revision C. 82C311 Revision B is referred to in this manual as 82C311B; and 82C311 Revision C is referred to as 82C311C.

82C311B works only up to 25 MHz and 82C311C operates up to 33 MHz. 82C311B is pin compatible to 82C311C. The cache, DRAM and DMA state machines are different compared to 82C311C. The timing diagrams for cache, DRAM and DMA cycles are included at the end of this section.

82C311B does not have index register 2F. The wait state definitions, RAS precharge, and RAS pulse width definitions in registers 11, 13, 15, and 17 are different compared to the 82C311C. The version register 04 contents are different.

The following table identifies the differences between 82C311B and 82C311C.

Table 2-73. *Feature Differences between 82C311B and C*

Feature	82C311B	82C311C
Wait states on DRAM cycles	2, 3, or 4 wait states	3, 4, or 5 wait states
RAS precharge for DRAM	2, 3, 4, or 5 CLK2 cycles	4, 6, or 8 CLK2 cycles
RAS pulse width during refresh cycles	4, 5, or 6 CLK2 cycles	4, 5, 6, or 7 CLK2 cycles
Posted write cycle for DRAM	Posted write cycle is always enabled	Posted write cycle can be enabled or disabled
Wait state for posted write cycle for DRAM	Zero wait state only	0 or 1 wait state
Wait state between back to back DRAM cycles	Zero wait state only	0 or 1 wait state option available
Page mode operation during Read/Miss cycle for 128K cache operation	Always non-page mode	Page mode or non-page mode option available
Fast GATEA20	Fast GATEA20 should be enabled through register 2B	Fast GATEA20 should be enabled using register 2F
Index registers 2FH	Absent	Present
Version register 04H content	40	80

82C311B Register Descriptions

Configuration Registers

There are 42 configuration and diagnostics registers in the 82C311. These are accessed through I/O ports 22H and 23H normally found in the interrupt controller. An indexing scheme is used to reduce the number of I/O addresses required to access all registers needed to configure and control the CHIPSet. Each access (either read or write) to an internal register is done by first writing its index into port 22. This index then controls the multiplexers gating the appropriate register data accessible as port 23H. Every access to port 23H must be preceded by writing the index value to port 22H even if the same data port is being accessed again. The ( ) in the bit description of any indicates the default value after power up.

The *82C311B* does not have index register *2FH*. *The definitions of index* registers 11, 13, 15, and 17 are different in 82C311B compared to 82C311C. The rest of the registers are identical between 82C311B and 82C311C. The registers mentioned here refer to 82C311 Revsion B.

This register defines the version numberof the 82C311B. bits 7:6 indicates the version number.

Table 2-74. Version Register

Index	Bits	Values and Functions
04H	7:6	Version number. 01 : version number for 82C311B
	5:0	Reserved (000000)

Table 2-75. *Name: Block 0 RAM Timing and RAS- Pulse Width During Refresh of all Banks(READ/WRITE)*

This register defines wait states, RAS precharge for block 0 and RAS pulse width for all banks

Index	Bits	Values and Functions
11H	7:6	DRAM wait state. 00 : 2 wait states. 01 : 3 wait states. (10): 4 wait states. 11 : Not used
	5	Reserved. Default value(0)
	4:3	RAS- precharge time. 00 : 2CLK2 cycles. 01 : 3CLK2 cycles. 10 : 4CLK2 cycles. (11): 5CLK2 cycles.
	2:1	Reserved. 00 : 4 CLK2 cycles. 01 : 4 CLK2 cycles. 10 : 5 CLK2 cycles. (11): 6 CLK2 cycles.
	0	Reserved. Default Value (0)
Default = 94		

Table 2-76. *Name: BLOCK 1RAM Timing (READ/WRITE)*

This register defines wait states, RAS precharge for block 1

Index	Bits	Values and Functions
13H	7:6	DRAM wait state 00 : 2 wait states. 01 : 3 wait states. (10): 4 wait states. 11 : Not used
	5	Reserved. Default value (0)
	4:3	RAS- precharge time. 00 : 2CLK2 cycles. 01 : 3CLK2 cycles 10 : 4CLK2 cycles (11): 5CLK2 cycles
	2:0	Reserved. Default value (0)
Default = 98H		

Table 2-77. *Name: BLOCK 2 RAM Timing (READ/WRITE)*

This register defines wait states, RAS precharge for block 2.

Index	Bits	Values and Functions
15H	7:6	DRAM wait state . 00 : 2 wait states. 01 : 3 wait states. (10): 4 wait states. 11 : Not used
	5	Reserved. Default value(0)
	4:3	RAS- precharge time. 00 : 2CLK2 cycles 01 : 3CLK2 cycles 10 : 4CLK2 cycles (11): 5CLK2 cycles
	2:0	Reserved. Default Value

Default = 98H

Table 2-78. *Name: BLOCK 3 RAM Timing (READ/WRITE)*

This register defines wait states, RAS precharge for block 3.

Index	Bits	Values and Functions
17H	7:6	DRAM wait state. 00 : 2 wait states. 01 : 3 wait states. (10): 4 wait states. 11 : Not used
	5	Reserved. Default value(0)
	4:3	RAS- precharge time. 00 : 2CLK2 cycles. 01 : 3CLK2 cycles. 10 : 4CLK2 cycles. (11): 5CLK2 cycles.
	2:0	Reserved. *BIOS should write a pattern 101*

Default = 98H

82C311B DC Characteristics

	Symbol	Min.	Max.	Units
Input low voltage	V_{IL}			
TTL level (all pins except RESET1)			.8	V
SHMT level (RESET1 pin)			1.0	V
Input high voltage	V_{IH}			
TTL level (all pins except RESET1 and CLK2)		2.0		V
CLK2 level		3.7		V
SHMT level (RESET1 pin)		4.0		V
Output low voltage	V_{OL}		.45	V
Output high voltage	V_{OH}			
All pins except IOCHRDY and NA- pins		2.4		V
IOCHRDY and NA- pins have open drain driver				
Input LOW current @ Vo = Vss CLK2, RESET4 and MA<7:0>	I_{IL}		-10	
All input and I/O pins except CLK2, RESET4 and MA<7:0>		-90	-10	µA
Input HIGH current @Vo = Vdd CLK2 RESET4 and MA<7:0>	I_{IH}		10	
All input and I/O pins except CLK2, RESET4 and MA<7:0>			40	µA
3-state output OFF current LOW	I_{OZL}		-10	µA
3-state output OFF current HIGH	I_{OZH}		10	µA
Output leakage current	I_{OH}			
Output short circuit current	I_{OS}			
Power supply current @ 25 MHz	I_{CC}		200	mA
Input capacitance	C_{IN}			
Output or I/O capacitance	C_{OUT}			

82C311B AC Characteristics

All timing parameters are specified under capacitive load of 50 pf and temperature of 70 degree C. All the units discussed in the following timing tables are in nanoseconds, unless otherwise specified. Also, the AC specifications mentioned in this document are subject to change.

Table 2-79. Memory Cycle

	Memory Cycle	25 MHz	
		Min.	Max.
t101	Operating frequency	8	25 MHz
t102	CLK2 period	20	
t103	CLK2 high time at 2V	7	
t104	CLK2 high time at Vcc-0.8V	4	
t105	CLK2 low time at 2V	7	
t106	CLK2 low time at 0.8V	5	
t107	CLK2 fall time(Vcc-0.8 to 0.8V)	7	
t108	CLK2 rise time(0.8V to Vcc-0.8V)	7	
t120	Address setup to CLK2 low	18	
t126	MALE- active from CLK2 high	0	15
t127	MALE- inactive from CLK2 low	0	15
t130	CRD<1:0>- active delay from CLK2 low 0WS read hit cycles	0	11
t131	CRD<1:0>- active delay from CLK2 low for all other cycles	0	20
t132	CRD<1:0>- active delay from CLK2 high (for 1 ws read hits)	0	28
t133	CRD<1:0>- inactive delay from CLK2 high	0	20
t134	READY- active delay from CLK2 low	4	19
t135	READY- inactive delay from CLK2 high	4	19
t136	CALE- high to low delay from CLK2 low	0	25
t137	CALE- high to low delay from CLK2 high	0	25
t138	CALE- inactive from CLK2 high	0	25
t141	RAS- active delay from CLK2 low	0	28
t142	RAS- active delay from CLK2 high	9	24
t143	RAS- inactive delay from CLK2 high	2	24
t144	RAS- inactive delay from CLK2 low	2	26
t145	Row address set up time from CPU address active	0	33
t146	Row address hold time from CLK2 low	7	25
t147	Column address valid to CAS- active	7	
t149	CAS- active delay from CLK2 low	5	25

Table 2-79. Memory Cycle (continued)

	Memory Cycle	25 MHz	
		Min.	Max.
t150	CAS- active delay from CLK2 high	0	40
t151	CAS- incative delay from CLK2 high	5	25
t152	DRD- active delay from CLK2 low(0 ws)	0	25
t153	DRD- active delay from CLK2 high(1 ws)	0	25
t154	DRD- inactive delay from CLK2 low	0	25
t155	FBE- active delay from CLK2 low(0 ws)	0	25
t156	FBE- active delay from CLK2 high(1 ws)	0	25
t157	FBE- inactive delay from CLK2 low	0	25
t158	CWE- active delay from CLK2 low	0	25
t159	CWE- active delay from CLK2 high	0	25
t160	CWE- inactive delay fromCLK2 high	0	16
t161	DWE- active delay from CLK2 low	0	25
t162	DWE- inactive delay from CLK2 high	0	25
t163	LDBCAB low to high delay from CLK2 high	0	13
t164	LDBCAB high to low delay from CLK2 high	0	25
t165	LDBDIR valid from CLK2 low	0	26
t166	Row address hold time from RAS active	9	
t167	BWBUSY active delay from CLK2 low	0	30
t167a	BWBUSY inactive delay from CLK2 high	0	30
t168	BST128K active delay from CLK2 low	0	30
t168a	BST128Kinactive delay from CLK2 low	0	30

Table 2-80. DMA Cycle

	DMA Cycle	25 MHz		
		Min.	Type	Max.
t170	Command setup time to CLK2 high	10		
t171	RAS- active delay from CLK2 high	0		20
t172	RAS- inactive delay from commands inactive	0		30
t173	Row address delay from address valid			20
t174	Row address hold time from CLK2 high	10		20
t175	Column address setup to CAS- active		1CLK2	
t176	Column address hold time from commands inactive	10		40
t177	CAS- active delay from RAS- active for DMA memory read cycle		2CLK2	
t178	CAS- active delay from RAS- active for DMA memory write cycle		3CLK2	
t179	CAS- active delay from CLK2 high	8		20
t180	CAS- inactive delay from commands inactive	8		20
t183	DRD- active delay from CLK2 high	5		20
t184	DRD- inactive delay from commands inactive	5		20

Table 2-80. DMA Cycle (continued)

	DMA Cycle	25 MHz		
		Min.	Type	Max.
t185	AF32- active delay from command active	0		20
t186	AF32- inactive delay from command inactive	0		15
t187	DWE- active delay from CLK2 high	0		17
t188	DWE- inactive delay from commands inactive	0		17
t189	CRD- and CWE- active delay from CLK2 high	0		20
t190	CRD- and CWE- inactive delay from CLK2 high	10		25

Table 2-81. ROM Cycle

	ROM Cycle	25 MHz		
		Min.	Type	Max.
t191	ROMCS- active delay from CLK2 high	0		28
t192	ROMCS- inactive delay from CLK2 high	0		25
t193	READY- input setup time to CLK2 high	15		
t194	READY- input hold time from CLK2 high	5		

Table 2-82. AT Bus Access

	AT Bus Access	25 MHz		
		Min.	Type	Max.
t1100	ATEN- active from CLK2 high	0		22
t1101	ATEN- inactive from CLK2 high	0		22
t1102	BALE active from BUSCLK low	10		20
t1103	BALE inactive from BUSCLK high	10		20
t1104	Command active delay from BUSCLK low	10		20
t1105	Command inactive from BUSCLK high	10		20
t1106	ACEN- active delay from BUSCLK low (read)	10		20
t1107	ACEN- inactive delay from BUSCLK high	10		20
t1108	AC<3:0> active delay from BUSCLK low	10		20
t1110	IOCHRDY setup to BUSCLK low	10		
t1111	IOCHRDY hold from BUSCLK low	5		
t1112	MCS16-,IOCS16- setup to BUSCLK high	20		
t1114	MCS32-,IOCS32- setup from BUSCLK high	20		
t1116	Command active delay from BUSCLK high (write or 0WS)	10		20
t1117	ACEN- active delay from BUSCLK high (write)	10		25
t1118	ACEN- inactive delay from BUSCLK high (write)	10		25
t1119	0WS- setup to BUSCLK low	20		
t1120	0WS- hold time from BUSCLK low	20		
t1123	XA<1:0>, SBHE- valid delay from BUSCLK low	0		18
t1124	XA<1:0>, SBHE invalid delay from BUSCLK low	0		18

Table 2-83. *DMA Arbitration*

	DMA Arbitration	25 MHz Min.	25 MHz Max.
1140	HRQn active setup to CLK2 high	15	
t1142	HOLD active delay from CLK2 high	2	25
t1144	HLDAn active delay from HLDA	0	19

Table 2-84. *REFRESH Arbitration*

	REFRESH Arbitration	25 MHz Min.	25 MHz Max.
t1150	MEMR- delay from BUSCLK high	0	25

Table 2-85. *RESET Timing*

	RESET Timing	25 MHz Min.	25 MHz Type	25 MHz Max.
t1170	RESET3 active delay from CLK2	0		25
t1171	RESET3 inactive delay from CLK2 high	2		15
t1172	RESET3 pulse width		78CLK2	
t1173	RESET4 active delay from CLK2 high	0		25
t1174	RESET4 inactive delay from CLK2 high	2		25
t1175	RESET4 active from RESET1- active		4CLK2	
t1176	RESET3 active from RESET1- inactive		2CLK2	

Table 2-86. *Miscellaneous*

	Miscellaneous	25 MHz Min.	25 MHz Max.
t1185	BUSCLK low delay from BCLK high	0	22
t1186	BUSCLK high delay from BCLK high	0	22
t1187	BUSCLK high pulse width		140
t1188	BUSCLK low pulse width		140
t1189	BUSCLK rise time		6
t1190	BUSCLK low time		6
t1191	FGA20 valid from IOW-		18
t1192	PEN valid from IOW- high		18
t1193	A20 delay from CPUA20	0	7

Table 2-87. REFRESH Cycle

REFRESH Cycle		25 MHz		
		Min.	Typical	Max.
t1200	RASi- active delay from CLK2 high	0		25
t1201	RASi- inactive delay from CLK2 high	0		25
t1202	RASi pulse width		4CLK2	
t1203	RAS(i+1) active delay RASi active		1CLK2	
t1204	REFERSH address setup time to RAS0		2CLK2	
t1205	REFERSH address hold from RAS		2CLK2	

Table 2-88. I/O Cycle

I/O Cycle		25 MHz	
		Min.	Max.
t1214	XDEN- active delay from XIOR- or XIOW-	15	26
t1215	XDEN- inactive delay from XIOR- or XIOW-	12	25
t1218	XDA output valid delay to XIOR-	0	30
t1219	XDA output hold time to XIOR-	0	30

Table 2-89. LPAR Timing

LPAR Timing		25 MHz	
		Min.	Max.
t1220	LPAR- input setup time to CAS-	10	

Note: The parameters t158 and t160 tracks so that the write pulse width for SRAM is met. The tracking requirement is T158-T160 should be greater than -2 and less than 8ns.

The New tracking parameters are

1. t160 - t151 < 6ns
2. t138 - t160 > 1ns
3. t158 - t160 < 8ns
4. t141 - t144 < 5ns

82C311B Timing Diagrams

Figure 2-43. *82C311B and 80386 Interface*

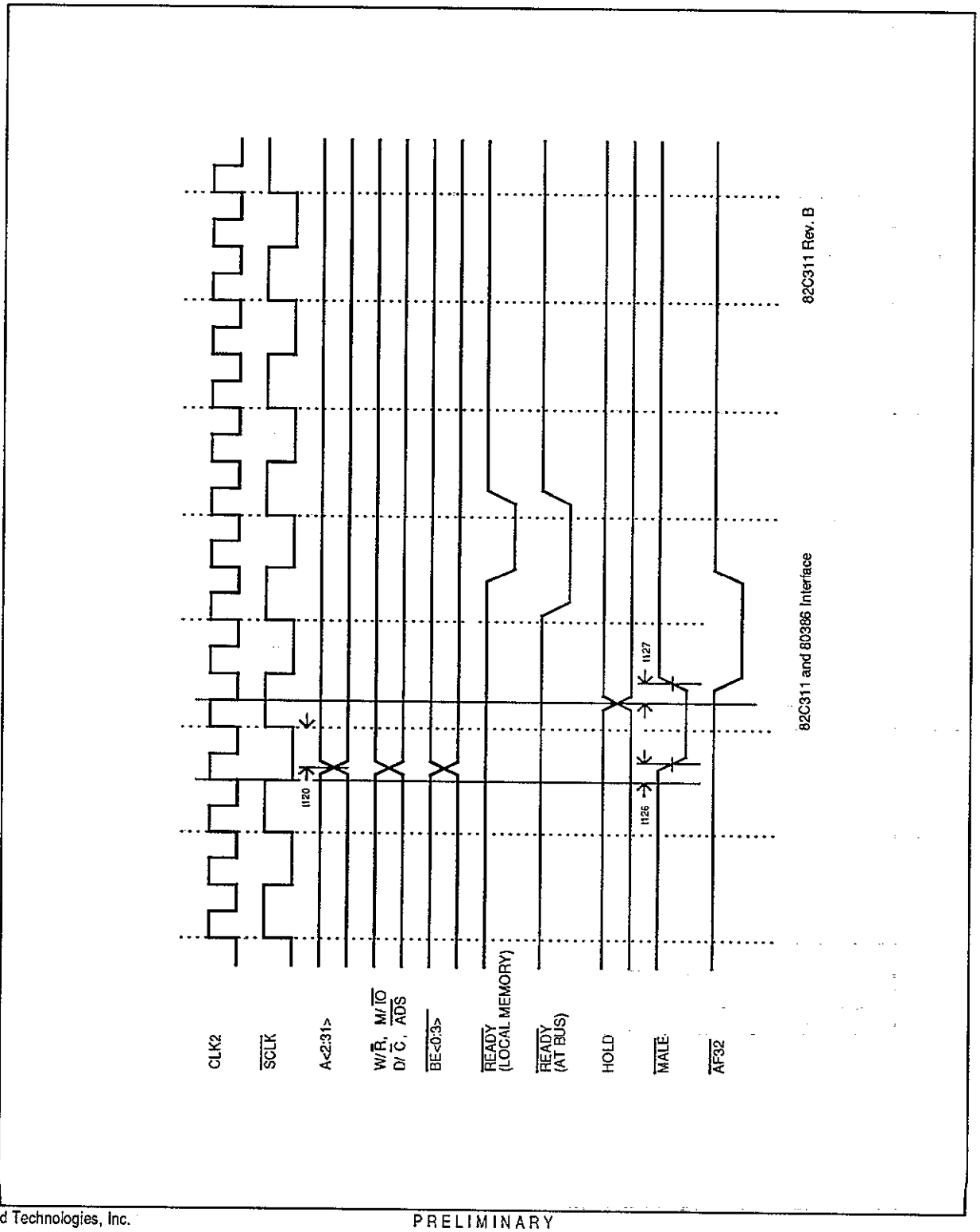
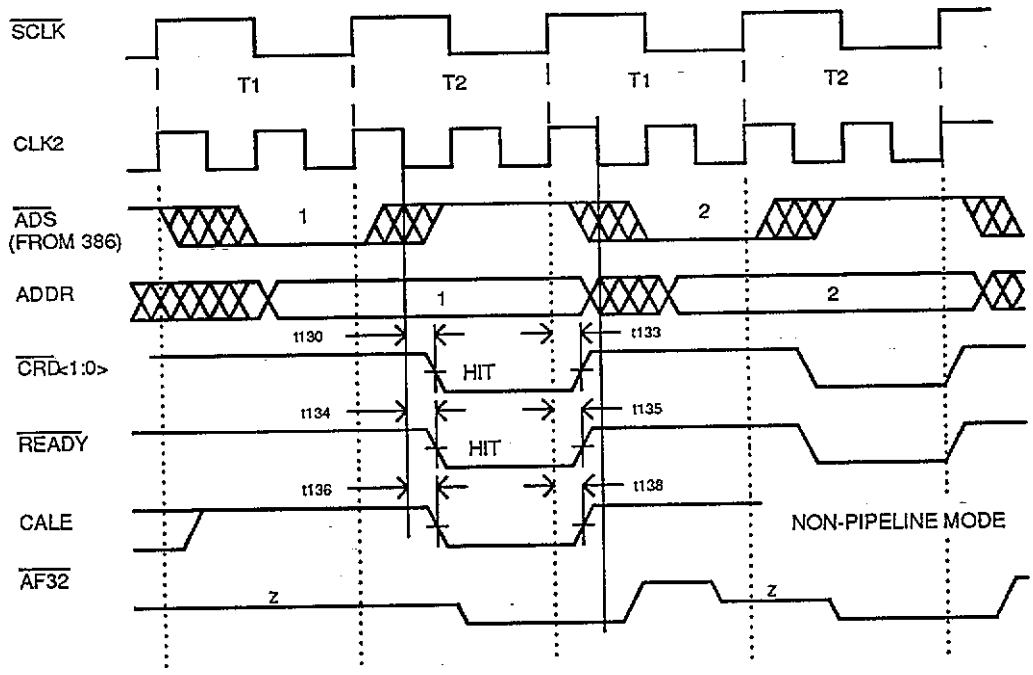
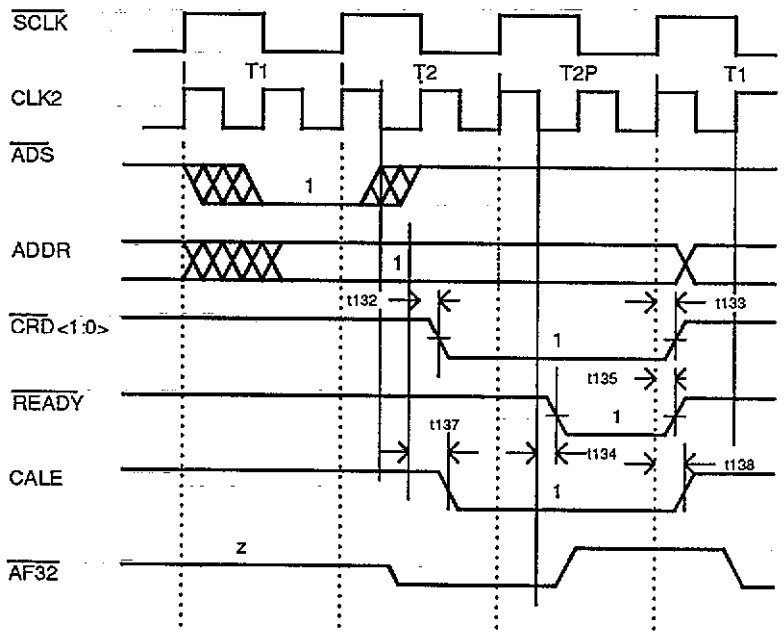


Figure 2-44. *82C311B Read Hit Cycle, 0 WS SRAM*



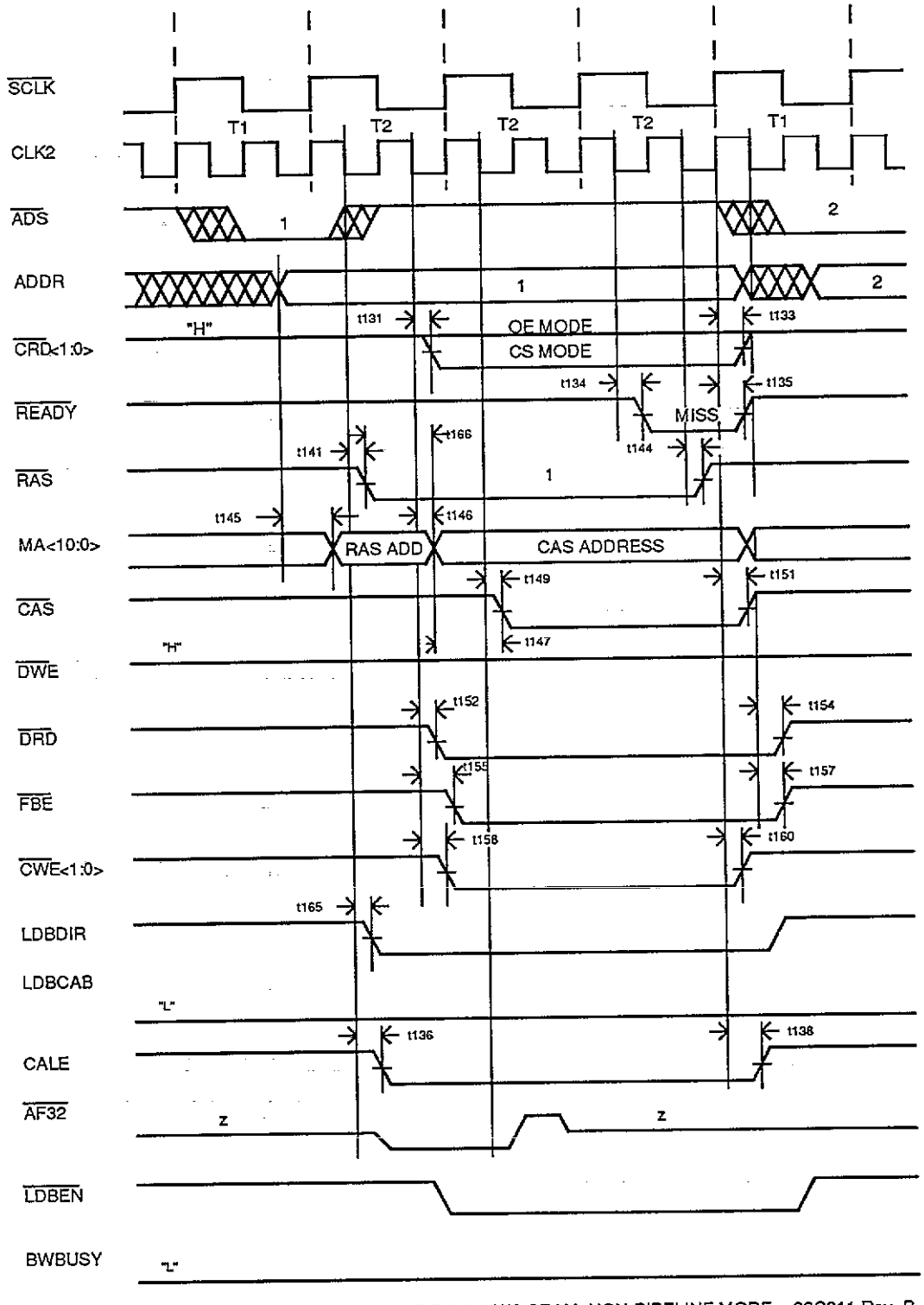
READ HIT CYCLE, 0 WS SRAM, NON-PIPELINE MODE 82C311 Rev. B

Figure 2-45. *82C311B Read Hit Cycle, 1 WS SRAM*



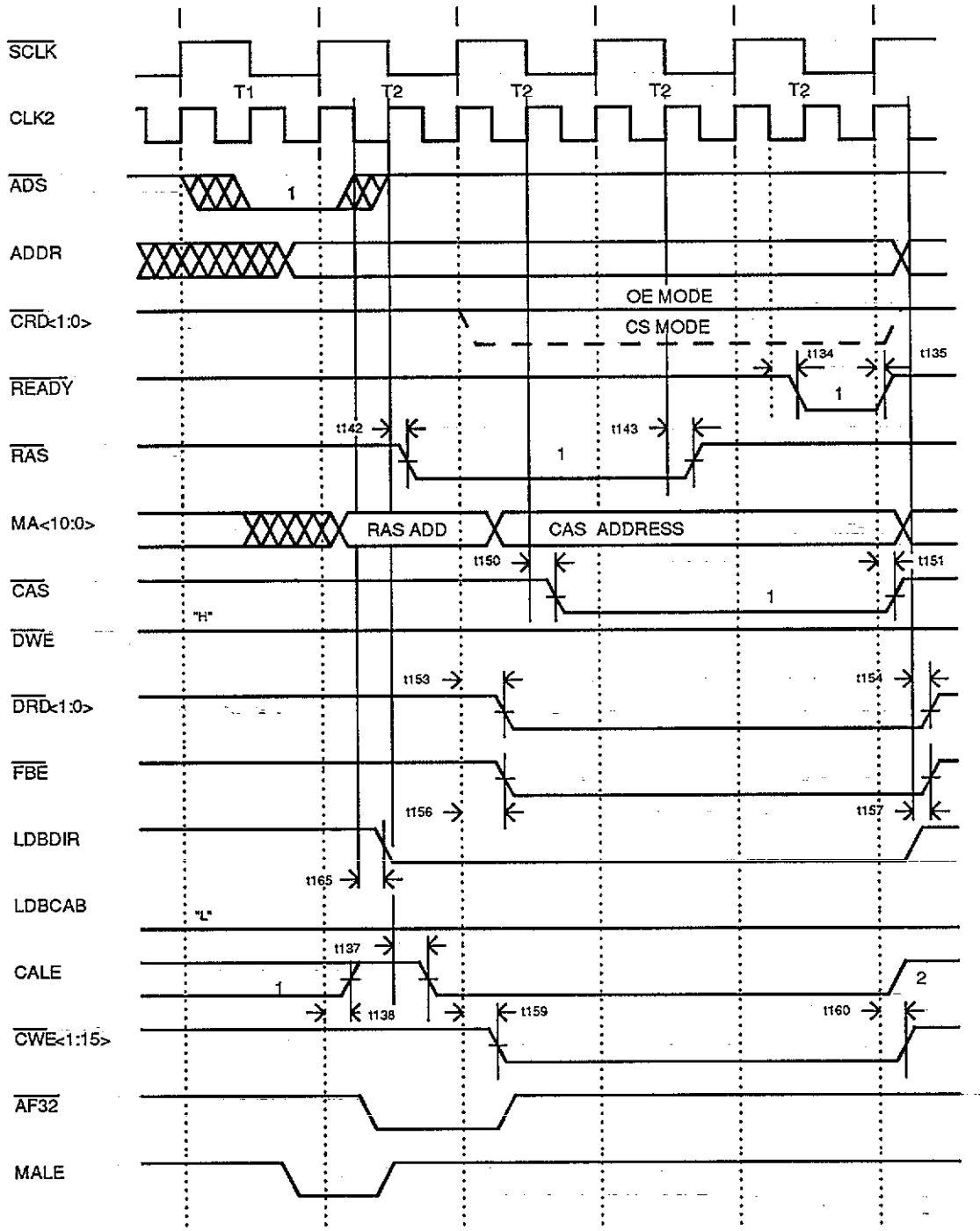
READ HIT CYCLE, 1WS NON-PIPELINED 82C311 Rev. B

Figure 2-46. *82C311B Read Miss Cycle, 2 WS DRAM, 0 WS SRAM*



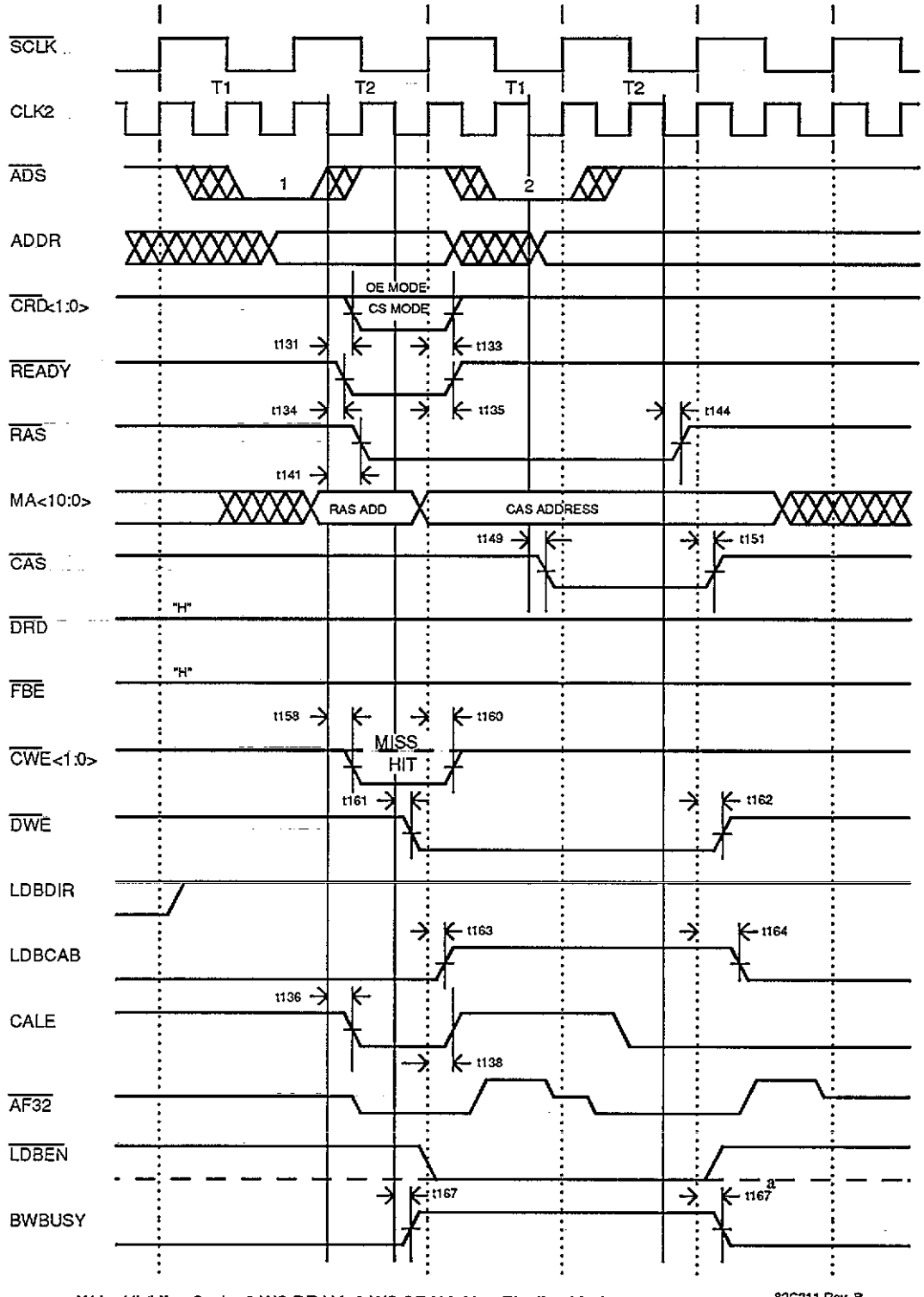
READ MISS CYCLE, 2 WS DRAM, 0 WS SRAM, NON-PIPELINE MODE 82C311 Rev. B

Figure 2-47. *82C311B Read Miss Cycle, 2 WS DRAM, 1 WS SRAM*



Read Miss Cycle, 2 WS DRAM, 1 WS SRAM, Non-Pipeline 82C311 Rev. B

Figure 2-48. 82C311B Write Hit/Miss Cycle, 2 WS DRAM, 0 WS SRAM



Write Hit/Miss Cycle, 2 WS DRAM, 0 WS SRAM, Non-Pipeline Mode

82C311 Rev. B

NOTE : $\overline{CRD}$ and $\overline{CWE}$ signals are not generated during the Write Miss Cycles.
$\overline{CRD}$ is only generated for the chip select type of SRAMs during the Write Hit Cycles.

Figure 2-49. 82C311B 128K Cache Read Miss Cycle

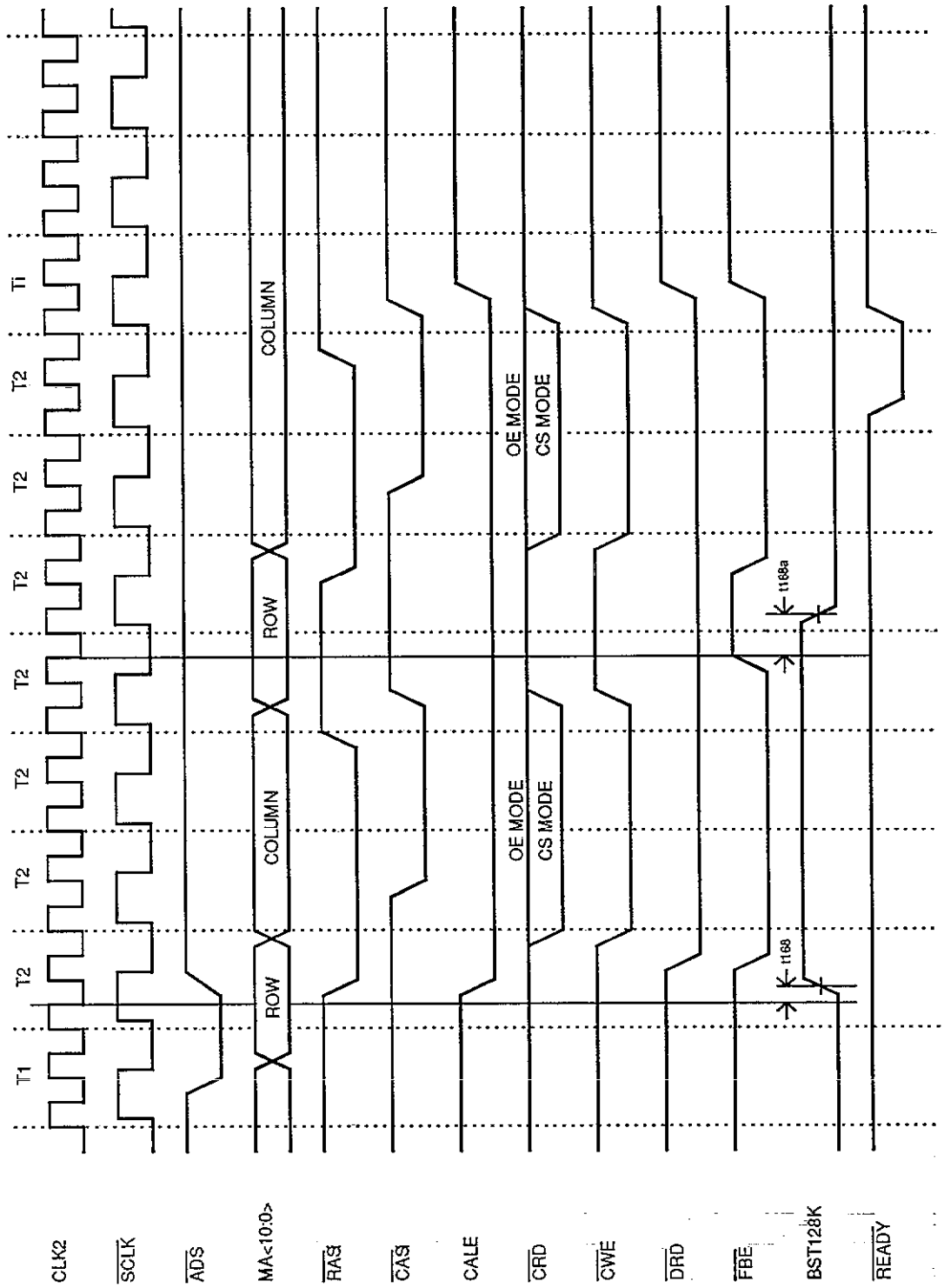
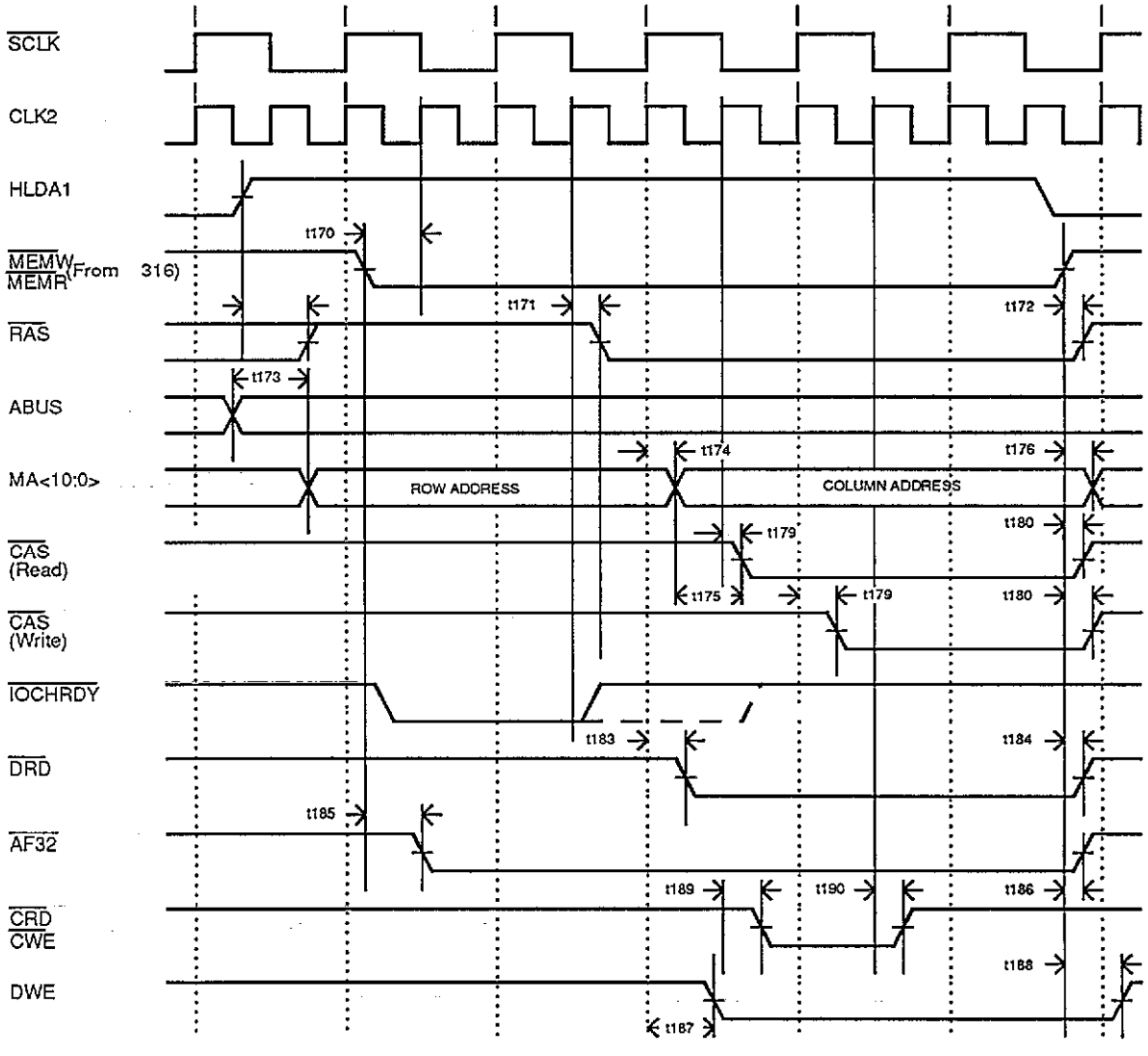


Figure 2-50. *82C311B DMA Cycle*



DMA Cycle 82C311 Rev. B

NOTE : $\overline{CRD}$ and $\overline{CWE}$ are generated during DMA Write Hit Cycles.
$\overline{CRD}$ is generated for chip select type SRAMs.
$\overline{AF32}$ is generated during DMA Cycle for 82C301 to generate the proper Action Code.

Figure 2-51. *82C311 Pin Diagram (Revision B and C)*

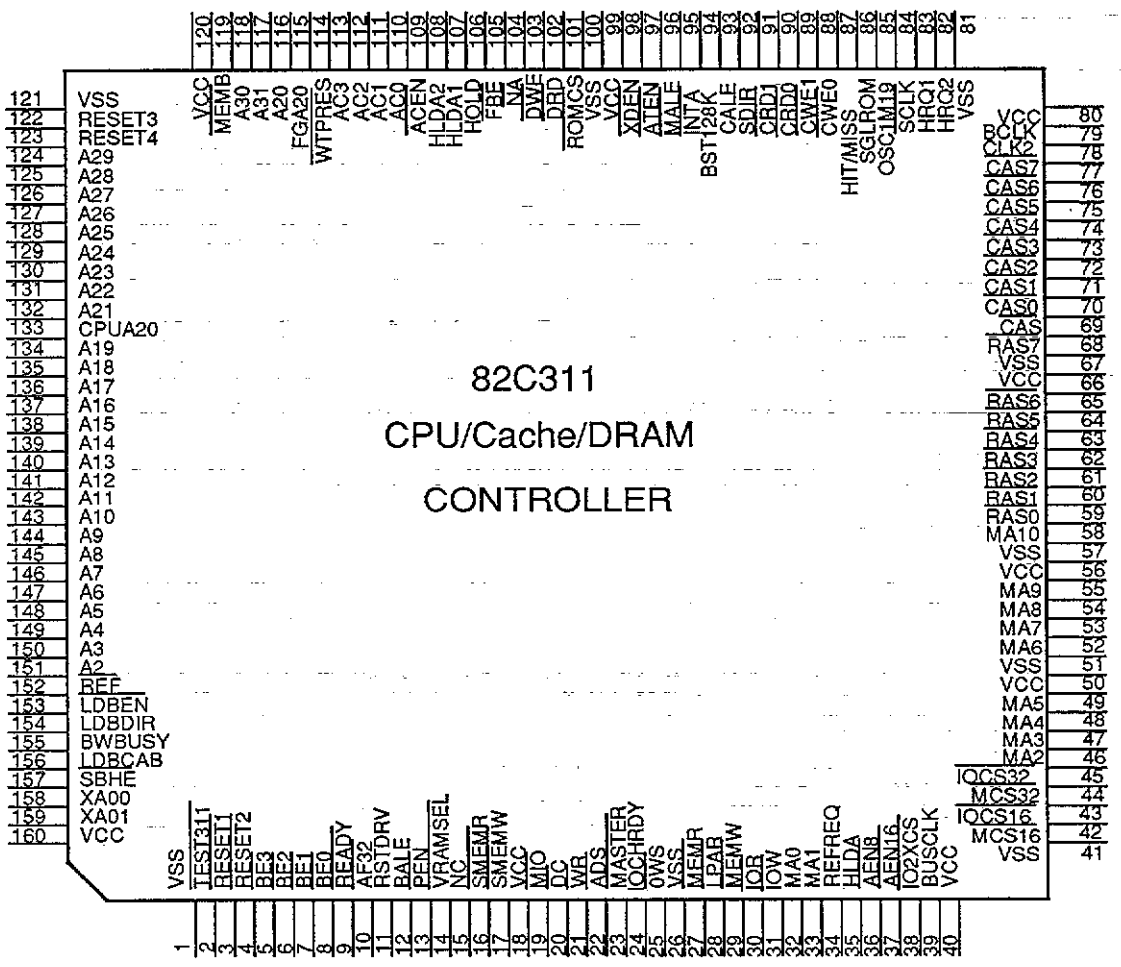
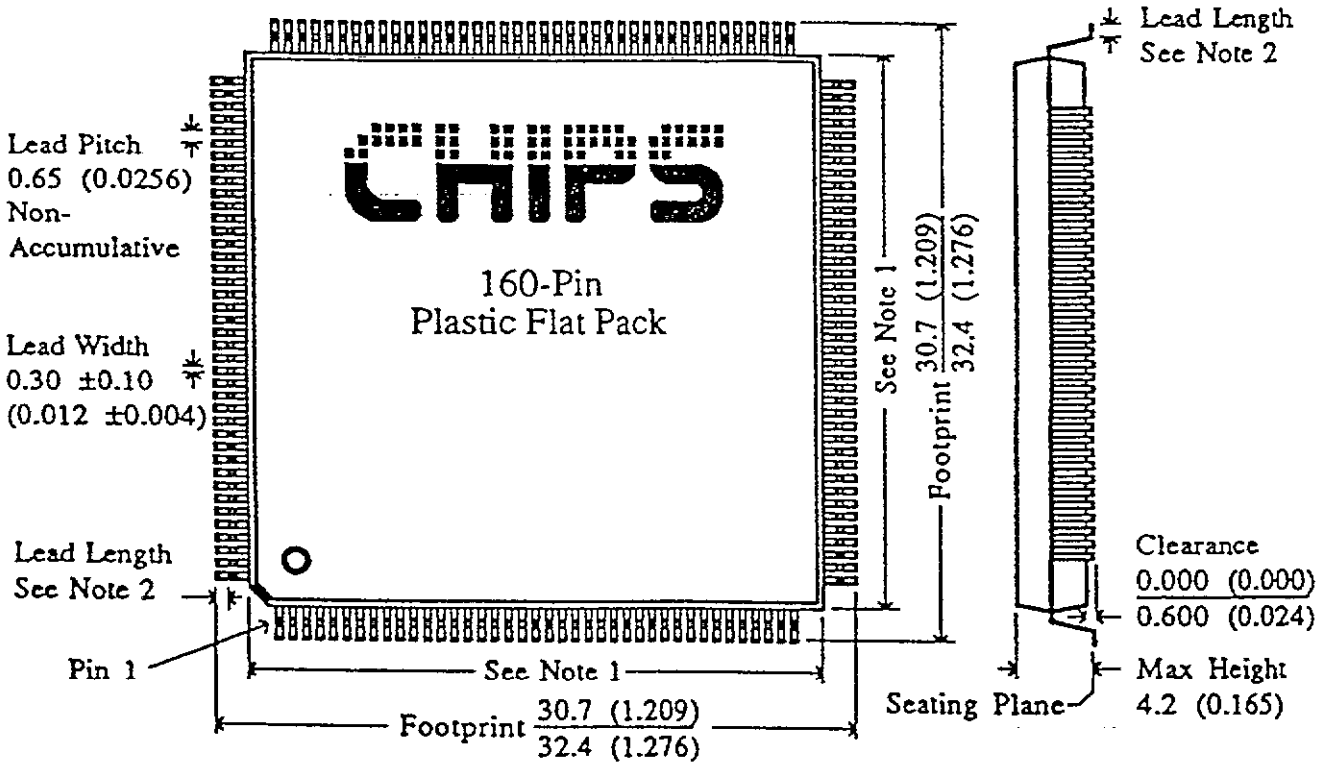


Figure 2-52. 82C311 Mechanical Dimensions (Revision B and C)

DIMENSIONS: mm (in)



Note 1: Package Body Size = 28 +0.2/-0.4 (1.102 +0.008/-0.016) (Swire)
Package Body Size = 28 ±0.2 (1.102 ±0.008) (All Other Package Vendors)

Note 2: Lead Length = 0.6 ±0.3 (0.024 ±0.012) (Package Vendor = Seiko)
Lead Length = 0.7 ±0.2 (0.028 ±0.008) (Package Vendor = Yamaha)
Lead Length = 0.8 ±0.2 (0.031 ±0.008) (All Other Package Vendors)

Section 3

82C315 Bus Controller

Features

The 82C315 provides all the logic required to interface with the memory data bus (MD<0:31>), system data bus (SD<0:15>), and peripheral data bus (XD<0:15>), and also does data alignment and size conversion. The 82C315 also provides parity detection and generation logic, clock selection logic, and the 80387 and Wietek coprocessor interface logic.

Functional Description

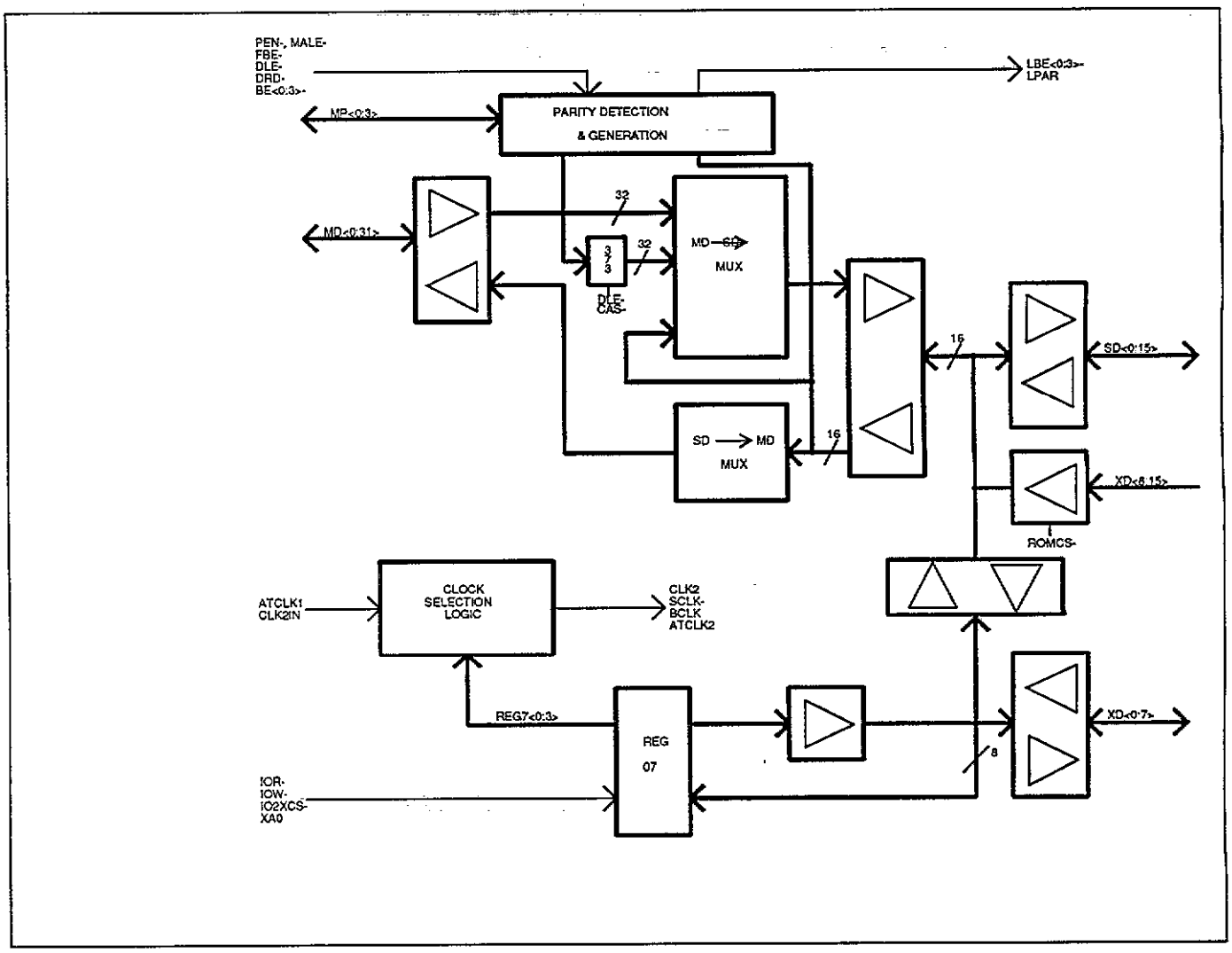
The 82C315 Bus Controller consists of the following functional subsystems as illustrated in Figure 3-1:

- Bus interface between MD, SD, and XD
- Data conversion
- Clock selection logic
- Parity detection and generation logic
- 80387/Weitek coprocessor interface logic
- 14.318 MHz oscillator circuit and divide by 12 counter
- Byte enable latches
- Configuration register

Bus Interface

The 82C315 controls the direction of the data flow between the MD, SD, and XD buses according to the signals HLDA1, ATEN-, SDIR, DRD-, XDIR, XDIR1, ROMCS-, and AEN. The first group of signals: HLDA1, ATEN-, SDIR, and DRD-, control the direction of the buffers between the MD and SD buses and the cycle type as shown in Table 3-1. The second group of the signals: XDIR, XDIR1, ROMCS, and AEN, control the direction of data flow between the SD and the XD buses as shown in Figure 3-2.

Figure 3-1. *82C315 Functional Block Diagram*

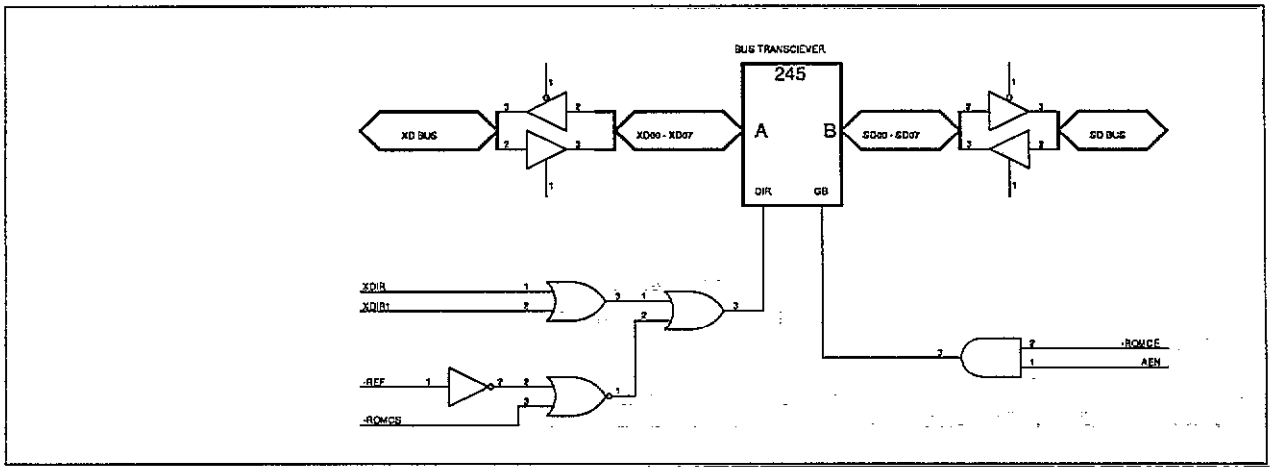


Data Conversion

Table 3-1. *Bus Control Definition*

HLDA	ATEN-	SDIR	DRD-	Cycle Type	Source	Dest
0	0	0	-	CPU AT Read	SD	MD
0	0	1	-	CPU AT Write	MD	SD
1	1	1	0	Master/DMA Loc Mem Read	MD	SD
1	1	0	1	Master/DMA Loc Mem Write	SD	MD

Figure 3-2. *Direction of Data Flow Between SD and XD Buses*



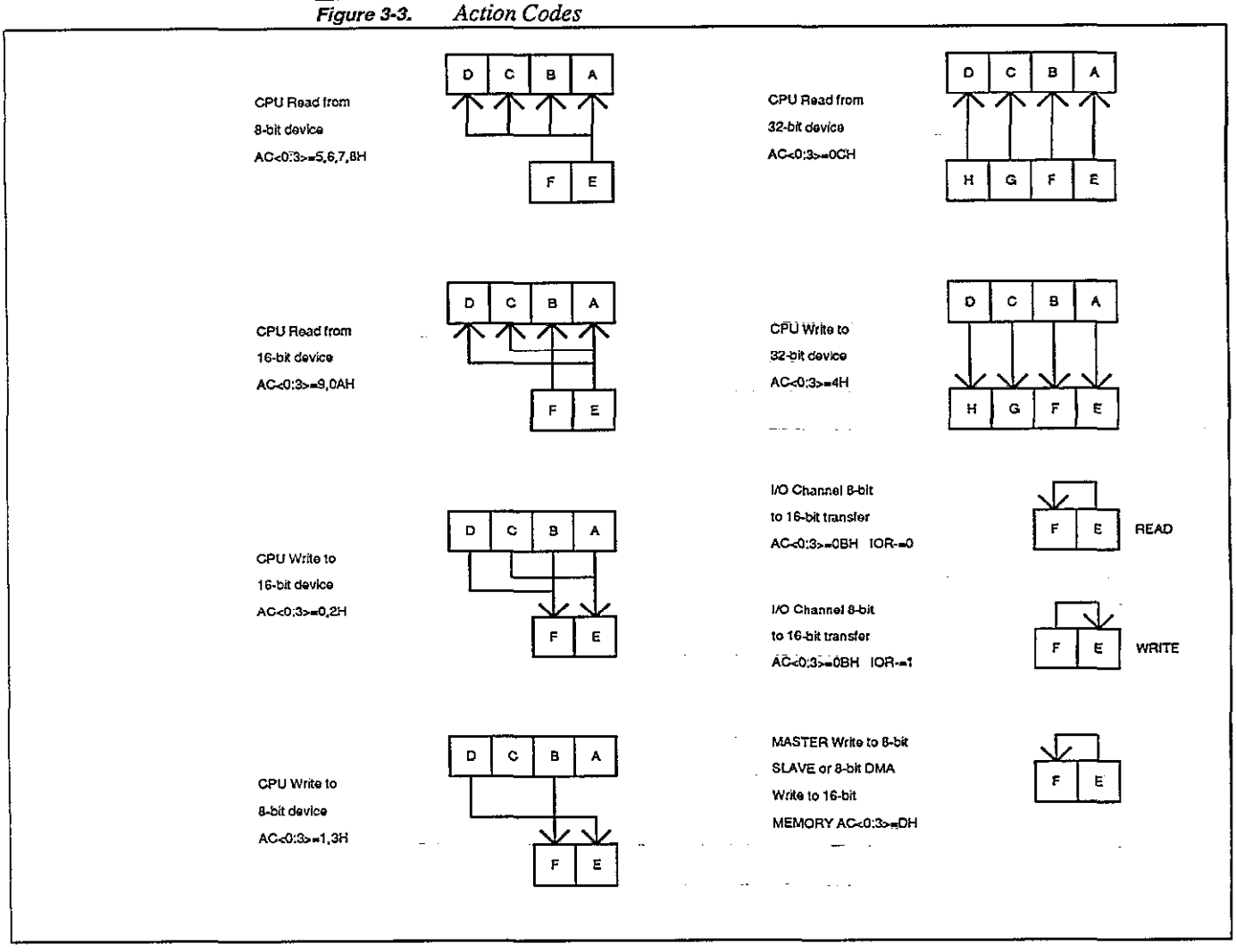
The 82C315 provides all the data connections between the MD, SD, and XD buses; as well as proper data conversions for the CPU initiated accesses to the AT bus. The action codes (AC<0:3>) are used to control the flow of data between the 32-bit MD data bus, the 16-bit SD data bus, and the 16-bit XD data bus. The action codes are generated by the 82C311 according to the signals MCS16-, IOCS16-, MCS32-, and IOCS32-. The action codes are generated to control the CPU accesses to the AT bus and is qualified by the ACEN-. The action codes are defined in Table 3-2 and shown graphically in Figure 3-3.

Table 3-2. *Action Code Definition*

AC<0:3>	FROM	TO
0	AB	EF
1	B	EF
2	CD	EF
3	D	EF
4	ABCD	EFGH
5	E	A
6	E	B
7	E	C
8	E	D
9	EF	AB
A	EF	CD
B	E	F
B	F	E
C	EFGH	ABCD
D	E	F

IOR = 0
IOR-1 = 1

Figure 3-3. Action Codes



Note A, B, C, and D are CPU bytes with A being the Least Significant Byte, and D being the Most Significant Byte.
E, F, G, and H are 4 AT bus bytes with E being the Least Significant Byle and H being the Most Significant Byte.

Clock Selection Logic

The 82C315 provides a flexible clock selection scheme (shown in Figure 3-4). It has two inputs: CLK2IN and ATCLK1. CLK2IN is driven from a packaged CMOS crystal oscillator circuit, running at twice the processor rated CPU frequency. An oscillator circuit is provided for the ATCLK1 signal, so that it can be connected to either a packaged CMOS oscillator or a parallel resonant crystal. Figure 3-5 shows a crystal oscillator circuit for ATCLK. Typically, the ATCLK1 should be of a lower frequency than the CLK2IN.

The 82C315 generates CLK2, SCLK-, and BCLK. The processor clock (CLK2), is for driving the 80386 processor; as well as the 82C311 CPU state machine. SCLK- is CLK2 divided by two and is 180 degrees out of phase with

Figure 3-4. *Clock Selection Logic*

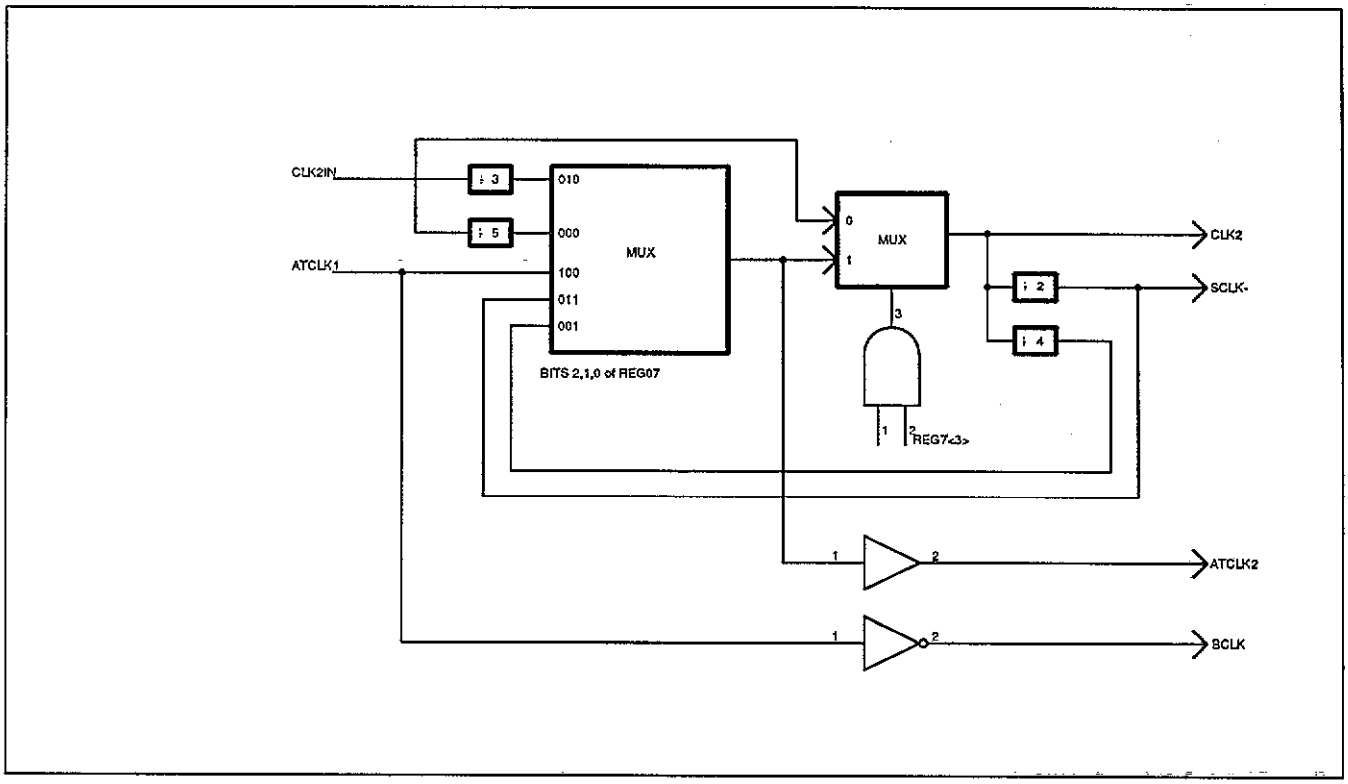
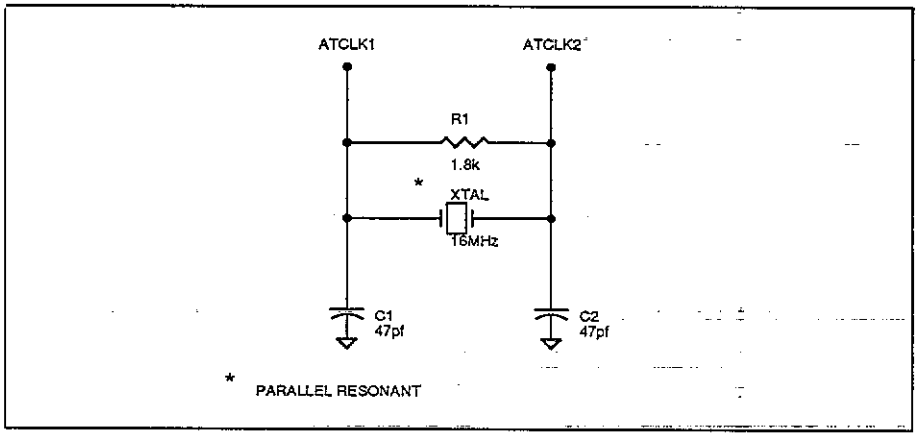


Figure 3-5. *Crystal Oscillator for ATCLK*



the internal SCLK of the 80386. BCLK is used to drive the 82C311 AT bus state machine.

CLK2 can be derived from CLK2IN or from ATCLK1. In the synchronous mode, both CLK2 and BCLK are derived from CLK2IN, so the processor state machine and the AT bus state machine run synchronously. In the asynchronous mode, BCLK is generated from ATCLK1 and CLK2 is generated from CLK2IN or ATCLK1.

In this case, the processor state machine and the AT state machine run asynchronous to each other. The processor and bus clock selections are determined by REG7<0:3>.

Under normal operation, CLK2IN should be selected as the processor clock (CLK2) to allow the processor to operate at the maximum rated speed. BCLK can either be a sub-division of CLK2IN (1/2, 1/3, 1/4, or 1/5) or derived from ATCLK1. ATCLK1 may be selected to generate CLK2 only when it is desired to slow down the processor for timing dependent code execution. Once the options for the clock selections are set, the clock switching occurs with a clean transition in the synchronous or asynchronous mode. During clock switching, no phase of CLK2 is less than the minimum value, or greater than the maximum value specified for the 80386 CPU.

Possible clock selections are shown in Table 3-3. Examples of BCLK and CLK2 and SCLK- derived from CLK2IN are shown in Table 3-4.

Parity Detection and Generation Logic

Table 3-3. Clock Selection Options

REG7<0:3>	BCLK	CLK2
0000	1/5 CLK2IN	CLK2IN
0001	1/4 CLK2IN	CLK2IN
0010	1/3 CLK2IN	CLK2IN
0011	1/2 CLK2IN	CLK2IN
0100	ATCLK	CLK2IN
1100	ATCLK	ATCLK

Table 3-4. Examples of Clock Selection

REG7<0:3>	CLK2IN	ATCLK	Mode	CLK2	SCLK-	BCLK
0100	50 MHz	16 MHz	ASYNC	50	25	16
0010	50 MHz	-	SYNC	50	25	16.6
0001	66 MHz	-	SYNC	66	33	16.5
0000	80 MHz	-	SYNC	80	40	16

The 82C315 provides the logic required to generate parity bits (one parity bit per byte) during the memory write cycles. It also detects and generates parity errors during local memory read cycles.

During a local memory write cycle, the data is presented to the parity logic through the MD bus. Write parity bits for each byte is generated and propagated onto the memory parity bus (MP<0:3>) which is directly connected to the DRAMs. Then, the parity bits on the MP bus along with the write data on the MD bus are strobed into the DRAMs.

During the local memory read cycle, the data (32 bits) and the parity bits (4 bits) are read from the DRAMs onto the MD and MP bus, respectively. These buses are latched internally so they stay valid during parity checking. The parity generation logic uses the data on the MD bus to generate the correct parity bits and compares them against the data on the MP bus. The results of the byte wise comparison are further gated by the latched byte enables (LBE<0:3>-) to ignore errors for bytes which are not valid. The OR'ed byte-wise parity error is then latched as the output latched parity error (LPAR-) if parity enable (PEN-) input is asserted. Figure 3-6 shows the logic for parity detection and generation, and Table 3-5 shows the buses involved for different cycles.

Figure 3-6. *Parity Detection and Generation Logic*

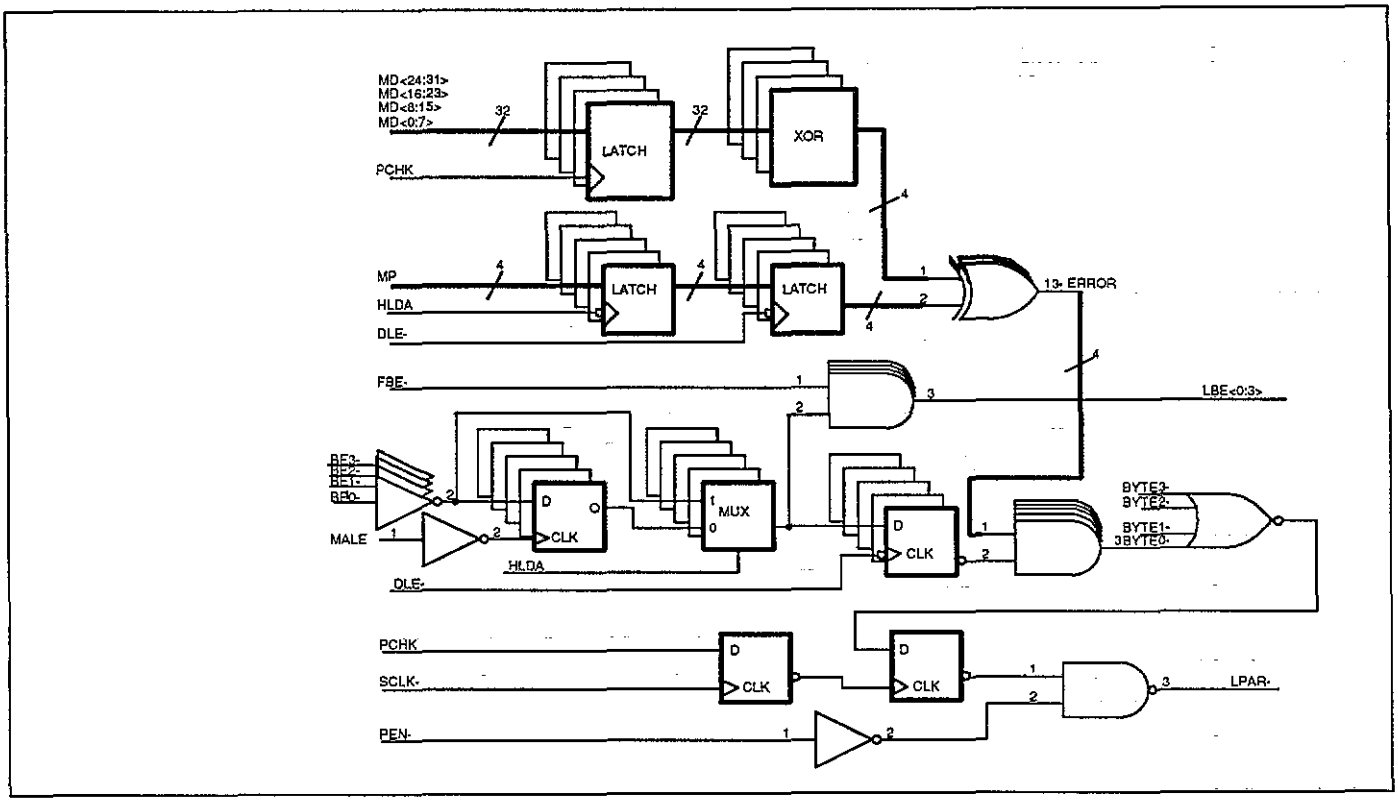


Table 3-5. Parity Detection/Generation

Cycle Type	From	To	Gen/Det	Data Source
Non-AT Read	MD	D	Detection	MD
Non-AT Write	D	MD	Generation	MD
Master/DMA Mem Read	MD	SD	Detection	MD
Master/DMA Mem Write	SD	MD	Generation	SD

80387/WEITEK Coprocessor Interface

The 82C315, in conjunction with 82C311 and 82C316, provides all the control logic required to interface with the 80387 or 3167 WEITEK coprocessor. It provides signals BUSY386-, ERR386-, PRQ386, and IRQ386 derived from PRQ387, 387ERR-, 387BUSY-, INTCLR, WTPRES-, and WTINTR to interface with the 80387 or WEITEK coprocessors.

The 82C315, after reset, monitors the 80387 error (387ERR-) input for the presence of an 80387 in the system and generates the 80387 present (387PRES) output. If the 80387 is present and the current cycle is an 80387 cycle (decoded by 82C311), the 82C311 generates an AF32- to set the current cycle into the non-AT cycle and generates READY- upon completion of the cycle.

During the reset, the 80387 error (ERR387-) input is allowed to propagate through the 82C315 to become ERR386- output to the 80386 for proper recognition of 80387 by the 80386. Any other 387ERR- thereafter will not be presented to the CPU; however, they will cause the busy signal to the coprocessor to be held in the busy state and generate IRQ386.

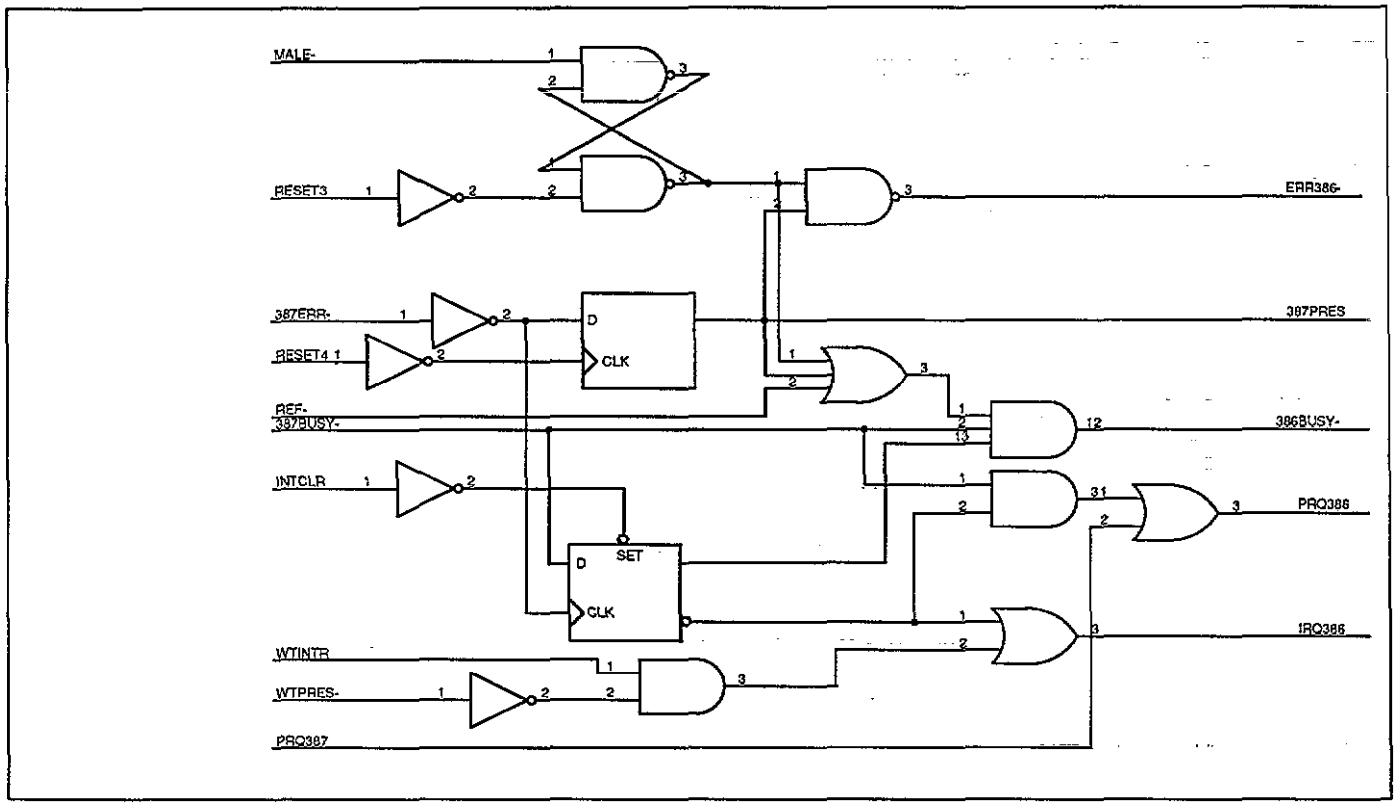
If an unmasked exception occurs during a coprocessor cycle, the coprocessor sets its error signal (ERROR-). The 82C315, upon receiving the 80387 error (387ERR-) input, latches the coprocessor busy signal (387BUSY-) and generates an IRQ386. The IRQ386 output is directly connected to the IRQ13 signal in an IBM AT implementation. The latched busy signal clears upon receiving the INTCLR input from the 82C316. The INTCLR is generated by the 82C316 as a result of RESET3 or an Out command to port F0H or F1H.

BUSY386 output is derived from three different sources: 387BUSY, latched 387BUSY due to the 387 unmasked exception, or REF- when the 80387 is not present in the system.

When the 80387 is not present in a system, the BUSY- input of the 80386 needs to be toggled following the code write to the 80387 for at least 16 CLK2s before being deactivated again. The 82C315 implements the BUSY- toggling by allowing the DRAM refresh request (REF-) input from 82C311 to become 80386 busy (386BUSY-) output when the coprocessor is not present.

The 82C315 PRQ386 output to the 80386 PEREQ is active when either the 80387 PEREQ (PRQ387) is active or an error has occurred. The IRQ386 output is active when either an error has been detected or the Weitek coprocessor has requested an interrupt. In an AT implementation, the IRQ386 is connected to IRQ13. Figure 3-7 shows the interface logic for the 80387 and Weitek Coprocessor.

Figure 3-7. 80387/WEITEK Coprocessor Interface Logic



14.318 MHz oscillator circuit and divide by 12 counter

The 82C315 provides the reference oscillator (OSC) for the AT bus eliminating the 8224 normally used in AT compatible systems. The OSC output is a high speed clock with a 14.31818 MHz frequency (70 ns period). A divide by 12 counter is also included to generate the OSC/12 (1.19 MHz) signal used on the system board. A parellel resonanat crystal is used for this oscillator.

Byte Enable Latch

The 82C315 provides registers to hold the byte enables valid during the entire length of the memory cycle. The 82C315 latches the BE<0:3>- signals on the rising edge of MALE- and generates latched byte enables LBE<0:3>-. An additional input FBE- is also provided to force all byte enables active during read miss cycles and DMA cycles to perform a full 32-bit memory access.

Configuration Register

The configuration register, REG07 in the 82C315, is used for clock selection. An indexing scheme to port 22H and 23H is used to access the register. Port 22H is used as an indexing register and port 23H is used as a data register. The index value is placed on port 22 to access a particular register; the data read from or written to that register is located at port 23H. Every access to port 23H must be preceded by a write of the index value to port 22H even if the same register data is being accessed again.

Bus Controller's Internal Registers

The register in 82C315 is accessed using Port 22 and port 23. Each access (either read or write) to configuration register is done by first writing its index(in case of 315 it is 07) into port 22and then reading port 23 to read the contents of 07 or writing to port 23 the data required to be written to the register. Each access to port 23 should be preceeded by writing the index value to port 22H, even if the same data port is accessed again.

Name: Processor and Bus Clock Source Select

Index	Bits	Values and Functions
07H	7:5	Reserved
02		(0): Default value
	4	Presence of 80387 (Read Only)
		0: The 80387 is not present
		1: The 80387 is present
	3	Processor Clock Select
		(0): Select CLK2IN as processor clock
		1: Select AT bus state machine clock as processor clock
	2:0	Bus Clock Source Select
		(000): Select CLK2IN/5
		001: Select CLK2IN/4
		010: Select CLK2IN/3
		011: Select CLK2IN/2
		100: Select ATCLK

82C315 Pin Descriptions

Pin #	Symbol	Type	Signal Description
143-140	AC<0:3>	I	ACTION CODEs are a four bit encoded command from the 82C311 and are used for data bus sizing and byte assembly operations. The four bit encoded command controls how the data bus bits are connected between the SD (I/O Channel) bus and the LD (CPU Local) bus or the MD (System Memory) bus. Signals AC<0:3> are qualified by the ACEN signal.
139	ACEN-	I	ACTION CODE ENABLE is an active low input from the 82C311. When active ACEN- validates Action Code signals AC<0:3>.
145	SDIR	I	SYSTEM bus DIRECTION is an input signal which controls the direction of data transfers between the SD (I/O Channel) bus and the MD bus. When low, it enables data transfers from the SD bus to the LD bus. A high input enables transfers from the LD bus to the SD bus.
146	ATEN-	I	AT ENABLE is an active low input signal and when active indicates the current CPU cycle is an AT bus access.
147	HLDA1	I	HOLD ACKNOWLEDGE 1 is an active high input signal from the 82C311 and indicates the CPU has relinquished control of the system buses in response to HRQ1.
120	RESET3	I	RESET3 is an active high input from the 82C311. RESET3 is used in 82C315 to detect the 387 coprocessor during system reset.
119	RESET4	I	RESET4 is an active high input used to reset the 82C315 internal registers as well as the 80387 coprocessor detection during the system reset. RESET4 is an input from 82C311 and is synchronized with the processor clock.
148	DRD-	I	DRAM READ or MEMORY BUS DIRECTION is an active low signal. When active, it enables data movement from the MD bus to the SD bus. A high input enables the drivers from the SD to the MD bus.
118	REF-	I	Refresh is an active low input indicating a refresh cycle for the main memory DRAMs from 82C311. It is also used to toggle the 80386 BUSY signal if a Coprocessor is not present to prevent the 80386 from hanging.
150	DLE-	I	DATA LATCH ENABLE is an active low input signal used to latch the data in the 82C315 memory data buffers. This pin is normally connected to the CAS- output of the 82C311.

Pin #	Symbol	Type	Signal Description
151	IO2XCS-	I	I/O ADDRESS 22H and 23H CHIP SELECT is an active low signal from the 82C316. I/O port 22H is the index register for the configuration register set and I/O port 23H is accessed as the 8 bit data register selected by the index written to I/O port 22H.
135	MSE(AEN)	I	MODULE SELECT ENABLE from 82C316 indicates a chip select on one of the following modules: (DMA CONTROLLER, INT CONTROLLER, TIMER, RTC, DMA PAGE REGISTER, CONFIGURATION REGISTERS). When active during the DMA cycle, it disables the data transfer between the SD and XD buses.
136	XDIR	I	X DIRECTION is an active low signal from the 82C316 and controls the drivers between the X bus and the S bus. When low, XDIR drives the S bus signals towards the X bus. When high, XDIR drives the X bus signals towards the S bus. This input is ignored when AEN is active. XDIR is generated by 82C316 for I/O address 0 to 256H for read cycles(and also INTA cycles)
137	XDIR1	I	X BUS DIRECTION 1 is used for functional enhancements. As compared to XDIR, XDIR1 is not limited to I/O address of 256H boundary. Internal to 82C315 the XDIR1 is ORred with XDIR. The XDIR1 input can be a I/O address decode (using external decode) output.This input is ignored when AEN is active and should be tied to ground if not used.
114	PRQ387	I	PROCESSOR REQUEST 80387 is an active high signal which indicates a coprocessor request for a data operand to be transferred to or from memory by the CPU.
116	387ERR-	I	80387 ERROR is an active low signal from the 80387 which indicates the previous coprocessor instruction generated is a non-masked error. A 4.7K pull-up is recommended.
117	387BUSY-	I	80387 BUSY is an active low signal from the 80387 which indicates the coprocessor is still executing an instruction. A 4.7K pull-up is recommended.
43	XA0	I	Peripheral ADDRESS bit 0 is an input signal from 82C316. It is used with IO2XCS- signal to access I/O PORTS 022H or 023H.
123	BUSY386-	O	BUSY 80386 is an active low output signal to the 80386 which indicates to the CPU the coprocessor is still executing an instruction. BUSY386- is latched when an error condition has occured. This output has a 4mA drive capability.
122	ERR386-	O	ERROR 80386 is an active low output signal to the 80386 which indicates to the CPU the coprocessor has encountered an error with the last instruction. This output also indicates to the 80386 the presence of a coprocessor during the reset. This output has a 4mA drive capability.

Pin #	Symbol	Type	Signal Description
124	PRQ386	O	PROCESSOR REQUEST 80386 is an active high output signal to the 80386 which indicates the coprocessor's request for a data operand to be transferred to or from memory by the CPU. This signal is also forced high when an error has occured and 387BUSY- has gone inactive. This output has a 4mA drive capability.
125	IRQ386	O	INTERRUPT REQUEST 80386 is an active high output signal to the 80386 which indicates an interrupt request from the coprocessor. This signal is active when an error condition has occurred or a Weitek interrupt is initiated. This signal is the same as IRQ13 in an IBM AT implementation. This output has a 4mA drive capability.
112	WTPRES-	I	WEITEK PRESENT is an active low signal and indicates the persence of a WEITEK coprocessor. This signal is used to qualify WTINTR to generate IRQ386. A 10K pull-up is recommended.
113	WTINTR	I	WEITEK INTERRUPT is active high and is the interrupt signal from WEITEK coprocessor. A 2.2K pull down is recommended.
133-126	XD<0:7>	I/O	EXPANSION DATA bits 0 through 7 are bidirectional signals for the XD (Peripheral Data) bus. XD<0:7> is used to communicate to and from the keyboard controller, the 82C311 and the 82C316. These signals have a 4mA drive capability.
34-27	XD<8:15>	I	EXPANSION DATA bits 8 through 15 for the Peripheral Data Bus are input only signals and are enabled internally by the ROMCS- signal. This bus is connected to the high byte of EPROM data bus only.
102-98 95-91 88-83 69,66, 62 58-54 51-47	MD<0:31>	I/O	MEMORY DATA bits 0 through 31 are for the System Memory Data Bus interface. These signals have an 8 mA drive capability.
3-6 9-13 16-19 23-25	SD<0:15>	I/O	I/O CHANNEL DATA bits 0 through 15 are for the I/O Channel Data interface. These signals have a 12mA drive capability.
110-107	BE<0:3>-	I	BYTE ENABLE signals are inputs from the 80386 during a CPU cycle. BE3- controls the most significant byte while BE0- controls the least significant byte.
80-77	LBE<0:3>-	O	LATCH BYTE ENABLE signals are the BE<0:3>- input signals latched from the trailing edge of MALE-. These signals have a 12mA drive capability.
111	MALE-	I	MEMORY ADDRESS LATCH ENABLE is an active low input signal and clocks addresses into the address registers on the rising edge.

Pin #	Symbol	Type	Signal Description
106	FBE-	I	FORCE BYTE ENABLE is an active low input signal and forces all byte enables LBE<0:3>- active independent of MALE- and the BE<0:3>- inputs. It is an input from 82C311 and is active during local memory read miss or DMA read cycles.
73-70	MP<0:3>	I/O	MEMORY PARITY is the data parity bits for the DRAMs. These are inputs during DRAM read cycles and output during DRAM write cycles. These signals have an 8mA drive capability.
144	BWBUSY	I	BUFFER WRITE BUSY is an input signal from the 82C311 which indicates a buffer write cycle. It is used in 82C311 to tri-state the MD lines to avoid data contention.
115	INTCLR	I	INTERRUPT CLEAR is an active high input signal from the 82C316 which clears IRQ13. INTCLR is generated during reset, output to port F1, and write to port F0.
105	PEN-	I	PARITY ENABLE is an active low input signal from 82C311 which indicates overall parity check is enabled.
74	LPAR-	O	LATCHED PARITY ERROR is an active low output signal and indicates when an even parity error is detected on a memory access. The failing address is latched within 82C311 by this signal. This output signal has a 4mA drive capability.
26	ROMCS-	I	ROM CHIP SELECT is an active low signal which enables the XD<0:15> input lines to transfer data from the XD (Peripheral Data) Bus to the MD (System Memory Data) Bus.
149	IOR-	I	I/O READ is an active low input signal and is used to read the configuration register 07H.
42	IOW-	I	I/O WRITE is an active low input signal and is used to write to configuration register 07H.
2	CLK2IN	I	CLOCK 2 INPUT from a packaged CMOS crystal oscillator having twich the rated frequency of the processor.
159	CLK2	O	CLK2 is an output to the CLOCK 2 INPUT of the 80386, 80387, and 82C311. This clock output is derived from CLK2IN input and has a 50% duty cycle. The clock can also be programmed to be the same as the BCLK. This output signal has a 12mA drive capability.
156	SCLK-	O	SCLK- is CLK2 divided by two and is an output generated as a reference to verify the phase relationship of the internal clock and CLK2. This output signal has an 8mA drive capability.
45	ATCLK1	I	ATbus CLOCK is a CMOS input for a crystal or oscillator. This clock input is used for the AT Bus operation and is required if the AT Bus state machine clock (BLK) is not derived from the CLK2 input. This signal should be tied low or high if not used, and its frequency should be lower than CLK2IN.

Pin #	Symbol	Type	Signal Description
44	ATCLK2	O	AT bus CLOCK is connected to the crystal oscillator circuit if a packaged oscillator is not used. A series resistor of 10 ohms should be used to reduce the amplitude of the resonant circuit. It should be left unconnected if a packaged CMOS oscillator is used. This signal has a 4mA drive capability.
36	CX1	I	14.318MHz CMOS oscillator input from the crystal.
37	CX2	O	14.318MHz oscillator output to the crystal. This output has a 4mA drive capability.
39	OSC	O	OSCILLATOR System 14.318MHz output has a 24mA drive capability. It drives the AT I/O channel.
38	OSC1M19	O	OSCILLATOR 1.19MHz = 14.318MHz/12. OSC1M19 is used for RAS low time out. This output has a 24mA drive capability.
153	BCLK	O	BUS CLOCK is the clock used for the AT bus state machine in the 82C311 chip. It can be 1/2, 1/3, 1/4, or 1/5 of CLK2IN frequency or as ATCLK1 input. This output has a 12mA drive capability.
46, 155, 157	NC		No connection. For normal operation, these pins should be left floating.
35	TEST-		Test is an active low input signal. It should be pulled high with a 10K ohm resistor for normal operation.
1,8,15,21, 22,41,53, 61,68,76, 82,90,97, 104,121, 152,158	VCC	I	Supply Voltage, 5V± 5%.
7,14,20,40 52,59,60, 67,75,81, 89,96,103, 134,138, 154,160	VSS	I	Ground.

82C315 Absolute Maximum Ratings

Table 3-6. *Absolute Maximum Ratings*

	Symbol	Min.	Max.	Units
Supply Voltage	Vcc		7.0	V
Input Voltage	VI	-.5	5.5	V
Output Voltage	VO	-.5	5.5	V
Operating Temperature	Top	-25	85	C
Storage Temperature	Tstg	-40	125	C

Note Exposure to absolute maximum ratings for extended periods may affect device reliability. Exceeding the absolute maximum ratings can cause permanent damage to the device.

Table 3-7. *Operating Condition*

	Symbol	Min.	Max.	Units
Supply Voltage	Vcc	4.75	5.25	V
Ambient Temperature	TA		70	C

DC Parameters

Table 3-8. DC Parameters

		Min.	Max.	Units
ViL	(all pins except CX1 ATCLK1 and CLK2IN)	-0.3	0.8	V
ViH	(all pins except CX1 ATCLK1 and CLK2IN)	2.0	Vcc + 0.3	V
Vil	(CX1, CLK2IN, ATCLK1)	-0.3	0.8	
Vih	(CX1, CLK2IN, ATCLK1)	Vcc-0.8	Vcc+0.3v	V
Vol			0.45	V
Voh		2.4		V
IIL	(all inputs except 387BUSY- and 387ERR-)		-10	µA
IIH			10	µA
IIL	(387BUSY- and 387ERR-)		1	mA
	3-state output OFF current low		-10	µA
	3-state output OFF current high		10	µA
IOL	MD bus, OSC, OSC1M19, BCLK	8		mA
IOH		-8		mA
IOL	SD bus, LBE<3:0>-	24		mA
IOH		-3.3		mA
IOL	XDBUS, CX2, BUSY386-, ERR386-, PRQ386	.4		mA
IOH	IRQ386, LPAR-, all others	-4		
IOL	CLK2	16		mA
IOH	CLK2	-16		mA
ICC			90	mA

AC Characteristics

All timing parameters are specified under capacitive load of 50 pf and temperature of 70 degree C. The AC specifications mentioned in this section are subject to change.

Table 3-9. *Clocks*

	Clocks	33 MHz		
		Min.	Max.	Unit
t501	CLK2 period	15		ns
t502	CLK2 high time	6.5		ns
t503	CLK2 low time	6.5		ns
t504	CLK2 rise time		3	ns
t505	CLK2 fall time		3	ns
t506	BCLK period	30		ns
t507	BCLK high time	10		ns
t508	BCLK low time	10		ns
t509	BCLK rise time		5	ns
t510	BCLK fall time		5	ns
t511	SCLK- delay from CLK2	0	8	ns
t512	OSC low delay from CX1 high	4	20	ns
t513	OSC delay from CX1 low	4	23	ns
t514	OSCM19 delay from CX1 high	7	40	ns
t515	OSC1M19 delay from CX1 low	7	40	ns
t516	RESET 4 active hold time	6		ns
t517	RESET 4 inactive setup time	0		ns

Table 3-10. Parity Timing

Parity Timing		33 MHz		
		Min.	Max.	Unit
t518	LPAR- inactive delay from SCLK- high		30	ns
t519	LPAR- inavtice delay from PEN- high		30	ns
t520	LPAR- active delay from SCLK- high		30	ns
t521	LPAR-active delay from PEN- low	0	20	ns
t522	MP<3:0> set up time to CAS- high		23	ns
t523	MP<3:0> valid from MD<31:0>		23	ns
t524	MP<3:0> hold time to CAS- high	5		ns

Table 3-11. IO2XCS Cycles

IO2XCS Cycles		33 MHz		
		Min.	Max.	Unit
t526	XA0 setup to IOW- or IOR-	20		ns
t528	XD<7:0> hold to IOW-	7		ns
t530	XA0 hold to IOW- or IOR-	12		ns
t531	IOW- or IOR- pulse width	80		ns
t532	XD<7:0> valid from IOR-		28	ns

Table 3-12. 80387 Timing

	80387 Timing	33 MHz		
		Min.	Max.	Unit
t535	387ERR- setup to RESET 4 low	7		ns
t536	387ERR- hold to RESET 4 low	6		ns
t537	ERR386- delay from RESET 4 low	4	18	ns
t538	ERR386- delay from MALE- low	4	16	ns
t539	BUSY386- active delay from 387BUSY- active		22	ns
t540	BUSY386- inactive delay from 387BUSY- inactive	4	21	ns
t541	BUSY386- inactive delay from INTCLR high	3	22	ns
t542	IRQ386 active from 387ERR-low		22	ns
t543	IRQ386 inactive from INTCLR high		23	ns
t544	BUSY386- active from REF- low	6	25	ns
t545	BUSY386- inactive from REF- high	4	22	ns
t546	PRQ386 active from 387BUSY- high		23	ns
t547	PRQ386 inactive from INTCLR high	6	22	ns
t548	IRQ386 active from WTINTR high	4	18	ns
t549	IRQ386 inactive from WTINTR low	4	18	ns
t550	PRQ386 active from PRQ387 high	4	18	ns
t551	PRQ386 inactive from PRQ387 low	4	18	ns
t552	387BUSY- set up to 387ERR- low	4		ns
t553	387BUSY- hold to 387ERR- low	4		ns

Table 3-13. Data Paths

	Data Paths	33 MHz		
		Min.	Max.	Unit
t555	MD bus setup to DLE- high	8		ns
t556	MD bus hold to DLE- high	7		ns
t557	SD data valid from MD	8	35	ns
t558	XD data valid from MD	9	30	ns
t559	SD data setup to ACEN-	11		ns
t560	SD data hold to ACEN-	4		ns
t561	MD data valid from SD	8	25	ns
t562	MP data valid from SD		35	ns
t563	XD data setup to ACEN-	15		ns
t564	XD data hold to ACEN-	4		ns
t565	MD data valid from XD	10	35	ns
t566	SD Hi (Lo) byte valid from SD Lo (Hi) byte valid	9	35	ns
t567	MD tristate from BWBUSY high		21	ns

Table 3-14. Byte Enables Timing

	Byte Enables Timing	33 MHz		
		Min.	Max.	Unit
t575	BE<3:0>- setup to MALE- high	8		ns
t576	BE<3:0>- hold to MALE- high	4		ns
t577	LBE<3:0>- valid from BE<0:3>-	0	15	ns
t578	LBE<3:0>- delay from HLDA1	11	ns	
t579	LBE<3:0>- delay from BE<3:0>-	4	18	ns
t580	LBE<3:0>- active delay from FBE-	4	19	ns
t581	LBE<3:0>- inactive delay from FBE- inactive	4	9	ns

Table 3-15. Clocks

	Clocks	25 MHz		
		Min.	Max.	Unit
t501	CLK2 period	20		ns
t502	CLK2 high time	7		ns
t503	CLK2 low time	7		ns
t504	CLK2 rise time		4	ns
t505	CLK2 fall time		4	ns
t506	BCLK period	30		ns
t507	BCLK high time	10		ns
t508	BCLK low time	10		ns
t509	BCLK rise time		5	ns
t510	BCLK fall time		5	ns
t511	SCLK- delay from CLK2	0	8	ns
t512	OSC low delay from CX1 high	4	20	ns
t513	OSC delay from CX1 low	4	23	ns
t514	OSCM19 delay from CX1 high	7	40	ns
t515	OSC1M19 delay from CX1 low	7	40	ns
t516	RESET 4 active hold time	6		ns
t517	RESET 4 inactive setup time	0		ns

Table 3-16. Parity Timing

Parity Timing		25 MHz		
		Min.	Max.	Unit
t518	LPAR- inactive delay from SCLK- high		30	ns
t519	LPAR- inavtice delay from PEN- high		30	ns
t520	LPAR- active delay from SCLK- high		30	ns
t521	LPAR-active delay from PEN- low	0	20	ns
t522	MP<3:0> set up time to CAS- high		23	ns
t523	MP<3:0> valid from MD<31:0>		23	ns
t524	MP<3:0> hold time to CAS- high	5		ns

Table 3-17. IO2XCS Cycles

IO2XCS Cycles		25 MHz		
		Min.	Max.	Unit
t526	XA0 setup to IOW- or IOR-	20		ns
t528	XD<7:0> hold to IOW-	7		ns
t530	XA0 hold to IOW- or IOR-	12		ns
t531	IOW- or IOR- pulse width	80		ns
t532	XD<7:0> valid from IOR-		28	ns

Table 3-18. 80387 Timing

	80387 Timing	25 MHz		
		Min.	Max.	Unit
t535	387ERR- setup to RESET 4 low	7		ns
t536	387ERR- hold to RESET 4 low	6		ns
t537	ERR386- delay from RESET 4 low	4	18	ns
t538	ERR386- delay from MALE- low	4	16	ns
t539	BUSY386- active delay from 387BUSY- active		22	ns
t540	BUSY386- inactive delay from 387BUSY- inactive	4	21	ns
t541	BUSY386- inactive delay from INTCLR high	3	22	ns
t542	IRQ386 active from 387ERR-low		22	ns
t543	IRQ386 inactive from INTCLR high		23	ns
t544	BUSY386- active from REF- low	6	25	ns
t545	BUSY386- inactive from REF- high	4	22	ns
t546	PRQ386 active from 387BUSY- high		23	ns
t547	PRQ386 inactive from INTCLR high	6	22	ns
t548	IRQ386 active from WTINTR high	4	18	ns
t549	IRQ386 inactive from WTINTR low	4	18	ns
t550	PRQ386 active from PRQ387 high	4	18	ns
t551	PRQ386 inactive from PRQ387 low	4	18	ns
t552	387BUSY- set up to 387ERR- low	4		ns
t553	387BUSY- hold to 387ERR- low	4		ns

Table 3-19. Data Paths

	Data Paths	25 MHz Min.	25 MHz Max.	Unit
t555	MD bus setup to DLE- high	8		ns
t556	MD bus hold to DLE- high	7		ns
t557	SD data valid from MD	8	35	ns
t558	XD data valid from MD	9	30	ns
t559	SD data setup to ACEN-	11		ns
t560	SD data hold to ACEN-	4		ns
t561	MD data valid from SD	8	25	ns
t562	MP data valid from SD		35	ns
t563	XD data setup to ACEN-	15		ns
t564	XD data hold to ACEN-	4		ns
t565	MD data valid from XD	10	35	ns
t566	SD Hi (Lo) byte valid from SD Lo (Hi) byte valid	9	35	ns
t567	MD tristate from BWBUSY high		21	ns

Table 3-20. Byte Enables Timing

	Byte Enables Timing	25 MHz Min.	25 MHz Max.	Unit
t575	BE<3:0>- setup to MALE- high	8		ns
t576	BE<3:0>- hold to MALE- high	4		ns
t577	LBE<3:0>- valid from BE<0:3>-	0	15	ns
t578	LBE<3:0>- delay from HLDA1		11	ns
t579	LBE<3:0>- delay from BE<3:0>-	4	18	ns
t580	LBE<3:0>- active delay from FBE-	4	19	ns
t581	LBE<3:0>- inactive delay from FBE- inactive	4	9	ns

82C315 Timing Diagrams

Figure 3-8. *AT CLK1 , CLK2IN Timing*

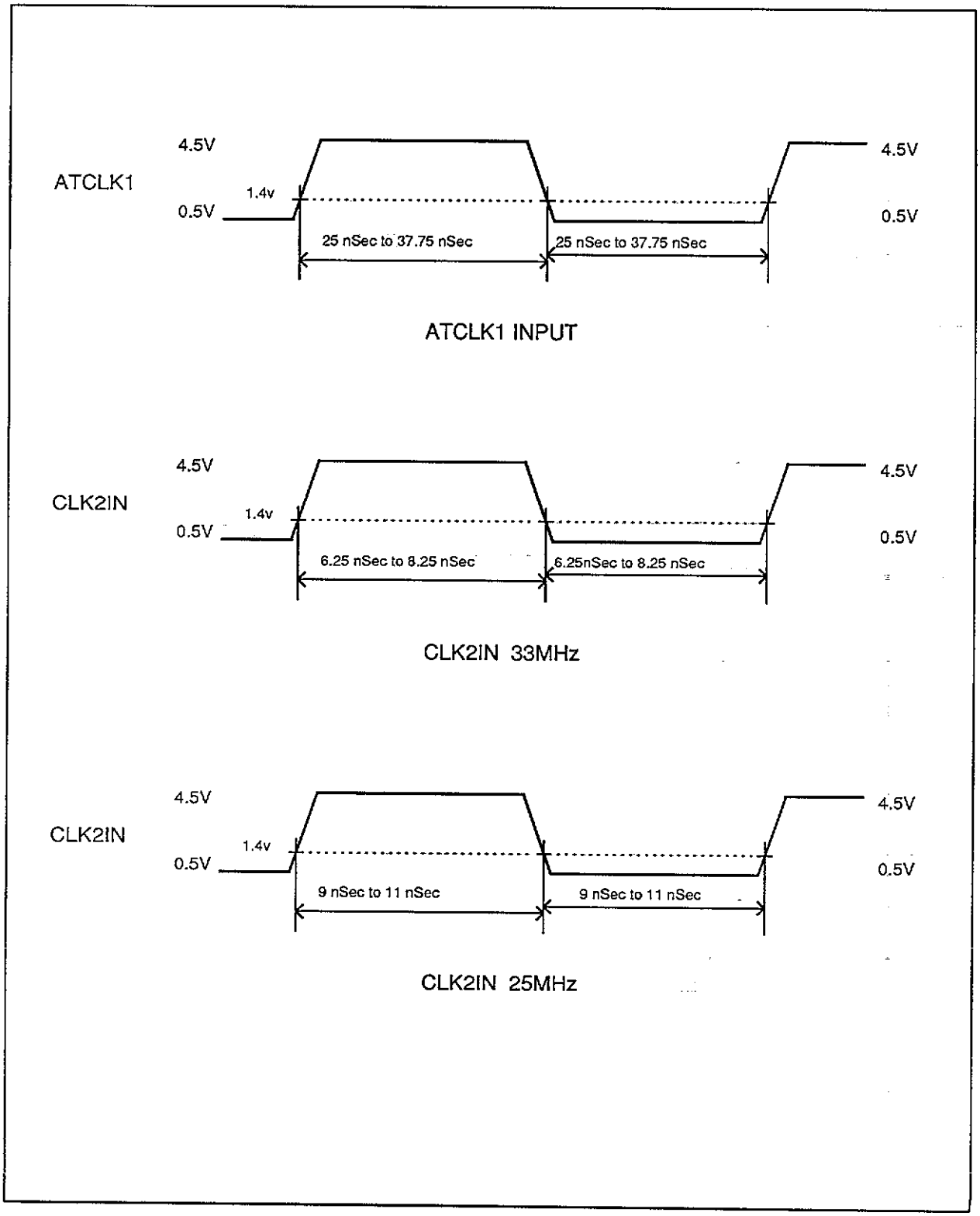
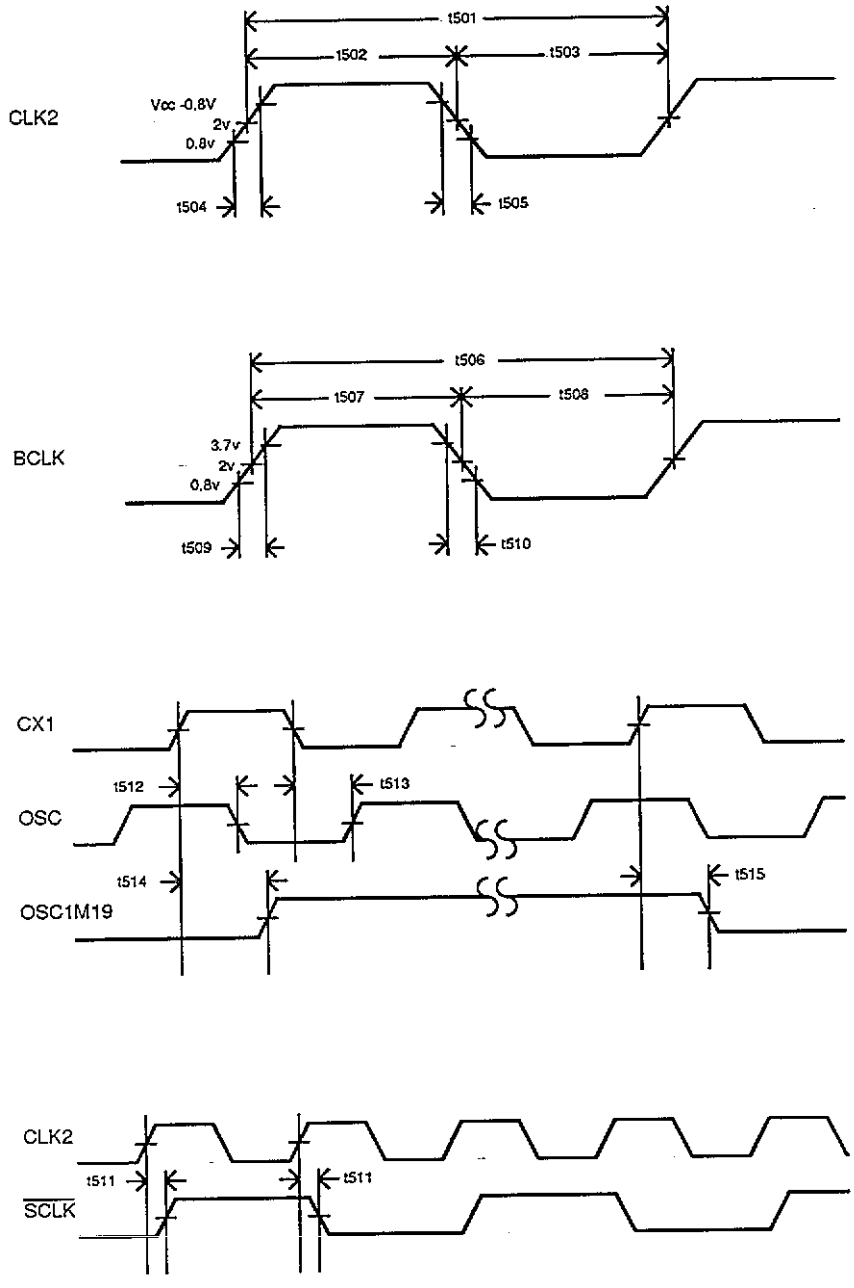


Figure 3-9. *CLK2, BCLK, OSC1M19, SCLK*



82C315 CLOCK TIMING

Figure 3-10. *Clock Switching*

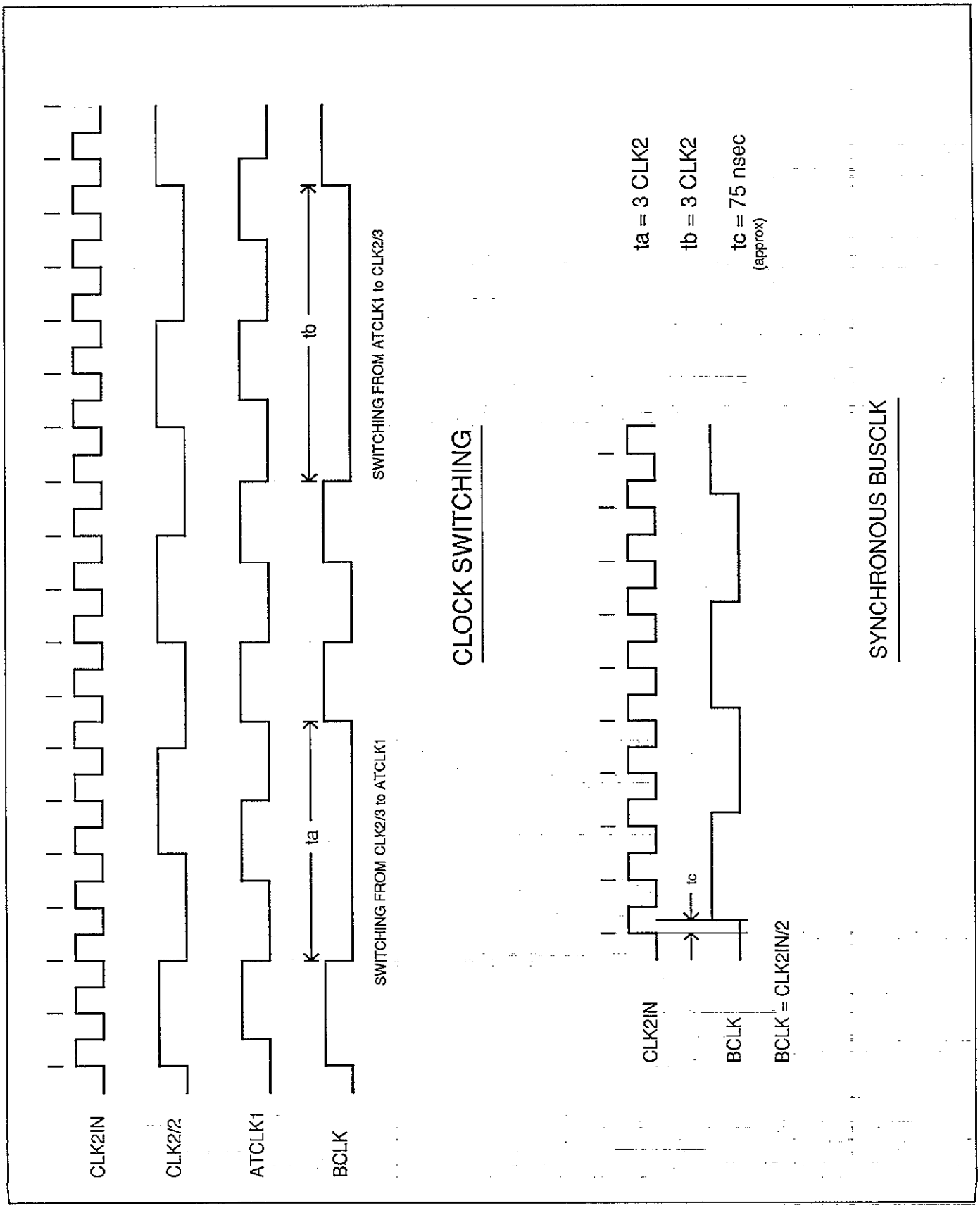
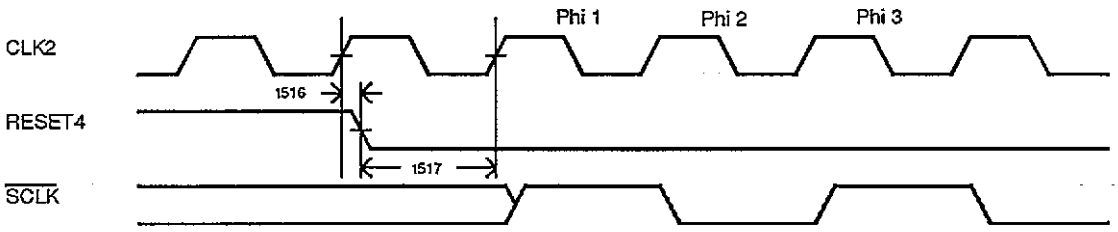


Figure 3-11. Reset Timing



82C315 RESET TIMING

Figure 3-12. *Write Parity Timing*

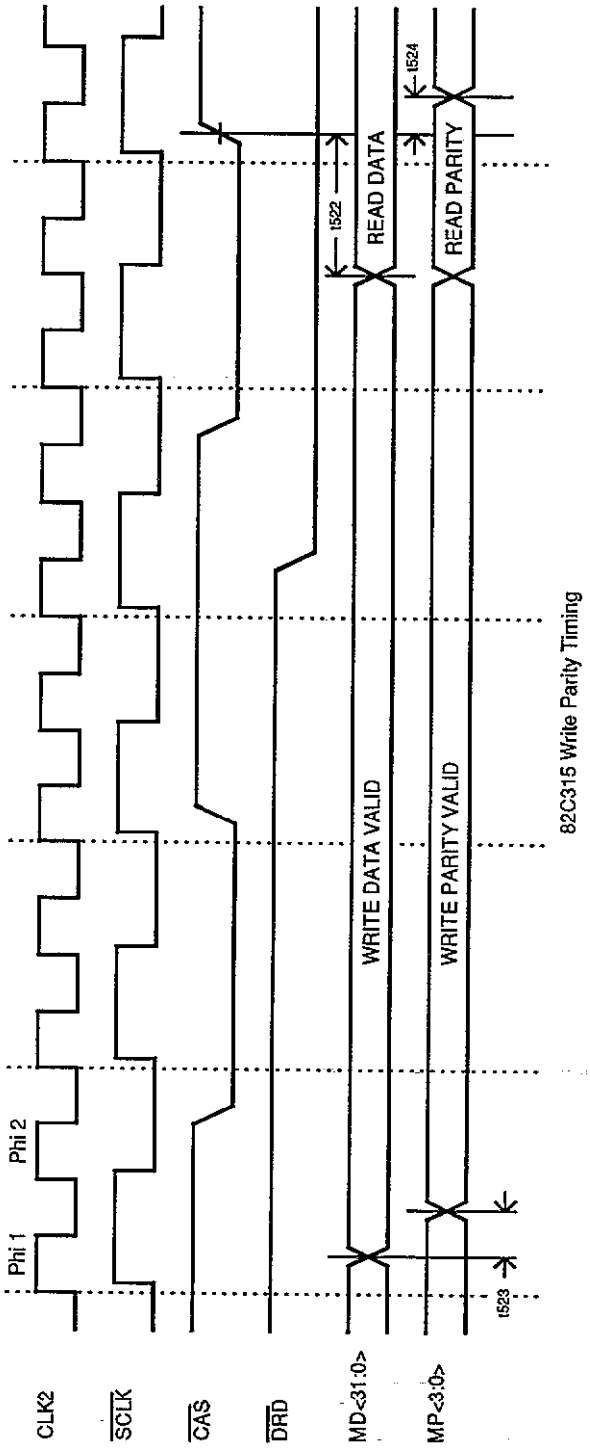


Figure 3-13. LPAR Timing

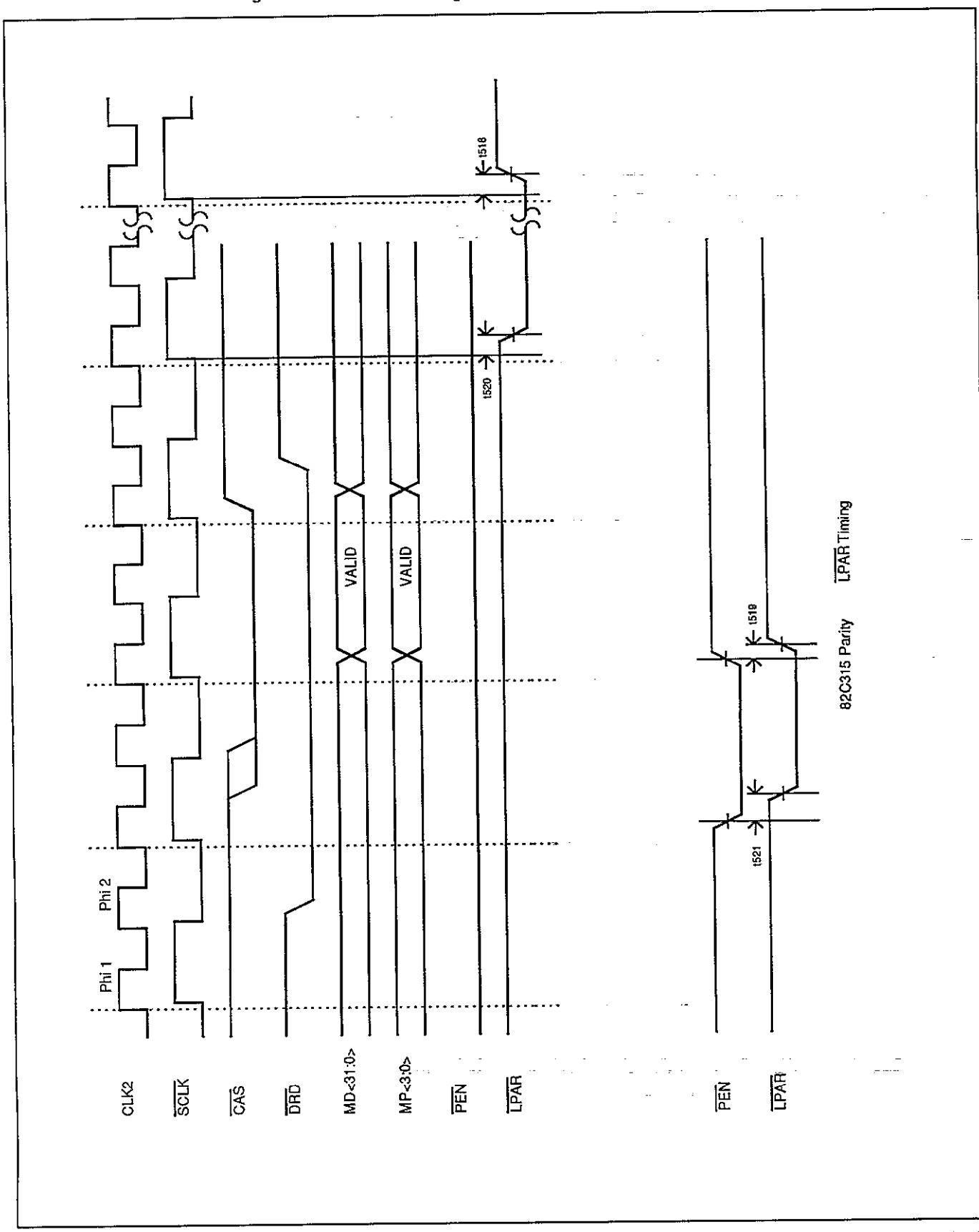


Figure 3-14. *IO2XCS Cycles*

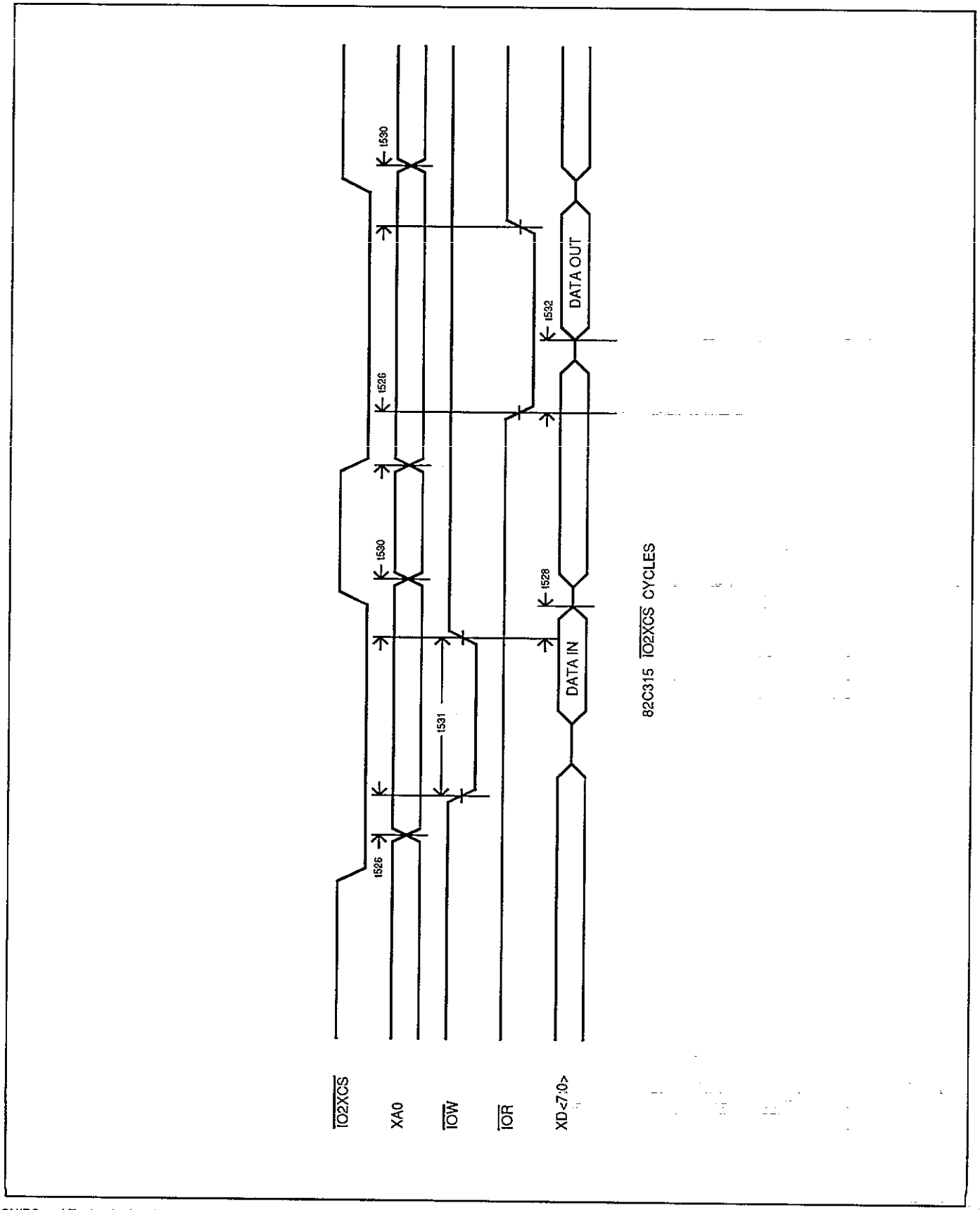


Figure 3-15. *387 Interface*

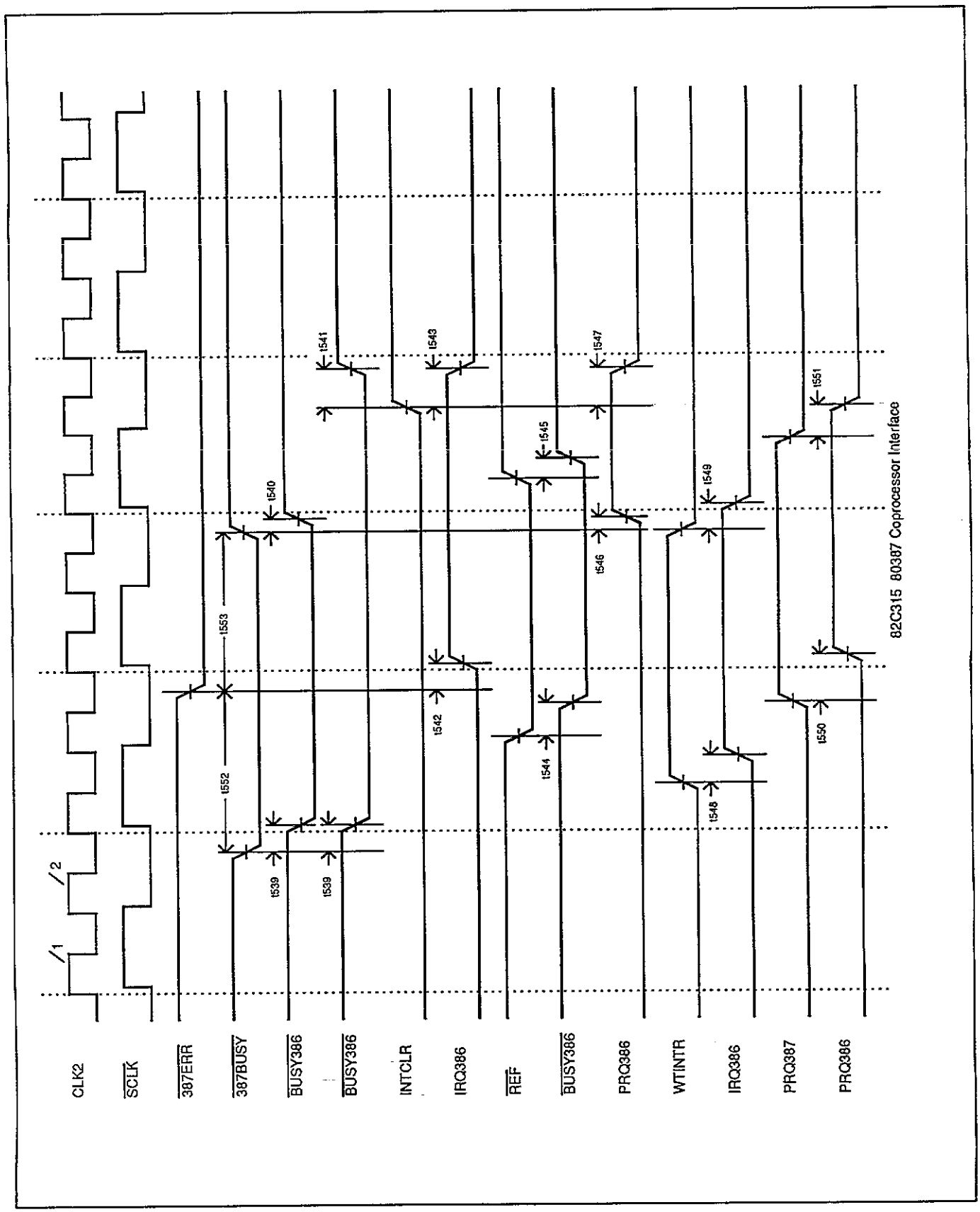
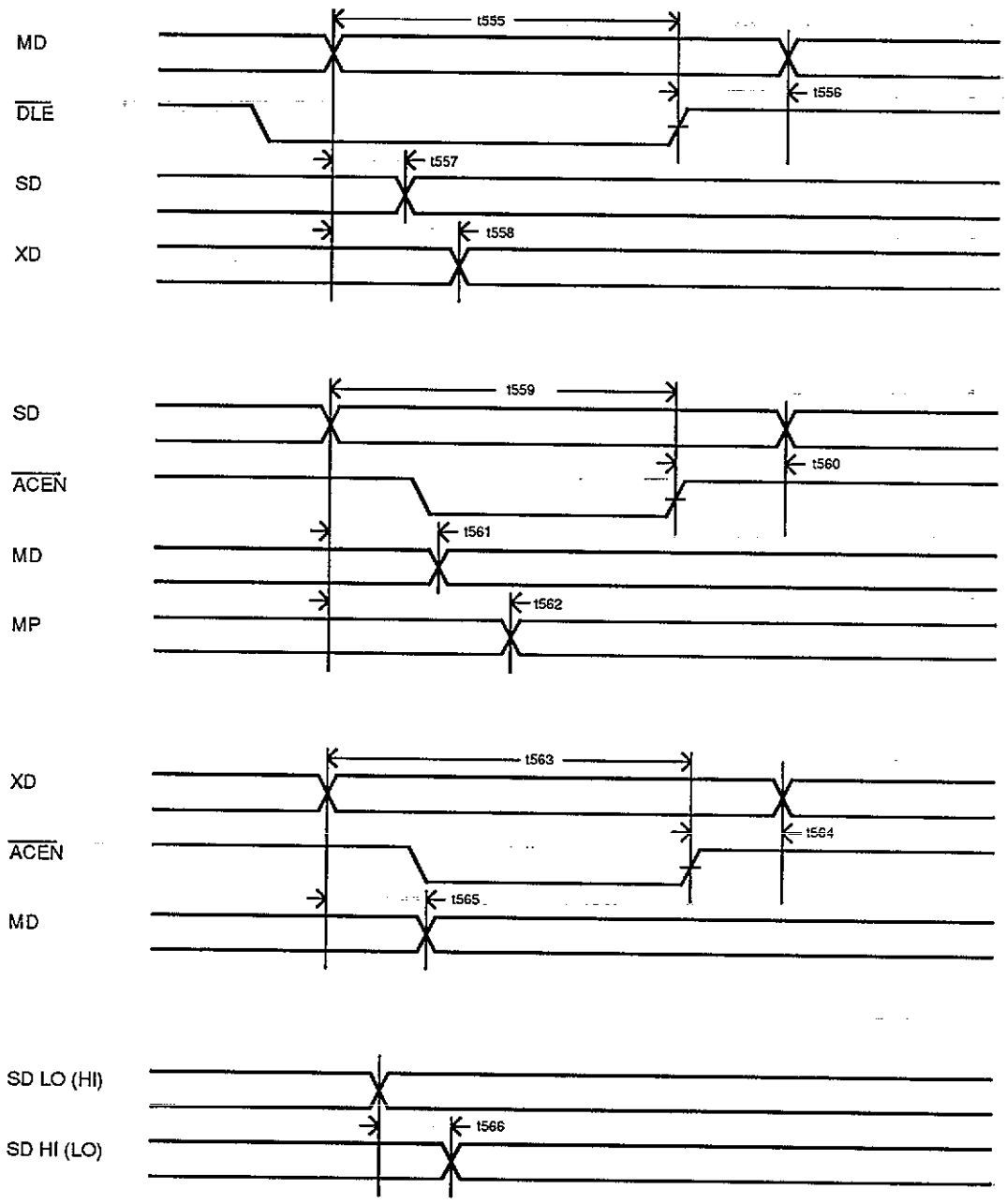
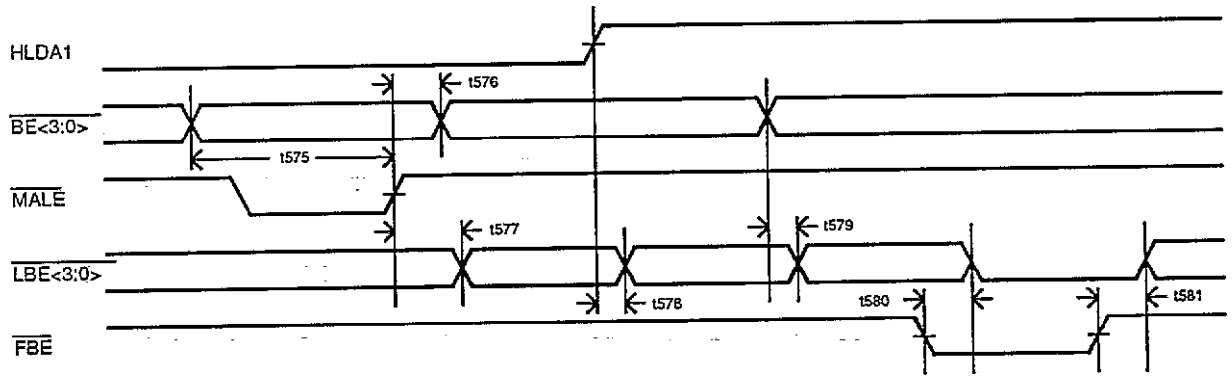


Figure 3-16. *Data Paths*

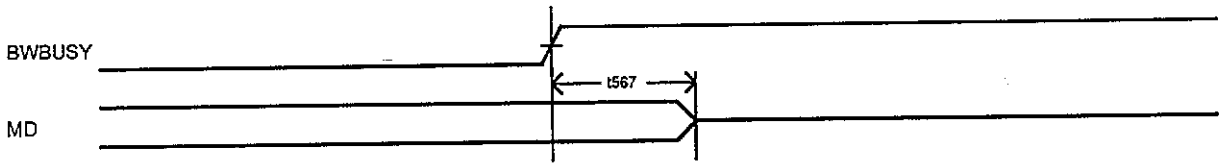


82C315 Data Paths

Figure 3-17. *More Data Paths*



82C315 LBE<3:0> Timing



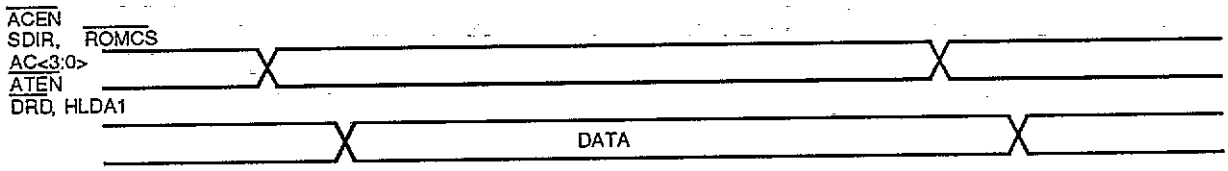


Figure 3-18. *82C315 Pin Diagram*

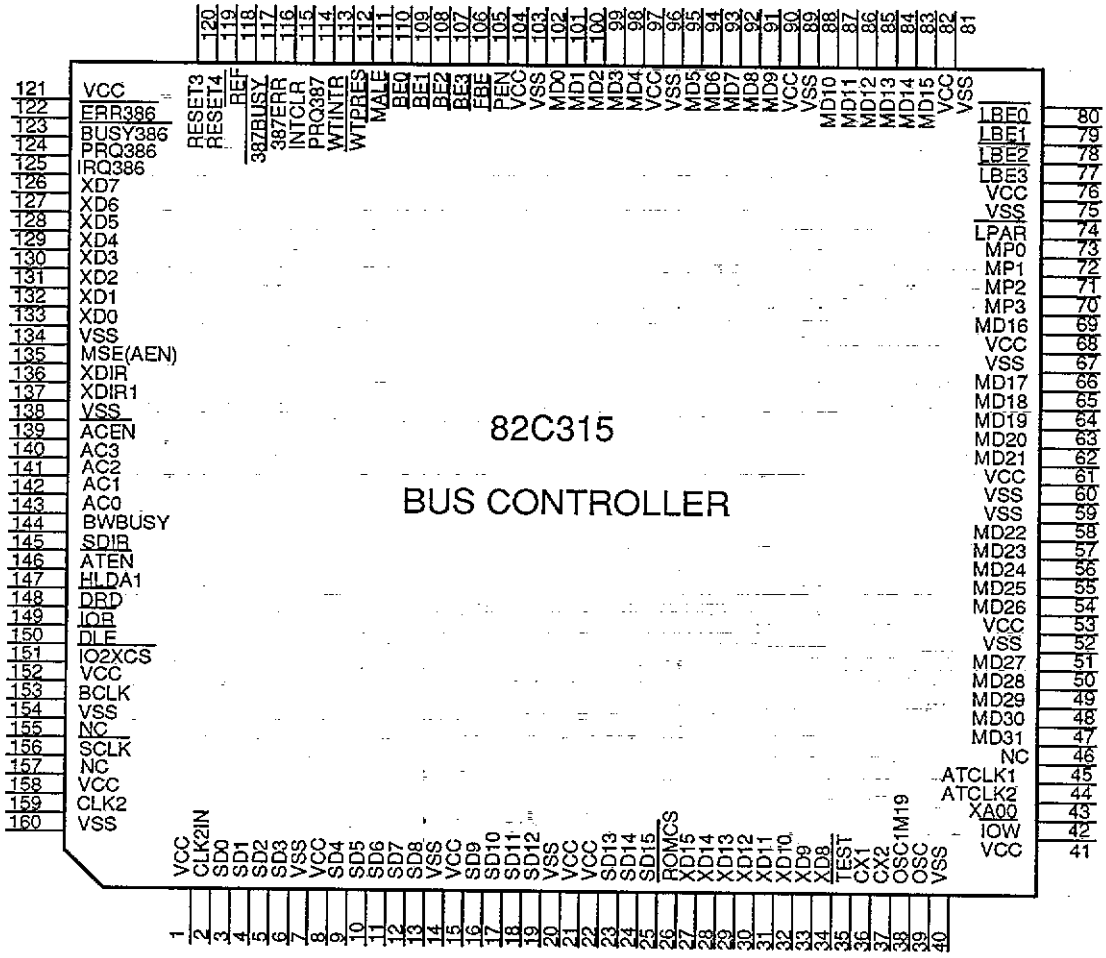
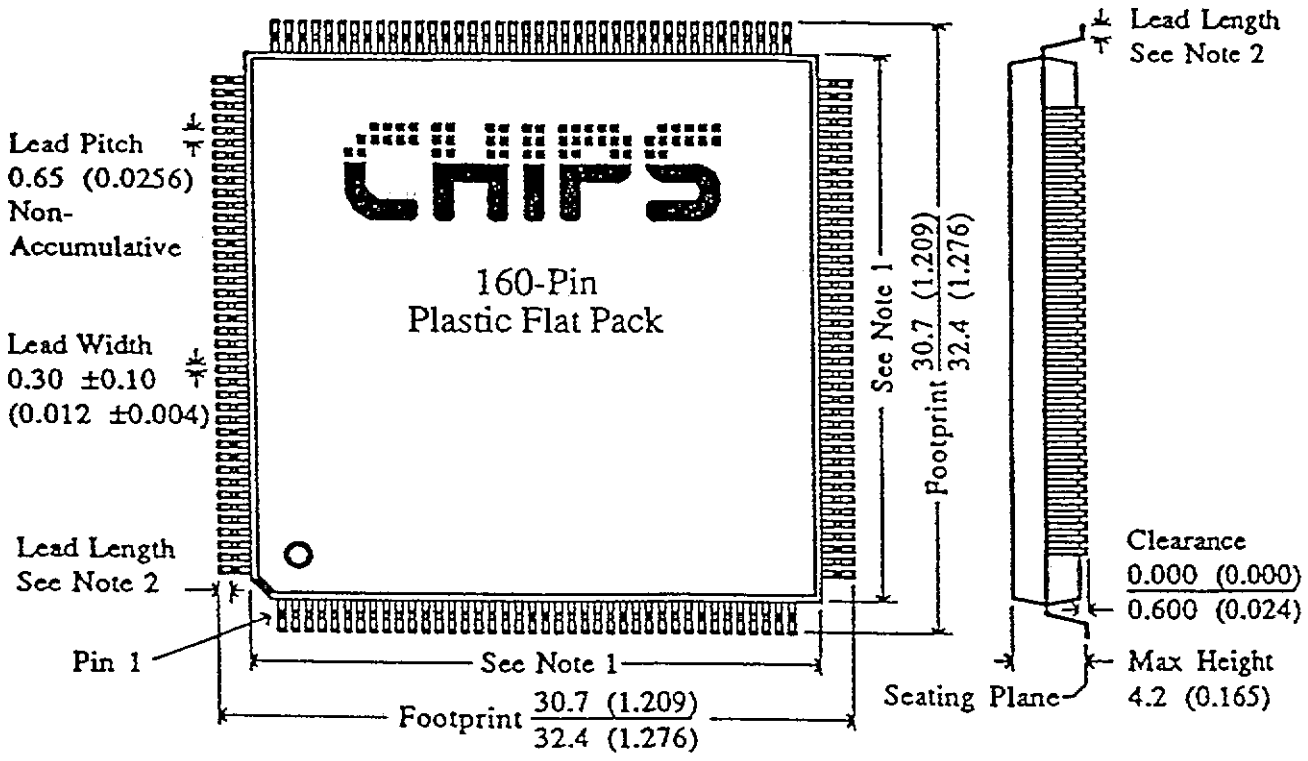


Figure 3-19. 82C315 Mechanical Dimensions

DIMENSIONS: mm (in)



Note 1: Package Body Size = 28 +0.2/-0.4 (1.102 +0.008/-0.016) (Swire)
Package Body Size = 28 ±0.2 (1.102 ±0.008) (All Other Package Vendors)

Note 2: Lead Length = 0.6 ±0.3 (0.024 ±0.012) (Package Vendor = Seiko)
Lead Length = 0.7 ±0.2 (0.028 ±0.008) (Package Vendor = Yamaha)
Lead Length = 0.8 ±0.2 (0.031 ±0.008) (All Other Package Vendors)

Section 4

82C316 Peripheral Controller

Features

The 82C316 peripheral controller contains the address buffers used to interface the local address bus (A<2:23>) and the I/O channel address bus (SA<0:19> and LA<17:23>). It also contains an equivalent Integrated Peripheral Controller (IPC) which incorporates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one MC146818 real time clock, and the 74LS612 memory mapper, in addition to several other SSI interface logic devices.

Functional Description

The 82C316 peripheral controller consists of the following functional subsystems as shown in Figure 4-1:

- Address bus interface between the SA and LA buses
- Address decode
- Programmable chip selects
- Port B and NMI logic
- 80387 RESET logic
- Integrated peripheral controller (IPC)
- Configuration register

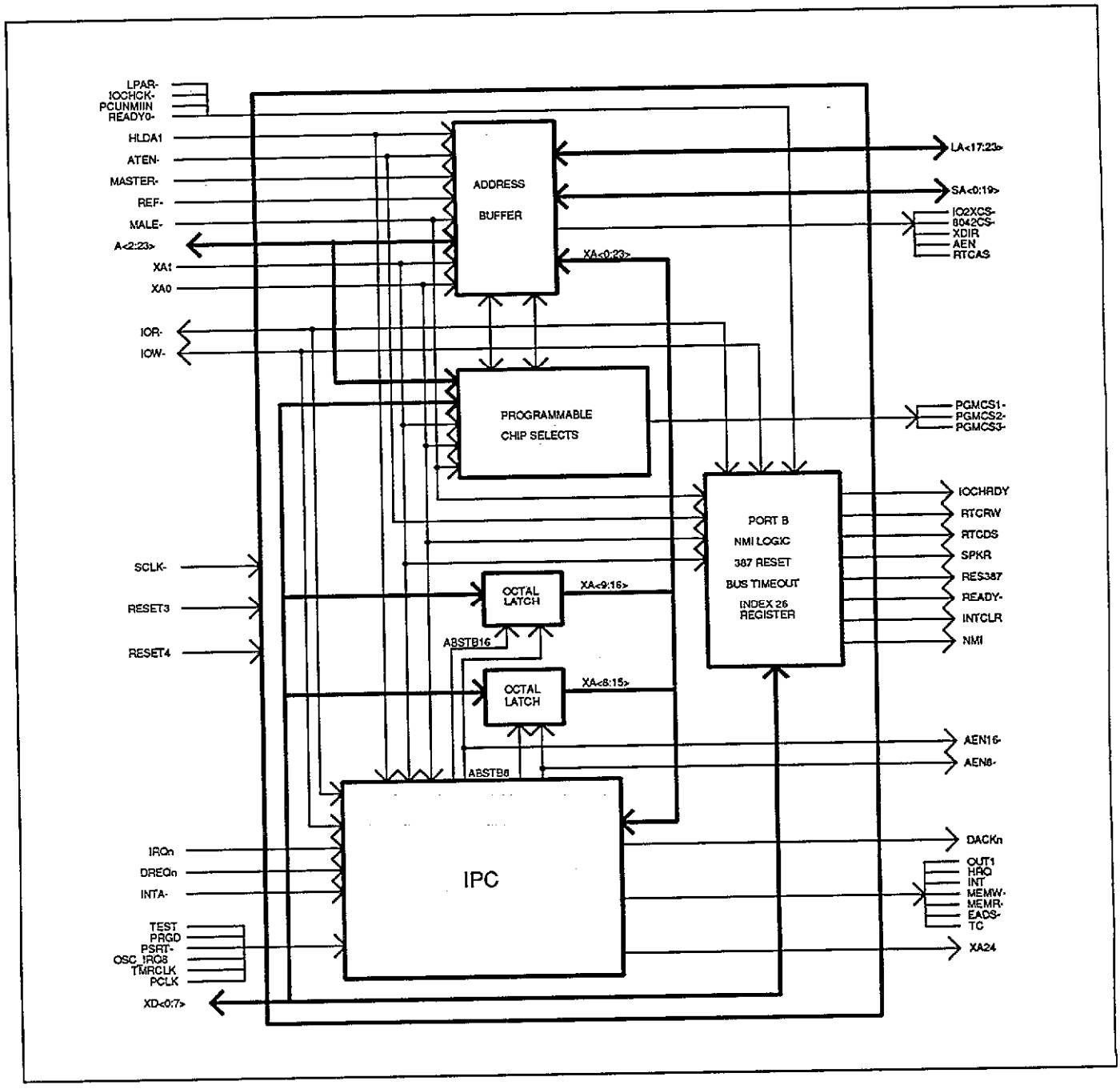
Address Bus Interface Between SA and LA Buses

The 82C316 interconnects the System Address bus (SA<0:19> and LA<17:23>) to the local bus (A<2:31>) with bi-directional drivers. There is also an internal peripheral address bus XA<0:23> which connects the peripherals to the system and local buses.

The drivers provided are 24mA current drivers for direct connection to the I/O channel address bus. The buffers are controlled by the HLDA1, MASTER-, REF-, and ATEN- to drive the signals from the source to the target buses.

When REF- is asserted, the refresh address is latched onto the SA bus as the refresh row address and the refresh counter for the I/O channel residing in the 82C316 is incremented.

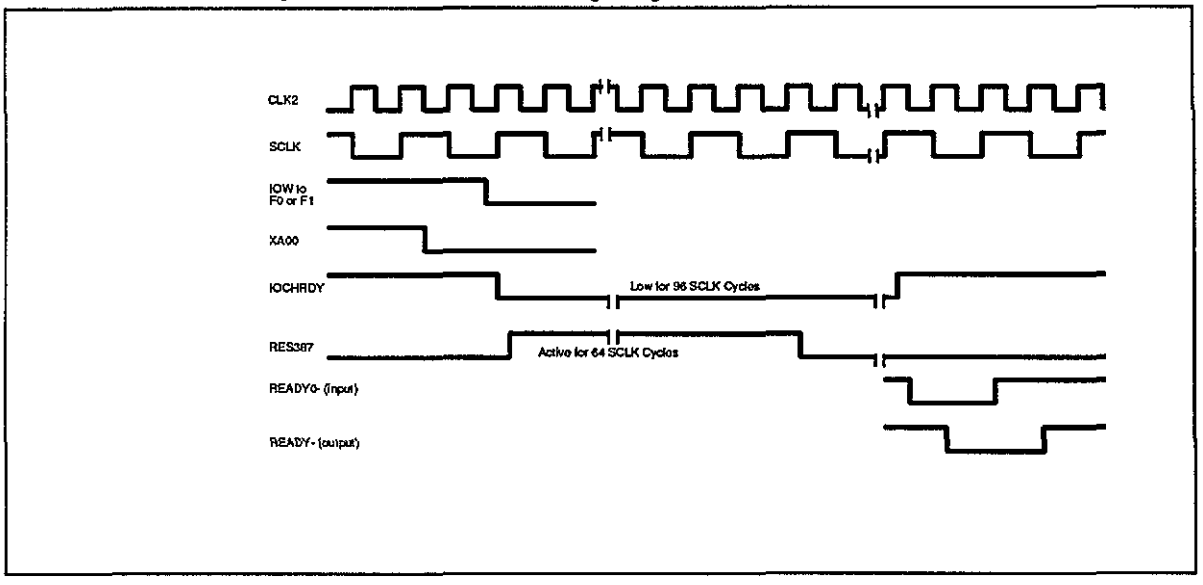
Figure 4-1. 82C316 Block Diagram



When none of the listed signals are active, the default buffer direction is from the A bus to the SA bus for memory accesses initiated by the CPU. For all CPU sourced accesses, the addresses are latched on the trailing edge of MALE-.

Table 4-1 shows how the drivers are configured between the buses for each type of active bus requests.

Figure 4-2. 387 Reset Timing Diagram



Integrated Peripheral Controller (IPC)

The 82C316 portion of 82C316 is an LSI implementation of the standard peripherals required to implement an IBM PC/AT system board. This device contains the equivalent of two 8237A DMA Controllers, a 74LS612 Mapper, two 8259A Interrupt Controllers, an 8254 Counter/Timer, and an MC 146818 Real Time Clock with RAM. The 82C316 provides all of the standard peripherals required for a system board implementation except the keyboard interface controller. Figure 4-3 illustrates the subsystems contained within the 82C316.

Two DMA Controllers are provided and connected in such a way as to provide the user with four channels of DMA (DMA1) for 8-bit transfers, and three channels of DMA (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMAPAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Sixteen channels of interrupt are provided in the 82C316. These channels are partitioned into two cascaded controllers (INTC1,INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices; allowing 13 user definable channels of interrupt. The three internally connected channels are as follows:

Channel 0	Counter/Timer Counter 0 Interrupt
Channel 2	Cascade to Slave Interrupt Controller (INTC2)
Channel 8	Real Time Clock Interrupt

The remaining 13 channels may be defined and utilized as necessary to meet the users specific system requirements.

A Counter/Timer (CTC) subsystem is provided which contains three independent counters. All three counters are driven from a clock input pin

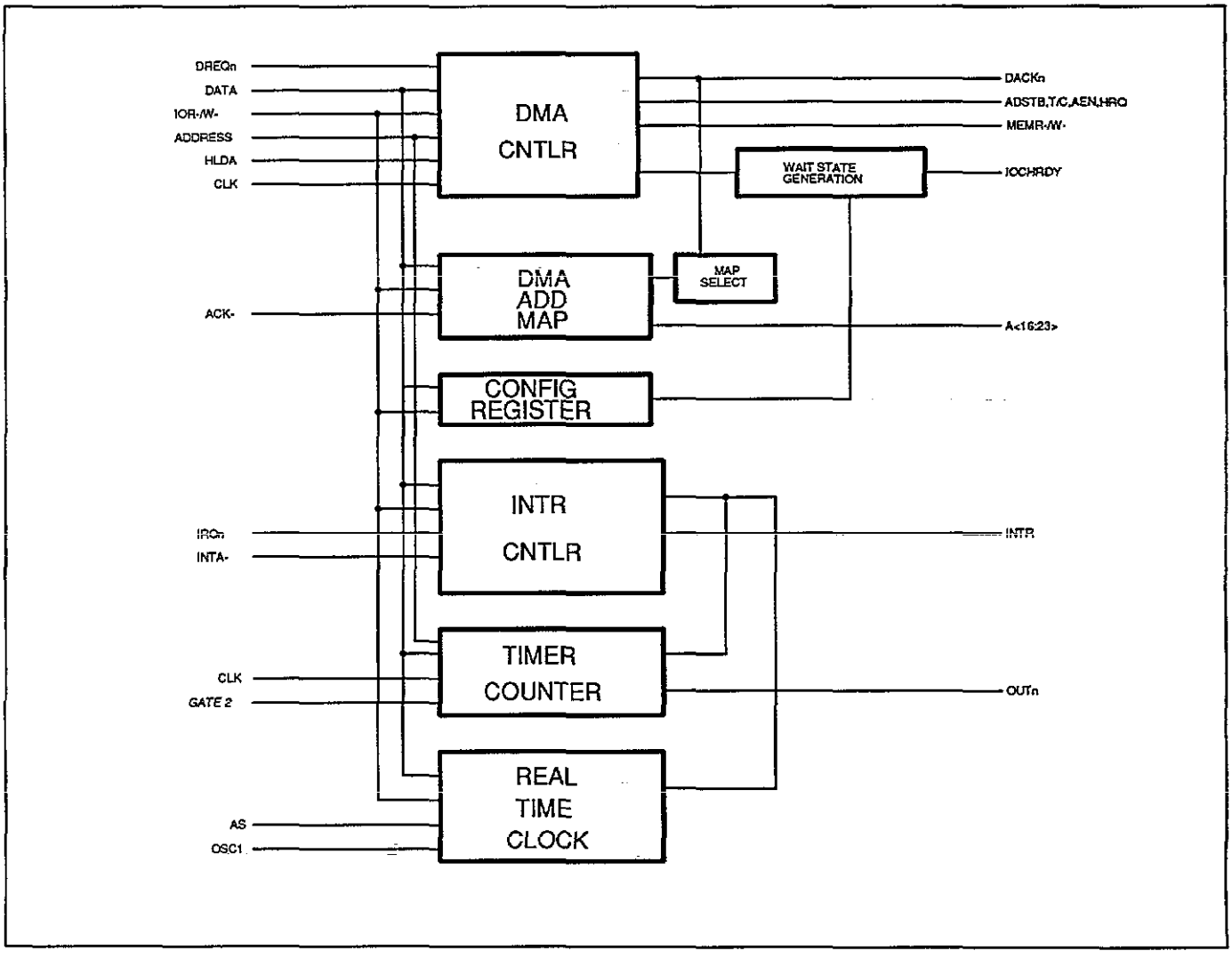
which is independent from the other clock inputs to the divide. Counter 0 is connected to Interrupt 0 of INTC1. It is intended as a multi-level interrupt to the system for such tasks as time keeping, and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third channel (Counter 2) is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

A Real Time Clock (RTC) is included in the 82C316 for maintaining the time and date. This subsystem also contains 114 bytes of RAM in addition to the Clock/Calendar. The Clock/Calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

To interconnect and control all these major subsystems, a top level control section is employed which is divided into subsystems for purposes of discussion.

The first section is the Clock and Wait State Control section. This subsystem controls the generation of DMA wait states and the negation of IOCHRDY (if

Figure 4-3. Integrated Peripheral Controller Block Diagram



programmed to do so) during CPU access of the device. The last subsystem is the Top Level Decode.

In order to accommodate over 200 registers in the 82C316 and maintain I/O decode compatibility with the IBM PC/AT, a multi-level decode scheme is employed. The Top Level Decode subsystem performs the function of generating enables to the various subsystems. Control and direction of the XD<0:7> data bus buffers are also handled by this subsystem.

Top Level Decode

The 82C316 Top Level Decode provides 8 separate enables to various subsystems of the device. Table 4-3 contains a truth table of the Top Level Decode. The enabling of the 82C316 XD<0:7> output buffers is also controlled by this section. The output buffers are enabled whenever an enable is generated to an internal subsystem and the IOR- signal is asserted.

The decode is enabled by three signals: AEN, XA9 and XA8. To enable any internal device ACK must be "1" and both XA9 and XA8 must be "0."

The decode scheme employed in the 82C316 is designed to comply with the IBM PC/AT requirements and is more fully decoded. If the user wishes to take advantage of the areas which are unused by inserting additional peripherals in the I/O map, he may do so since the subsystems in the 82C316 will not respond to the unused address spaces established by the Top Level Decode. The extra peripherals may be tied directly to the <XD0:7> data lines since the 82C316 output buffers are not enabled unless an internal subsystem is enabled.

Table 4-3. *IPC Internal Decode(023H) (Index 01H)*

AEN-	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address Range	Selected Device
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA1
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	X	X	X	X	070-071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DAMPAGE
1	0	0	1	0	1	X	X	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	X	X	X	X	X	X	X	X	X	X	DISABLED	
X	1	X	X	X	X	X	X	X	X	X	DISABLED	
X	X	1	X	X	X	X	X	X	X	X	DISABLED	

Clock and Wait State Control

The Clock and Wait Sate Control subsystem performs four functions, control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the Configuration Register located at address 023H.

Writing and reading this register is accomplished by first writing an 01H to location 022H to select the 82C316 Configuration Register, and then performing either a read or write to location 023H.

Table 4-4. Clock/Wait State Control Register 01H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

RW1 - RW0: When the higher speed CPU's are accessing the 82C316, the cycle can be extended by programming up to four wait states into the Configuration Register. This causes the 82C316 to assert a not ready condition on IOCHRDY (low) whenever a valid decode from the Top Level Decode is detected and either IOR- or IOW- is asserted. IOCHRDY remains low for the number of wait states programmed into the Clock/Wait State Control Register bits 6 and 7.

Table 4-5. Read/Write Cycle Wait State

RW1	RW0	Read/Write Cycle Wait States
0	0	1
0	1	3
1	0	3
1	1	4

Wait states are in increments of one SCLK cycle and are not affected by the DMA Clock Divider.

16W1 - 16W0: Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles. This allows the user to tailor the DMA cycle more closely to the application.

Table 4-6. 16-Bit DMA Wait States

16W1	16W0	16-bit DMA Wait States
0	0	1
0	1	3
1	0	3
1	1	4

8W1 - 8W0: Wait states may be inserted in 8-bit DMA cycles by programming these two bits in the Configuration Register.

Table 4-7. 8-Bit DMA Wait States

8W1	8W0	8-bit DMA Wait States
0	0	1
0	1	3
1	0	3
1	1	4

Further control of the cycle length is available through the use of the IOCHRDY pin on the 82C316. During DMA, this pin is used as an input to the wait state generation logic to extend the cycle if necessary. This input is driven low (0) by the peripheral to extend the cycle. The cycle can then be completed by releasing IOCHRDY and allowing it to return high (1).

EMR: This bit enables the extended DMA MEMR- function. Normally, the assertion of DMA MEMR is delayed one clock cycle later than IOR- in the IBM PC/AT implementation. This may not be desirable in some systems. A "1" programmed into this bit position starts DMAMEMR- at the same time as IOR-.

CLK: This bit allows the user to insert a divider between the DMA Controller subsystems and the SCLK input pin, or connect the two directly. When this bit position contains a "0," the SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems. A "1" in this position bypasses the divider and uses the SCLK input directly. Whenever the state of this bit is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

The Clock/Wait State Control Register contents are preloaded by Reset 4 to an initial value of 0C0 hex. This value establishes a default which is IBM PC/AT compatible and corresponds to:

Read/Write cycles 4 wait states
16-bit DMA transfers 1 wait state
8-bit DMA transfers 1 wait state
DMA MEMR- delayed 1 DMA clock cycle later than IOR-
DMA clock is equal to SCLK/2

DMA Functional Description

The equivalent of two 8237A DMA Controllers is implemented in the 82C316. Each controller is a four channel DMA device which generates the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. This allows high speed information transfer with little CPU intervention.

The two DMA Controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection to the two DMA devices; thereby maintaining IBM PC/AT compatibility.

DMA cycle length control is provided internally in the 82C316 allowing independent control for both 8-bit and 16-bit cycles. This is done throughout

the programmable registers which can extend command signals or insert wait states.

Each DMA Channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA to transfer blocks as large as 65536 words. The register associated with each counter allows the channel to reinitialize without reprogramming. The following descriptions of the DMA subsystem pertains to both DMA1 and DMA2 unless otherwise noted.

DMA Operation

During normal operation of the 82C316, the DMA subsystem is either in idle condition, program condition, or active condition. In the idle condition, the DMA controller is executing cycles consisting of only one state. The idle state SI is the default condition. The DMA remains in this condition unless the device has been initialized and one of the DMA requests is active; or unless the CPU attempts to access one of the internal registers.

When a DMA request becomes active, the device enters the active condition and issues a hold request to the system. Once in the active condition, the 82C316 generates the necessary memory addresses and command signals to accomplish a memory-to-I/O, I/O-to-memory, or a memory-to-memory transfer. Memory-to-I/O and I/O-to-memory transfers take place in one cycle while memory-to-memory transfers between memory and I/O. Data is presented on the system bus by either memory or the requesting device and the transfer is completed in one cycle. Memory-to-memory transfers, however, require the DMA to store data from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

During transfers between memory and I/O, two commands are activated during the same cycle. In the case of a memory-to-I/O transfer, the 82C316 asserts both DMAMEMR- and IOW- allowing data to be transferred directly to the requesting device from memory. Note that the 82C316 does not latch data from, or drive data out, on this type of cycle.

The number of clock cycles required to transfer a word of data may be varied by programming the DMA, or may be optionally extended by the peripheral device. During an active cycle, the DMA sequences through a series of states. Each state is one DMA clock cycle length. The number of states in a cycle varies depending on how the device is programmed, and what type of cycle is being performed. The states are labeled S0-S4 and are explained in detail in the section titled *Active Condition*.

Idle Condition

When no device is requesting service, the DMA is in an idle condition which maintains the state machine in the SI state. During this time, the 82C316 samples the DREQ input pins every clock cycle. The internal select from the top level decoder and HLDA are also sampled at this same time to determine if the CPU is attempting to access the internal registers. When either of the above situations occurs, the DMA exits the idle condition. Note that the program

condition has priority over the active condition since a CPU cycle has already started.

Program Condition

The program condition is entered whenever HLDA is inactive and the internal select is active. The internal select is derived from the top level decode described previously. During this time, address lines XA<0:3> become inputs if DMA1 is selected, or XA<1:4> become inputs if DMA2 is selected. Note that when DMA2 is selected, XA0 is ignored. These address inputs are used to select the DMA controller registers which are to be read or written. Due to the large number of internal registers in the DMA subsystem, and internal flip-flop is used to supplement the addressing of the count and address registers. This bit is used to select between the high and low bytes of these registers. The flip-flop toggles each time a read or write occurs to any of the word count or address registers in the DMA. This internal flip-flop can be cleared by a hardware RESET or a master clear command. The internal flip-flop can also be set or cleared by the CPU issuing the appropriate command.

Special commands are supported by the DMA subsystem in the program condition to control the device. These commands do not make use of the d ta but, but are derived from a set of addresses, the internal select, and the IOW- or IOR-. These commands are: Master Clear, Clear Register, Clear Mode Register Counter, Set and Clear Byte Pointer Flip-Flop.

The 82C316 enables programming whenever HLDA has been inactive for one DMA clock cycle. It is the responsibility of the system to ensure that programming and HLDA are mutually exclusive. Erratic operation of the 82C316 can occur if a request for service occurs on an unmasked channel which is being programmed. The channel should be masked, or the DMA disabled, to prevent the 82C316 attempting to service a device with a channel which is partially programmed.

Active Condition

The 82C316 DMA subsystem enters the active condition whenever a software request occurs, or a DMA request on an unmasked channel occurs and the device is not in the program condition. The 82C316 then begins a DMA transfer cycle.

In a read cycle, for example, after receiving a DREQ, the 82C316 issues an HRQ to the system. Until a HLDA is returned, the DMA remains in an idle condition. On the next clock cycle, the DMA exits idle condition and enters the S0 state. During S0, the device resolves priority and issues DACK on the highest priority channel requesting service. The DMA then proceeds to state S1 where the multiplexed addresses are output and latched. State S2 is then entered; at which time the 82C316 asserts DMA MEMR-. The device then makes the transition into S3 where the IOW- command is asserted. The 82C316 then remains in S3 until the wait state counter has decremented to zero and IOCHRDY is true. Note that at least one additional S3 will occur unless Compressed Timing is selected. Once a ready condition is detected, the DMA enters S4 where both commands are de-asserted. In Burst Mode and Demand

Mode, subsequent cycles begin in S2 unless the intermediate addresses require updating. In these subsequent cycles, the lower addresses are changed in S2. The DMA can be programmed on a channel by channel basis to operate in one of four modes. The four modes are as follows:

Single Transfer Mode: This mode directs the DMA to execute only one transfer cycle at a time. DREQ must be held active until DACK becomes active. If DREQ is held active throughout the cycle, the 82C316 de-asserts HRQ and releases the bus once the transfer is complete. After HLDA has gone inactive, the 82C316 again asserts HRQ and executes another cycle on the same channel unless a request from a higher priority channel has been received. In this mode, the CPU is ensured of being allowed to execute at least one bus cycle between transfers.

Following each transfer, the word count is decremented and the address is incremented or decremented. When the word count decrements from 0000H to FFFFH, the terminal count bit in the status register is set and a T/C pulse is generaed. If the auto-initialization option has been enabled, the channel reinitializes itself. If auto-initialize is not selected, the DMA sets the DMA requests bit mask and suspends transferring on the channel.

Block Transfer Mode: When block transfer mode is selected, the 82C316 begins transfer in response to either a DREQ or a software request. It continues until a terminal count (FFFFH) is reached. When the terminal count is reached, the T/C is pulsed and the status register terminal count bit is set. In this mode, DREQ need only be held active until DACK is asserted. Auto-initialization is also operational in this mode.

Demand Transfer Mode: In demand transfer mode, the DMA begins transfers in response to the assertion of DREQ and continues until either the terminal count is reached or DREQ becomes inactive. This mode is normally used for peripherals which have limited buffering availability. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. The peripheral may then re-establish service by again asserting DREQ. During idle periods between transfers, the CPU is released to operate and can monitor the operation by reading intermediate values from the address and word count registers. Once DREQ has been de-asserted, higher priority channels are allowed to intervene. Reaching terminal count results in the generation of a T/C pulse, the setting of the terminal bit in the status register, and auto-initialization (if enabled).

Cascade Mode: This mode is used to interconnect more than one DMA controller, to extend the number of DMA channels while preserving the priority chain. In cascade mode, the master DMA controller does not generate address or control signals. The DREQ and DACK signals of the master are used to interface the HRQ and HLDA signals of the slave DMA devices. Once the master has received an HLDA from the CPU in response to a DREQ caused by the HRQ from a slave DMA controller, the master DMA controller ignores all inputs except HLDA from the CPU and DREQ on the active channel. This prevents conflicts between the DMA devices.

Figure 4-4 shows the cascade interconnection for two levels of DMA devices. Note that Channel 0 of DMA2 is internally connected for cascade mode to

Table 4-1. *Address Buffer Function*

HLDA	ATEN	REF	MSTR	Mode	Action
0	1	1	1	non-AT	All buses are tri-stated in this mode
0	0	1	1	AT	The SA bus is driven by the A bus
0	1	0	1	REFRESH	A<16:2> are disabled, A<23:17> output the value of the Refresh page register, SA<19:12> are set to '0,' and SA<11:0> output the vlaue of the DMA counter
1	1	1	0	Master	The SA bus drives the A bus while A<23:17> is tri-stated
1	1	0	0	Master-REFRESH	The A bus is disabled; SA<19:12> are set to '0,' and SA<11:0> output the value of the DMA counter
1	1	1	1	DMA	The 82C316 drives the A bus and the SA bus

Address Decode

The 82C316 decodes I/O addresses for port B logic, 8042 keyboard controller, NMI register, and all ports in 82C316. The signals IO2XCS- and 8042CS provide the address decoding for the keyboard controller. The IO2XCS- output, in conjunction with XA<0:1>, are used to access index registers 22H and 23H. The 8042CS- is an I/O decode of addresses 60H and 64H.

Normally, I/O decode in 82C316 uses address range A0 through A9. The decode does not include A10-A15. When this bit is set to 0, the I/O decode does not include A10-A15 for decoding. If this bit is set to 1, A10 to A15 are included for I/O addresses decode. This is the extended I/O decode mode. For example, when extended I/O decode is disabled, and for I/O address of 64, the I/O decode will be active for address 064 and F64 (the addresses A10-A15 are neglected). When extended I/O decode is enabled, the I/O decode will be active for I/O address 64 only and AT cycle is performed for I/O address F64.

Programmable Chipselects

There are three programmable I/O decode chipselects available in the 82C316, that eliminate the need for extra circuitry for I/O decodes. They are PGMCS1-, PGMCS2-, and PGMCS3-. Three programmable registers are allocated for each I/O space to decode an address or range of addresses (up to sixteen bytes) and set the access rights. The decoded range can be programmed for read only, write only, and read/write by setting bits 4 and 5 of the Enable registers (REG<73>, REG<76>, and REG<79>. The 82C316 generates a chipselect (PGMCS1-, PGMCS2-, and PGMCS3-) based on the addresses and the access rights set on configuration registers REG71H thru REG79H. The programmable chip selects work for master cycles also.

Port B and NMI Logic

The 82C316 provides access to Port B defined for the PC/AT as shown in Table 4-2. The NMI (non-maskable interrupts) circuitry latches and enables the I/O channel check and parity error conditions. If the corresponding NMIs are enabled in port B, a non-maskable interrupt is generated to the CPU and the source of the NMI is recorded in port B. Reading port B indicates the source of the error condition (CHK and PCK). The master enable for NMI generation, as defined for PC/AT system at system I/O port 70H bit 7, is implemented in the 82C316. If this bit is set to "1," NMI generation is disabled. If set to "0," it is enabled.

Table 4-2. Port B Bit Definition

Address	Bit	Function	Description
61H		Port B Register	
	7	Read only	PCK - System memory parity check
	6	Read only	CHK - I/O channel check
	5	Read only	T2O - Timer 2 out
	4	Read only	RFD - Refresh detect
	3	Read write	EIC - Enable I/O channel check
	2	Read write	ERP - Enable system memory parity check
	1	Read write	SPK - Speaker Data
	0	Read write	T2G - Timer 2 Gate Speaker

The 82C316 also accepts an NMI due to power fail (PFAIL), READY timeout and from the Power Control Unit (PCU). The PCU and PFAIL NMI are combined onto one pin since the PCU can supply the PFAIL interrupt. REG26<4> and REG26<2> are used to enable the NMI sourced from PCU and READY timeout respectively. REG26<3> and REG26<0> indicates the source of the NMI.

80387DX RESET Logic

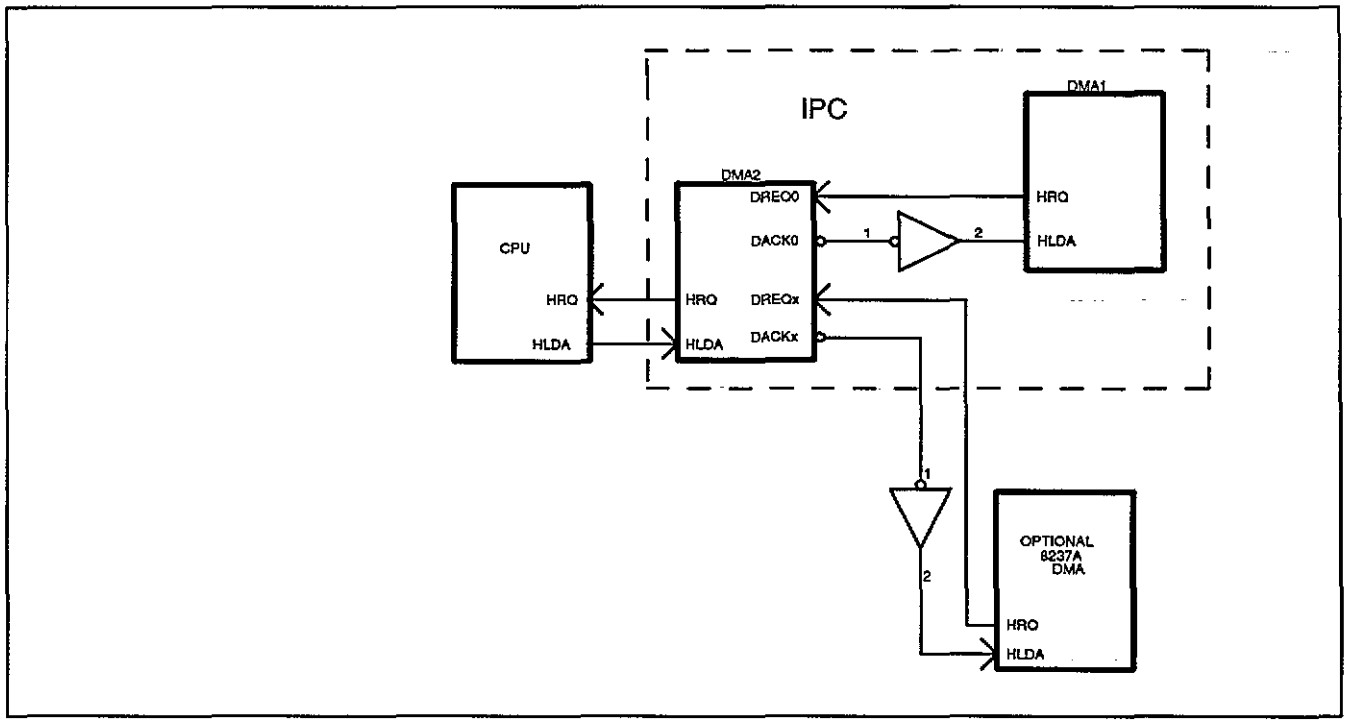
The 82C316 provides the necessary logic for resetting the 80387 coprocessor. The 80387 coprocessor reset (RES387) is asserted after a RESET3 from 82C311 or an Out command to port F1H is detected and held active for at least 128 CLK2 cycles. The RES387 output is directly connected to the 80387 RESETIN input.

After an Out command to port F0H or F1H, or during a RESET3, the 82C316 generates INTCLR output. The INTCLR output is connected to the INTCLR input of the 82C315 and is used to clear the latched Math coprocessor BUSY- signal (the latch BUSY- signal is the coprocessor BUSY- signal latched on ERROR- due to coprocessor unmasked exception).

Figure 4-2 shows the timing sequence for the 387 reset (387RST) output.

DMA1. Additional devices can be cascaded to the available channels in either DMA1 or DMA2 since cascade is not limited to two levels of DMA controllers.

Figure 4-4. *Cascade Mode Interconnect*



When programming cascaded controllers, begin with the device which is actually generating HRQ to the system (first level device), and then proceed to the second level devices. RESET 4 causes the DACK outputs to become active low and are placed in the inactive state. To allow the internal cascade between DMA1 and DMA2 to function correctly, the active low state of DACK should not be modified. This is because the 82C316 has an inverter between DACK0 of DMA2 and the HLDA of DMA1. The first level device's DMA request mask bit prevents second level cascaded devices from generating unwanted hold requests during the initialization process.

DMA Transfers

Four types of transfer modes are provided in the 82C316 DMA subsystem. These transfer types are as follows.

Read Transfer: Read transfers move data from memory to an I/O device by generating the memory address and asserting DMA MEMR- and IOW- during the same cycle.

Write Transfer: Write transfers move data from an I/O device to memory by generating the memory address and asserting IOR- and DMA MEMW.

Memory-to-Memory Transfer: The memory-to-memory trasfer is used to move a block of memory from one location in memory to another. DMA

Channels 0 and 1 may be programmed to operate as memory-to-memory channels by setting bit 1 in the Command register. Once programmed to perform a memory-to-memory transfer, the process can be started by generating either a software or an external request to Channel 0. Once the transfer is initiated, Channel 0 provides the address for the source block during the memory read portiion of the cycle. Channel 1 generates the address for the memory write cycle. During the read cycle, a byte of data is latched in the internal Temporary register of the 82C316. The contents of this register are then output on the XD<0:7> data lines during the write portion of the cycle and subsequently written to memory. Channel 0 may be programmed to maintain the same source address on every cycle. This allows the CPU to initialize large blocks of memory with the same value. The 82C316 continues performing transfer cycles until Channel 1 reaches terminal count.

Verify Transfer: The verify transfer is a pseudo-transfer useful for diagnostics. In this type of transfer, the DMA operates as if it is performing a read or write transfer by generating HRQ addresses and DACK; but will do so without asserting a command signal. Since no transfer actually takes place, IOCHRDY is ignored during verify transfer cycles.

Auto-initialization

Each of the four DMA channel mode registers contains a bit which causes the channel to reinitialize after reaching terminal count. During this process, referred to as auto-initialization, the base address and base word count registers, which were originally written by the CPU, are reloaded into the current address and current word count registers (both the base and current registers are loaded during a CPU write cycle). The base register remains unchanged during DMA active cycles and can only be changed by the CPU. If the channel has been programmed to auto-initialize, the request mask bit will not be set upon reaching terminal count. This allows the DMA to continue operation without CPU intervention.

During memory-to-memory transfers the word count registers of both Channel 0 and Channel 1 must be programmed with the same starting value for full auto-initialization. If Channel 0 reaches terminal count before Channel 1, then Channel 0 will reload the starting address and word count and continue transferring data from the beginning of the source block. Should Channel 1 reach terminal count first, it will reload the current registers and Channel 0 will remain uninitialized.

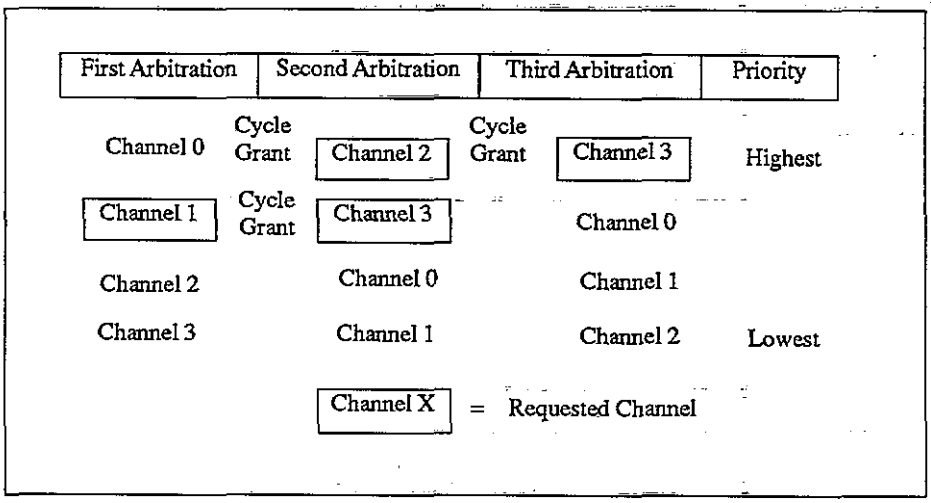
DREQ Priority

The 82C316 supports two schemes for establishing DREQ priority. The first is fixed priority which assigns priority based on channel position. In this method, Channel 0 is assigned highest priority. Priority assignment then progresses downward through the channels in order; with Channel 3 receiving the lowest priority.

The second type of priority assignment is rotating priority. In this scheme, the ordering of priority from Channel 0 to Channel 3 is maintained, but the actual assignment of priority changes. The channel most recently serviced is assigned the lowest priority and, since the order of priority assignment remains fixed, the

remaining three channels rotate accordingly. The rotating priority assignment is illustrated in Figure 4-5.

Figure 4-5. Rotating Priority Scheme



In instances where multiple requests occur at the same time, the 82C316 issues an HRQ but does not freeze the priority logic until HLDA is returned. Once HLDA becomes active, the priority logic is frozen and DACK is asserted on the highest requesting channel. Priority is not re-evaluated until HLDA has been deactivated.

Address Generation

Eight intermediate bits of the address are multiplexed onto the data lines during active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During state S1, the intermediate addresses are output on data lines XD<0:7>. These addresses should be externally latched and used to drive the system address bus. Since DMA1 is used to transfer 8-bit data and DMA2 transfers 16-bit data, a one bit skew occurs in the intermediate address fields. DMA1 therefore outputs addresses A<8:15> on the data bus at this time; whereas DMA2 outputs A<9:16>. A separate set of latch and enable signals are provided for both DMA1 and DMA2 to accommodate the address skew.

The DMA page register is a set of sixteen 8-bit registers in the 82C316 used to generate the high order address during DMA cycles. Only eight of the registers are actually used, but all sixteen were included to maintain IBM PC/AT compatibility. Each DMA channel has a register associated with it, except Channel 0 of DMA2 which is used for internal cascading to DMA1. Assignment of each of these registers is shown in Table 4-8 along with its read/write address.

Table 4-8. DMA Address Extension Map

Address	Register Function
080H	Unused
081H	8-bit DMA Channel 2 (DACK2)
082H	8-bit DMA Channel 3 (DACK3)
083H	8-bit DMA Channel 1 (DACK1)
084H	Unused
085H	Unused
086H	Unused
087H	8-bit DMA Channel 0 (DACK0)
088H	Unused
089H	16-bit DMA Channel 2 (DACK6)
08AH	16-bit DMA Channel 3 (DACK7)
08BH	16-bit DMA Channel 1 (DACK5)
08CH	Unused
08DH	Unused
08EH	Unused
08FH	Refresh Cycle

During demand and block transfers, the DMA subsystem generates multiply sequential transfers. For most of these transfers, the information in the external address latches remains the same; eliminating the need to be relatched. Since the need to update the latches occurs only when a carry or borrow from the lower 8-bits of the address counter exists, the 82C316 only updates the latch contents when necessary. The DMA therefore only executes S1 cycles when necessary; resulting in an overall through-put improvement.

Compressed Timing

The DMA subsystem in the 82C316 can be programmed to transfer a word in as few as 3 DMA clock cycles. The normal DMA cycle consists of three states: S2, S3, and S4 (this assumes demand or block transfer mode). Normal transfers require 4 DMA clock cycles since S3 is executed twice due to the 1 wait state insertion. In systems capable of supporting high through-put, the DMA can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generating the address and asserting both commands. One S3 cycle is executed and the cycle terminates in S4. If compressed timing is selected, TC is output in S2 and S1 cycles are executed as necessary to update the address latch. Note that compressed timing is not allowed for memory-to-memory transfers.

Register Description

Current Address Register

Each DMA channel has a 16-bit current address register to hold the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If auto-initialization is selected,

this register reloads from the base address register upon reaching terminal count in the current word count register. Channel 0 can be prevented from incrementing or decrementing by setting the address hold bit in the command register.

Current Word Count Register

Each channel has a current word count register to determine the number of transfers to perform. The actual number of transfers performed is one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFH. When this roll-over occurs, the 82C316 generates TC, suspends operation on that channel, and sets the appropriate request mask bit or auto-initialize and continues.

Base Word Count Register

This register preserves the initial value of the current word count register. It is also a write only register which is loaded by writing the current word count register. This register is loaded in the current word count register during auto-initialization.

Command Register

This register controls the overall operation of a DMA subsystem. The register can be read or written by the CPU and is cleared by either RESET 4 or a master clear command.

Table 4-9. Command Register

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK: DACK active level is determined by bit 7. Programming a 1 in this bit position makes DACK an active high signal.

DRQ: DREQ active level is determined by bit 6. Writing a 1 in this bit position causes DREQ to become active low.

EW: Extended write is enabled by writing a 1 to bit 5; causing the write commands to be aserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.

RP: Writing a 1 to bit 4 causes the 82C316 to utilize a rotating priority scheme for honoring DMA requests. The default condition is fixed priority.

CT: Compressed timing is enabled by writing a 1 to bit 3 of this register. The default 0 condition causes the DMA to operate with normal timing.

CD: Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem (DMA1 or DMA2). This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles from occuring.

AH: Writing a 1 to bit 1 enables the address hold feature in Channel 0 when performing memory-to-memory transfers.

M-M: A 1 in the bit 0 position enables Channel 0 and Channel 1 to be used for memory-to-memory transfers.

Mode Register

Each DMA channel has a mode register associated with it. All four mode registers reside at the same I/O address. Bits 0 and 1 of the write mode register determines which channel's mode register is written. The remaining six bits control the mode of the selected channel. Each channel's mode register can be read by sequentially reading the mode register location. A clear mode register counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operation, bits 0 and 1 will both be a 1.

Table 4-10. Mode Register

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

M1-M0: Mode selection for each channel is accomplished by bits 6 and 7.

Table 4-11. Mode Selection

M1	M0	Mode
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

DEC: Determines the direction of the address counter. A one in bit 5 decrements the address after each transfer. A zero increments the address after each transfer.

A1: The auto-initialization function is enabled by writing a 1 in bit 4 of the mode register.

TT1-TT0: Bits 2 and 3 control the type of transfer to be performed.

Table 4-12. Transfer Select

TT1	TT0	Type
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Illegal

CS1-CS0: The channel select bits 1 and 0 determine which channel's mode register will be written. Reading the mode register results in bit 1 and 0 to both be ones.

Table 4-13. Channel Select

CS1	CS0	Channel
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

Request Register

This is a four bit register used to generate software requests (DMA service can be requested either externally or under software control). Request register bits can be set or cleared independently of the CPU. The request mask has no effect on software generated requests. All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones. All four request bits are clear to zero by RESET4.

Table 4-14. Request Register

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	RB	RS1	RS0

(write operation)

RB: The request bit is set by writing a 1 to bit 2. RS1-RS0 select which bit (channel) is to be manipulated.

RS<0:1>: Channel select 0 and 1 determine which channel's mode register will be written. Reading back to the mode register results in bits 0 and 1 to both be ones.

Table 4-15. Channel Select

RS1	RS0	Channel
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

The format for the request register read operation is shown as follows:

Table 4-16. Request Register Read

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	RC3	RC2	RCD1	RC0

(read operation)

RC<0:3>: During a request register read, the state of the request bit associated with each channel is returned in bits 0 through 3 of the byte. The bit position corresponds to the channel number.

Request Mask Register

The request mask register is a set of four bits used to inhibit external DMA requests from generating transfer cycles. This register can be programmed in two ways. Each channel can be independently masked by writing to the write single mask bit location. The data format for this operation is shown as follows:

Table 4-17. Request Mask Register

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	MB	MS1	MS0

(set/reset operation)

MD: Bit 2 sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a 1 in this bit position sets the mask, inhibiting external requests.

MS<0:1>: These two bits select the specific mask bit which is to be set or reset.

Table 4-18. Channel Select

MCS1	MS0	Channel
0	0	Channel 0 Select
0	1	Channel 1 Select
1	0	Channel 2 Select
1	1	Channel 3 Select

Alternatively, all four mask bits can be programmed in one operation by writing to the write all masks bits address. Data format for this and read all mask bits function is shown as follows:

Table 4-19. Data Format for Mask Bits

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	MB3	MB2	MB1	MB0

MB<0:3>: Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit.

All four mask bits are set following a RESET4 or a master clear command. Individual channel mask bits will be set as a result of terminal count being reached, if auto-initialized is disabled. The entire register can be cleared, enabling all four channels, by performing a clear mask register operation.

Status Register

The status of all four channels can be determined by reading the status register. Information is available to determine if a channel has reached terminal count and whether an external service request is pending. Bit 0-3 of this register are cleared by RESET4, master clear or each time a status read takes place. Bits 4-7 are cleared by RESET4, master clear or the pending request being deasserted. Bits 4-7 are not affected by the state of the mask register bits. The channel number corresponds to the bit position.

Table 4-20. Status Register

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
DRQ3	DRQ2	DRQ1	DRQ0	TC3	TC2	TC1	TC0

(read only register)

Temporary Register

The temporary register is used as a temporary holding register for data during memory-to-memory transfers. The register is loaded during the first cycle of a memory-to-memory transfer from XD<0:7>. During the second cycle of the transfer, the data in the temporary register is output on the XD<0:7> pins. Data from the last memory-to-memory transfer remains in the register unless a RESET4 or master clear occurs.

Special Commands

Five special commands are provided to make the task of programming the device easier. These commands are activated as a result of a specific address and assertion of either an IOR- or IOW-. Information on the data lines is ignored by the 82C316 whenever an IOW- activated command is issued, thus data returned on IOR- activated commands is invalid.

Clear Byte Pointer Flip-Flop: This command is normally executed prior to reading or writing to the address or word count register. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write the register bytes in correct sequence.

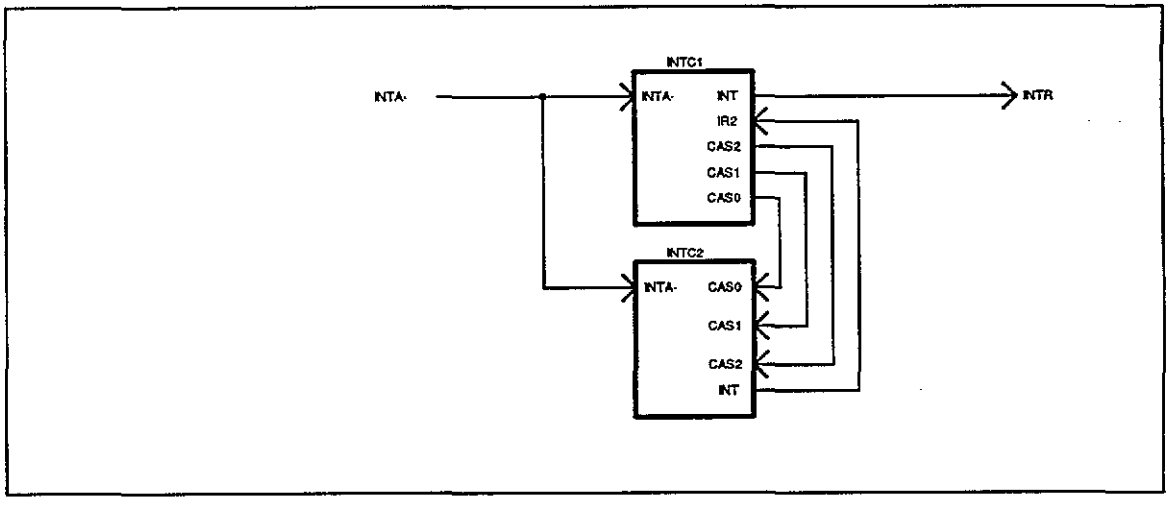
Set Byte Pointer Flip-Flop: Setting the byte pointer flip-flop allows the CPU to adjust the pointer to the high byte of an address or word count register.

Master Clear: This command has the same effect as a hardware RESET4. The command register, status register, request register, temporary register, mode register counter, and byte pointer flip-flop are cleared and the request mask register is set. Immediately following master clear or RESET4, the DMA begins the idle condition.

Clear Request Mask Register: This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

Clear Mode Register Counter: In order to allow access to four mode registers while only using one address, an additional counter is used. After clearing te counter, all four mode registers may be read by doing successive reads to the read mode register address. The order in which the register is read is Channel 0 first, Channel 3 last.

Figure 4-6. Internal Cascade Interconnect

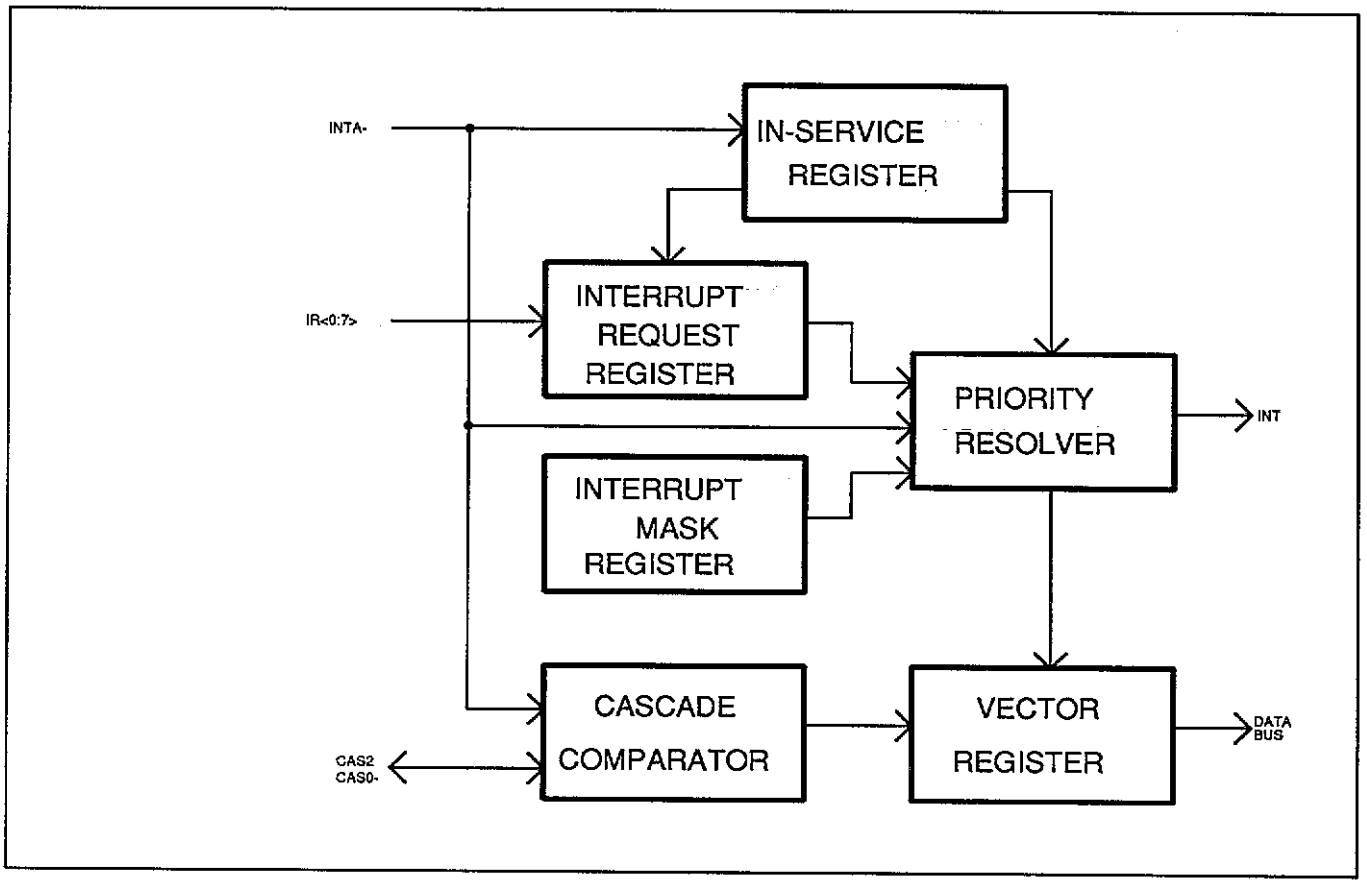


Interrupt Controller Functional Description

The programmable interrupt controllers in the 82C316 function as a system wide interrupt manager in an APX86 system. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided, which can be reconfigured at any time during system operation, allowing the complete interrupt subsystem to be restructured, based on the system.

Figure 4-7. Interrupt Controller Block Diagram



Overview

Two interrupt controllers, INTC1 and INTC2, are included in the 82C316. Each of the interrupt controllers is equivalent to an 8259A device operating in !APX86 mode. The two devices are interconnected and must be programmed to operate in cascade mode (see Figure 4-6) for proper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and is configured for master operation in cascade mode. INTC2 is a slave device and is located at 0A0H-0A1H. The interrupt request output signal from INTC2 is internally connected to the interrupt request input Channel 2 IR20 of INTC1. The address decoding and cascade interconnection matches that of the IBM PC/AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of time 0 in the counter/timer subsystem is connected to Channel 0 of INTC1. Interrupt request from the real time clock is connected to Channel 0 of INTC2. Table 4-21 lists the sixteen interrupt channels and their interrupt request source.

Table 4-21. Interrupt Request Source

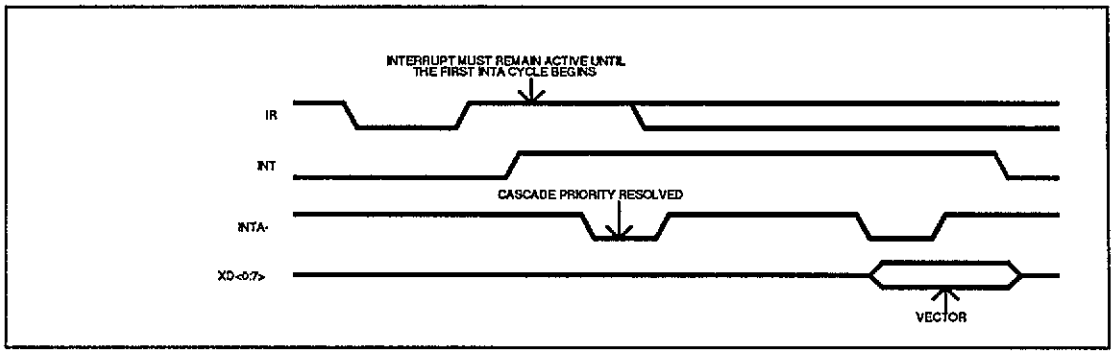
Controller Number	Channel Number	Interrupt Request Source
INTC1	IR0	Counter/Timer Out 0
INTC1	IR1	IRQ1 Input Pin
INTC1	IR2	INTC2 Cascade Interrupt
INTC1	IR3	IRQ3 Input Pin
INTC1	IR4	IRQ4 Input Pin
INTC1	IR5	IRQ5 Input Pin
INTC1	IR6	IRQ6 Input Pin
INTC1	IR7	IRQ7 Input Pin
INTC2	IR0	Real Time Clock IRQ
INTC2	IR1	IRQ9 Input Pin
INTC2	IR2	IRQ10 Input Pin
INTC2	IR3	IRQ11 Input Pin
INTC2	IR4	IRQ12 Input Pin
INTC2	IR5	IRQ13 Input Pin
INTC2	IR6	IRQ14 Input Pin
INTC2	IR7	IRQ15 Input Pin

Description of the interrupt subsystem pertains to both INTC1 and INTC2 unless otherwise noted. Wherever register addresses are used, the address for the INTC1 register is listed first and the address for the INTC2 register follows in parenthesis. For example 020H (0A0H).

Controller Operation

Figure 4-7 is a block diagram of the major elements in the interrupt controller. The interrupt request register (IRR) is used to store requests from all of the channels requesting service. Interrupt request register bits are labeled using the channel name IR<0:7>. The in-service register (ISR) contains all the channels currently being serviced (more than one channel can be in service at a time). In-service register bits are labeled IS<0:7>. The interrupt mask register (IMR) allows the CPU to disable any or all of the interrupt channels. The priority resolver evaluates inputs from the registers discussed earlier, issues an interrupt request, and latches the corresponding bit into the in-service register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the cascade buffer/comparator with a three bit ID code previously written. If a match occurs in the slave controller, it will generate an interrupt vector. The contents of the vector register are used to provide the CPU with an interrupt vector during interrupt acknowledge (INTA) cycles.

Figure 4-8. Interrupt Sequence



Interrupt Sequence

The 82C316 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device. The indirect jump is based on a vector which is provided by the 82C316 on the second of two CPU generated INTA cycles (the first INTA cycle is used for resolving priority and the second cycle is for transferring the vector to the CPU). The events which occur during an interrupt sequence are as follows:

1. One or more of the interrupt requests (IR7-IR0) becomes active, setting the corresponding IRR bit(s).
2. The interrupt controller resolves priority based on the state of the IRR, IMR and ISR and asserts the INTR output, if appropriate.
3. The CPU accepts the interrupt and responds with an INTA cycle.
4. During the first INTA cycle, the highest priority ISR bit is set and the corresponding IRR bit is cleared. The internal cascade address is generated and XD<0:7> outputs remain tri-stated.
5. The CPU will execute a second INTA cycle, during which the 82C316 will drive an 8-bit vector onto the data pins XD<0:7>, which is in turn latched by the CPU. The format of this vector is shown in Table 4-22. Note that V<3:7> in Table 4-22 is programmable by writing to initialization control word 2 (see the section titled *Initialization Command Words*).

Table 4-22. Interrupt Vector Byte

IRQ	D7	D6	D5	D4	D3	D2	D1	D0
IRQ7	V7	V6	V5	V4	V3	1	1	1
IRQ6	V7	V6	V5	V4	V3	1	1	0
IRQ5	V7	V6	V5	V4	V3	1	0	1
IRQ4	V7	V6	V5	V4	V3	1	0	0
IRQ3	V7	V6	V5	V4	V3	0	1	1
IRQ2	V7	V6	V5	V4	V3	0	1	0
IRQ1	V7	V6	V5	V4	V3	0	0	1
IRQ0	V7	V6	V5	V4	V3	0	0	0

6. At the end of the second INTA cycle, the ISR bit will be cleared if the automatic end of interrupt mode is selected (see the section titled *End of Interrupt*). Otherwise, the ISR bit must be cleared by an End of Interrupt (EOI command from the CPU at the end of the interrupt service routine).

If no interrupt request is present at the beginning of the first INTA cycle (i.e., a spurious interrupt), INTC1 will issue an interrupt level 7 vector during the second INTA cycle.

End of Interrupt

EOI is defined as the condition which causes an ISR bit to be cleared. Determination of which ISR bit is to be cleared can be done by a CPU command (specific EOI) or, the priority resolver can be instructed to clear the highest priority ISR bit (non-specific EOI).

The 82C316 can determine the correct ISR bit to reset when operated in modes which do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in special mask mode by an IMR bit, will not be clear by a non-specific EOI command. The interrupt controller can optionally generate an automatic end of interrupt (AEOI) on the trailing edge of the second INTA cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 has the lowest, and priority assignment is fixed (fixed priority mode). Priority assignment can be rotated either manually (specific rotation mode) or automatically (automatic rotation mode) by programming operational command word 2 (OCW2).

Fixed Priority Mode: This is the default condition which exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for polled mode. In fixed priority mode, interrupts are fully nested with priority assigned as shown in the following:

Table 4-23. Fixed Priority Mode

Priority Status	Lowest							Highest
	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt request prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority interrupt which occurs during an interrupt service routine, will only be acknowledged if the CPU has internaly re-enabled interrupts.

Table 4-24. *Before Rotation*

Specific Rotation Mode: Specific rotation allows the system software to re-assign priority levels by issuing a command which redefines the highest priority channel (specific rotation command issued with Channel 5 specified).

Table 4-25. *After Rotation*

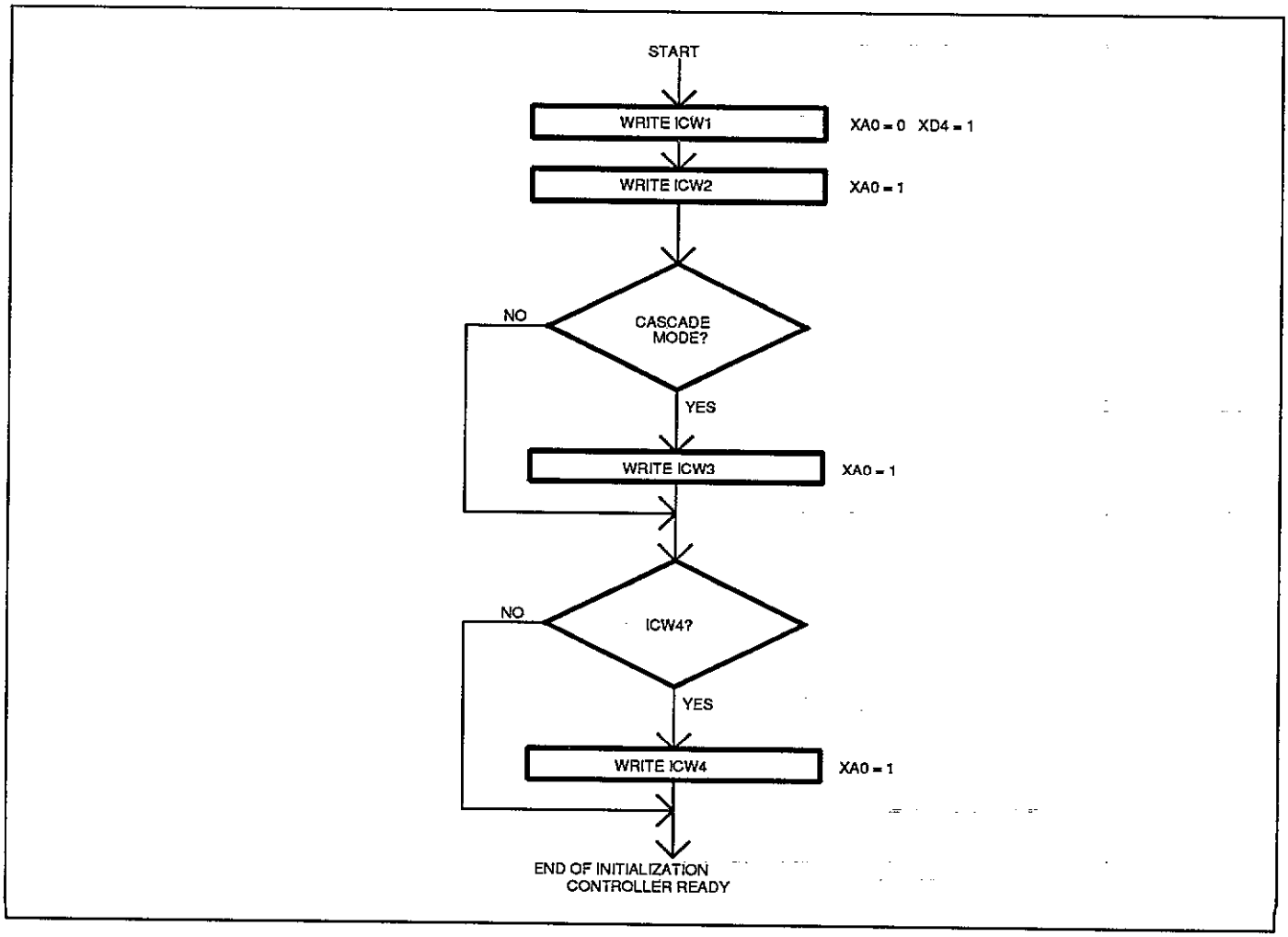
Priority Status	Lowest							Highest
	7	6	5	4	3	2	1	0

(specific rotation command issued with Channel 5 specified)

Priority Status	Lowest							Highest
	5	4	3	2	1	0	7	6

Automatic Rotation Mode: In applications where a number of equal priority peripherals are requesting interrupts, automatic rotation may be used to equalize the priority assignment. In this mode, a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the

Figure 4-9. *Initialization Sequence*



controller will be serviced at least once in eight interrupt requests to the CPU from the controller. Automatic rotation will occur, if enabled, due to the occurrence of EOI (automatic or CPU generated). Table 4-26 and 4-27 provide examples of specific rotation modes.

Table 4-26. Before Rotation (IR4 is highest priority request being serviced)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0
Priority Status	**Lowest**							**Highest**
	7	6	5	4	3	2	1	0

Table 4-27. After Rotation (IR4 service completed)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0
Priority Status	**Lowest**							**Highest**
	4	3	2	1	0	7	6	5

Programming the Interrupt Controller

Two types of commands are used to control the 82C316 interrupt controllers, initialization command words (ICWs) and operational command words (OCWs).

Initialization Command Words

The initialization process consists of writing a sequence of 4 bytes to each interrupt controller. The initialization sequence is started by writing the first initialization command word (ICW1) to address 020H (0A0H) with a 1 on bit 4 of the data byte. The interrupt controller interprets this as the start of the initialization sequence and does the following:

1. The initialization command word counter is reset to zero.
2. ICW1 is latched into the device.
3. Fixed priority mode is selected.
4. IR7 is assigned the highest priority.
5. The interrupt mask register is cleared.
6. The slave mode address is set to 7.
7. The special mask mode is disabled.
8. The IRR is selected for status read operations.

The next three I/O writes to address 021H (0A1H0) loads ICW2-ICW4. See Figure 4-9 for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all 4 bytes must be written for the controller to be properly initialized) by writing to address 020H (0A0H) with a 0 in data bit 4. Note that this causes 0CW2 or 0CW3 to be written.

Table 4-28. ICW1 Address 020H (0A0H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	X

(write only register)

SI: Bit 4 indicates to the interrupt controller that an initialization sequence is starting and must be a 1 to write ICW1.

LTM: Bit 3 selects level or edge triggered inputs to the IRR. If a 1 is written to LTM, a 'high' level on the IRR input will generate an interrupt request. The IR must be active until the first INTA cycle is started to generate the proper interrupt vector (an IR7 vector will be generated if the IRR input is deasserted early) and the IR must be removed prior to EOI to prevent a second interrupt from occuring.

SM: Bit 1 selects between single mode and cascade mode. Single mode is used whenever only one interrupt controller (INTC1) is used. Cascade mode allows the interrupt controllers to be connected through IR2 of INTC1. INTC1 will allow INTC2 to generate its own interrupt vectors if cascade mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for cascade mode for both devices to operate.

Table 4-29. ICW2 - Address 021H (0A1H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4I	V3	X	X	X

(write only register)

V<3:7>: These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the priority resolver during INTA (see Figure 4-12). INTC1 and INTC2 need not be programmed with the same value in ICW2.

Table 4-30. ICW3 Format for INTC1 - Address 021H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
S7	S6	S5	S4I	S3	S2	S1	S0

(write only register)

S<0:7>: Select which IR inputs have slave mode controllers connected. ICW3 in INTC1 must be written with a 04H for INTC2 to function.

Table 4-31. ICW3 Format for INTC2 - Address 0A1H

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0I	0	ID2	ID1	ID0

(write only register)

ID2-ID0: Determine the slave mode address the controllers will respond to during the cascaded INTA sequence. ICW3 in INTC2 should be written with a 02H for cascade mode operation. Note, b<3:7> should be zero.

Table 4-32. ICW4

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	EMI	X	X	AEOI	X

(write only register)

EMI: Bit 4 will enable multiple interrupts from the same channel in fixed priority mode. This allows INTC2 to fully nest interrupts, when cascade mode and fixed priority mode are both selected, without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and check its in-service register for zero, when exiting an interrupt service routine. If zero, a non-specific EOI command should be sent to INTC1. If non-zero, no command is issued.

AEOI: Auto end of interrupt is enabled when ICW4 is written with a zero in bit 1. The interrupt controller will perfom a non-specific EOI on the trailing edge of the second INTA cycle. Note that this function should not be used in a device with fully nested interrupts; unless the device is a cascade master.

Operational Command Words

Operational command word 1 (OCW1) is located at address 021H (0A0H) and may be written any time the controller is to in initialization mode. Operational command words 2 and 3 (OCW2, OCW3) are located at address 020H (0A0H) with a 0 in bit 4 will place the controller in operational mode and load controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

Table 4-33. OCW1 - Address 021H (0A1H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

(read/write register)

M<0:7>: These bits control the state of the interrupt mask register. Each interrupt request can be masked by writing a 1 in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no affect on lower priority requests. All IMR bits are cleared by writing ICW1.

Table 4-34. OCW2 - Address 020h (0A0h)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

(write only register)

R: This bit is in conjunction with SL and EOI selects oprational function. Writing a 1 in bit 7 causes one of the rotate functions to be selected.

Table 4-35. Rotate Function

R	SL	EOI	Function
1	0	0	Rotate on auto EOI enable*
1	0	1	Rotate on non-specific EOI
1	1	0	Specific Rotate Command
1	1	1	Rotate on specific EOI

* This function is disabled by writing a zero to all three bit positions.

SL: This bit, in conjunction with R and EOI, selects operational function. Writing a 1 in this bit position causes a specific or immediate function to occur. All pecific commands require LS-L0 to be valid except no operation.

Table 4-36. Specific Function

R	SL	EOI	Function
0	1	0	No operation
0	1	1	Specific EOI Command
1	1	0	Specific Rotate Command
1	1	1	Rotate on Specific EOI

EO1: This bit, in conjunction with R and SL, selects operational function. Writing a 1 in this bit position causes a function related to EO1 to occur.

Table 4-37. End of Interrupt

R	SL	EOI	Function
0	0	1	Non-specific EOI Command
0	1	1	Specific EOI Command
1	0	1	Rotate on non-specific EOI
1	1	1	Rotate on specific EOI

S1: Writing a 0 in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

2/3: If the I/O write places a 0 in bit 4 (SI), then writing a 0 in bit 3 (2/3) selects OCW2 and writing a 1 will select OCW3.

L<0:2>: These three bits are internally decoded to select which interrupt channel is to be affected by the specific command. L<0:2> must be valid during three of the four specific cycles.

Table 4-38. OCW3 - Address 020H (0A0H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

(write only register)

ESMM: Writing a 1 in this bit position enables theset/reset special mask mode function controlled by bit 5 (SMM). ESMM allows the other function in OCW3 to be accessed and manipulated without affecting the special mask mode state.

SMM: If ESMM qand SMM both are written with a 1 the special mask mode is enabled. Writing a 1 to ESMM and a 0 to SMM disables special mask mode. During special mask mode, writing a 1 to any bit position inhibits interrupts and a 0 enables interrupts on the associated channel by causing the priority resolver to ignore the condition of the ISR.

SI: See SI above.

2/3: See 2/3 above.

PM: Polled mode is enabled by writing a 1 to bit 2 of OCW- causing the 82C316 to perform the equivalent of an INTA cycle during the next I/O read operation to the controller. The byte read during this cycle will have bit 7 set if an interrupt is pending. If bit 7 of the byte is set, the level of the highst pending request will be encoded on bits 2-0. The IRR will remain frozen until the read cycle is completed at which time the PM bit is reset.

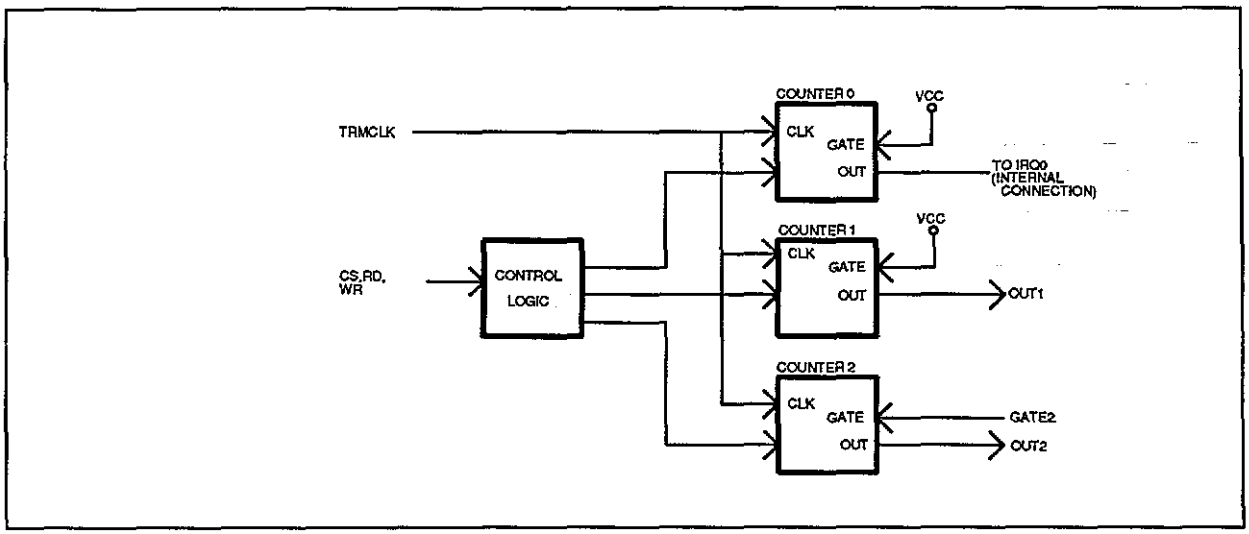
RR: When the RR bit (bit 1) is 1, reading the status port at address 020H (0A0H) will cause the contents of IRR or ISR (determined by RIS) to be placed on XD7-XD0. Asserting PM forces RR reset.

RIS: This bit selects between the IRR and the ISR during status read operations if IRR = 1.

Counter/Timer Functional Description

The counter/timer (CTC) in the 82C316 is general purpose, and can be used to generate accurate time delays under software control. The CTC contains 3 16-bit counter (Counter 0-3) which can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of theother two and can be programmed for operation as a timer of a counter.

Figure 4-10. Counter/Timer Block Diagram



All three of the counters shown in Figure 4-10 are controlled from a common set of control logic. The control logic decodes control information written to the CTC and provides the controls necessary to load, read configure and control each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the lack of an external hardware trigger signal. Counter 2 can be operated in any of six modes listed below.

Mode 0 interrupt on terminal count

Mode 1 hardware retriggerable one-shot

Mode 2 rate generator

Mode 2 square wave generator

Mode 4 software triggered strobe

Mode 5 hardware retriggerable strobe

All three counters in the CTC are driven from a common clock input pin (TMRCLK) which is independent from other clock inputs to the 82C316. Counter 0's output (Out0) is connected to IR0 of INTC1 (see the section titled *Interrupt Controller Functional Description*) and may be used as an interrupt to the system for time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third counter (Counter 2) is a full function counter/timer. This channel can be used as an interval timer, a counter, or as a gated rate/pulse generator.

Counter Description

Each counter in the CTC contains a control register, a status register, a 16-bit counting element (CE), a pair of 8-bit counter input latches (CIL, CIH), and a pair of 8-bit counter output latches (COL, COH). Each counter also has a clock

input for loading and decrementing the CE, a mode defined GATE input for controlling the counter (only GATE2 is externally accessible), and an OUT signal (OUT0 is not externally accessible). The OUT signal's state and function are controlled by the Counter Mode and condition of the CE.

The Control register stores the mode and command information used to control the counter. The control register may be loaded by writing a byte, containing a pointer to the desired counter, to the write control word address (043H). The remaining bits in the byte contain the mode, the type of command, and count format information.

The status register allows the software to monitor counter condition and read back the contents of the control register.

The counting element is a loadable 16-bit synchronous down counter. The CE is loaded or decremented on the falling edge of TMRCLK. The CE contains the maximum count when a 0 is loaded; which is equivalent to 655536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In Modes 2 and 3 the CE will be reloaded and in all other modes it will wrap around to FFFFH in binary operation or 9999 in BCD.

The CE is indirectly loaded by writing one or two bytes (optional) to the counter input latches, which are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the counter output latches. COL and COH are transparent latches which can be read while transparent or latched.

Programming the CTC

After power-up, the conditionn of CTC control registers, counter registers, CE and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a control word and then an initial count. The control register of a counter is written by writing to the control word address (see Table 4-39). The control word is a write only location.

Table 4-39. Counter/Timer Address Map

Address	Function
040H	Counter 0 Read/Write
041H	Counter 1 Read/Write
042H	Counter 2 Read/Write
043H	Counter Register Write Only

Table 4-40. Control Word - (043H)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
F3	F2	F1	F0	M2	M1	M0	BCD

(write only register)

F<0:3>: Bits 4-7 determine the command to be performed as shown in Table 4-41.

Table 4-41. Counter Commands

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (see Counter Latch Command)
0	0	0	1	Read/Write Counter 0 LSB only
0	0	1	0	Read/Write Counter 0 MSB only
0	0	1	1	Read/Write Counter 0 LSB then MSB
0	1	0	0	Latch Counter 1 (see Counter Latch Command)
0	1	0	1	Read/Write Counter 1 LSB only
0	1	1	0	Read/Write Counter 1 MSB only
0	1	1	1	Read/Write Counter 1 LSB then MSB
1	0	0	0	Latch Counter 2 (see Counter Latch Command)
1	0	0	1	Read/Write Counter 2 LSB only
1	0	1	0	Read/Write Counter 2 MSB only
1	0	1	1	Read/Write Counter 2 LSB then MSB
1	1	X	X	Read-Back Command (see Counter Read-Back Command)

MSB = most significant byte
LSB = least significant byte

M<0:2>: Bits 1-3 determine the counter's mode during read/write counter commands, or select the counter during a read-back command. Bits 1-3 become "don'tcare" during latch counter commands.

BCD: Bit 0 selects binary coded decimal counting format during read/write counter commands. When bit 0 is 0, then it is a binary count and when bit 0 is set to 1, it is a BCD count. Note that during read-back command this bit must be 0.

Read/Write Counter Command

When writing to a counter, two conventions must be observed:

1. Each counter control word must be written before the initial count is written.
2. Writing the initial count must follow the format specified in the control word (least significant byte only, most significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count can be written into the counter at any time after programming without rewriting the control word; providing the programmed format is observed.

During read/write counter commands, M<0:2> are defined as shown in Table 4-42.

Table 4-42. Counter Mode

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	1	0	Select Mode 4
1	1	1	Select Mode 5

Latch Counter Command

When a latch counter command is issued, the counter's output latches (COL, COH) latch the current state of the CE, COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then returns to a "transparent" condition. In this condition, the latches are enabled and the contents of the CE may be read directly.

Latch counter commands may be issued to more than one counter before reading the first counter to which the command was issued. Also, multiple latch counter commands issued to the same counter without reading the counter will cause all but the first command to be ignored.

Read-Back Command

The read-back command allows the user to check the count value, mode and state of the OUT signal and null count flag of the selected counter(s). The format of the Read-Back command is as shown in Table 4-43.

LC: Writing a 0 in bit 5 causes the selected counter(s) to latch the state of the in COL and COH.

LS: Writing a 0 in bit 4 causes the selected counter(s) to latch the current condition of its control register, null count and output into the status register. The next read of the counter results in the contents of the status register being read.

C<0:2>: Writing a 1 in bit 3 causes counter 3 to latch one or both of the registers specified by LC and LS. The same is true for bits 2 and 1 except that they enable counters 1 and 0 respectively.

Table 4-43. Status Byte

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
F3	F2	F1	F0	M2	M1	M0	BCD

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS = LC = 0, status will be returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned.

OUT: Bit 7 contains the state of the OUT signal of the couner.

NC: Bit 6 contains the condition of the Null count flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the Control register or the counter. NC is cleared to a 0 whenever the counter is loaded from the counter input registers.

F<0:1>: Bits 4-5 contain the F0 and F1 command bits which were written to the command register of the counter during initialization. This information is useful in determining whether the high byte, the low byte or both must be transferred during counter read/write operations.

M<1:2>: These bits reflect the mode of the counter and are interpreted in the same manner as in write command operations.

BCD: Bit 0 indicates the CE is operating in BCD format.

Counter Operation

Due to the previously stated restrictions in Counter 0 and Counter 1, Counter will be used as the example in describing counter operation, but the description of Mode 0, 2, 3, and 4 is relevant to all counters.

The following terms are defined for describing CTC operation.

TMRCLK pulse: A rising edge followed by a falling edge of the 82C316 TMRCLK input.

Trigger: The rising edge of the GATE2 input (refer to Figure 4-10).

Counter Load: The transfer of the 16-bit value in CIL and CIH to the CE.

Initialized: A control word written and the counter input latches loaded.

Counter 2 operates in one of the following modes.

Mode 0 - Interrupt on Terminal Count

Writing the control word causes OUT2 to go low and remain low until the CE reaches 0, at which time it goes back high and remains high until a new count or control word is written. Counting is enabled when GATE2 = 1. Disabling the count has no effect on OUT2.

The CE is loaded with the first TMRCLK pulse after the control word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written. This TMRCLK pulse does not decrement the count, so far an initial count of N, OUT2 doesn't go high until N + 1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2 = 0, it will still be loaded on the next TMRCLK pulse but counting does not begin until GATE2 = 1. OUT2 therefore, goes high N TMRCLK pulses after GATE2 = 1.

Mode 1 - Hardware Retriggerable One-Shot

Writing the control word causes OUT2 to go high initially. Once initialized the counter is armed and a trigger causes OU>T2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches 0. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT>2 is low cause the C to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH will not affect the current one-shot unless the counter is retriggered.

Mode 2 - Rate Generator

Mode functions as a divide-by-N counter, with OUT2 as the carry. Writing the control word during initialization sets OUT2 high.

When the initial count is decremented to 1, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE and the process is repeated. In Mode 2 the counter continues counting (if GATE2 = 1) and will generate an OUT2 pulse every N TMRCLK cycles. Note that a count of 1 is illegal in Mode 2.

GATE2 = 0 disables counting and forces OUT W2 high immediately. A trigger reloads the CE on the TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

Mode 3 - Square Wave Generator

Mode 3 is similar to Mode 2 inevery respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high = low = N/2). For odd count values, OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N + 1)2 and low = (N - 1)2.

Mode 4 - Software Triggered Strobe

Writing the control word causes OUT2 to go initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, (N + 1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be "retriggerable" by software.

Mode 5 - Hardware Triggered Strobe

Writing the control word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

The CE is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter "retriggerable."

GATE2

In Modes 0, 2, 3, and 4, GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3, and 5, the GATE2 input is rising-edge sensitive. This rising edge sets ann internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flip-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge and level sensitive. Table 4-45 summarizes the GATE pin function for all modes.

Table 4-44. Gate Pin Function

Mode	Condition		
	Low	Rising	High
0	Disables Counting	—	Enables Counting
1	—	a) Initiates Counting b) Resets Out Pin	—
2	a) Disables Counting b) Forces Out Pin High	Initiates Counting	Enables Counting
3	a) Disables Counting b) Forces Out Pin High	Initiates Counting	Enables Counting
4	Disables Counting	—	Enables Counting
5	—	Initiates Counting	—

Real Time Clock Functional Description

This section of the 82C316 combines a complete time-of-day clock with alarm, one hundred year calendar, a programmable period interrupt, and 114 bytes of low power static RAM. Provisions are made to enable the device to operate in a low power (battery powered) mode and protect the contents of both the RAM and clock during system power-up and power-down.

Register Access

I/O ports 70H and 71H are used for accessing the 128 locations in the Real Time Clock. First the index address (0 to 7FH) is output to port 70H. Then the data is read or written at port 71H. The entire port 70H/71H sequence should be completed while interrupts are inhibited or during an interrupt service routine before re-enabling interrupts. Otherwise, an interrupt service routine potentially could intervene between the output to port 70H and the subsequent I/O to port 71H, over-writing the port 70H value.

Address Map

Table 4-46 illustrates the internal register/RAM organization of the real time clock portion of the 82C316. The 128 addressable locations in the real time clock are divided into 10 bytes which normally contain the time, calendar and alarm data, four control and status bytes and 114 general purpose RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except registers C, D, bit 7 of register A, and bit 7 of the seconds byte which is always 0.

Table 4-45. Address Map for Real Time Clock

Index	Function
00	Seconds
01	Seconds Alarm
02	Minutes
03	Minutes Alarm
04	Hours
05	Hours Alarm
06	Day of the Week
07	Day of the Month
08	Month
09	Year
0A	Register A
0B	Register B
0C	Register C
0D	Register D
0E	User RAM
0F	User RAM
—	
—	
—	
7E	User RAM
7F	User RAM

Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the real time clock. Initialization of the time, calendar and alarm information is accomplished by writing to these location. Information is stored in these locations in binary-coded decimal (BCD) format.

Before initialization of the internal registers can be performed, the set bit in register B should be set to a "1" to prevent real time clock updates from occurring. The CPU then initializes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initialized and enabled, the real time clock will perform clock/calendar updates at a 1 Hz rate.

Table 4-47 shows the format for the ten clock, calendar and alarm locations. The 24/12 bit in register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization, the 24/12 bit cannot be changed without reinitializing the hour locations. In 12 hour format the high order bit of the hours byte in both the time and alarm bytes will indicate PM when it is a "1."

Table 4-46. Time, Calendar, Alarm Data Format

Index Register Address	Function	BCD Range
0	Seconds	00-59
1	Seconds Alarm	00-59
2	Minutes	00-59
3	Minutes Alarm	00-59
	Hours (12 hour mode)	01-12 (AM) 81-92 (PM)
4		
	Hours (24 hour mode)	00-23
	Hours Alarm (12 hour mode)	01-12 (AM) 81-92 (PM)
5		
	Hours Alarm (24 hour mode)	00-23
6	Day of the Week	01-07
7	Day of the Month	01-31
8	Month	01-12
9	Year	00-99

During updates, which occur once per second, the 10 bytes of time, calendar and alarm information are unavailable to be read or written by the CPU for a period of 2ms. These 10 locations cannot be written during this time. Information read while the real time clock is performing updates will be undefined. The update cycle section shows how to avoid update cycle/PCU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or they can be programmed to generate a periodic interrupt. To generate an interrupt at a specific time, the user need only program the time that the interrupt is to occur into the 3 alarm bytes. Alternately, a periodic interrupt can be generated by setting the high order two bits in alarm register to a "1," which turns that byte into a "don't care." For instance, an interrupt can be generated once a second by programming the same evaluate into all three alarm register.

Static RAM

The 114 bytes of RAM from index address 0EH to 7FH are not affected by the real time clock. These bytes are accessible during the update cycle and may be used for whatever the designer wishes. Typical applications will use this as

non-volatile storage for configuration and calibration parameters since this device is normally battery powered when the system is turned off.

Control and Status Registers

The 82C316 contains four registers used to control operation and monitor the status of the real time clock. These registers are located at index address 0AH-0DH and are accessible by the CPU at all times.

Table 4-47. Register A (0AH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

(Read/Write register except UIP)

UIP: Update in progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (high) 244us prior to the start of an update cycle and will remain active for an additional 2ms while the update is taking place. The UIP bit is read only and is not affected by RESET4. Writing a "1" to the SET bit in register B will clear the UIP status bit.

DV<0:2>: These three bits control the divider/prescaler on the Real-Time Clock. While the 82C316 can operate at frequencies higher than 32.768KHz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies.

Table 4-48. Real Time Clock Divide

DV2	DV1	DV0	OSCI Freq	Mode
0	0	0	4.194304 MHz	Operate
0	0	1	1.048576 MHz	Operate
0	1	0	32.768 KHz	Operate
1	1	X	Reset Divider	

RS<0:3>: These four bits control the periodic interrupt rate. The periodic interrupt is derived from the divider/prescaler in the real time clock and is separate from the alarm interrupt. Both the alarm and periodic interrupts do however, use the same interrupt channel in the interrupt controller. Use of the periodic interrupt allows the generation of interrupts at rates higher than once per second. Table 4-50 shows the interrupt rates for which the real time clock can be programmed.

Table 4-49. Periodic Interrupt Rate

Rate Selection				Time Base	
RS3	RS2	RS1	RS0	4.194304 MHz 1.048576 MHz	32.768 KHz
0	0	0	0	None	None
0	0	0	1	30.517 µs	3.90526 ms
0	0	1	0	61.035 µs	7.8125 ms
0	0	1	1	122.070 µs	122.070 µs
0	1	0	0	244.141 µs	244.141 µs
0	1	0	1	488.281 µs	488.281 µs
0	1	1	0	976.562 µs	976.562 µs
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1	1	31.25 ms	31.25 ms
1	1	0	0	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

Table 4-50. Register B (0BH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	0	24/12	DSE

(Read/Write register)

SET: Writing a "0" to this bit enables the update cycle and allows the real time clock to function normally. When set to a "1" the update cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the RESET4 input pin.

PIE: The periodic interrupt enable bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of register A. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to a "0" by Reset.

AIE: The generation of alarm interrupts is enabled by setting this bit to a "1." Once this bit is enabled the real time clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the alarm registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by Reset.

24/12: 24/12 control bit is used to establish the format of both the hours and hours alarm bytes. If this bit is a "1," the real time clock will interpret and update the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by Reset.

DSE: The real time clock can be instructed to handle daylight savings time changes by setting this bit to a "1." This enables two exceptions to the normal time keeping sequence to occur. On the last Sunay in April AM. Setting this bit to a "0" disables the execution of these two exceptions. PSRSTC- has no affect on this bit.

Table 4-51. Register C (0CH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

(Read only register)

IRQF: The interrupt request flag is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is:

IRQF = PF & PIE
+ AT & AIE
+ UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB/input pin. Writing to this register has no affect on the contents.

PF: The period interrupt flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt and set IRQF if PIE is a "1."

AF: A "1" appears in the AF bit whenever a match has occurred between the time register and alarm registers during an update cycle. This flag is also independent of tis enable (AIE) and will generate an interrupt if AIE is true.

Table 4-52. Register D (0DH)

MSB							LSB
b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

(Read only register)

VRT: The valid RAM and time bit indicates the condition of the contents of the real time clock. This bit is cleared to a "0" whenever the PS input pin is LOW. This pin is normally derived from the power supply which supplies Vcc to the device and will allow the user to determine whether the registers have been initialized since power was applied to the device. PSRSTB has no effect on this

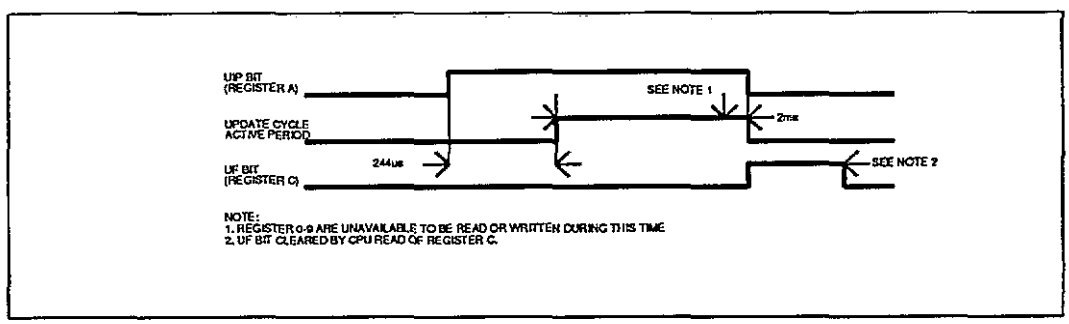
on this bit and it can only be set by reading register D. All unused register bits will be "0" when read and are not writeable.

Update Cycle

During normal operation, the real time clock performs an update cycle once every second. The performance of an update cycle is contingent upon the divider bits DV<0:2> not being cleared, and the SET bit in register B cleared. The function of the update cycle is to increment the clock/calendar registers and compare them to the alarm registers. If a match occurs between the two sets of registers, an alarm is issued and an interrupt will be issued if the alarm and interrupt control bits are enabled.

During the time that an update is taking place, the lower 10 registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the real time clock and the CPU, a flag is provided in register A to alert the user of an impending update cycle. This update in process bit (UIP) is asserted 244us before the actual start of the cycle and is maintened until the ccle is complete. Once the cycle is complete the UIP bit will be cleared and the update flag (UF) in register C will be set. Figure 4-11 illustrates the update cycle. CPU access is always allowed to register A through D during update cycles.

Figure 4-11. Update Cycle



Two methods for reading and writing to the real time clock are recommended. Both of these methods will allow the user to avoid contention between the CPU and the real time clock for access to the time and date information.

The first method is to read register A, determine the state of the UIP bit and if it is "0," perform the read or write operation. For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require longer than 244us to complete from the beginning of the read of register A to the completion of the last read or write operation to the clock calendar registers.

The second method of accessing the lower 10 registers is to read register C once and disregard the contents. Then subsequently continue reading this register until the UF bit is a "1." This bit will become true immediately after an update has been completed. the user then has until the start of the next update cycle to complete a read or write operation.

Power-up/Down

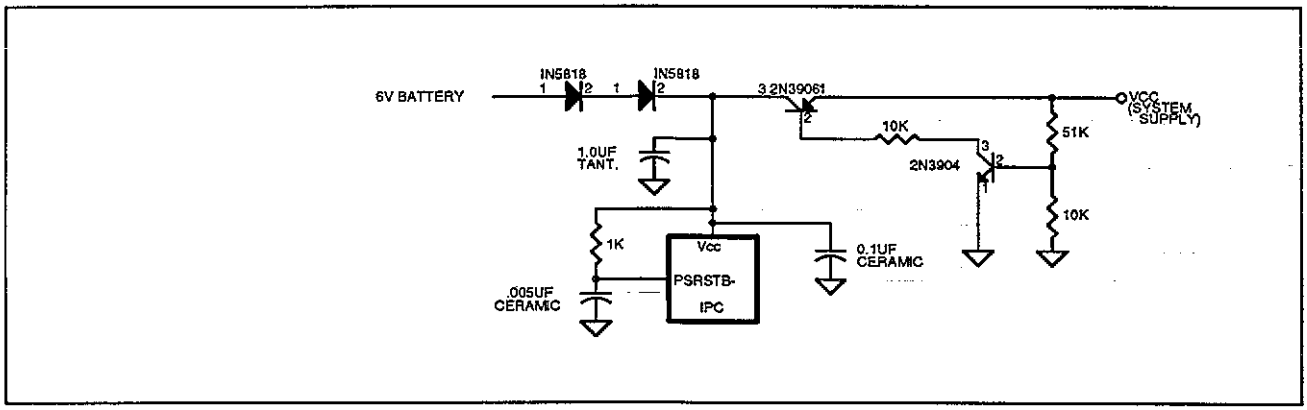
Most applications will require the real time clock to remain active whenever the system power is turned off. To accomplish this the user must provide an alternate source of power to the 82C316. This alternate source of power is normally provided by connecting a battery to the Vcc supply pin of the device. A means should be provided to switch from the system power supply to the battery. A circuit such as the one shown in Figure 4-12 may be used to eliminate power drain on the battery when the entire 82C316 is active. The circuit shown here will allow for reliable transitions between system and battery power without undue battery power drain.

The user should also ensure that the Vin maximum specification is never exceeded when powering the system up or down. Failure to observe this specification may result in damage to the device.

A pin is provided on the device to protect the contents of the real time clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper operation of the system. This signal may be generated by circuitry in either the power supply or on the system board. The PWRGD input will disable all unnecessary inputs during the time the system is powered down to prevent noise on the inactive pins from causing increased Icc. This pin must therefore be inactive for the remainder of the device to operate properly when system power is applied.

One pin is provided to initialize the device whenever power is applied to the 82C316. This pin (PSRSTB-) will not alter the RAM or clock/calendar contents but it will initialize the necessary control register bits. (See the pin description for a list of the control register bits affected by PSRSTB-). Assertion of PSRSTB- disables the generation of interrupts and sets a flag indicating that the contents of the device may not be valid. A recommended circuit for controlling the PSRSTB- input is also shown in Figure 4-12.

Figure 4-12. *Power Conversion and Reset Circuitry*



82C316 Internal Registers

Table 4-53. *82C316 Internal Decode*

Device	Address Range
DMA Controller #1	000H-00FH
Interrupt Controller #1	020H-021H
Configuration Registers	022H-023H
Counter Timer Controller	040H-043H
Real Time Clock (CMOS RAM)	070H-071H
DMAPAGE Registers	080H-08FH
Interrupt Controller #2	0A0H-0A1H
DMA Controller #2	0C0H-0DFH

Table 4-54. *Name: DMA1 Channel 0 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
000H	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address
	1	1	0	1	Write base & current high byte address.

Table 4-5. *Name: DMA1 Channel 0 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
001H	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-56. *Name: DMA1 Channel 1 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
002H	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address.
		1	0	1	Write base & current high byte address.

Table 4-57. *Name: DMA1 Channel 1 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
003H	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-58. *Name: DMA1 Channel 2 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
004H	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address.
		1	0	1	Write base & current high byte address.

Table 4-59. *Name: DMA1 Channel 2 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
005H	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-60. *Name: DMA1 Channel 3 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
006H	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address.
		1	0	1	Write base & current high byte address.

Table 4-61. *Name: DMA1 Channel 3 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
007H	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-62. *Name: DMA1 Status Register (READ ONLY)*

Index	Bits	Values and Functions
008H	7	Channel 3 pending DMA service.
		(0): DRQ3 not active.
		1 : DRQ3 active.
	6	Channel 2 pending DMA service.
		(0): DRQ2 not active.
		1 : DRQ2 active.
	5	Channel 1 pending DMA service.
		(0): DRQ1 not active.
		1 : DRQ1 active.
	4	Channel 0 pending DMA service.
		(0): DRQ0 not active.
		1 : DRQ0 active.
	3	Channel 3 Terminal Count status.
		(0): TC not reached.
		1 : Channel 3 has reached TC.
	2	Channel 2 Terminal Count status.
		(0): TC not reached.
		1 : Channel 2 has reached TC.
	1	Channel 1 Terminal Count status.
		(0): TC not reached.
		1 : Channel 1 has reached TC.
	0	Channel 0 Terminal Count status.
		(0): TC not reached.
		1 : Channel 0 has reached TC.

Table 4-63. *Name: DMA1 Command Register (WRITE ONLY)*

Addr	Bits	Values and Functions
008H	7	DACK input active level.
		(0): DACK active low.
		1 : DACK active high.
	6	DREQ input active level.
		(0): DREQ active low.
		1 : DREQ active high.
	5	Extended Write enable.
		(0): Write commands are asserted late.
		1 : Write commands are asserted one DMA cycle earlier during a transfer.
	4	Priority type for channel servicing.
		(0):Fixed priority.
		1 :Rotating priority.
	3	Transfer compression enable.
		(0):Normal timing
		1 :Compressed timing
	2	Master disable for the DMA controller.
		(0):DMA controller enable.
		1 :DMA controller disable.
	1	Address hold during memory-to-memory transfers.
		(0):Address hold for Channel 0 disable.
		1 :Address hold for Channel 0 enable.
	0	Memory-to-Memory transfer enable.
		(0):Memory-to-Memory transfers disable.
		1 :Memory-to-Memory transfers for channel 0 and 1 enable.

Table 4-64. *Name: DMA1 Request Register (READ ONLY)*

Addr	Bits	Values and Functions
009H	7:4	(1111): These bits are always set during a read.
	3	Request bit for channel 3.
		(0): No request pending.
		1 : Request pending for channel 3.
	2	Request bit for channel 2.
		(0): No request pending.
		1 : Request pending for channel 2.
	1	Request bit for channel 1.
		(0): No request pending.
		1 : Request pending for channel 1.
	0	Request bit for channel 0.
		(0): No request pending.
		1 : Request pending for channel 0.

Table 4-65. *Name: DMA1 Request Register (WRITE ONLY)*

Addr	Bits	Values and Functions
009H	7:3	(XXXXX): Don't Cares.
	2	Request bit.
		(0): Reset Request bit.
		1 : Set Request bit.
	1:0	DMA Channel Request bit Selection.
		(00): DMA Channel 0.
		01 : D A Channel 1.
		10 : DMA Channel 2.
		11 : DMA Channel 3.

Table 4-66. Name: DMA1 Command Register (READ ONLY)

Addr	Bits	Values and Functions
00AH	7	DACK input active level.
		(0): DACK active low.
		1 : DACK active high.
	6	DREQ input active level.
		(0): DREQ active low.
		1 : DREQ active high.
	5	Extended Write enable.
		(0): Write commands are asserted late.
		1 : Write commands are asserted one DMA cycle earlier during a transfer.
	4	Priority type for channel servicing.
		(0):Fixed priority.
		1 :Rotating priority.
	3	Transfer compression enable.
		(0):Normal timing
		1 :Compressed timing
	2	Master disable for the DMA controller.
		(0):DMA controller enable.
		1 :DMA controller disable.
	1	Address hold during memory-to-memory transfers.
		(0):Address hold for Channel 0 disable.
		1 :Address hold for Channel 0 enable.
	0	Memory-to-Memory transfer enable.
		(0):Memory-to-Memory transfers disable.
		1 :Memory-to-Memory transfers for channel 0 and 1 enable.

Table 4-67. Name: DMA1 Single Bit Request Mask Register (WRITE ONLY)

Addr	Bits	Values and Functions
00AH	7:3	(XXXXX): Don't Cares.
	2	Request bit.
		(0): Reset Request bit.
		1 : Set Request bit.
	1:0	DMA Channel Request bit Selection.
		(00): DMA Channel 0.
		01 : DMA Channel 1.
		10 : DMA Channel 2.
		11 : DMA Channel 3.

Table 4-68. *Name: DMA1 Mode Register (READ/WRITE)*

Addr	Bits	Values and Functions
00BH	7:6	Channel Mode type.
		(00): Demand Mode.
		01 : Single Cycle Mode.
		10 : Block Mode.
		11 : Cascade Mode.
	5	Address counting direction.
		(0): Increment address.
		1 : Decrement address.
	4	Autoinitialization enable.
		(0): Autoinitialization function disable.
		1 : Autoinitialization function enable.
	3:2	Type of transfer.
		(00): Verify transfer.
		01 : Write transfer.
		10 : Read transfer.
		11 : Illegal.
	1:0	DMA Channel Mode Selection.
		(00): DMA Channel 0.
		01 : DMA Channel 1.
		10 : DMA Channel 2.
		11 : DMA Channel 3.

Table 4-69. *Name: DMA1 Set Byte Pointer Flip-Flop (READ ONLY)*

Addr	Bits	Values and Functions
00CH	7:0	Bits 7:0 are don't cares. The Set Byte Pointer Flip-Flop Clear command is activated as a result of the address 00CH access and the assertion of IOR-. This command allows the CPU to adjust the pointer to the high byte of an address or word count register.

Table 4-70. *Name: DMA1 Clear Byte Pointer Flip-Flop (WRITE ONLY)*

Addr	Bits	Values and Functions
00CH	7:0	Bits 7:0 are don't cares. The Clear Byte Pointer Flip-Flop Clear command is activated as a result of the address 00CH access and the assertion of IOW-. This command allows the CPU to adjust the pointer to the low byte of an address or word count register.

Table 4-71. *Name: DMA1 Temporary Register (READ ONLY)*

Addr	Bits	Values and Functions
00DH	7:0	Bits 7:0 contains values of XD<7:0> during the first cycle of a memory-to-memory transfer. Data from the last memory-to-memory transfer will remain in the register unless a RESET4 or Master Clear occurs.

Table 4-72. *Name: DMA1 Master Clear (WRITE COMMAND ONLY)*

Addr	Bits	Values and Functions
00DH	7:0	Bits 7:0 are don't cares. The Master Clear command is activated as a result of the address 00EH access and the assertion of IOW-. This command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, and Byte Pointer Flip-Flop are cleared and the Request Mask Register is set.

Table 4-73. *Name: DMA1 Clear Mode Register Counter (READ COMMAND ONLY)*

Addr	Bits	Values and Functions
00EH	7:0	Bits 7:0 are don't cares. The Clear Mode Register Counter command is activated as a result of the address 00EH access and the assertion of IOR-. This command is provided to allow the CPU to restart the mode read process at a known point. After clearing the counter all four Mode Registers may be read by doing successive reads to the Read Mode Register address. The order in which the registers will be read is Channel 0 first, Channel 3 last.

Table 4-74. *Name: DMA1 Clear Request Mask Bits (WRITE COMMAND ONLY)*

Addr	Bits	Values and Functions
00EH	7:0	Bits 7:0 are don't cares. The Clear Mask Register command is activated as a result of the address 00EH access and the assertion of IOW-. This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

Table 4-75. *Name: DMA1 Request Mask Register Bits (READ/WRITE)*

Addr	Bits	Values and Functions
00FH	7:2	(XXXX): Don't Cares.
	3	Channel 0 Mask bit.
		0 : No bit mask
		(1): Bit mask
	2	Channel 1 Mask bit.
		0 : No bit mask
		(1): Bit mask
	1	Channel 2 Mask bit.
		0 : No bit mask
		(1): Bit mask
	0	Channel 3 Mask bit.
		0 : No bit mask
		(1): Bit mask

Table 4-76. *Name: INTC1 Initialization Command Word #1 (1ST WRITE ONLY)*

Addr	Bits	Values and Functions
020H	7:5	(XXX): Don't Cares.
	4	Start Initialization Sequence.
		(0): Do not begin initialization Sequence.
		1 : Begin Sequence and write to ICW1.
	3	Interrupt Level or Edge Trigger Select.
		0 : Edge Trigger enabled; Low to high transitions.
		1 : Level Trigger enabled; Active high.
	2	(X): Don't Care.
	1	Single or Cascade Mode Select.
		(0): Cascade Mode enabled; Cascade Mode allows the second interrupt controller
		1 : Single Mode Enabled; Single Mode is used whenever only one interrupt controller is used.
	0	(X): Don't Care.

Table 4-77. *Name: INTC1 Initialization Command Word #2 (2ND WRITE ONLY)*

Addr	Bits	Values and Functions
021H	7:3	Upper five bits of interrupt vector byte. These bits are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during interrupt acknowledge.
	2:0	Reserved.

Table 4-78. *Name: INTC1 Initialization Command Word #3 (3RD WRITE ONLY)**

Addr	Bits	Values and Functions
021H	7	Slave Mode Controller connected to IR7 select.
		(0): No Slave Mode Controller connected to IR7.
		1 : Slave Mode Controller connected to IR7.
	6	Slave Mode Controller connected to IR6 select.
		(0): No Slave Mode Controller connected to IR6.
		1 : Slave Mode Controller connected to IR6.
	5	Slave Mode Controller connected to IR5 select.
		(0): No Slave Mode Controller connected to IR5.
		1 : Slave Mode Controller connected to IR5.
	4	Slave Mode Controller connected to IR4 select.
		(0): No Slave Mode Controller connected to IR4.
		1 : Slave Mode Controller connected to IR4.
	3	Slave Mode Controller connected to IR3 select.
		(0): No Slave Mode Controller connected to IR3.
		1 : Slave Mode Controller connected to IR3.
	2	Slave Mode Controller connected to IR2 select.
		(0): No Slave Mode Controller connected to IR2.
		1 : Slave Mode Controller connected to IR2.
	1	Slave Mode Controller connected to IR1 select.
		(0): No Slave Mode Controller connected to IR1.
		1 : Slave Mode Controller connected to IR1.
	0	Slave Mode Controller connected to IR0 select.
		(0): No Slave Mode Controller connected to IR7.
		1 : Slave Mode Controller connected to IR0.

* Note: ICW3 in INTC1 must be written with a 04H for INTC2 to function.

Table 4-79. *Name: INTC1 Initialization Command Word #4 (4TH WRITE ONLY)*

Addr	Bits	Values and Functions
021H	7:5	(XXX): Don't Cares.
	4	Enable Multiple Interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts
	3:2	(XX): Don't Cares.
	1	Auto End of Interrupt enable. This bit is active low. The interrupt controller will perform a nonspecific EOI on the trailing edge of the second INTA cycle.
	0	(X): Don't Care.

Table 4-80. *Name: INTC1 Initialization Command Word #1 (READ/WRITE)*

Addr	Bits	Values and Functions
021H	7	IR7 Mask bit.
		(0): No mask.
		1 : Mask IR7.
	6	IR6 Mask bit.
		(0): No mask.
		1 : Mask IR6.
	5	IR5 Mask bit.
		(0): No mask.
		1 : Mask IR5.
	4	IR4 Mask bit.
		(0): No mask.
		1 : Mask IR4.
	3	IR3 Mask bt.
		(0): No mask.
		1 : Mask IR3.
	2	IR2 Mask bit.
		(0): No mask.
		1 : Mask IR2.
	1	IR1 Mask bit.
		(0): No mask.
		1 : Mask IR1.
	0	IR0 Mask bit.
		(0): No mask.
		1 : Mask IR0.

Table 4-81. *Name: INTC1 Operational Command Word #2 (2ND WRITE ONLY)*

Addr	Bits	Values and Functions	
020H	7	Rotate function select. Bit 7 is used in conjunction with bits 6 and 5 to select operational function.	
B7	**B6**	**B5**	**Function**
1	0	0	Rotate on auto EOI enable.
1	0	1	Rotate on non-specific EOI.
1	1	0	Specific Rotate Command.
1	1	1	Rotate on specific EOI.
	6	Specific or immediate function select. Bit 6 is used in conjunction with bits 7 and 5 to select operational function.	
B7	**B6**	**B5**	**Function**
0	1	0	No operation.
0	1	1	Specific EOI Command.
1	1	0	Rotate on specific EOI.
	5	Function related to EOI select. Bit 5 is used in conjunction with bits 7 and 6 to select operational function.	
B7	**B6**	**B5**	**Function**
0	1	0	Non-specific EOI Command.
0	1	1	Specific EOI Command.
1	1	0	Rotate on non-specific EOI.
1	1	1	Rotate on specific EOI.
	4	Interrupt controller out of initialize mode select.	
		0 : Disable initialization mode and write OCW2 & OCW3.	
		1 : Enable initialization mode.	
	3	Operational Command Word Select.	
		0 : OCW2 selected.	
		1 : OCW3 selected.	
	2:0	Bits 2:0 are internally decoded to select which interrupt channel is to be affected by the Specific Command.	
		000: IR7.	
		001: IR6.	
		010: IR5.	
		011: IR4.	
		100: IR3.	
		101: IR2.	
		110: IR1.	
		111: IR0.	

Table 4-82. *Name: INTC1 Operational Command Word #3 (3RD WRITE ONLY)*

Addr	Bits	Values and Functions
020H	7	Bit 7 must be set to 0 for proper operation.
	6	Enable Special Mask Mode.
		(0): Special Mask Mode bit becomes a don't care.
		1 : Enable Special Mask Mode bit.
	5	Special Mask Mode.
		(0): Reset Special Mask.
		1 : Set Special Mask.
	4	Interrupt controller out of initialize mode select.
		0 : Disable initialization mode and write OCW2 & OCW3.
		1 : Enable initialization mode.
	3	Operational Command Word Select.
		0 : OCW2 selected.
		1 : OCW3 selected.
	2	Enable Poll Command.
		(0): No Poll Command.
		1 : Poll Command.
	1	Enable Read Register Command.
		(0): Read Register bit becomes a don't care.
		1 : Enable Read Register Command bit.
	0	Read Register Command.
		(0): Read Interrupt Request Register .
		1 : Read In-Service Register .

Table 4-83. *Name: Clock/Wait State Control Register (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
01H	7:6	Read/Write Cycle Wait States.
		00 : 1 Wait State.
		01 : 2 Wait States.
		10 : 3 Wait States.
		(11): 4 Wait States.
	5:4	16-bit DMA Cycle Wait States.
		(00): 1 Wait State.
		01 : 2 Wait States.
		10 : 3 Wait States.
		11 : 4 Wait States.
	3:2	8-bit DMA Cycle Wait States.
		(00): 1 Wait State.
		01 : 2 Wait States.
		10 : 3 Wait States.
		11 : 4 Wait States.
	1	Extended DMA Memory Read enable.
		(0): Delay MEMR- by one clock cycle later than IOW-.
		1 : Start MEMR- at the same time as IOW-.
	0	DMA source clock.
		(0): DMA Clock is equal to BCLK/2.
		1 : DMA Clock is equal to BCLK.

Table 4-84. *Name: RTC, NMI & Coprocessor Reset Register (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
26H	7	Real Time Clock selection.
		(0): Selects internal RTC.
		1 : Selects external RTC.
	6	Coprocessor Reset Type.
		(0): 80387 asynchronous reset.
		1 : 80387 synchronous reset.
	5	Power Fail warning active during last NMI(R/O).
		(0): Power Fail warning pin not active.
		1 : Power Fail warning pin was active.
	4	Power Fail Warning Enable.
		(0): PCU NMI disabled.
		1 : PCU NMI enabled.
	3	PCU NMI active level.
		(0): PCU NMI active low.
		1 : PCU NMI active high.
	2	Local Bus READY timeout/NMI Enable.
		(0): NMI is generated when READY timeout occurs.
		1 : NMI is not generated and READY timeout does not occur.
	1	Normally, I/O decode in 82C316 uses address range A0 through A9. The decode does not include A10 - A15. When this bit is set to 0, the I/O decode does not include A10 to A15 for decoding. If this bit is set to 1, A10 to A15 are included for I/O address decode. This is the extended I/O decode mode. For example, when extended I/O decode is disabled, and I/O address of 64. The I/O decode will be active for address 064 and F64 (the addresses A10 - A15 are neglected). When extended I/O decode is enabled, the I/O decode will be active for I/O address 64 only and AT cycle is performed for I/O address F64.
		(0): Disable extended I/O.
		1 : Enable extended I/O.
	0	NMI READY- timeout bit.
		(0): READY timeout has not occurred.
		1 : READY timeout has occurred.

Table 4-85. *Name: Programmable Port 1 Register MSBs (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
71H	7:0	Address bits A15-A8 of programmable I/O PORT 1.

Table 4-86. *Name: Programmable Port 1 Register LSBs (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
72H	7:0	Address bits A7-A0 of programmable I/O PORT 1.

Table 4-87. *Name: Port 1 Enable Register (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
73H	7:6	Reserved.
	5	PORT 1 I/O Read Enable.
		0 : I/O read disable.
		(1): I/O read enable.
	4	PORT 1 I/O Write Enable.
		0 : I/O write disable.
		(1): I/O write enable.
	3:0	The bits 0:3 correspond to addresses A<0:3>. These select the I/O address range for the programmable Chipselect. Setting a bit will cause the corresponding address bit to be masked for decoding. For example, if I/O address is 80, and if bit 0 is set to 1, the programmable chip select will be active for I/O addresses 80 and 81.

Table 4-88. *Name: Programmable Port 2 Register MSBs (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
74H	7:0	Address bits A15-A8 of programmable, I/O PORT 2.

Table 4-89. *Name: Port 1 Enable Register (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
75H	7:0	Address bits A7-A0 of programmable I/O PORT 2.

Table 4-90. *Name: Port 2 Enable Register (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
76H	7:6	Reserved.
	5	PORT 2 I/O Read Enable.
		0 : I/O read disable.
		(1): I/O read enable.
	4	PORT 2 I/O Write Enable.
		0 : I/O write disable.
		(1): I/O write enable.
	3:0	The bits 0:3 correspond to addresses A0:A3. These select the I/O address range for the programmable Chipselect. Setting a bit will cause the corresponding address bit to be masked for decoding. For example, if I/O address is 80, and if bit 0 is set to 1, the programmable chip select will be active for I/O addresses 80 and 81.

Table 4-91. *Name: Programmable Port 3 Register MSBs (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
77H	7:0	Address bits A15-A8 of programmable I/O PORT 3.

Table 4-92. *Name: Programmable Port 3 Register LSBs (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
78H	7:0	Address bits A7-A0 of programmable I/O PORT 3.

Table 4-93. *Name: Port 3 Enable Register (READ/WRITE)*
Index Register Address: 022H
Data Register Address: 023H

Addr	Bits	Values and Functions
79H	7:6	Reserved.
	5	PORT 3 I/O Read Enable.
		0 : I/O read disable.
		(1): I/O read enable.
	4	PORT 3 I/O Write Enable.
		0 : I/O write disable.
		(1): I/O write enable.
	3:0	The bits 0:3 correspond to addresses A0:A3. These select the I/O address range for the programmable Chipselect. Setting a bit will cause the corresponding address bit to be masked for decoding. For example, if I/O address is 80, and if bit 0 is set to 1, the programmable chip select will be active for I/O addresses 80 and 81.

Table 4-94. *Name: Counter/Timer Counter 0 (READ/WRITE)*

Addr	Bits	Values and Functions
040H	7:0	Counter 0 count register (Read/Write).

Table 4-95. *Name: Counter/Timer Counter 1 (READ/WRITE)*

Addr	Bits	Values and Functions
041H	7:0	Counter 1 count register (Read/Write).

Table 4-96. *Name: Counter/Timer Counter 2 (READ/WRITE)*

Addr	Bits	Values and Functions
042H	7:0	Counter 2 count register (Read/Write).

Table 4-97. *Name: Counter/Timer Control Word Register (WRITE ONLY)*

Addr	Bits	Values and Functions
043H	7:4	Determine the command to be performed
		0000 Latch counter 0
		0001 Read/Write counter 0 LSB only.
		0010 Read/Write counter 0 MSB only.
		0011 Read/write counter 0 LSB then MSB.
		0100 Latch counter 1.
		0101 Read/Write counter 1 LSB only.
		0110 Read/Write counter 1 MSB only.
		0111 Read/write counter 1 LSB then MSB.
		1000 Latch counter 2
		1001 Read/Write counter 2 LSB only.
		1010 Read/Write counter 2 MSB only.
		1011 Read/write counter 2 LSB then MSB.
		11xx Read-Back command.
	3:1	Determine the counter's mode
		000 Select mode 0.
		001 Select mode 1.
		x10 Select mode 2.
		x11 Select mode 3.
		110 Select mode 4.
		111 Select mode 5.
	0	Determines the type of the count
		0 Binary count.
		1 Binary coded decimal count.

Table 4-98. *Name: Index Register Address*

Addr	Bits	Values and Functions
070H	7:0	Index register address. The index value is placed in port 70H to access a particular register. The valid address range for the 82C316 are 0 thru 7FH.

Table 4-99. *Name: Data Register Address*

Addr	Bits	Values and Functions
071H	7:0	Data register address. The index value is placed in port 70H to access a particular register and the data to be read from or written to that register is placed in port 71H.

Table 4-100. *Name: Unused*

Addr	Bits	Values and Functions
080H	7:0	Not defined.

Table 4-101. *Name: 8-bit DMA Channel 2 (READ/WRITE)*

Addr	Bits	Values and Functions
081H	7:0	Address bits A16-A23 during 8-bit DMA(DACK2) cycles.

Table 4-102. *Name: 8-bit DMA Channel 3 (READ/WRITE)*

Addr	Bits	Values and Functions
082H	7:0	Address bits A16-A23 during 8-bit DMA(DACK3) cycles.

Table 4-103. *Name: 8-bit DMA Channel 1 (READ/WRITE)*

Addr	Bits	Values and Functions
083H	7:0	Address bits A16-A23 during 8-bit DMA(DACK1) cycles.

Table 4-104. *Name: Unused*

Addr	Bits	Values and Functions
084H	7:0	Not defined.

Table 4-105. *Name: Unused*

Addr	Bits	Values and Functions
085H	7:0	Not defined.

Table 4-106. *Name: Unused*

Addr	Bits	Values and Functions
086H	7:0	Not defined.

Table 4-107. *Name: 8-bit DMA Channel 0 (READ/WRITE)*

Addr	Bits	Values and Functions
087H	7:0	Address bits A16-23 during 8-bit DMA(DACK0) cycles.

Table 4-108. *Name: Unused*

Addr	Bits	Values and Functions
088H	7:0	Not defined.

Table 4-109. *Name: 16-bit DMA Channel 2 (READ/WRITE)*

Addr	Bits	Values and Functions
089H	7:0	Address bits A17-23 during 16-bit DMA(DACK6) cycles.

Table 4-110. *Name: 16-bit DMA Channel 3 (READ/WRITE)*

Addr	Bits	Values and Functions
08AH	7:0	Address bits A17-23 during 16-bit DMA(DACK7) cycles.

Table 4-111. *Name: 16-bit DMA Channel 1 (READ/WRITE)*

Addr	Bits	Values and Functions
08BH	7:0	Address bits A17-23 during 16-bit DMA(DACK5) cycles.

Table 4-112. *Name: Unused*

Addr	Bits	Values and Functions
08CH	7:0	Not defined.

Table 4-113. *Name: Unused*

Addr	Bits	Values and Functions
08DH	7:0	Not defined.

Table 4-114. *Name: Unused*

Addr	Bits	Values and Functions
08EH	7:0	Not defined.

Table 4-115. *Name: Refresh Cycle (READ/WRITE)*

Addr	Bits	Values and Functions
08FH	7:0	Address bits A23-A16 during a refresh cycle.

Table 4-116. Name: INTC2 Initialization Command Word #1 (1ST WRITE ONLY)

Addr	Bits	Values and Functions
0A0H	7:5	(XXX): Don't Cares.
	4	Start Initialization Sequence.
		(0): Do not begin initialization Sequence.
		1 : Begin Sequence and write to ICW1.
	3	Interrupt Level or Edge Trigger Select.
		0 : Edge Trigger enabled; Low to high transitions.
		1 : Level Trigger enabled; Active high.
	2	(X): Don't Care.
	1	Single or Cascade Mode Select.
		(0): Cascade Mode enabled. Cascade Mode allows the second interrupt controller, INTC2 to be connected through IR2 of INTC1. InTC1 will allow INTC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both devices to operate.
		1 : Single Mode Enabled. Single Mode is used whenever only one interrupt controller is used. This mode is not recommended for this device.
	0	(X): Don't Care.

Table 4-117. Name: INTC2 Initialization Command Word #2 (2ND WRITE ONLY)

Addr	Bits	Values and Functions
0A1H	7:3	Upper five bits of interrupt vector byte. These bits are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during interrupt acknowledge.
	2:0	Reserved.

*Table 4-118. Name: INTC2 Initialization Command Word #3 (3RD WRITE ONLY)**

Addr	Bits	Values and Functions
0A1H	7:3	Bits 7 to 3 should be zero.
	2:0	Bits 2 to 0 determines the Slave Mode address the controller will respond to during the cascaded INTA sequence.

* Note: ICW3 in INTC2 should be written with a 02H for Cascade Mode operations.

Table 4-119. Name: INTC2 Initialization Command Word #4 (4TH WRITE ONLY)

Addr	Bits	Values and Functions
0A1H	7:5	(XXX): Don't Cares.
	4	Enable Multiple Interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nest interrupts
	3:2	(XX): Don't Cares.
	1	Auto End of Interrupt enable. This bit is active low. The interrupt controller will perform a non-specific EOI on the trailing edge of the second INTA cycle.
	0	(X): Don't Care.

Table 4-120. *Name: INTC2 Operational Command Word #1 (READ/WRITE)*

Addr	Bits	Values and Functions
0A1H	7	IR7 Mask bit.
		(0): No mask.
		1 : Mask IR7.
	6	IR6 Mask bit.
		(0): No mask.
		1 : Mask IR6.
	5	IR5 Mask bit.
		(0): No mask.
		1 : Mask IR5.
	4	IR4 Mask bit.
		(0): No mask.
		1 : Mask IR4.
	3	IR3 Mask bit.
		(0): No mask.
		1 : Mask IR3.
	2	IR2 Mask bit.
		(0): No mask.
		1 : Mask IR2.
	1	IR1 Mask bit.
		(0): No mask.
		1 : Mask IR1.
	0	IR0 Mask bit.
		(0): No mask.
		1 : Mask IR0.

Table 4-121. Name: INTC2 Operational Command Word #2 (2ND WRITE ONLY)

Addr	Bits	Values and Functions
0A0H	7	Rotate function select. Bit 7 is used in conjunction with bits 6 and 5 to select operational function.
B7	**B6**	**B5**
1	0	0
1	0	1
1	1	0
1	1	1
	6	Specific or immediate function select. Bit 6 is used in conjunction with bits 7 and 5 to select operational function.
B7	**B6**	**B5**
0	1	0
0	1	1
1	1	0
1	1	1
	5	Function related to EOI select. Bit 5 is used in conjunction with bits 7 and 6 to select operational function.
B7	**B6**	**B5**
0	1	0
0	1	1
1	1	0
1	1	1
	4	Interrupt controller out of initialize mode select.
		0 : Disable initialization mode and write OCW2 & OCW3.
		1 : Enable initialization mode.
	3	Operational Command Word Select.
		0 : OCW2 selected.
		1 : OCW3 selected.
	2:0	Bits 2:0 are internally decoded to select which interrupt channel is to be affected by the Specific Command.
		000: IR7.
		001: IR6.
		010: IR5.
		011: IR4.
		100: IR3.
		101: IR2.
		110: IR1.
		111: IR0.

Table 4-122. *Name: INTC2 Operational Command Word #3 (3RD WRITE ONLY)*

Addr	Bits	Values and Functions
0A0H	7	Bit 7 must be set to 0 for proper operation.
	6	Enable Special Mask Mode.
		(0): Special Mask Mode bit becomes a don't care.
		1 : Enable Special Mask Mode bit.
	5	Special Mask Mode.
		(0): Reset Special Mask.
		1 : Set Special Mask.
	4	Interrupt controller out of initialize mode select.
		0 : Disable initialization mode and write OCW2 & OCW3.
		1 : Enable initialization mode.
	3	Operational Command Word Select.
		0 : OCW2 selected.
		1 : OCW3 selected.
	2	Enable Poll Command.
		(0): No Poll Command.
		1 : Poll Command.
	1	Enable Read Register Command.
		(0): Read Register bit becomes a don't care.
		1 : Enable Read Register Command bit.
	0	Read Register Command.
		(0): Read Interrupt Request Register.
		1 : Read In-Service Register.

Table 4-123. *Name: DMA2 Channel 0 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0C0H	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address.
		1	0	1	Write base & current high byte address.

Table 4-124. *Name: DMA2 Channel 0 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0C2H	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-125. *Name: DMA2 Channel 1 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0C4H	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address.
		1	0	1	Write base & current high byte address.

Table 4-126. *Name: DMA2 Channel 1 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0C6H	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-127. *Name: DMA2 Channel 2 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0C8H	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address.
		1	0	1	Write base & current high byte address.

Table 4-128. *Name: DMA2 Channel 2 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0CAH	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-129. *Name: DMA2 Channel 3 Address Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0CCH	7:0	0	1	0	Read current low byte address.
		0	1	1	Read current high byte address.
		1	0	0	Write base & current low byte address.
		1	01	1	Write base & current high byte address.

Table 4-130. *Name: DMA2 Channel 3 Word Count Register (READ/WRITE/FLIP-FLOP)*

Addr	Bits	IOR-	IOW-	FF	Values and Functions
0CEH	7:0	0	1	0	Read current word count low byte.
		0	1	1	Read current word count high byte.
		1	0	0	Write base & current word count low byte.
		1	0	1	Write base & current word count high byte.

Table 4-131. Name: DMA2 Status Register (READ ONLY)

Addr	Bits	Values and Functions
0D0H	7	Channel 3 pending DMA service.
		(0): DRQ3 not active.
		1 : DRQ3 active.
	6	Channel 2 pending DMA service.
		(0): DRQ2 not active.
		1 : DRQ2 active.
	5	Channel 1 pending DMA service.
		(0): DRQ1 not active.
		1 : DRQ1 active.
	4	Channel 0 pending DMA service.
		(0): DRQ0 not active.
		1 : DRQ0 active.
	3	Channel 3 Terminal Count status.
		(0): TC not reached.
		1 : Channel 3 has reached TC.
	2	Channel 2 Terminal Count status.
		(0): TC not reached.
		1 : Channel 2 has reached TC.
	1	Channel 1 Terminal Count status.
		(0): TC not reached.
		1 : Channel 1 has reached TC.
	0	Channel 0 Terminal Count status.
		(0): TC not reached.
		1 : Channel 0 has reached TC.

Table 4-132. Name: DMA2 Command Register (WRITE ONLY)

Addr	Bits	Values and Functions
0D0H	7	DACK input active level.
		(0): DACK active low.
		1 : DACK active high.
	6	DREQ input active level.
		(0): DREQ active low.
		1 : DREQ active high.
	5	Extended Write enable.
		(0): Write commands are asserted late.
		1 : Write commands are asserted one DMA cycle earlier during a transfer.
	4	Priority type for channel servicing.
		(0):Fixed priority.
		1 :Rotating priority.
	3	Transfer compression enable.
		(0):Normal timing
		1 :Compressed timing
	2	Master disable for DMA controller
		(0):DMA controller enable.
		1 :DMA controller disable.
	1	Address hold during memory-to-memory transfers.
		(0):Address hold for Channel 0 disable.
		1 :Address hold for Channel 0 enable.
	0	Memory-to-Memory transfer enable.
		(0):Memory-to-Memory transfers disable.
		1 :Memory-to-Memory transfers for channel 0 and 1 enable.

Table 4-133. Name: DMA2 Request Register (READ ONLY)

Addr	Bits	Values and Functions
0D2H	7:4	(1111): These bits are always set during a read.
	3	Request bit for channel 3.
		(0): No request pending.
		1 : Request pending for channel 3.
	2	Request bit for channel 2.
		(0): No request pending.
		1 : Request pending for channel 2.
	1	Request bit for channel 1.
		(0): No request pending.
		1 : Request pending for channel 1.
	0	Request bit for channel 0.
		(0): No request pending.
		1 : Request pending for channel 0.

Table 4-134. Name: DMA2 Request Register (WRITE ONLY)

Addr	Bits	Values and Functions
0D2H	7:3	(XXXXX): Don't Cares.
	2	Request bit.
		(0): Reset Request bit.
		1 : Set Request bit.
	1:0	DMA Channel Request bit Selection.
		(00): DMA Channel 0.
		01 : DMA Channel 1.
		10 : DMA Channel 2.
		11 : DMA Channel 3.

Table 4-135. Name: DMA2 Command Register (READ ONLY)

Addr	Bits	Values and Functions
0D4H	7	DACK input active level.
		(0): DACK active low.
		1 : DACK active high.
	6	DREQ input active level.
		(0): DREQ active low.
		1 : DREQ active high.
	5	Extended Write enable.
		(0): Write commands are asserted late.
		1 : Write commands are asserted one DMA cycle earlier during a transfer.
	4	Priority type for channel servicing.
		(0):Fixed priority.
		1 :Rotating priority.
	3	Transfer compression enable.
		(0):Normal timing
		1 :Compressed timing
	2	Master disable for the DMA controller.
		(0):DMA controller enable.
		1 :DMA controller disable.
	1	Address hold during memory-to-memory transfers.
		(0):Address hold for Channel 0 disable.
		1 :Address hold for Channel 0 enable.
	0	Memory-to-Memory transfer enable.
		(0):Memory-to-Memory transfers disable.
		1 :Memory-to-Memory transfers for channel 0 and 1 enable.

Table 4-136. *Name: DMA1 Single Bit Request Mask Register (WRITE ONLY)*

Addr	Bits	Values and Functions
0D4H	7:3	(XXXXX): Don't Cares.
	2	Request bit.
		(0): Reset Request bit.
		1 : Set Request bit.
	1:0	DMA Channel Request bit Selection.
		(00): DMA Channel 0.
		01 : DMA Channel 1.
		10 : DMA Channel 2.
		11 : DMA Channel 3.

Table 4-137. *Name: DMA2 Mode Register (READ/WRITE)*

Addr	Bits	Values and Functions
0D6H	7:6	Channel Mode type.
		(00): Demand Mode.
		01 : Single Cycle Mode.
		10 : Block Mode.
		11 : Cascade Mode.
	5	Address counting direction
		(0): Increment address.
		1 : Decrement address.
	4	Auto-initialization enable.
		(0): Auto-initialization function disable.
		1 : Auto-initialization function enable.
	3:2	Type of transfer.
		(00): Verify transfer.
		01 : Write transfer.
		10 : Read transfer.
		11 : Illegal.
	1:0	DMA Channel Mode Selection.
		(00): DMA Channel 0.
		01 : DMA Channel 1.
		10 : DMA Channel 2.
		11 : DMA Channel 3.

Table 4-138. Name: DMA2 Set Byte Pointer Flip-Flop (READ ONLY)

Addr	Bits	Values and Functions
0D8H	7:0	Bits 7:0 are don't cares. The Set Byte Pointer Flip-Flop Clear command is activated as a result of the address 0D8H access and the assertion of IOR-. This command allows the CPU to adjust the pointer to the high byte of an address or word count register.

Table 4-139. Name: DMA2 Clear Byte Pointer Flip-Flop (WRITE ONLY)

Addr	Bits	Values and Functions
0D8H	7:0	Bits 7:0 are don't cares. The Clear Byte Pointer Flip-Flop Clear command is activated as a result of the address 0D8H access and the assertion of IOW-. This command allows the CPU to adjust the pointer to the low byte of an address or word count register.

Table 4-140. Name: DMA2 Temporary Register (READ ONLY)

Addr	Bits	Values and Functions
0DAH	7:0	Bits 7:0 contains values of XD<7:0> during the first cycle of a memory-to-memory transfer. Data from the last memory-to-memory transfer will remain in the register unless a RESET4 or Master Clear occurs.

Table 4-141. Name: DMA2 Master Clear (WRITE COMMAND ONLY)

Addr	Bits	Values and Functions
0DAH	7:0	Bits 7:0 are don't cares. The Master Clear command is activated as a result of the address 0DAH access and the assertion of IOW This command has the same effect as a hardware RESET. The Command Register

Table 4-142. Name: DMA2 Clear Mode Register Counter (READ COMMAND ONLY)

Addre	Bits	Values and Functions
0DCH	7:0	Bits 7:0 are don't cares. The Clear Mode Register Counter command is activated as a result of the address 0DCH access and the assertion of IOR-. This command is provided to allow the CPU to restart the mode read process at a known point. After clearing the counter all four Mode Registers may be read by doing successive reads to the Read Mode Register address. The order in which the registers will be read is Channel 0 first, Channel 3 last.

Table 4-143. Name: DMA2 Clear Request Mask Bits (WRITE COMMAND ONLY)

Addr	Bits	Values and Functions
0DCH	7:0	Bits 7:0 are don't cares. The Clear Mask Register command is activated as a result of the address 0DCH access and the assertion of IOW-. This command enables all four DMA channels to accept requests by clearing the mask bits in the register.

Table 4-144. Name: DMA2 Request Mask Register Bits (READ/WRITE)

Addr	Bits	Values and Functions
0DEH	7:2	(XXXX): Don't Cares.
	3	Channel 0 Mask bit.
		0 : No bit mask
		(1): Bit mask
	2	Channel 1 Mask bit.
		0 : No bit mask
		(1): Bit mask
	1	Channel 2 Mask bit.
		0 : No bit mask
		(1): Bit mask
	0	Channel 3 Mask bit.
		0 : No bit mask
		(1): Bit mask

Table 4-145. Name: Control Port/Status

Addr	Bits	Values and Functions
61H	7	PARITY CHECK (read only). This bit indicates an error has occurred on the planar memory.
		0 = no error occurred.
		1 = an error occurred.
	6	IOCH CHK (read only). This bit indicates an I/O channel check has occurred (usually a parity error) on the system I/O channel.
		0 = no error occurred.
		1 = an error occurred.
	5	TMR 2 OUT (read only). This bit returns the condition of the timer 2 output.
	4	RFSH DETECT (read only). This bit toggles on each refresh cycle.
	3	CHCK DIS (read/write). This bit disables NMI generation for channel check errors.
		0 = disables NMI (default).
		1 = enables NMI.
	2	PARITY DISABLE (read/write). This bit
		0 = parity is enabled (default).
		1 = parity is disabled.
	1	SPKR DATA (read/write). This bit gates the output of channel 2 of the timer/counter.
		0 = output is disabled (default).
		1 = output is enabled.
	0	TMR 2 GATE (read/write). This bit controls operation of timer channel 2.
		0 = channel 2 timer operation is disabled (default).
		1 = channel 2 timer operation is enabled.

82C316 Pin Descriptions

Pin #	Symbol	Type	Signal Description
1	SCLK-	I	SYSTEM CLOCK INPUT is from the 82C315 and is the processor signal used to control 'bus timeout' and 80387 Synchronous reset.
145	TMRCLK	I	TIMER CLOCK is the clock input for Counter 0, Counter 1 and Counter 2 and has a value of 1.19MHz. TMRCLK is connected to the OSC1M19 output of the 82C315.
39	BUSCLK	I	BUS CLOCK is used to generated the timing signals which control the DMA operations. This input may be driven from DC to 10 MHz. The internal clock used for DMAC is either the BCLK or BUSCLK depending on the setting of DMA CLOCK SELECT bit in the configuration register.
141-134	XD<0:7>	I/O	Data bits 0 through 7 are 3-state bi-directional Data Bus lines and are connected to the system data bus, the XD bus in a PC/AT design. The outputs are enabled in the program condition during the I/O READ to output the contents of the DMA controller registers, the three Interrupt Controller registers, the Timer/Counters registers, the Real Time Clock's internal registers, the page registers of the memory mapper, index register 26H, port B, and programmable chip select registers. During an I/O WRITE cycle, the outputs are disabled and the CPU can program the DMA Controller registers, the Interrupt Controller registers, the Timer/Counters registers, the DMA Page register, the Real Time Clock registers, the internal RAM, index register 26H, port B, and programmable chip select registers. During the interrupt sequence, the interrupt controllers output the interrupt vector byte on the data bus. Data bus XD<0:7> also acts as the multiplexed address/data bus for the Real Time Clock.
133	XA24	O	Extended page register address is the most significant address bit coming out of the DMA page register. It is normally not used in an AT compatible design, however, it is possible to use it as an extra feature to extend the DMA address range.
127	IOR-	I/O	I/O READ is an active low bidirectional signal. In an idle cycle, non-DMA or non-interrupt, it is a schmitt-triggered input control signal used by the CPU to read information from the 82C316's internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to access data from a peripheral during a DMA write transfer. This signal has a 24mA drive capability.

Pin #	Symbol	Type	Signal Description
126	IOW-	I/O	I/O Write is an active low bidirectional signal. In an idle cycle, non-DMA or non-interrupt, it is a schmitt triggered input control signal used by the CPU to write information to the 82C316's internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to write data to a peripheral during a DMA read transfer. This signal has a 24mA drive capability.
10	MEMR-	O	MEMORY READ is an active low three-state output and is used to access data from the selected memory location during a DMA read or memory to memory transfers. This output has a 24mA drive capability.
9	MEMW-	O	MEMORY WRITE is an active low three-state output and is used to write data to the selected memory location during DMA write or memory to memory transfers. This output has a 24mA drive capability.
131	IOCHRDY	I/O	I/O CHANNEL READY is a bidirectional signal. During input mode, driving IOCHRDY low causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA Clock cycle will elapse before internal DMA Ready goes high. This signal is used to extend memory read and write pulses for the DMA controllers to accommodate slow memories or I/O devices. During output mode, this pin is an open drain output and provides an active low output whenever any 82C316 register is addressed for a read or write. IOCHRDY provides a means of introducing a programmed number of wait-states for I/O read/write cycles to the 82C316. As an output IOCHRDY has a 8mA drive capability.
72	HLDA1	I	HOLD ACKNOWLEDGE 1 is an active high input signal from the 82C311 and indicates the CPU has relinquished control of the system busses in response to HRQ1.
32	RESET3	I	RESET3 is an active high input from the 82C311. RESET3 is OR'ed with 80387 Synchronous RESET to generate RES387 for the 80387 RESET in revision 0 of 82C316.
125	RESET4	I	RESET4 is an active high input from 82C311 which effect the following registers: DMA Controllers - Clear the command, Status, DMA Request, Temporary register, First/Last flip-flop; sets the mask register. Following reset, the DMA controller is in an idle state. INTERRUPT Controller: Clears the edge sense circuit, the interrupt mask register, all ICW4 functions, IRQ0 is assigned highest priority, slave address is set to 7, special mask mose is disabled, and status read is set to IRR.
24-21	DREQ<0:3>	I	DMA REQUEST are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. DREQ0 through DREQ3 support 8-bit transfers between 8 bit I/O and 8 or 16 bit system memory. In fixed priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Unused DREQ inputs should be pulled high or low and the corresponding mask bit set.

Pin #	Symbol	Type	Signal Description
11-13	DREQ<5:7>	I	DMA REQUEST are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. DREQ5 through DREQ7 support 16-bit peripheral and 16-bit system memory. In fixed priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Unused DREQ inputs should be pulled high or low and the corresponding mask bit set. DREQ<4:7> lines have internal 10K pullups.
14-16	DACK<5:7>-	O	DMA ACKNOWLEDGE is an active low output signal and is used to notify the individual peripherals when one has been granted a DMA cycle. The active polarity of these lines is programmable. This signal has a 4mA drive capability.
5	HRQ	O	HOLD REQUEST is an active high output and is used to request control of the system bus. HRQ is normally connected directly to 82C311's HRQ1 pin. However, HRQ may be tied to HLDA. This will result in one SO state before the transfer. This signal has a 4mA drive capability.
7	AEN16-	O	ADDRESS ENABLE FOR 16-BIT DMA TRANSFERS is an active low signal and is the output enable for the 8-bit latch containing the upper 8 address bits (A9-A16). It is inactive when external bus master controls the system bus. This signal has a 4mA drive capability.
147	IRQ1	I	INTERRUPT REQUEST 1 is an asynchronous input. An interuupt request is executed by raising an IRQ1 from low to high and holding it high until it is acknowledged (edge triggered mode) or just a high level on an IRQ input (level triggered mode). This signal has a 10K internal pullups.
148-152	IRQ<3:7>	I	INTERRUPT REQUESTS 3 through 7 are asynchronous inputs. An interrupt requestis executed by raising an IRQ input from low to high and holding it high until it is acknowledged (edge triggered mode) or just a high level on an IRQ input (level triggered mode).
3	OSCI/IRQ8	I	OSCILLATOR INPUT is a schmitt triggred input used as a time base for the time functions. External square waves of 32.768KHz may be connected to this input. When the external RTC is enabled through index register 26H, this pin is conneceid to IRQ8 instead of OSC.
153-158, 160	IRQ<9:15>	I	INTERRUPT REQUESTS 9 through 15 are asynchronous inputs and are executed by raising an IRQ input low to high and holding it high until it is acknowledged (edge triggered mode) or just a high level on an IRQ input (level triggered mode). These signals have internal 10K pullups.
30	INTA-	I	INTERRUPT ACKNOWLEDGE from 82C311 is an active low signal and is used to enable the interrupt controllers interrupt vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
4	INTR	O	INTERRUPT goes high whenever a valid interrupt request is asserted and is connected to the 80386 to interrupt the CPU. This signal has a 4mA drive capability.
129	INTCLR	O	INTERRUPT CLEAR is an active high output signal and is used to clear IRQ13 on the 82C315. INTCLR is generated during RESET, Out command to port F1H, or Out command to port F0. This signal has a 4mA drive capability.
132	READY-	I/O	READY is the system ready signal to the CPU. It is an active low input after the requested local memory or AT cycle is completed. It is an output during the 387/coprocessor cycle and READY time out. This signal has a 4mA drive capability as an open drain output.

Pin #	Symbol	Type	Signal Description
116	OUT1	O	OUTPUT 1 is the output of TIMER 1 and is programmed as a rate generation to produce a15uS period signal used for interrupt request for refresh cycles. This signal has a 4mA drive capability.
143	PSRSTB-	I	PSRSTB- is an active low input and is used to establish the condition of the control registers when power is applied to the device. In a PC/AT compatible design, this pin should be tied to the battery back-up circuit.
144	PWRGD	I	POWER GOOD must be high for all bus cycles in which the CPU accesses the 82C316. When PWRGD is low, all address, data, data strobe and R/W pins are disconnected from the processor.
33	READYO-	I	NUMERICAL PROCESSOR READY OUTPUT is an active low input and is connected directly to the READYO- pin of the 80387 COPROCESSOR. This pin is active only during bus cycles that select the numerical processor. It has a 10K internal pullup.
31	RES387	O	RESET OUTPUT is an active high output and is used to reset the 80387 Numerical Processor. This signal has a 4mA drive capability.
25	IO2XCS-	O	IOX2CS- CHIP SELECT is a active low output signal and is a I/O decode of addresses 022H OR 023H. IO2XCS- in conjunction with XA00 is used to access the IO internal registers at 022H or 023H in the 82C311 and 82C315. This signal has a 4mA drive capability.
26	8042CS-	O	8042 CHIP SELECT is a active low signal and is a I/O decode of addresses 060H or 064H. This signal has a 4mA drive capability.
27	XDIR	O	X BUS DIRECTION controls within the 82C315 the direction of data transfer between the peripheral bus and the IO channel. When low XDIR should drive the SD bus signals toward the XD bus. When high XDIR should drive the XD bus signals toward the SD bus. This signal has a 4mA drive capability.
76	MASTER-	I	BUS MASTER IS active low input signal from AT expansion bus from AT expansion bus from AT expansion bus and is generated by a device active on the AT expansion Bus. It is pulled high with 10K Ohm resistor.
115	MALE-	I	MEMORY ADDRESS LATCH ENABLE clocks local addresses into the address registers on the rising (trailing) edge.
75	REF-	I	REFRESH is an active low input from 82C311 or an I/O device on the AT bus which incruments the address counter and controls the address buffer direction. When active, the contents of the refresh address counter is gated to the SA address bus. On the rising edge of REF-, the internal refresh counter is incremented.
73	ATEN-	I	AT BUS ENABLE is an active low input signal from 82C311 and is active when the CPU makes an AT Bus access.
40, 44	XA<0:1>	I/O	EXPANSION ADDRESS bits 0 and 1 are bidirectional signals. These signals have a 4mA drive capability.
45-50, 52-59, 2, 62-69	A<2:23>	I/O	LOCAL ADDRESS bus bits through 23 are bidirectional signals, inputs during the CPU AT cycle and output during DMA/master cycles. These signals have a 4mA drive capability.
77-79, 81, 83-86, 89-92, 94-97, 100-103	SA<0:19>	I/O	IO CHANNEL ADDRESS bus bits 0 through 19 are bidirectional signals. These signals have a 24mA drive capability.

Pin #	Symbol	Type	Signal Description
105-107, 110-113	LA<17:23>	I/O	LOCAL ADDRESS bus bits 17 through 23 are bidirectional signals and are connected to the AT IO channel. As outputs, they generate memory decodes for memory cycles. They also may be driven by the microprocessor or DMA controller that resides on the I/O channel. These signals have a 24mA drive capability.
117	NMI	O	NON-MASKABLE INTERRUPT is an active high output and is connected to the NMI of the CPU. This input signal has a 4mA drive capability.
34	LPAR-	I	LATCHED PARITY ERROR is an active low input and indicates a parity error during a DRAM read. When active it will cause an NMI to be generated.
36	IOCHCK-	I	I/O CHANNEL CHECK is an active low input and is used to signal an error condition form an I/O device. When active and enabled, it causes an NMI to be generated.
124	PGMCS1-	O	PROGRAMMABLE I/O PORT 1 CHIP SELECT is an active low output and becomes active when the programmed address or address range is accessed during an I/O READ or WRITE cycle. The 16 bit address is programmed at locations 71H and 72H. Its range and command enable is programmed at location 73H. This signal has a 4mA drive capability.
123	PGMCS2-	O	PROGRAMMABLE I/O PORT 2 CHIP SELECT is a active low output and becomes active when the programmed address or address range is accessed during an I/O READ or WRITE cycle. The 16 bit address is programmed at locations 74H and 75H. It's range and command enable is programmed at location 76H. This signal has a 4mA drive capability.
122	PGMCS3-	O	PROGRAMMABLE I/O PORT 3 CHIP SELECT is a active low output and becomes active when the programmed address or address range is accessed during an I/O READ or WRITE cycle. The 16 bit address is programmed at locations 77H and 78H. It's range and command enable is programmed at location 79H. This signal has a 4mA drive capability.
120	SPKR	O	SPEAKER gates the speaker data and Timer Out 2 to drive the internal speaker. This signal has a 4mA drive capability.
119	RTCDS	O	RTC DATA STROBE is an active high output and is used to control the bi-directional bus on an external MC146818 REAL-TIME CLOCK plus RAM peripheral device. During a READ cycle, a high RTCRW signal, the RTCDS output drives the bus with the read data. On the other hand, during a WRITE cycle, a low RTCRW signal, the RTCDS's trailing edge causes the MC146818 to latch the written data. This signal has a 4mA drive capability.
118	RTCRW	O	RTC R/W CONTROL OUTPUT is an output and is used to indicate a READ or WRITE mode for an external MC146818 REAL-TIME CLOCK plus RAM peripheral device. A high level on RTCRW indicates to the MC146818 that the current cycle is a READ cycle. A low level on RTCRW indicates to the MC146818 that the current cycle is a WRITE cycle. This signal has a 4mA drive capability.
37	RTCAS	O	REAL TIME CLOCK ADDRESS STROBE is an active high output and is used to demultiplex the bus on an external MC146818 REAL-TIME CLOCK plus RAM peripheral device. The falling edge of RTCAS causes the address to be latched within the MC146818. This signal has a 4mA drive capability.
35	PCUNMIIN	I	POWER CONTROL UNIT NONMASK INTERRUPT INPUT is a programmable input from the Power Control Unit. It is an active low input signal by default and can be programmed by bit 3 of index register 26H. PCUNMIIN should be tied to Vcc for the 82C316 to operate correctly.

Pin #	Symbol	Type	Signal Description
142	TEST	I	TEST is an active high input. It initializes various internal registers so that the test program starts in a known state. It should be tied low for normal operation.
42	EADS-	O	external address strobe Indicates a valid external address on the bus. This address will be used to perform an internal cache invalidation cycle.
38, 61, 70, 80, 88, 99, 109, 121, 146, 159	VCC		Voltage Supply, +5± 5%. Stand-by voltage supply, +3.0V.
2, 28, 41, 43, 51, 60, 71, 74, 82, 87, 93, 98, 104, 108, 114, 128, 130	VSS	I	GROUND.

82C316 Maximum Ratings and Operating Conditions

82C316 Absolute Maximum Ratings	Symbol	Min.	Max.	Units
Supply Voltage	Vcc		7.0	V
Input Voltage	V_I	-.5	5.5	V
Output Voltage	V_O	-.5	5.5	V
Operating Temperature	Top	-25	85	C
Storate Temperature	Tstg	-40	125	C

Note Exposure to absolute maximum ratings conditions for extended periods may affect device reliability. Exceeding the absolute maximum ratings can cause permanent damage to the device.

82C316 Absolute Maximum Ratings	Symbol	Min.	Max.	Units
Supply Voltage	Vcc	4.75	5.25	V
Input Voltage	T_A		70	C

DC Characteristics

	DC Parameter	Min.	Max	Units
Vil	(all pins except SCLK and PCLK)		0.8	V
Vih	(all pins except SCLK and PCLK)	2.0		V
Vil	(SCLK and PCLK)	-0.3	0.8	V
Vih	(SCLK and PCLK)	Vcc -0.8	Vcc +0.3	V
Vol			0.45	V
Voh	(all pins except IOCHRDY and READY)	2.4		V
IIL	(except IR15, IR14-9, IR7-3, IR1, DREQ 5-7, DREQ 0-3, READY0, IOCHCK)		±10	µA
IIH	(except PWRGD)		±10	µA
IIL	(IR15-9, IR7-3, IR1, DREQ 5-7, DREQ 0-3, READYOB, IOCHCKB)		-1	mA
IIH	PWRGD		200	µA
	3-state output OFF curent LOW		±10	µA
	3-state output OFF current HIGH		±10	µA
IOL	(all pins except SA0-19, LA17-23, IOR, IOW, READY, IOCHRDY, TC, MEMR, MEMW, AEN)	4		mA
IOL	(SA0-19, LA17-23, IOR, IOW, TC, MEMR, MEMW, AEN)	24		mA
IOL	(READY, IOCHRDY)	8		mA
IOL	(all pins except SA0-9, LA17-23, IOR, IOW, READY, IOCHRDY, TC, MEMR, MEMW, AEN)	-4		mA
IOH	(SA0-19, LA17-23, IOR, IOW, TC, MEMR, MEMW, AEN)	-3.3		mA
IOH	(READY, IOCHRDY)	-8		mA
ICC	Dynamic	60		mA
ICC	Static (OSC = 32.768KHz, Vcc = 5V)	10		µA

AC Characteristics

All timing parameters are specified under capacitive load of 50 pf and temperature of 70 decree C. All the units discussed in the following timing tables are in nanoseconds, unless otherwise specified. Also, the AC specifications mentioned in this document are subject to change.

Table 4-146. CPU AT Cycle

	CPU AT Cycle	Min.	Max
t601	A<23:0> setup to MALE- high	15	
t602	A<23:0> hold to MALE- high	10	
t603	SA<19:0> valid from ATEN- low	0	50
t604	LA<23:17> valid from ATEN- low	0	26
t605	SA<19:0> float from ATEN- high	0	25
t606	LA<23:17> float from ATEN- high	0	30
t607	IO2XCS- active from MALE- high	10	46
t608	8042CS- active from MALE- high	0	60
t609	PGMCS<3:1>- active from command active		30
t610	IO2XCS- inactive from MALE- high	0	32
t611	8042CS- inactive from command inactive	0	32
t612	PGMCS<3:1> inactive from IOW- high		27

Table 4-147. Master Cycle

	Master Cycle	Min.	Max
t615	A<23:2> valid from LA & SA	6	35
t616	XA<1:0> valid from SA	5	30
t617	IO2XCS- active from SA valid	10	60
t618	8042CS- active from SA valid	10	60
t621	XA<1:0> invalid from MASTER	6	19

Table 4-148. DMA Cycle

	DMA Cycle	Min.	Max
t625	BUSCLK period (1X)	125	
t625A	BUSCLK period (2X)	62	
t626	BUSCLK high time (1X)	55	
t626A	BUSCLK high time (2X)	27	
t627	BUSCLK low time (1X)	43	
t627A	BUSCLK low time (2X)	22	
t628	DREQn setup to BUSCLK low	0	
t629	HRQ delay from BUSCLK low	70	
t630	HLDA setup to BUSCLK high	40	
t631	AEN8/16- valid from BUSCLK low		95
t632	AEN8/16- invalid from BUSCLK		75
t633	AEN active from HLDA1 active	5	38
t651	AEN inactive from HLDA1 low	5	50
t634	Address valid from BUSCLK high		100
t635	Address hold from BUSCLK high		50
t636	DACKn valid from BUSCLK low		100
t637	Command enable dly from BUSCLK high		80
t638	Command active dly from BUSCLK high		100
t639	Write cmnd inactive dly from BUSCLK high		70
t640	Address hold from Write high	70	
t641	Address hold from MEMR- high	50	
t642	Command float dly from BUSCLK high		75
t643	IOR- inactive dly from BUSCLK high		115
t644	TC delay from BUSCLK		50
t649	IOCHRDY setup to BUSCLK low	25	
t650	IOCHRDY hold from BUSCLK low	15	

Table 4-149. Internal Register Access

	Internal Register Access	Min.	Max
t655	Command active period	150	
t656	XD<7:0> active from IOR- low	0	35
t657	XD<7:0> valid from IOR- low		140
t658	XD<7:0> hold from IOR- high	8	
t659	XD<7:0> setup to IOW- inactive	130	
t660	XD<7:0> hold from IOW- high	20	
t663	IOCHRDY active delay from cmnd	6	30
t664	IOCHRDY inactive dly from BUSCLK high	6	25
t665	NMI valid delay from IOW- high	20	

Table 4-150. *Internal Register Access*

	Internal Register Access	Min.	Max
t666	RTCAS active dly from IOW- low	5	40
t667	RTCAS inactive dly from IOW- high	5	40
t668	Cycle time	960	DC
t672	RTCDS active dly from IOR- low	5	28
t673	RTCDS inactive dly from IOR- high	5	28

Table 4-151. *INTA Sequence*

	INTA Sequence	Min.	Max
t682	IRQn pulse width (low)	100	
t683	IRQn pulse width (high)	200	
t684	INT active delay from IRQn high		300
t685	XD<7:0> valid from INTA- active		120
t686	XD<7:0> hold from INTA- inactive	8	

Table 4-152. *Miscellaneous Signals*

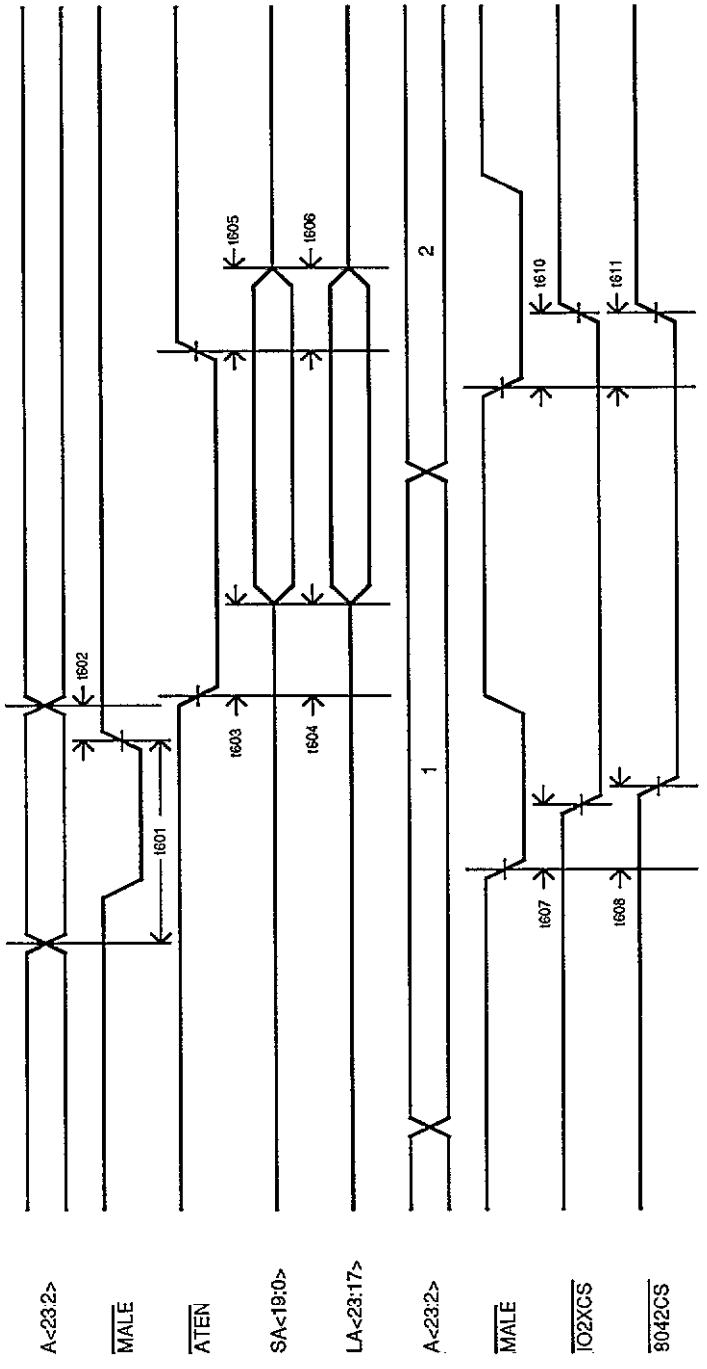
	Miscellaneous Signals	Min.	Max
t690	TMRCLK period	125	DC
t691	TMRCLK high time	50	
t692	TMRCLK low time	50	
t693	SPKR delay from TMRCLK low		25
t694	OUT1 delay from TMRCLK low		40
t695	OSC1 period	500	
t696	OSC1 high time	200	
t697	OSC1 low time	200	
t698	PSRST- inactive dly from Vcc	5us	
t699	PSRST- low pulse width	5us	
t6100	VRT bit valid delay(intrnl)		2us
t6105	XDIR high from INTA- active	3	30
t6106	XDIR high from IOR- active	3	30
t6107	XDIR low from INTA- inactive	3	25
t6108	XDIR low from IOR- inactive	3	25
t6110	SA valid from REF- active	13	50
t6111	SA hold from REF- inactive	0	25
t6112	AEN active from REF- active		40
t6113	AEN inactive from REF- inactive	21	
t6115	READYO- setup to SCLK- high	12	

Table 4-152. Miscellaneous Signals (continued)

	Miscellaneous Signals	Min.	Max
t6116	READYO- hold to SCLK- high	8	
t6117	READY- active dly from SCLK- high	0	15
t6118	READY- inactive dly from SCLK high	0	15
t6121	LPAR- pulse width	15	
t6122	IOCHCK- pulse width	15	
t6123	PCUNMIIN pulse width	15	
t6130	INTCLR active dly from IOW- low		35
t6131	RES387 active dly from SCLK- high		21
t6132	RES387 pulse width		64 SCLK-
t6133	RES387 inactive dly from SCLK- low		8
t6134	IOCHRDY pulse width		96 SCLK-
t6135	INTCLR inactive dly from IOW- high		40
t6136	RES387 active dly from RESET3 high		18
t6137	RES387 inactive dly from RESET3 low		20
t6138	INTCLR active dly from RESET3 high		18
t6139	INTCLR inactive dly from RESET3 low		18

Timing Diagrams

Figure 4-13. *82C316 Address Buffers Timing for CPU AT Cycle*



Note : HLDA, REF, MASTER inactive

82C316 Address Buffers Timing for CPU AT Cycles

Figure 4-14. *82C316 Master Cycle*

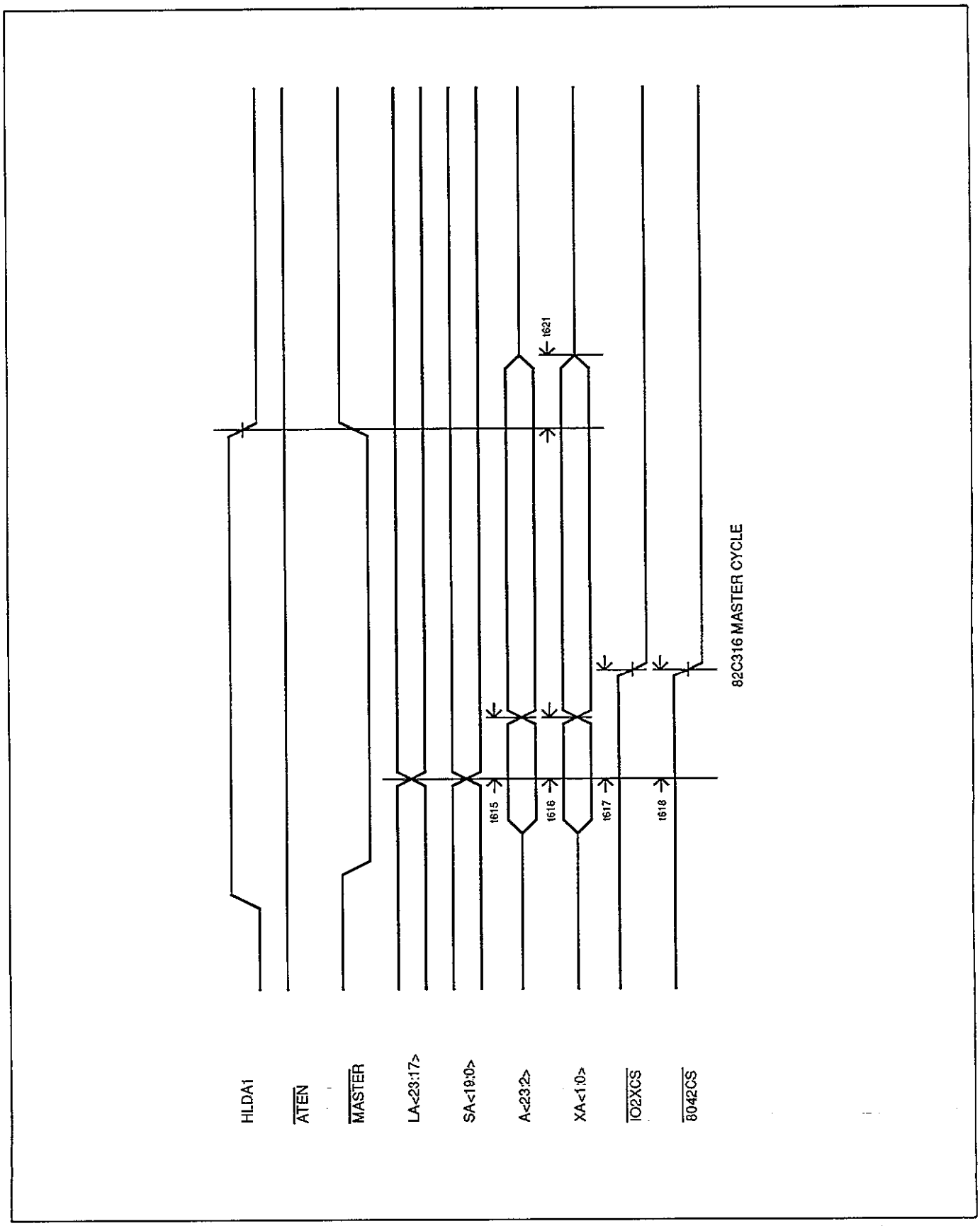
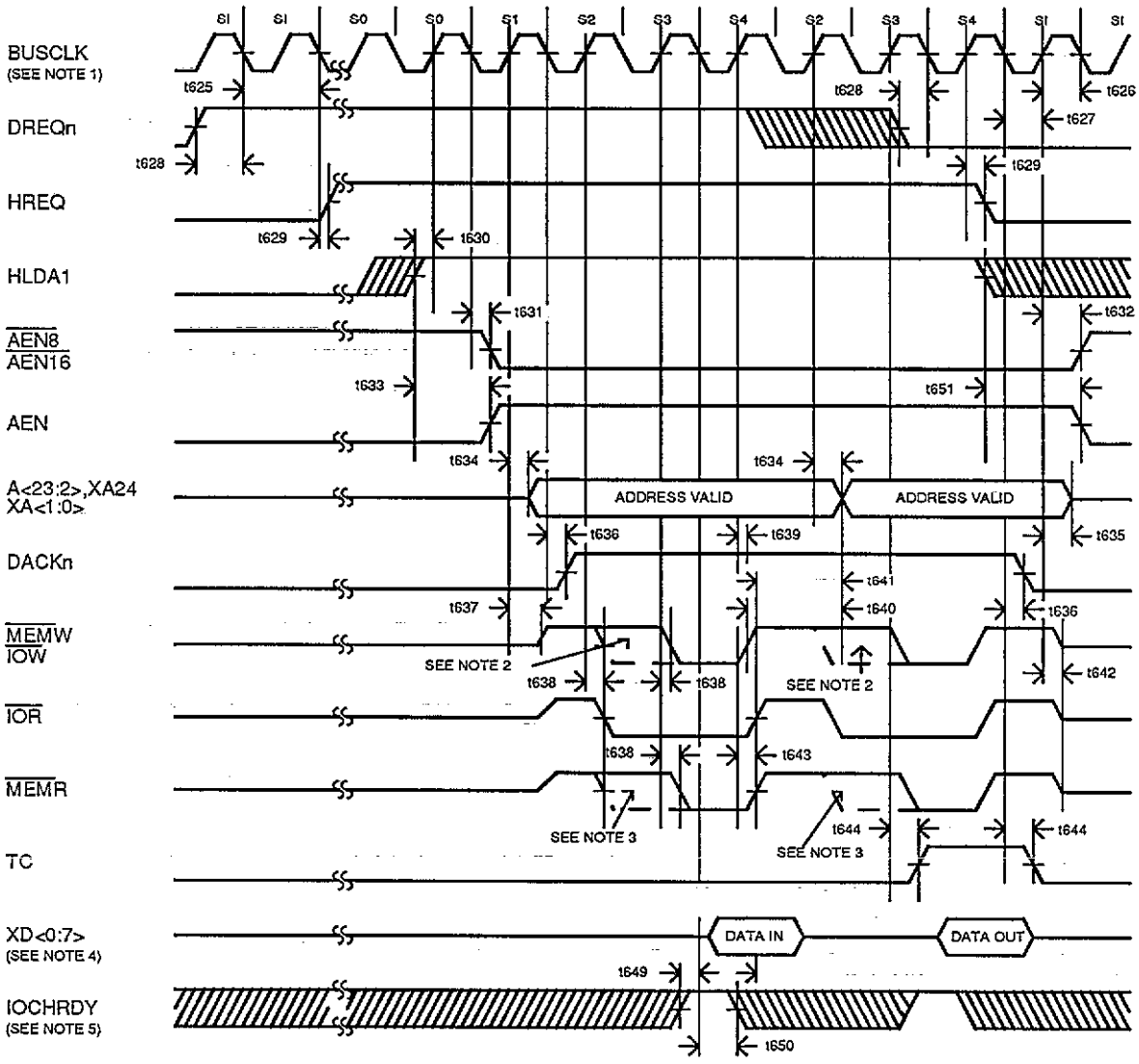


Figure 4-15. *82C316 DMA Cycle*



82C316 DMA Cycle

NOTES:
1. All timings referenced to BUSCLK are independent of the state of the clock select bit in the configuration register. BUSCLK shown in this diagram is the undivided clock directly from the input.
2. Extended write mode selected.
3. Extended read mode selected.
4. Data bus during memory to Memory Transfer.
5. IOCHRDY input timing

Figure 4-16. *82C316 Internal Register Access*

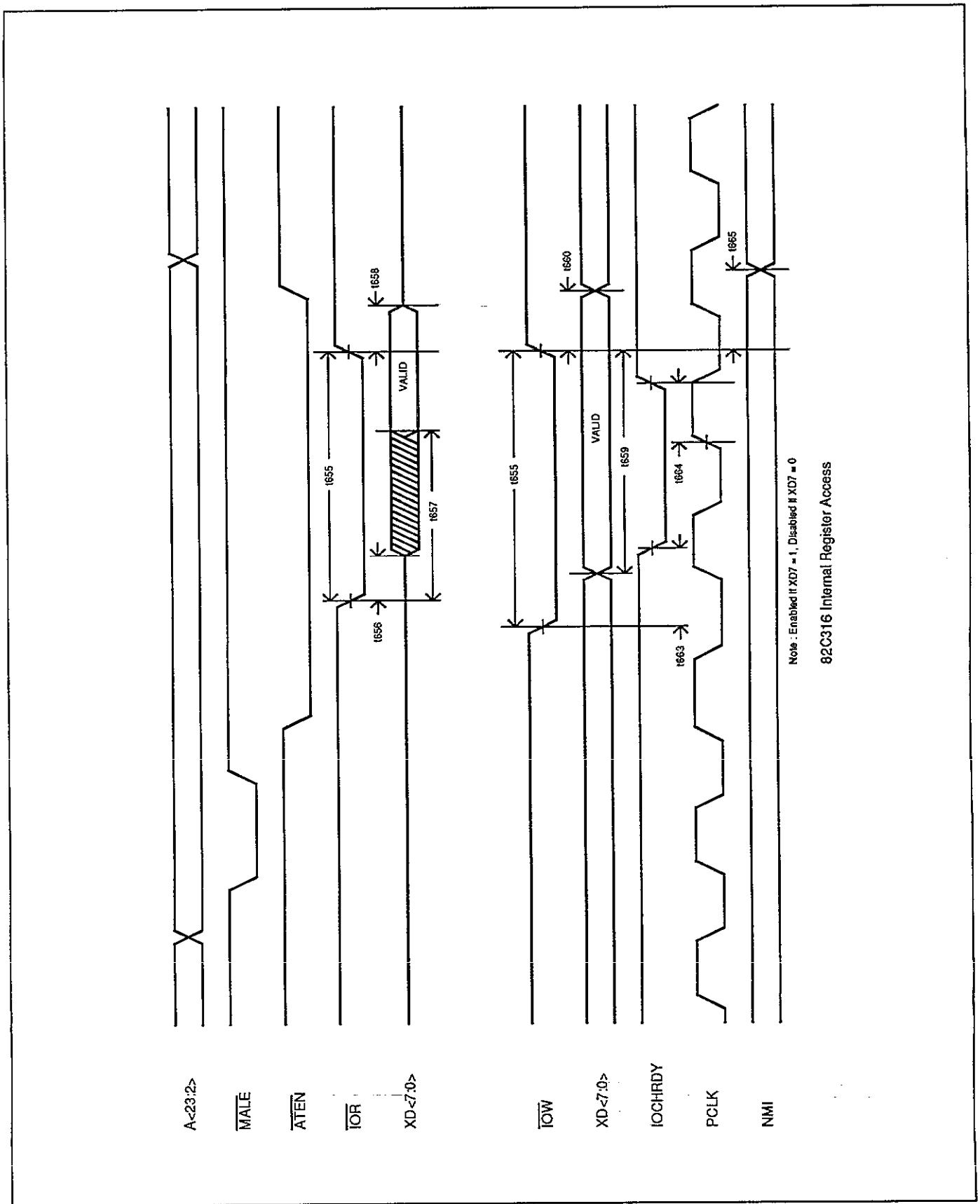


Figure 4-17. *82C316 INTA Sequence*

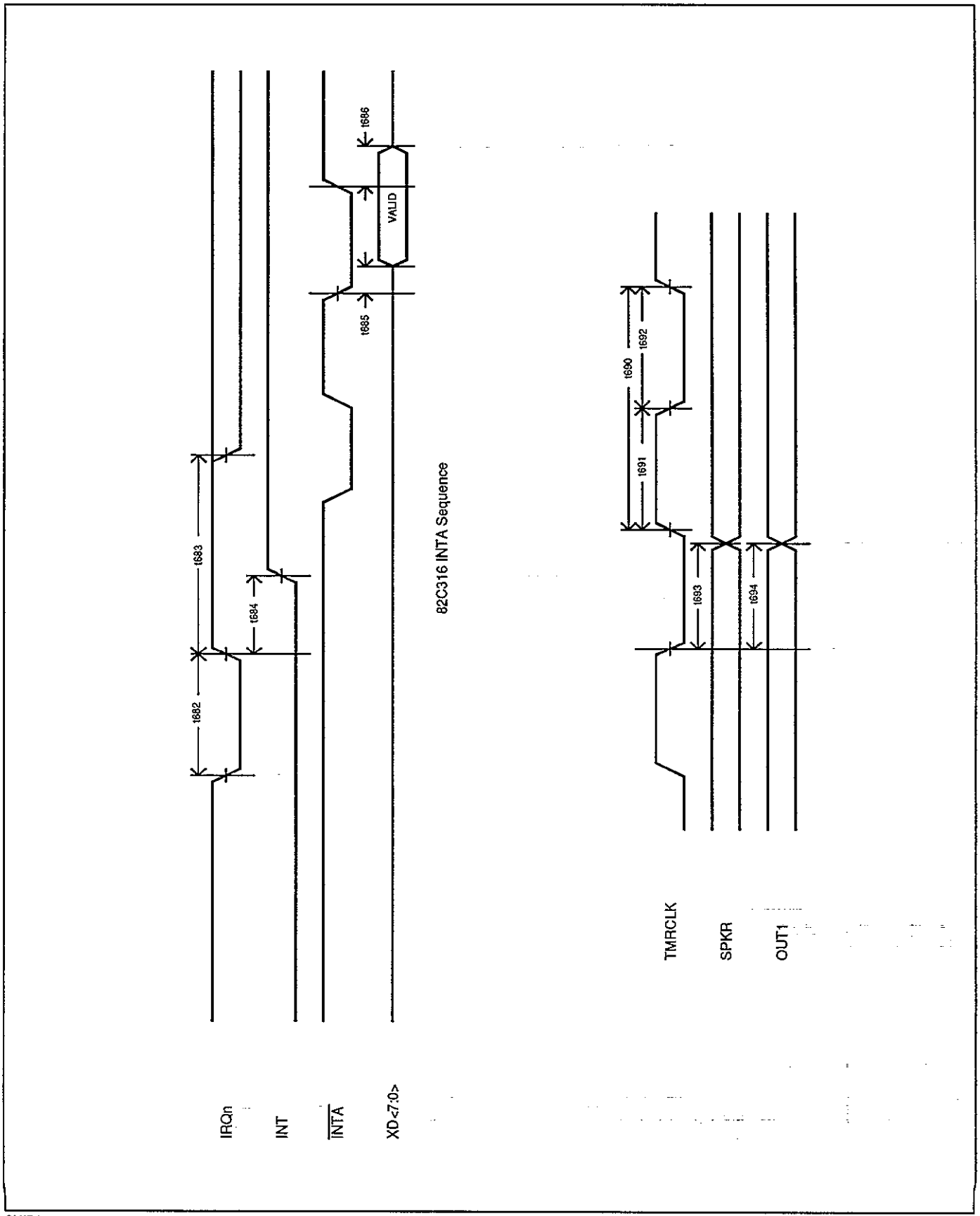
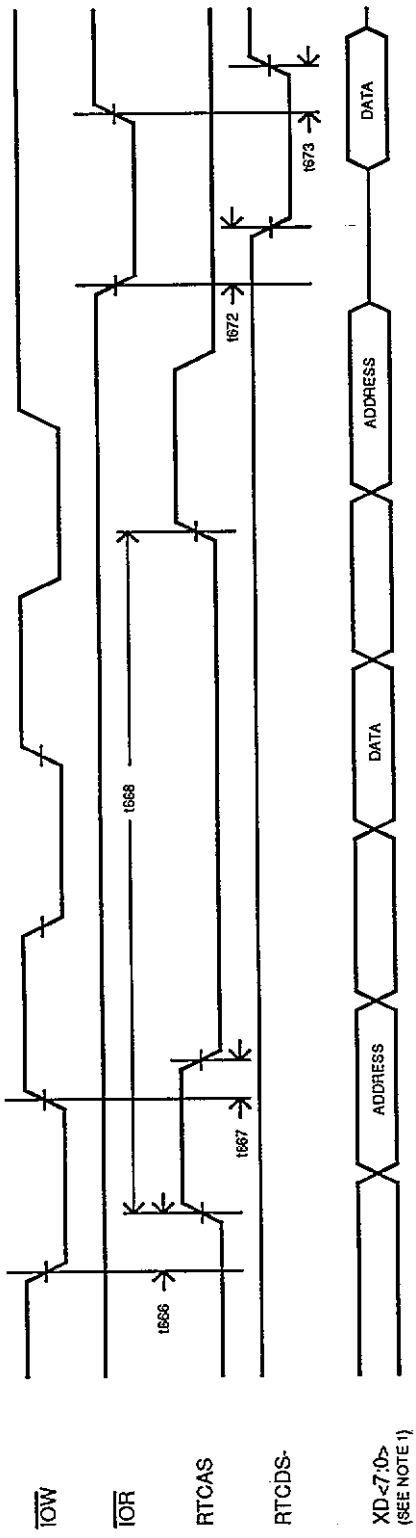


Figure 4-18. *82C316 External RTC Timing*



Note : 1. Timing requirements for XD<7:0> are shown for completeness. They are required by the MC146818A but not the 82C316.

82C316 External RTC Timing

Figure 4-19. *82C316 PGMCS <3:1>, VRT Timing*

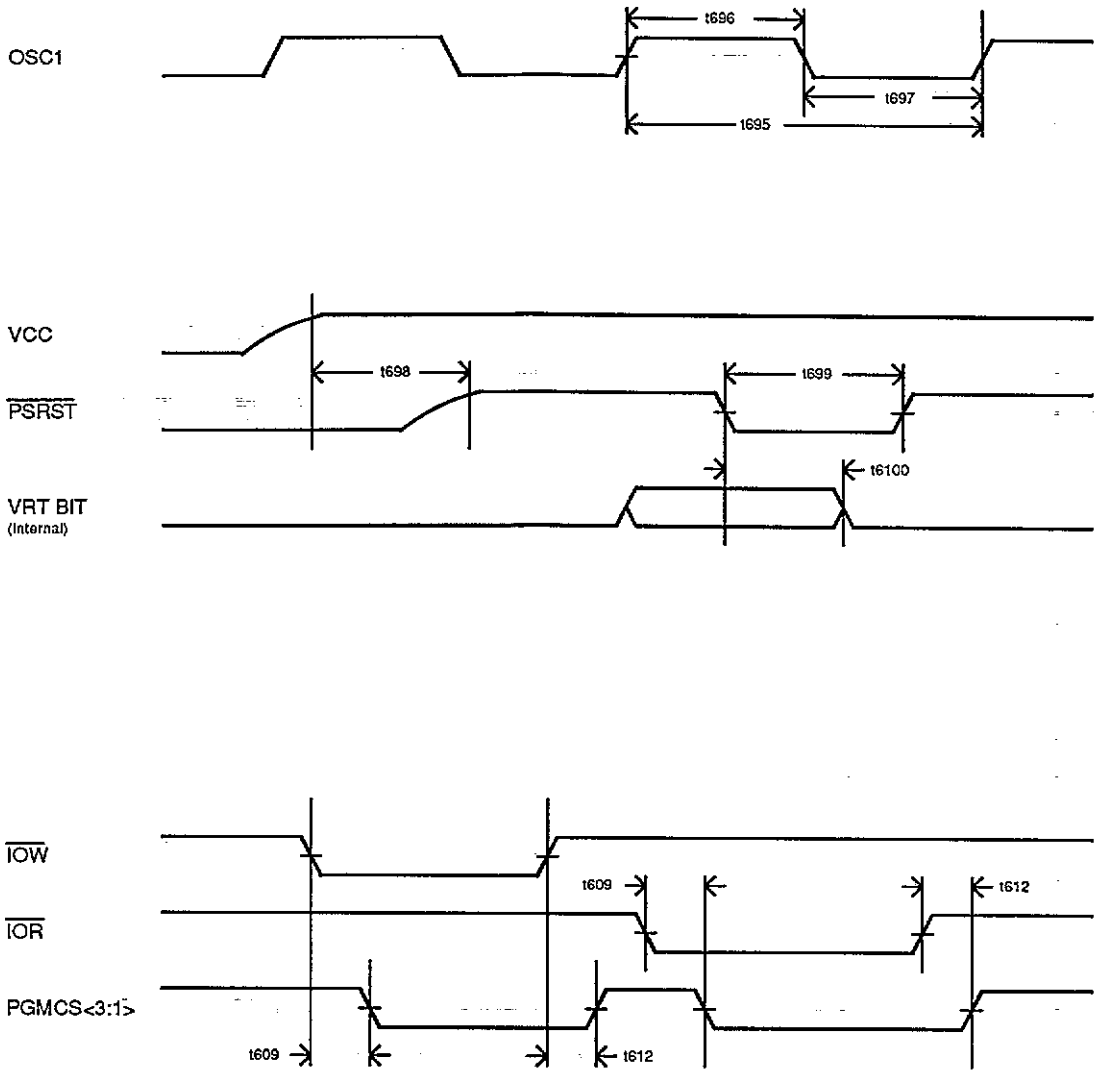
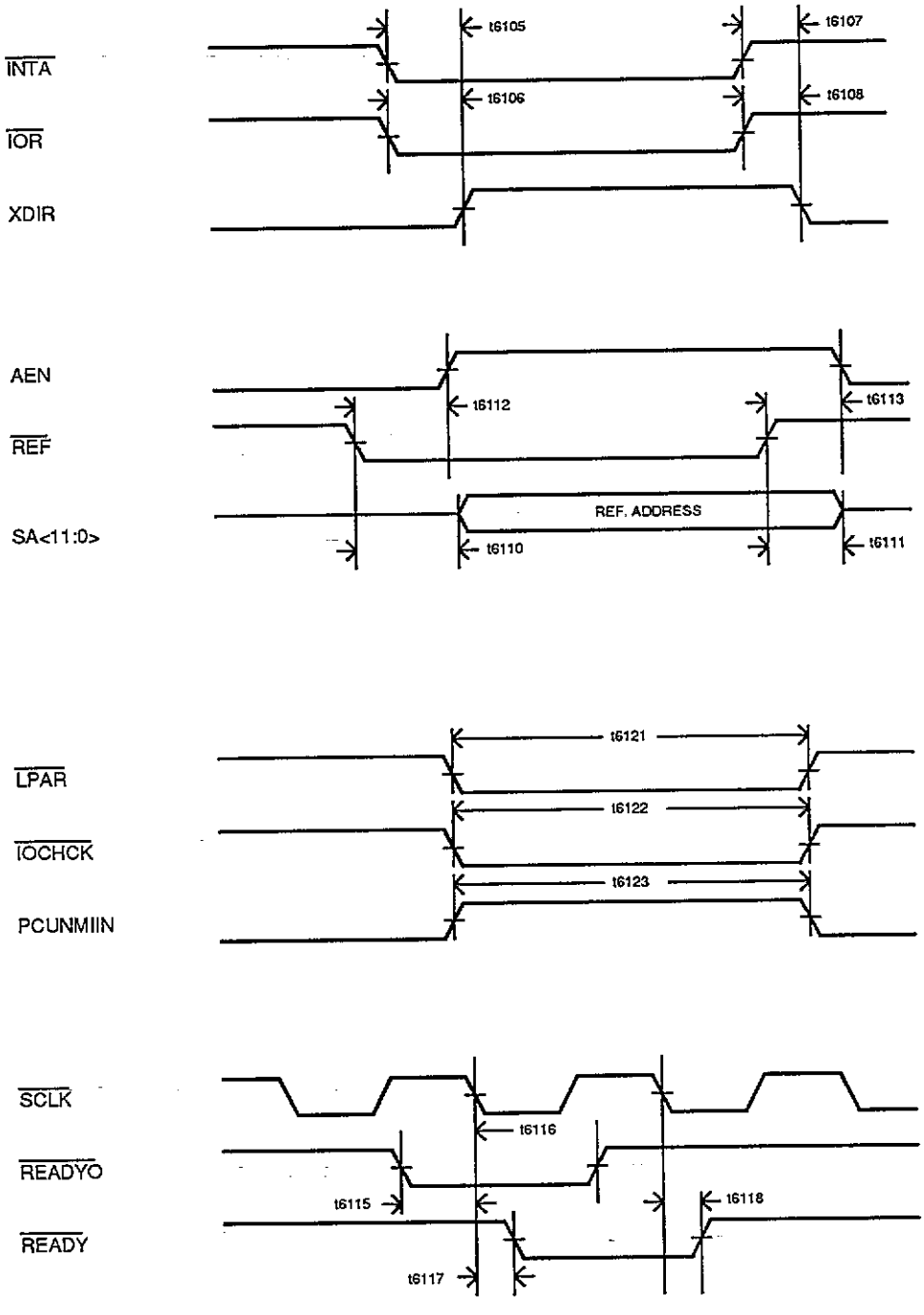


Figure 4-20. *82C316 Miscellaneous Signals*



82C316 MISC SIGNALS

Figure 4-21. *82C316 80387 RESET Timing*

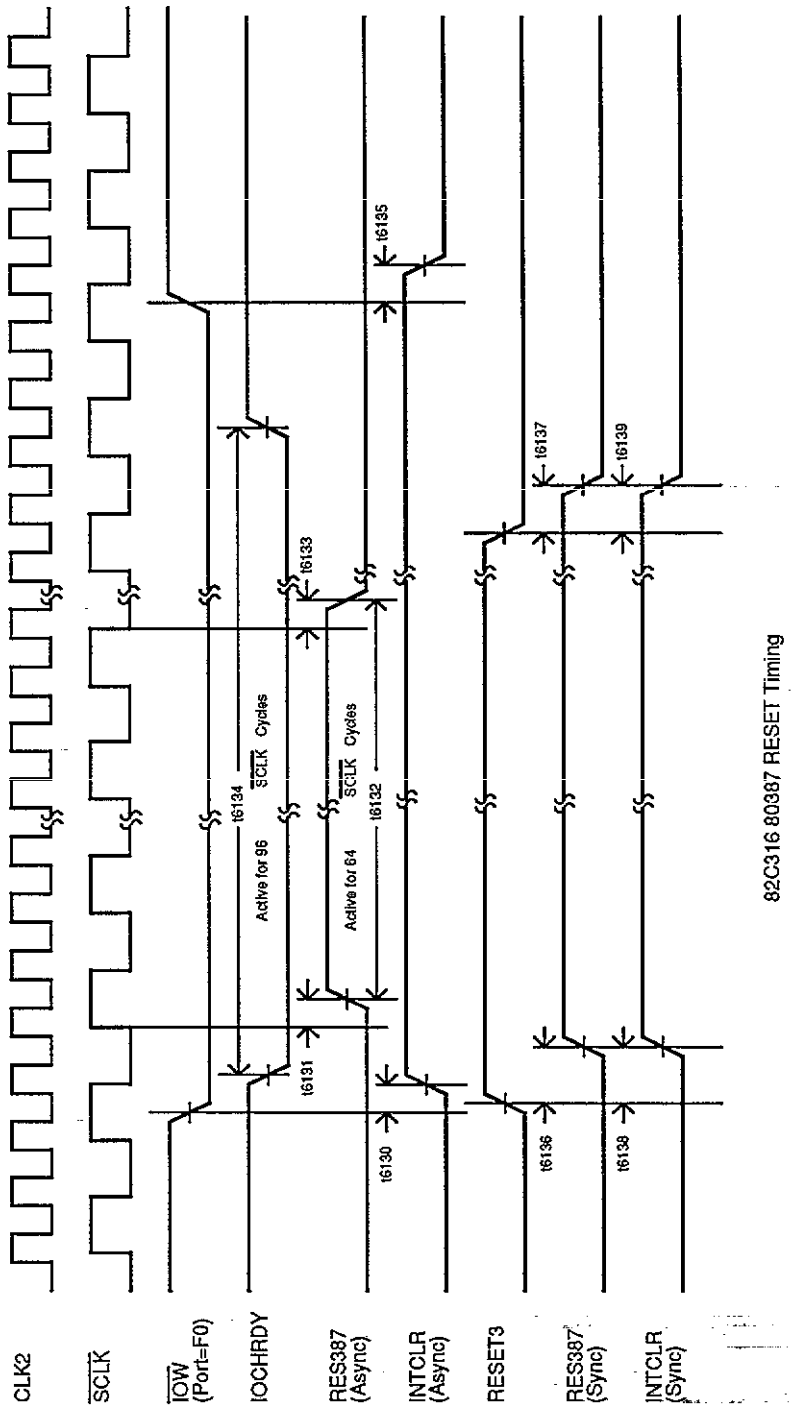


Figure 4-22. *82C316 Pin Diagram*

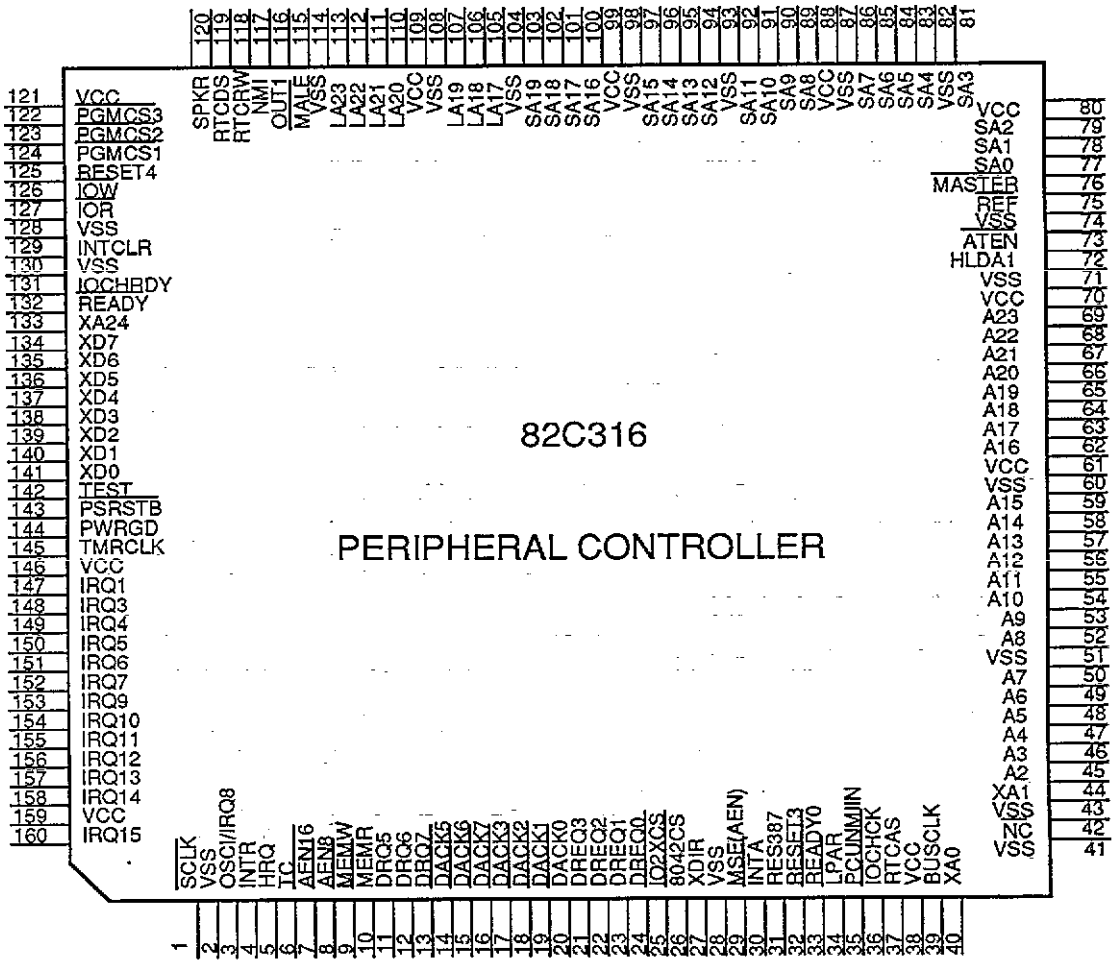
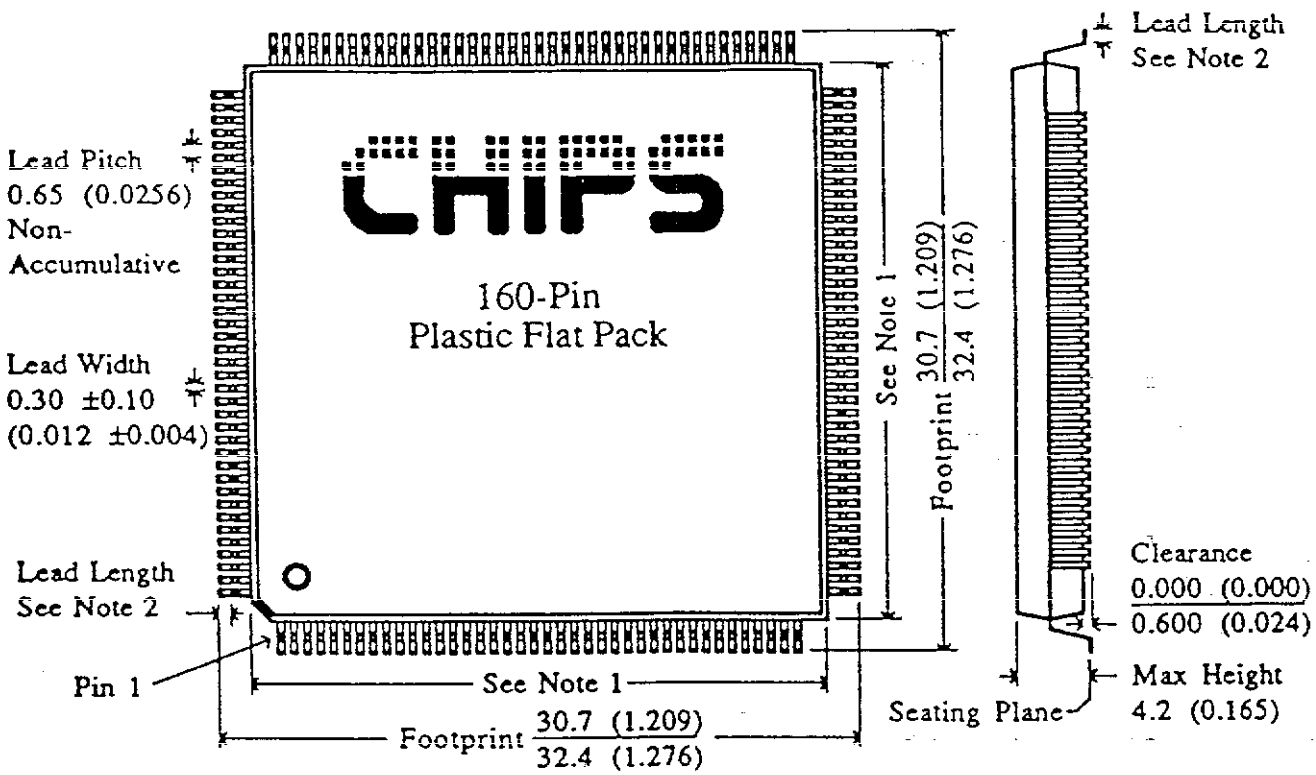


Figure 4-23. Mechanical Dimensions

DIMENSIONS: mm (in)



Note 1: Package Body Size = 28 +0.2/-0.4 (1.102 +0.008/-0.016) (Swire)
Package Body Size = 28 ±0.2 (1.102 ±0.008) (All Other Package Vendors)

Note 2: Lead Length = 0.6 ±0.3 (0.024 ±0.012) (Package Vendor = Seiko)
Lead Length = 0.7 ±0.2 (0.028 ±0.008) (Package Vendor = Yamaha)
Lead Length = 0.8 ±0.2 (0.031 ±0.008) (All Other Package Vendors)