T-49-17-40

CS82310
PEAK/DM 386 AT CHIPSet

82C351, 82C355, 82C356

The CS82310 PEAK/DM CHIPSet is a three chip VLSI implementation of the systems logic required to implement a cache-based 386DX system. This CHIPSet is designed to offer a 100% PC/AT compatabile integrated solution. The flexible architecture of the PEAK/DM allows it to be used in any iAPX386-based system design such as CAD/CAE workstations, office systems, industrial and financial transaction systems. The CS82310 PEAK/DM CHIPSet provides a complete cache based 386/AT system using only 19 components plus memory devices. The CS82310 PEAK/DM CHIPSet consists of one 82C351 CPU/cache/DRAM controller, one 82C355 data buffer, and one 82C356 peripheral controller. The CHIPSet supports a local CPU bus, a 32-bit memory bus, and AT buses.

Features

- Supports 25 and 40 MHz 386DX cache based systems, and 20, 25, and 33 MHz 486sx and 486DX based AT compatible systems
- Supports asynchronous AT bus timing through independent clock or division of CPU clock
- Requires only 16 IC's plus memory for a 386/AT cache based PC/AT
- Supports page mode and page interleaved memory controllers
- Supports cache and non-cache systems
- Includes an integrated CPU/Cache/DRAM/bus controller
- Enhanced performance of the 386DX and memory system due to simultaneous activation of cache and DRAM accesses by the integrated controller
  - Zero wait state non-pipelined read hit access
  - Buffered write through DRAM update scheme to minimize write cycle penalty
  - Supports 32KB, 64KB, 128KB and 256KB direct mapped cache
  - Supports 4 blocks (variable size from 4KB to 4MB) of main memory as programmable non-cacheable address space
- Supports up to 128MB of local memory through flexible memory architecture
  - Programmable wait states and RAS precharge time for each block (2 pair of banks)
  - Supports 256KB, 1MB, and 4MB DRAMS in configurations of up to 4 blocks (8 banks)
  - Supports staggered RAS during refresh

82C351 CPU/Cache/DRAM/Controller

By integrating both the cache and DRAM control functions in one chip, the 82C351 supports simultaneous activation of cache and DRAM accesses; minimizing the cache miss penalty. It has hardware support to allow the user to designate up to four blocks (of variable size from 4KB to 4MB) of main memory as non-cacheable address space. The 82C351 cache controller supports a direct mapped cache architecture and cache sizes of 32KB, 64KB, 128KB, or 256KB. Memory write updates are implemented using a buffered write-through scheme. The 82C351 is available in a 160-pin PFP package.

82C355 Data Buffer

The 82C355 bus controller contains the data buffers used to interface the local and system memory buses and a path for the AT data bus. In addition to having high current bus drive, it also performs conversions between the different sized data paths and provides parity generation and checking. The 82C355 is available in a 120-pin PFP package.

82C356 Peripheral Controller

The 82C356 peripheral controller contains the address buffers used to interface between the processor address bus (A<23:2>) and the system address bus (SA<19:0>). It also contains an equivalent 82C206 integrated peripheral controller that incorporates: two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one MC146818 real time clock, and several TTL/SSI interface logic chips.

Figure 1-7. *PEAK/DM System Block Diagram*