CS4031 CHIPSet

84031 and 84035 Chip Set

Advance Product Information

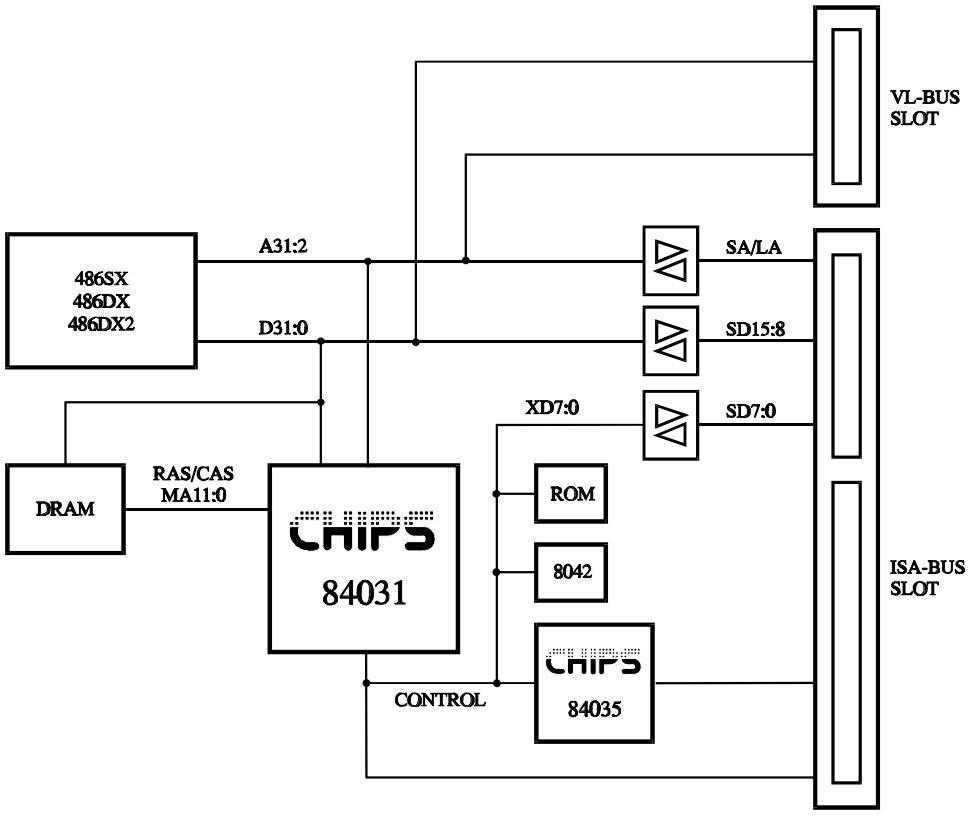
May 1993

P R E L I M I N A R Y

CHIPS®

CS4031 CHIPSet

- Very low-cost and high-integration chip set
- Supports 486SX, 487SX, 486DX, and 486DX2 CPUs
- Operating speeds of up to 33MHz
- Two-chip chip set, no external IPC needed
- Integrated industry-standard CHIPS IPC core; no external RTC needed
- Integrated on-chip oscillators for 14.318MHz and 32.768KHz clocks
- Only 8 TTL devices required for a complete system with one VL-Bus slot
- Full VESA VL-Bus supports up to 3 slots for superior system performance, e.g. graphics
- Patented high-performance "Page-interleave" DRAM controller
- 3-2-2-2 or 4-3-3-3 for reads, and 0 or 1WS for writes
- Up to 64MB memory with 4 banks of DRAM or 32MB with 2 banks
- Supports 256KB, 1MB, 4MB, and 16MB DRAM with a depth of 256K, 1M, or 4M
- Hidden refresh supported for higher performance
- Integrated Flash Rom support
- External ISA-Bus drivers for design flexibility and optimum drive
- 100% PC/AT® compatible
- 160-pin PQFP for the F84031 and 100-pin PQFP for the F84035



System Diagram

Revision History

Revision	Date	By	Comment
0.1	3/2/93	PD	Internal review—Rough draft.
0.2	3/26/93	PD	Internal review—Added Product Overview and Introduction sections.
0.3	4/30/93	PD	Internal review.
1.0	5/10/93	PD	Final release.

Table of Contents

Table of Contents

List of Figures

List of Tables

Introduction

CS4031 is a very high-integration and low-cost chip set for 486-based PC/AT compatible systems. It consists of two chips, the F84031 and F84035. These are optimally partitioned to minimize the external TTL count.

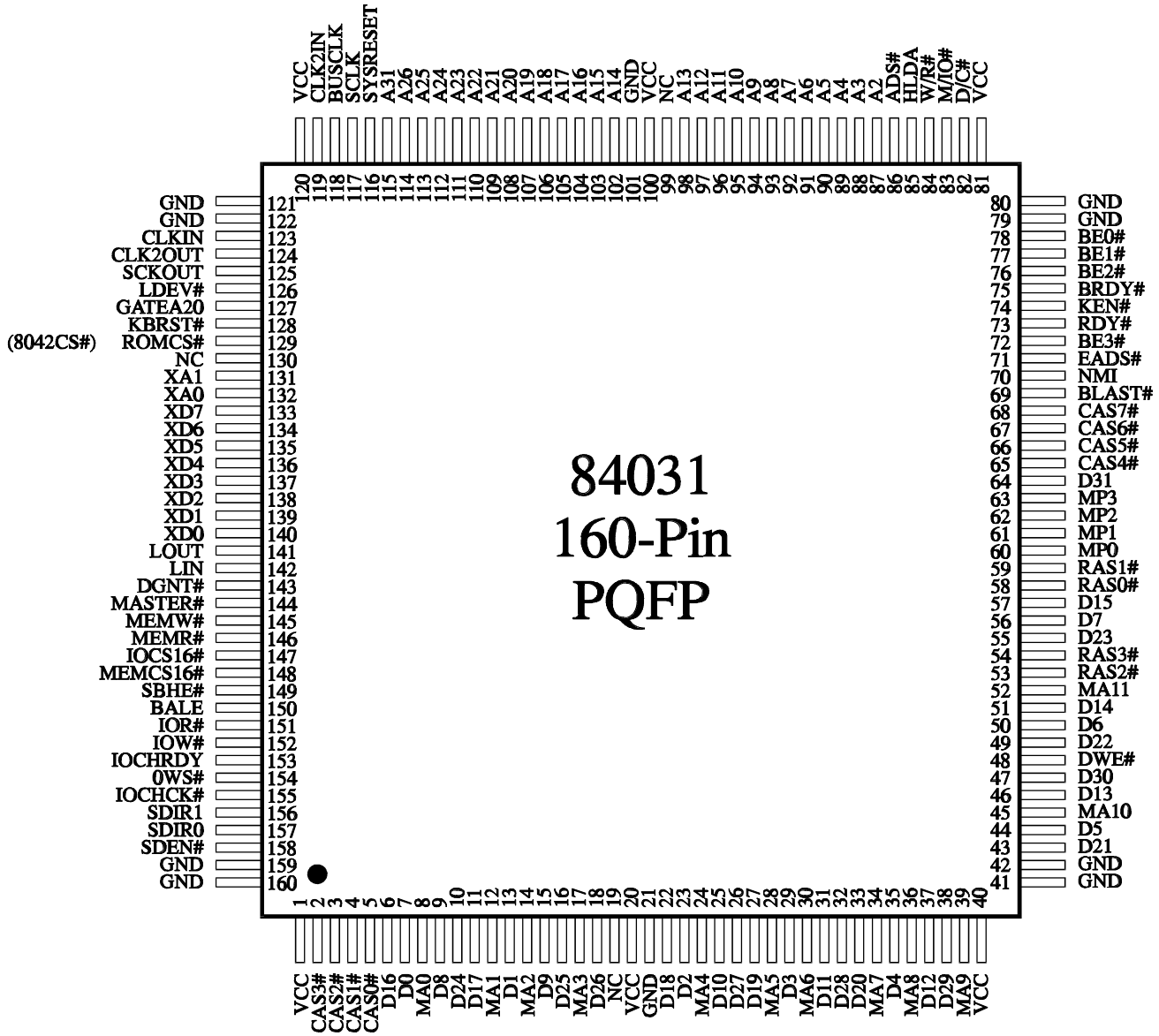
Only 8 TTL devices are required to implement a 100% PC/AT compatible complete system with a 2-bank DRAM (up to 32MB) and one VESA VL-Bus slot for either a master or a slave. Only one additional TTL is needed for the system supporting two VL-Bus slots with no more than one master.

The 84031 integrates DRAM controller, ISA-bus controller, and VESA VL-Bus controller in a 160-pin PQFP package.

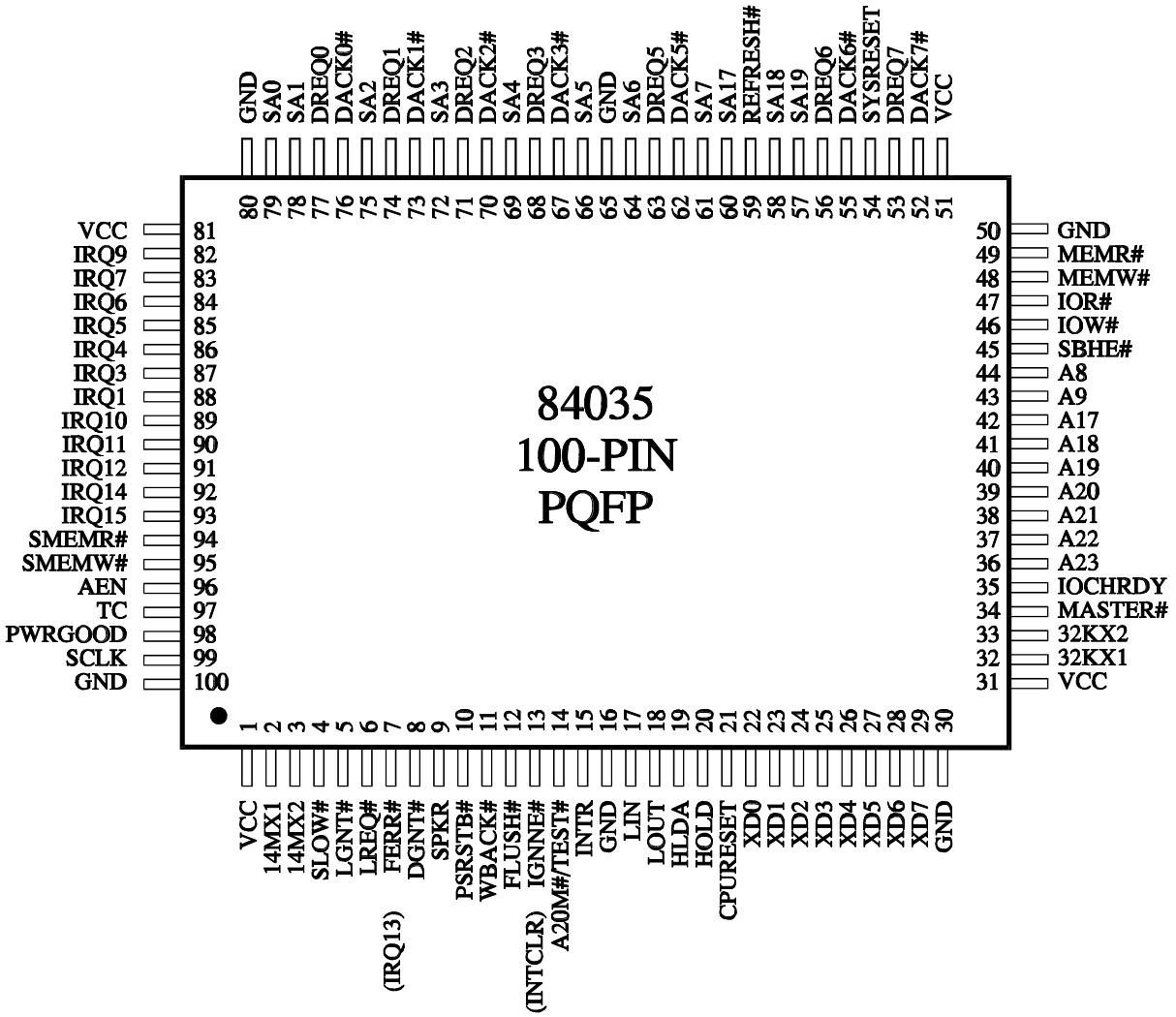
The 84035 is a super set of the industry-standard CHIPS IPC (Integrated Peripheral Controller, 82C206) which integrates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 timer/counter, one MC146818 real time clock, and a 74LS612 memory mapper in a 100-pin PQFP package.

CS4031 Pinouts

The CS4031 CHIPSet is comprised of two chips, the 84031 and the 84035. Following the 84031 and 84035 pinout diagrams are the pin assignments listed by signal names.



84031 Pinout



84035 Pinout

CS4031 Pin Descriptions

84031 PIN OVERVIEW

The 84031 Pin Overview table below lists the pins by signal names. The detailed pin functional descriptions for the 84031 follows the pin overview tables.

84031 PIN OVERVIEW

Signal Name	Pin No.	Input/ Output	I_{OL} (mA)	I_{OH} (mA)	Load (pF)	Pull-up (Ω)	Notes
V_{CC} (6 Pins)	1, 20, 40, 81, 100, and 120	—	—	—	—	—	System V_{CC}
GND (10 Pins)	21, 41, 42, 79, 80, 81, 101, 121, 122, 160, and 159	—	—	—	—	—	System ground
0WS#	1	In	—	—	—	300	ISA-bus
A02	87	In	—	—	—	—	CPU, local bus devices, and AT buffers
A03	88	In	—	—	—	—	CPU, local bus devices, and AT buffers
A04	89	In	—	—	—	—	CPU, local bus devices, and AT buffers
A05	90	In	—	—	—	—	CPU, local bus devices, and AT buffers
A06	91	In	—	—	—	—	CPU, local bus devices, and AT buffers
A07	92	In	—	—	—	—	CPU, local bus devices, and AT buffers
A08	93	In	—	—	—	—	CPU, local bus devices, and AT buffers
A09	94	In	—	—	—	—	CPU, local bus devices, and AT buffers
A10	95	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A11	96	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A12	97	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A13	98	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A14	102	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A15	103	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A16	104	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A17	105	In	—	—	—	—	CPU, local bus devices, and AT buffers
A18	106	In	—	—	—	—	CPU, local bus devices, and AT buffers
A19	107	In	—	—	—	—	CPU, local bus devices, and AT buffers
A20	108	In	—	—	—	—	CPU, local bus devices, and AT buffers
A21	109	In	—	—	—	—	CPU, local bus devices, and AT buffers
A22	110	In	—	—	—	—	CPU, local bus devices, and AT buffers
A23	111	In	—	—	—	—	CPU, local bus devices, and AT buffers
A24	112	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A25	113	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A26	114	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
A31	115	I/O	4	-2	50	—	CPU, local bus devices, and AT buffers
ADS#	86	I/O	4	-2	40	10K	CPU and local bus devices
BALE	150	Out	18	-10	240	—	ISA-bus
BE0#	78	I/O	4	-2	50	—	CPU and local bus devices
BE1#	77	I/O	4	-2	50	—	CPU and local bus devices
BE2#	76	I/O	4	-2	50	—	CPU and local bus devices
BE3#	72	I/O	4	-2	50	—	CPU and local bus devices
BLAST#	69	I/O	4	-2	40	—	CPU and local bus devices
BRDY#	75	I/O	4	-2	40	10K	CPU and local bus devices
BUSCLK	118	Out	18	-10	50	—	8042 inverter

84031 PIN OVERVIEW (continued)

Signal Name	Pin No.	Input/ Output	I_{OL} (mA)	I_{OH} (mA)	Load (pF)	Pull-up (Ω)	Notes
CAS0#	5	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CAS1#	4	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CAS2#	3	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CAS3#	2	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CAS4#	65	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CAS5#	66	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CAS6#	67	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CAS7#	68	Out	18	-10	65	—	6 DRAMs @ 7pF plus wiring
CLK2	119	In	—	—	—	—	CLK2OUT or oscillator circuit
CLK2OUT	124	Out	9	-5	30	—	84031 CLK2
CLKIN	123	In	—	—	—	—	Oscillator
D/C#	82	I/O	4	-2	40	—	CPU and local bus devices
D0	7	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D1	13	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D2	23	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D3	29	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D4	35	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D5	44	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D6	50	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D7	56	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D8	9	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D9	15	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D10	25	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D11	31	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D12	37	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D13	46	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D14	51	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D15	57	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D16	6	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D17	11	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D18	22	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D19	27	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D20	33	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D21	43	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D22	49	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D23	55	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D24	10	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D25	16	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D26	18	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D27	26	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D28	32	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D29	38	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D30	47	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
D31	64	I/O	4	-2	65	—	CPU, DRAMs, and local bus devices
DGNT#	143	In	—	—	—	—	IPC
DWE#	48	Out	18	-10	240	—	24 DRAMs @ 7pF plus wiring
EADS#	71	Out	9	-5	40	10K	CPU and local bus devices
GATEA20	127	In	—	—	—	4.7K	Keyboard controller
HLDA	85	In	—	—	—	—	CPU

84031 PIN OVERVIEW (continued)

Signal Name	Pin No.	Input/ Output	I_{OL} (mA)	I_{OH} (mA)	Load (pF)	Pull-up (Ω)	Notes
IOCHCK#	155	In	—	—	—	4.7K	ISA-bus
IOCHRDY	153	I/O	18	—	240	1K	ISA-bus
IOCS16#	147	In	—	—	—	300	ISA-bus
IOR#	151	I/O	18	-10	240	10K	ISA-bus
IOW#	152	I/O	18	-10	240	10K	ISA-bus
KBRST#	127	In	—	—	—	4.7K	Keyboard controller
KEN#	74	Out	4	-2	40	—	CPU
LDEV#	125	In	—	—	—	10K	From VL-Bus slots.
LIN	142	In	—	—	—	10K	IPC
LOUT	141	Out	4	-2	30	—	IPC
M/IO#	83	I/O	4	-2	200	—	CPU and local bus developers
MA0	8	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA1	12	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA2	14	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA3	17	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA4	24	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA5	28	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA6	30	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA7	34	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA8	36	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA9	39	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA10	45	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MA11	52	Out	18	-10	200	—	24 DRAMS @ 6pF plus wiring
MASTER#	144	In	—	—	—	300	ISA-bus
MEMCS16#	148	I/O	18	—	240	300	ISA-bus
MEMR#	146	I/O	18	-10	240	10K	ISA-bus
MEMW#	145	I/O	18	-10	240	10K	ISA-bus
MP0	60	I/O	4	-2	65	—	CPU and DRAMs
MP1	61	I/O	4	-2	65	—	CPU and DRAMs
MP2	62	I/O	4	-2	65	—	CPU and DRAMs
MP3	63	I/O	4	-2	65	—	CPU and DRAMs
NC	19	—	—	—	—	—	Reserved
NC	99	—	—	—	—	—	Reserved
NC	130	—	—	—	—	10K	Requires 10K pull-up
NMI	70	Out	4	-2	30	—	CPU
RAS0#	58	Out	18	-10	120	—	12 DRAMs @ 7pF plus wiring
RAS1#	59	Out	18	-10	120	—	12 DRAMs @ 7pF plus wiring
RAS2#	53	Out	18	-10	120	—	12 DRAMs @ 7pF plus wiring
RAS3#	54	Out	18	-10	120	—	12 DRAMs @ 7pF plus wiring
RDY#	73	I/O	4	-2	40	10k	CPU and local bus devices
ROMCS# (8042CS#)	129	Out	4	-2	50	—	ROM and 8042 chip select
SBHE#	149	I/O	18	-10	240	—	ISA-bus
SCLK	117	In	—	—	—	—	Oscillator circuit
SCLKOUT (VBUFDIR#)	125	Out	9	-5	85	—	84031, 84035, CPU, or VRAM buffers
SDEN#	158	Out	4	-2	30	—	F245 and inverter
SDIR0	157	Out	4	-2	40	—	F245
SDIR1	156	Out	4	-2	40	—	F245
SYSRESET	116	In	—	—	—	—	IPC

84031 PIN OVERVIEW (continued)

Signal Name	Pin No.	Input/ Output	I_{OL} (mA)	I_{OH} (mA)	Load (pF)	Pull-up (Ω)	Notes
W/R#	84	I/O	4	-2	40	—	CPU and local bus devices
XA0	132	I/O	4	-2	40	—	F245
XA1	131	—	—	—	—	—	—
XD0	140	I/O	4	-2	65	—	8042, ROM, LS245, or 84035
XD1	139	—	4	-2	—	—	—
XD2	138	—	4	-2	—	—	—
XD3	137	—	4	-2	—	—	—
XD4	136	—	4	-2	—	—	—
XD5	135	—	4	-2	—	—	—
XD6	134	—	4	-2	—	—	—
XD7	133	—	4	-2	—	—	—

84035 PIN OVERVIEW

The 84035 Pin Overview table below lists the pins by signal names. The detailed pin functional descriptions for the 84035 follows this overview table.

84035 PIN OVERVIEW

Signal Name	Pin No.	Input/ Output	Driver	I_{OL} (mA)	I_{OH} (mA)	Load (pF)	Pull-up (Ω)	Notes
V_{CC} (4 Pins)	1, 31, 51, and 81	—	—	—	—	—	—	Battery backup circuit
GND (6 Pins)	16, 30, 50, 65, 80, and 100	—	—	—	—	—	—	System ground
NC	1	—	—	—	—	—	—	Reserved, do not connect
14MX1	2	In	—	—	—	—	—	14.31818MHz crystal input
14MX2	3	Out	TP	2	-1	50	—	14.31818MHz crystal output
32KX1	32	In	—	—	—	—	—	Crystal circuit
32KX2	33	Out	TP	1	-1	—	—	Crystal circuit
A8	44	I/O	TS	4	-1	65	—	CPU and 84031
A9	43	I/O	TS	4	-1	65	—	CPU and 84031
A17	42	I/O	TS	4	-1	65	—	CPU and 84031. Driven for DMA; inputs to generate SA.
A18	41	I/O	TS	4	-1	65	—	CPU and 84031. Driven for DMA; inputs to generate SA.
A19	40	I/O	TS	4	-1	65	—	CPU and 84031. Driven for DMA; inputs to generate SA.
A20	39	Out	TS	4	-1	65	—	CPU and 84031. Driven for DMA.
A21	38	Out	TS	4	-1	65	—	CPU and 84031. Driven for DMA.
A22	37	Out	TS	4	-1	65	—	CPU and 84031. Driven for DMA.
A23	36	Out	TS	4	-1	65	—	CPU and 84031. Driven for DMA.
A20M#/TEST#	14	I/O	TS	4	-1	30	10K	CPU
AEN	96	Out	TP	24	-3	240	—	ISA-bus
CPURESET	21	Out	TP	4	-1	50	—	CPU(s)
DACK0#	76	Out	TP	4	-1	240	—	ISA-bus
DACK1#	73	Out	TP	4	-1	240	—	ISA-bus
DACK2#	70	Out	TP	4	-1	240	—	ISA-bus
DACK3#	67	Out	TP	4	-1	240	—	ISA-bus
DACK5#	62	Out	TP	4	-1	240	—	ISA-bus
DACK6#	55	Out	TP	4	-1	240	—	ISA-bus
DACK7#	52	Out	TP	4	-1	240	—	ISA-bus
DGNT#	8	Out	TP	4	-1	40	—	84031; one buffer direction
DREQ0	77	In	—	—	—	—	10K	ISA-bus
DREQ1	74	In	—	—	—	—	10K	ISA-bus
DREQ2	71	In	—	—	—	—	10K	ISA-bus
DREQ3	68	In	—	—	—	—	10K	ISA-bus
DREQ5	63	In	—	—	—	—	10K	ISA-bus
DREQ6	56	In	—	—	—	—	10K	ISA-bus
DREQ7	53	In	—	—	—	—	10K	ISA-bus
FERR# (IRQ13)	7, 83	In	—	—	—	—	—	CPU or coprocessor logic
FLUSH#	12	Out	TS	4	-1	30	—	CPU
HLDA	19	In	—	—	—	—	—	CPU
HOLD	20	Out	TP	4	-1	30	—	CPU(s)
IGNNE#/INTCLR	13	Out	TP	4	-1	30	—	CPU or coprocessor logic
INTR	15	Out	TP	4	-1	30	—	CPU
IOCHRDY	35	In	—	—	—	—	1K	ISA-bus and 84031
IOR#	47	I/O	TS	24	-3	240	10K	ISA-bus and 84031. Driven for DMA cycles only.

84035 PIN OVERVIEW (continued)

Signal Name	Pin No.	Input/ Output	Driver	I_{OL} (mA)	I_{OH} (mA)	Load (pF)	Pull-up (Ω)	Notes
IOW#	46	I/O	TS	24	-3	240	10K	ISA-bus and 84031. Driven for DMA cycles only.
IRQ01	88	In	—	—	—	—	—	ISA-bus
IRQ03	87	In	—	—	—	—	—	ISA-bus
IRQ04	86	In	—	—	—	—	—	ISA-bus
IRQ05	85	In	—	—	—	—	—	ISA-bus
IRQ06	84	In	—	—	—	—	—	ISA-bus
IRQ07	83	In	—	—	—	—	—	ISA-bus
IRQ09	82	In	—	—	—	—	—	ISA-bus
IRQ10	89	In	—	—	—	—	—	ISA-bus
IRQ11	90	In	—	—	—	—	—	ISA-bus
IRQ12	91	In	—	—	—	—	—	ISA-bus
IRQ14	92	In	—	—	—	—	—	ISA-bus
IRQ15	93	In	—	—	—	—	—	ISA-bus
LGNT#	5	Out	TP	4	-1	50	—	Local bus
LIN	17	In	—	—	—	—	—	84031
LOUT	18	Out	TP	4	-1	30	—	84031
LREQ#	6	In	—	—	—	—	10K	Local bus (pull-up if not used).
MASTER#	34	In	—	—	—	—	300	ISA-bus
MEMR#	49	Out	TS	24	-3	240	10K	ISA-bus and 84031. Driven for DMA cycles only.
MEMW#	48	Out	TS	24	-3	240	10K	ISA-bus and 84031. Driven for DMA cycles only.
PSRSTB#	10	In	—	—	—	—	RC	RC circuit
PWRGOOD	98	In	—	—	—	—	—	Power supply of PUC circuit
REFRESH#	59	I/O	OC	24	—	240	300	ISA-bus
SA0	79	I/O	TS	24	-3	240	—	ISA-bus and F245
SA1	78	I/O	TS	24	-3	240	—	ISA-bus and F245
SA2	75	I/O	TS	24	-3	240	—	ISA-bus and F245
SA3	72	I/O	TS	24	-3	240	—	ISA-bus and F245
SA4	69	I/O	TS	24	-3	240	—	ISA-bus and F245
SA5	66	I/O	TS	24	-3	240	—	ISA-bus and F245
SA6	64	I/O	TS	24	-3	240	—	ISA-bus and F245
SA7	61	I/O	TS	24	-3	240	—	ISA-bus and F245
SA17	60	Out	TS	24	-3	240	—	ISA-bus (driven from A19:17)
SA18	58	Out	TS	24	-3	240	—	ISA-bus (driven from A19:17)
SA19	57	Out	TS	24	-3	240	—	ISA-bus (driven from A19:17)
SBHE#	45	Out	TS	24	-3	240	—	ISA-bus and 84031
SCLK	99	In	—	—	—	—	—	Oscillator circuit
SLOW	4	In	—	—	—	—	10K	Turbo switch
SMEMR#	94	Out	TP	24	-3	240	—	ISA-bus and 84031
SMEMR#	95	Out	TP	24	-3	240	—	ISA-bus and 84031
SPKR	9	Out	TP	4	-1	30	—	Speaker buffer
SYSRESET	54	Out	TP	8	-2	50	—	Coprocessor, 4025, and buffer to ISA-bus.
TC	97	Out	TP	4	-1	240	—	ISA-bus
XD0	22	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM
XD1	23	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM
XD2	24	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM
XD3	25	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM
XD4	26	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM
XD5	27	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM
XD6	28	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM
XD7	29	I/O	TS	4	-1	65	—	84031, LS244, 8042, and ROM

84031 PIN DESCRIPTIONS

The pin functional descriptions for the 84031 are listed below. For a pin overview by signal names, see the 84031 Pin Overview table or the pinout diagram.

CLOCKS AND RESET

Signal Name	Pin No.	Input/ Output	Description
CLKIN	123	In	Clock Input (2x clock from oscillator). Used only to create CLK2OUT and SCLKOUT.
CLK2OUT	124	Out	Clock 2x Output. CLK2OUT is a buffered version of CLK2, with very low skew to SCLKOUT. It is fed back to CLK2 on the 84031 and any other logic requiring a 2x clock.
SCLKOUT	125	Out	1x clock output. This is CLKIN divided by 2, and is used to drive SCLK on the 84031, 84035, as well as the CPU.
CLK2	119	In	2x clock input. Used for the DRAM state machine. It is also used as a source for the ISA-bus clock divider.
SCLK	117	In	1x clock input.
SYSRESET	116	In	System Reset from the 84035.
BUSCLK	118	Out	ISA-Bus Clock.

ARBITRATION

Signal Name	Pin No.	Input/ Output	Description
HLDA	85	In	CPU Hold Acknowledge. When low, indicates that the CPU has control of the local bus. When high, either the local master, the DMA controller, or the ISA master has the bus. The 84031 generates parity for DRAM write cycles when this pin is high.
DGNT#	143	In	DMA controller Grant. When low, indicates that either the DMA controller or an ISA-bus master has control of the bus. The 84031 becomes the ISA slave and floats the ISA-bus commands when this signal is low.
MASTER#	144	In	ISA-bus Master signal. Indicates that the ISA master has the bus. The 84031 uses this to determine the difference between DMA and ISA master cycles. It is also used in determining the timing for IOCHRDY generation.

CPU AND LOCAL BUS CONTROL SIGNALS

Signal Name	Pin No.	Input/ Output	Description
ADS#	86	I/O	Address Strobe. Input for CPU and local master cycles. Output for DMA and ISA master cycles.
W/R#	84	I/O	Write/Read status signal. Input for CPU and local master cycles. Output for DMA and ISA master cycles.
D/C#	82	I/O	Data/Code status signal. Input for CPU and local master cycles. Output for DMA and ISA master cycles.
M/IO#	83	I/O	Memory/IO status signal. Input for CPU and local master cycles. Output for DMA and ISA master cycles.
RDY#	73	I/O	Non-burst ready. Output when a slave. Input from a local bus slave or external cache controller.
BRDY#	75	I/O	Burst Ready. Output when a slave. Input from a local bus slave or external cache controller.
KEN#	74	Out	Cache Enable to the CPU. Always driven. Optionally inactive for shadow RAM.
BLAST#	69	I/O	Burst Last. Driven (low) for DMA and ISA master cycles.
EADS#	71	Out	External Address Strobe. Used to invalidate the 486 cache on DMA and ISA master cycles. Optionally floated when a local master takes the cycle (the local master drives it on the VL-bus).

ISA-BUS

Signal Name	Pin No.	Input/ Output	Description
BALE	150	Out	Buffered Address Latch Enable. Direct drive of the ISA-bus.
MEMR#	146	I/O	Memory Read Strobe. Direct drive of the ISA-bus. Output when HLDA or LGNT# are low. Input when these are both high.
MEMW#	145	I/O	Memory Write Strobe. Direct drive of the ISA-bus. Output when HLDA or LGNT# are low. Input when these are both high.
IOR#	151	I/O	I/O Read strobe. Direct drive of the ISA-bus. Output when HLDA or LGNT# are low. Input when these are both high.
IOW#	152	I/O	I/O Write strobe. Direct drive of the ISA-bus. Output when HLDA or LGNT# are low. Input when these are both high.
IOCHRDY	153	I/O	ISA-bus ready (I/O Channel Ready). Output when an ISA slave (DMA and ISA master accesses to local DRAM or local bus slaves). Input for CPU or local master accesses to the ISA-bus (open collector).
0WS#	154	In	ISA-bus zero wait state signal. The ISA-bus slave will drive this signal low when a memory command falls to force a 0 wait state cycle. It may also be used to force an 8-bit memory or I/O signal into 2 wait state cycles.
MEMCS16#	148	I/O	16-bit ISA memory indicator. Output for DMA and ISA master accesses to local DRAM or local bus slaves. Input for CPU or local master accesses to the ISA-bus (open collector).
IOCS16#	147	In	Input for CPU or local master accesses to the ISA-bus.

ADDRESS BUS

Signal Name	Pin No.	Input/ Output	Description
BE0# BE1# BE2# BE3#	78 77 76 72	I/O	Byte enables (BE3:0#). Input for CPU or local master accesses to the ISA-bus. Output for DMA or ISA master cycles. Generated from XA1:0 and SBHE#.
SBHE#	149	I/O	ISA-bus BHE#. Output for CPU or local master accesses to the ISA-bus. Input for DMA or ISA master cycles.
XA0 XA1	132 131	I/O	Output for CPU or local master accesses to the ISA-bus. Input for DMA or ISA master cycles.
A2 A3 A4 A5 A6 A7 A8 A9	87 88 89 90 91 92 93 94	In	Local bus address (A9:2). Always inputs.
A10 A11 A12 A13 A14 A15 A16	95 96 97 98 102 103 104	I/O	Local bus address (A16:10). Output for DMA cycles. A16:10 of the DMA address is sent on XD6:0 from the 84035 and latched in the 84031.
A17 A18 A19 A20 A21 A22 A23	105 106 107 108 109 110 111	In	Local bus address (A23:17). Always inputs.
A24 A25 A26 A31	112 113 114 115	I/O	Local bus address (A26:24, A31). Driven low for DMA and ISA master cycles.
ROMCS# (8042CS#)	129	Out	Logical OR of the ROM chip select and 8042 chip select. The 8042 chip select is active for I/O ports 60 and 64. The ROM chip select is programmable.
LDEV#	126	In	Local Device. A local bus slave or cache controller drives this signal low to indicate that it will handle the cycle. This signal is sampled either at the end of the first or second T2.

DRAM CONTROLLER

Signal Name	Pin No.	Input/ Output	Description
RAS0#	58	Out	RAS for each of 4 DRAM banks (RAS3:0#). Direct Drive.
RAS1#	59		
RAS2#	53		
RAS3#	54		
CAS0#	5	Out	CAS7:0#. CAS3:0# are for banks 0 and 2. CAS7:4# are for banks 1 and 3. Direct drive.
CAS1#	4		
CAS2#	3		
CAS3#	2		
CAS4#	65		
CAS5#	66		
CAS6#	67		
CAS7#	68		
DWE#	48	Out	DRAM Write Enable. Direct drive for 2 banks.
MA0	8	Out	DRAM address (MA11:0). Direct drive for 2 banks.
MA1	12		
MA2	14		
MA3	17		
MA4	24		
MA5	28		
MA6	30		
MA7	34		
MA8	36		
MA9	39		
MA10	45		
MA11	52		

DATA BUS

Signal Name	Pin No.	Input/ Output	Description
D0	7	I/O	Local bus data (D31:0).
D1	13		
D2	23		
D3	29		
D4	35		
D5	44		
D6	50		
D7	56		
D8	9		
D9	15		
D10	25		
D11	31		
D12	37		
D13	46		
D14	51		
D15	57		
D16	6		
D17	11		
D18	22		
D19	27		
D20	33		
D21	43		
D22	49		
D23	55		
D24	10		
D25	16		
D26	18		
D27	26		
D28	32		
D29	38		
D30	47		
D31	64		
MP0	60	I/O	DRAM parity bits (MP3:0). Connected to DP0:3 of the 486. The 486 generates parity when it has the bus. For local masters, DMA cycles, and ISA masters, the 84031 generates parity. Parity is checked by the 84031 for all cycles.
MP1	61		
MP2	62		
MP3	63		
XD0	140	I/O	Intermediate data bus (XD7:0). Connected directly to the 84035, BIOS ROM, 8042, and, through an LS245, to the ISA-bus.
XD1	139		
XD2	138		
XD3	137		
XD4	136		
XD5	135		
XD6	134		
XD7	133		
SDIR0	157	Out	Direction control for the XD7:0 to SD7:0 (SDIR0) and the D15:8 to SD15:8 (SDIR1) buffer. 0 = SD to XD (or D). 1 = XD (or D) to SD.
SDIR1	156		
SDEN#	158	Out	SD bus Enable. Connects to the enable of the D15:8 to SD15:8 buffer and, through an inverter, to the enables of the D31:24 to SD15:8 buffer that is normally low. Goes high for CPU or local master high word writes to the ISA-bus. Then DMA and ISA master reads from the high word of the local DRAM or the local bus slaves.

INTERRUPTS

Signal Name	Pin No.	Input/ Output	Description
IOCHCK#	155	In	I/O Channel Check (parity error indicator from the ISA-bus). Generates an NMI and sets the IOCHCK flag.
NMI	70	Out	Nonmaskable Interrupt request to the CPU. Generated for parity errors and when IOCHCK# has gone low. Each of these has enable bits plus a final mask.

CONTROL LINK AND KEYBOARD

Signal Name	Pin No.	Input/ Output	Description
LIN/TEST	142	In	Control Link Input from the 84035. Transfers the following information: Refresh Request, Refresh Complete, and DMA Address Strobe.
		In	Test Mode input.
LOUT	141	Out	Control Link Output to the 84035. Transfers the following information: Interrupt Acknowledge cycle, CPU Reset Request, Refresh Request Acknowledge, and GATEA20 from the keyboard controller
GATEA20	128	In	GATEA20 signal from the 8042. The 84031 detects transitions on this pin and transmits them to the 84035 over the control link.
KBRST#	127	In	Keyboard Reset from the 8042. When this signal goes low, the 84031 sends a code across the control link to inform the 84035 of this. The 84035 will perform the CPU restart.

84035 PIN DESCRIPTIONS

The pin functional descriptions for the 84035 are listed below. For a pin overview by signal names, see the 84035 Pin Overview table or the pinout diagram.

CLOCKS

Signal Name	Pin No.	Input/ Output	Description
14MX1	2	In	14.31818MHz crystal input.
14MX2	3	Out	14.31818MHz crystal output
SCLK	99	In	1x CPU clock input. Used for arbitration logic, reset generation, and selectively divided down to make the DMA clock.

RESETS

Signal Name	Pin No.	Input/ Output	Description
PWRGOOD	98	In	Power Good. From the power supply or power-on clear circuit.
CPURESET	21	Out	Reset to the CPU only. Synchronized to SCLK.
SYSRESET	54	Out	System Reset. Reset to the rest of the system. Has the same timing as CPURESET, but is only active following PWRGOOD being low.

ARBITRATION

Signal Name	Pin No.	Input/ Output	Description
HOLD	20	Out	Bus Hold Request (HOLD) to the CPU. Synchronous to SCLK.
HLDA	19	In	Bus Hold Acknowledge (HLDA) from the CPU. The 84035 assumes it is synchronous to SCLK.
LREQ#	6	In	Local bus Request from the local masters. If more than one LREQ# is present, external arbitration logic (from a PAL) creates additional LGNT# signals.
LGNT#	5	Out	Local bus Grant to local bus masters. This signal goes low to give control to a local bus master.
DGNT#	8	Out	DMA controller Grant hold acknowledge. Indicates that the DMA controller or ISA master has control of the bus. Used for buffer steering and goes to the 84031.
MASTER#	34	In	ISA master pulls this signal low after gaining control of the bus through a DMA channel's DREQ/DACK# signals. When this signal goes low the AEN output is taken low.
REFRESH#	59	I/O	ISA-bus Refresh signal. The 84035 drives this signal low during refresh cycles. During refresh cycles while an ISA master has control of the bus, the master drives it low.
AEN	96	Out	DMA Address Enable. High for DMA and refresh cycles, low at all other times, including when the CPU, local masters, or ISA masters have control of the bus. The main function of this signal is to disable all IO decodes in the system.
TC	97	Out	DMA Terminal Count. This signal goes high during the final cycle of a DMA transfer. It is used mainly by the floppy disk controller, but may also be used by other DMA devices.

ARBITRATION (continued)

Signal Name	Pin No.	Input/ Output	Description
DREQ0 DREQ1 DREQ2 DREQ3 DREQ5 DREQ6 DREQ7	77 74 71 68 63 56 53	In	DMA Requests. DREQ3:0 are 8-bit channels. DREQ7:5 are 16-bit channels. Any of these channels may be used for ISA masters, except DREQ7:5 are preferred because there is less arbitration overhead.
DACK0# DACK1# DACK2# DACK3# DACK5# DACK6# DACK7#	76 73 70 67 62 55 52	Out	DMA Acknowledge.
SLOW#	4	In	Turbo switch input. Polarity is programmable. Normally, low is slow, high is fast. The signal can be programmed to emulate the speed of an 8MHz AT-compatible CPU. (Note: Some software applications require certain speeds in order to execute.) The Performance Control registers must be programmed before this signal has any effect.
FLUSH#	12	Out	This signal should be connected to the CPU FLUSH# pin. It is used in conjunction with the performance control register. The CPU cache is optionally flushed each time the CPU is put into HOLD; the register can better control the speed of execution.

ISA-BUS

Signal Name	Pin No.	Input/ Output	Description
MEMR#	49	I/O	Memory Read strobe. Connected directly to the ISA-bus. Output during DMA cycles. Input at all other times to generate SMEMR#.
MEMW#	48	I/O	Memory Write strobe. Connected directly to the ISA-bus. Output during DMA cycles. Input at all other times to generate SMEMR#.
SMEMR#	94	Out	Memory Read strobe for the bottom 1MB. Connected directly to the ISA-bus. Output at all times. This signal is a function of A23:20 and MEMR#, and is low when all of those signals are low.
SMEMW#	95	Out	Memory Write strobe for the bottom 1MB. Connected directly to the ISA-bus. Output at all times. This signal is a function of A23-20 and MEMW#, and is low when all of those signals are low.
IOR#	47	I/O	I/O Read strobe. Connected directly to the ISA-bus. Output during DMA cycles. Input at all other times, to access internal I/O.
IOW#	46	I/O	I/O Write strobe. Connected directly to the ISA-bus. Output during DMA cycles. Input at all other times, to access internal I/O.
IOCHRDY	35	I/O	ISA-bus ready. Input during DMA cycles to add wait states to the command strobes. Output during accesses to the DMA controller registers to optionally add a wait state.

ADDRESS BUS

Signal Name	Pin No.	Input/ Output	Description
SBHE#	45	Out	ISA-bus byte high enable. Driven only during DMA cycles. For 8-bit DMA (channels 3:0) it is driven with the inverse of A0. For 16-bit DMA (channels 7:5) it is driven low.
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7	79 78 75 72 69 66 64 61	I/O	ISA-bus address bits 7:0. Direct drive of the ISA-bus. Outputs during DMA cycles and refresh cycles. Inputs at all other times.
A8 A9	44 43	I/O	Local bus address bits 9:8. Connected to the CPU local bus. Outputs during DMA cycles. Inputs at all other times.
SA17 SA18 SA19	60 58 57	Out	ISA-bus address bits 19:17. Direct drive of the ISA-bus. Outputs at all times except ISA master cycles, where these are floated. These are driven from A19:17.
A17 A18 A19	42 41 40	I/O	Local bus address bits 19:17. Connected to the CPU local bus. Outputs during DMA cycles. Inputs (to drive SA19:17) at all other times.
A20 A21 A22 A23	39 38 37 36	Out	Local bus address bits 23:20. Connected to the CPU local bus. Outputs during DMA cycles, floated at all other times.
A20M#/TEST#	14	Out	Address bit 20 Mask/Test. Connected to the CPU A20M# pin. This is the logical OR of the emulated keyboard GATEA20 and fast GATEA20 (port 92 bit 1). This pin becomes the TEST# input after reset . If pulled low, the 84035 will go into test mode. It becomes the A20M output after a configuration bit has been set. At that time the 84035 begins driving the pin and ignoring it as an input. A 10K pull-up should be connected to this pin to prevent the test mode from being entered and to keep A20M# high at power up.

DATA BUS

Signal Name	Pin No.	Input/ Output	Description
XD0 XD1 XD2 XD3 XD4 XD5 XD6 XD7	22 23 24 25 26 27 28 29	I/O	Data bus. Outputs for I/O reads of internal registers. Also outputs to pass A16:10 to the 84031 at the start of DMA cycles. Inputs for I/O writes of internal registers.

INTERRUPTS

Signal Name	Pin No.	Input/ Output	Description
IRQ01 IRQ03 IRQ04 IRQ05 IRQ06 IRQ07 IRQ09 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	88 87 86 85 84 83 82 89 90 91 92 93	In	Interrupt inputs to the 8259s.
FERR# (IRQ13)	7	In	Floating-point Error/Interrupt Request 13. Dual function pin. Normally it is FERR# from the CPU and goes to the internal coprocessor error logic. It may optionally be IRQ13 if the coprocessor error logic is external.
IGNNE# (INTCLR)	13	Out	Ignore Numeric Error/Interrupt Clear. Dual function pin. Normally it is IGNNE# to the CPU and comes from the internal coprocessor error logic. It may optionally be INTCLR (active high write strobe for I/O ports F0 and F1) if the coprocessor error logic is external .
INTR		Out	Interrupt request to the CPU.

INTERVAL TIMER AND DATE-TIME CLOCK

Signal Name	Pin No.	Input/ Output	Description
SPKR	9	Out	Speaker output. Driven continuously high when speaker is not in use. See port 61h for description.
32KX1	32	In	Real time clock 32KHz crystal input.
32KX2	33	Out	Real time clock 32KHz crystal Output.
PSRSTB#	10	In	Real Time Clock Power Strobe. This signal, when low, indicates that the real time clock has lost power. For battery backup power, the 84035 Vcc pins should be connected to a 100K ohm pull-up resistor and a 0.1µF capacitor.

CONTROL LINK

Signal Name	Pin No.	Input/ Output	Description
LIN	17	In	Control Link Input from the 84031. Transfers the following information: Interrupt Acknowledge cycle, CPU Reset Request, Refresh Request Acknowledge cycle, and GATEA20 from keyboard controller.
LOUT	18	Out	Control Link Output to the 84031. Transfers the following information: Refresh Request, Refresh Complete, and DMA Address Strobe.

CS4031 Registers

84031 AND 84035 I/O PORT SUMMARY

Port Address	84031	84035	Description
00-0F		✔	DMA controller no. 1 (8-bit DMA)
20-21		✔	Interrupt controller no. 1 (IRQ7:0)
22-23	✔	✔	Configuration register address and data port
40-43		✔	Timer (8254)
60	✔		Keyboard data port
61	✔	✔	Port B
64	✔		Keyboard command/status port
70	✔	✔	Real time clock address port and NMI mask, (84031 bit 7 is write only)
71		✔	Real time clock data port
80-8F		✔	DMA page registers
92		✔	Fast CPU reset and GATEA20
A0-A1		✔	Interrupt controller no. 2 (IRQ15:8)
C0-DF		✔	DMA controller no. 2 (16-bit DMA)

84031 AND 84035 CONFIGURATION REGISTER SUMMARY

Index Register	84031	84035	Description
01		✔	IPC DMA controller wait states, clock.
05	✔		ISA-bus command delays
06	✔		ISA-bus wait states, address hold
07	✔		ISA-bus clock selection
08		✔	Performance control
09		✔	Miscellaneous control
0A		✔	DMA clock selection
0B-0F	—	—	Reserved
10	✔		DRAM timing
11	✔		DRAM setup
12	✔		DRAM configuration, blocks 0 and 1
13	✔		DRAM configuration, blocks 2 and 3
14	✔		DRAM block 0 starting address
15	✔		DRAM block 1 starting address
16	✔		DRAM block 2 starting address
17	✔		DRAM block 3 starting address
18	✔		Video shadow and local bus control
19	✔		DRAM shadow read enable
1A	✔		DRAM shadow write enable
1B	✔		ROMCS enable
1C	✔		Soft reset and GATEA20
1D-1F	—	—	Reserved
20-2F	—	—	Reserved

84031 I/O PORT ADDRESSES

Listed below are the 84031 I/O port addresses that are described in this section. (Figures are provided for the registers, where applicable.)

- Configuration register address and data port
- Keyboard data port
- Port B
- Keyboard command status port
- Real time clock address port and NMI mask.

All registers specific to the 84031 are summarized in the 84031 and 84035 I/O Port Summary and the 84031 and 84035 Configuration Register Summary tables.

CONFIGURATION REGISTER ADDRESS PORT
Port Address 22

Write only port which holds the address of Chips and Technologies, Inc. index register that is accessed through I/O port 23. This register must be written before each access to port 23; even if the same index register is being accessed twice in a row.

CONFIGURATION REGISTER DATA
Port Address 23

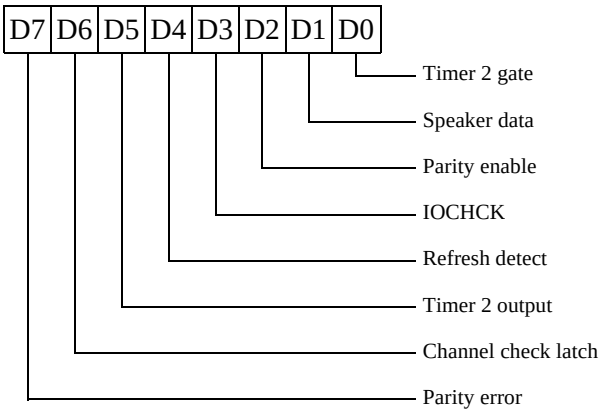
Port address 23 accesses the configuration register that points to port 22. A second access to port 23 without writing in between to port 22 will be ignored.

"Reserved" bits are unpredictable on read and may vary from one read to the next. For compatibility with future revisions and to avoid unexpected anomalies, reserved bits should be set to 0 on write (or left in their default state or written with the value as read) unless otherwise stated.

KEYBOARD DATA PORT
Port Address 60

Used for keyboard GATEA20 and Fast Reset function.

PORT B
Port Address 61
Default = 0F



This is an AT-compatible port with miscellaneous information. Bits 3:0 are read/write. Bits 7:4 are read only. Only bits 2, 3, 6, and 7 are available on the 84031. The remainder is available on the 84035. For I/O reads, half of the bits comes from each chip.

7 Parity check latch.

Read only. 1 indicates that a local parity error has occurred. Bit 7 is the Q# output result from the bit 3 above.

6 Channel check latch.

Read only. A logic 1 indicates that IOCHCK# has been activated. Bit 6 is the Q output result from the bit 4 above.

5 Timer 2 output.

Read only. (Bit 5 is also available on the 84035.) Bit 5 allows software to monitor the output of timer 2. Timer 2, ANDed together with bit 1 and inverted, produces the speaker signal. If bit 1 is 1, the SPKR output signal will be low when this bit is 1.

4 Refresh detect.

Read only. (Bit 4 in the 84035.) Bit 4 toggles on each refresh. It should toggle whenever timer 1 produces a pulse (at about every 15µs). The software may use this as a time delay.

3 Enable IOCHCK.

0 enables local the IOCHCK interrupt. 1 disables IOCHCK and clears the IOCHCK flip-flop. Bit 3 is inverted and sent to the active low clear of a flip-flop. IOCHCK is sent to the active low preset input. The Q# output is fed to the NMI logic. The Q output is sent to bit 6. The flip-flop is an index register, where the preset input of the flip-flop (ALS74 on AT-compatibles) has precedence over Q. The clear input has precedence over Q#.

2 Enable parity check.

Bit 2 has R/W function. 0 enables local DRAM parity checking. 1 disables local DRAM parity checking and clears the local parity error flip-flop. Bit 2 is inverted and sent to the active low preset input on the flip-flop . The Q output is PCK and is fed to the NMI logic. A parity error clocks the flip-flop to 0. An index register bit is used to block local DRAM parity errors, plus prevents the flip-flop from being clocked. The preset input from the flip-flop (F74 on AT-compatibles) has precedence over Q. The clear input has precedence over Q#.

1 Speaker data.

Bit 1 has R/W function. Bit 1 is available in the 84035. This bit is ANDed with the output of timer 2 (and inverted) to produce the actual signal sent to the speaker. When the gate is low (see bit 0) this bit gives direct software control of the speaker. If this bit is 0, the SPKR output signal is unconditionally driven high.

0 Timer 2 gate.

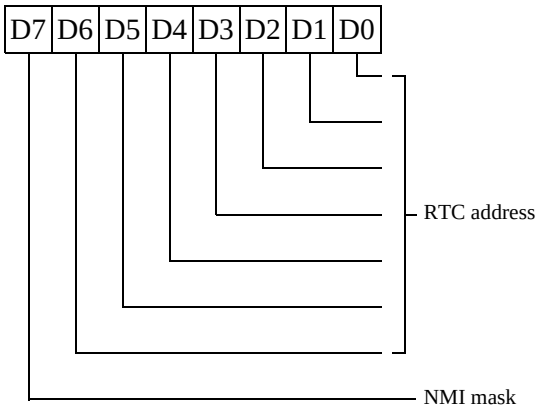
Timer 2 is the speaker with R/W function. (Bit 0 is contained in the 84035.) When this bit is 1, the timer is enabled and if programmed to do so, it will produce a square wave of the programmed frequency. When this bit is 0, the internal timer output bit (as read via port 61h bit 5) will be forced to 1. For SPKR output signal, see bit 1. The following table summarizes the effects of bits 0 and 1 when Timer 2 has been programmed for square wave generation.

Bit			
1	0	Bit 5	SPKR
0	0	1	H
0	1	TOG	H
1	0	1	L
1	1	TOG	TOG#

KEYBOARD COMMAND/STATUS PORT
Port Address 64

Used for keyboard GATEA20 and Fast Reset function.

REAL TIME CLOCK ADDRESS PORT AND NMI MASK
Port Address 70



7 NMI Mask—Nonmaskable interrupt mask.

Write only. Bit 7 is inverted and ANDed with the NMI sources (the OR from several sources). The result of the AND function is NMI to the CPU.

6:0 RTC—Real Time Clock address.

Also available on the 84035.

84031 CONFIGURATION REGISTERS

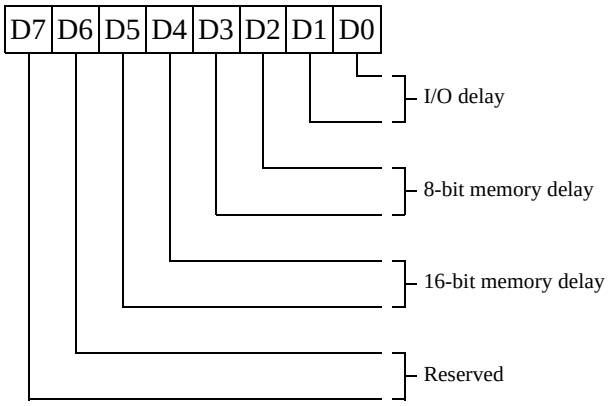
Listed below are the 84031 configuration registers that are described in this section. (Figures are provide for the registers, where applicable.)

- ISA-bus command delays
- ISA-bus wait state and address hold
- ISA-bus clock selection
- DRAM timing
- DRAM setup
- DRAM configuration, blocks 0 and 1
- DRAM configuration, blocks 2 and 3
- DRAM block 0 starting address
- DRAM block 1 starting address
- DRAM block 2 starting address
- DRAM block 3 starting address
- Video shadow and local bus control
- DRAM shadow read enable
- DRAM shadow write enable
- ROMCS enable
- Soft reset and GATEA20.

All registers specific to the 84031 are summarized in the 84031 and 84035 I/O Port Summary and the 84031 and 84035 Configuration Register Summary tables.

ISA-BUS COMMAND DELAYS

Index Register 05
Default = 05



The normal ISA timing is default = 05.

The two bits selected for each cycle types are:

00: 0 BUSCLK delay (command active at falling edge of ALE—default for 16-bit memory).

01: 0.5 BUSCLK delay (default for all cycles except 16-bit memory).

10: 1.0 BUSCLK delay.

11: 1.5 BUSCLK delay.

7:6 Reserved, write as 0s.

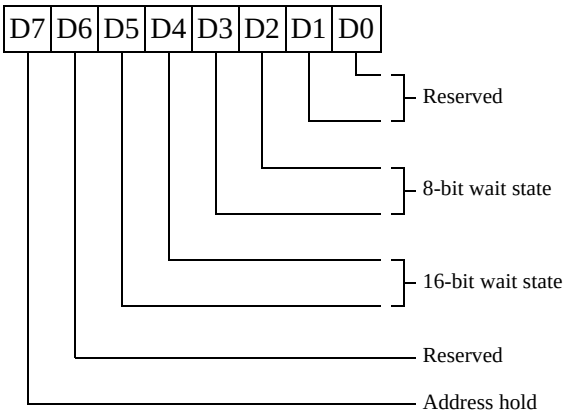
5:4 16-bit memory command delay. Default is 0.

3:2 8-bit memory command delay. Default is 1.

1:0 I/O cycle command delay. Default is 1.

ISA-BUS WAIT STATES AND ADDRESS HOLD

Index Register 06
Default = 00



For normal ISA timing, set this register to 24h. (Note: ISA wait states are defined as BUSCLK cycles in excess of two. Thus, 4 ISA wait states represents 6 BUSCLKs total including the ALE cycle.)

7 AT bus address hold time.

Ready delayed by an extra clock after the AT command goes inactive.

0: No additional hold time (default).
1: Additional hold time.

6 Reserved.

5:4 16-bit AT bus wait states.

00: 3 BUSCLK wait states (default).
01: 2 BUSCLK wait states.
10: 1 BUSCLK wait states.
11: 0 BUSCLK wait states.

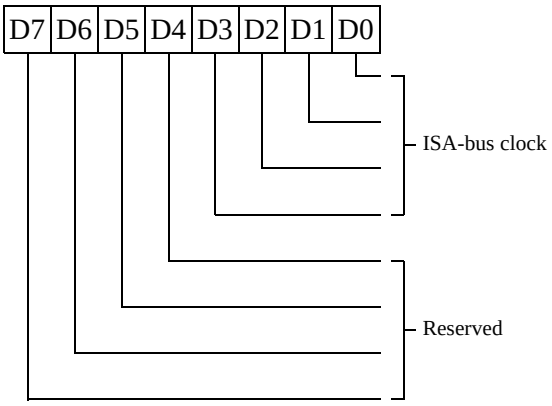
3:2 8-bit AT bus wait states.

00: 5 BUSCLK wait states (default).
01: 4 BUSCLK wait states.
10: 3 BUSCLK wait states.
11: 2 BUSCLK wait states.

1:0 Reserved.

ISA-BUS CLOCK SELECTION

Index Register 07
Default = 00



7:4 Reserved

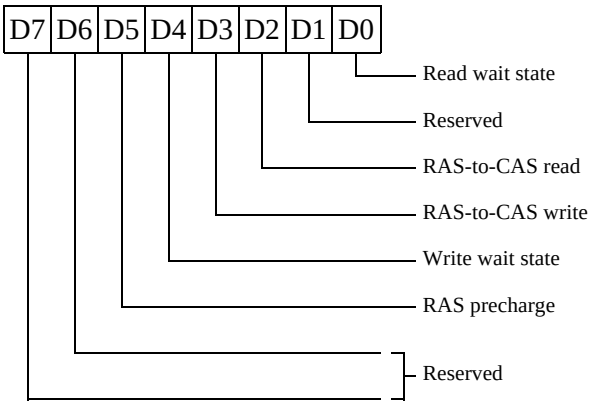
3:0 Clock select for ISA-bus.

The source of the clock is CLK2. Internally, the 84031 uses a clock that is 2x the BUSCLK rate. The CPU speed in parenthesis indicates which settings to use to yield an 8 or 8.33MHz BUSCLK rate. Bit 3 selects a prescaler to the divider of divide by 2 or divide by 1. Bits 2:0 determine the second stage divider.

0000: CLKIN/20
0001: CLKIN/16
0010: CLKIN/12
0011: Reserved
0100: Reserved
0101: Reserved
0110: Reserved
0111: Reserved

1000: CLKIN/10 (40MHz CPU)
1001: CLKIN/8 (33MHz CPU)
1010: CLKIN/6 (25MHz CPU)
1011: CLKIN/5 (20MHz CPU)
1100: CLKIN/4 (16MHz CPU)
1101: CLKIN/3
1110: Reserved
1111: Reserved

DRAM TIMING
Index Register 10
Default = 00



7:6 Reserved, write as 0s.

5 RAS Precharge Time.

0: 2 T states of RAS precharge time.

1: 3 T states of RAS precharge time.

4 Write wait states. Specifies the write timing on DRAM page hits.

0: 0 wait state writes. CAS pulled in the middle of T2.

1: 1 wait state writes. CAS pulled at the end of the first T2.

3 RAS-to-CAS timing for memory write cycles.

0: CAS generated 1 T state after RAS; 1.5 for 1WS write mode (default).

1: CAS generated 2 T states after RAS; 2.5 for 1WS write mode.

2 RAS-to-CAS timing for memory read cycles.

0: CAS generated 1 T state after RAS (default).

1: CAS generated 2 T states after RAS.

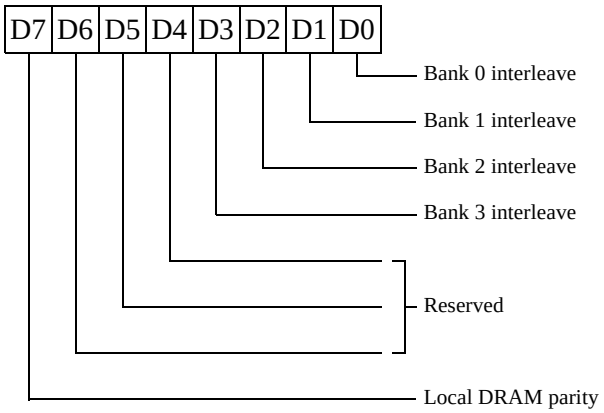
1 Reserved, write as 0.

0 Read Timing Mode.

0: Fast mode; 3-2-2-2 page hits (default).

1: Slow mode; 4-3-3-3 page hits.

DRAM SETUP
Index Register 11
Default = 00



7 Enable Local DRAM parity.

0: Disable.

1: Enable. Bit 7 provides an additional way to disable the parity over and above I/O Port 61. Both bit 7 and bit 2 from I/O port 61 must be enabled (set port 61 to 0). The NMI mask must also be set to send the NMI to the CPU (I/O port 70 bit 7).

6:4 Reserved, write as 0s.

3 Interleave for bank 3.

2 Interleave for bank 2.

1 Interleave for bank 1.

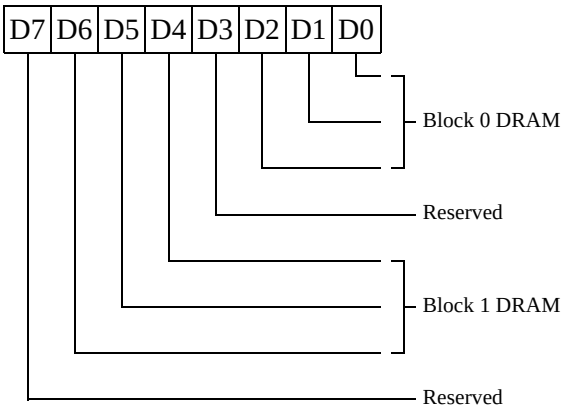
0 Interleave for bank 0.

If a bank is interleaved, its address range is doubled; and it is active only when the interleave bit (A11 or A12) does the comparison. Banks 0 and 2 compare the interleave bit to 0; banks 1 and 3 compare the bit to 1. Two banks must be interleaved at the same address for proper operation. For more information on proper interleaving, see the DRAM Controller section.

0: Do not interleave the bank.

1: Interleave

DRAM CONFIGURATION—BLOCKS 0 AND 1
Index Register 12
Default = 00



Block 0 uses RAS0#. Block 1 uses RAS1#.

7 Reserved, write as 0.

6:4 Block 1 DRAM type:

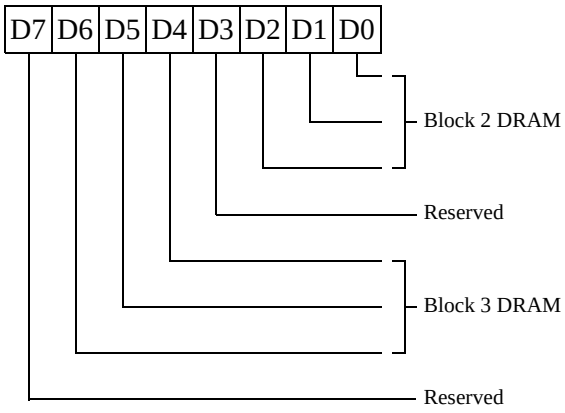
Bit definitions same as block 0.

3 Reserved, write as 0.

2:0 Block 0 DRAM type:

000: Bank disabled.
001: 256K deep DRAMs (256K x 1 or 256K x 4).
010: 1M deep DRAMs (1M x 1 or 1M x 4).
011: 4M deep DRAMs (4M x 1 or 4M x 4).
1xx: Reserved

DRAM CONFIGURATION—BLOCKS 2 AND 3
Index Register 13
Default = 00



Block 2 uses RAS2#. Block 3 uses RAS3#.

7 Reserved, write as 0.

6:4 Block 3 DRAM type:

Bit definitions same as block 0.

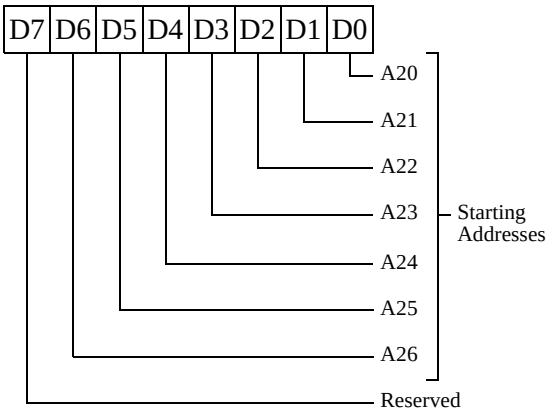
3 Reserved, write as 0.

2:0 Block 2 DRAM type:

Bit definitions same as block 0.

DRAM BLOCK 0-3 STARTING ADDRESS

Index Registers 14 through 17
Default = 00



Index 14—DRAM block 0 starting address.

Index 15—DRAM block 1 starting address.

Index 16—DRAM block 2 starting address.

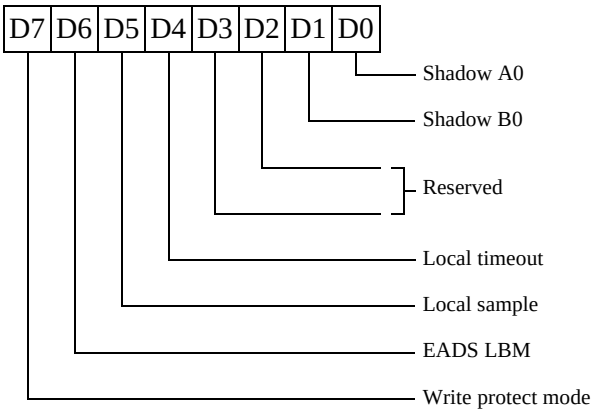
Index 17—DRAM block 3 starting address.

7 Reserved, write as 0.

6:0 A26:20 of starting addresses.

VIDEO AREA SHADOW AND LOCAL BUS CONTROL

Index Register 18
Default = 00



7 Write protect mode.

0: Write protect DRAM *is not* cached in the 486.

1: Write protect DRAM *is* cached in the 486, and EADS# is generated on all writes.

6 EADS generation for a local master.

0: EADS# is floated when a local master has the bus.

1: EADS# is driven when a local master has the bus; and EADS is asserted during the second T2 for all memory write cycles (LBM, ISA master, and DMA).

5 LDEV# sample point.

0: End of first T2 cycle.

1: End of second T2 cycle. This delays the start of all ISA-bus accesses.

4 Local bus timeout.

0: No time out (default).

1: Time out enabled. (84031 generates RDY# if LBT fails to do so within approximately 60 SCLKs after claiming the cycle.)

3:2 Reserved, write as 0s.

1 B0000-BFFFF shadow enable.

0: Access goes to the ISA-bus

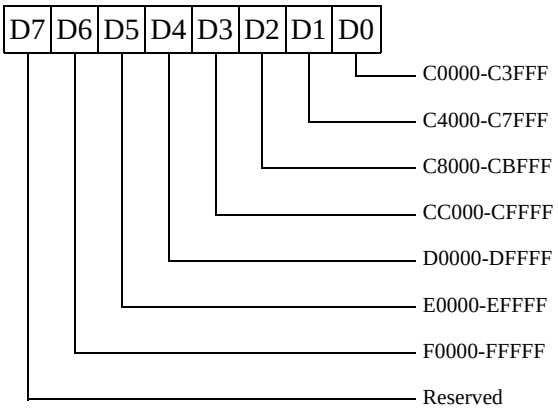
1: Access goes to local DRAM

0 A0000-AFFFF shadow enable.

0: Access goes to the ISA-bus

1: Access goes to local DRAM

DRAM SHADOW READ ENABLE
Index Register 19
Default = 00



If the address range bit is set to 0, it reads that memory location as coming from the ISA-bus. If a bit is set to 1, it reads that memory location as coming from the local DRAM.

7 Reserved

6 F0000-FFFFF

5 E0000-EFFFF

4 D0000-DFFFF

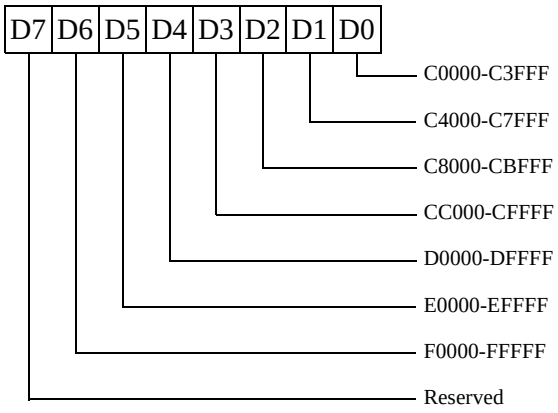
3 CC000-CFFFF

2 C8000-CBFFF

1 C4000-C7FFF

0 C0000-C3FFF

DRAM SHADOW WRITE ENABLE
Index Register 1A
Default = 00



If the address range bit is set to 0, writes to the memory location go to the ISA-bus. If a bit is 1, writes to the memory location go to the local DRAM.

7 Reserved

6 F0000-FFFFF

5 E0000-EFFFF

4 D0000-DFFFF

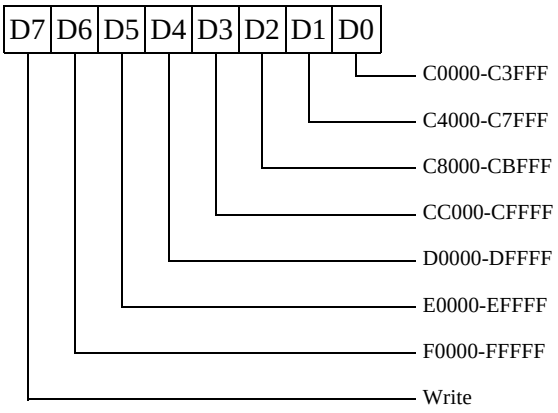
3 CC000-CFFFF

2 C8000-CBFFF

1 C4000-C7FFF

0 C0000-C3FFF

ROMCS ENABLE
Index Register 1B
Default = 60h



If the address range bit is set to 1, the ISA-bus reads from that memory location and activates ROMCS#. If the memory bit is set to 0, ROMCS# is not activated. Note: ROMCS# is not activated if an access is directed to local DRAM.

7 Activate ROMCS on writes also, default = 0.

0: Does not activate on writes.

1: Activates ROMCS# on ISA writes to the addresses selected by the remainder of this register.

6 F0000-FFFFF, default = 1.

5 E0000-EFFFF, default = 1.

4 D0000-DFFFF, default = 0.

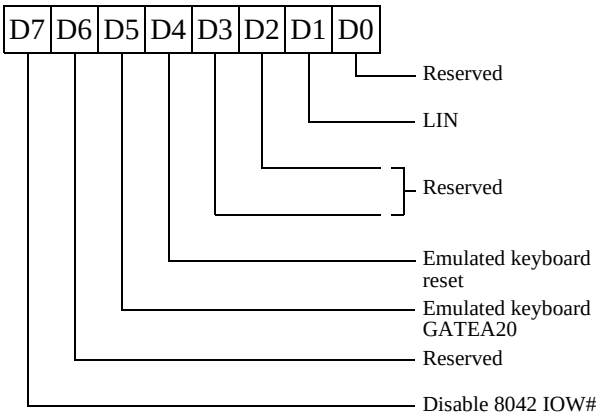
3 CC000-CFFFF, default = 0.

2 C8000-CBFFF, default = 0.

1 C4000-C7FFF, default = 0.

0 C0000-C3FFF, default = 0.

SOFT RESET AND GATEA20
Index Register 1C
Default = 00



7 Disables IOW# to 8042 for emulated commands.

0: All 8042 commands go to the 8042.

1: GATEA20 and RESET2 commands to the 8042 have IOW# blocked to speed up the operation of the 8042 commands.

6 Reserved, write as 0.

5 8042 GATEA20 emulation.

0: The emulated 8042 GATEA20 logic ignores 8042 commands.

1: 8042 commands are enabled to the emulated 8042 GATEA20 logic.

4 8042 RESET2 emulation.

0: Disabled

1: The emulated 8042 KBRST# function will cause a soft reset to the CPU.

3:2 Reserved, write as 0s.

1 LIN pin function.

0: Test function (default).

1: Link input (normal operation).

0 Reserved, write as 0.

RESERVED (DO NOT WRITE)
Index 1D-1F

84035 I/O PORT ADDRESSES

Listed below are the 84035 I/O port addresses that are described in this section. (Figures are provide for the registers, where applicable.)

- DMA controller 1 (8-bit DMA)
- Interrupt controller 1 (IRQ7:0)
- Configuration register address port
- Timer (8254)
- Port B
- Real time clock address port and NMI mask
- Real time clock data port
- DMA page registers
- Fast CPU reset and GATEA20
- Interrupt controller 2 (IRQ15:8)
- DMA controller 2 (16-bit DMA)

All registers specific to the 84035 are summarized in the 84031 and 84035 I/O Port Summary and the 84031 and 84035 Configuration Register Summary tables.

DMA CONTROLLER 1 (8-BIT DMA)
Port Addresses 00-0F

Port addresses 00 through 0F are contained in the IPC megacell. The DMA controller will *not* respond to accesses to 10-1F. (In the original AT-compatible, 00-0F repeats at 10-1F.)

INTERRUPT CONTROLLER 1 (IRQ7:0)
Port Addresses 20-21

These ports are contained in the IPC megacell. The Interrupt controller does *not* respond to ports 22-3F.

CONFIGURATION REGISTER ADDRESS PORT
Port Address 22

This is a write only port which holds the address of the Chips and Technologies index register. The register can only be accessed through I/O port 23. It must be written before each access to port 23, even if the same index register is being accessed twice in a row.

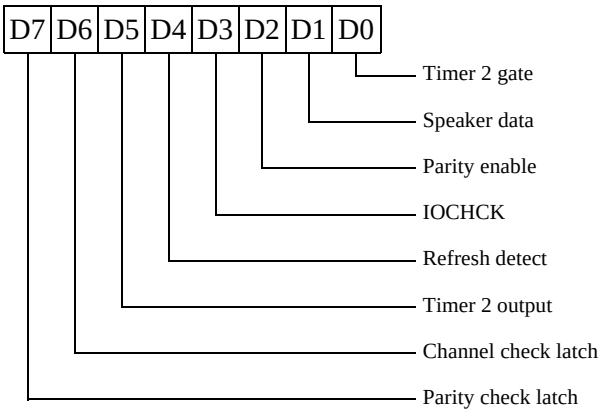
CONFIGURATION REGISTER DATA
Port Address 23

Accessing port 23 accesses the configuration register as pointed to by port 22. A second access to port 23 without writing to port 22 in between will be ignored. On write, "reserved" bits should be written as 0s. On read, the value read back may be unpredictable. The value read can always be safely written.

TIMER (8254)
Port Addresses 40-43

These ports are contained in the IPC megacell. The timer does *not* respond to ports 44-4F.

PORT B
Port Address 61
Default = 0F



This is an AT-compatible port with miscellaneous information. Bits 3:0 are read/write. Bits 7:4 are read only. Only bits 5:0 are available in the 84035 (bits 2 and 3 are there for read-back purposes only). The remainder is available on the 84031. On I/O reads, the 84035 drives bits 5:0 to their proper values, and bits 6 and 7 to 0s.

7 Parity check latch.

Read only. Bit 7 is not available in the 84035. The 84035 will drive bit 7 to 0 on reads. This bit will result from bit 3 Q# output.

6 Channel check latch.

Read only. Bit 6 is not available on the 84035. The 84035 will drive bit 6 to 0 on reads. This bit will result from bit 4 flip-flop Q output.

5 Timer 2 output.

Read only. Bit 5 allows the software to monitor the output of timer 2. Timer 2 is ANDed together with bit 1 produces the speaker signal.

4 Refresh detect.

This read only bit toggles on each refresh. It should toggle whenever timer 1 produces a pulse (about every 15µs). This should be done even if ISA refresh is disabled. Some software uses this as a time delay.

3 Enable IOCHCK.

0 enables local the IOCHCK interrupt. 1 disables IOCHCK and clears the IOCHCK flip-flop. Bit 3 is inverted and sent to the active low clear of a flip-flop. IOCHCK is sent to the active low preset input. The Q# output is fed to the NMI logic. The Q output is sent to bit 6. The flip-flop (ALS74 on AT-compatibles) has preset input precedence over Q. The clear input has precedence over Q#.

2 Enable parity check.

0 enables local DRAM parity checks. 1 disables local DRAM parity checks and clears the local parity error flip-flop. Bit 2 is inverted and sent to the active low preset of a flip-flop. The Q output is PCK# and is fed to the NMI logic. A parity error clocks the flip-flop to 0. An index register bit blocks local DRAM parity errors. It prevents the flip-flop from being clocked. The flip-flop (F74 on AT-compatibles) has preset input precedence over Q. The clear input has precedence over Q#.

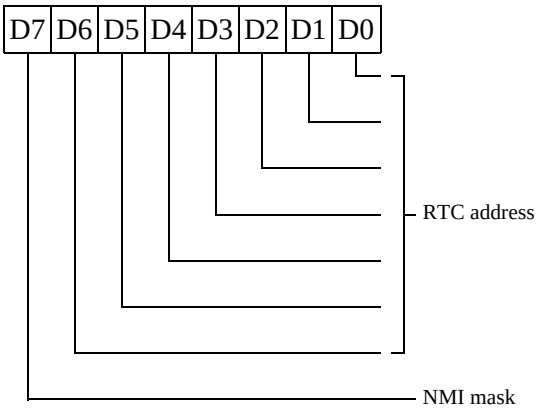
1 Speaker data.

Bit 1 is ANDed with the output of timer 2 to produce the actual signal sent to the speaker. When the gate is low (see bit 0) this bit gives direct software control of the speaker.

0 Timer 2 gate.

Timer 2 is the speaker with R/W function. When this bit is 1, the timer is enabled, and if programmed to do so, will produce a square wave of the programmed frequency. When this bit is a 0 the timer output will be high.

REAL TIME CLOCK ADDRESS PORT AND NMI MASK
Port Address 70



7 NMI mask—Nonmaskable interrupt mask.

Bit 7 is not available on the 84035. It is available in the 84031 as write only. Bit 7 is inverted and ANDed with the NMI sources (the OR from several sources). The result of the AND function is NMI to the CPU.

6:0 RTC—Real Time Clock address.

Write only. The values written to bits 6:0 becomes the address for RTC/CMOS RAM. (The actual reading and writing is performed with port 71.)

REAL TIME CLOCK DATA PORT
Port Address 71

Reading or writing this port will read or write the RTC register pointed to by the last occurrence of write to port 70.

DMA PAGE REGISTERS
Port Addresses 80-8F

These ports are contained in the IPC megacell. DMA accesses are through A23:16. (A23:17 for 16-bit DMAs).

Port Address 80—Not used. This port is written to by BIOS routines to indicate BIOS status. A pair of hex 7 segment LEDs are often placed on test boards to display BIOS information.

Port Address 81—Channel 2 page register.

Port Address 82—Channel 3 page register.

Port Address 83—Channel 1 page register.

Port Addresses 84-86—Not used.

Port Address 87—Channel 0 page register.

Port Address 88—Not used.

Port Address 89—Channel 6 page register.

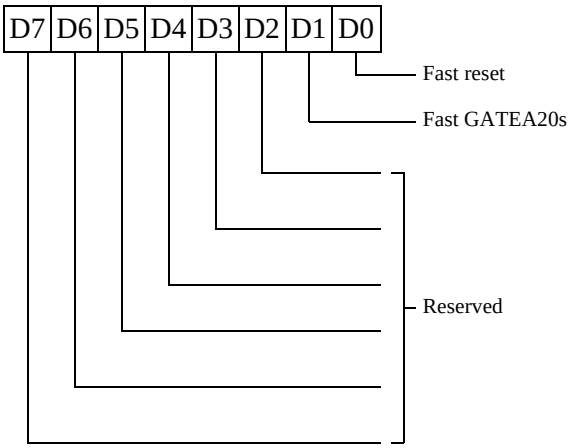
Port Address 8A—Channel 7 page register.

Port Address 8B—Channel 5 page register.

Port Addresses 8C-8E—Not used.

Port Address 8F—Refresh page register. This register is placed on SA19-17 during refresh cycles.

FAST CPU RESET AND GATEA20
Port Address 92



7:2 Reserved, write as 0s.

1 Fast GATEA20.

ORed with other GATEA20 signals (from 8042, for example).

0: Force A20 low from the CPU (assuming all other GATEA20s are low).

1: Allow A20 from the CPU to pass through.

0 Fast CPU reset.

0 to 1 transition activates a CPU reset.

INTERRUPT CONTROLLER 2 (IRQ15:8)
Port Addresses A0-A1

These ports are contained in the IPC megacell. The interrupt controller does *not* respond to ports A2-BF.

DMA CONTROLLER 2 (16-BIT DMA)
Port Addresses C0-DF

These ports are contained in the IPC megacell. Only the even numbered ports are used. Reads or writes to the odd numbered ports will access the same register as its corresponding even numbered port.

84035 CONFIGURATION REGISTERS

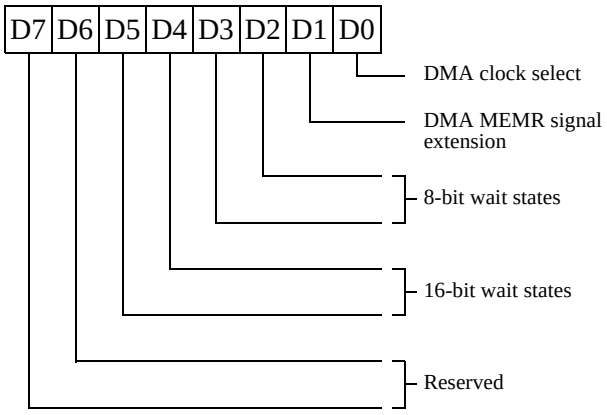
Listed below are the 84035 configuration registers that are described in this section. (Figures are provide for the registers, where applicable.)

- DMA wait state control
- Performance control
- 84035 miscellaneous control
- DMA clock selection.

All registers specific to the 84035 are summarized in the 84031 and 84035 I/O Port Summary and the 84031 and 84035 Configuration Register Summary tables.

DMA WAIT STATE CONTROL

Index Register 01
Default = 00



The normal ISA timing is default = 00.

7:6 Reserved.

5:4 16-bit DMA wait states.

Bits 5:4 controls the number of wait states inserted during 16-bit DMA transfers. Use the values below:

00: One wait state (default).
01: Two wait states.
10: Three wait states.
11: Four wait states.

3:2 8-bit DMA wait states.

Bits 3:2 controls the number of wait states inserted during 8-bit DMA transfers. Use the values below:

00: One wait state (default).
01: Two wait states.
10: Three wait states.
11: Four wait states.

1 DMA MEMR# signal extension.

In the IBM PC /AT, the assertion of MEMR# is delayed by one DMA clock cycle compared to IOR#. This may not be desirable in some systems.

0: Enables delayed MEMR# function (default).
1: Starts MEMR# at the same time as IOR#.

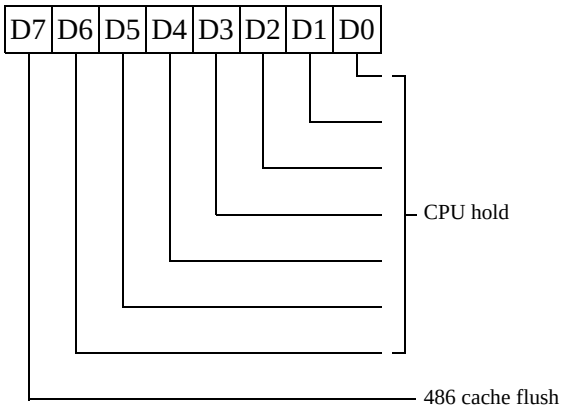
0 DMA clock select.

Bit 0 allows the user to program the DMA clock to operate at either BUSCLK or BUSCLK/2. The same DMA clock drives both 8-bit and 16-bit operations.

0: BUSCLK/2 (default).

1: BUSCLK.

PERFORMANCE CONTROL
Index Register 08
Default = 00



7 486 cache flush.

0: Does not flush cache during slow mode HOLD.

1: Flush cache during each slow mode hold request. Setting this bit to a 1 prevents the 486 from running out of internal cache during the slow mode hold.

6:0 CPU hold pulse width.

Bits 6:0 sets the amount of time in which the CPU is kept on hold following each AT bus refresh. Once the count is set, the mode must be enabled by a separate register or by switching the turbo button. The values below are the number of BUSCLKs in which the CPU is kept on hold. This occurs about every 15µS.

000000: No hold request (default).

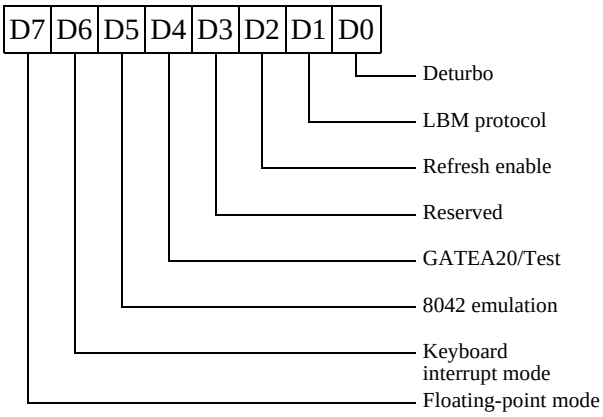
000001: Minimum speed reduction (1 BUSCLK).

000010: 2 BUSCLKs.

.
.
.

111111: Maximum speed reduction (127 BUSCLKs).

84035 MISCELLANEOUS CONTROL
Index Register 09
Default = 00



7 Floating-point error mode.

0: For internal (486) mode, FERR# and IGNNE# pins are provided. IRQ13 is generated internally (default).

1: For external mode, IRQ13 and INTCLR pins are provided. The remainder of the logic is provided externally. This mode is used for systems where a pin for IRQ13 is required (e.g. systems with a Weitek coprocessor).

6 Keyboard interrupt mode. Bit 6 should be 0.

0: IRQ1 is received on the pin directly.

1: IRQ1 is received over the control link.

5 GATEA20 emulation disable.

0: A20M# is controlled only by port 92h GATEA20—the default. Following reset, port 92h is 00, but bit 4 above is also 0. This causes the A20M# pin to act as the TEST# input and an external pull-up keeps the CPU A20M# signal in the high state as needed for proper CPU startup.

1: Pin A20M# is the OR of port 92 GATEA20 and the emulated 8042 GATEA20 information received across the control link.

4 A20M#/TEST# and LOUT pin enable function. Note: Index register 1C bit 1 should be set to 1 before setting this bit to 1.

0: A20M#/TEST#, when low, forces the input signal of the 84035 into test mode. The LOUT signal is also floated to allow the 84031 LIN signal to be used for the test mode (default).

1: A20M#/TEST# as an output signal, drives A20M#. Test mode is disabled and the LOUT pin is driven.

3 Reserved, write as 0.

2 Refresh request enable.

Bit 2 blocks the Timer 1 refresh request when disabled. It prevents reset problems, which may occur when a refresh request is generated during the reset sequence. For the 8254, timing is not disabled at reset.

0: Block the Timer 1 refresh requests.

1: Enable Timer 1 refresh requests.

1 Preemptive protocol for LGNT.

0: Non-preemptive protocol. The arbitration will not take LGNT# inactive until LREQ# has gone inactive (default).

1: Preemptive protocol. The arbitration logic will take LGNT# low when the DMA controller requests the bus. It will wait for LREQ# to go inactive before granting the bus to the DMA controller. This is VL-Bus compatible.

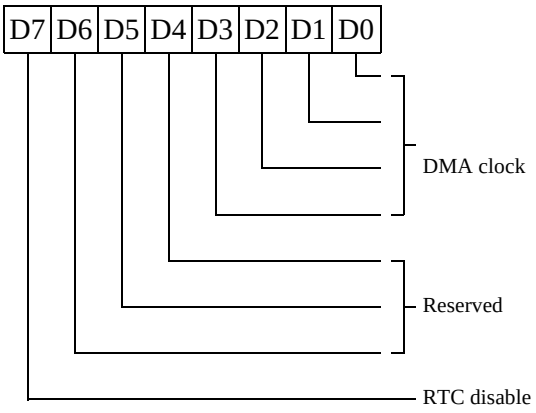
0 Deturbo (performance control enable).

Bit 0 enables the performance control that is programmed into register 0A. This bit is ORed with the inverting of the turbo switch.

0: Normal mode (default).

1: Performance control enabled.

DMA CLOCK SELECTION
Index Register 0A
Default = 00



7 RTC disable.

0: Enable normal operation of the internal RTC.

1: Disable the internal RTC. This allows an external RTC to be used. 32KHz input becomes IRQ8#. Ports 70h and 71h are disabled, except for port 70h bit 7 in the 84031 (NMI control.)

6:4 Reserved, write as 0s.

3:0 Clock select for DMA controllers.

Bits 3:0 in this register normally should be set to the same hex value as index 07 bits 3:0.

The IPC may optionally further divide this clock by 2 before sending it to the DMA controllers (it should be programmed to do so, see index 00). The source of the clock is SCLK, which is the 1x CPU clock. The resulting clock should be about 8MHz. The IPC megacell will then divide by 2 to get the 4MHz used by the DMA controllers. Higher rates may be used at the risk of incompatibilities with the DMA devices. Bit 3 selects a prescaler to the divider of divide by 2 or divide by 1. Bits 2:0 determines the second stage dividers, which is /2, /4, /3, /2.5, /2, or /1.5.

0000: SCLK/10
0001: SCLK/8
0010: SCLK/6
0011: Reserved
0100: Reserved
0101: Reserved
0110: Reserved
0111: Reserved

1000: SCLK/5 (40MHz SCLK)
1001: SCLK/4 (33MHz SCLK)
1010: SCLK/3 (25MHz SCLK)
1011: SCLK/2.5 (20MHz SCLK)
1100: SCLK/2 (16MHz SCLK)
1101: SCLK/1.5
1110: Reserved
1111: Reserved

CS4031 System Level Functions

The overview of the system level functions for the 84031 and the 84051 is listed below.

- Clocks
- Reset and GATEA20
- Arbitration
- Refresh
- Coprocessor Logic
- Address Mapping
- ISA-Bus
- Local Bus Support
- DRAM Controller
- Data Buffers.

CLOCKS

A 2x clock is provided in the 84031, which then creates a 2x and 1x clock with very low skew. In most systems these may be used for the system 2x and 1x clocks and are fed back into the 84031, with the 1x clock also going to the 84035 and the CPU. If additional clock loading is necessary, such as for local bus devices including VL-Bus slots, both clocks may be buffered externally. If buffered, the same chip should be used for all of the buffering, such as half of a F244.

The 1x and 2x may also be provided as an external option. This is done with either a F112 chip or one of several clock generator chips such as the Avasem 9155 or ICD2027. The 2x clock is sent to the 84031, while the 1x is sent to the 84031, the 84035, and the CPU.

The following clocks are used in the system:

CLK2	2x CPU clock for the DRAM controller.
SCLK	1x CPU clock for the CPU, etc.
OSC	14.31818MHz for the timers and ISA-bus.
32KHz	Real time clock.

RESET AND GATEA20

The reset and GATEA20 logic is available in the 84035. In addition, the CS4031 CHIPSet has the ability to emulate the reset and/or GATEA20 signals normally generated by the 8042.

The 84035 receives the reset from the power supply or power up clear logic. It also receives CPU restart commands from the 8042 (or emulation of the 8042) across the control link from the 84031 and from port 92, which is internal to the 84035. The 84035 generates SYSRESET and CPURESET. SYSRESET goes active only at power up or by pushing a RESET button. CPURESET goes active for CPU soft restarts also.

A20 is gated in the CPU only. The 84035 provides A20M#, which is the OR of the port 92 GATEA20 and the 8042 GATEA20.

ARBITRATION

The 84035 contains all of the arbitration logic. It arbitrates between the CPU, local bus masters, DMA, and ISA masters. Refresh is always hidden, and occurs when either the CPU or local master has control of the bus.

Local bus masters are supported in accordance to the VL-Bus standard. The 84035 will preempt the local bus master off of the bus when an unmasked DMA request occurs.

REFRESH

ISA-bus refresh is done by the 84035. It drives REFRESH#, MEMR#, and SA7:0. Refresh is always hidden. The ISA-bus must be arbitrated to prevent the 84031 from doing an ISA-bus cycle at the same time as the 84035 is doing a refresh cycle. This is handled by the control link. The sequence are as follows:

1. When timer 1 produces a refresh request, the 84035 sends a REFRESH REQUEST code to the 84031.
2. The 84031 will arbitrate this request with any pending ISA-bus request from CPU or local bus master. When the ISA-bus is free and available for refresh it sends a REFRESH ACKNOWLEDGE to the 84035. The 84031 will delay any ISA-bus requests at this point.
3. The 84035 will do the refresh cycle on the ISA-bus, then issue a REFRESH COMPLETE code to the 84031.
4. The 84031 is free to do an ISA-bus access after receiving the REFRESH COMPLETE code.

Local DRAM receives the timer tick refresh requests and the master refresh indicator from the control link. DRAM refresh cycles are then placed between other DRAM activity.

COPROCESSOR LOGIC

The coprocessor logic is in the 84035. It has pins for FERR# and IGNNE#. IRQ13 is generated internally. A write to I/O ports F0 or F1 clears the interrupt.

ADDRESS MAPPING

Each chip decodes the I/O ports and configuration registers used internally. The 84031 also decodes memory for local DRAM.

ISA-BUS

CPU and local master accesses to the ISA-bus are handled by the 84031. The 84035 is an ISA slave at that time. The 84035 contains the DMA controllers, and becomes the master for DMA cycles, and provides the arbitration for ISA masters. The 84031 is an ISA slave at that time, and converts ISA cycles to local bus cycles for local DRAM and local bus slaves.

LOCAL BUS SUPPORT

The CS4031 CHIPSet fully supports the VESA VL-Bus. Both local bus slaves and masters are supported and does not require external logic for a single VL-Bus slot. Below is a brief description of the VL-Bus support. Refer to the Local Bus section for more details:

For the 84031:

Samples LDEV# at the start of each bus cycle (either the end of the first or second T2) and allows a local bus slave to capture the cycle if active.

Translates DMA and ISA master cycles to local bus cycles when LDEV# is active.

Allows local masters to access most of the system resources as if it were the CPU.

For the 84035:

Provides a set of LREQ and LGNT# signals for local bus masters.

DRAM CONTROLLER

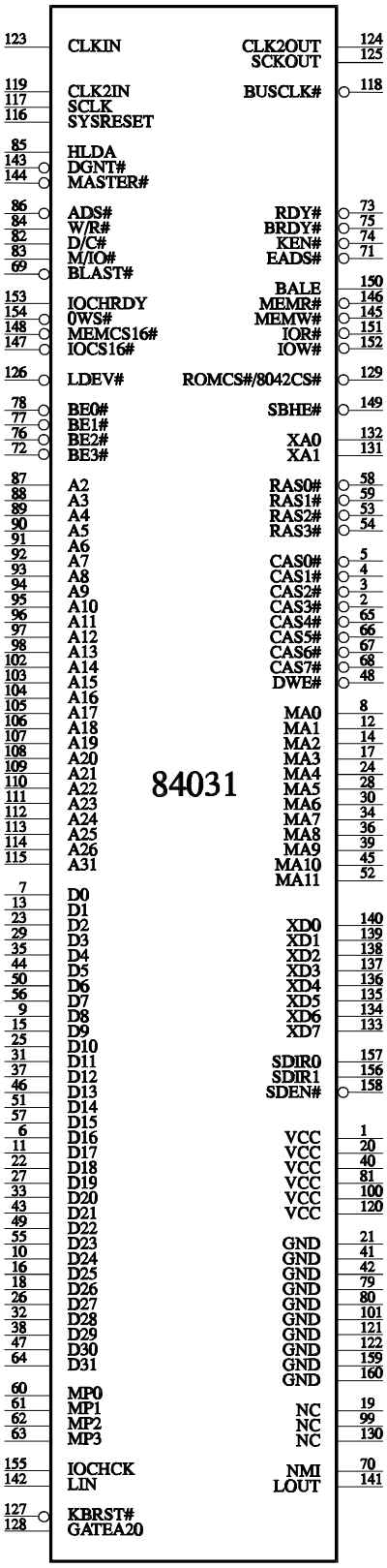
The 84031 integrates a high-performance DRAM controller that supports page mode or 2-way page interleave operation. The DRAM controller supports up to four banks of DRAM with mixing of 256K, 1M, and 4M devices. This includes 4M x 4 DRAMs with either 11/11 or 12/10 row/column addressing.

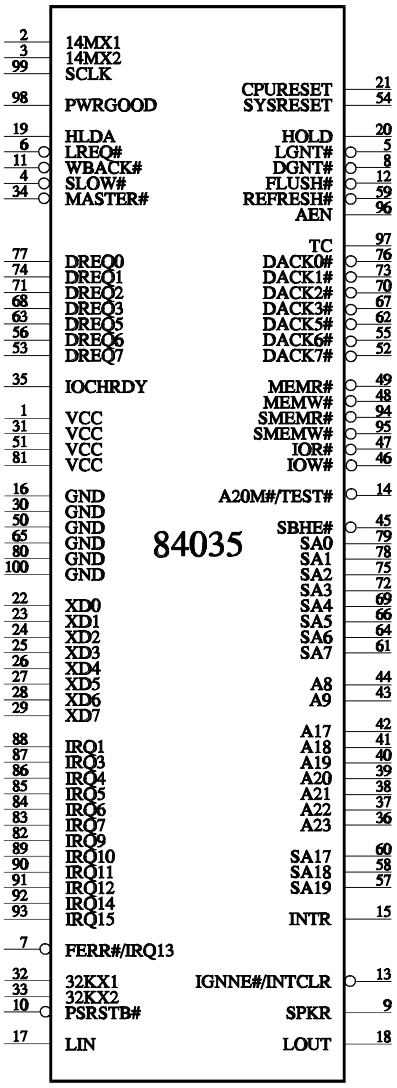
The DRAM is directly interfaced to the local data bus. The RAS#, CAS#, DWE#, and MA lines are driven directly from the 84031 for up to two banks, with a maximum of 24 loads. For additional banks, F244 buffers must be used on the MA and DWE lines.

For reads, the page hit cycles perform a 3-2-2-2 burst at all speeds. For writes, the page hits are either 0 or 1WS accesses.

DATA BUFFERS

Data buffering for the ISA bus is performed by the 84031. XD7:0 are generated by the 84031. These are buffered by an LS245 to form SD7:0. SD15:8 are generated by external buffers from either D15:8 or D31:24, as appropriate.





Schematic Symbols

84031 Functional Descriptions

CLOCKS

The 84031 receives the 1x and 2x CPU clock, and generates BUSCLK for the ISA-bus. It also contains an optionally used clock divider which takes a 2x clock from the oscillator and provides a low skew 1x and 2x clock for the system.

Clock Divider

The clock divider consists of the following pins:

CLKIN	2x clock from the oscillator.
CLK2OUT	2x clock output.
SCLKOUT	1x clock output.

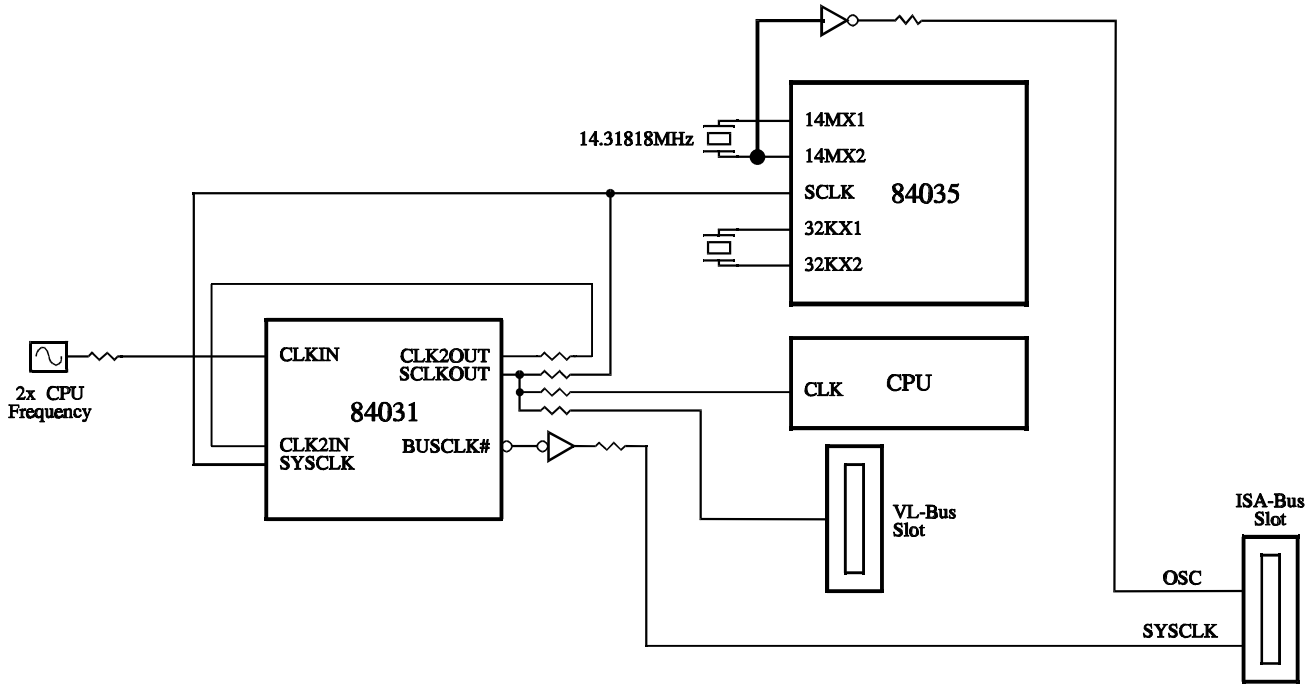
This circuit is completely independent from the other clocks (i.e. CLK2 or SCLK) and are not used internally. In minimum systems the CLK2OUT and SCLKOUT pins may be used directly. CLK2OUT will be fed back into the 84031. SCLKOUT will feed back into the 84031 and also feed into the 84035 and CPU. In a system where there are additional clock loadings, such as one containing VL-Bus slots, CLK2OUT and SCLKOUT may be buffered externally before being used. Half of the F244 should be used, with one gate being used for CLK2 and the other three gates for SCLK. Care should be taken to avoid adding skew to the clocks.

Clock Inputs

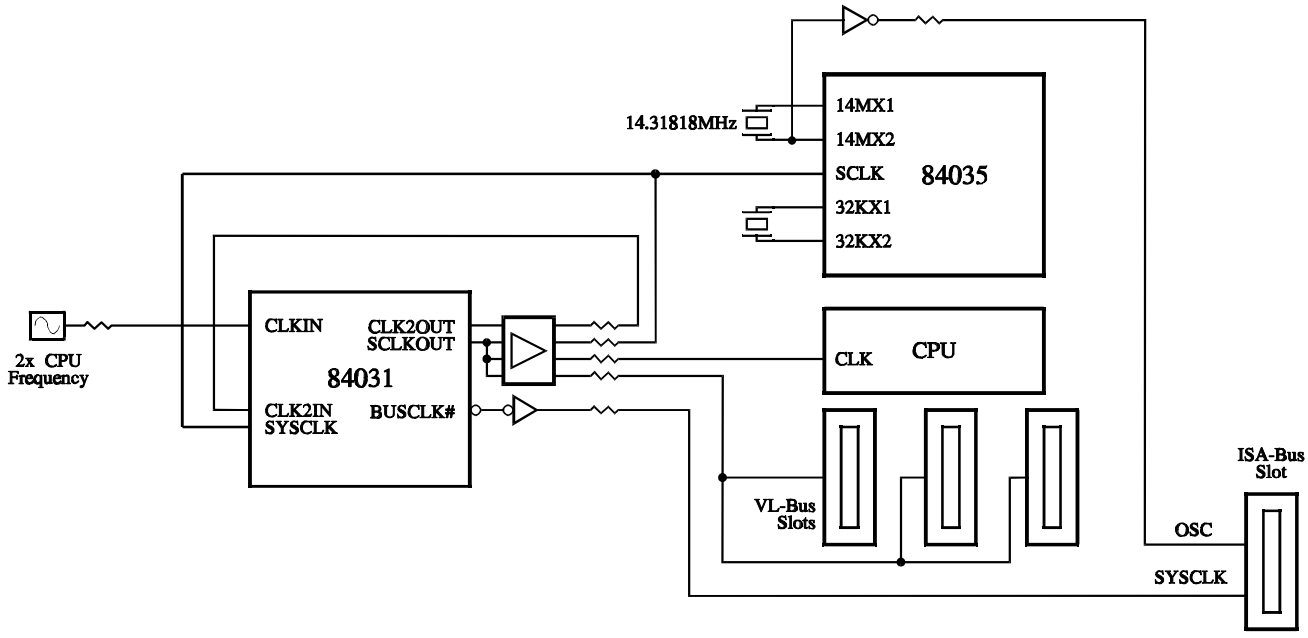
The 84031 has two clock inputs which are as follows:

CLK2	2x CPU clock.
SCLK	1x CPU clock.

The following two figures shows clock connections for normal and for heavy load connections.



Normal Clock Connection



Clock Connections With Heavier SCLK Load

BUSCLK Generation

BUSCLK is generated from a divider from CLK2. The divider produces the clock used by the ISA-bus state machine which is twice the BUSCLK rate. The following table lists the dividers and the frequencies at which it will be used to obtain a standard ISA-bus frequency.

SUGGESTED BUSCLK DIVIDERS FOR EACH CPU FREQUENCY

Divider	CLK2 Freq. (MHz)	CPU Freq. (MHz)	ISA State Machine Rate (MHz)	BUSCLK Rate (MHz)
4	66	33	16.67	8.33
3	50	25	16.67	8.33
2.5	40	20	16	8
2	32	16	16	8

The power-up default is divide by 10, which is then changed by the BIOS to the appropriate value.

The following table lists the resulting BUSCLK rate for the most common dividers at all CPU rates.

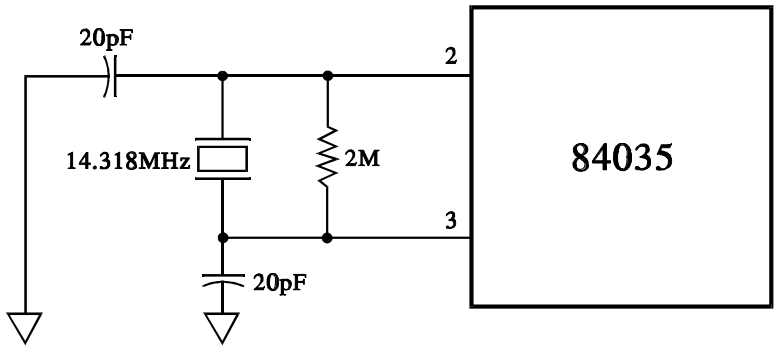
POSSIBLE ISA-BUS CLOCK FREQUENCIES AT EACH CPU FREQUENCY

Selection	CPU Operating Speed			
	16MHz	20MHz	25MHz	33MHz
CLK2/1.5	10.7	13.3	16.6	22.2
CLK2/2	8	10	12.5	16.3
CLK2/2.5	6.4	8	10	13.3
CLK2/3	5.3	6.7	8.33	11.1
CLK2/4	4	5	6.25	8.3
CLK2/5	3.2	4	5	6.67
CLK2/6	2.67	3.3	4.17	5.56

14.31818MHz Clock

The 84035 requires a 14Mhz clock input. Crystal pins are provided for clocks that run at 14.31818MHz. Each pin should include 20pF capacitors for grounding as well as a 2M resistor across the pins. X2 should be buffered with a bus driver or inverter to form oscillation for the bus. A 33 ohm series resistor should be placed between the buffer and the bus. Place the resistor as close to the buffer as possible.

The 14.31818MHz clock is divided by 12 internally to form the 1.19MHz clock which is used by the IPC timers.



14MHz Clock Circuit

SCLK

SCLK, the 1x CPU clock, is provided to the 84035. In a 486 system, a 1x clock with low skew to the 2x clock must be provided (this is also required for VL-Bus slots).

SCLK is used for the arbitration logic, for the control link timing, and generation of the clock to the DMA controllers and refresh logic.

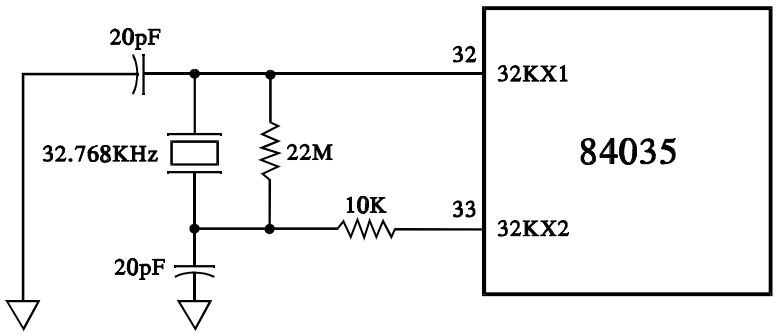
The DMA controller together with the refresh clock should be configured to run approximately 8MHz. It is divided by 2 by the IPC core to obtain 4MHz for the DMA controllers normally operate. The following dividers are provided from SCLK to form the DMA clock. The divider is actually implemented as a selectable divide by 2 prescaler followed by a programmable divider of 2, 2.5, 3, 4, or 5. See table 84035 Clock Divider.

32.768KHz Clock

The clock source is a 32KHz internal oscillator used by the real time clock in the 84035. An external oscillator can be used if desired. In that case, use 32KX1 as input and leave 32KX2 unconnected.

84035 CLOCK DIVIDER

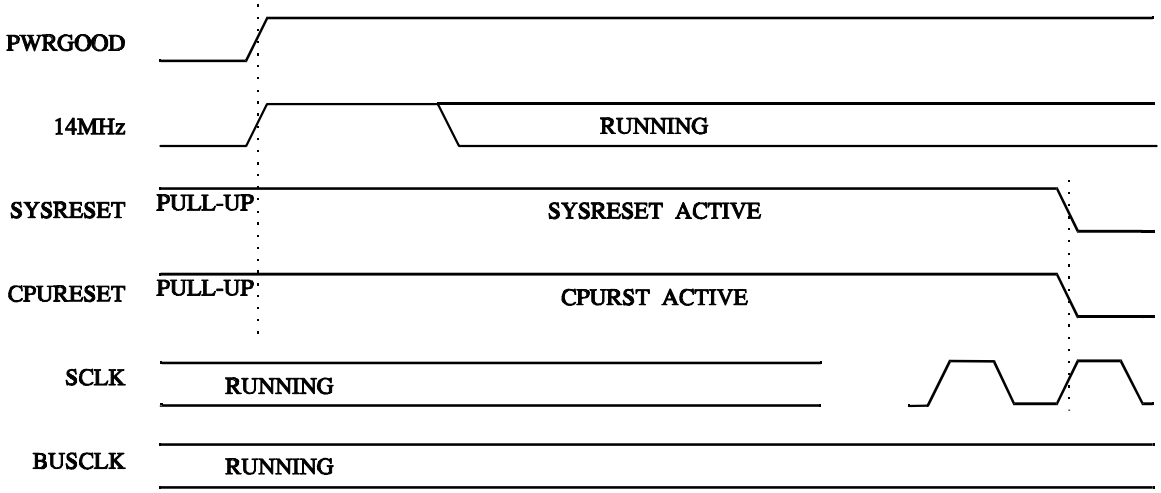
Divider	Pre-scale	2nd Stage	CPU Freq. Used (MHz)	DMA Clock Freq. (MHz)	8237 Clock Rate (MHz)
10	/2	/5	80	8	4
8	/2	/4	66	8	4
6	/2	/3	50	8.33	4.17
5	/1	/5	40	8	4
4	/1	/4	33	8.33	4.17
3	/1	/3	25	8.33	4.17
2.5	/1	/2.5	20	8	4
2	/1	/2	16	8	4



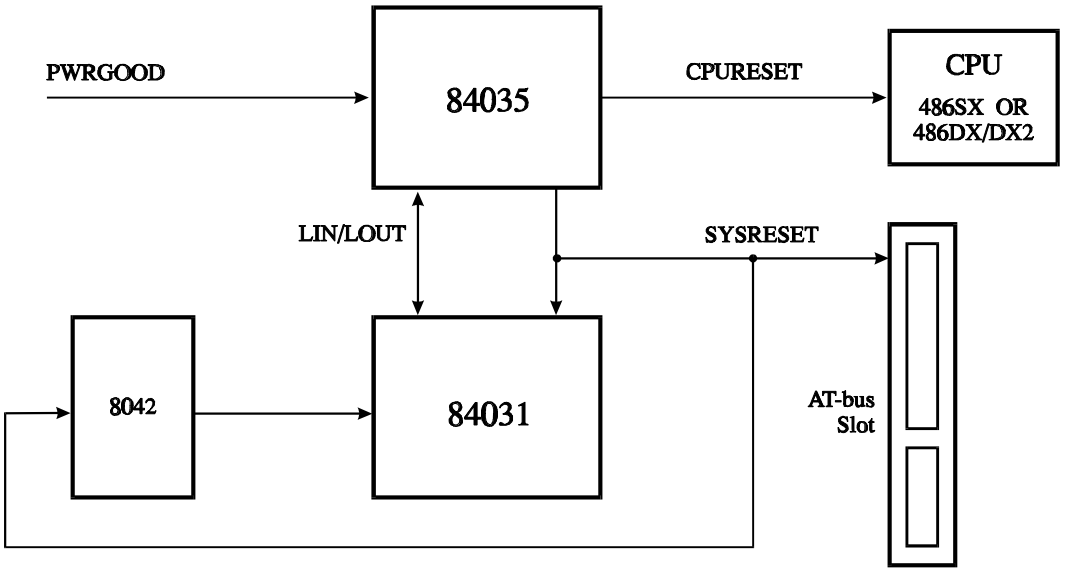
Recommended 32KHz Clock Circuit Diagram

SYSTEM RESET LOGIC

There are two input sources used to initiate a system reset, these are PWRGOOD and KBRST#. The PWRGOOD reset is usually provided by the power supply and will activate the CPURESET and SYSRESET outputs. The KBRST# is supplied by the 8042 keyboard controller or by an emulated KBRST# function within the 84031.



Power-On Reset Timing Diagram



Reset Block Diagram

Reset From PWRGOOD

The 84035 contains the reset logic for the system. It receives PWRGOOD reset request signals and generates SYSRESET and CPURESET signals. It also receives soft reset requests over the control link to generate CPURESET.

PWRGOOD disables all outputs and gates off all inputs to the 84035 except for PSRSTB, the 32KHz oscillator pins, and PWRGOOD itself. When PWRGOOD goes high the outputs are enabled. SYSRESET and CPURESET are driven high, and remain high for 8 million SCLKs (0.24 second at 33.3MHz) to assure proper startup of the 14.31818MHz oscillator, and to allow the 486 VCO to stabilize.

If a 2x clock is provided, the 84035 determines the phase of SCLK, and indicates this to the rest of the system by the generating of SYSRESET and CPURESET. It does so based on its internal SCLK, and will make the high to low transition of the reset pins during phase 1, when SCLK is high. Once the 84035 has determined the phase, it will use this same phase for CPU resets which occur after power up.

If the 84035 is used in an 80386 system (non-84031), a flip-flop should be used to delay CPURESET to the CPU until the low state of SCLK (phase 2).

SYSRESET is generated from the PWRGOOD circuit alone. CPURESET is generated from the PWRGOOD, and can also be generated for "soft resets." The following are the sources of soft resets:

- Keyboard controller reset
- CPU shutdown cycle
- Port 92 bit 0 transitioning from 0 to 1.

Keyboard reset and shutdown are sent to the 84035 through a control link from the 84031. When the 84035 receives the request, it immediately passes the request on to the logic that arbitrates CPURESET with CPU HOLD. See the Control Link section for information on how the reset request is sent from the 84031.

Port 92 is available on the 84035. When bit 0 makes a 0 to 1 transition a CPU reset is requested at about 16 BUSCLKs later. This delay allows the CPU to execute a HALT instruction.

The 84035 arbitrates between CPURESET and the CPU HOLD signal to prevent both from occuring simultaneously. If the CPU is currently in HOLD when the reset request occurs, the reset is delayed until after the HOLD is removed. Likewise if a hold request is issued during the CPU reset sequence, it is delayed until after the CPURESET is removed.

CPURESET is 16 SCLKs long for soft resets. The falling edge always occurs during phase 1 while SCLK is high.

SYSRESET

The 84031 receives SYSRESET as an input from the 84035. This input resets all registers and state machines to a known state. Since the 84035 receives its clock from SCLK, which it uses to generate resets, the clock divider circuit operates while SYSRESET is active.

Both the CPURESET and A20M (final GATEA20 to the CPU) pins are available on the 84035. The 84031 provides information to the 84035 for both functions. This information is sent to the 84035 over the control link. The 84031 performs the following functions:

- Detects a CPU shutdown.
- Detects a CPU reset request from the external 8042.
- Optionally emulates the 8042 CPU reset request.
- Detects a change on the GATEA20 signal from the external 8042.
- Optionally emulates the 8042 GATEA20 signal for speeding up the operation.

CPU Shutdown

The CPU shutdown is detected (see the "Special Cycle Encoding" table below). The table also shows the encoding for all of the "special" cycles. Only SHUTDOWN causes the CPU to restart. The 84031 transmits a shutdown code to the 84035 as soon as it is detected. Then the 1-wait state RDY is returned in response to any of the special cycles.

SPECIAL CYCLE ENCODING

Cycle	M/IO#	D/C#	W/R#	Address	BE3:0#	BE3#	BE2#	BE1#	BE0#
Shutdown	0	0	1	00000000	E	1	1	1	0
Flush	0	0	1	00000001	D	1	1	0	1
Halt	0	0	1	00000002	B	1	0	1	1
Write Back	0	0	1	00000003	7	0	1	1	1

GATEA20 Function

The 84035 generates A20M#. The 486 actually does the gating. There are two sources for A20M:

- Keyboard controller GATEA20
- Port 92 bit 1.

The keyboard controller GATEA20 information is sent from the 84031 through the control link. GATEA20 = 1 and GATEA20 = 0 codes are sent across. This sets and resets the flip-flop to form the keyboard GATEA20 in the 84035. This flip-flop powers up in the high state to allow the CPU to boot.

Port 92 bit 1 is an output port bit internal to the 84035.

The two internal sources of A20M# are ORed together and driven out on the A20M# pin.

The A20M# output pin is shared with the TEST# input. At power up this pin is floated and remains that way until index register 09 bit 4 is written to a 1. This bit disables the test input and begins driving A20M#. Until the bit is set to 1, the external pull-up resistor keeps the pin high, prevents the 80435 from going into test mode, and holds A20M# high before the CPU is allowed to boot.

8042 KBRST# and GATEA20 Inputs—The 84031 optionally receives the KBRST# and GATEA20 inputs from the 8042. It generates a KBRST# code on the control link when KBRST# goes low, and generates GATEA20 codes each time GATEA20 performs a transition. The information is sent to the 84035 where the arbitration of the CPURESET signal is performed.

Emulated 8042 KBRST# and GATEA20—The CPU reset and GATEA20 functions are normally done by the 8042. The CPU issues I/O commands to the 8042 to manipulate these signals. The 84031 can be configured to monitor these signals and simulate the RESET and GATEA20 functions. Optionally, the commands can be blocked to the 8042 in order to speed up the operation.

The commands are written to the 8042 through address 64. The commands that affect GATEA20 and KBEST# are:

AA Self test. KBRST# and GATEA20 go high.

D1 Write output port. Next byte written to port 60 is the data. Bit 0 = KBRST#, bit 1 = GATEA20.

Fx Pulse output ports.

F0, F1, F4, F5, F8, F9, FC, and FD pushes GATEA20 high.

All even command codes cause KBRST#.

The Fx and D1 commands are optionally blocked from the 8042. The 84031 does this by not issuing an IOW#. F0, F1, F2, F4, F5, F6, F8, F9, FA, FC, FD, and FE commands are blocked. The D1 commands are a bit more complicated and follow these rules:

1. D1 commands are blocked.
2. Following a D1 command, the next write to port 60 is blocked. If another (non-D1) command occurs before port 60 is written, the next port 60 write is not blocked.
3. Following a blocked port 60 write, if the FF command (writing FF to port 64) occurs as the next write to the keyboard controller, it is blocked also. If multiple FF commands are issued, only the first one is blocked.

This will block all three writes in the typical sequence, which are as follows:

1. Write the D1 command to port 64.
2. Write the data to port 60.
3. Write the FF command to the keyboard controller to detect when it has finished updating GATEA20.

The GATEA20 and KBRST# pins of the 8042 may remain connected to the 84031 GATEA20 input pin when the GATEA20 and KBRST# functions are being emulated. They will be ignored when the function is emulated.

ADDRESS MAPPING

I/O Addressing

All I/O accesses go the ISA-bus *except* for cycles claimed by local bus slaves. All accesses to the 84031 or 84035 I/O ports are ISA-bus cycles. The only I/O decodes in the 84031 are for the configuration registers and internal I/O ports. The 84031 decodes all 16 bits of I/O address. The 84035 decodes A9:0. A15:10 are decoded as 0s in the 84031. The following I/O ports are decoded:

Configuration registers	22 and 23
8042 registers	60 and 64
Port B	61
NMI mask	70
Port 92h	92
XD bus I/O	0000-00FF

All internal I/O decodes are disabled when DGNT# is low and MASTER# is high, which indicates that the DMA controller has the bus.

Memory Addressing

Memory accesses may go to DRAMs, local bus slaves, or the ISA-bus (including the BIOS ROM). The slave priorities are as follows:

1. DRAM
2. Local Bus Slaves
3. ISA-bus.

Local bus slaves must not overlap local DRAM in the memory map or there will be a collision. Normally this can be avoided by the local slave. The DRAM controller takes off as soon as it determines that the address is programmed for it. This is generally in the middle of the first T2 cycle. The ISA-bus logic samples the DRAM decode and the LDEV# pin at either the end of the first or second T2 cycle (it is programmable). If either is low, or RDY# or BRDY# were returned, the ISA-bus state machine will ignore the cycle. If both were high and no ready was returned, the ISA cycle begins.

The DRAM decode consists of the 4 DRAM bank decodes and the shadow RAM registers. The shadow registers selectively disable the DRAM decode in the 640-1M address range. The 4 DRAM decodes are ORed together, and then ANDed with the disable signal of the shadow registers.

The DRAM bank decodes consist of a starting address and a length, which comes from the DRAM size and the interleave bit. The interleave bit doubles the size of the decode. It also forces the decode to show up in alternate DRAM pages, but the other pages will presumably be in another DRAM bank.

The shadow registers selectively disable DRAM in the 640-1M address range if it is present (there will always be memory present in this range for normal systems). The default for all bits is 0. 0 disables the memory in the specified range. The following ranges are individually controllable:

These address ranges have one bit which controls reads and writes together:

A0000-AFFFF	Video graphics area
B0000-BFFFF	Video text area

These address ranges have separate bits to control reads and writes:

C0000-C3FFF	Video BIOS
C4000-C7FFF	Video BIOS extension (usually used)
C8000-CBFFF	Other adapter BIOS (disk)
CC000-CFFFF	Other adapter BIOS
D0000-DFFFF	Miscellaneous (often EMS page frame)
E0000-EFFFF	System BIOS extension (rarely used) or EMS page frame
F0000-FFFFF	System BIOS.

The video graphics and text areas do not require write protection since the memory is either enabled or disabled (Note: It is almost always disabled). The C0000-FFFFF areas often contain ROMs, which may be shadowed, and when shadowed are generally write protected. It requires separate read and write controls. When a memory address falls into one of the above ranges, the appropriate shadow bit is compared. If the bit is 0, the DRAM decode is forced inactive. If the bit is 1, the DRAM decode from the bank decodes is allowed to pass through.

ROMCS#

In addition to the shadow bits, each of the ranges above C0000-FFFFF have a ROMCS# bit that enables the ROMCS# signal for those ranges. Motherboard BIOS ROM then becomes available at any or all of those ranges. ROM can only be accessed if the cycle reaches the ISA-bus. If a local slave or the DRAM controller takes the cycle, the ROM will be ignored. The ROMCS# may optionally be activated for write cycles in addition to read cycles in order to support FLASH ROMs. ROMCS will always be activated for the top 64K of the memory space (FFFF0000-FFFFFFFF) to provide the CPU reset vector. The ROMCS# and 8042CS# share a pin, which is the OR of the two decodes.

DRAM CONTROLLER

DRAM Configuration

Four banks of DRAM are supported at one time. Each DRAM bank has the following programming:

Bank size (256K, 1M, or 4M deep)
Programmable starting address (A26:20)
Interleave bit.

Each DRAM bank may have a different DRAM size. But two banks must have the same DRAM size for interleaving (see the interleaving section).

The starting address must be on a bank size boundary, which means that the largest banks are at the lowest address in order to achieve a linear memory map. The following table summarizes the starting address restrictions.

DRAM BANK STARTING ADDRESS

DRAM Depth	Interleave	Bank Size	Programmed Address Bits	Boundary Size Placement
256K	No	1M	A26:20	1M
	Yes	2M	A26:21	2M
1M	No	4M	A26:22	4M
	Yes	8M	A26:23	8M
4M	No	16M	A26:24	16M
	Yes	32M	A26:25	32M

The interleave bit doubles the decode size of a bank and causes it to appear in alternate DRAM pages only. Banks 0 and 2 will appear in the even numbered pages while banks 1 and 3 will appear in the odd numbered pages.

DRAM Controller Page Interleaving

The 84031 employs Page Mode, Page Interleaving, and Multi-RAS active techniques. These three different techniques may be used independently or together.

Page Mode—is always used in this chip set for CPU accesses, both for bursts and between bursts. Page mode simply means keeping RAS low while reading or writing multiple words within a DRAM page by providing only a new column address and toggling CAS.

Page Interleaving—involves interleaving DRAM banks on a DRAM page boundary. This gains the most advantage when used with multi-RAS active, but also has a performance gain with single RAS active since many cycles, which would be page miss cycles, are now RAS inactive cycles.

Multi-RAS Active—allows multiple banks of DRAMs to have pages open simultaneously thus allowing a page hit in any open page. When combined with page interleaving this allows faster cycles when the CPU is bouncing between several areas (code, data, and stack for instance) or when looping across a page boundary. Multi-RAS active is automatic where possible in the 84031. Two RASes may be active only if the two banks of DRAMs have separate CAS lines. When a page must be opened in a bank of DRAMs, the RAS of a currently active bank will only go high if the new bank shares CAS lines with it.

Page mode and Multi-RAS active are automatic. Page mode is always used for CPU and local master initiated cycles. Multi-RAS active is used where possible. Page interleaving is controlled by the DRAM configuration bits.

The CS4031 CHIPSet supports two way interleaving. Two banks may be interleaved if they are the same size and one is an even numbered bank (0 or 2) and the other is an odd numbered bank (1 or 3). Interleaving and noninterleaving may be mixed, and multiple sets of banks may be interleaved. See examples below:

Example 1:

Banks 0 and 1 have 256K deep parts and be interleaved with each other.

Bank 2 may have 1M parts, not interleaved with anything.

Bank 3 may have 4M parts, not interleaved with anything.

Example 2:

Banks 0 and 3 have 256K deep parts and are interleaved with each other.

Banks 1 and 2 have 1M parts and are interleaved with each other.

Example 3:

All 4 banks have 1M DRAMs installed. The interleaving could be done either of the following ways:

Banks 0 and 1 interleaved and Banks 2 and 3 interleaved.

Banks 0 and 3 interleaved and Banks 1 and 2 interleaved.

The following bank combinations may be interleaved:

0 and 1
2 and 3
0 and 3
1 and 2

The interleave scheme used in the CS4031 CHIPSet is designed to be very versatile for the user. When a block is interleaved, its block decode is doubled in size. The interleave bit (either A11 or A12) is included in the bank decode and decoded to either a 0 or a 1 depending on the bank number. This makes the bank show up in every other page (2K or 4K). The Page Interleaving Example figure shows what CPU address bits are used for the DRAM row address, column address, bank decode, and the interleave bit. It also shows the interleaving structure for 2 banks of 1M DRAM, for a total of 8M of DRAM.

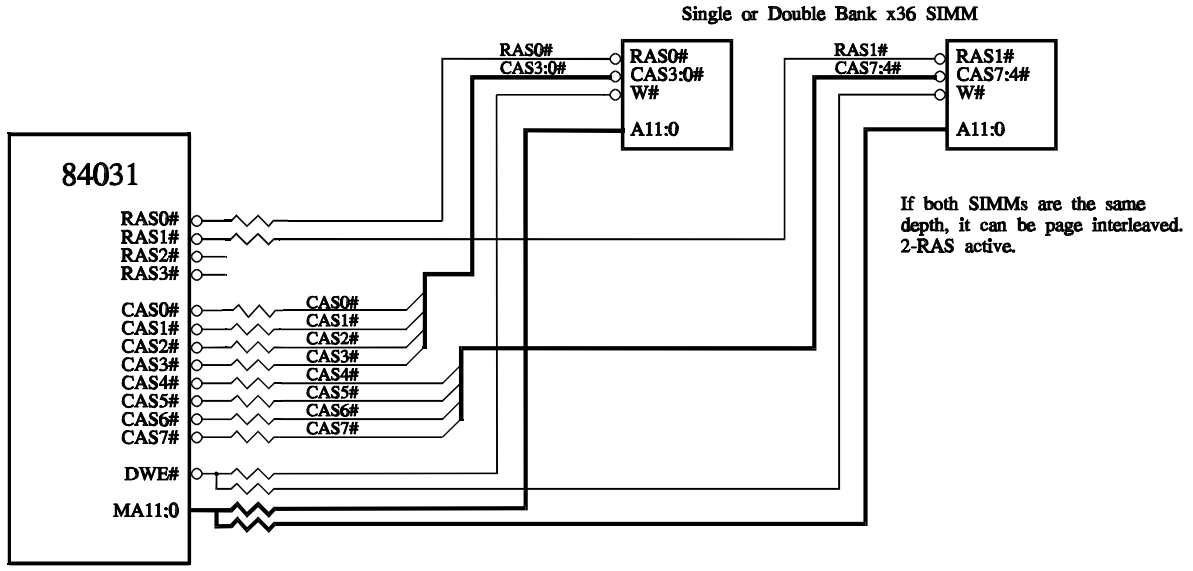
Memory Address		Bank 0	Bank 1	Memory Map
Page 0	000000-0007FF	Row 0		Bank 0, Row 0
Page 1	000800-000FFF		Row 0	Bank 1, Row 0
Page 2	001000-0017FF	Row 1		Bank 0, Row 1
Page 3	001800-001FFF		Row 1	Bank 1, Row 1
Page 4	002000-0027FF	Row 2		Bank 0, Row 2
Page 5	002800-002FFF		Row 2	Bank 1, Row 2
...		...		...
Page 0	07F000-07F7FF	Row 1023		Bank 0, Row 1023
Page 0	07F800-07FFFF		Row 1023	Bank 1, Row 1023

Page Interleaving Example

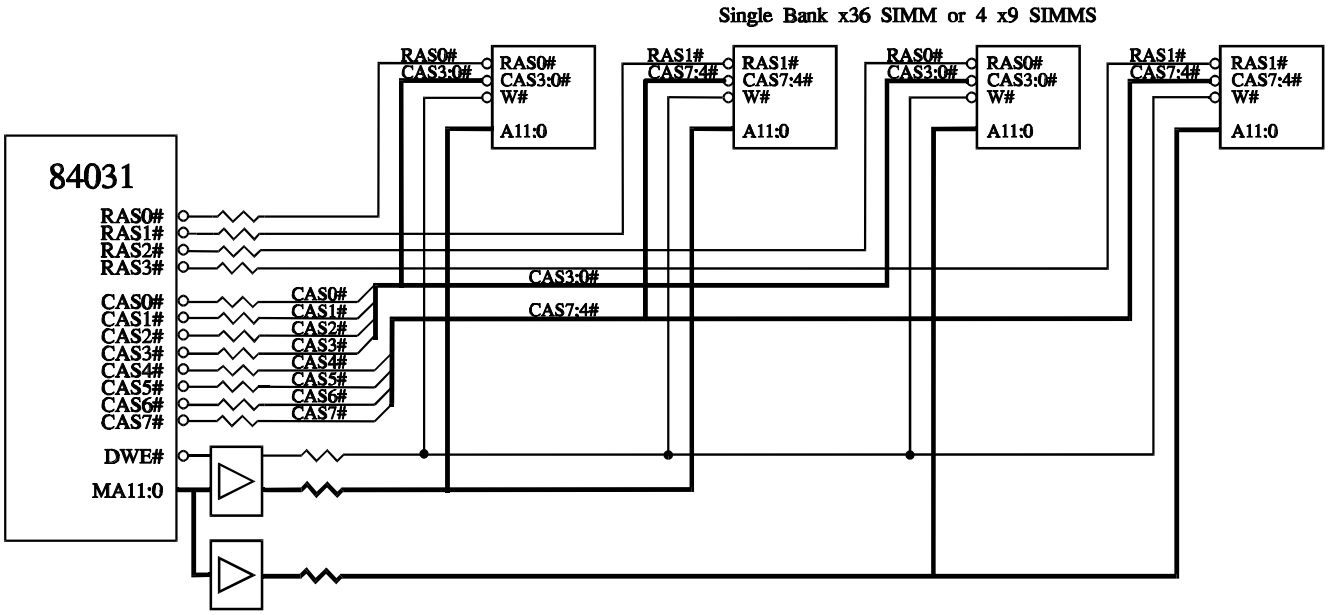
The algorithm below can be used to auto-configure interleaving:

```
if block 0 & 1 are the same size
     Program blocks 0 & 1 to the same
     address and set both interleave bits.
endif
if block 2 & 3 are the same size.
     Program blocks 2 & 3 to the same
     address and set both interleave bits.
endif
if blocks 0 & 3 are the same size and
neither have been interleaved above
     Program blocks 0 & 3 to the same
     address and set both interleave bits.
endif
if blocks 1 & 2 are the same size and
neither have been interleaved above
     Program blocks 1 & 2 to the same
     address and set both interleave bits.
endif
```

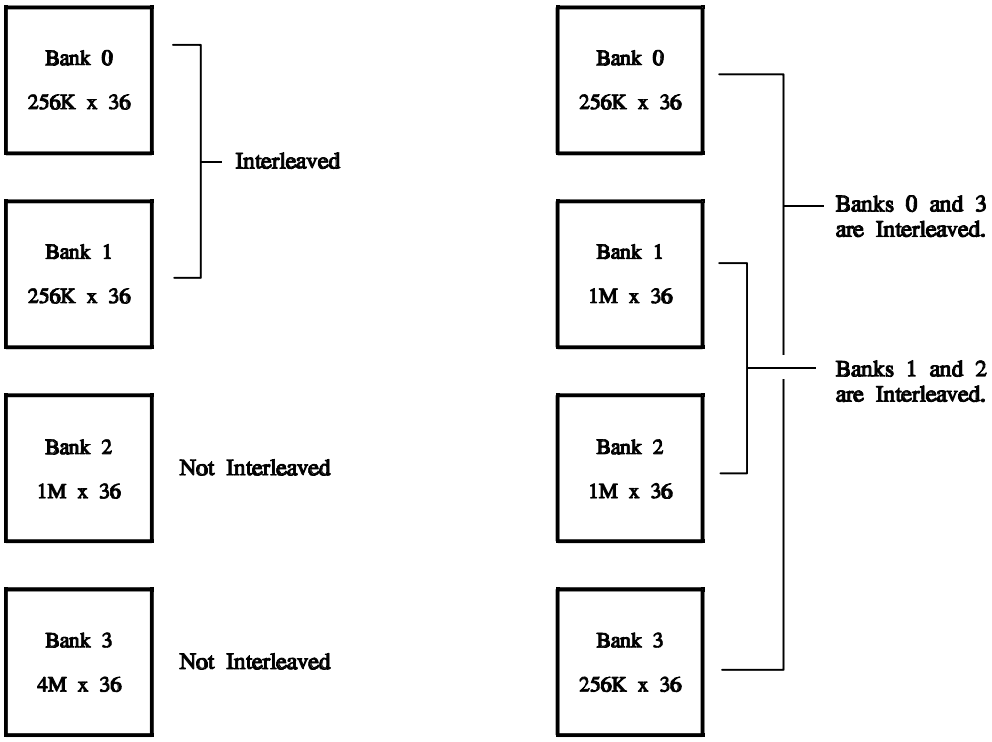
Two banks in different blocks may be interleaved by programming the starting addresses to be the same value and setting the interleave bit for both blocks. The DRAM depth must be the same size in order to avoid gaps in the memory map. It's required that one of the blocks be even numbered and one be odd numbered so that one will decode even pages (interleave bit decoded to 0) and the other will decode the odd pages (interleave bit decoded to 1). If both blocks were programmed as even numbered, the two banks will overlap each other as even pages and the odd pages will be left empty. If both blocks were programmed as odd numbered pages, the opposite is true.



DRAM Hookup Diagram—Two Bank Support



DRAM Hookup Diagram—Four Bank Support



DRAM Hookup Diagram—Interleave Examples

DRAM Memory Map

At power-up, the DRAMs are disabled and do not appear in the memory map. The BIOS will program the DRAM controller that will build the memory map. The DRAM memory map consists of the sum of the DRAM bank decodes with selectable areas between 640K and 1M removed. See Address Mapping section for further details.

DRAM Timing Modes

The local bus protocol is used by the DRAM controller for all accesses, including DMA and ISA master accesses. The 84031, ISA-bus logic treats the DRAM controller as a local bus slave, latching the data on read cycles when RDY# is received, and passing it on to the DMA device or ISA master.

The DRAM controller has configuration bits for the following:

- Read cycle timing mode
- Write cycle timing mode
- RAS-to-CAS delay for reads
- RAS-to-CAS delay for writes
- RAS precharge time
- Delayed start for reads
- Delayed start for writes.

In all cases there are two modes. All DRAM banks have the same timing.

The two modes for read cycles are 3-2-2-2 mode and 4-3-3-3 mode bursts for page hits. 3-2-2-2 is the standard mode, which works through 33MHz. (See the DRAM Timing Diagrams.)

The RAS-to-CAS timing for reads is either 1 or 2 T states. In both cases, the row-to-column switch is half way between RAS fall and CAS fall. The RAS to CAS delay should be set according the CPU speed and DRAM speed. Use the following table as a guide.

SUGGESTED RAS-TO-CAS DELAY FOR READ CYCLES

CPU Speed	60ns		70ns		80ns	
	3-2-2-2	4-3-3-3	3-2-2-2	4-3-3-3	3-2-2-2	4-3-3-3
16MHz	1	1	1	1	1	1
20MHz	1	1	1	1	1	1
25MHz	1	1	2	2	2	2
33MHz	2	2	2*	2	2*	2

*60ns DRAM recommended.

The two modes for write cycles are 0 wait state and 1 wait state writes. With 0 wait state writes, CAS# is pulled low in the middle of T2.

For 1 wait state writes CAS is pulled low at the end of the first T2. This allows adequate setup and hold times at all speeds. When a local bus master has the bus, 1 wait state writes are forced, since the 84031 must generate parity. The 1 wait state writes allow half a T state for the 84031 to do so.

The RAS-to-CAS timing for writes is either 1 or 2 T states. For 1 wait state writes, where CAS is pulled low at T state boundaries, there is actually a 1.5 or 2.5 T state delay. The RAS to CAS delay should be set according the CPU speed and DRAM speed. For example, at 33MHz/60ns DRAM or 25MHz/80ns DRAM, 1wait state writes and 2T RAS-CAS delays are the recommended settings.

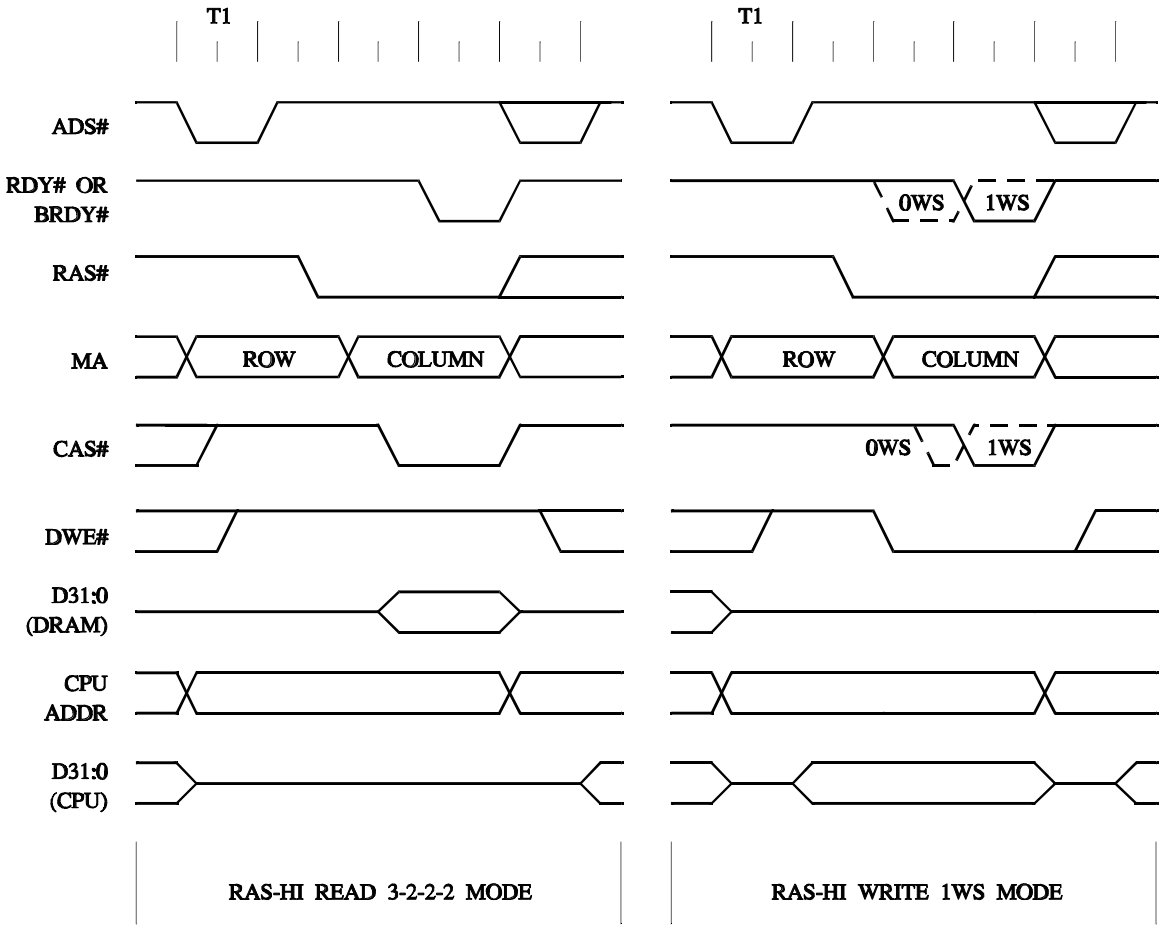
DRAM Timing Mode Recommendations

The recommended DRAM timing mode for a given CPU speed and DRAM access time is shown in the table below. These are based on a conservative worst case system timing analysis and may be more restrictive than necessary.

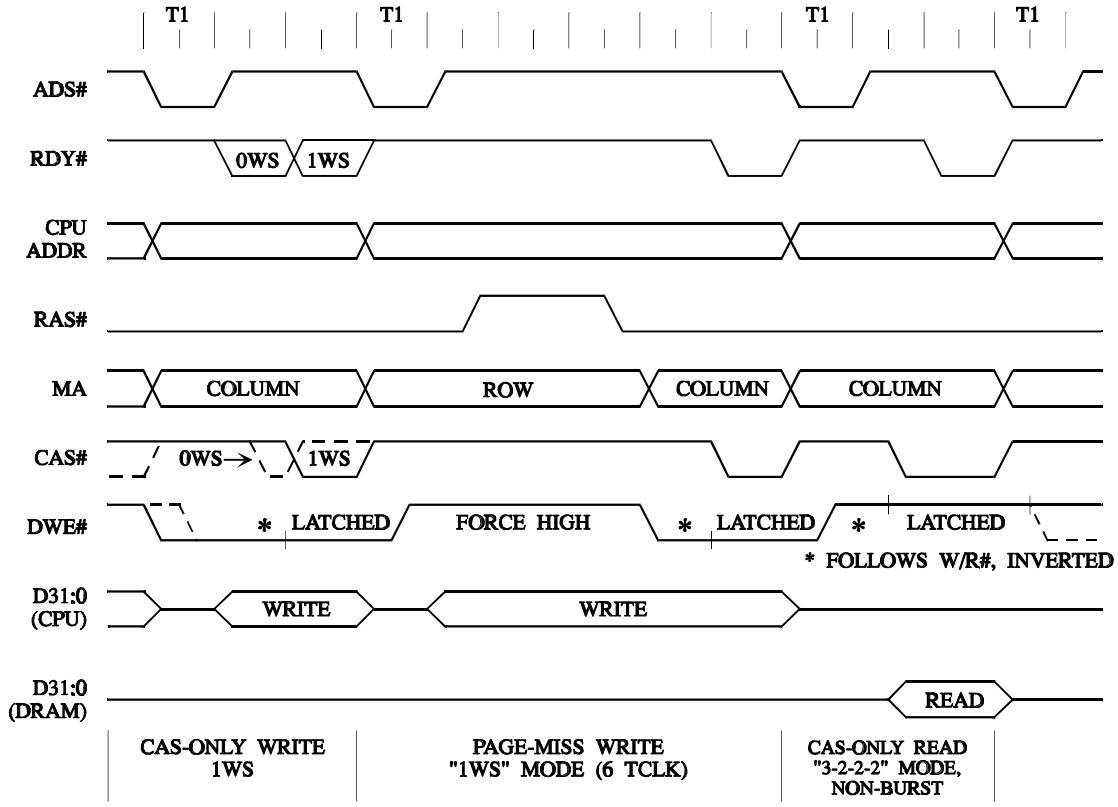
DRAM TIMING MODE

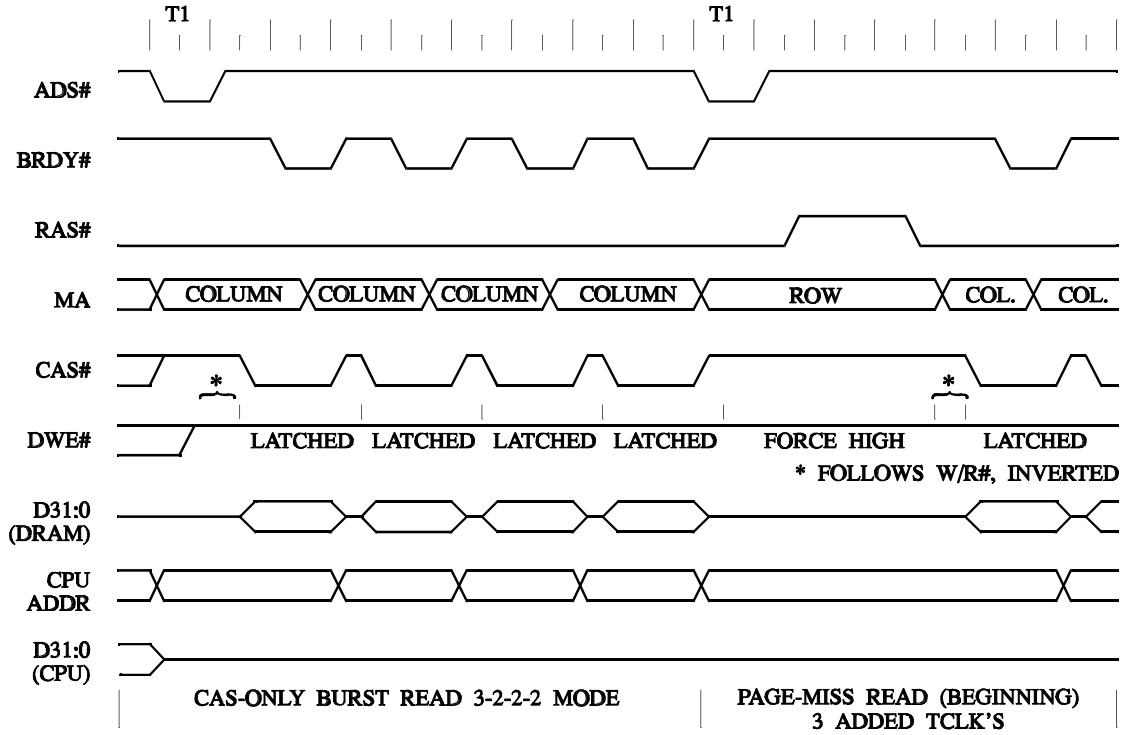
DRAM Timing Mode	Maximum Recommended CPU Speed and DRAM Access Time
3-2-2-2 Read/1T	25MHz @ 60ns, 20MHz @ 80ns
3-2-2-2 Read/2T	33MHz @ 60ns, 25MHz @ 80ns
4-3-3-3 Read/1T	25MHz @ 60ns, 20MHz @ 80ns
4-3-3-3 Read/2T	33MHz @ 80ns
0WS Write/1T	16MHz @ 70ns
0WS Write/2T	16MHz @ 70ns
1WS Write/1T	25MHz @ 60ns, 20MHz @ 80ns
1WS Write/2T	33MHz @ 70ns, 25MHz @ 80ns
2T RAS Precharge	33MHz @ 60ns, 25MHz @ 80ns
3T RAS Precharge	33MHz @ 80ns

/*n*T Denotes RAS-CAS delay.



DRAM Timing Diagram





DRAM Timing Diagrams (continued)

DRAM Address Multiplexing

The DRAM address line multiplexing is shown in the table below. The column address is the same for all configurations. The row address will change depending on the DRAM size and the interleaving.

ADDRESS MULTIPLEXING

MA	Column Address (All Size)	Row Address Choices	Row Address Assignment for:			
			256K		1M or 4M	
			non-	intrlve	non-	intrlve
0	2	11 or 20	11	20	20	20
1	3	12 or 20	12	12	12	21
2	4	13	13	13	13	13
3	5	14	14	14	14	14
4	6	15	15	15	15	15
5	7	16	16	16	16	16
6	8	17	17	17	17	17
7	9	18	18	18	18	18
8	10	19	19	19	19	19
9	11	20, 21, or 22	20	20	21	22
10	23	22 or 24	x	x	22	24
11	—	23	—	—	23	23
Interleave bit:			—	11	—	12
Page Size:			2K	2K	4K	4K

A11 is a special case for 4M x 4 DRAMs, some of which will have 12 row addresses and 10 column addresses. A23, which is provided on column address 10 is repeated on row address 11. This allows 11/11 and 12/10 addressing chips to be used transparently, and even be mixed.

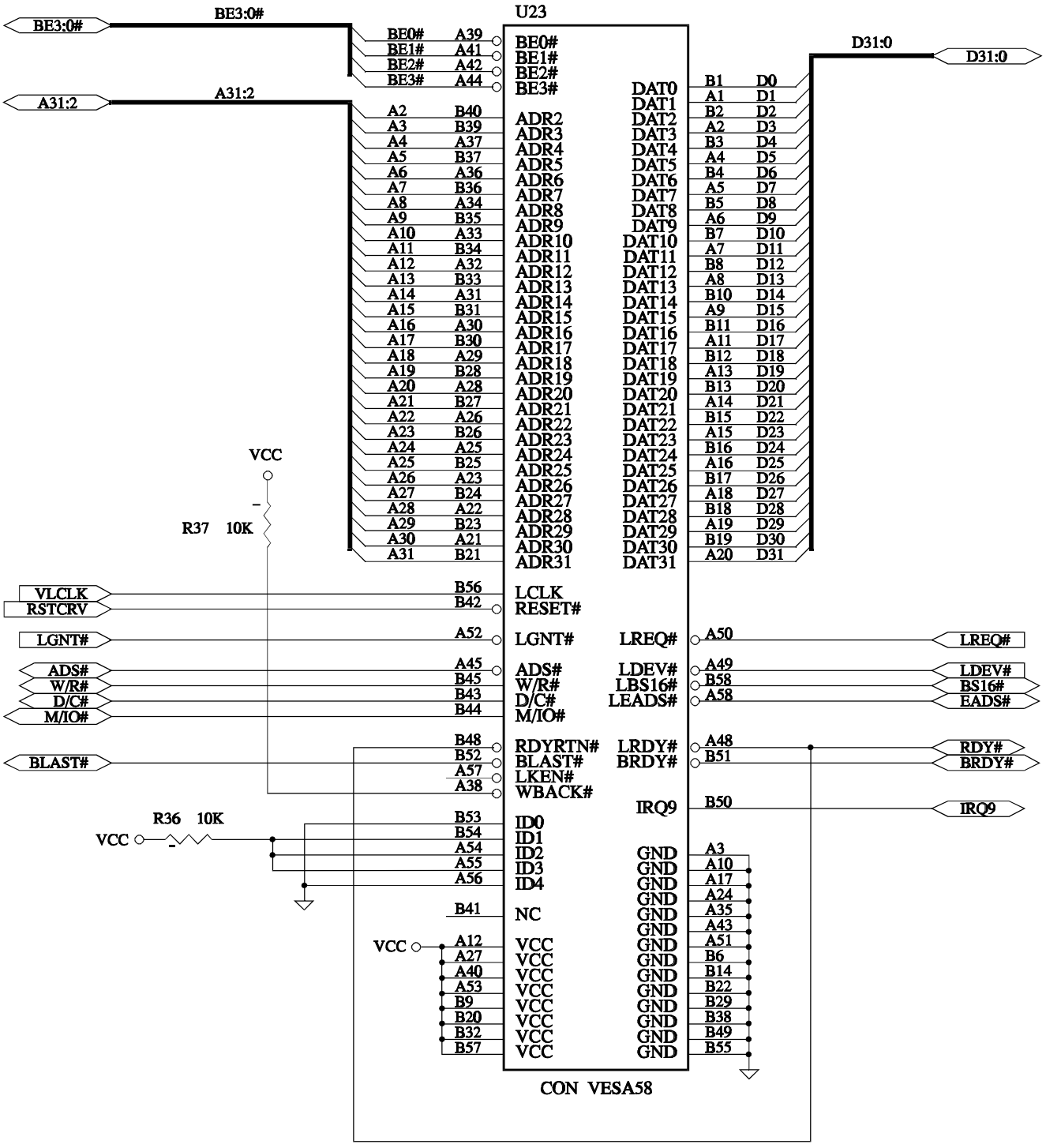
Local Bus Support

The 84031 fully supports the VL-Bus (VESA Local Bus) for both slaves and masters. Local bus peripherals provide a much higher throughput for devices such as video, mass storage, and LAN. (See the VL-Bus Block Diagrams.)

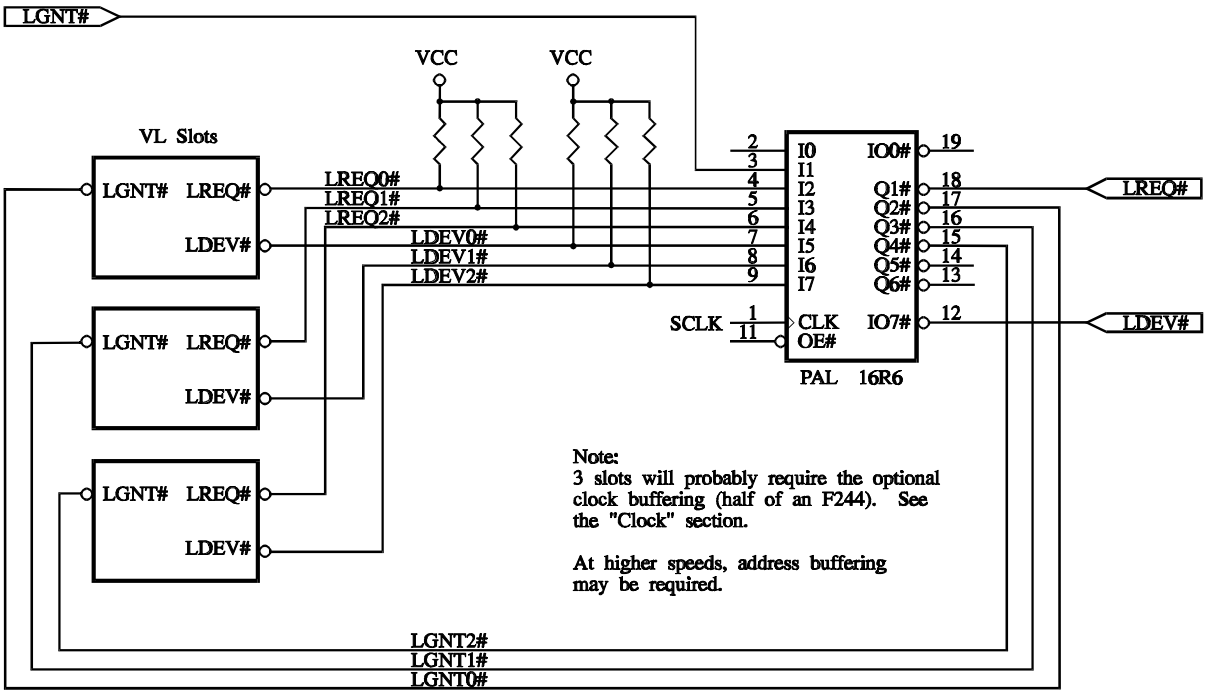
The VL-Bus standard is from the Video Electronics Standards Association (VESA). It specifies a standard interface, including a connector, for local bus slaves and masters. Adapter cards are expected for video, disk, and LAN interfaces, as well as other applications.

The following local bus support is provided:

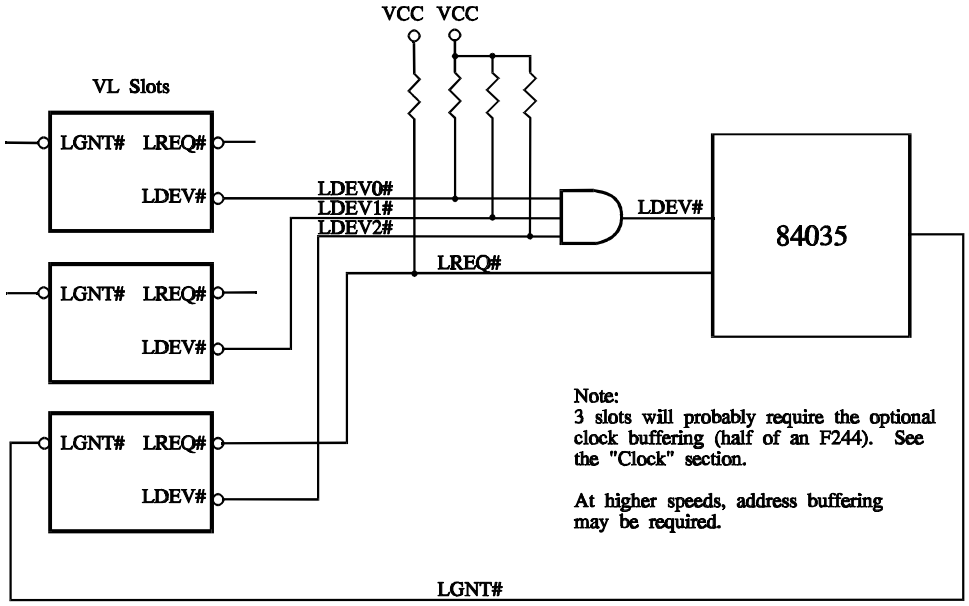
- A single VL-Bus slot is supported with *no additional external logic.* Some additional logic is required for multiple slots to OR the LDEV# signals and provide additional LREQ# and LGNT# pairs.
- A clocking scheme which provides a 1x clock with little or no skew to the local bus device is used. The VL-Bus requires this 1x clock. A 2x clock with little or no skew is also available on the motherboard for non-VL peripherals which may require it. For a single slot the clock directly from the 84031 may be used. For multiple slots, the clocks from the 84031 should be buffered before being used. In this case the buffered clocks are used at all places to avoid clock skew.
- Support for the LDEV# signal allows a local bus slave to claim a bus cycle. For timing reasons each VL-Bus slot provides a totem pole output on LDEV#, which are ORed together with an F11 (for 3 slots) and sent to the LDEV# pin. For a single slot no gating is necessary. The 84031 will sample LDEV# at the end of either the first or second T2 of each bus cycle, as specified by a configuration register. If it is low at the sample point, the cycle will not go to the ISA-bus. Note that the LDEV# signal will not take the cycle away from the DRAM controller unless the "delayed start" bits are set. Delayed start reduces DRAM performance. It will rarely be required.
- Generating local bus control signals for DMA and ISA Master cycles. During DMA and ISA master cycles, the LDEV# signal as well as the internal local bus decodes are checked to see if the addressed device is on the CPU local bus. If it is, an ADS# is generated to read or write the local bus device. The data is passed through the 84031 and/or through the 245s to or from the ISA-bus. IOCHRDY is pulled low by the 84031 until the local bus slave completes the cycle. On reads from the local bus, the data is latched in the chip when the slave generates RDY# and held there until the DMA controller or ISA master takes the command signal high.
- Support for local bus masters. The 84035 provides the LREQ# and LGNT# signals for the local masters. The 84031 handles the bus cycles. These cycles are handled the same as 486-initiated cycles with the following exceptions:
  - Parity is generated for DRAM writes (the 486 supplies the parity when it has the bus).
  - Writes are forced to the 1 wait state mode due to the delay in generating parity.
  - The DRAM controller returns RDY# for all accesses since local bus masters may not accept BRDY#.



VL-Bus Block Diagram—One Slot



VL-Bus Block Diagram—Multiple Slots With Multiple Masters



VL-Bus Block Diagram—Multiple Slots With Single Master

ISA-BUS

CPU and Local Master Accesses to the ISA-bus

Bus cycles which are not claimed by a local slave or the DRAM controller go to the ISA-bus.

The ISA-bus runs off of a clock which is derived from CLK2. It should normally be set at about 8MHz, but may be set faster if all of the peripherals can handle the faster cycles. See the Clock section for programming the ISA-bus clock rate.

DMA and ISA Master Accesses to Local Slaves and DRAM

When DGNT# goes active (for DMA or ISA master cycles) the 84031 becomes an ISA-bus slave by floating the ISA commands, and a local bus master by driving the local bus control signals. When a DMA or ISA master cycle attempts to access a device on the local bus, the 84031 performs the control signal translation and data steering for the cycle. Local slaves and DRAM are handled identically. The following is the basic sequence.

For default states:

When DGNT# goes low, the 84031 floats the ISA-bus commands and drives the local bus control signals. The default values are:

W/R# = 1
D/C# = 1
M/IO# = 1
BLAST# = 0

D/C# and BLAST# will remain at their default values the entire time. W/R# and M/IO# will be changed according to the ISA-bus commands, but will return to the default values between cycles. During DMA cycles (DGNT# low and MASTER# high) M/IO# will always be high. The DMA I/O device will never be on the local bus.

The default direction for the data bus drivers is the "writing" direction, and they are turned around when an ISA read command is received. SDEN is driven according to XA1.

For address decoding:

The address from the DMA controller or ISA master is decoded asynchronously by the local slaves and DRAM controller. Local slaves drive LDEV# with the decode result while the DRAM controller provides the decode internally to the 84031. The 84031 drives MEMCS16# low asynchronously if either decode is active. Since MEMCS16# is an open collector signal, the 84031 floats it when neither decode is active. IOCS16# is not driven. The 84031 also drives BE3:0# from SBHE#, XA0, and XA1 asynchronously.

No further action is taken on this decode until an ISA command goes active, because it is not known whether the address is for I/O, memory, or whether it is valid at all.

For ISA command going active:

If a memory command goes active, the decodes from the local slaves and DRAM controller may be checked immediately to determine if the cycle is for the local bus or not. If both decodes are inactive the cycle is ignored, except to provide the proper data bus steering, when necessary. If either is active, IOCHRDY is pulled low and a local bus cycle is initiated.

If an I/O command goes active, M/IO# must be pulled low to allow the local bus slave to switch from doing a memory decode to an I/O decode. The DRAM decode will go inactive when M/IO goes low. After driving M/IO# low, the 84031 waits 2 T states to sample the decode. If it is low, IOCHRDY is pulled low immediately with the command, and a local bus cycle is initiated.

For read cycles the data bus buffers are turned around as soon as the command is received. During DMA, the memory commands are used for data bus steering.

For local bus cycle:

To initiate the local bus cycle, W/R# goes low if an ISA read command goes active, or remains high if an ISA write command goes active. For DMA cycles, the I/O commands are ignored. ADS# is then generated for one T state.

For write cycles, data is being driven through the 84031 and the 245s. When the local bus slave or DRAM controller returns RDY, IOCHRDY is floated and the DMA controller or ISA master will complete the cycle.

Read cycles are more complicated. The local bus slave or DRAMs will float the data as soon as it returns RDY#. The DMA device or ISA master will not read the data until much later. The 84031 latches the local bus data on the clock edge where RDY# is received, then redrives the data onto the local bus for bytes 1 and 3 and drives the appropriate data on the XD bus. IOCHRDY is floated when RDY# is received. The 84031 holds the data until the ISA command goes back high.

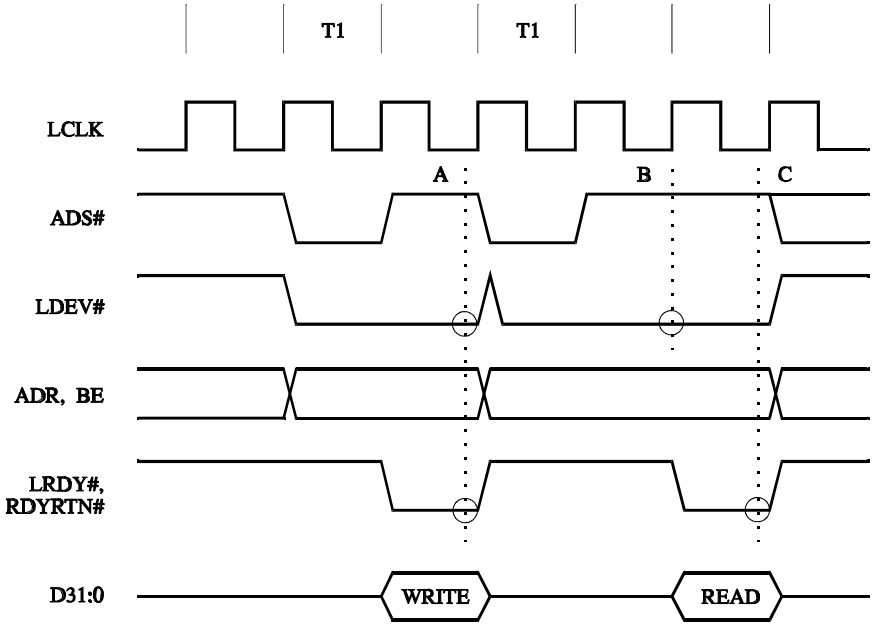
BUS CYCLE DESCRIPTIONS

CPU/LBM Read and Write to Local Bus Target

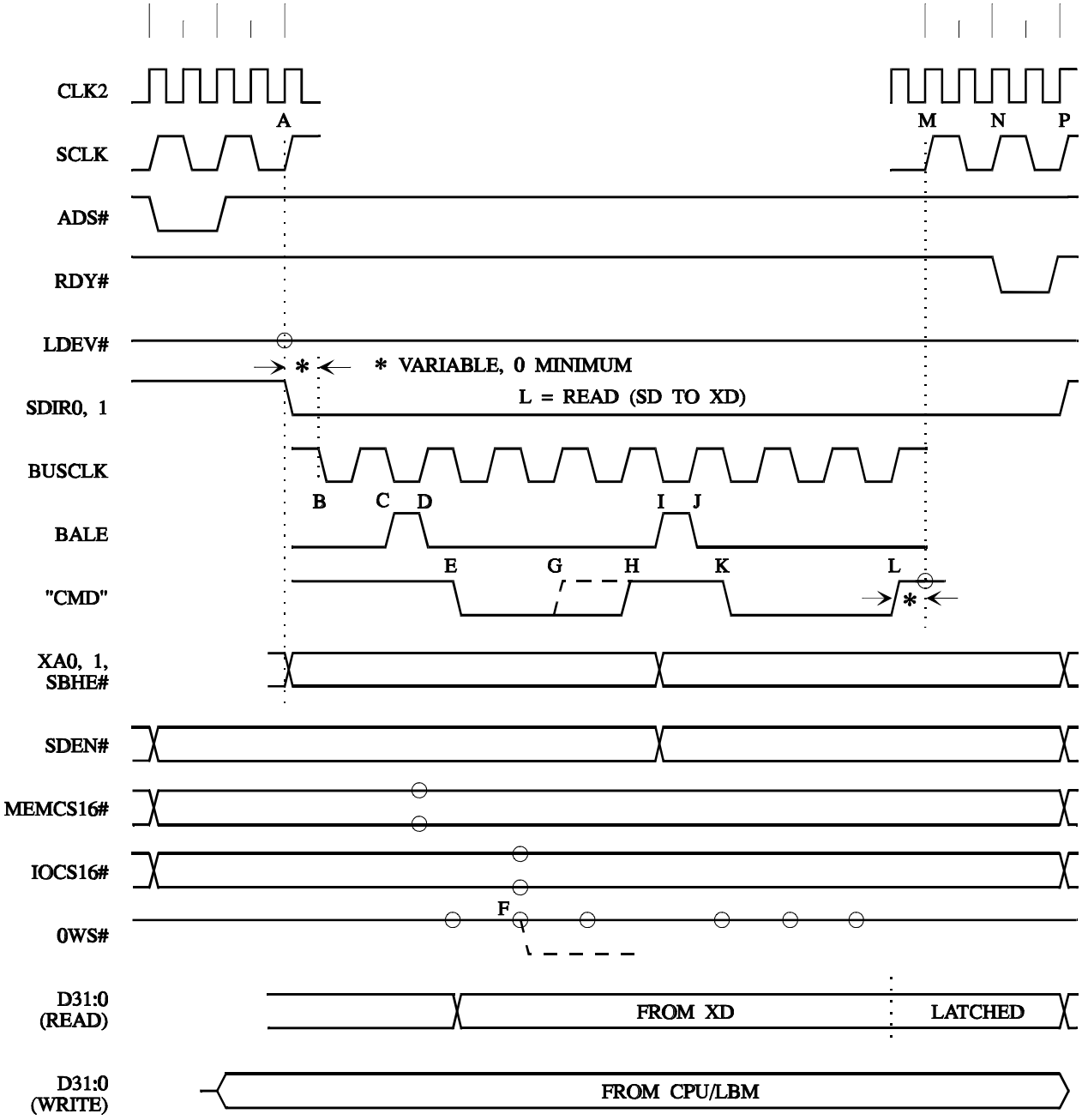
The CPU or a Local Bus Master can access a Local Bus Target. The figure below shows a write followed by a read cycle. The cycle is claimed by the local bus target. The 84031 will sample the LDEV# signal at points A and B on the diagram. The sampling point can be changed to point C, if the index register 18h is programmed. The diagram shows a 0 wait state write, the LBT asserts LRDY# during the same T2 state (point A) in which LDEV# is sampled by the 84031. Any number of T states can occur before the LRDY# signal is asserted.

CPU/LBM Access to the ISA-Bus

The CPU or a Local Bus Master can access the ISA-bus. The next figure shows a typical access cycle, with the sampling points for some of the signals. The 84031 will sample LDEV# at point A, and it must be high for a valid ISA-bus cycle. Point A to B is a variable synchronization time. The 84031 must synchronize with the BUSCLK at the beginning and the end of the ISA cycle. This time is a minimum of 0 CLK2 cycles.



CPU/LBM Read and Write to LBT Timing Diagram



CPU/LBM Access to ISA-Bus Timing Diagram

The CMD refers to any ISA command signal, IOR#, IOW#, MEMR#, MEMW#, SMEMR#, and SMEMW#. The timing for the CMD signal is programmable by using index 05h and 06h. The command delay shown as point D to E is programmable. The CMD pulse width shown as point E to H is also programmable.

MEMCS16# is sampled at point D at the BUSCLK rising edge.

IOCS16# is latched at the end of one full BUSCLK after the CMD falling edge. This is shown in the diagram as point F. In this case the CMD falling edge is on BUSCLK falling; so the IOCS16 latch point is also a BUSCLK falling edge. If the CMD falling edge was on a BUSCLK rising edge, the IOCS16# latch point would also be at the BUSCLK rising edge.

0WS# is sampled on each falling edge of BUSCLK. If sampled low, the command ends 0.5 BUSCLKs later. The exception would be if IOCHRDY is also pulled low at the same time as 0WS#; in this case the 0WS# is ignored. The diagram shows a normal cycle that terminates the CMD at point H. If 0WS# is pulled low the CMD is terminated at point G.

The diagram shows an 8-bit cycle with a bus conversion cycle. The delay from the end of the first cycle to the beginning of the next cycle is fixed at 0.5 BUSCLK, this is shown as point H to I.

The cycle terminates with the RDY# signal. The minimum delay from final command, point L, to the falling edge of RDY#, point N, is one SCLK cycle. The resynchronization time point L to M is variable, with a minimum of 0 SCLK cycles, so the maximum delay could be longer than 1 SCLK from L to N.

SDIR0 and SDIR1 defaults to a high state; this directs data from XD bus to SD bus. The SDIR transition is synchronized to CLK2, and will only be in a low state when data must be driven from SD to XD bus.

ROMCS# follows the local bus address timing from CPU and LBM. To access the ROM or flash memory, the ROMCS# must be gated with the command (MEMR# or MEMW#). The same ROMCS# is used to enable accesses to the keyboard controller by gating with the command (IOR# or IOW#).

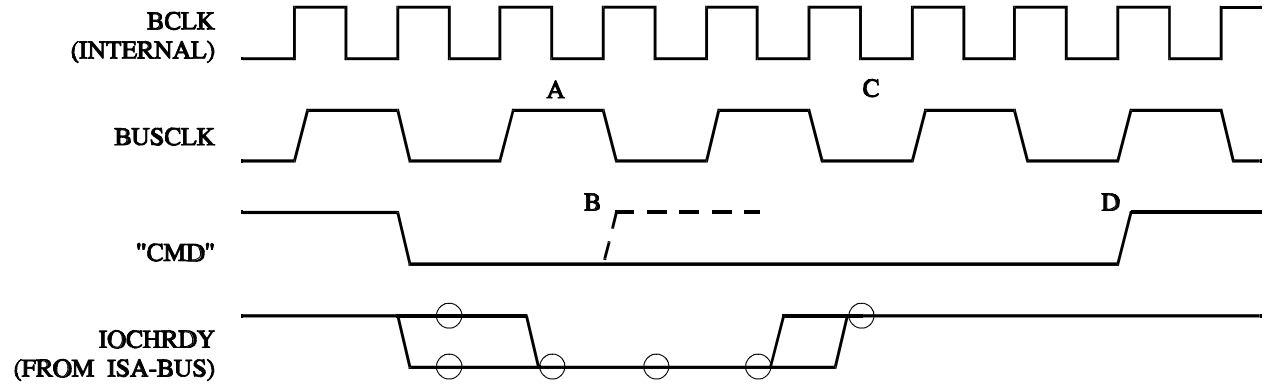
Interrupt acknowledge cycle follows the 8-bit ISA bus I/O read timing. Except that no ISA CMD is generated externally, and the target is the 84035 on the XD bus. The same programmable options apply to the timing of the cycle.

IOCHRDY Operation

The timing diagrams shown in the following two figures, IOCHRDY Effect and DMA and ISA Master Memory Access, shows when the CS4031 CHIPSet samples the IOCHRDY signal.

DMA and ISA Master Memory Access to a Local Bus Target

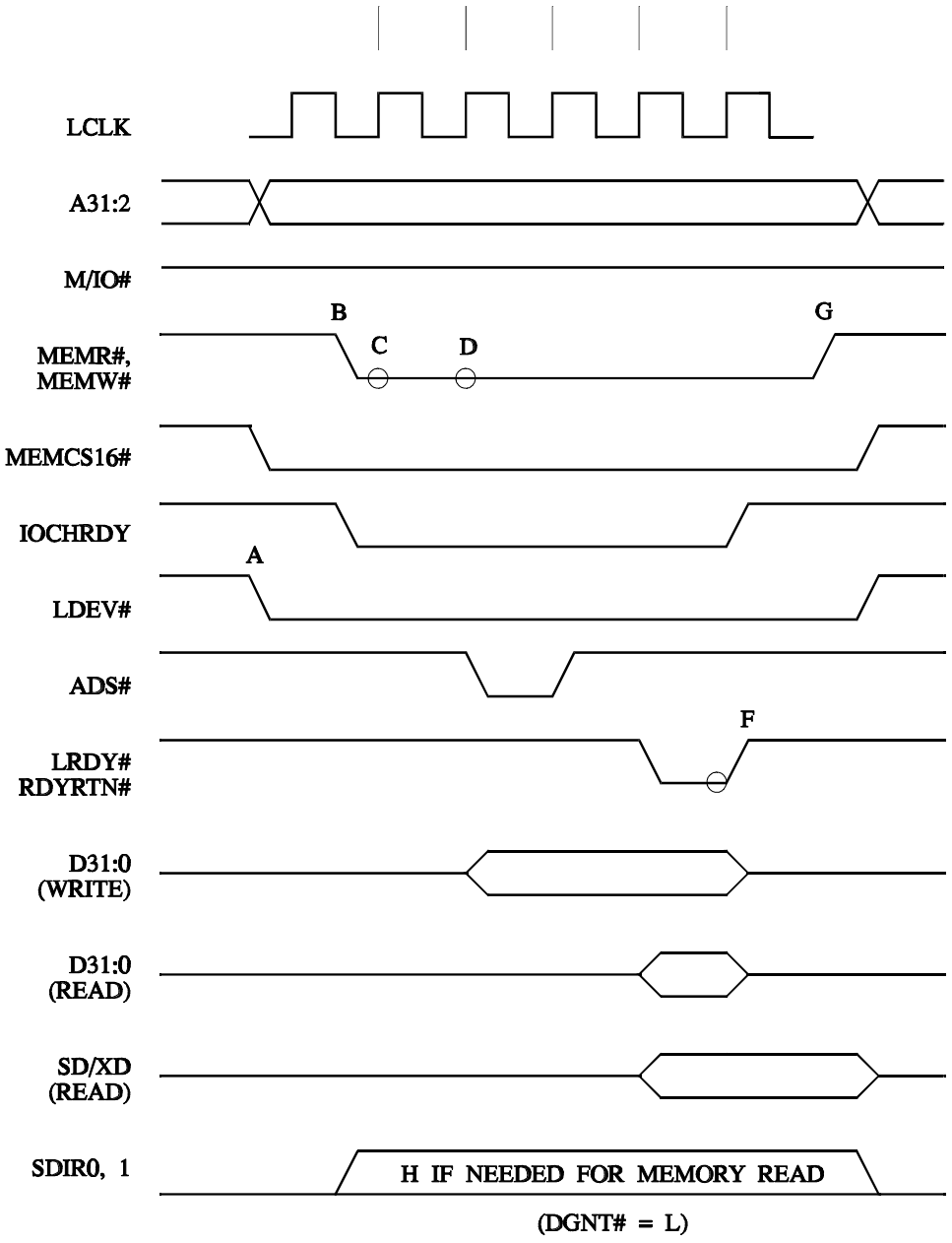
The DMA and ISA Master Memory Local Bus Target Timing Diagram shows the timing for a typical access to a local bus target (LBT) by a ISA Master or DMA device. The LBT will assert LDEV# as a decode of local address and M/IO# at point A. MEMCS16# is asserted in response to the LDEV# signal and the 84031 will drive out the local bus status to indicate a memory data write. The 84031 detects the command fall at point B and pulls IOCHRDY low. The 84031 samples the command at point C and D using SCLK, and generates the local bus cycle starting with the output of ADS# low at point D and terminates the local



IOCHRDY Effect Timing Diagram (CPU/LBM Access to ISA-Bus)

bus cycle when the LBT returns a LRDY# low which is sampled at point F. The 84031 will release IOCHRDY at point F and the DMA or Master device will release the command after the IOCHRDY has gone high. If the cycle is a read cycle, the 84031 will maintain valid latched data on the SD and XD busses until the end of the command—at point G.

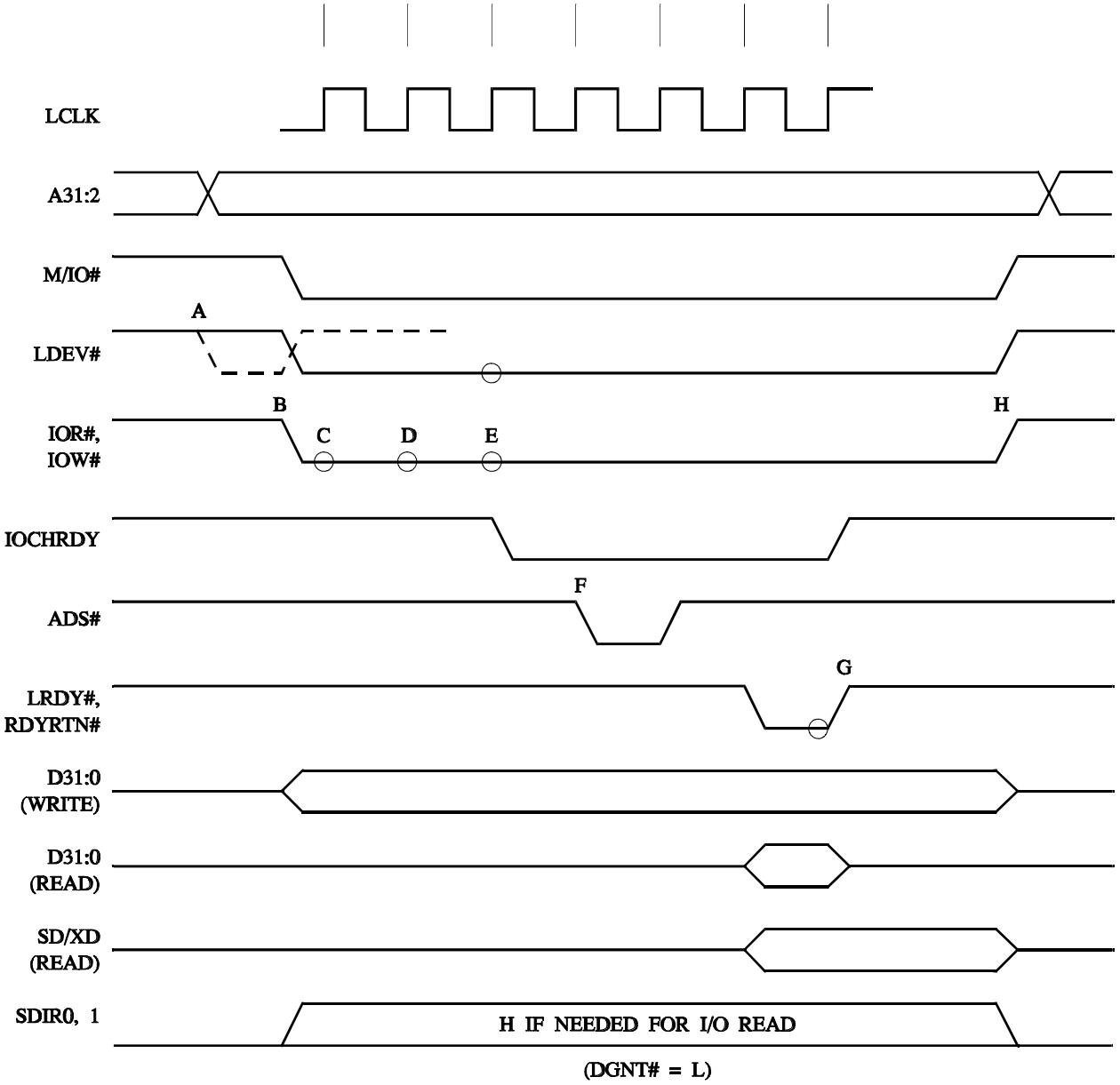
For the DMA or ISA Master to access local DRAM the same sequence is followed up to point D. Between points D and F the local DRAM cycle will occur. The cycle is dependent on the DRAM controller.



DMA and ISA Master Memory Local Bus Target Timing Diagram

ISA Master I/O Access to a Local Bus Target

The diagram below shows an ISA Master I/O access to a Local Bus Target (LBT). The sequence is similar to that of an access to a LBT memory, with some exceptions. A memory device may assert the LDEV# signal at point A. If the cycle generates an I/O command at point B, the 84031 will pull M/IO# low causing the memory device to raise LDEV# and the 84031 will deassert the MEMCS16 signal. The 84031 will synchronize for two full LCLK cycles, points C to E, and then at E pull IOCHRDY low. After one LCLK cycle, at point F the 84031 will generate the ADS# to start the local bus I/O cycle. The cycle terminates when LRDY# is sampled low at point G and the 84031 will release IOCHRDY. The ISA Master will release the I/O command at point H.



ISA Master I/O Access to LBT

PORT B AND NMI LOGIC

Port B is the I/O port at address 0061. It controls miscellaneous things such as parity, the speaker, etc. Bits 3:0 are read/write and control these functions. Bits 7:4 are read only and provide status information. These bits are split between the 84031 and 84035 as shown in the table below:

PORT B BITS

Bit	R/W, R	Chip	Function
0	R/W	84035	Timer gate 2 (speaker timer enable)
1	R/W	84035	Speaker data
2	R/W	84031	Enable parity check (0 = enabled)
3	R/W	84031	Enable IOCHCK (0 = enabled)
4	R	84035	Refresh detect (toggles on each refresh)
5	R	84035	Timer 2 out (monitor the speaker timer).
6	R	84031	Channel check latch (status of IOCHCK)
7	R	84031	Parity check latch (parity error status).

The 84035 latches bits 3:0 on write cycles. On read cycles it drives bits 5:0 on the XD bus, and drives 0s on bits 6 and 7. The 84031 latches bits 2 and 3 on writes. For read cycles, since the XD data passes through the chip, it receives the XD bus, uses bits 1:0 and 5:4 from the 84035, and replaces bits 3:2 and 7:6 with its internal data before sending it to the CPU.

DATA BUS BUFFERS

The data bus buffer external logic consists of three F245s, one for SD7:0, and two for SD15:8. These are controlled by SDIR0, SDIR1, and SDEN# signals. These signals are generated as follows:

For the SDIR0 signal:

The default when CPU and local masters have the bus (DGNT high) is high, which drives data from XD to SD. It turns around (goes low) at the following times:

- Read cycles from the ISA bus, but *not* XD reads (ROM, 8042, 84035, and internal 84031 I/O). It does *not* go low for interrupt acknowledge cycles.

The read command timing is used to take it low.

The default direction for DMA or ISA master cycles (DGNT# low) is low, which drives data from SD to XD. It turns around (goes high) at the following times:

- DMA reads from DRAM or local bus slaves.
- ISA master reads from DRAM, local bus slaves, or XD bus peripherals.
- 8-bit DMA reads from odd byte of 16-bit memory slaves.
- ISA master writes to odd byte of 8-bit ISA slaves.

For the SDIR1 signal:

The default when CPU and local masters have the bus (DGNT# high) is high, which drives data from D to SD. It turns around (goes low) at the following times:

- Read cycles from the ISA bus, but *not* XD reads (ROM, 8042, 84035, internal 84031 I/O). It does *not* go low for interrupt acknowledge cycles.

SDIR1 must go high with the command to allow the D buffers to turn on at the end of the cycle to give the data to the CPU.

The default direction for DMA or ISA master cycles (DGNT# low) is low, which drives data from SD to D. It turns around (goes high) at the following times:

- DMA reads from DRAM or local bus slaves.
- ISA master reads from DRAM, local bus slaves, or XD bus peripherals.
- 8-bit DMA writes to odd byte of 16-bit memory slaves.
- ISA master reads from odd byte of 8-bit ISA slaves.

For the SDEN# signal:

SDEN# determines which 245 is enabled. A 0 enables the D15:8 to SD15:8 buffer while a 1 enables the D31:24 to SD15:8 buffer. This is mostly determined by XA1. The exception to this is the following two cases, where it is always low. This is for the high speed byte swap.

- 8-bit DMA write cycles.
- ISA bus master reads from the ISA bus (not a local slave or DRAM).

CONTROL LINK

The control link is a mechanism to pass information between the 84031 and 84035 using a minimum number of pins. Both chips have an LIN and an LOUT pin. The LOUT of one chip is connected to the LIN of the other.

When PWRGOOD is low, the 84035 LOUT pin is at a high impedence state and the 84031 LIN pin is the test mode enable input. An external pull-up resistor is required on the 84031 LIN pin to prevent 84031 from entering the test mode during reset.

Control Link From the 84035 to the 84031

The following information must be sent from the 84035 to the 84031:

Refresh Request	Occurs only when DGNT# is high (CPU or local master has bus).
Refresh End	Same as above.
DMA address Strobe	Occurs only when DGNT# is low and MASTER# is high (DMA cycle).
Master refresh	Occurs only when MASTER# is low (ISA master has the bus).

Control Link From the 84031 to the 84035

Several pieces of information must be sent from the 84031 to the 84035 for things to occur simultaneously. These are as follows:

Hidden Refresh Acknowledge	Occurs only when DGNT# is high.
GATEA20 = 0	Could happen at any time.
GATEA20 = 1	Could happen at any time.
Interrupt Acknowledge	Occurs only when DGNT# is high.
Soft Reset Request	Could happen at any time.

These events are communicated as 3-bit codes sent serially from 84031 to 84035. Each code is preceded by a start bit. One or more stop bits occur between successive codes. One bit is sent during each SCLK cycle.

TEST MODES FOR THE 84031 AND 84035

There are several test modes to help in the testability of systems using the 84031. Both parts have a connectivity test mode that is initiated by the following steps:

1. Start with PWRGOOD low and initialize the chip set by raising PWRGOOD and keeping it high.
2. The test mode is entered by pulsing the A20M#/TEST# pin on the 84035.
3. While the TEST# pin is low the test mode code must be presented on the XD7:0 pins. This data is latched in on the rising edge of the TEST signal. Test Mode Code = FEh
4. In this mode the pins of the 84035 are internally chained together by a series of AND gates. To test a pin for a good solder connection, pull all pins to a high state. The output of the AND chain is the SPKR pin. This pin will be in a high state. Pulse each pin low one at a time and the SPKR pin should also be changed to a low state, if there is continuity. There are some pins that are not included in the chain and cannot be tested in this way. They are as follows:

   14MX1
   14MX2
   SPKR
   A20M#/TEST#
   PWRGOOD
   32KX1
   32KX2

5. The test mode can be exited by two methods.
   - Pulse PWRGOOD to reset the system.
   - Enter the Terminate Test Mode Code on XD7:0 and pulse the TEST pin.

     Terminate Test Mode Code = 00h

The 84031 has several test modes. There is a solderability test similar to that for the 84035 and there is a high impedence mode where the output pins are put in a high impedence state.

1. Start with PWRGOOD low and initialize the chip set by raising PWRGOOD and keeping it high.
2. The test mode is entered by pulsing the LIN pin on the 84031.
3. While the LIN pin is low the test mode code must be presented on the XD7:0 pins. This data is latched in on the rising edge of the LIN signal.

   Test Mode Code = 02h
4. In this mode the pins of the 84031 are internally chained together by a series of AND gates. To test a pin for a good solder connection, pull all pins to a high state. The output of the AND chain is the ROMCS pin. This pin will be in a high state. Pulse each pin low one at a time and the ROMCS pin should also be changed to a low state, if there is continuity. There are some pins that are not included in the chain and cannot be tested in this way. They are as follows:

   SYSRESET
   LIN
5. The test mode can be exited by two methods.
   - Pulse PWRGOOD to reset the system.
   - Enter the Terminate Test Mode Code on XD7:0 and pulse the LIN pin.

     Terminate Test Mode Code = 00h

In order to have the output pins of the 84031 in a high impedence state the same procedure should be followed, using the test code 01h on XD7:0 during the rising edge of the LIN pin.

84035 Functional Descriptions

The 84035 is an 82C206 with additional logic added to reduce signal and chip count of the external logic. The following features are added to the '206 to create the 84035:

- 14MHz crystal circuit and divider.
- DMA clock divider from SCLK.
- System reset logic.
- System arbitration logic, including support for local bus masters.
- ISA-bus hidden refresh logic.
- Performance control logic to emulate an 8MHz AT-compatible.
- DMA controller address generation logic.
- A20M# generation.
- 486 floating-point error logic.
- Speaker logic.
- Control link logic to communicate with the chip set.

The 84035 is suitable for use in 80386 systems (non-84031) as well as 80486 systems.

CLOCKS

There are three clock frequencies used in the 84035:

- 14.31818MHz for the timer chip.
- SCLK for the CPU related functions and to generate DMACLK.
- 32KHz for the real time clock.

14.31818MHz Clock

Crystal pins are provided for the 14MHz clock. 20pF capacitors should be included from each crystal pin to ground as well as a 2M resistor used across the crystal pins. X2 should be buffered with a bus driver or inverter to form an oscillation for the bus. A 33 ohm series resistor should be placed between the buffer and the bus. Place the resistor as close to the buffer as possible.

The 14MHz clock is divided by 12 internally to form the 1.19MHz clock used by the IPC timers.

SCLK

SCLK, the 1x CPU clock, is provided to the 84035. In a 386 system, a 1x clock with low skew to the 2x clock must be provided (this is also required for VL-Bus slots).

SCLK is used for the arbitration logic, for the control link timing, and for generating the clock to the DMA controllers and refresh logic.

The DMA controller and refresh clock should be around 8MHz. It is divided by 2 by the IPC core to obtain the 4MHz at which the DMA controllers normally operate. The following dividers are provided from SCLK to form the DMA clock. The divider is actually implemented as a selectable divide by 2 prescaler followed by a programmable divider of 2, 2.5, 3, 4, or 5.

84035 CLOCK DIVIDER

Divider	Pre-scale	2nd Stage	CPU Freq. Used (MHz)	DMA Clock Freq. (MHz)	8237 Clock Rate (MHz)
10	/2	/5	80	8	4
8	/2	/4	66	8	4
6	/2	/3	50	8.33	4.17
5	/1	/5	40	8	4
4	/1	/4	33	8.33	4.17
3	/1	/3	25	8.33	4.17
2.5	/1	/2.5	20	8	4
2	/1	/2	16	8	4

32.768KHz CLOCK

The clock source is a 32KHz external or internal oscillator that must be made to run from the battery when power from the AT is turned off. It is used by the real time clock in the 84035.

RESET

The 84035 contains the reset logic for the system. It receives PWRGOOD signals and generates SYSRESET and CPURESET signals. It also receives soft reset requests over the control link to generate CPURESET.

PWRGOOD disables all outputs and gates off all inputs to the chip except for PWRSTB#, 14MX2, the 32KHz oscillator pins, and from PWRGOOD itself. When PWRGOOD goes high the outputs are enabled. SYSRESET and CPURESET are driven high, and remain high for 8 million SCLKs to assure proper startup of the 14.31818MHz oscillator, and to allow the 486 VCO to stabilize. This is accomplished by a 23-bit counter clocked by SCLK.

SYSRESET is generated based on the PWRGOOD circuit alone. CPURESET is generated based on PWRGOOD, but is also be generated for "soft resets". The following are the sources of soft resets:

- Keyboard controller reset
- CPU shutdown cycle
- Port 92 bit 0 transitioning from a 0 to a 1.

Keyboard reset and shutdown are sent to the 84035 through the control link from the 84031. When the 84035 receives the request, it immediately passes the request onto the logic which arbitrates CPURESET with CPU HOLD. See the DRAM Controller, Control Link section for information on how the reset request is sent from the 84031.

Port 92 is contained in the 84035. When bit 0 makes a 0 to 1 transition a CPU reset is requested at about 16 BUSCLKs later. This delay allows the CPU to execute a HALT instruction.

CPURESET is 16 SCLKs long for soft resets. The falling edge always occurs during phase 1 while SCLK is high.

GATEA20

The 84035 generates the A20M# signal. The 486 actually does the gating. The keyboard controller GATEA20 and port 92 bit 1 are the two sources that generate the A20M# signal.

The keyboard controller GATEA20 information is sent from the 84031 through the control link. There are GATEA20 = 1 and GATEA20 = 0 codes that are sent across. This sets and resets a flip-flop to form the keyboard GATEA20 in the 84035. This flip-flop powers up in the high state, to allow the CPU to boot.

Port 92 bit 1 is an output port bit internal to 84035.

The two internal sources of A20M# are ORed together and driven out on the A20M# pin.

The A20M# output pin is shared with the TEST# input. At power-up, this pin is floated and remains that way until index register 09 bit 4 is written to a 1. This bit disables the test input and begins driving A20M#. Until the bit is set to 1, an external pull-up resistor keeps the pin high, prevents the 84035 from going into test mode, and holds A20M# high before the CPU is allowed to boot.

ARBITRATION

The arbitration logic for the system is contained in the 84035. It arbitrates between the CPU, local bus masters, and the internal DMA controllers. It also puts the CPU in HOLD to slow it down when performance control is enabled, arbitrates between CPU HOLD and CPURESET, and arbitrates between the DMA controller and hidden refresh.

The following signal pins are in the arbitration block:

- HOLD and HLDA for the CPU
- LREQ# and LGNT# for local bus masters
- DGNT# indicating the DMA controller has the bus.

There is a two way arbitration between local bus masters and the DMA controller. The CPU gets the bus when no other master wants it. The arbitration is performed using SCLK, and all signals are synchronous to it.

There is a fixed priority to bus activity. The priority are as follows:

1. DMA controller
2. Hidden Refresh
3. Local Master
4. CPU.

Note that either a local master or the CPU have control of the bus when a hidden refresh occurs. Hidden refresh is listed above because it may not occur when the DMA controller has the bus; it has a lower priority. For instance, if the DMA controller requests the bus and a hidden refresh request occurs before the CPU or local master gives up the bus, the hidden refresh will be delayed until after the DMA controller gives up the bus.

Hidden refresh is arbitrated for with the DMA controller, since these must be mutually exclusive. The hidden refresh may occur while the CPU or a local master is in control. The CPU refresh is arbitrated for

with the CPU HOLD signal. The CPU will not be reset while it is in hold.

The LREQ# and LGNT# signals support a preemptive protocol for the VL-Bus masters. If a DMA HOLD occurs while a VL-Bus master has the bus, LGNT# is driven back high, requesting that the local master give up the bus. The local master will take LREQ# back high to indicate that it has given up the bus.

The performance control HOLD request is ORed with the other sources of HOLD, but does not enter into the arbitration. A DMA cycle or ISA master may gain access to the bus during a performance control HOLD without waiting for it to finish.

The 84031 receives the CPU HLDA, DGNT#, and MASTER# signals as an indication of what device is in control of the bus. The encoding is as follows:

BUS OWNER INDICATION

Bus Owner	HLDA	DGNT#	MASTER#
(Invalid)	0	0	0
(Invalid)	0	0	1
(Invalid)	0	1	0
CPU	0	1	1
ISA-Bus Master	1	0	0
DMA Controller	1	0	1
(Invalid)	1	1	0
Local Bus Master	1	1	1

The major functions controlled by the arbitration signals are as follows:

- The 84031 does not generate parity for CPU writes to DRAM, but does for local masters, DMA and ISA masters (HLDA used to select).
- DRAM write cycles are forced to 1 wait state when a local bus master has the bus (due to the extra time required to generate parity).
- The control link functions change (particularly the 84035 to 84031 direction) with DGNT#.
- When DGNT# is high, the 84031 is a local bus slave and the ISA-bus master. ISA-bus cycles are generated in response to local bus activity.
- When DGNT# is low, the 84031 is the local bus master and an ISA-bus slave. Local bus cycles are generated in response to ISA-bus activity.
- When DGNT# is low and MASTER# is high, the 84031 drives A16:10 with the contents of the DMA latch.

PERFORMANCE CONTROL

Performance control refers to slowing the CPU down. A 486 may execute code too rapidly for some speed sensitive software. The 84035 makes no attempt to reduce speed via the CPU clock since the 486 cannot handle a rapid frequency change. Instead it puts the CPU in hold for a programmable percentage of time. This is implemented as follows:

1. On every refresh request the CPU is put in HOLD for a programmable period of time. The FLUSH# pin is also pulled low during this time to make sure the CPU doesn't continue to execute out of its internal cache. The length of the HOLD pulse is selected to provide the desired degradation in performance. The intent is to match the speed of an 8MHz AT in order to allow some games and copy protection programs to work properly. The FLUSH# and HOLD functions may be enabled separately, but generally these will be used together. After the HOLD length is set, the slow mode may be enabled and disabled by either of two ways: Index register access and the "slow" input. This is an OR function, allowing either of these to slow the system down (these both should be disabled for full speed).
2. The clock generated for the IPC DMA controllers is used for the time base of the performance control. This clock is normally about 8MHz. The CPU is always given a small slice of time between performance control HOLDs even if the count is set above the time between refresh periods.
3. The HOLD is initiated each time the refresh request occurs from timer 1. Local bus master, DMA, ISA master, or refresh cycles may occur while the performance control HOLD is taking place.

REFRESH

The refresh function involves both the 84031 and 84035. The refresh arbitration must be coordinated between the two chips with the 84035 performing the refresh cycle. It drives SA7:0, REFRESH#, and MEMR# directly. SA7:0 are the refresh address for the ISA-bus and the REFRESH# and MEMR# signals indicate to the 84031 that this is a DRAM refresh cycle.

The refresh mechanism starts with the 84035. When timer 1 produces a refresh request, the internal logic of the 84035 must arbitrate with the DMA controllers before the refresh request code is sent through the control link to the 84031. When hidden refresh wins the arbitration, LOUT is pulled low, indicating a refresh request to the 84031. (When DGNT# is high, the LOUT is used only for hidden refresh). The 84031 will arbitrate this with CPU or local master accesses to the ISA-bus, and send a refresh grant back to the 84035. This will be encoded and come in the LIN pin. At this point the 84035 will perform the refresh cycle. When the refresh cycle is complete, the 84035 will take LOUT back high, indicating the end of the refresh to the 84031. After LOUT goes high, HLDA to the DMA controller may go active. There should be at least 1 clock between LOUT going high and HLDA to the DMA controller going active.

The 84031 contains the DRAM controller, it receives all refresh requests, both hidden refresh and master refresh, and will perform a CAS before RAS refresh on the DRAMs. It places the refresh cycles between other DRAM activity. The CPU is never put in a HOLD state specifically for refresh.

For master refresh no arbitration need be done since the current master is requesting the refresh. When the ISA master pulls REFRESH# low, the 84035 performs the refresh by driving SA7:0 with the refresh and driving MEMR# and SMEMR#. The 84035 also pulls LOUT low for the duration of REFRESH# active to indicate to the 84031 that a refresh is occuring. The 84031 will use this to refresh the local DRAMs. The 84031 knows this is a master refresh and not a hidden refresh request by looking at the DGNT# and MASTER# pins.

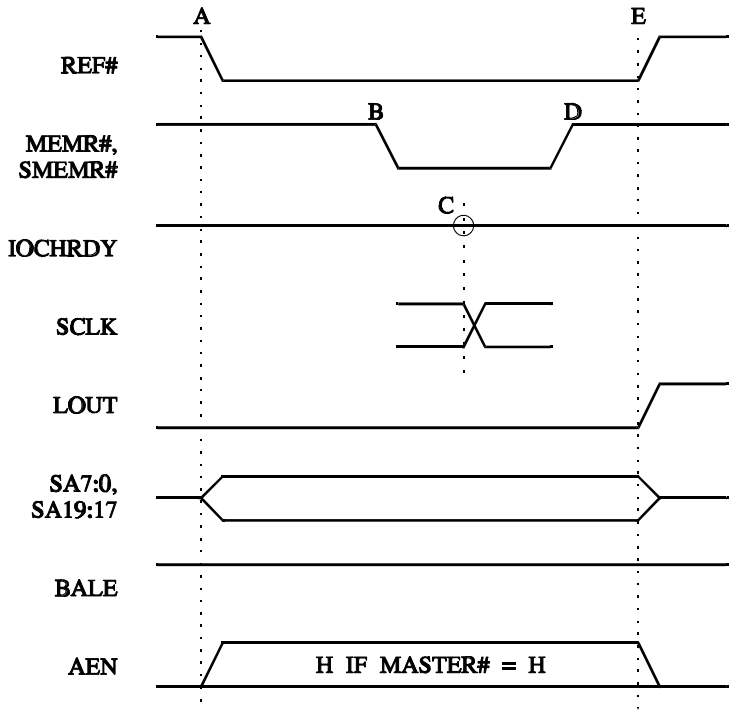
The 84035 will drive both MEMR# and SMEMR# low for refresh cycles, regardless of the address on the upper bits (for normal bus cycles SMEMR# is only driven when A23:20 are all low).

ISA-Bus Refresh Cycles

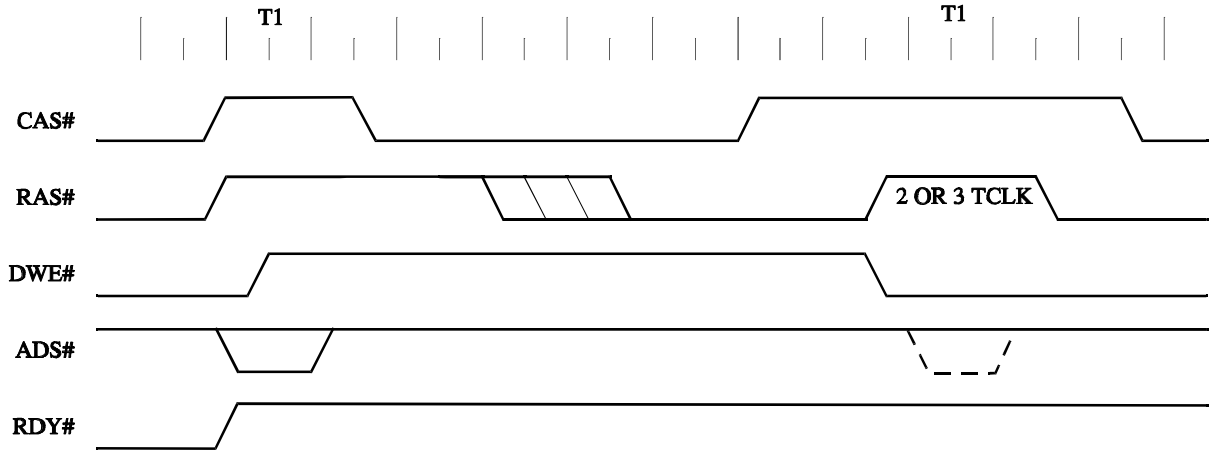
The refresh cycle starts at point A, when the 84035 has received a Refresh Acknowledge code from the 84031 via the LIN/LOUT control link. The falling edge of the command at point B is 2 BUSCLK cycles from point A. At point C the IOCHRDY signal is sampled, if it is high the command will end at D 1 BUSCLK cycle later. If IOCHRDY is low the command will be extented. At point E the REF# signal terminates the refresh and the 84035 raises its LOUT signal to indicate the “end of refresh.” See the timing diagram on the following page.

DRAM Refresh Cycles

These are always hidden refresh cycles; there is no HOLD/HLDA needed. All DRAM refreshes are CAS before RAS refresh cycles. The hidden refresh cycle can begin immediately at the end of the RDY# from the previous cycle, or anytime after RDY# and before the end of the next ADS#. The RAS# and CAS# signals go high at end of the cycle. Once the hidden refresh cycle begins and CAS# is low the RAS# signals will fall in staggered timings, 0.5 CLK cycles apart. The last RAS# to fall has a 3 CLK cycle low time.



ISA-Bus Refresh Timing Diagram



DRAM Refresh Timing Diagram

ISA-BUS

This section describes the generation and usage of the ISA-bus control signals on the 84035.

For the AEN signal:

This signal is high when DGNT# is low and MASTER# high. It is always an output. Internally it disables all of the I/O decodes. It goes to the IPC megacell, where it disables its I/O decodes. It signifies that a DMA cycle is coming or in progress; the address on the ISA-bus is a memory address and not an I/O address.

For the MASTER# signal:

This is an input. It is used to force AEN# low during ISA master cycle.

For DREQ7:0, DACK7:0#, and TC signals:

These come directly from the IPC megacell and are sent out as is. DREQ7:0 are inputs. DACK7:0# and TC are always outputs.

For MEMR# and MEMW# signals:

When DGNT# is high these signals are inputs to the 84031 that is used to generate SMEMR# and SMEMW. During hidden refresh (DGNT# will be high here also), MEMR# is an output from the refresh logic. MEMW# remains an input during hidden refresh.

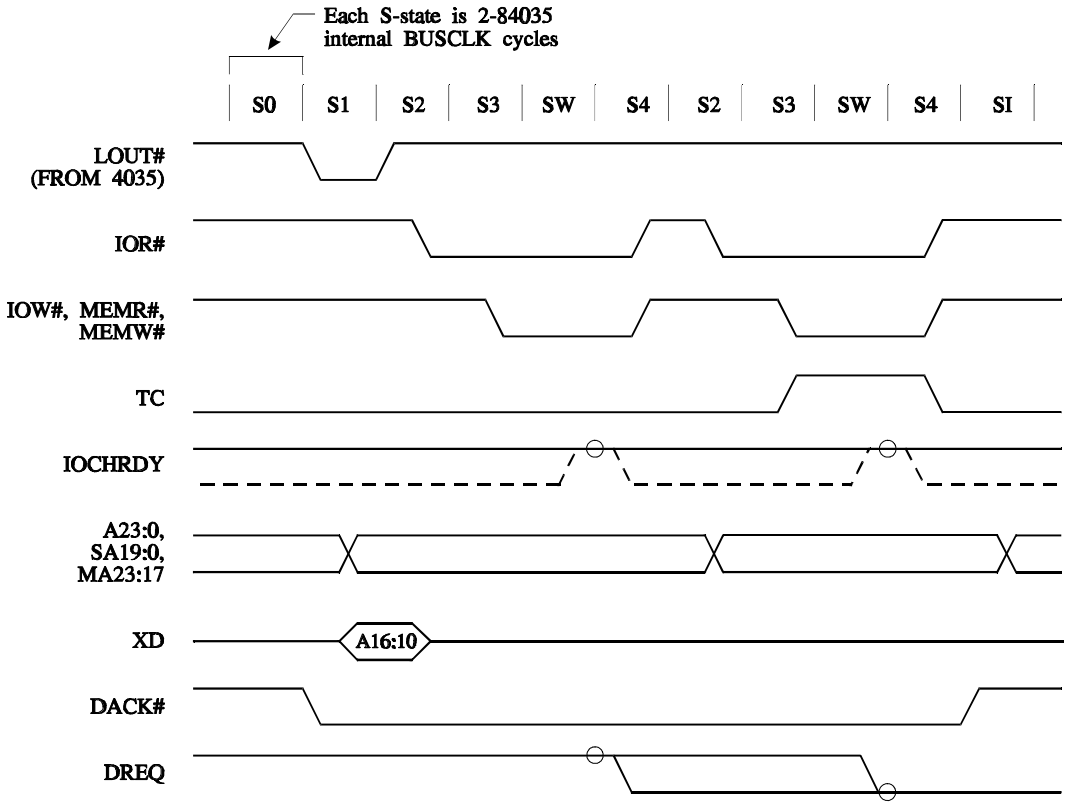
When DGNT# is low and MASTER# is high these signals are outputs from the IPC megacell. When MASTER# is low these are inputs, used to generate SMEMR# and SMEMW#, except for Master Refresh cycles (MASTER# and REFRESH# are both low) at which time MEMR# becomes an output from the refresh logic.

For SMEMR# and SMEMW# signals:

These follow MEMR# and MEMW# respectively when the address is below 1MB (A23:20 are all low). These are high if any of A23:20 are high. An exception to this is when REFRESH# is low, at which time SMEMR# follows MEMR# regardless of the address.

For IOR# and IOW# signals:

These signals are driven from the IPC megacell when DGNT# is low and MASTER# is high. At all other times these are inputs to the internal I/O.



DMA Timing Diagram

486 FLOATING-POINT LOGIC

The 84035 has two modes for the floating-point error handling. It may do the error handling either internally or externally.

Internal mode is used for the 486, or other CPUs which have the coprocesspor internally and have FERR# and IGNNE# signals. In this mode the 84035 receives the FERR# signal and generates IGNNE#. Internally, it generates IRQ13 to the IPC megacell. There is no IRQ13 input signal in this mode.

External mode is required for using the Weitek coprocessor because it generates IRQ13 directly. The FERR# pin becomes the IRQ13 input pin in this mode, and the IGNNE# pin becomes INTCLR, which is a decode of I/O ports F0 and F1. An external PAL uses these signals, as well as the coprocessor error signals to handle the AT-compatible coprocessor function.

Port B and Speaker Logic

The 84035 contains the following bits for port B (I/O port 61):

84035 PORT B BITS

Bit	I/O Write	I/O Read	Usage
0	Tmr Gate 2	Tmr Gate 2	Speaker circuit
1	Spkr Data	Spkr Data	Speaker circuit
2	ENB RAM PCK	ENB RAM PCK	(In the 84031)
3	EN IO CK	EN IO CK	(In the 84031)
4	—	REF Det	from ref det circuit
5	—	OUT2	from tmr 2 output
6	—	—	(In the 84031)
7	—	—	(In the 84031)

Bits 6 and 7 are supplied by the 84031. Bits 2 and 3 also exist in the 84031 and are used for enabling the parity check logic. These are latched and driven back in the 84035.

The speaker circuit consists of an AND gate and the output driver.

CS4031 Electrical Specifications

The tables and figures in this section describes the operating environment and signal timing required by the CS4031 CHIPSet.

84031/84035 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	—	7	V
V_I	Input voltage	-0.5	5.50	V
V_O	Output voltage	-0.5	5.50	V
T_{OP}	Operating temperature	-25	85	C
T_{STG}	Storage temperature	-40	125	C

Note: Permanent device damage may occur if the absolute maximum conditions are exceeded. The functional operation should be restricted to the recommended operating conditions. See the next table.

84031/84035 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	84035 operating	4.50	5.25	V
V_{CC}	Supply voltage	84031 operating	4.75	5.25	V
V_{CC}	Supply voltage	84035 standby	3.0	5.25	V
T_A	Ambient temperature	—	0	70	C

84031/84035 DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input capacitance	—	10	pF
$C_{I/O}$	I/O capacitance	—	20	pF
C_{OUT}	Output capacitance	—	20	pF
V_{IL}	Input low voltage	-0.5	0.8	V
V_{IH}	Input high voltage	2.0	V_{CC} +0.5	—
V_{OL}	Output low voltage	—	.4	V
V_{OH}	Output high voltage	2.4	—	V
V_{CL}	Clock output low	—	0.4	V
V_{CH}	Clock output high	—	V_{CC} -0.5	V
I_{IL}	Input leakage current	-10	20	µA
I_{OL}	Output leakage current	-10	20	µA
I_{CC}	V_{CC} supply current	—	100	mA
I_{CCSB}	V_{CC} supply current, 84035 standby mode	—	50	µA

84031 AC CHARACTERISTICS

The following tables provide the signal timings required by the 84031. The specifications are based on supporting the following system configurations:

- 33MHz CPU speed with 60ns DRAM, or 25MHz CPU speed with 80ns DRAM.
- 3-2-2-2/2T read timing, 1WS/2T write timing, 3T RAS precharge, 1-bit wide DRAMs, 2 banks, direct drive with a separate set of series resistors for each bank; or, up to four banks, F244 drive, with a separate set of F244 drivers for each bank.
- Maximum of 36 DRAMs driven by any one series resistor or F244 output.

All parameters are output delays unless otherwise defined as input setup or hold times. Output delays are specified at 50pF maximum load unless otherwise stated.

Specifications are in nanoseconds (ns) unless otherwise stated. All specifications apply over the full temperature and voltage range, i.e., 0-70°C and 4.75-5.25 VDC (4.5-5.25 VDC for 84035).

For timing diagrams, see the timing waveforms at the end of this section. The functional timing diagrams are shown earlier in the data sheet.

CLOCK SIGNALS

Parameter	Description	Min	Max
t1	CLKIN input low time	6*	—
t2	CLKIN input high time	6*	—
t3	CLK2OUT output delay from CLKIN	—	20
t4	SCLKOUT output delay from CLK2OUT rise	-2	+2
t6	CLK2 input low time	5*	—
t7	CLK2 input high time	5*	—
t8	SCLK input delay from CLK2 rise	-2*	+2*

* Input specification.

DRAM SIGNALS

Parameter	Description	Load (pF)	Max
t10	RAS# fall from CLK2 rise	—	32
t10a	RAS# fall from CLK2 rise	250	32
t11	RAS# rise from CLK2 rise	—	50
t11a	RAS# rise from CLK2 rise	250	50
t12	CAS# fall from CLK2 rise	—	15
t12a	CAS# fall from CLK2 rise	125	15
t13	CAS# rise from CLK2 rise	—	14
t13a	CAS# rise from CLK2 rise	125	14
t15	Row address hold from CLK2 rise	—	see te15
t16	Row address delay from BE3:0/A31:2	—	see te16
t16a	Row address delay from BE3:0/A31:2	432	see te16
t18	Column address valid from CLK2 rise	—	23
t18a	Column address valid from CLK2 rise	432	33
t20	Column address delay from A31:2	—	24
t20a	Column address delay from A31:2	432	34
t22	DWE# fall from CLK2 rise	—	see te22
t22a	DWE# fall from CLK2 rise	500	see te22
t23	DWE# rise from CLK2 rise	—	see te23
t23a	DWE# rise from CLK2 rise	500	see te23
t24	DWE# delay from local bus status	—	see te24
t24a	DWE# delay from local bus status	500	see te24

84031 DRAM FORMULA SPECIFICATIONS

Formula specifications are provided to aid in performing worst-case timing margin calculations for actual system designs. Formula specifications refer to the minimum or maximum result of a specified calculation involving other chip parameters. For any particular chip, formula specifications usually express a "tracking" relationship over temperature and voltage for the parameters involved in the formula.

For any given test chip, formula specifications may be verified by the following procedure:

1. At selected combinations of temperature and voltage, the actual values of the parameters involved in the formula are measured.
2. The resulting formula value is then computed at each temperature and voltage measurement point. The specified formula limit applies to any 84031 chip at any combination of temperature and voltage within the rated operating range.

The following abbreviations are used in the table below to indicate the type of cycle in cases where it might otherwise be unclear:

Rd	Memory read cycle
Rf	CAS-bore-RAS refresh
W	Memory write cycle

"Critical Path" refers to the timing case for the formula specification that is critical.

DRAM FORMULA SPECIFICATIONS

Parameter	Critical Path	Formula	Max
te12b	CAS# fall before RAS# fall (Rf)	t12a-t10	19
te12c	CAS# fall to RAS# rise	t12-t11	10
te12e	CAS# pulse width (low time)	t12a-t13a	10
te13a	CAS# rise after RAS# fall (Rf)	t10a-t13	10
te13b	CAS# precharge (high time)	t13-t12	4
te13c	CAS# precharge (high time)	t13a-t12a	4
te15	Row address hold after RAS fall	t10-t15	16
te16	Row address setup before RAS# fall	t16-t10	14
te16a	Row address setup before RAS# fall	t16a-t10a	20
te18	Column address setup before CAS# fall	t18-t12	16
te18a	Column address setup before CAS# fall	t18a-t12a	26
te20	Column address setup before CAS# fall	t20-t12	13
te20a	Column address hold after CAS# fall	t12-t20	16
te22f	DWE# hold high after CAS# rise	t13-t22	15
te23	DWE# rise before CAS# fall for read	t23-t12	14
te24b	DWE# rise before CAS# fall for read	t24-t12	11
te24c	DWE# rise before CAS# fall for read	t24a-t12a	22

CPU AND LOCAL BUS SIGNALS

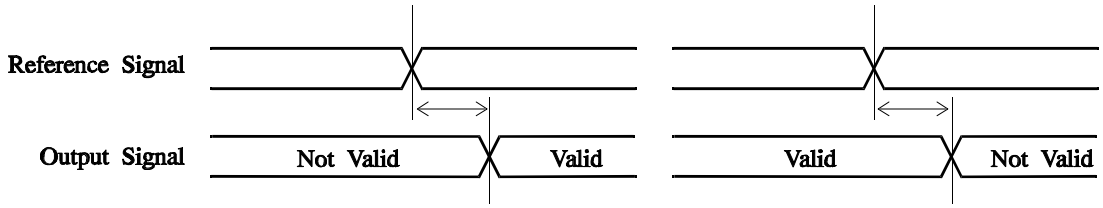
Parameter	Definition	Min	Max
t40	ADS#, A31:2, BE3:0#, M/IO#, D/C#, W/R#, and HLDA input setup before CLK2 rise (CPU/LBM)	12*	—
t43	ADS#, A31-2, BE3:0#, M/IO#, D/C#, W/R#, and HLDA input hold before CLK2 rise (CPU/LBM)	1*	—
t41	BLAST# input setup before CLK2 rise (CPU/LBM)	8*	—
t44	BLAST# input hold after CLK2 rise (CPU/LBM)	1*	—
t42	ADS# delay from SCLK (ISA master)	5	20
t42a	M/IO# fall from XIOR# or XIOW# fall (ISA master)	—	25
t42b	BE3:0 delay from XA0, XA1, and SBHE# (ISA master)	—	23
t45	RDY# and BRDY# delay from CLK2 (CPU/LBM access to DRAM)	6	21
t45a	RDY# delay from SCLK (CPU/LBM ISA-bus access)	4	23
t46	(LBT) RDY#input setup before CLK2 rise	10*	—
t46a	(LBT) RDY# input hold after CLK2 rise	1*	—
t47	CPU read, D31:0, and MP3:0 input setup before CLK2 rise (for parity checking)	3*	—
t50	EADS# delay from CLK2	6	21
t51	KEN# delay from CLK2	6	21
t54	NMI delay from CLK2	6	23
t56	LIN input setup before SCLK rise	10*	—
t57	LOUT delay from SCLK	—	15
t58	DGNT# input setup before SCLK rise	5*	—
t59	DGNT# input hold after SCLK rise	3*	—
t60	LEDV# input setup before CLK2 rise	7*	—
t62	MEMCS16# output delay from LDEV# (ISA master access to VL-Bus)	—	15
t63	IOCHRDY output fall from ISA memory command fall (DMA and ISA master)	—	50
t65	IOCHRDY output delay from CLK2 rise (ISA master I/O)	—	50
t70	XA0, XA1, and SBHE# delay from BUSCLK (ISA-bus convert cycle)	—	25
t102	BALE delay from BUSCLK	—	15
t103	MEMR#/MEMW# delay from BUSCLK	3	15
t104	IOR#/IOW# delay from BUSCLK	3	15
t105	IOCHRDY setup before BUSCLK	10*	—
t107	XD7:0 or D31:0 setup before MEMR# rise/fall for AT read	10*	—
t108	XD7:0 or D31:0 hold after MEMR# rise	5*	—
t109	D31:0 valid from XD7:0	—	40
t110	XD7:0 valid from D31:0	3	15
t111	A16-10 delay from XD7:0 during DMA	—	70
t113	MEMCS16# or IOCS16# setup before BUSCLK	20*	—

* Input requirement.

84035 AC CHARACTERISTICS

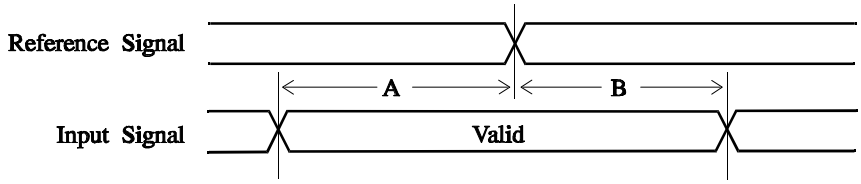
Parameter	Description	Min	Max
t200	CPURESET delay from CLK	—	22
t201	SYSRESETdelay from CLK	—	22
t202	HOLD delay from CLK	3	19
t203	REFRESH delay from CLK	—	30
t204	AEN delay from SCLK/BUSCLK	—	50
t205	TC delay from SCLK/BUSCLK	—	50
t206	DACK# delay from BUSCLK	5	50
t207	MEMR#/MEMW# delay from BUSCLK (DMA Cycle)	3	15
t208	SMEMR#/SMEMW# delay from MEMR#/MEMW#	—	15
t209	IOR#/IOW# delay from BUSCLK (DMA Cycle)	3	15
t210	IOCHRDY setup to CLK (DMA Cycle)	—	10
t211	SA7:0, A8, and A9 delay from LA bus (DMA Cycle)	—	70
t212a	XD7:0 delay from IOR#	5	50
t212b	XD7:0 hold from IOR#	—	10
t212c	XD7:0 setup to IOW#	—	50
t212d	XD7:0 hold from IOW#	0	—
t213	INTR delay from SCLK	—	22
t214	IGNNE#/INTCLR from SCLK	—	22
t215	SPKR output valid delay from SCLK	—	100
t216	LOUT output valid delay from SCLK	—	15
t217	Setup time to SCLK	—	15
t218	IRQ setup time to SCLK	10*	—
t219	DREQ setup time to SCLK	10*	—
t220	LGNT setup to SCLK	10*	—
t221	HLDA setup to SCLK	5*	—
t222	FERR# setup to SCLK	5*	—
t223	FLUSH# delay from SCLK	—	22

* Input requirement.

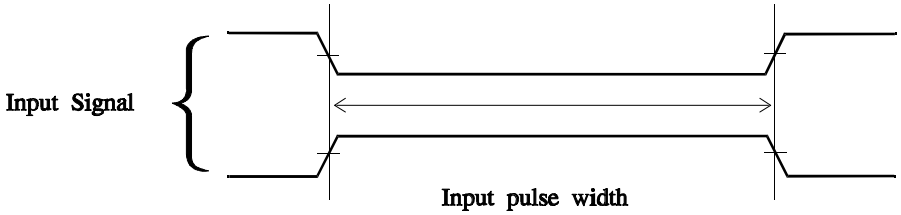


Output valid from reference.
Output delay from reference.
Output rise from reference.
Output fall from reference.
Output active from reference.
Output inactive from reference.

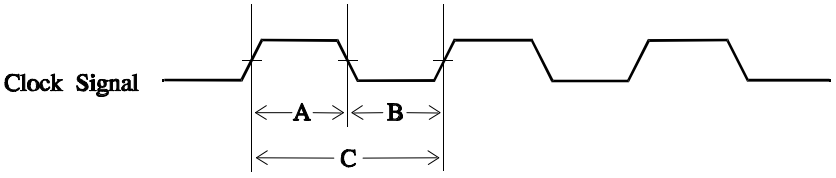
Output hold from reference



A = Input setup before reference
B = Input hold after reference



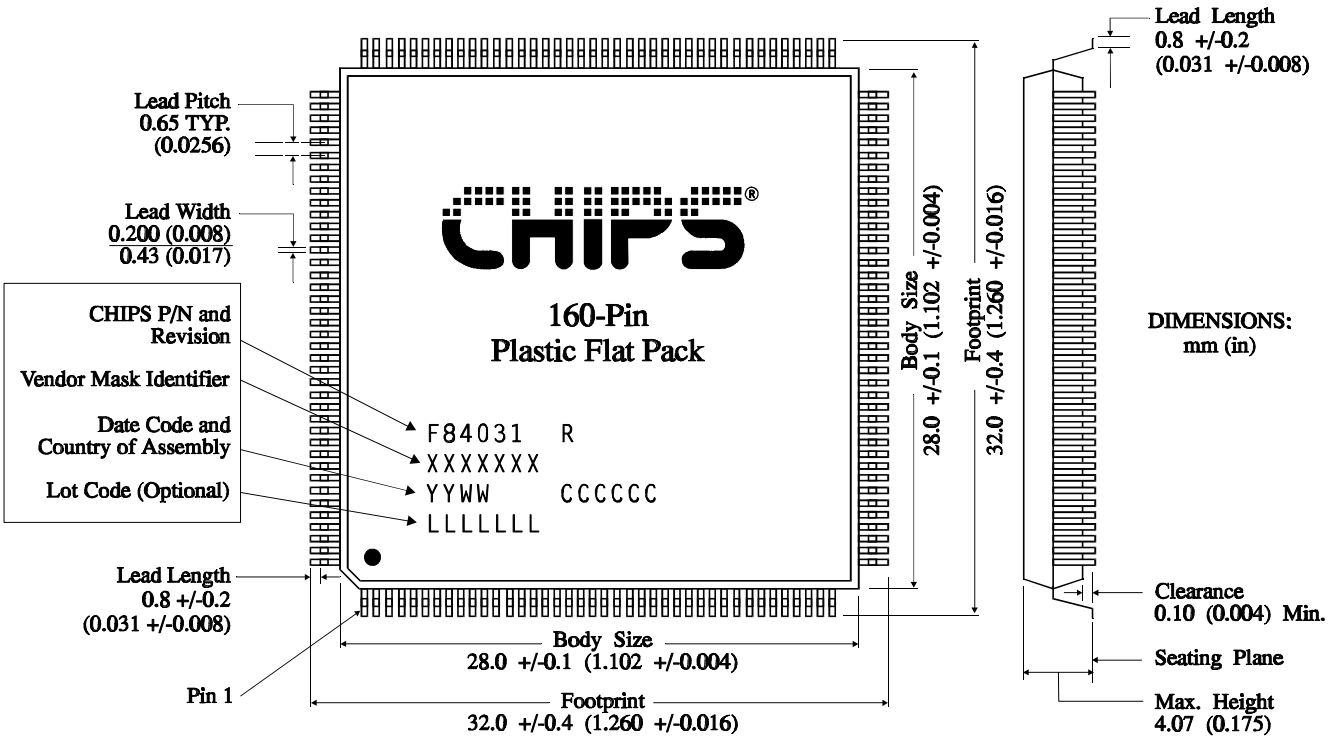
Input pulse width



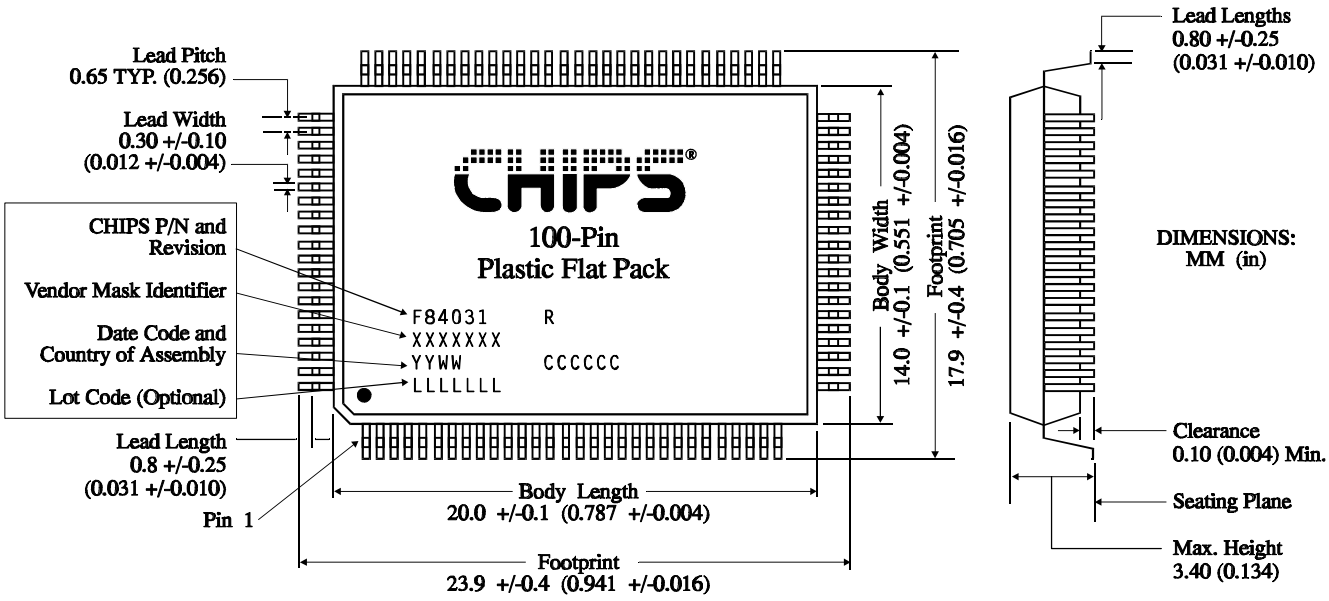
A = Clock high time
B = Clock low time
C = Clock cycle time

Timing Waveforms

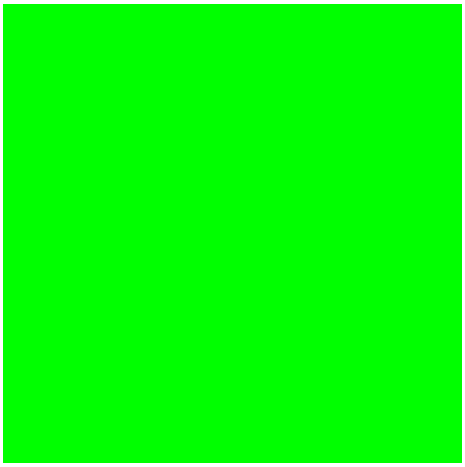
CS4031 Mechanical Specifications



84031 Packaging Dimensions



84035 Packaging Dimensions



Chips and Technologies, Inc.
2950 Zanker Road
San Jose, California 95134
Phone: 408-434-0600
Telex: 272929 CHIPS UR
FAX: 408-894-2080

Title: CS4031 CHIPSet
Advance Product Information

Publication No.: API22
Stock No.: 011022-001
Revision No.: 1.0