82C735

I/O Peripheral Controller With Printgine™

Data Sheet

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PRELIMINARY

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82C735
I/O Peripheral Controller With Printgine

Floppy Disk Controller

- Single-chip floppy solution
- Software compatible with NEC 765B and Intel 82077
- Perpendicular recording support
- 48mA disk drivers and Schmitt-trigger inputs
- Direct support for two drives, and up to four drives with external decoder
- Enhanced digital data separator
- No external filter components required
- Support for 250KB/s, 300KB/s, 500KB/s and 1MB/sec data rates
- Primary and secondary floppy address port selects

Serial Ports

- Two NS16550 compatible UARTs
- 16-byte FIFO
- Modem control circuitry
- Optional PS/2 type mouse port logic operated under BIOS and software driver control

IDE Interface

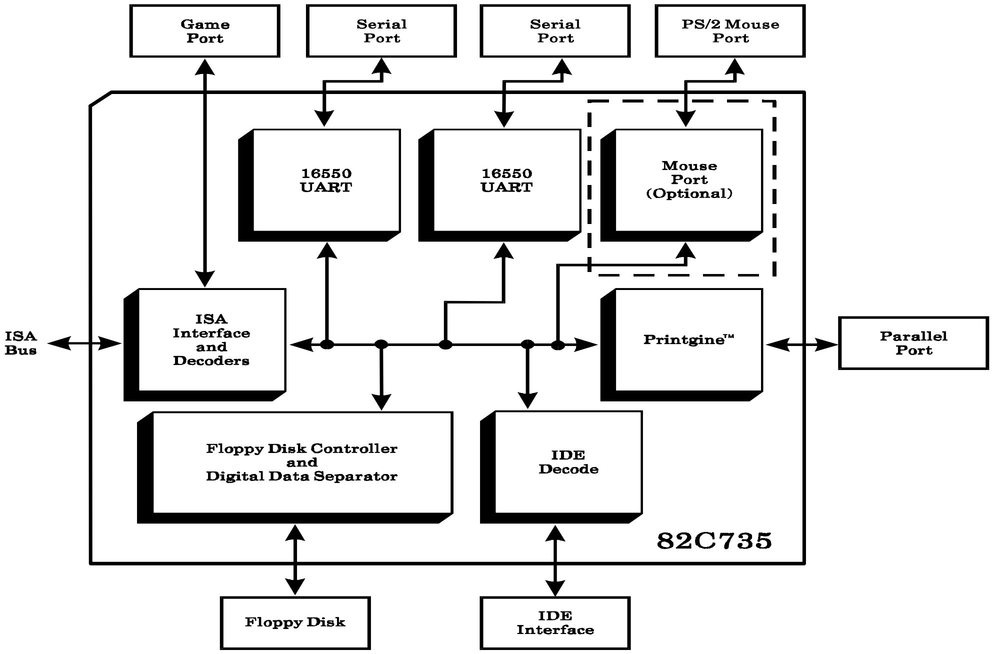
- Provides a complete IDE interface for embedded hard disk drives.
- Primary and secondary IDE address port selects.

Parallel Port—Printgine™

- Multiprotocol parallel port interface, P1284-compatible
- Compatible with IBM PC, XT, AT, and PS/2 architectures
- Standard and bidirectional parallel port
- Microsoft and Hewlett-Packard Extended Capabilities Port (ECP), Enhanced Parallel Port (EPP), and fast Centronics protocols support
- Transfer rates up to 2MB/sec possible with fast protocols
- Protocols implemented in hardware to reduce software overhead
- 24mA parallel port output drivers
- 128-byte FIFO

General

- 100-percent compatible with IBM PC, XT and AT architectures
- 24mA AT/XT bus interface buffers
- Game port and general purpose chip select logic
- On-chip power management features, controllable through hardware and/or software
- Configuration via software
- 100-pin QFP package



System Block Diagram

Revision History

Revision	Date	By	Comment
0.1	4/93	PK	First Draft - Internal Review
0.2	5/93	PK	First Review - Added DC electrical specs; revised registers and mechanical
0.3	6/93	PK	Second Review - Added AC timing
0.4	7/93	PK	Final Draft - Revised AC timing and added mouse port timing; added Tape Drive Register; revised and reformatted register summary tables; added four serial port registers; revised Product Overview; added Register Summary; revised Pinout, Pin List, and Pin Description tables

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Introduction

The CHIPS® 82C735 enhanced I/O peripheral controller is a single-chip solution offering complete I/O capabilities for PC/AT and PC/XT motherboard applications. The controller is configured via software.

The 82C735 features a floppy disk controller, a digital data separator, two 16550 compatible UARTs, an enhanced bidirectional parallel port interface called Printgine, IDE interface control logic, and a game port chip select. For more information about these systems, see the "Functional Description."

4MB FLOPPY DISK CONTROLLER

The floppy disk controller is software compatible with 765B and 82077 controller functions. It provides a 4MB perpendicular recording format as well as the standard floppy drive format for 5.25-inch and 3.5-inch media. The controller supports two drives directly and up to four drives with an external decoder.

DIGITAL DATA SEPARATOR

The digital data separator is capable of data transfer rates up to 1MB/sec and requires no external components.

NS16550 UARTS AND IDE

The two licensed NS16550 UARTs are improved versions of the NS16450 UARTs. They are provided with individual 16-byte FIFOs to relieve the CPU of excessive software overhead and are still capable of running existing 16450 software.

The IDE control logic provides a complete IDE interface for embedded hard disk drives.

MOUSE PORT LOGIC

The 82C735 controller features optional PS/2 style mouse port logic with BIOS and driver support. Only one of the UARTs can be used when the mouse is operational.

PRINTGINE PARALLEL PORT INTERFACE

The parallel port interface, Printgine, is a multiprotocol interface capable of supporting both unidirectional and bidirectional transfer modes. It is fully compatible with ISA and PS/2 in the standard modes, and also supports Microsoft ECP, EPP, and fast Centronics in the enhanced modes. The output on the control pins switch to become bidirectional TTL drivers in the fast modes. This makes the port run faster than is possible with the open-drain drivers provided for the standard modes.

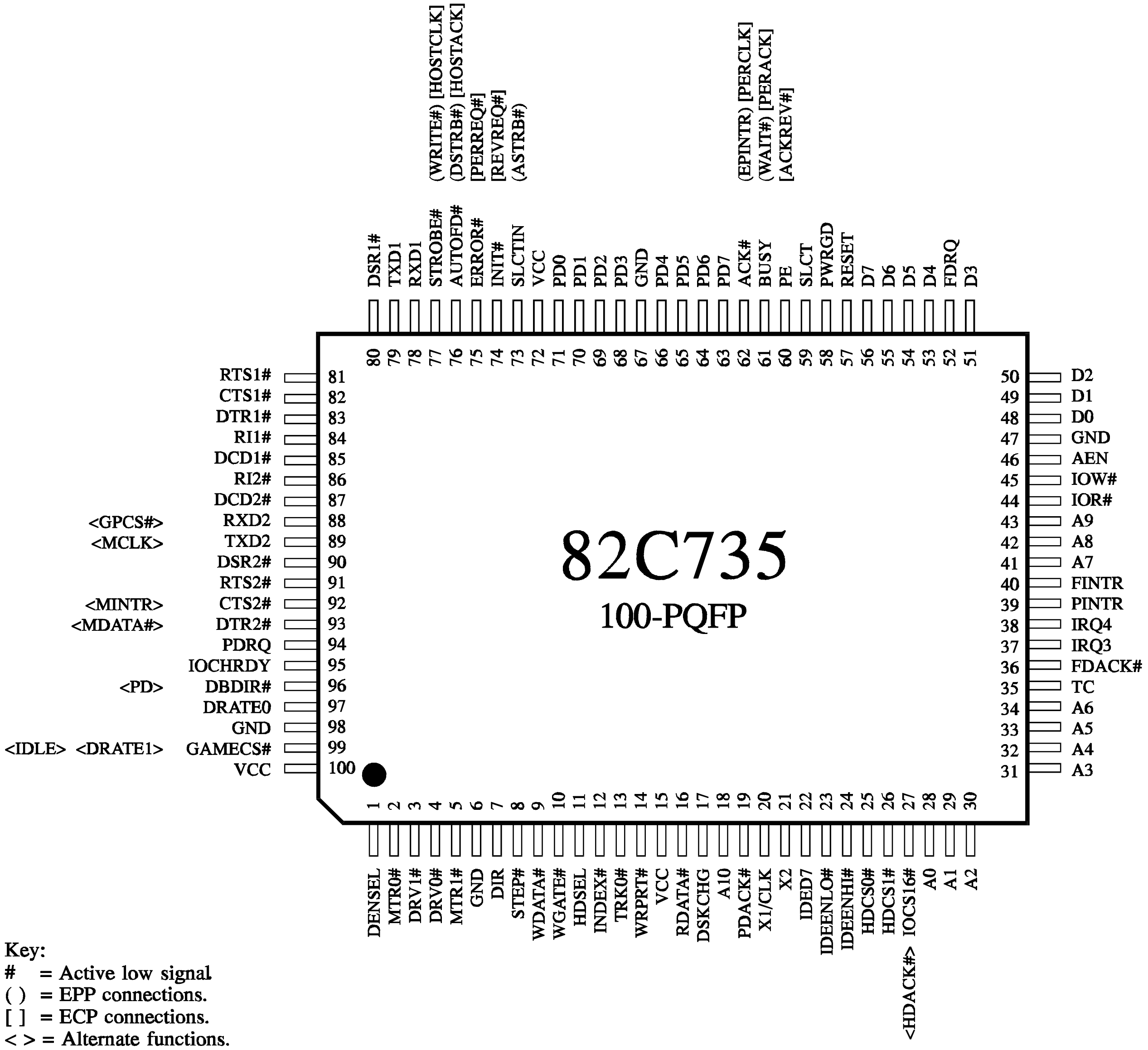
Printgine provides an economical mechanism for significantly improving the throughput of an improved parallel port that is upward compatible with the existing parallel port. The interface can operate in five different modes: standard (ISA-style unidirectional), bi-di (PS/2-style bidirectional), Microsoft ECP, EPP, and fast Centronics. The standard and bi-di modes are compatible with existing parallel port protocols.

The ECP, EPP, and fast Centronics protocols are enhanced bidirectional modes that achieve dramatic improvement by implementing the protocols in hardware. The fast Centronics mode is capable of a data transfer rate of 200KB/sec, while the ECP and EPP modes are capable of data transfer rates of 2MB/sec, compared to 15KB/sec in the standard mode.

POWER MANAGEMENT

The 82C735 is provided with several power management features that are controllable through hardware or software. In hardware, the device can be completely powered down through a powerdown pin. In this mode, all inputs are disabled, all outputs are inactive, and the contents of all registers are preserved (as long as the power supply is maintained). In software, the device allows each port to be powered down independently.

Pinout Diagram



Key:
# = Active low signal
( ) = EPP connections.
[ ] = ECP connections.
< > = Alternate functions.
On power-up, the first signal listed
(not the alternate) is the default.

Pin List

Pin Name	Pin No.	Dir.	Buffer	Driver
A0	28	I	I	—
A1	29	I	I	—
A2	30	I	I	—
A3	31	I	I	—
A4	32	I	I	—
A5	33	I	I	—
A6	34	I	I	—
A7	41	I	I	—
A8	42	I	I	—
A9	43	I	I	—
A10	18	I	I	—
ACK# (EPINTR) [PERCLK]	62	I I	I** I**	— —
AEN	46	I	I	—
AUTOFD# (DSTRB#) [HOSTACK]	76	O O	OC,OH*OH OH	24mA 24mA
BUSY (WAIT#) [PERACK]	61	I I	I** I**	— —
CTS1#	82	I	I	—
CTS2# <MINTR>	92	I O	I T	— 24mA
D0	48	I/O	I/OH	24mA
D1	49	I/O	I/OH	24mA
D2	50	I/O	I/OH	24mA
D3	51	I/O	I/OH	24mA
D4	53	I/O	I/OH	24mA
D5	54	I/O	I/OH	24mA
D6	55	I/O	I/OH	24mA
D7	56	I/O	I/OH	24mA
DBDIR# <PD>	96	O	O	4mA
DCD1#	85	I	I	—
DCD2#	87	I	I	—
DENSEL	1	O	OD	48mA
DIR	7	O	OD	48mA
DRATE0	97	O	O	4mA
DRV0#	4	O	OD	48mA
DRV1#	3	O	OD	48mA
DSKCHG	17	I	IS	—
DSR1#	80	I	I	—
DSR2#	90	I	I	—
DTR1#	83	O	O	4mA
DTR2# <MDATA#>	93	O I/O	OC IS/OC	16mA 16mA
ERROR# [PERREQ]	75	I	I**	—
FDACK#	36	I	I	—
FDRQ	52	O	T	24mA
FINTR	40	O	T	24mA
GAMECS# <DRATE1> <IDLE>	99	O O	O O	4mA 4mA
GND	6, 47, 67, 98			
HDCS0#	25	O	O	4mA
HDCS1#	26	O	OH	24mA
HDSEL	11	O	OD	48mA
IDED7	22	I/O	I/OH	24mA
IDEENHI#	24	O	O	4mA
IDEENLO#	23	O	O	4mA
INDEX#	12	I	IS	—
INIT# [REVREQ]	74	O O	OC,OH* OH	24mA 24mA
IOCHRDY	95	O	OC	24mA
IOCS16# <HDACK#>	27	I	I	—
IOR#	44	I	I	—
IOW#	45	I	I	—
IRQ3	37	O	T	24mA
IRQ4	38	O	T	24mA
MTR0#	2	O	OD	48mA
MTR1#	5	O	OD	48mA
PD0	71	I/O	OH	24mA
PD1	70	I/O	OH	24mA
PD2	69	I/O	OH	24mA
PD3	68	I/O	OH	24mA
PD4	66	I/O	OH	24mA
PD5	65	I/O	OH	24mA
PD6	64	I/O	OH	24mA
PD7	63	I/O	OH	24mA
PDACK#	19	I	I**	—
PDRQ	94	O	T	24mA
PINTR	39	O	T	24mA
PE [ACKREV#]	60	I	I**	—
PWRGD	58	I	I	—
RDATA#	16	I	IS	—
RESET	57	I	IS	—
RI1#	84	I	I	—
RI2#	86	I	I	—
RTS1#	81	O	O	4mA
RTS2#	91	O	O	4mA
RXD1	78	I	I	—
RXD2 <GPCS#>	88	I O	I O	— 4mA
SLCT	59	I	I**	—
SLCTIN# (ASTRB#)	73	O O	OC,OH* OH	24mA 24mA
STEP#	8	O	OD	48mA
STROBE# (WRITE#) [HOSTCLK]	77	O O	OC,OH* OH	24mA 24mA
TC	35	I	I	—
TRK0#	13	I	IS	—
TXD1	79	O	O	4mA
TXD2 <MCLK>	89	O I/O	OC IS/OC	16mA 16mA
Vcc	15, 72, 100			
WDATA#	9	Out	OD	48mA
WGATE#	10	Out	OD	48mA
WRPRT#	14	In	IS	—
X1/CLK	20	In	Iclk	—
X2	21	Out	O	4mA

Notes:
I = TTL input; Iclk = clock input; IS = Schmitt-trigger input;
O = TTL output (4mA); OC= open-drain output (16mA or 24mA);
OD = high-current open-drain output (48mA); OH = high-current TTL output (24mA); T= tristate TTL output (24mA);

Pin Descriptions

HOST INTERFACE PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Active Level	Description
18, 43-41, 34-28	A10-A0	I	High	**Host I/O Address Bus.** Pins A10-0 are latched internally at the beginning of IOR# or IOW#. Pin A10 accommodates enhanced parallel port modes. It is provided with a weak pull-down, so in standard parallel port modes (unidirectional and bidirectional) it can be left open or tied low. In all other modes it is used to access the parallel port control registers at +40x from the base address.
56-53, 51-48	D7-0	I/O	High	**Host Bidirectional Data Bus.** The data bus transfers information between the CPU and the 82C735.
57	RESET	I	High	**Master Reset.** This Schmitt-trigger input from the host resets serial ports, parallel port, mouse port, integrated drive electronics (IDE), and floppy drive controller (FDC). Configuration registers are not affected.
44	IOR#	I	Low	**I/O Read.** IOR# is an active low input from the host.
45	IOW#	I	Low	**I/O Write.** IOW# is an active low input from the host.
46	AEN	I	Low	**Address Enable.** AEN indicates DMA activity. It is normally used with the address bus and IOW#/IOR# to decode I/O address ports.
37 38	IRQ3 IRQ4	T T	High High	**Serial Port Interrupt Request (programmable Polarity).** These interrupts are associated with the serial ports. IRQ4 initiates the signal if the serial channel has been designed as COM1 or COM3. IRQ3 initiates the signal if the channel is COM2 or COM4. The appropriate interrupt is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after the appropriate interrupt service routine is executed, after it is disabled via the IER, or after a RESET. For more information see "Serial Port Registers."
94	PDRQ	O	High	**Parallel Port DMA Request.** If DMA is not used during parallel port data transfers, this pin is tristated.
19	PDACK#	I	Low	**Parallel Port DMA Acknowledge.** This pin has a weak pull-up resistor to accommodate the 82C735 in existing 711 or 721 designs; thus, it can be left open if DMA is not used for parallel port data transfers.
39	PINTR	O	High	**Printer Port Interrupt Request (programmable polarity).** This signal is generated following the ACK# signal input.
95	IOCHRDY	O	High	**I/O Channel Ready.** This signal slows down host transfers when the controller is not ready to respond.
52	FDRQ	O	High	**Floppy Controller DMA Request.** If DMA is not used, this pin is tristated.
36	FDACK#	I	Low	**Floppy Controller DMA Acknowledge.** This pin is normally used to enable DMA read or write.
40	FINTR	O	High	**Floppy Controller Interrupt Request (programmable polarity).** FINTR is used to get the CPU's attention. The required action depends on the current function of the controller.
35	TC	I	High	**Terminal Count.** This input indicates termination of DMA transfer. The signal is qualified by DACK# before it is used on the chip.

PRIMARY SERIAL PORT PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Active Level	Description
82	CTS1#	I	Low	**Clear to Send (primary).** When low, CTS1# indicates that the modem or data set is ready to exchange data. The CPU can monitor this signal's status by reading bit 4 of the modem status register (MSR) of the primary serial port. MSR<4> is the complement of CTS#. MSR<0> shows whether the signal has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when CTS# changes state. This signal has no effect on the transmitter. For additional register information, see "Serial Port Registers."
80	DSR1#	I	Low	**Data Set Ready (primary).** When low, DSR1# indicates that the modem or data set is ready to establish a communications link. The CPU can monitor the signal's status by reading bit 5 of the Modem Status Register (MSR) of the primary serial port. MSR<5> is the complement of DSR#. MSR<1> indicates whether the signal has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when signal DSR# changes state. See "Serial Port Registers" for more register information.
85	DCD1#	I	Low	**Data Carrier Detect (primary).** When low, DCD1# indicates that the modem or data set has detected the data carrier. The CPU can monitor the status of DCD1# by reading bit 7 of the Modem Status Register (MSR) primary serial port. MSR<7> is the complement of DCD#. MSR<3> indicates whether the signal has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when DCD# changes state. For additional register information, see "Serial Port Registers."
84	RI1#	I	Low	**Ring Indicator (primary).** When low, RI1# indicates that the modem has received a telephone ringing signal. The CPU can monitor the status of RI1# by reading bit 6 of the Modem Status Register (MSR) of the primary serial port. MSR<6> is the complement of RI#. MSR<2> indicates whether the signal has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when RI# changes state. See "Serial Port Registers" for more register information.
78	RXD1	I	Low	**Serial Input (primary).** This signal receives serial data input from the communications link.
81	RTS1#	O	Low	**Request to Send (primary).** When low, RTS1# indicates to the modem or data set that the UART is ready to exchange data. This signal can be set to an active low by programming bit 1 of the Modem Control Register (MCR) to a high level (see "Serial Port Registers"). A hardware reset sets the signal to its inactive (high) state; a loop mode operation holds it in its inactive state.
83	DTR1#	O	Low	**Data Terminal Ready (primary).** When low, DTR1# indicates that the modem or data set is ready to establish a communications link. This signal can be set to an active low by programming bit 0 of the Modem Control Register (MCR) to a high level (see "Serial Port Registers"). A hardware reset sets this signal to its inactive (high) state; a loop mode operation holds it in its inactive state.
79	TXD1	O	High	**Serial Output (primary).** TXD1 sends serial output to the communications link. This signal is set to a marking (logic 1) state on a hardware reset, when the transmitter is empty, or when a loop mode operation is initiated.

SECONDARY SERIAL PORT, MOUSE PORT PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Active Level	Description
92	CTS2#	I	Low	**Clear to Send (secondary).** When low, this input indicates that the modem or data set is ready to exchange data. The CPU can monitor this signal's status by reading bit 4 of the Modem Status Register (MSR) of the secondary serial port. MSR<4> is the complement of CTS#. MSR<0> shows whether the signal has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when CTS# changes state. This signal has no effect on the transmitter. For more register information, see "Serial Port Registers."
	<MINTR>	I	High	**Mouse Port Interrupt Request (alternate).** This signal interrupts the host for attention. It is enabled/disabled by bit 4 of the Mouse Control Register (see "Mouse Port Registers").
90	DSR2#	I	Low	**Data Set Read (secondary).** When low, DSR2# indicates that the modem or data set is ready to establish a communications link. The CPU can monitor this signal's status by reading bit 5 of the Modem Status Register (MSR) of the secondary serial port. MSR<5> is the complement of DSR#. MSR<1> indicates whether this input has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when signal DSR# changes state. For additional register information, see "Serial Port Registers."
87	DCD2#	I	Low	**Data Carrier Detect (secondary).** When low, DCD2# indicates that the modem or data set has detected the data carrier. The CPU can monitor the status of this signal by reading bit 7 of the Modem Status Register (MSR) secondary serial port. MSR<7> is the complement of DCD#. MSR<3> indicates whether this input has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when DCD# changes state. For additional register information, see "Serial Port Registers."
86	RI2#	I	Low	**Ring Indicator (secondary).** When low, RI2# indicates that the modem has received a telephone ringing signal. The CPU can monitor the status of RI2# by reading bit 6 of the Modem Status Register (MSR) of the secondary serial port. MSR<6> is the complement of RI#. MSR<2> indicates whether the signal has changed state since the previous MSR reading. If bit 3 of the Interrupt Enable Register (IER) is set, the interrupt is generated when RI# changes state. See "Serial Port Registers" for additional register information.
88	RXD2	I	High	**Serial Input (secondary).** This signal receives serial data input from the communications link.
	<GPCS#>	O	Low	**General Purpose Chip Select (alternate)**. When low, GPCS# decodes the address in configuration register CR09H. For register information, see "Configuration Registers."
91	RTS2#	O	Low	**Request to Send (secondary).** When low, RTS2# indicates to the modem or data set that the UART is ready to exchange data. RTS2# can be set to an active low by programming bit 1 of the Modem Control Register (MCR) to a high level (see "Serial Port Registers"). A hardware reset sets this signal to its inactive (high) state; a loop mode operation holds it in its inactive state.

SECONDARY SERIAL PORT, MOUSE PORT PIN DESCRIPTIONS (*Continued*)

Pin Number	Pin Name	Type	Active Level	Description
93	DTR2#	O	Low	**Data Terminal Ready (secondary).** When low, DTR2# indicates that the modem or data set is ready to establish a communications link. This signal can be set to an active low by programming bit 0 of the Modem Control Register (MCR) to a high level (see "Serial Port Registers"). A hardware reset sets this signal to its inactive (high) state; a loop mode operation holds it in its inactive state.
	<MDATA>	I/O	High	**Mouse Data (alternate).** This serial bidirectional pin is used to transmit and receive data from the mouse.
89	TXD2	O	High	**Serial Output (secondary).** TXD2 sends serial output to the communications link. This signal is set to the marking (logic 1) state on a hardware reset, when the transmitter is empty, or when a loop mode operation is initiated.
	<MCLK>	I/O	High	**Mouse Port Clock (alternate).** MCLK is the synchronizing clock for data being transferred between the mouse port and the mouse. This signal is generated by the mouse port when it is transmitting data to the mouse, and by the mouse when it is transmitting to the mouse port.

IDE INTERFACE PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Active Level	Description
27	IOCS16#	I	Low	**I/O Chip Select 16-Bit.** This pin is driven by the peripheral device when it can accommodate a 16-bit access. The hard disk interface generates IOCS16# to inform the host and the 82C735 that 16-bit I/O transfers are about to begin. This signal is active only when data is being transferred in AT mode.
	<HDACK#>	I	Low	**Hard Disk Acknowledge (alternate).** This input is used to acknowledge the DMA request in the XT hard disk mode.
25	HDCS0#	O	Low	**Hard Disk Chip Select 0 for IDE Interface.** In AT mode, this signal decodes addresss space 1F0H-1F7H if the primary address is used, or space 170H-177H if the secondary address is used. In XT mode, HDCS0# decodes address space 320H-323H. This pin is inactive if IDE is disabled via the configuration registers (see "Configuration Registers").
26	HDCS1#	O	Low	**Hard Disk Chip Select 1 for IDE Interface.** In AT mode, HDCS1# decodes addresss space 3F6H-3F7H if the primary address is used, or space 376H-377H if the secondary address is used. This pin is inactive in XT mode and when IDE is disabled via the configuration registers (see "Configuration Registers").
22	IDED7	I/O	High	**IDE Data Bit 7.** This pin provides the data bus bit 7 signal to the IDE hard drive during accesses to addresses 1F0H-1F7H, 170H-177H, 3F6H, and 376H. The pin is tristated during read or write accesses to 3F7H and 377H. In the XT hard disk mode, IDED7 is not used.
24	IDEENHI#	O	Low	**IDE High Data Buffer Enable.** This output enables the high byte data latch during a read or write to the hard disk. The pin is active only when IOCS16# is active and AT mode is selected. It is not used in XT mode and is also inactive when the IDE is disabled.
23	IDEENLO#	O	Low	**IDE Low Data Buffer Enable.** This output enables the low byte data latch during a read or write to the hard disk. It is valid in both AT and XT modes.

PARALLEL PORT PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Active Level	Description
63-66, 68-71	PD7-PD0	I/O	High	**Parallel Port Data Bus.** This bidirectional parallel data bus is used to transfer information between the CPU and peripherals. PD7-0 are configured as open drain pins in standard Centronics and PS/2 bidirectional modes, and as TTL drivers in all the enhanced modes.
77	STROBE#	O	Low	**Data Strobe.** In the Centronics modes, this output indicates to the peripheral device that the data at the parallel port is valid. A pull-up resistor should be provided for this pin.
	(WRITE#)	O	Low	**Write Signal.** In EPP mode, this signal goes low to indicate that the parallel port is performing a write operation.
	[HOSTCLK]	O	High	**Host Clock.** In ECP mode, this signal is used in a closed-loop handshake with [PERACK] (pin 61) to transfer data or address information from the host to the peripheral device.
61	BUSY	I	High	**Busy.** In the Centronics modes, this input indicates that the printer cannot accept more data. The pin has an internal pull-up resistor attached to it.
	(WAIT#)	I	Low	**Wait.** In EPP mode, the peripheral device uses this pin to acknowledge that data or an address transfer requested by the host has been completed.
	[PERACK]	I	High	**Peripheral Acknowledge.** In ECP mode, this signal deasserts to indicate that the peripheral device can accept data. [PERACK] handshakes with [HOSTCLK] (pin 77) in the forward direction. In the reverse direction, it also provides command information.
62	ACK#	I	Low	**Acknowledge.** In the Centronics modes, this input is pulsed by the peripheral device to indicate that it has received the data and is ready to accept more data. The pin has an internal pull-up resistor attached to it.
	(EPINTR)	I	High	**EPP Interrupt.** In EPP mode, this signal is used by the peripheral device to interrupt the host.
	[PERCLK]	I	High	**Peripheral Clock.** In ECP mode, this signal is used in a closed-loop handshake with [HOSTACK] (pin 76) to transfer data or address information from the peripheral device to the host.
76	AUTOFD#	O	Low	**Automatic Feed.** In the Centronics modes, this active low output causes the printer to add a line feed after each line is printed. The pin should be provided with a pull-up resistor.
	(DSTRB#)	O	Low	**Data Strobe.** In EPP mode, the host uses this signal to denote a data cycle.
	[HOSTACK]	O	High	**Host Acknowledge.** When asserted in ECP mode, this signal requests a data byte from the peripheral device, handshaking with [PERCLK] (pin 62) in the reverse direction. In the forward direction, this signal also provides command information.
73	SLCTIN#	O	Low	**Select Input.** In the Centronics modes, this active low output selects the printer. A pull-up resistor should be provided on this pin.
	(ASTRB#)	O	Low	**Address Strobe.** In EPP mode, the host uses this signal to denote an address cycle. This pin is not used in ECP mode.

PARALLEL PORT PIN DESCRIPTIONS (*Continued*)

Pin Number	Pin Name	Type	Active Level	Description
74	INIT#	O	Low	**Initialize.** In the Centronics modes, this active low output initializes (resets) the printer. A pull-up resistor should be provided on this pin.
	(INIT#)	O	Low	**Initiate.** In EPP mode, the host uses this output to initiate a termination cycle to return the interface to the standard Centronics mode.
	[REVREQ#]	O	Low	**Reverse Request.** In ECP mode, the host uses this output to set the transfer direction (asserted = reverse; deasserted = forward).
74	INIT#	O	Low	**Initialize.** In the Centronics modes, this active low output initializes (resets) the printer. A pull-up resistor should be provided on this pin.
	(INIT#)	O	Low	**Initiate.** In EPP mode, the host uses this output to initiate a termination cycle to return the interface to the standard Centronics mode.
	[REVREQ#]	O	Low	**Reverse Request.** In ECP mode, the host uses this output to set the transfer direction (asserted = reverse; deasserted = forward).
59	SLCT	I	High	**Select.** The printer sets this input high when it is selected. SLCT has an internal pull-up resistor attached to it.
75	ERROR#	I	Low	**Error.** In the Centronics modes, the printer sets this input low when it detects an error. The pin has an internal pull-up resistor attached to it. This pin is not used in EPP mode.
	[PERREQ#]	I	Low	**Peripheral Request.** In ECP mode, the peripheral device drives this pin low to request a reverse transfer. The signal is usually used to generate an interrupt to the host.
60	PE	I	High	**Paper End.** In the Centronics modes, this input indicatesthat the printer is out of paper. The pin has an internal pull-up resistor attached to it. This pin is not used in EPP mode.
	(ACKREV#)	I	Low	**Acknowledge Reverse.** In ECP mode, the peripheral device drives this signal low to acknowledge a change in the direction of data transfer (asserted = forward).
96	DBDIR#	O	Low	**Host Data Bus Buffer Direction.** This active low signal indicates read cycles for 82C735 internal accesses.
	<PD>	O	High	**Power Down (alternate).** This signal goes high when the floppy disk controller is in powerdown mode.

FLOPPY DRIVE PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Active Level	Description
16	RDATA#	I	Low	**Read Data.** This Schmitt-trigger input reads raw data from the disk.
9	WDATA#	O	Low	**Write Data.** This output writes precompensated serial data to the selected drive and is gated internally with WGATE#. Precompensation is software selectable.
10	WGATE#	O	Low	**Write Gate.** This output signal enables the head of the selected disk drive to write to the disk.
4 3	DRV0# DRV1#	O O	Low Low	**Drive Select 0 and 1.** These signals are decoded drive select outputs for drives 0 and 1, respectively. They are controlled by bits D0 and D1 of the Digital Ouput Register (see "Floppy Drive Control (FDC) Registers"). Two drives can be supported directly when the 2-drive option is selected via bit 3 of CR05H (see "Configuration Registers"). When the 4-drive option is selected, these pins are encoded with information to control four floppy drives.
2 5	MTR0# MTR1#	O O	Low Low	**Motor Select 0 and 1.** These are motor enable outputs for drives 0 and 1, respectively. They are controlled by bits D4-D7 of the Digital Output Register (see "Floppy Drive Control (FDC) Registers"). Two drives can be supported directly when the 2-drive option is selected via bit 3 of CR05H (see "Configuration Registers"). When the 4-drive option is selected, these pins are encoded with information to control four floppy drives.
97	DRATE0	O	High	**Data Rate 0.** This totem-pole buffered output reflects the currently selected FDC data rate (bit 0 of the Configuration Control Register or the Data Rate Register, whichever was written to last). For additional register information, see "Floppy Drive Control (FDC) Registers."
17	DSKCHG	I	High	**Diskette Change.** This Schmitt-trigger input notifies the floppy drive controller that the disk drive door has been opened. The state of this pin is available from the Digital Input Register (see "Floppy Drive Control (FDC) Registers").
1	DENSEL	O	High	**Density Select.** This output indicates whether a low data rate (250/300Kbps) or a high data rate (500Kbps/1Mbps) has been selected.
7	DIR	O	High	**Direction.** This output signal controls the direction of the floppy disk drive head movement during a seek operation (low = step in; high = step out).
8	STEP#	O	Low	**Step.** This output signal supplies step pulses, at a software programmable rate, to move the head during a seek operation.
11	HDSEL	O	High	**Head Select.** This output determines the side of the floppy disk being accessed (low = side 0; high = side 1).
13	TRK0#	I	Low	**Track 0.** This Schmitt-trigger input indicates that the head of the selected floppy drive is on track zero.
14	WRPRT#	I	Low	**Write Protect.** This Schmitt-trigger input indicates that the disk in the selected drive is write-protected.
12	INDEX	I	High	**Index.** This Schmitt-trigger input indicates the beginning of a track.

CLOCK AND MISCELLANEOUS PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Active Level	Description
20	X1/CLK	I	High	**Crystal 1/Clock.** This pin is an external connection for a resonant 24MHz crystal. A TTL or CMOS compatible oscillator is connected to this pin if a crystal is not used.
21	X2	O	High	**Crystal 2.** This pin is the second connection for a 24MHz crystal. If an external clock is used, the pin is left unconnected.
58	PWRGD	I	High	**Power Good.** This input signal indicates that power (VCC) is valid. For the device to be operational, the signal must be active high. The 82C735 is fully functional when PWRGD is active. When Vcc is valid and PWRGD is inactive, the 82C735 is isolated from the rest of the circuit: all accesses are ignored, all inputs are disabled, and all outputs are tristated. However, the contents of all registers are preserved, and the current drain drops to standby current (Istby). An internal weak pull-up resistor is attached to this pin.
99	GAMECS#	O	Low	**Game Port Chip Select.** This pin is low when I/O address 201H is selected. The function of this pin is determined by bits 2 and 1 of CR05H (see "Configuration Registers").
	<DRATE1>	O	High	**Data Rate 1 (alternate).** This totem-pole buffered output reflects the current floppy drive controller data rate (bit 1 of the Configuration Control Register or the Data Rate Register, whichever was written to last). For additional register information, see "Floppy Drive Control (FDC) Registers."
	<IDLE>	O	High	**Idle (alternate).** This pin goes high when the floppy drive Idle state is selected.
15, 72 100	VCC			+5VDC digital power supply
6, 47 67, 98	GND			Ground

Register	Register Group	Register Name	Bits	Access	Port (Hex)	Alt Port	Alt Port	Alt Port	Index
CR00	Configuration	FDC / HDC Configuration	7	R/W	3F0-3F1h	–	–	–	00
CR01	Configuration	Serial / Parallel Configuration	8	R/W	3F0-3F1h	–	–	–	01
CR02	Configuration	Serial Pri / Sec Configuration	8	R/W	3F0-3F1h	–	–	–	02
CR03	Configuration	Serial Port Test Mode	4	R/W	3F0-3F1h	–	–	–	03
CR04	Configuration	Serial Port 2 Configuration	1	R/W	3F0-3F1h	–	–	–	04
CR05	Configuration	FDC Configuration	8	R/W	3F0-3F1h	–	–	–	05
CR06	Configuration	Mouse Configuration	2	R/W	3F0-3F1h	–	–	–	06
CR07	Configuration	Mouse Base Address	8	R/W	3F0-3F1h	–	–	–	07
CR08	Configuration	General Purpose Base Address	8	R/W	3F0-3F1h	–	–	–	08
CR09	Configuration	General Purpose Configuration	5	R/W	3F0-3F1h	–	–	–	09
DOR	FDC	Digital Output	8	R/W	3F2	372	–	–	n/a
MSR	FDC	Main Status	8	R	3F4	374	–	–	n/a
DSR	FDC	Data Rate Select	7	W	3F4	374	–	–	n/a
FIFO	FDC	Data (FIFO)	8	R/W	3F5	375	–	–	n/a
DIR	FDC	Digital Input	1	R	3F7	377	–	–	n/a
CCR	FDC	Configuration Control	2	W	3F7	377	–	–	n/a
HDATA	HDC	Data	8	R/W	1F0	170	–	–	n/a
HWCMP	HDC	Write Precomp	8	W	1F1	171	–	–	n/a
HERR	HDC	Error	6	R	1F1	171	–	–	n/a
HSC	HDC	Sector Count	8	W	1F2	172	–	–	n/a
HSN	HDC	Sector Number	8	R/W	1F3	173	–	–	n/a
HCL	HDC	Low Cylinder	8	R/W	1F4	174	–	–	n/a
HCH	HDC	High Cylinder	8	R/W	1F5	175	–	–	n/a
HDH	HDC	Drive Select / Head #	8	R/W	1F6	176	–	–	n/a
HCMD	HDC	Command	8	W	1F7	177	–	–	n/a
HSTAT	HDC	Status	8	R	1F7	177	–	–	n/a
HSTAT2	HDC	Alternate Status	8	R	3F6	376	–	–	n/a
HCTRL	HDC	Fixed Disk Control	3	W	3F7	377	–	–	n/a
HIN	HDC	Digital Input	8	R	3F7	377	–	–	n/a
DATA	Parallel (Cen,Bidir,EPP)	Data	8	R/W	278	378	3BC	–	n/a
DSR	Parallel (All)	Status	6	R	279	379	3BD	–	n/a
DCR	Parallel (All)	Control	6	R/W	27A	37A	3BE	–	n/a
EPPADDR	Parallel (EPP only)	Address	8	R/W	27B	37B	3BF	–	n/a
EPPDATA	Parallel (EPP Only)	Data	8	R/W	27C-27F	37C-37F	3C0-3	–	n/a
CFIFO	Parallel (Fast Cent Only)	Data FIFO	8	R/W	678	778	7BC	–	n/a
ECPAFIFO	Parallel (ECP Only)	Address FIFO	8	R/W	278	378	3BC	–	n/a
ECPDFIFO	Parallel (ECP Only)	Data FIFO	8	R/W	678	778	7BC	–	n/a
TFIFO	Parallel (Test)	Test FIFO	8	R/W	678	778	7BC	–	n/a
CFGA	Parallel (Config)	Configuration A	8	R	678	778	7BC	–	n/a
CFGB	Parallel (Config)	Configuration B	1	R/W	679	779	7BD	–	n/a
ECR	Parallel (All)	Extended Control	8	R/W	67A	77A	7BE	–	n/a
DLL	Serial (1 of 2 sets)	Divisor Latch LSB (DLAB=1)	8	R/W	Base+0	–	–	–	n/a
DLM	Serial (1 of 2 sets)	Divisor Latch MSB (DLAB=1)	8	R/W	Base+1	–	–	–	n/a
RBR	Serial (1 of 2 sets)	Rcv Buffer Reg (DLAB=0)	8	R	Base+0	–	–	–	n/a
THR	Serial (1 of 2 sets)	Xmt Holding Reg (DLAB=0)	8	W	Base+0	–	–	–	n/a
IER	Serial (1 of 2 sets)	Interrupt Enable (DLAB=0)	4	R/W	Base+1	–	–	–	n/a
IIR	Serial (1 of 2 sets)	Interrupt ID	6	R	Base+2	–	–	–	n/a
FCR	Serial (1 of 2 sets)	FIFO Control	6	W	Base+2	–	–	–	n/a
LCR	Serial (1 of 2 sets)	Line Control	8	R/W	Base+3	–	–	–	n/a
MCR	Serial (1 of 2 sets)	Modem Control	5	R/W	Base+4	–	–	–	n/a
LSR	Serial (1 of 2 sets)	Line Status	8	R/W	Base+5	–	–	–	n/a
MSR	Serial (1 of 2 sets)	Modem Status	8	R/W	Base+6	–	–	–	n/a
SCR	Serial (1 of 2 sets)	Scratchpad	8	R/W	Base+7	–	–	–	n/a
	COM1 Base Address			Base:	3F8	–	–	–	n/a
	COM2 Base Address			Base:	2F8	–	–	–	n/a
	COM3 Base Address			Base:	338	3E8	2E8	220	n/a
	COM4 Base Address			Base:	238	2E8	2E0	228	n/a
MSPDR	Mouse	Mouse Data	8	R/W	(CR07*4)+0	–	–	–	n/a
MPSR	Mouse	Mouse Status	8	R/W	(CR07*4)+1	–	–	–	n/a
GPSEL	General Purpose	General Purpose Select	8	R/W	(CR08*4)+(GPLSB*2)		–	–	n/a

Registers

CONFIGURATION REGISTERS

The ten read/write configuration registers are configurable by software. Two consecutive I/O addresses, one even and one odd, are used to select and access the registers (see "Configuration Procedures"under "Configuration Registers"). These addresses should not conflict with any other devices. By IBM PC convention, the address range 3F0H to 3F7H is reserved for the floppy disk controller (FDC). In the 82C735, address range 3F0H to 3F1H can be used for configuring the system.

The configuration registers do not have to be initialized if the default values are used for normal operation. The registers are set to the default state only upon power-up and are not affected by the RESET signal. Settings are retained as long as power to the chip is maintained.

SERIAL PORT REGISTERS

The 82C735 provides two identical serial port (UART) register sets, one for each channel. The register descriptions provided in the section "Serial Port Registers" apply to both sets of UART registers.

The base address of all registers is software programmable during the configuration sequence. Serial port registers are located at sequentially increasing addresses above the base address.

MOUSE PORT REGISTERS

The mouse port has two registers for communication with a PS/2 style mouse: the Mouse Port Data Register and the Mouse Port Status Register. The base address for the mouse port registers is CR07H x 4. This address must be set in Configuration Register CR07H before the mouse port can be enabled and powered up (CR06H, bits 1 and 0). The Secondary Serial Port must be disabled and powered down (CR02H, bits 7 and 6).

HARD DISK CONTROLLER REGISTERS

The Hard Disk Controller (HDC) registers communicate data, command, and status information to the AT host. The output of Hard Disk Chip Select 0 (HDCS0#) is active when I/O address space 1F0H to 1F7H (170H to 177H if secondary) is chosen. The output of Hard Disk Chip Select 1 (HDCS1#) is active when address space 3F6H to 3F7H (376H to 377H if secondary) is chosen. Additional information can be obtained from IBM AT technical reference manuals.

PARALLEL PORT (PRINTGINE) REGISTERS

The 82C735 parallel port is equivalent to a generic parallel port interface and may be operated in standard and bidirectional as well as extended modes. The modes supported by the registers vary, depending on the Mode field bits in the Extended Control Register. See the parallel port register descriptions ("Parallel Port (Printgine) Registers") for the mode field dependencies. Operation of the device in modes other than those specified in this data sheet is undefined. All of the parallel port register addresses are based on the standard LPT addresses: 278H, 378H, and 3BCH.

FLOPPY DRIVE CONTROL REGISTERS

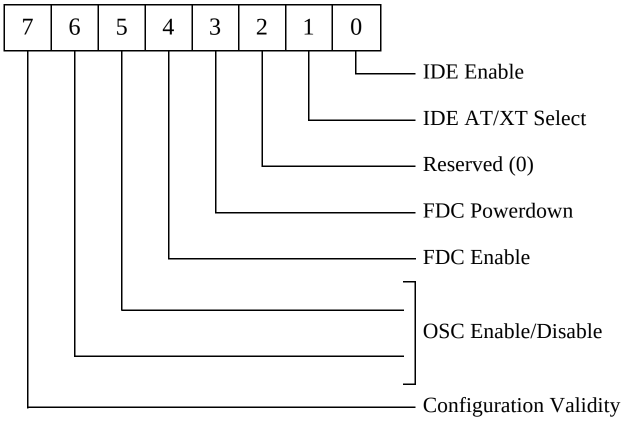
The Floppy Drive Control (FDC) registers are mapped onto the addresses shown in the register summary table provided under "Floppy Drive Control (FDC) Registers." The base address range is provided by the on-chip address decoder pin. The primary address range is 3F0H to 3F7H, and the secondary address range is 370H to 377H.

Configuration Registers

Register Mnemonic	Register Name	Index (hex)	Access	Address Range (hex)	Default State (hex)	Page
CR00	Configuration Register 0	00	R/W	3F0-3F1	3F	26
CR01	Configuration Register 1	01	R/W	3F0-3F1	9F	27
CR02	Configuration Register 2	02	R/W	3F0-3F1	DC	28
CR03	Configuration Register 3	03	R/W	3F0-3F1	00	28
CR04	Configuration Register 4	04	R/W	3F0-3F1	01	29
CR05	Configuration Register 5	05	R/W	3F0-3F1	00	29
CR06	Configuration Register 6	06	R/W	3F0-3F1	X1	30
CR07	Configuration Register 7	07	R/W	3F0-3F1	XX	30
CR08	Configuration Register 8	08	R/W	3F0-3F1	XX	31
CR09	Configuration Register 9	09	R/W	3F0-3F1	00	31

CONFIGURATION REGISTER CR00H

Read/Write at Address 3F0H-3F1H
Default: 3FH



0 IDE Enable

0 IDE disabled
1 IDE enabled (default)

1 IDE AT/XT Select

0 IDE XT type
1 IDE AT type (default)

2 Reserved (0)

3 FDC Powerdown

0 FDC powerdown
1 FDC powerup (default)

4 FDC Enable

0 FDC disabled
1 FDC enabled (default)

6-5 Oscillator Enable/Disable

The following table defines the possible values for these two bits.

Bits		
6	**5**	**Function**
0	0	Oscillator always ON
0	1	Oscillator ON; BR generator ON when PWRGD active, otherwise OFF (default)
1	0	Oscillator ON; BR generator ON when PWRGD active, otherwise OFF
1	1	Oscillator always OFF

0 Oscillator ON; baud rate generator clock enabled. In this state, the oscillator and baud rate generator clock are always enabled. They are not shut off when the PWRGD pin becomes inactive.

1 Oscillator ON; baud rate generator clock enabled. In this state, the oscillator is ON and the baud rate generator clock is enabled as long as the PWRGD pin is active. When PWRGD becomes inactive, the clock and baud rate generator are turned off.

2 Oscillator ON; baud rate generator clock enabled. In this state, the oscillator is ON and the baud rate generator clock is enabled as long as the PWRGD pin is active. When PWRGD becomes inactive, the clock and baud rate generator are turned off.

3 Oscillator OFF; baud rate generator clock disabled.

7 Configuration Validity

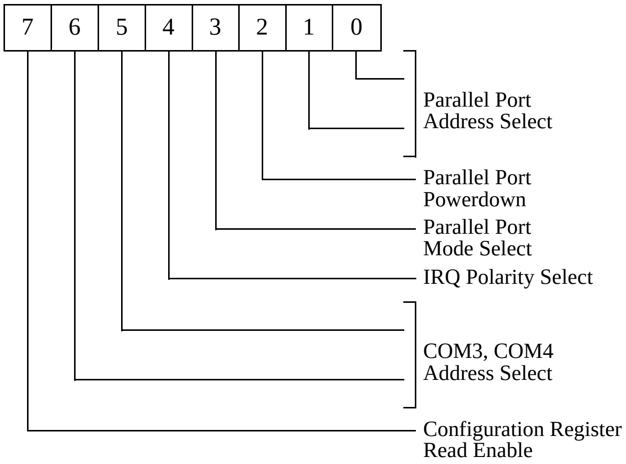
This bit indicates that a valid configuration cycle has taken place. The configuration software should set this bit to 1 after it has initialized the required configuration registers.

0 Invalid Configuration (default on powerup). UPC has power but the registers are not fully initialized. RESET has no effect.

1 Valid Configuration. Configuration software has initialized all necessary registers since the last time power was applied to the UPC**.**

CONFIGURATION REGISTER CR01H

Read/Write at Address 3F0H-3F1H
Default: 9FH


7
6
5
4
3
2
1
0
Parallel Port Address Select
Parallel Port Powerdown
Parallel Port Mode Select
IRQ Polarity Select
COM3, COM4 Address Select
Configuration Register Read Enable

1-0 Parallel Port Address Select

00	Disabled
01	3BCH
10	378H
11	278H (default)

2 Parallel Port Powerdown

0	Parallel port powerdown
1	Parallel port powerup (default)

3 Parallel Port Mode Select

0	Bidirectional mode enable
1	Printer unidirectional mode (default)

Bidirectional mode has to be selected for all the enhanced modes: fast Centronics, EPP, and ECP.

4 IRQ Polarity Select

0	IRQ active low; inactive hi-Z
1	IRQ active high; inactive low (default)

Note that when IRQ is active high, IRQ output is low when it is inactive. When IRQ is active low, IRQ output is tristated when it is inactive. This allows interrupt sharing.

6-5 COM3, COM4 Address Select

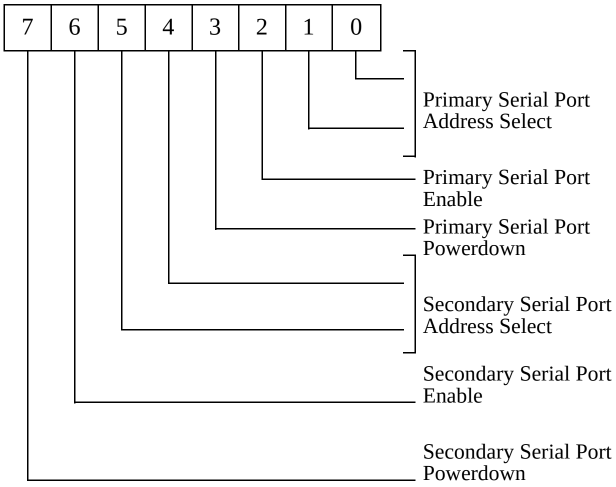
	COM3 (hex)	COM4 (hex)
00 (default)	338	238
01	3E8	2E8
10	2E8	2E0
11	220	228

7 Configuration Registers Read Enable

0	Disable reading of registers
1	Enable reading of registers (default)

CONFIGURATON REGISTER CR02H

Read/Write at Address 3F0H-3F1H
Default: DCH


7
6
5
4
3
2
1
0
Primary Serial Port Address Select
Primary Serial Port Enable
Primary Serial Port Powerdown
Secondary Serial Port Address Select
Secondary Serial Port Enable
Secondary Serial Port Powerdown

1-0 Primary Serial Port Address Select

00	COM1, 3F8H (default)
01	COM2, 2F8H
10	COM3, depending on bits 6 and 5 of CR01H
11	COM4, depending on bits 6 and 5 of CR01H

2 Primary Serial Port Enable

0	Disabled
1	Enabled (default)

3 Primary Serial Port Powerdown

0	Serial port powerdown
1	Serial port powerup (default)

5-4 Secondary Serial Port Address Select

00	COM1,3F8H
01	COM2,2F8H (default)
10	COM3, depending on bits 6 and 5 of CR01H
11	COM4, depending on bits 6 and 5 of CR01H

6 Secondary Serial Port Enable

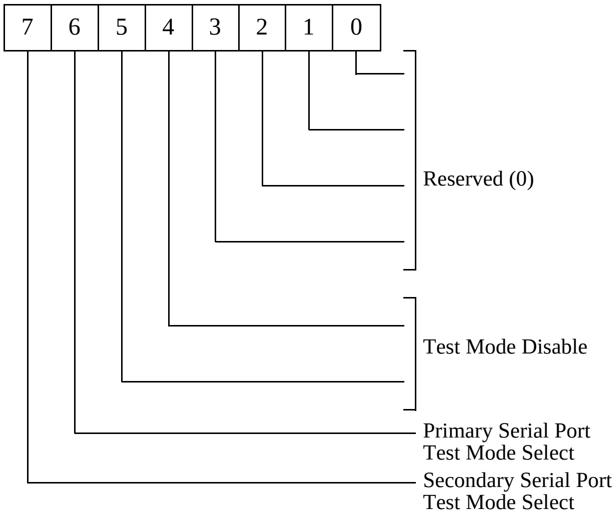
0	Disabled
1	Enabled (default)

7 Secondary Serial Port Powerdown

0	Serial port powerdown
1	Serial port powerup (default)

CONFIGURATION REGISTER CR03H

Read/Write at Address 3F0H-3F1H
Default: 00H


7
6
5
4
3
2
1
0
Reserved (0)
Test Mode Disable
Primary Serial Port Test Mode Select
Secondary Serial Port Test Mode Select

3-0 Reserved (0)

5-4 Test Mode Disable

00	Normal mode; test disabled (default)
01	Reserved
10	Reserved
11	Reserved

6 Primary Serial Port Test Mode Select

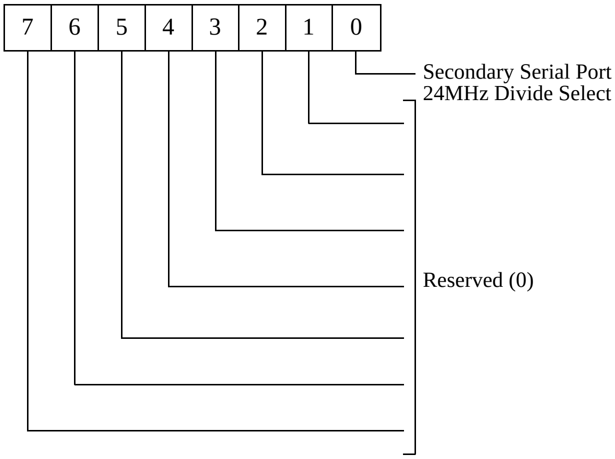
0	Normal mode (default)
1	Test mode

7 Secondary Serial Port Test Mode Select

0	Normal mode (default)
1	Test mode

CONFIGURATION REGISTER CR04H

Read/Write at Address 3F0H-3F1H
Default: 01H



0 Secondary Serial Port 24MHz Divide Select

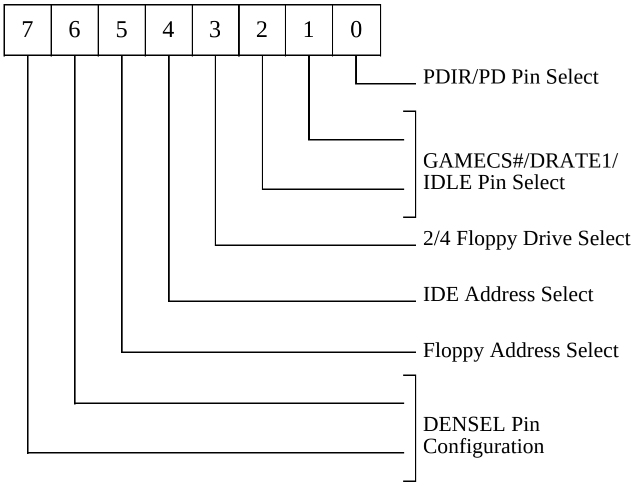
0 Divide by 12
1 Divide by 13 (default)

Note: MIDI operates at 31.25 Kbaud, which can be derived from 125KHz (24MHz/12 = 2MHz; 2MHz/16 = 125KHz).

7-1 Reserved (0)

CONFIGURATION REGISTER CR05H

Read/Write at Address 3F0H-3F1H
Default: 00H



0 DBDIR#/PD Pin Select (Pin 96)

0 DBDIR# select (default)
1 PD select

2-1 GAMECS#/DRATE1/IDLE Pin Select (Pin 99)

00 GAMECS# select (default)
01 DRATE1 select
10 IDLE select
11 Reserved

3 Two or Four Floppy Drive Select

0 Two drive select (default)
1 Four drive select

4 IDE Address Select

0 IDE1 select 1F0H-1F7H, 3F6H, 3F7H (default)
1 IDE2 select 170H-177H, 376H, 377H

5 Floppy Address Select

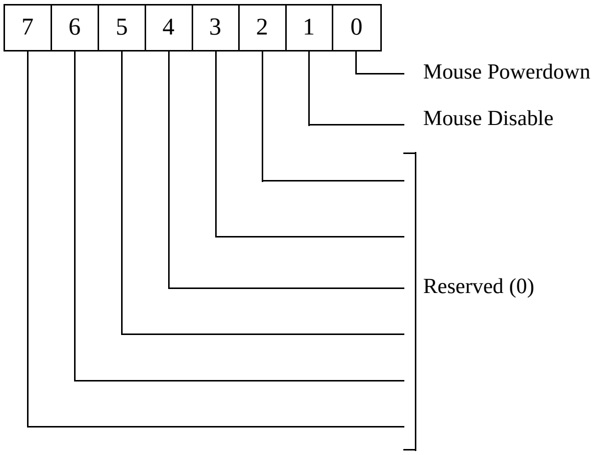
0 FDC 1 select 3F0H-3F7H (default)
1 FDC 2 select 370H-377H

7-6 Density Select (DENSEL) Pin Configuration

00 High for 500Kbps/1Mbps, low for 250/300Kbps (default)
01 DENSEL pin always low
10 DENSEL pin always high
11 DENSEL low for 500Kbps/1Mbps, high for 250/300Kbps

CONFIGURATION REGISTER CR06H

Read/Write at Address 3F0H-3F1H
Default: X1H



0 Mouse Powerdown

0 Mouse powerup
1 Mouse powerdown (default)

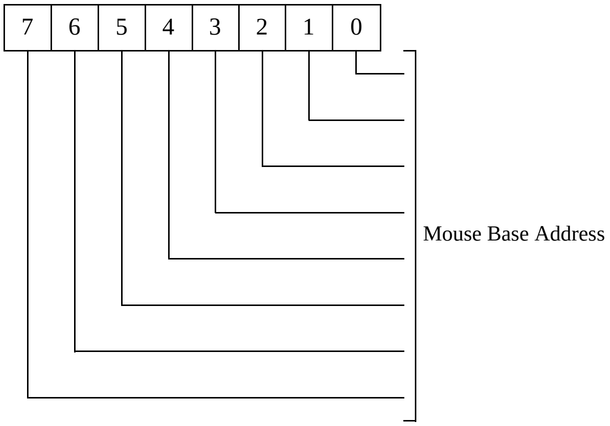
1 Mouse Disable

0 Mouse disabled (default)
1 Mouse enabled

7-2 Reserved (0)

CONFIGURATION REGISTER CR07H

Read/Write at Address 3F0H-3F01H
Default: XXH

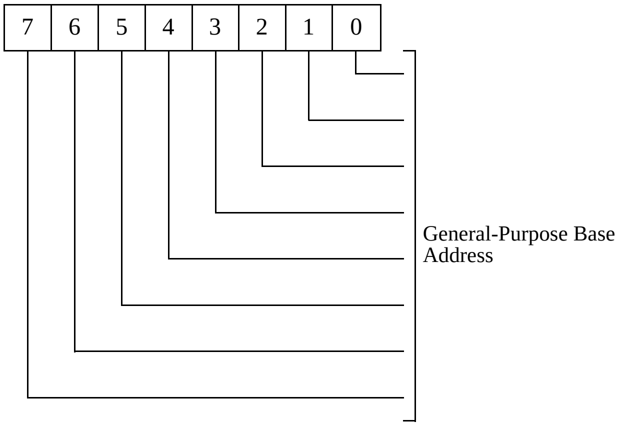


7-0 Mouse Base Address Register

The base address, CR07H x 4, must be programmed before the mouse port can be enabled (CR06H, bit 1). Also, the mouse must be powered up (CR06H, bit 0) and the secondary serial port must be disabled and powered down (CR02H, bits 7 and 6).

CONFIGURATION REGISTER CR08H

Read/Write at Address 3F0H-3F01H
Default: XXH

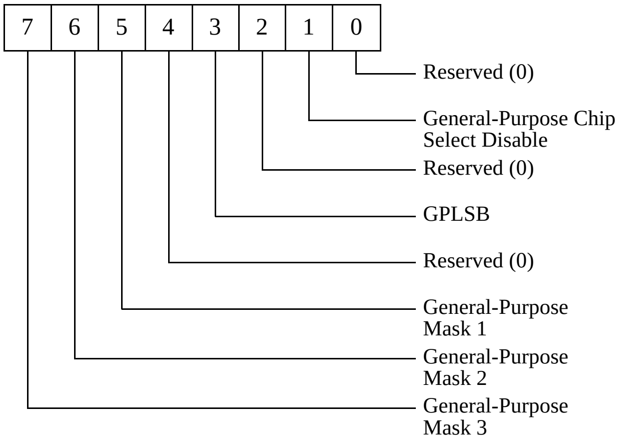


7-0 General-Purpose Base Address Register

The base address, CR08H x 4, must be programmed before the general-purpose chip select can be enabled (CR09H, bit 1). In addition, the secondary serial port must be disabled and powered down (CR02H, bits 7 and 6) before this function can be used.

CONFIGURATION REGISTER CR09H

Read/Write at Address 3F0H-3F1H
Default: 00H



0 Reserved (0)

1 General-Purpose Chip Select Disable

0 Enabled
1 Disabled (default)

2 Reserved (0)

3 General-Purpose LSB (GPLSB)

Base address is (CR08H x 4) + (GPLSB x 2)

4 Reserved (0)

5 General-Purpose Mask 1

0 Do not mask (default)
1 Mask general-purpose least significant bit (GPLSB) (not used in decoding)

6 General-Purpose Mask 2

0 Do not mask (default)
1 Mask CR08H, bit 0 (not used in decoding)

7 General-Purpose Mask 3

0 Do not mask (default)
1 Mask CR08H, bit 1 (not used in decoding)

CONFIGURATION PROCEDURES

Configuration is accomplished in three basic steps:

1. Enter configuration mode.
2. Configure the 82C735.
3. Escape from configuration mode.

Any deviation from this sequence causes the configuration state machine to return to its initial idle state. The configuration procedure is intentionally complicated to prevent an errant program from making accidental changes to the chip configuration.

Enter Configuration Mode

Write two consecutive writes of value 55H to port 3F0H. The following is an example in 8086 assembly language:

```
MOV    DX,3F0H    ;Port address
MOV    AL,55H     ;Data
OUT    DX,AL
OUT    DX,AL      ;In configuration mode
```

Configure the Chip

The ten configuration registers can be written to or read. To write data to the registers:

1. Write <*CR0nH*> to port 3F0H

   where: <*CR0nH*> is the register to be configured.

2. Write <*data*> to 3F1H

   where: <*data*> is the data to be written into the register that port 3F0H points to.

To read data from the registers:

1. Set bit 7 of CR01H to 1 to enable reading.

2. Write <*CR0nH*> to port 3F0H

   where: <*CR0nH*> is the register to be configured.

3. Read data from 3F1H.

Example 1:

Access CR00H to turn on the oscillator and enable the FDC and IDE:

```
MOV    DX,3F0H    ;Access CR00H
MOV    AL,00H
OUT    DX,AL
MOV    DX,3F1H
MOV    AL,0BFH    ; set necessary bits
OUT    DX,AL
```

Example 2:

Access CR02H to set serial port 1 to COM 1 and serial port 2 to COM 3 in normal mode:

```
MOV    DX,3F0H    ;Access CR02H
MOV    AL,02H
OUT    DX,AL
MOV    DX,3F1H
MOV    AL,0EAH
OUT    DX,AL
```

Escape Configuration Mode

Write AAH value in port 3F0H as follows:

```
MOV    DX,3F0H
MOV    AL,0AAH
OUT    DX,AL      ;Out of configuration mode
```

Sample Program

The following 8086 assembly language program enters configuration mode, configures the 82C735, and escapes configuration mode.

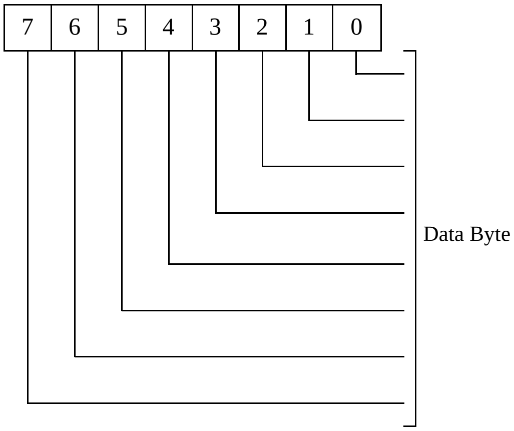
```
;Enter configuration mode:
MOV    DX,3F0H    ;Port address
MOV    AX,55H     ;Data
OUT    DX,AL
OUT    DX,AL

;Configure the 82C735:
MOV    DX,3F0H    ;Access CR00H
MOV    AL,00H
OUT    DX,AL
MOV    DX,3F1H
MOV    AL,0BFH    ;Set necessary bits
OUT    DX,AL
MOV    DX,3F0H    ;Access CR02H
MOV    AL,02H
OUT    DX,AL
MOV    DX,3F1H
MOV    AL,0EAH
OUT    DX,AL

;Escape configuration mode:
MOV    DX,3F0H
MOV    AL,0AAH
OUT    DX,AL
```

Serial Port Registers

Register Mnemonic	Register Name	Offset (hex)	Access	Address (hex) Base Address Options: COM1, COM2: 3F8, 2F8 COM3, COM4: 338, 3E8, 2E8, 220 238, 2E8, 2E0, 228				Page
				DLAB	A2	A1	A0	
RBR	Receive Buffer	0	R	0	0	0	0	34
THR	Transmit Buffer	0	W	0	0	0	0	34
IER	Interrupt Enable	1	R/W	0	0	0	1	35
IIR	Interrupt ID	2	R	0	0	1	0	36
FCR	FIFO Control	2	W	0	0	1	0	37
LCR	Line Control	3	R/W	X	0	1	1	38
MCR	Modem Control	4	R/W	X	1	0	0	40
LSR	Line Status	5	R/W	X	1	0	1	41
MSR	Modem Status	6	R/W	X	1	1	0	42
SCR	Scratchpad	7	R/W	X	1	1	1	42
DLM	Divisor Latch MSB	1	R/W	1	0	0	1	43
DLL	Divisor Latch LSB	0	R/W	1	0	0	0	43

RECEIVE BUFFER REGISTER

Read Only
Offset = 0H, DLAB = 0

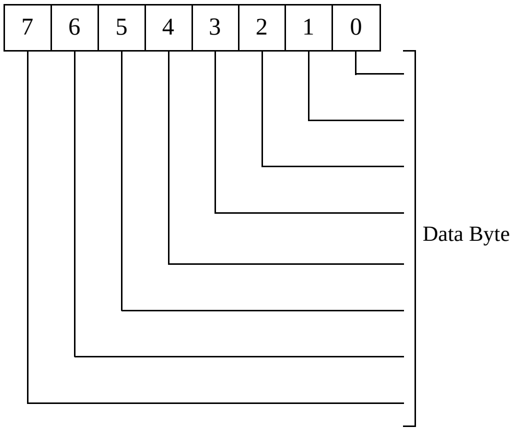


This register holds the incoming data byte. Bit 0, the Least Significant Bit (LSB), is received first. The data is initially assembled in the Receiver Shift Register (not user accessible) before it is loaded into the Receive Buffer or Receiver FIFO.

7-0 Incoming Data Byte

TRANSMIT BUFFER REGISTER

Write Only
Offset = 0H, DLAB = 0

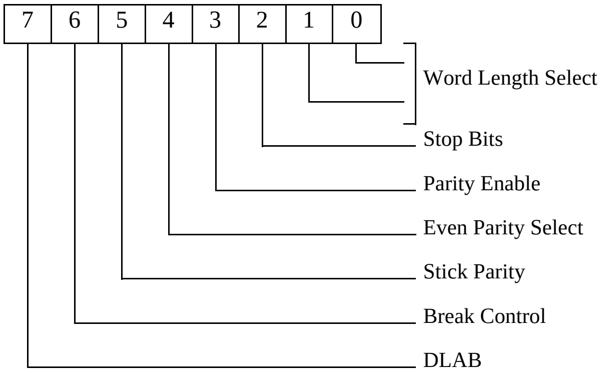


This register holds the data byte to be sent to the host. Bit 0, the Least Significant Bit (LSB), is transmitted first. The data is loaded into the Transmit Shift Register (not user accessible) from the Transmit Register or Transmitter FIFO. This byte is then transmitted to the TXD pin.

7-0 Outgoing Data Byte

LINE CONTROL REGISTER

Read/Write
Offset = 3H, DLAB = X



The Line Control Register (LCR) is used to specify the format of the asynchronous data communications exchange and to set the divisor latch access bit.

1-0 Word Length Select

Bits 1 and 0 specify the number of data bits in each transmitted or received serial character.

LCR BITS 0 AND 1 ENCODING

Bit 1	Bit 0	Data Length (bits)
0	0	5
0	1	6
1	0	7
1	1	8

2 Number of Stop Bits

Bit 2 specifies the number of stop bits transmitted with each serial character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If it is a logic 1 when a 5-bit data length is selected, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.

3 Parity Enable

When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of bits when the data bits and the parity bit are summed.)

4 Even Parity Select

When parity is enabled and bit 4 is a logic 0, an odd number of logic 1s are transmitted or checked in the data word bits and parity bit. When parity is enabled and bit 4 is a logic 1, an even number of logic 1s are transmitted or checked.

5 Stick Parity

When parity is enabled, bit 5 is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are logic 1, the parity bit is transmitted and checked as a logic 0 (space parity). If bits 3 and 5 are 1 and bit 4 is a logic 0, then the parity bit is transmitted and checked as a logic 1 (mark parity). If bit 5 is a logic 0, stick parity is disabled.

6 Break Control

This bit causes a break to be transmitted to the receiving UART and allows the CPU to alert a terminal. When the bit is set to a logic 1, the serial output (TXD) is forced to the spacing state (logic 0). The break is disabled by setting the bit to a logic 0. The break control bit acts only on TXD and has no effect on the transmitter logic.

The break will not cause erroneous characters to be transmitted if the following sequence is used:

1. Wait for the transmitter to be idle (TEMT = 1).
2. Set the break for the appropriate amount of time. If the transmitter will be used to time the break duration, check that TEMT = 1 before clearing the break control bit.
3. Clear the break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer, establishing the break duration accurately by sending characters and monitoring THRE and TEMT (see Line Status Register bits 5 and 6).

7 Divisor Latch Access Bit (DLAB)

Bit 7 must be set to a logic 1 to access the divisor latches of the baud rate generator during a read or write operation. It must be set to a logic 0 to access any register.

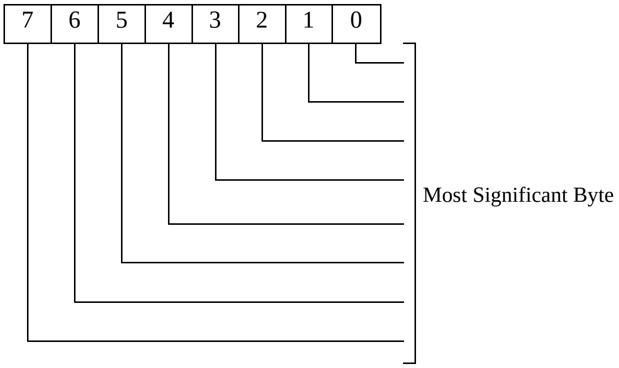
The UART reset configuration is shown on the following page.

UART RESET CONFIGURATION

Register/Signal	Reset Control	Reset State
Interrupt Enable	Master Reset	0000 0000
Interrupt Identification	Master Reset	0000 0001
FIFO Control	Master Reset	0000 0000
Line Control	Master Reset	0000 0000
Modem Control	Master Reset	0000 0000
Line Status	Master Reset	0110 0000
Modem Status	Master Reset	XXXX 0000
TXD	Master Reset	High
Interrupt (Receiver Errors)	Read LSR/MR	Low/Tristate
Interrupt (Receiver Data Ready)	Read RBR/MR	Low/Tristate
Interrupt (THRE)	Read IIR/Write THR/MR	Low/Tristate
Interrupt (Modem Status Changes)	Read MSR/MR	Low/Tristate
Interrupt Enable Bit	Master Reset	Low
RTS	Master Reset	High
DTR	Master Reset	High
RCVR FIFO	MR/FCR1.FCR0/FCR0	All bits low
XMIT FIFO	MR/FCR1.FCR0/FCR0	All bits low

DIVISOR LATCH MSB REGISTER

Read /Write
Offset = 1H, DLAB = 1



The 82C735 contains two independently programmable baud rate generators. The 24MHz crystal oscillator frequency input is divided by 13, resulting in a frequency of 1.8462MHz. This frequency is sent to each baud rate generator and divided by the divisor of the associated UART. The output frequency of the baud rate generator is 16 x the baud rate:

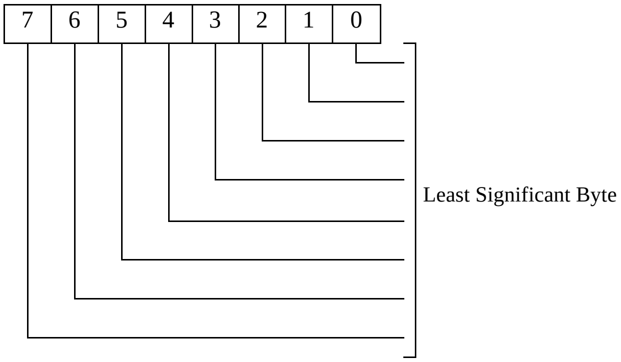
divisor # = (frequency input/baud rate x 16)

The output of each baud rate generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud rate generator. Upon loading either of the divisor latches, a 16-bit baud counter is loaded. The Divisor, Baud Rates, and Clock Frequencies table shows the decimal divisors for use with crystal frequencies of 24MHz.

The oscillator input to the chip should always be 24MHz to ensure that the floppy disk controller timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

DIVISOR LATCH LSB REGISTER

Read /Write
Offset = 0H, DLAB = 1

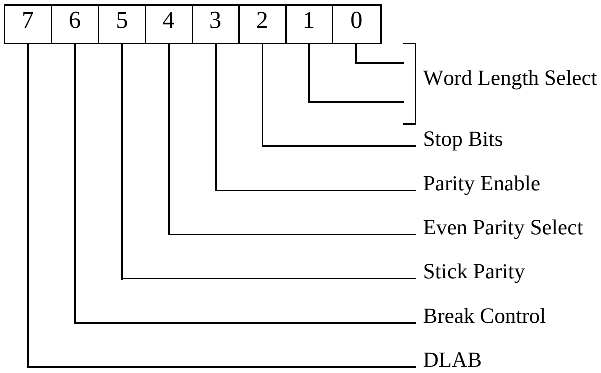


DIVISORS, BAUD RATES, AND CLOCK FREQUENCIES

	24MHz Input Divided to 1.8462MHz	
Baud Rate	**Decimal Divisor for 16X Clock**	**0.2% Error except as noted**
50	2304	0.1
75	1536	—
110	1047	—
134.5	857	0.4
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.5
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	3.0

LINE CONTROL REGISTER

Read/Write
Offset = 3H, DLAB = X



The Line Control Register (LCR) is used to specify the format of the asynchronous data communications exchange and to set the divisor latch access bit.

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Bits 1 and 0 specify the number of data bits in each transmitted or received serial character.

LCR BITS 0 AND 1 ENCODING

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This bit causes a break to be transmitted to the receiving UART and allows the CPU to alert a terminal. When the bit is set to a logic 1, the serial output (TXD) is forced to the spacing state (logic 0). The break is disabled by setting the bit to a logic 0. The break control bit acts only on TXD and has no effect on the transmitter logic.

The break will not cause erroneous characters to be transmitted if the following sequence is used:

1. Wait for the transmitter to be idle (TEMT = 1).
2. Set the break for the appropriate amount of time. If the transmitter will be used to time the break duration, check that TEMT = 1 before clearing the break control bit.
3. Clear the break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer, establishing the break duration accurately by sending characters and monitoring THRE and TEMT (see Line Status Register bits 5 and 6).

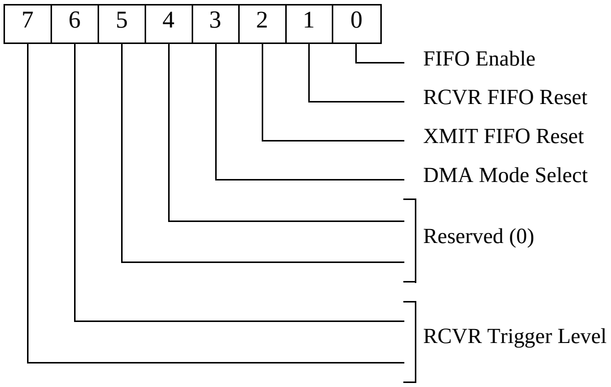
7 Divisor Latch Access Bit (DLAB)

Bit 7 must be set to a logic 1 to access the divisor latches of the baud rate generator during a read or write operation. It must be set to a logic 0 to access any register.

The UART reset configuration is shown on the following page.

FIFO CONTROL REGISTER

Write Only
Offset = 2H, DLAB = 0



This write-only register is at the same location as the Interrupt Identification Register, a read-only register. The FIFO Control Register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signaling

0 FIFO Enable

Writing a 1 to this bit enables both the XMIT and RCVR FIFOs. Resetting the bit clears all bytes in both FIFOs. When a change is made from FIFO mode to NS16450 mode, or vice-versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to, or they will not be programmed.

1 RCVR FIFO Reset

Writing a 1 to this bit clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 written to this bit position is self-clearing.

2 XMIT FIFO Reset

Writing a 1 to bit 2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 written to this bit position is self-clearing.

3 DMA Mode Select

Writing to bit 3 causes no change in UART operations.

Note: TXRDY# and RXRDY# are not available in the 82C735.

5-4 Reserved (0)

7-6 RCVR Trigger Level

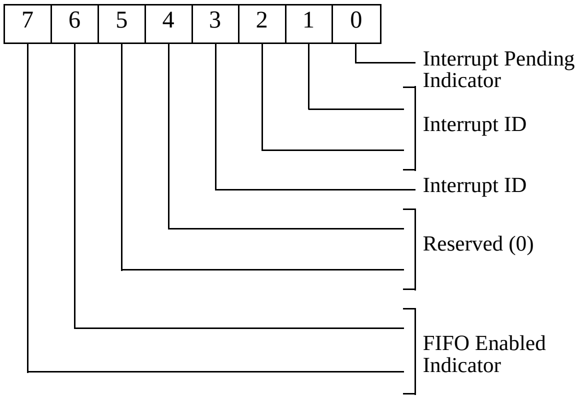
These bits designate the interrupt trigger level and are the MSB and LSB, respectively. When the number of bytes in the RCVR FIFO equals the designated interrupt trigger level, a Received Data Available interrupt is activated. This interrupt must be enabled by setting bit 0 of the Interrupt Enable Register.

RCVR FIFO TRIGGER LEVELS

FCR Bit		Trigger Level (bytes)
7	**6**	
0	0	01
1	0	04
0	1	08
1	1	14

INTERRUPT IDENTIFICATION REGISTER

Read Only
Offset = 2H , DLAB = 0



To provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register (IIR). The four levels of interrupt conditions in order of priority are

1. Receiver line status
2. Received data ready
3. Transmitter holding register empty
4. Modem status

When the CPU accesses the IIR register, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, the UART records new interrupts, but it does not change its current indication until the current access is complete.

0 Interrupt Pending Indicator

Bit 0 can be used in an interrupt environment to indicate whether an interrupt condition is pending. When this bit is a logic 0, an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

2-1 Interrupt ID

Bits 2 and 1 are used to identify the highest priority interrupt pending, as indicated in the IIR Control Functions table.

3 Interrupt ID

In the NS16450 mode this bit is 0. In the FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending (see the IIR Control Functions table on the following page).

5-4 Reserved (0)

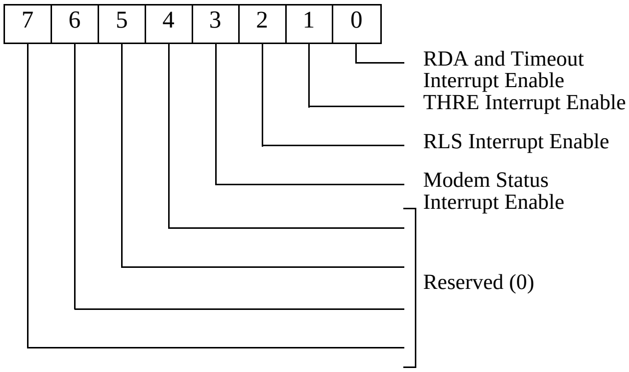
These bits are always logic 0.

7-6 FIFO Enabled Indicators

These two bits are set when FCR0 = 1 (FIFO mode enabled).

INTERRUPT ENABLE REGISTER

Read/Write
Offset = 1H, DLAB = 0


7
6
5
4
3
2
1
0
RDA and Timeout Interrupt Enable
THRE Interrupt Enable
RLS Interrupt Enable
Modem Status Interrupt Enable
Reserved (0)

The Interrupt Enable Register (IER) enables the five types of UART interrupts. Each interrupt can individually activate the appropriate interrupt output signal (IRQ3 or IRQ4). Setting bits of this register to a logic 1 enables the selected interrupt(s). Resetting bits 3-0 totally disables the interrupt system. Disabling an interrupt prevents it from being indicated as active in the Interrupt Identification Register and from activating the interrupt output signal.

All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status registers. For more information on enabling the interrupt pin, see the the Modem Control Register, bit 3.

0 Received Data Available (RDA) and Timeout Interrupt Enable

When set to logic 1, this bit enables the RDA and Timeout interrupts in FIFO mode.

1 Transmitter Holding Register Empty (THRE) Interrupt Enable

When set to logic 1, this bit enables the THR Empty interrupt.

2 Received Line Status (RLS) Interrupt Enable

When set to logic 1, this bit enables the RLS interrupt.

3 Modem Status Interrupt Enable

When set to logic 1, this bit enables the Modem Status interrupt.

7-4 Reserved (0)

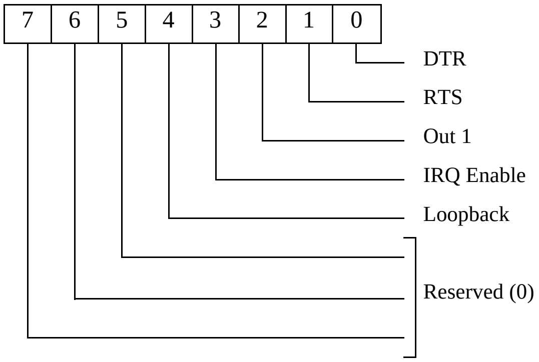
These bits are always logic 0.

INTERRUPT ENABLE REGISTER CONTROL FUNCTIONS

Bit Number				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
3	2	1	0				
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver line status	Overrun error, parity error, framing error, or break interrupt	Reading LSR register
0	1	0	0	Second	Received data available	Receiver data available	Read receiver buffer
1	1	0	0	Second	Character timeout indication	No characters removed from or input to RCVR FIFO during last character times, and at least one character in FIFO.	Reading RBR register
0	0	1	0	Third	THR register empty	THR register empty	Reading IIR register if interrupt source, or writing to THR register
0	0	0	0	Fourth	Modem status	Clear to send, data set ready, ring indicator, or data carrier detect	Reading modem status register

MODEM CONTROL REGISTER

Read/Write
Offset = 4H, DLAB = X



This register controls the interface with the modem, data set, or peripheral device emulating a modem.

0 Data Terminal Ready (DTR)

Bit 0 controls the DTR# output. When bit 0 is set to a logic 1, the DTR# output is forced to a logic 0. When it is reset to a logic 0, the DTR# output is forced to a logic 1. In logical loopback mode, this bit controls bit 5 of the MSR register.

Note: The DTR# and RTS# outputs of the UART may be applied to an EIA inverting line driver to obtain the proper polarity input at the modem or data set.

1 Request to Send (RTS)

This bit controls the RTS# output in the same way that bit 0 controls the DTR# output. In local loopback mode, this bit controls bit 4 of the MSR register.

2 Out 1

This bit does not have an output pin associated with it. It can be written to and read by the CPU. In local loopback mode, OUT1 controls bit 6 of the MSR register.

3 IRQ Enable

When set, bit 3 enables the interrupt. No external pin is associated with this bit other than IRQ 3 and 4. In local loopback mode, this bit controls bit 7 of the Modem Status Register (MSR).

4 Loopback

Bit 4 provides a local loopback feature for diagnostic testing of the UART. When the bit is set to logic 1, the following occur:

1. Transmitter serial output (TXD) is set to the marking (logic 1) state.
2. Receiver serial input (RXD) is disconnected.
3. Output of the transmitter holding register (THR) is ‘‘looped back’’ (connected) to the receiver buffer register (RBR).
4. Modem control inputs DSR#, CTS#, RI#, and DCD# are disconnected.
5. MCR enable bits DTR, RTS, OUT1, and IRQ are internally connected to MSR bits DSR, CTS, RI, and DCD, respectively.

The modem control output pins are forced to their high (inactive) states. In loopback mode, transmitted data is immediately received, allowing the processor to verify the transmit-and-received-data paths of the serial port.

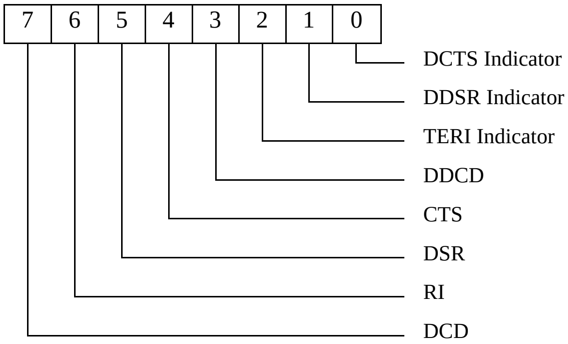
In loopback mode, receiver and transmitter interrupts are fully operational, but the sources of the interrupts are the lower four bits of the MCR register instead of the four modem control inputs. Writing a 1 to any of these four bits causes an interrupt, which is controlled by the Interrupt Enable Register. The IRQ3 and four pins are tristated.

7-5 Reserved (0)

Theses bits are permanently set to logic 0.

MODEM STATUS REGISTER

Read /Write
Offset = 6H, DLAB = X



The MCR shows the current state of the control lines from the modem or peripheral device to the CPU. Four of the bits provide change data. These bits are set to 1 when a control input from the modem changes state, and are reset to 0 when the CPU reads the MSR.

0 Delta Clear to Send (DCTS) Indicator

Indicates that the CTS# input to the chip has changed state since the last reading.

1 Delta Data Set Ready (DDSR) Indicator

Indicates that the DSR# input has changed state since the last reading.

2 Trailing Edge of Ring Indicator (TERI)

Indicates that the RI# input has changed from a low to a high state.

3 Delta Data Carrier Detect (DDCD) Indicator

Indicates that the DCD# input has changed state.

Note: Setting bit 0, 1, 2, or 3 to a logic 1 generates a modem status interrupt.

4 Clear to Send (CTS)

Complement of the CTS# input. If the MCR loopback bit (bit 4) is set to a 1, this bit is equivalent to RTS in the MCR.

5 Data Set Ready (DSR)

Complement of the DSR# input. If MCR bit 4 is set to 1, this bit is equivalent to DTR in the MCR.

6 Ring Indicator (RI)

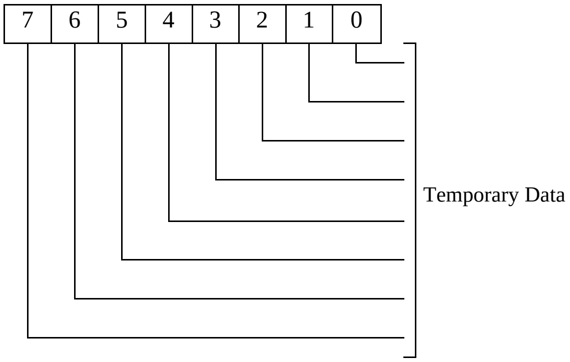
Complement of the RI# input. If MCR bit 4 is set to a 1, this bit is equivalent to OUT1 in the MCR.

7 Data Carrier Detect (DCD)

Complement of the DCD# input. If MCR bit 4 is set to 1, this bit is equivalent to IRQ enable (bit 3) in the MCR.

SCRATCHPAD REGISTER

Read/Write
Offset = 7H, DLAB = X



This eight-bit register does not control the UART in any way. Its purpose is to hold data temporarily.

FIFO INTERRUPT MODE OPERATION

Each serial channel has two 16-byte FIFOs associated with it. The operational description that follows is applicable to the FIFOs of both channels.

When the RCVR FIFO and Received Data Available Interrupt bits are enabled (FCR0 = 1, IER0 = 1) Received Data Available interrupts occur. The Received Data Available interrupt is issued to the CPU when the number of bytes in the RCVR FIFO equals the programmed trigger level. It is cleared as soon as the number of bytes in the RCVR FIFO drops below the trigger level.

The Received Data Available indication from the Interrupt Identification Register also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

The Receiver Line Status interrupt (IIR = 06), as before, has higher priority than the Received Data Available interrupt (IIR = 04).

The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the RCVR FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO Timeout interrupts can occur if the following conditions exist:

- At least one character is in the RCVR FIFO.
- The most recent serial character was received more than four continous character times ago. (If two stop bit s are programmed, the second one is included in thi s time delay.)
- The most recent CPU read of the RCVR FIFO was received more than four continuous character time ago.

The maximum time between a received character and a timeout interrupt is 160ms at 300 baud, with a 12-bit receive character (i.e., 1 START, 8 DATA, 1 PARITY, and 2 STOP bits). Character times are calculated by using the baud rate generator clock as the clock signal. This makes the delay proportional to the baud rate.

A timeout interrupt is cleared and the timer reset when the CPU reads one character from the RCVR FIFO. When the timeout interrupt indication is inactive, the timeout indication timer is reset after a new character is received or atfer the CPU reads the RCVR FIFO.

Transmit (XMIT) interrupts can occur when the XMIT FIFO interrupts are enabled (FCR0 = 1, IER1 = 1). The Transmitter Holding Register Empty (THRE) interrupt occurs when the XMIT FiFO is empty. It is cleared as soon as the IIR register is read or the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while this interrupt is being serviced).

Transmitter FIFO empty indications are delayed one character time minus the last stop bit time whenever THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFo since the last THRE = 1. This delay prevents the UART from issuing a second THRE interrupt as soon as it transfers the first character into the transmitter shift register. The first THRE interrupt occurs immediately after FCR0 is changed, assuming FCR0 is enabled.

Character Timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt. XMIT FIFO Empty has the same priority as the current THRE interrupt.

FIFO Polled Operation

With FCR0 = 1, resetting any or all of bits 3:0 of the Interrupt Enable Register puts the associated serial channel in the FIFO polled mode of operation. Since the receiver and transmitter are controlled seperately, either one or both can be in the polled mode of operation. In this mode, your program will check receiver and transmitter status via the LSR.

- LSR0 is set as long as there is one byte in the RCVR FIFO.
- LSR1 to LSR4 specifies which error(s) has occurred. Character error status is handled the same way as in the interrupt mode.
- LSR5 indicates when the XMIT FIFO is empty.
- nLSR6 indicates that both the XMITFIFO and shift register are empty.
- LSR7 indicates whether there are any errors in the RCVR FIFO.

In the FIFo polled mode, no trigger level reached or timeout condition is incicated; however, the RCVR and XMIT FIFOs are otherwise functional.

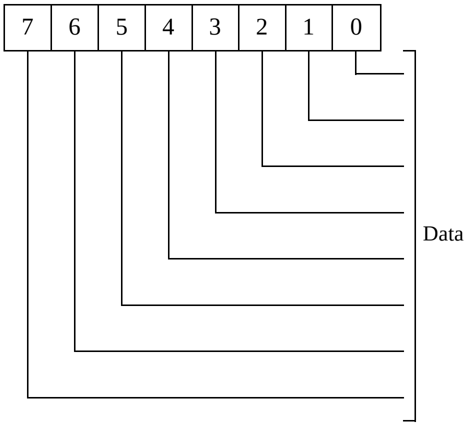
Mouse Port Registers

Register Mnemonic	Register Name	Offset (hex)	Access	Address (hex) (see Note)	Page
MSPDR	Mouse Port Data Register	0	R/W	CR07 x 4	46
MSPSR	Mouse Port Status Register	1	R/W	CR07 x4	46

Note: Address may be programmed in configuration register CR07H; however, the base address is normally 3104.

MOUSE PORT DATA REGISTER

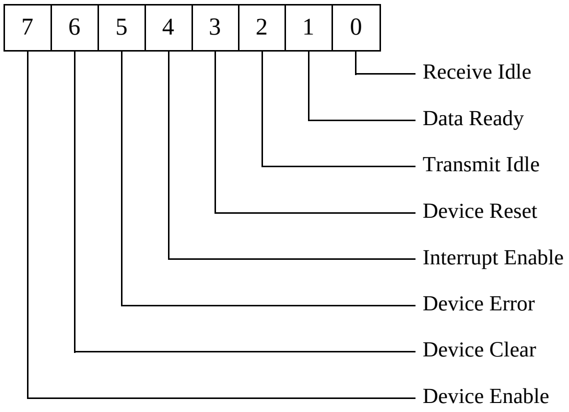
Read/Write at Address CR07H x 4,
Offset = 0H



The eight-bit Mouse Port Data Register (MSPDR) transfers data between the host and the mouse. The host sends command and data bytes to the data register on the MDATA line, using the MCLK as the synchronizing signal. The register converts status and other data from the mouse into 8-bit bytes and transfers the data to the host via the serial MDATA line.

MOUSE PORT STATUS REGISTER

Read/Write at Address CR07H x 4,
Offset = 1H



0 Receive Idle

Mouse port sets this bit to 1 when the receive buffer is empty. When the bit is 0, the host can read from the MSPDR.

1 Data Ready

Mouse port sets this bit to 1 when the MSPDR has a data byte for the host. The bit is reset after the host reads the data register.

2 Transmit Idle

Mouse port sets this bit to 1 when the host transmits data to the MSPDR on the MDATA line. When the bit is 0, the host should not write to the MSPDR.

3 Device Reset

A 1 resets the the mouse port. Set to 0 for normal operation.

4 Interrupt Enable

Host sets this bit to 1 to enable the mouse interrupt. The mouse port interrupts the host when the mouse has data or the transmit buffer is empty. This bit is cleared on reading or writing to the MSPDR. A 0 disables the mouse interrupt.

5 Device Error

Host sets this bit to 1 when a data transmission error (e.g., parity error) occurs. The mouse port must be reset and cleared for further operation.

6 Device Clear

Host sets this bit to 1 to clear all receive and transmit buffers. This bit must be set to 0 when transmitting or receiving data.

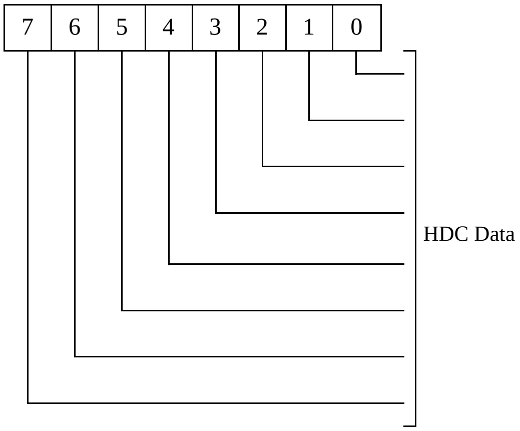
7 Device Enable

Host sets this bit to 1 to enable clocking to the pointing device. A 0 disables clocking. This bit must be enabled when the mouse is in use.

Hard Disk Controller (HDC) Registers

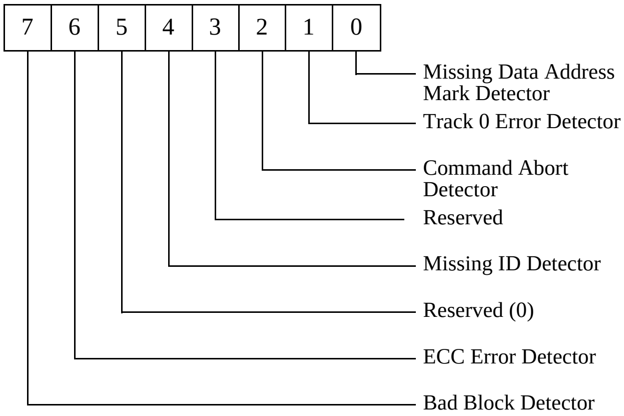
Register Mnemonic	Register Name	Access	Primary Address (hex)	Secondary Address (hex)	Page
HDATA	Data	R/W	1F0	170	48
HERR	Error	R	1F1	171	48
HWCMP	Write Compensation	W	1F1	171	49
HSC	Sector Count	W	1F2	172	49
HSN	Sector Number	R/W	1F3	173	50
HCL	Low Cylinder	R/W	1F4	174	50
HCH	High Cylinder	R/W	1F5	175	51
HDH	Drive Select/Head Number	R/W	1F6	176	51
HSTAT	Status	R	1F7	177	52
HCMD	Command	W	1F7	177	52
HSTAT2	Alternate Status	R	3F6	376	53
HCTRL	Fixed Disk Control	W	3F6	376	53
HIN	Digital Input	R	3F7	377	54

DATA REGISTER
Read/Write at Primary Address 1F0H
Secondary Address 170H



The data register provides an 8 or 16-bit data path to the IDE disk drive. This register handles all data transfers between the host and the hard disk.

ERROR REGISTER
Read Only at Primary Address 1F1H
Secondary Address 171H



This register contains the status of the last executed command.

0 **Missing Data Address Mark Detector**

Set to 1 if the data address mark is not found.

1 **Track 0 Error Detector**

Set to 1 if a track 0 error is detected.

2 **Command Abort Detector**

Set to 1 if a command is aborted.

3 **Reserved (0)**

4 **Missing ID Detector**

Set to 1 if the ID is not found.

5 **Reserved (0)**

6 **ECC Error Detector**

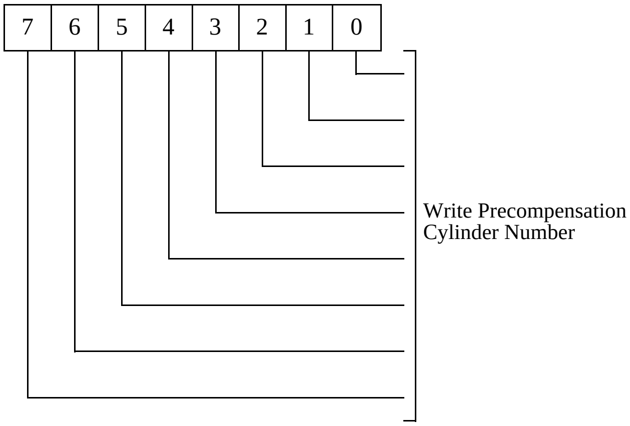
Set to 1 if a data ECC error occurred.

7 **Bad Block Detector**

Set to 1 if a bad block is detected.

WRITE COMPENSATION REGISTER

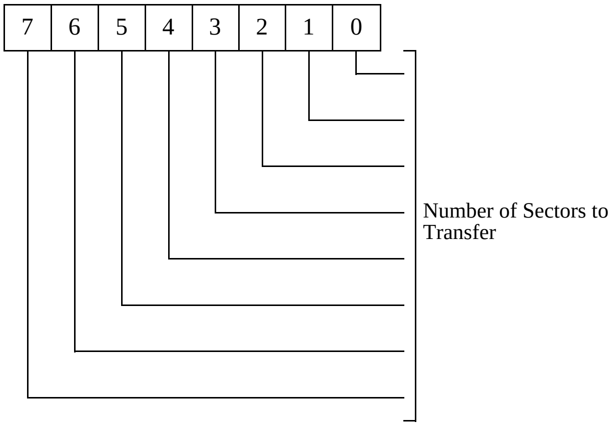
Write Only at Primary Address 1F1H
Secondary Address 171H



This register is written to by the host. It usually contains the number of the cylinder where the write precompensation is to be used.

SECTOR COUNT REGISTER

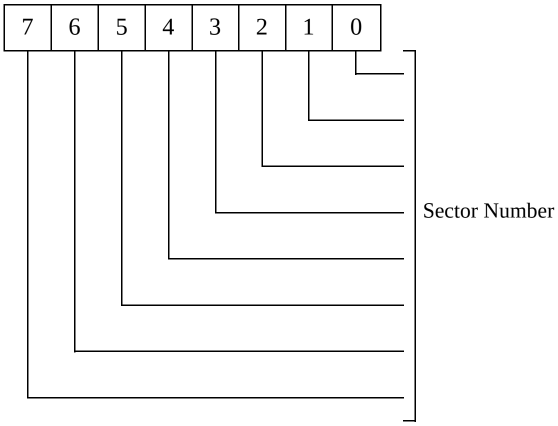
Write Only at Primary Address 1F2H
Secondary Address 172H



This register contains the number of sectors to be transferred during a VERIFY, READ, WRITE, or FORMAT command (see "FDC Command Set" for command descriptions). A 0 value means a 256 sector transfer.

SECTOR NUMBER REGISTER

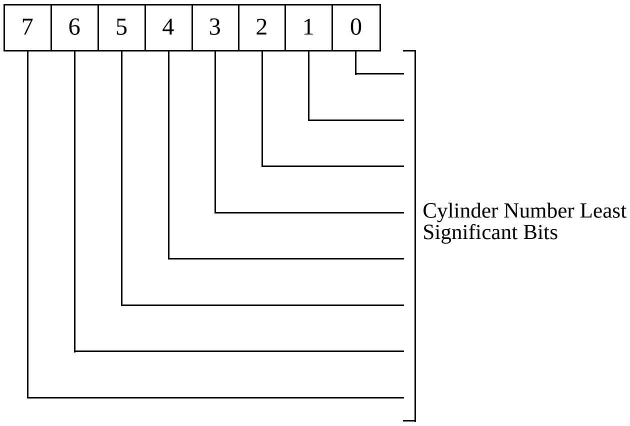
Read/Write at Primary Address 1F3H
Secondary Address 173H



The Sector Number Register contains the sector number for disk accesses during READ, WRITE, and VERIFY commands (see "FDC Command Set" for command descriptions).

LOW CYLINDER NUMBER REGISTER

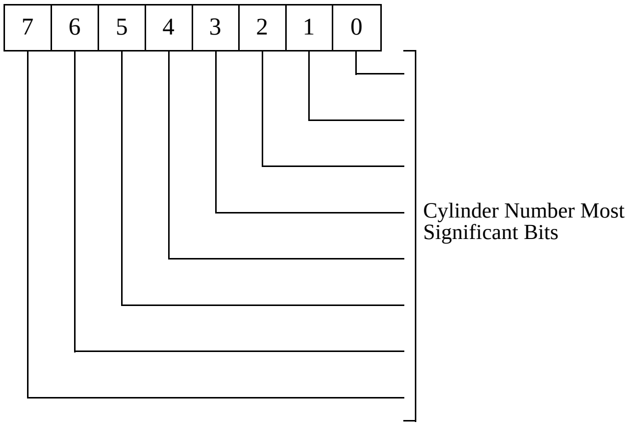
Read/Write at Primary Address 1F4H
Secondary Address 174H



This register contains the eight least significant bits (LSB) of the desired cylinder number.

HIGH CYLINDER NUMBER REGISTER

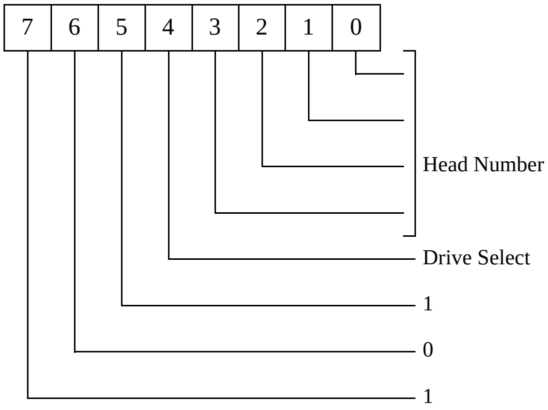
Read/Write at Primary Address 1F5H
Secondary Address 175H



This register contains the eight most significant bits (MSB) of the desired cylinder number.

DRIVE SELECT/HEAD NUMBER REGISTER

Read/Write at Primary Address 1F6H
Secondary Address 176H



3-0 Head Number

These bits constitute a four-bit binary number that represents the head number (bit 3 = MSB; bit 0 = LSB).

4 Drive Select

0 Primary
1 Secondary

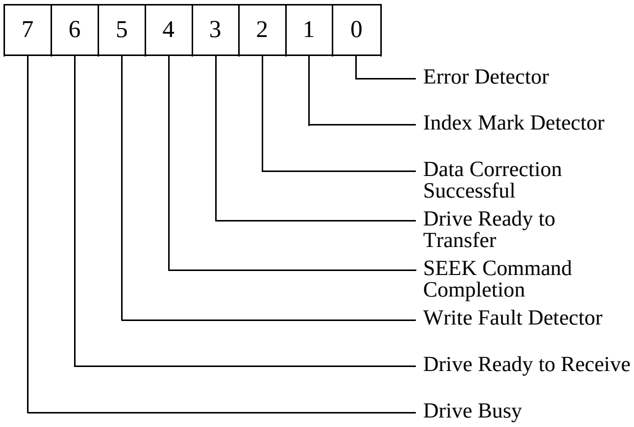
5 Set to 1.

6 Set to 0.

7 Set to 1.

STATUS REGISTER

Read Only at Primary Address 1F7H
Secondary Address 177H



The status register contains the status of the drive.

0 Error Detector

Set to 1 if an error from the last command is detected.

1 Index Mark Detector

Set to 1 if an index mark is detected.

2 Data Correction Successful

Set to 1 if data correction is sucessful.

3 Drive Ready to Transfer

Set to 1 if the drive is ready to transfer data.

4 SEEK Command Completion

Set to 1 if a SEEK command is completed.

5 Write Fault Detector

Set to 1 if a write fault condition occurred.

6 Drive Ready to Receive

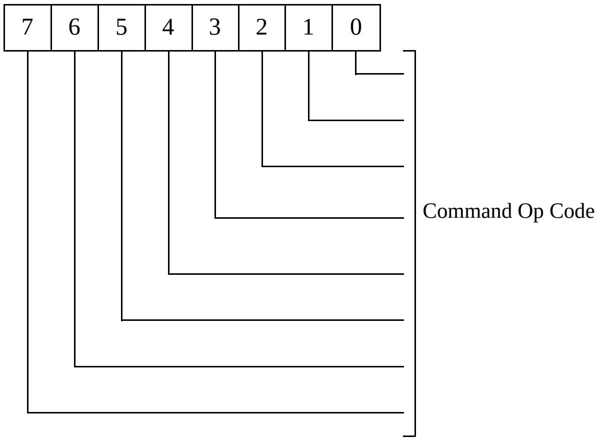
Set to 1 if the drive is ready to accept a command.

7 Drive Busy

Set to 1 if the drive is busy.

COMMAND REGISTER

Write Only at Primary Address 1F7H
Secondary Address 177H



This register contains the command op code for fixed disk operation. The IDE drive executes the specified command when written by the host.

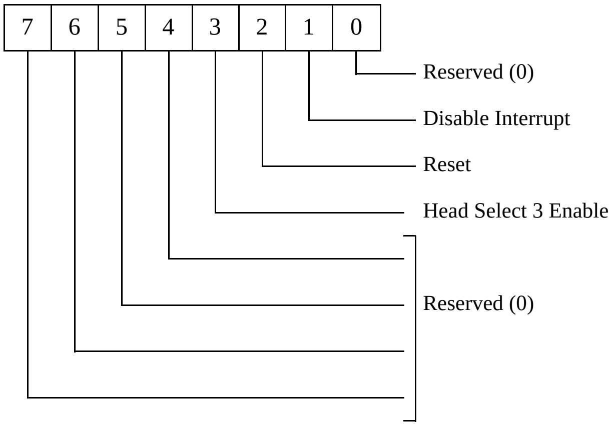
ALTERNATE STATUS REGISTER

Read Only at Primary Address 3F6H
Secondary Address 376H

This register contains the same status information as the Status Register (1F7H, 177H). However, reading this register does not clear the interrupt to the host processor, whereas reading the Status Register does clear the interrupt.

FIXED DISK CONTROL REGISTER

Write Only at Primary Address 3F6
Secondary Address 376H



0 Reserved (0)

1 Interrupt Disable

0 Enable interrupt
1 Disable interrupt (default)

2 Reset

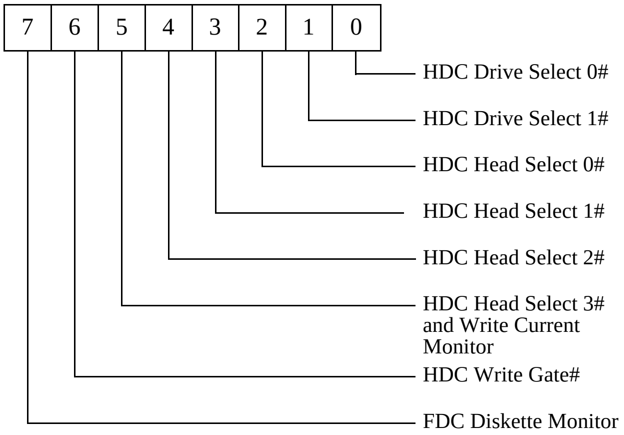
0 Normal operation (default)
1 Generate software reset to HDC bit 1 (IRQEN#)

3 Head Select 3 Enable

7-4 Reserved (0)

DIGITAL INPUT REGISTER

Read Only at Primary Address 3F7H
Secondary Address 377H



This register contains information from the Drive Select/Head Number Register.

0 HDC Drive Select 0#

Indicates that the primary drive is selected.

1 HDC Drive Select 1#

Indicates that the secondary drive is selected.

2 HDC Head Select 0#

Contains bit 0 of the four-bit binary head number.

3 HDC Head Select 1#

Contains bit 1 of the four-bit binary head number.

4 HDC Head Select 2#

Contains bit 2 of the four-bit binary head number.

5 HDC Head Select 3# and Reduced Write Current Monitor

Contains bit 3 of the four-bit binary head select number and detects a reduction in write current.

6 HDC Write Gate#

7 FDC Diskette Change Status

The host reads this bit to determine the floppy disk controller status.

Parallel Port (Printgine) Registers

Register Mnemonic	Register Name	Index (hex)	Access	Address (hex) Base Address: 278, 378, 3BC	Mode (see Note)	Page
DATA	Data	0x000	R/W (byte)	LPT +0	0,1,4	56
DSR	Status	0x001	R (byte)	LPT +1	All	56
DCR	Control	0x002	R/W (byte)	LPT +2	All	57
eppAddr	EPP Address	0x003	R/W (byte)	LPT +3	4	58
eppData	EPP Data	0x004:7	R/W (byte)	LPT +4:7	4	58
cFifo	Fast Centronics Data FIFO	0x400	R/W (word)	LPT +400	2	59
ecpAFifo	ECP Address FIFO	0x000	R/W (byte)	LPT +0	3	59
ecpDFifo	ECP Data FIFO	0x400	R/W (word)	LPT +400	3	60
TFifo	Test FIFO	0x400	R/W (word)	LPT +400	5	60
CnfgA	Configuration A	0x400	R	LPT +400	6	61
CnfgB	Configuration B	0x401	R/W	LPT +401	6	61
ECR	Extended Control	0x402	R/W	LPT +402	All	62

Note: 0 = Centronics

1 = Bidirectional

2 = Fast Centronics (FIFO)

3 = ECP

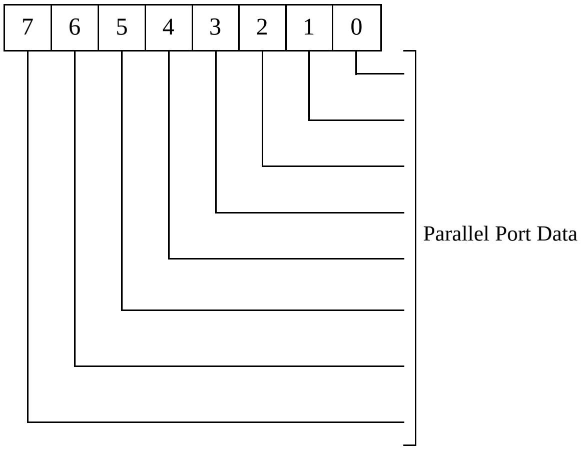
4 = EPP

5 = Test

6 = Configuration

DATA REGISTER

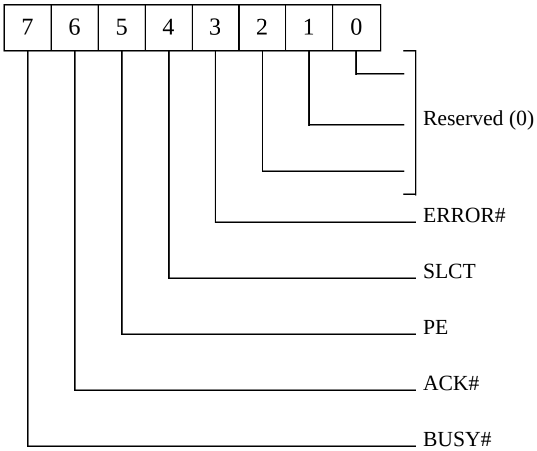
Read/Write Byte at LPT +0H in Centronics, Bi-di, and EPP Modes



The parallel port data register (DATA) is a bidirectional, 8-bit data port. Data written to this register is transmitted to the printer; data read to it is the data on the connector. This port is 100-percent compatible with the IBM PC/AT parallel port.

STATUS REGISTER

Read Only Byte at LPT +1H in All Modes



The parallel port status register (DSR) is a read-only register that provides the status of the pins described below.

2-0 Reserved (0)

3 ERROR#

This bit reflects the inverted state of the ERROR# input pin. A 0 signifies that an error has been detected

4 SLCT

The Select bit reflects the state of the SLCT input pin. A 1 indicates that the printer is on-line; a 0 indicates that the printer is not selected.

5 PE

The Paper End bit reflects the state of the PE input pin. A 1 means that the printer is out of paper.

6 ACK#

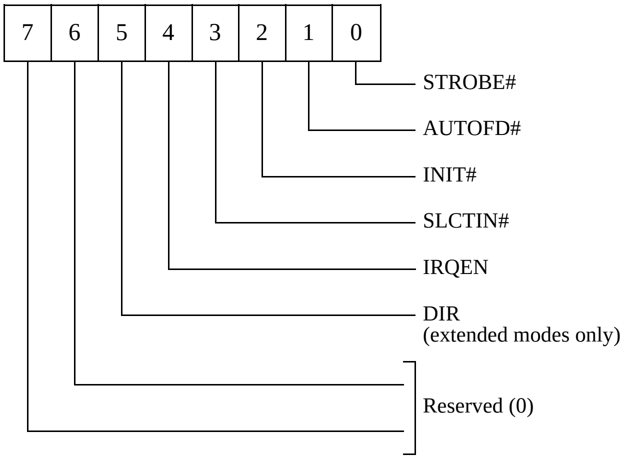
The Acknowledge bit reflects the state of the ACK# input pin. A 0 indicates that the printer has received a character and is ready to accept another. A 1 indicates that the printer is busy with the last character sent or has not received data.

7 BUSY#

This bit reflects the state of the BUSY# input pin. A 0 signifies that the printer is busy and cannot accept new data. A 1 indicates that the printer is ready to accept new data.

DATA CONTROL REGISTER

Read/Write Byte at LPT +2H in All Modes



The parallel port Data Control Register (DCR) provides all output control signals to the printer.

0 STROBE#

Controls the Data Strobe output to the printer (inverse of STROBE#). A 1 generates the active low pulse (50µs min.) that clocks data into the printer. A 0.5µs data setup time delay is required before STROBE# can be asserted.

1 AUTOFD#

Controls the Automatic Feed output to the printer (inverse of AUTOFD#). A 1 generates an automatic line feed at the end of each line.

2 INIT#

Controls the INIT# output to the printer. A 0 generates the active low pulse (50µs min.) that initializes the printer.

3 SLCTIN#

Drives the Select Input signal to select the printer (inverse of SLCTIN#). A 1 selects the printer.

4 IRQEN#

Enables parallel port interrupts in response to a transition of the printer ACK# signal from active to inactive. A 1 enables interrupts; a 0 disables all interrupts and clears all pending interrupts.

5 DIR

Controls parallel port direction in extended modes (bit 6 of CR01H =1). In these modes:

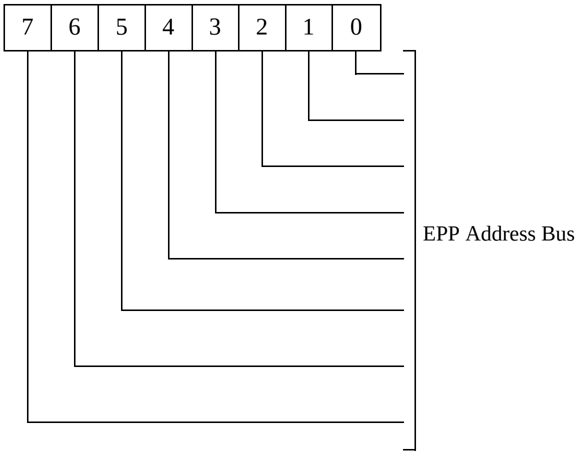
0	Forward direction (output/write condition)
1	Reverse direction (input/read condition)

In printer mode, the direction is always out, regardless of the state of this bit.

7-6 Reserved (0)

EPP ADDRESS REGISTER

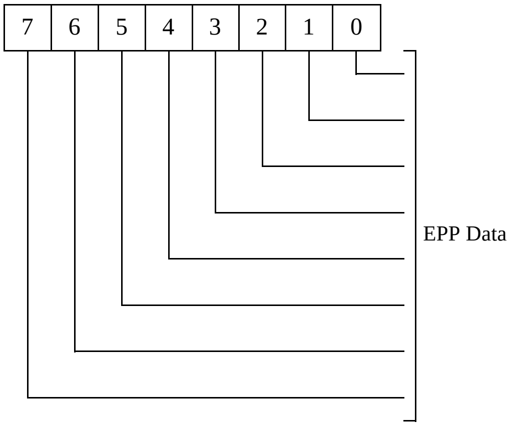
Read/Write Byte at LPT +3H
in EPP Mode



The read/write EPP Address Register (eppAddr) is valid only in EPP mode. The system writes to this register to select an EPP device on the parallel port bus. Writing to this register automatically generates an address strobe on the control signal.

EPP DATA REGISTER

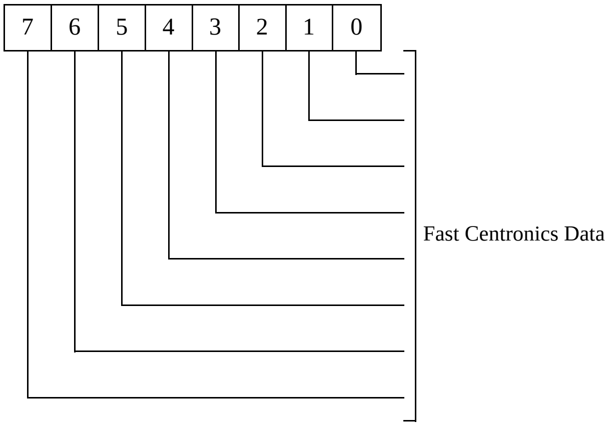
Read/Write Byte at LPT +4:7H
in EPP Mode



The EPP Data Register (eppData) is valid in EPP mode only. The system uses this register to transfer data to and from an EPP device.

FAST CENTRONICS DATA FIFO REGISTER

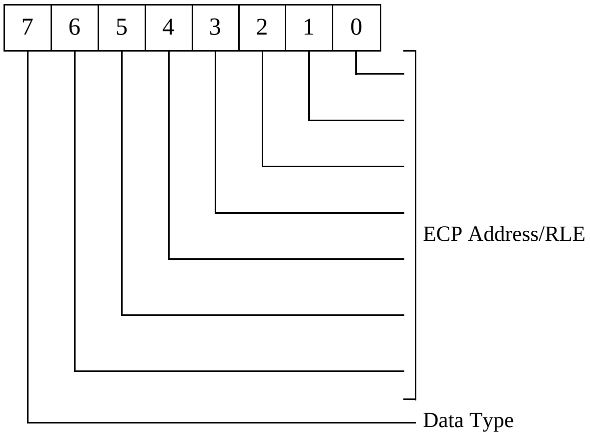
Read/Write Word at LPT +400H in
Fast Centronics Mode Only



The Fast Centronics Data FIFO (cFifo) receives 8-bit programmed I/O or DMA data from the system and transfers it to the peripheral device using a hardware handshake in Fast Centronics mode.

ECP ADDRESS FIFO REGISTER

Read/Write Byte at LPT +0H in
ECP Mode Only



6-0 Address or RLE Field

Bit 7 defines these bits as either the ECP address or the RLE field. The RLE indicates the number of times the next data byte will appear:

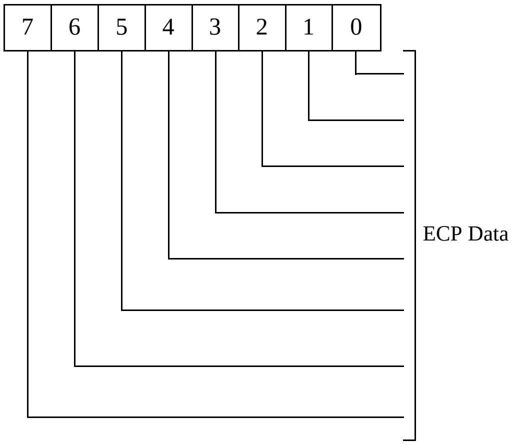
0	Once
1	Twice
2	Three times

7 Data Type

A 1 defines bits 6-0 as the ECP address. A 0 defines these bits as the Run Length field (RLE).

ECP DATA FIFO REGISTER

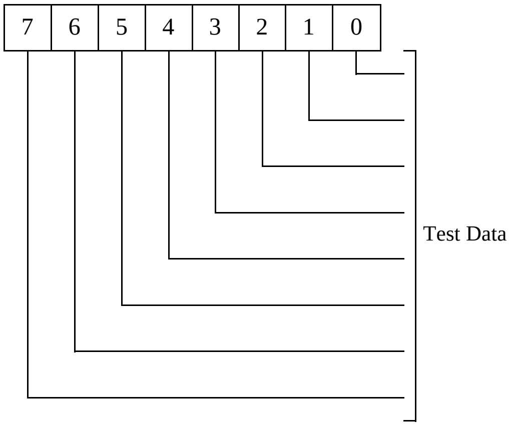
Read/Write Word at LPT +400H in ECP Mode Only



The ECP Data FIFO (ecpDFifo) is used to transfer 8-bit data in ECP mode between the system and the peripheral device. Transfers are made using an automatic hardware handshake in ECP protocol. In the forward direction (control bit DIR is 0), the FIFO relays programmed I/O or DMA data received from the system to the peripheral device. In the reverse direction (DIR is 1), the FIFO receives peripheral data via the ECP parallel port. The FIFO relays the data to the system on a read or DMA.

TEST FIFO REGISTER

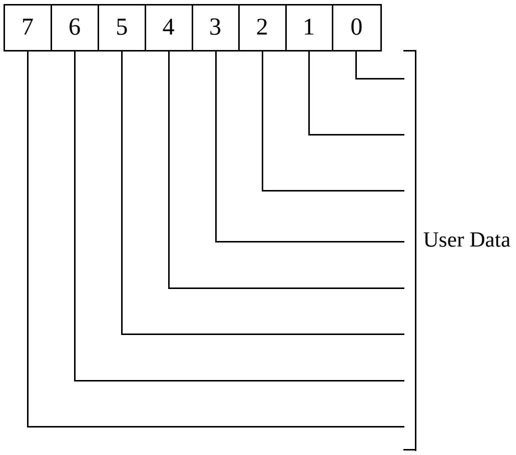
Read/Write Word at LPT +400H in Test Mode Only



TheTest FIFO (tFifo) transfers 8-bit programmed I/O or DMA test data to and from the system. FIFO data is not relayed to the parallel port lines with a hardware protocol handshake.

CONFIGURATION REGISTER A

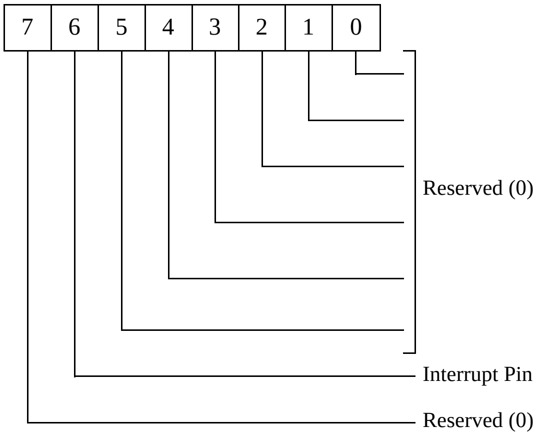
Read Only at LPT +400H in Configuration Mode Only



Configuration Register A (CnfgA) is a read-only register that stores 8-bit data specific to the user's application. When read, the register returns a 10, which indicates that the system is an 8-bit implementation (i.e., a Pword equal to one byte).

CONFIGURATION REGISTER B

Read/Write at LPT +401H in Configuration Mode Only



Configuration Register B (CnfgB) allows software to control the selection of interrupts and DMA channels. Except for a reset, hardware does not affect this register; the values are set only by software.

Some or all of the bits may be read-only. For example, if the port is configurable but only supports 8-bit DMA transfers, then bit 2 will be a read-only bit set to 0, while bits 1-0 may be read/write. Similarly, any or all of the interrupt bits (5-3) may be read-only. All ISA ports must implement this register as read-only as a minimum.

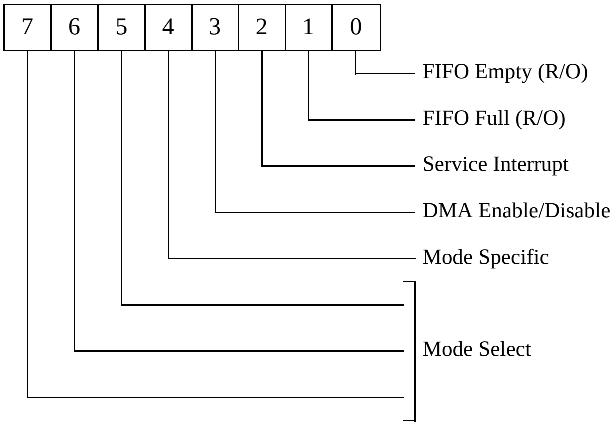
5-0 Reserved (0)

6 Interrupt Pin

7 Reserved (0)

EXTENDED CONTROL REGISTER

Read/Write at LPT +402 in
All Modes



The read/write Extended Control Register (ECR) controls the extended parallel port functions and is always accessible.

0 FIFO Empty (FE), Read Only

0 Not empty (default)
1 Completely empty

Bits 1 and 0 cannot be 1 simultaneously, but they can be 0 simultaneously, i.e., partially full and partially empty. These bits always reflect the current status of the FIFO, regardless of the mode. The pointers indicate when a byte transfer from the parallel port is completed, not when it is started.

1 FIFO Full (FF), Read Only

0 Not full (default)
1 Completely full

2 Service Interrupt (SI)

0 Enables a service interrupt when any of the following is true:

- ■ Bit DE (DMA Enable) is 1. Interrupt occurs during DMA. SI is disabled when terminal count is reached.
- ■ Bits DE and DIR (Direction) are both 0. SI is disabled when there are threshold or more Pwords in the FIFO.
- ■ Bit DE is 0 and bit DIR is 1. SI is disabled when there are threshold or more valid Pwords to be read from the FIFO.

1 Disables DMA and all of the service interrupts.

Following the interrupt, SI is set to a 1 by hardware. Writing this bit to a 1 does not cause an interrupt.

3 DMA Enable (DE)

1 DMA enabled (DMA starts when SI = 0)
0 DMA disabled unconditionally (default).

4 Mode Specific

Definition depends upon the mode selected. See "Mode-Specific Bit Definitions."

7-5 Mode Select

0 **Standard (STD) mode (default).** In this mode, the FIFO is reset and common collector drivers are used on the control lines. Setting the DIR bit (bit 5) of the Control Register does not tristate the output drivers.

1 **Bidirectional (BIDI) mode.** This PS/2-type mode is the same as standard mode except that the DIR bit may be used to tristate the output drivers. All drivers have active pull-ups (push-pull).

2 **Fast Centronics (CENT) mode.** Fast Centronics is the same as standard mode except that programmed I/O or DMA data is sent to a FIFO. FIFO data is automatically transmitted using the standard parallel port protocol.

3 **Extended Capabilities (ECP) mode.** In the forward direction (DIR = 0), data in the ECP Data FIFO and bytes in the ECP Address FIFO are placed in a single FIFO and transmitted automatically to the peripheral using ECP protocol. In the reverse direction (DIR = 1), data is moved from the ECP parallel port to the ECP Data FIFO. All drivers have active pull-ups (push-pull).

4 **Enhanced Parallel Port (EPP) mode.** This is an enhanced bidirectional non-FIFO protocol for programmed I/O or DMA data.

5 **Reserved**

6 **TEST.** In Test mode, the FIFO is enabled as read/write, but the data is not transmitted on the parallel port.

7 **Configuration.** When set, this bit enables Configuration Registers A and B.

MODE-SPECIFIC BIT DEFINITIONS

This section defines bit 4 and other mode-specific bits of the Extended Control Register (ECR). All other bits are defined under "Extended Control Register."

Fast Centronics Mode

4 Speed (SP)

0 Normal; data Hold/Setup sequential 1.5µs cycle
1 Fast; data Hold/Setup overlapped, 1.0 µs cycle (default)

EPP Mode

2 Timeout Interrupt (TI)

This timeout occurs if IOCHRDY is asserted during an EPP programmed I/O transfer for more than 2.6µs (63 clocks). The timeout prevents an error condition during a transfer to an EPP device from locking up the ISA bus and the system.

0 IOCHRDY timout interrupt enabled
1 IOCHRDY timeout interrupt disabled (default)

4 Speed (SP)

0 Normal; 500ns timing, 12 clocks
1 Fast; 250ns timing, 6 clocks (default)

ECP Mode

4 Error Interrupt (EI)

0 Error interrupt enabled
1 Error interrupt disabled (default)

Test Mode

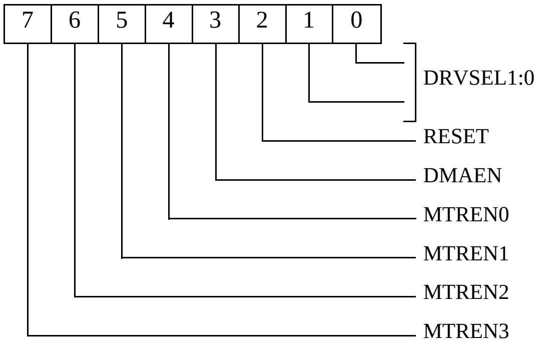
4 Reserved (0)

Floppy Drive Control (FDC) Registers

Register Mnemonic	Register Name	Index (hex)	Access	Primary Address (hex)	Secondary Address (hex)	Page
DOR	Digital Output	2	R/W	3F2	372	66
TDR	Tape Drive	3	R/W	3F3	373	67
DSR	Data Rate Select	4	W	3F4	374	68
MSR	Main Status	4	R	3F4	374	69
FIFO	Data (FIFO)	5	R/W	3F5	375	70
DIR	Digital Input	7	R	3F7	377	71
CCR	Configuration Control	7	W	3F7	377	71

DIGITAL OUTPUT REGISTER

Read/Write at Primary Address 3F2H
Secondary Address 372H



The Digital Output Register (DOR) controls the drive select and motor enable disk interface outputs, enables the DMA logic, and contains a software reset bit. The content of the DOR is set to 00H after a hardware reset and is unaffected by a software reset. The DOR can be written to at any time.

1-0 Drive Select 1and 0 (DRVSEL1-0)

These two bits are binary encoded for the four drive selects DR3-0, so that only one drive select output is active at a time. The following table shows the DOR values that enable each of the four drives.

FDC DRIVE ENABLE VALUES

Drive	DOR Value (hex)
0	1C
1	2D
2	4E
3	8F

It is common programming practice to enable both the motor enable and drive select outputs for a particular drive. The DOR reset bit and the motor enable bits have to be inactive when the FDC is in the powerdown mode. The DMAEN# and DRVESEL bits are unchanged. During power down, writing to the DOR does not activate the FDC, with the exception of the motor enable bits. Setting any of these bits active (high) will wake up the FDC.

2 Reset Controller (RESET)

Bit 2 clears the basic FDC core and the FIFO circuits. Once set, it remains set until the user clears it. This bit is set by a master reset to the 82C735 and remains set until the user clears it. Bit 2 has no effect upon the rest of the DOR register.

3 DMA Enable (DMAEN#)

In the PC AT mode, writing a 1 to this bit will enable the DRQ, DACK#, TC, and IRQ pins. Writing a 0 to this bit will disable the DACK# and TC pins and tristate the DRQ and IRQ pins.

4 Motor Enable 0 (MTREN0)

Bit 4 performs the same function as bit 7, except that it controls the MTR0 disk interface output.

5 Motor Enable 1 (MTREN1)

Bit 5 controls the MTR1 disk interface output. In all other respects it performs the same functon as bit 7.

6 Motor Enable 2 (MTREN2)

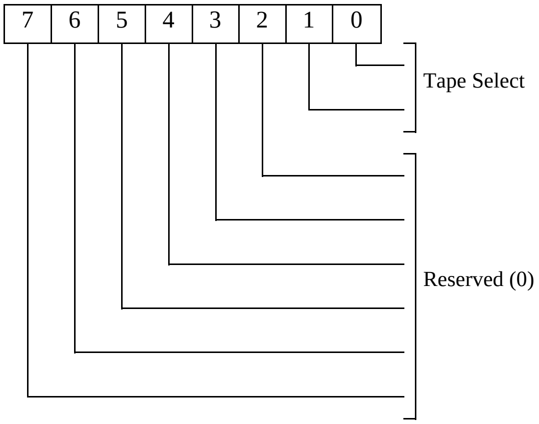
Bit 6 controls the MTR2 disk interface output. In all other respects it performs the same function as bit 7.

7 Motor Enable 3 (MTREN3)

Bit 7 controls the MTR3 disk interface output. A 1 in this bit causes the MTR3 pin to go active.

TAPE DRIVE REGISTER

Read/Write at PrimaryAddress 3F3H in Normal Mode
Secondary Address 373H



The Tape Drive Register (TDR) is included for software compatability. The 82C735 digital data separator does not have to be modified for tape support. The contents of this register are not internal to the device.

1-0 Tape Select

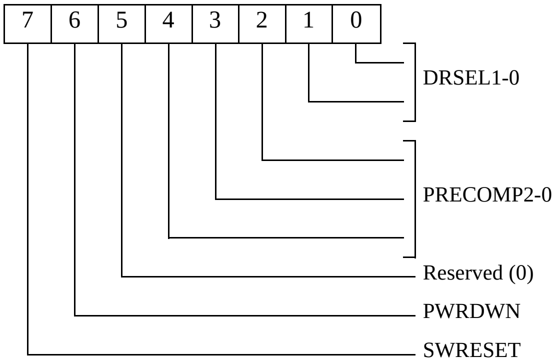
TAPESEL1	TAPESEL0	Drive Selected
0	0	None
0	1	1
1	0	2
1	1	3

7-2 Reserved (0)

Tristated when read in normal mode

DATA RATE SELECT REGISTER

Write Only at Primary Address 3F4H
Secondary Address 374H



The Data Rate Select Register (DSR) ensures backward compatibility. It is used to program the data rate, amount of write precompensation, powerdown mode, and software reset. For PC/AT applications, the data rate is programmed through the Configuration Control Register (CCR), not the DSR. Other applications may set the data rate in the DSR. The FDC data rate is determined by the most recent write to either the DSR or the CCR. Changing the data rate changes the timings of the drive control signals. To ensure that the drive timings are not violated when the data rate is changed, choose a drive timing such that the fastest data rate will not violate the timing.

This register is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and the 250Kb/s data rate setting.

1-0 Data Rate Select (DRSEL1-0)

These bits select one of four data rates, as listed in the following table. The default value is 250Kbps upon a hardware reset. Software resets do not affect the data rate or precompensation bits.

DATA RATE SELECT ENCODING

Data Rate Select		Data Rate	
1	**0**	**MFM**	**FM**
1	1	1Mbps	Illegal
0	0	500Kbps	250Kbps
0	1	300Kbps	150Kbps
1	0	250Kbps	125Kbps

4-2 Precompensation (PRECOMP2-0)

These bits adjust the write data output to the disk to compensate for bit shifting. The FDC compensates the data pattern as it is written to the disk.

The FDC starts precompensating the data pattern from track 0. Use the CONFIGURE command to change the starting track (see ‘‘FDC Command Set’’).

The amount of precompensation depends on the drive and media, but in most cases the default value is acceptable. Precompensation delay and default values are listed in the following tables.

PRECOMPENSATION DELAY VALUES

PRECOMP2-0 Value	Delay Value (nsec)
111	Disabled
001	41.67
010	83.34
011	125.00
100	166.67
101	208.33
110	250.00
000	Default

DEFAULT DELAY VALUES

Data Rate	Precompensation Delay(nsec)
1Mbps	41.67
500kbps	125.00
300kbps	125.00
250kbps	125.00

5 Reserved (0)

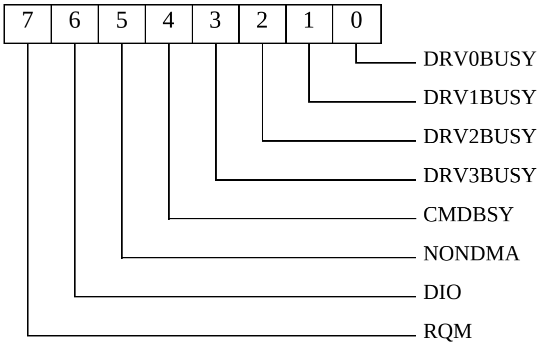
6 Powerdown (PWRDWN)

Bit 6 implements direct powerdown. Setting this bit high will put the FDC into the powerdown state regardless of the state of the 82C735. The FDC is internally reset and put into powerdown. No status is saved, and any operation in progress is aborted. The oscillator and data seperator circuits are turned off. Any hardware or software reset or access to the Data Register or Main Status Register will cause the FDC to exit this powerdown state.

7 Software Reset (SWRESET)

This bit behaves like the DOR reset except that it is self-clearing.

MAIN STATUS REGISTER
Read Only at Primary Address 3F4H
Secondary Address 374H



The Main Status Register (MSR) is always available to be read. The MSR is used for controlling command input and result output for all commands. It gives the current status of the FDC, and indicates when the disk controller is ready to send or receive data through the data register (FIFO).

The MSR should be read before transfering a byte to or from the FIFO, except during a DMA transfer. No delay is required when reading this register after a data transfer. After a hardware or software reset, or recovery from a powerdown state, the MSR can be read immediately by the microprocessor.

The MSR will contain a value of 00H until the oscillator circuit has stabilized and the internal registers have been initialized. When the FDC is ready to receive a new command, it will report a status of 80H to the microprocessor. System software polls on the MSR until it is ready. The worst case time allowed for the MSR to report an 80H value (RQM set) is 2.5µsec after reset or powerup.

0 **Drive 0 Busy (DRV0BUSY)**

This bit is set after the last byte of the command phase of a SEEK or RECALIBRATE command is issued for drive 0. It is cleared after receipt of the first byte in the result phase of a SENSE INTERRUPT command for this drive (see "FDC Command Handling" and ‘‘FDC Command Set’’).

1 **Drive 1 Busy (DRV1BUSY)**

Bit 1 is set after the last byte of the command phase in a SEEK or RECALIBRATE command is issued for drive 1. It is cleared after receipt of the first byte in the result phase of a SENSE INTERRUPT command for this drive (see ‘‘FDC Command Handling’’ and ‘‘FDC Command Set’’).

2 **Drive 2 Busy (DRV2BUSY)**

This bit is set after the last byte of the command phase in a SEEK or RECALIBRATE command is issued for drive 2. It is cleared after receipt of the first byte in the result phase of a SENSE INTERRUPT command for this drive (see ‘‘FDC Command Handling" and ‘‘FDC Command Set’’).

3 **Drive 3 Busy (DRV3BUSY)**

Bit 3 is set after the last byte of the command phase in a SEEK or RECALIBRATE command is issued for drive 3. It is cleared following receipt of the first byte in the result phase of a SENSE INTERRUPT command for this drive (see "FDC Command Handling" and ‘‘FDC Command Set’’).

4 **Command Busy (CMDBSY)**

This bit indicates that a command is in progress. It is set after the first byte of the command phase is written, and it is cleared after the last byte of the result phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the command phase is written (see ‘‘FDC Command Handling’’).

5 **Non-DMA Execution (NONDMA)**

When set to 1, this bit indicates that the controller is in the execution phase of a command. During polled data transfers, this bit segregates the data transfer phase from the result reading phase (see ‘‘FD Command Set’’).

6 **Data I/O (DIO)**

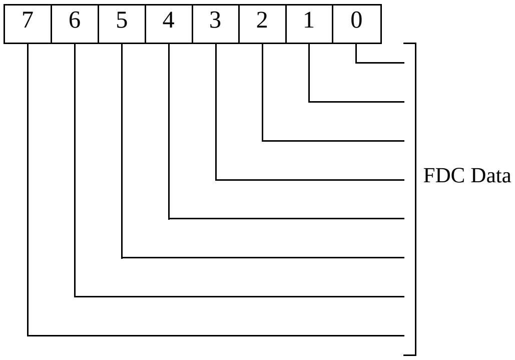
When the RQM bit is set, a 1 in bit D6 indicates a read from the data register and a 0 indicates a write to the data register.

7 **Request for Master (RQM)**

If bit 7 is set to a 1, it indicates that it is ready to send or receive data from the host through the FIFO. If this bit is set to a 0, access is denied. This bit is cleared immediately after a byte transfer and will become set again as soon as the FDC is ready for the next byte. During a non-DMA execution phase, the RQM bit indicates the status of the interrupt pin (see ‘‘FDC Command Handling’’).

DATA REGISTER (FIFO)

Read/Write at Primary Address 3F5H
Secondary Address 375H



All command/status parameter information and disk data transfers go through the Data Register or FIFO. The data transfers are controlled by bits D7 (RQM) and D6 (DIO) in the Main Status Register. The FIFO is 16 bytes and has programmable threshold values.

Enabling the FIFO and setting the FIFO threshold are done with the CONFIGURE command (see ‘‘FDC Command Set’’). The FIFO is enabled only for execution phase byte transfers. It is always disabled during the command and result phases of a controller operation. If the FIFO is enabled, it will not be disabled after a software reset if the LOCK bit is set in the LOCK command. After a hardware reset, the FIFO is disabled to maintain compatibility with PC/AT systems.

The FIFO can be used for DMA, interrupt, or programmed I/O transfers during the execution of a READ, WRITE, FORMAT, or SCAN command. In addition, the FIFO can be put into a burst or non-burst mode with the MODE command. In burst mode, DRQ or IRQ6 remains active until all of the bytes have been transferred to or from the FIFO. In non-burst mode, DRQ or IRQ6 is deasserted for 350ns to allow higher priority transfer requests to be serviced.

An advantage of this FIFO is that it allows the system a larger DMA latency without causing a disk overrun/underrun error. The default state of the FIFO is disabled, zero threshold, and is entered after a hardware reset. At the start of a command, the FIFO action is always disabled, and command parameters must be sent based upon the RQM and DIO bit settings. In the execution phase, the FIFO is cleared of any data to ensure that invalid data is not transferred. An error (overrun or underrun) will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

The following table gives several examples of FIFO delays.

EXAMPLES OF FIFO SERVICE DELAY

FIFO Threshold (bytes)	Maximum Delay to Servicing	
	At 1Mbps Data Rate	At 500Kbps Data Rate
1	1 x 8µs - 1.5µs = 6.5µs	1 x 16µs - 1.5µs = 14.5µs
2	2 x 8µs - 1.5µs = 14.5µs	2 x 16µs - 1.5µs = 30.5µs
8	8 x 8µs - 1.5µs = 62.5µs	8 x 16µs - 1.5µs = 126.5µs
15	15 x 8µs - 1.5µs = 118.5µs	15 x 16µs - 1.5µs = 238.5µs

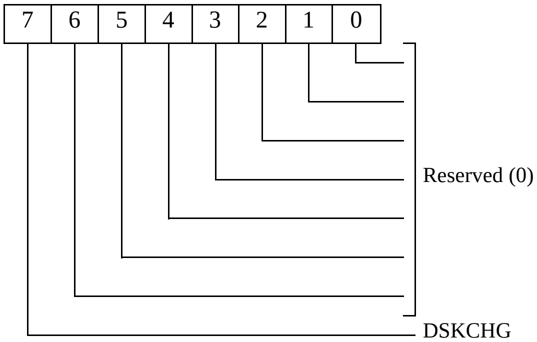
The formula used for these calculations is the following:

$$\text{Threshold} \times \left(\frac{1}{\text{Data Rate}} \times 8\right) - 1.5\mu\text{s} = \text{Delay}$$

The programmable FIFO threshold is useful in adjusting the FDC to the speed of the system. For example, a slow system with a sluggish DMA transfer capability would use a high value of threshold, giving the system more time to respond to a data transfer service request (DRQ for DMA mode or IRQ6 for Interrupt mode).

DIGITAL INPUT REGISTER

Read Only at Primary Address 3F7H
Secondary Address 377H



When the Digital Input Register (DIR) is in PC/AT mode, only bit 7 (DSKCHG) is driven. Bits 6-0 are tristated to avoid conflict with the fixed disk status register at the same address. The DSKCHG bit monitors the pin of the same name and reflects the opposite value seen on the disk cable. Bit 7 is forced inactive along with the inputs from the floppy drive, while the other bits remain tristated. The Digital Input Register is unaffected by a software reset.

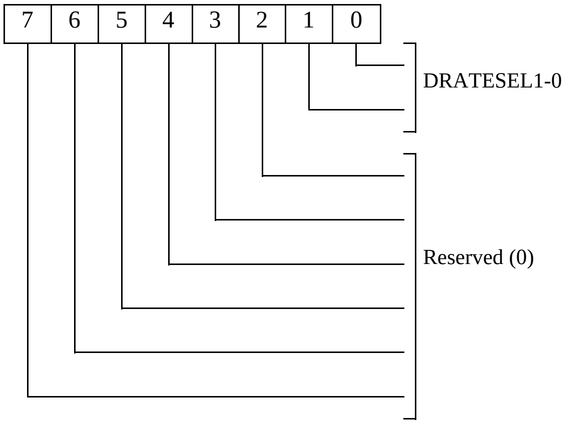
6-0 Reserved (0)

7 Disk Change (DSKCHG)

This bit monitors the DSKCHG pin.

CONFIGURATION CONTROL REGISTER

Write Only at Primary Address 3F7H
Secondary Address 377H



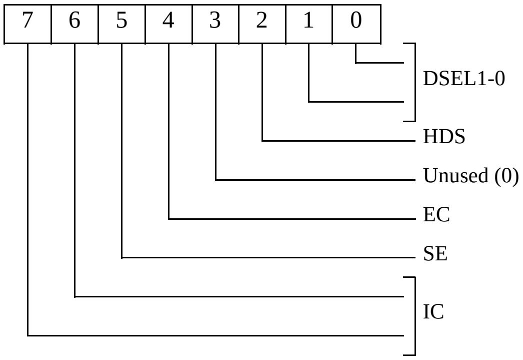
The Configuration Control Register (CCR) sets the data rate. This register is not affected by a software reset and defaults to 250Kb/s on a hardware reset. The data rate of the FDC is determined by the last write to either the configuration control register or the data rate select register.

1-0 Data Rate Select 1, 0 (DRATESEL1-0)

These bits determine the data rate of the floppy controller. The Data Rate Select Encoding table shows the possible values (see ‘‘Data Rate Select Register’’).

7-2 Reserved (0)

RESULT PHASE STATUS REGISTER 0 (ST0)



1-0 Drive Select 1, 0 (DSEL1-0)

These bits indicate the logical drive selected:

00	Drive 0
01	Drive 1
01	Drive 2
11	Drive 3

2 Head Select (HDS)

Bit 2 indicates the current head address

3 Unused (always 0)

4 Equipment Check (EC)

A 1 in bit D4 following a RECALIBRATE command indicates that the track 0 signal failed to occur. (See the RECALIBRATE command in the FDC Command Set.)

5 Seek End (SE)

This bit indicates that a SEEK, RELATIVE SEEK, or RECALIBRATE command, or a read or write with implied seek command has been completed by the controller. (See the SEEK command and SENSE INTERRUPT STATUS command in the FDC Command Set.)

7-6 Interrupt code (IC)

The IC code can be any of the following:

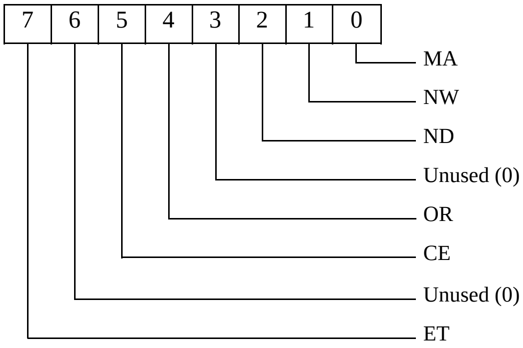
00 Normal termination of command. The specified command was properly executed and completed without error.

01 Abnormal termination of command. Execution of command was started, but was not successfully completed.

10 Invalid command issued. Command issued was not recognized as a valid command.

11 Internal drive ready status changed state during the drive polling mode. Occurs only after a hardware or software reset.

RESULT PHASE STATUS REGISTER 1 (ST1)



0 **Missing Address Mark (MA)**

This bit is set high if one of the following conditions occurs:

- Bit 0 of ST2 is 0, indicating that no ID field address mark was detected after two revolutions (index pulses).
- Bit 0 of ST2 is 1, indicating that no data field address mark was detected after the correct ID field was found.

1 **Not Writable (NW)**

Bit 1 is set high to indicate that the write protect pin (WRPRT#) is active when a write or format command is issued.

2 **No Data (ND)**

Bit 2 is set high to indicate one of the following conditions:

- Controller cannot find the specified sector during a READ DATA, READ DELETED DATA, WRITE DATA, SCAN, or VERIFY command.
- No (ID) address field found without a CRC error during a READ ID command.
- Controller cannot find the starting sector during execution of a READ TRACK command.

3 **Unused (always 0)**

4 **Overrun/Underrun (OR)**

This bit indicates an overrun during a read operation or an underrun during a write operation. It is set high when the controller does not receive CPU or DMA service within the required interval during a data transfer in the execution phase.

5 **CRC Error (CE)**

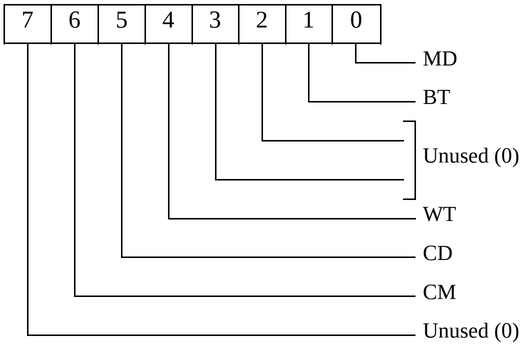
If this bit and bit 5 of ST2 are both clear, then a CRC error occurred in the address (ID) field. If these bits are both set, the CRC error occurred in the data field.

6 **Unused (always 0)**

7 **End of Track (ET)**

A 1 in bit 7 indicates that the controller transferred the last byte of the last sector after a READ DATA or WRITE DATA command without the TC pin becoming active. The last sector is the End of Track (EOT) sector number programmed in the command phase. This number implies that the FDC made an attempt to access a sector beyond the final sector of the track.

RESULT PHASE STATUS REGISTER 2 (ST2)



0 Missing Address Mark in Data Field (MD)

Bit 0 is set high if the controller cannot find the data field address mark or a deleted data field address mark during a READ DATA, SCAN, or VERIFY command. Bit 0 of ST1 is also set.

1 Bad Track (BT)

This bit sets high if the desired sector is not found and the track number recorded on any sector of the current track is FFH and is different from the track address specified in the command. A track numbered FF indicates a hard error in IBM format.

3-2 Unused (always 0)

4 Wrong Track (WT)

Bit 4 sets high if the desired sector is not found and the track number recorded on any sector of the current track is different from the track address specified in the command.

5 CRC Error in Data Field (CD)

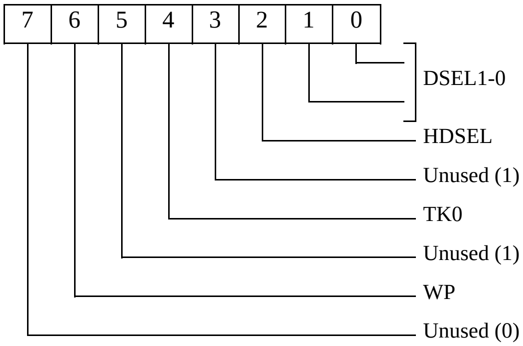
A high in D5 indicates a CRC error in the data field. Bit 5 of ST1 will also set high.

6 Control Mark (CM)

A high indicates that the controller tried to read a sector containing a deleted data address mark during a READ DATA or SCAN command. If the bit goes high during a READ DELETED DATA command, the controller detected a regular address mark.

7 Unused (always 0)

RESULT PHASE STATUS REGISTER 3 (ST3)



1-0 Drive Select 1, 0 (DSEL1-0)

These bits are set high to indicate the active status of the DS1, DS0 pins.

2 Head Select (HDSEL)

Bit D2 is set high to indicate the active high status of the HDS bit in the command phase.

3 Unused (always 1)

4 Track 0 (TK0)

Bit D4 is set high to indicate the active high status of the TRK0 pin.

5 Unused (always 1)

6 Write Protect (WP)

7 Unused (always 0)

FDC Command Handling

For simplicity, command handling in the 82C735 can be divided into three controller phases:

- Command phase: Host writes command and parameter bytes to FDC.
- Execution phase: FDC processes command and parameter bytes.
- Result phase: FDC sends result bytes to host; clears Command Busy bit for next command.

Each of the controller phases determines how data is transferred between the FDC in the 82C735 and the host microprocessor. When there is no command in progress, the 82C735 can be in an idle, drive polling, or powerdown state.

Each of the controller phases is described in the following sections.

COMMAND PHASE

After a reset, the controller enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the controller before the command phase is complete. These bytes of data must be transferred in the order prescribed.

Before writing to the FDC in the 82C735, the host must examine the RQM and DIO bits of the Main Status Register (MSR). These bits must be equal to 1 and 0, respectively, before the command bytes may be written. Bit RQM is set false by the controller after each write cycle until the received byte is processed. The controller asserts RQM again to request each parameter byte of the command, unless an illegal command condition is detected. After the last parameter byte is received, RQM remains 0 and the controller automatically enters the next phase as defined by the command definition.

A new command may be initiated after all the result bytes from the previous command have been read. If the next command requires selecting a different drive or changing the data rate, the Digital Output Register (DOR) and either the Data Rate Select Register (DSR) or the Configuration Control Register (CCR) should be updated. If the command is the last command, then the software should deselect the drive.

The FIFO is disabled during the command phase to retain compatibility with previous generation FDCs, which do not have a FIFO, and to provide for the proper handling of the *invalid command* condition.

EXECUTION PHASE

All data transfers to and from the 82C735 controller occur during the execution phase. This phase can proceed in DMA or non-DMA mode, as indicated by the SPECIFY command.

The DMA mode is used if the system has a DMA controller. Each data byte is transferred by the FINTR or DRQ pin, depending on the method of transfer used in DMA mode. In this mode the microprocessor can do other tasks while the data transfer takes place.

In the non-DMA mode, an interrupt is issued for each byte transferred during the execution phase. As an alternative to the interrupt, the MSR register can be polled by the software to indicate when a byte transfer is required. Both methods of transfer work with the FIFO enabled or disabled. The CONFIGURE command can be used to enable the FIFO and set the FIFO threshold value.

The following paragraphs describe the operation of the FIFO flow control. In these descriptions, *threshold* is defined as the number of bytes available to the FDC when service is requested from the host. The threshold ranges from 1 to 16 bytes. The FIFOTHR parameter, which the user programs as one less, ranges from 0 to 15 bytes.

A low threshold value (e.g., 2) is desirable for a "fast" system. A low threshold results in longer periods of time between service requests, for both read and write cases. The host reads from the FIFO until it is empty, or writes to the FIFO until it is full. The transfer request then goes inactive. The host must be very responsive to the service request.

A high value of threshold (e.g., 12) is used with a sluggish system. A high value provides a long latency period after a service request, but it results in more frequent service requests.

Non-DMA Transfers From FIFO to Host

Non-DMA transfers can be initiated by activating the FINTR pin or the RQM bit (bit 7) in the MSR register. The FINTR pin can be used for interrupt driven systems and the RQM bit for polled systems.

FINTR and RQM are activated when the FIFO contains (16 - <*threshold* >)bytes, or when the last bytes of a full sector transfer have been placed in the FIFO. The host must respond by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The controller deactivates FINTR and RQM when the FIFO becomes empty.

Non-DMA Transfers From Host to FIFO

The FINTR pin and RQM bit in the MSR register are activated at the beginning of the execution phase of the data transfer command. The host must respond by writing data to the FIFO. FINTR and RQM remain active until the FIFO becomes full; then the controller deactivates them. (FINTR is also deactivated if TC and DACK# both go inactive.) FINTR and RQM are set active again when the FIFO is emptied to its threshold byte level.

DMA Transfers From FIFO to Host

The controller activates the DRQ pin when the FIFO contains (16 - <*threshold*>) bytes, or when the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond by reading data from the FIFO. The controller deactivates DRQ when the FIFO is empty.

DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of RD#, on the last byte, if no edge is present on DACK#). A data underrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

DMA Transfers From Host to FIFO

The controller activates the DRQ pin upon entering the execution phase of the data transfer command. The DMA controller must respond by activating the DACK# and WR# pins and placing data in the FIFO. The DRQ pin remains active until the FIFO becomes full; then the controller deactivates the pin. DRQ is set active again when the FIFO is emptied to its threshold byte level.

The controller will also deactivate the DRQ pin when TC becomes active (qualified by DACK#), indicating that no more data is required. DRQ goes inactive after DACK# goes active for the last byte of a data transfer (or on the active edge of WR#, on the last byte, if no edge is present on DACK#). A data overrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

Data Transfer Termination

The controller supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and End of Track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single-sector or multi-sector transfer. If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, allowing the controller to complete the sector as if a hardware TC were received. The only difference between these implicit functions and the TC pin is that they return "abnormal termination" result status.

Note: When the host is sending data to the FIFO, the internal sector count will complete when the controller reads the last byte from its side of the FIFO. Removal of the transfer request signal may be delayed for as long as it takes the controller to read the last 16 bytes from the FIFO. The host must tolerate this delay.

RESULT PHASE

Generation of the FINTR signal determines the beginning of the result phase. For each command, a defined set of result bytes must be read from the controller before the result phase is completed and another command can start. Bits RQM and DIO of the Main Status Register must both equal 1 before the result bytes can be read from the FIFO.

After all the result bytes have been read, the RQM and DIO bits switch to 1 and 0, respectively, and the Command Busy bit (bit 5) is cleared. This indicates that the controller is ready to accept another command.

FDC Command Set

This section consists of a command summary followed by command descriptions. Commands are arranged alphabetically in the Command Summary and by function in the command description sections: "Data Transfer Command Descriptions" and "Control Command Descriptions."

COMMAND SUMMARY

Each of the commands has a unique set of parameters and status results, and a unique first byte called the *op code byte*. The controller identifies the op code byte as the number of command bytes to expect. If an invalid command byte is issued, the controller goes into the result phase and the status becomes 80H, signifying an invalid command. The following table describes the command parameters.

FDC COMMAND PARAMETERS

Parameter	Description
C	Cylinder number or address of the currently selected track, 0 to 255.
Data Pattern	Format of each data field in a sector of data.
DIR	Direction control bit. Controls the direction of head stepping during a RELATIVE SEEK operation: 0 = step head out; 1 = step head in.
DMA	DMA enable bit. A 0 selects DMA operation; a 1 selects non-DMA operation (default).
DS0, DS1	Disk Drive Select bits: DS = 0, DS0 = 0 selects drive 0; DS1= 0, DS0 = 1 selects drive 1; DS1=1, DS0 = 0 selects drive 2; and DS1=1,DS0 =1 selects drive 3.
DTL	Data Length parameter. Sets a special sector size. When N, the number of bytes per sector, is 00 hex, DTL can be used to set the number of bytes transferred in read and write commands. If the data length is less than 128 bytes, the controller transfers the specified number of bytes to the host. When N is not 00, DTL is invalid and should be set to FF hex. See "Data Transfer Command Descriptions" for details. See also N (Bytes per Sector) in this table.
EC	Enable Count bit. A 1 sends an implicit TC signal to the controller to terminate the VERIFY command.
EFIFO	Enable FIFO bit. A 0 enables the FIFO; a 1 disables it (default).
EIS	Enable Implied Seek bit. When this bit is set to 1, the FDC initiates a seek operation before executing a read or write command. A 0 disables implied seek (default).
EOT	End of Track parameter. Last sector of the current track.
FIFOTHR	FIFO Threshold bits. These bits determine the threshold level of the FIFO in the execution phase of a data transfer operation. The threshold can be from1 to16 bytes: 00 selects 1 byte (default); FF selects 16 bytes.
GAP	The GAP and WG (Write Gate) bits together select conventional or perpendicular modes of data transfer and thus determine the length of the GAP2 field: 0 GAP, 0 WG = conventional mode (default); 0 GAP, 1 WG = 500kbps perpendicular mode; 1 GAP, 1 WG = 1Mbps perpendicular mode. See "PERPENDICULAR MODE Command" under "Control Command Descriptions" for details. See also WG in this table.
GPL	Intersector Gap Length (GAP3) parameter. Size of the space between sectors, excluding the VCO sync field. See the FORMAT TRACK Command under "Data Transfer Command Descriptions" for tables of typical gap lengths for various formats and diskette media.
HDS	Head Number Select parameter. Selects head 0 or 1 (disk side 0 or 1), as specified by the Sector ID field.

Parameter	Description
HUT	Head Unload Time. Interval from the end of the execution phase of a read or write command to the head unload state.
LOCK	This bit specifies the use of a software reset to set parameters EFIFO, FIFOTHR, and PRETRK of the CONFIGURE command to their default values. A software reset is enabled by setting bit 2 of the Digital Output Register (DOR) or bit 7 of the Data Rate Select Register (DSR).
MFM/FM	Double-density/single-density select bit. A 1 selects MFM (double density); a 0 selects FM (single density).
MT	Multitrack sector bit. When set, this bit enables the controller to read from or write to both sides of the diskette. See the READ DATA Command under "Data Transfer Command Descriptions" for details.
N (Bytes per Sector)	N is the number of bytes per sector in hexadecimal units. Sector size can be from 128 bytes (N = 00) to 16 kbytes (N = 07). When N = 00, the Data Length (DTL) parameter can be used to specify the number of bytes transferred in read and write commands. See the READ DATA Command under "Data Transfer Command Descriptions" for a table of N values for various sector sizes. See also DTL in this table.
NCN	New Cylinder Number. Specifies the new location of the read/write head in a SEEK operation. See the SEEK command under "Control Command Descriptions" for details.
OW	Overwrite bit in the PERPENDICULAR MODE command. A 1 permits bits 3:0 of the data bus to be overwritten so that the corresponding drives (D3:D0) can be programmed for operation in perpendicular mode.
PCN	Present Cylinder Number. Specifies the current position of the head after completion of a SENSE INTERRUPT STATUS command.
POLL	Polling disable bit. A 0 enables drive polling (default); a 1 disables polling. See the CONFIGURE command under "Control Command Descriptions" for details.
PRETRK	Precompensation Start Track Number. This byte is programmable from 0 (default) to 255. A 00 selects track 0; FF selects track 255. See the CONFIGURE command under "Control Command Descriptions" for details.
R	Sector Number (Record). Number of the sector to be read or written; or number of the first sector if multiple sectors are to be read or written.
RCN	Relative Cylinder Number. Number of tracks to step the head in or out from the present cylinder number (PCN). See the RELATIVE SEEK command under "Control Command Descriptions" for details.
SC	Sectors per Cylinder (Sector Count). See the VERIFY and FORMAT TRACK commands under "Data Transfer Command Descriptions" for additional information.
SI	Sector Increment. Specifies whether contiguous or alternate sectors are to be scanned: SI = 01 specifies contiguous; SI = 02 specifies alternate. Note that if SI is set to 02, MT must be 0. See "SCAN Commands" under "Control Command Descriptions" for additional information.
SK	Skip Flag. When SK = 1, sectors containing Deleted Data Address (DDA) marks are automatically skipped if a READ DATA command is executed, and are the only sectors read if a READ DELETED DATA command is executed. When SK = 0, DDA sectors are read. See the READ DATA command under "Data Transfer Command Descriptions" for details.
SRT	Step Rate Time. Interval between FDC step pulses. Programmable from 0.5 to 8ms, in 0.5ms increments, at 1Mb data rate. See the SPECIFY command under "Control Command Descriptions" for details.
ST0...ST3	Status Registers 0, 1, 2 and 3 store status information for the host after execution of a command.
WG	Write Gate bit. When set, this bit alters GAP2 size and VCO timing to allow pre-erase time in perpendicular mode data transfers. Set to 0 for conventional mode (default); set to 1 for perpendicular mode. See PERPENDICULAR MODE command under "Control Command Descriptions" for additional information. See also GAP in this table.

CONFIGURE COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	EFIFO	POLL	FIFOTHR			
PRETRK							

Execution Phase: Internal registers written.

Result Phase: None

DUMPREG COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0

Execution Phase: Internal registers read.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
PCN DRIVE 0							
PCN DRIVE 1							
PCN DRIVE 2							
PCN DRIVE 3							
SRT				HUT			
HEAD LOAD TIME (HLT)							DMA
SC/EOT							
LOCK	0	DS3	DS2	DS1	DS0	GAP	WG
0	EIS	EFIFO	POLL	FIFOTHR			
PRETRK							

Note: The SC (Sectors per Cylinder) parameter is returned if the last command issued was FORMAT TRACK. The EOT (End of Track) parameter is returned if the last command was READ DATA or WRITE DATA.

FORMAT TRACK COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	MFM	0	0	1	1	0	1
0	0	0	0	0	HDS	DS1	DS0
BYTES PER SECTOR (N)							
SECTORS PER CYLINDER (SC)							
INTERSECTOR GAP LENGTH (GPL)							
DATA PATTERN							

Execution Phase: The host sends four system ID bytes per sector (track, head, sector, bytes/sector) to the floppy controller in DMA or non-DMA mode. The entire track is formatted. The data block in the data field of each sector is filled with the data pattern byte.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
UNDEFINED							
UNDEFINED							
UNDEFINED							
UNDEFINED							

INVALID COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2		0
INVALID CODES							

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0 (80 HEX)							

LOCK COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
LOCK	0	0	1	0	1	0	0

Execution Phase: Internal register is written.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	LOCK	0	0	0	0

PERPENDICULAR MODE COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
OW	0	DS3	DS2	DS1	DS0	GAP	WG

Execution Phase: Internal Register is written.

Result Phase: None

READ DATA COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	SK	0	0	1	1	0
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
DATA LENGTH (DTL)							

Execution Phase: Data read from the disk drive is transferred to the system in DMA or non-DMA mode.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

READ DELETED DATA COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	SK	0	1	1	0	0
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
DATA LENGTH (DTL)							

Execution Phase: Data read from the disk drive is transferred to the system in DMA or non-DMA mode.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

READ ID COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	MFM	0	0	1	0	1	0
0	0	0	0	0	HDS	DS1	DS0

Execution Phase: The controller reads the first ID field header bytes it finds and reports these bytes to the system in the result bytes.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

READ TRACK COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	MFM	0	0	0	0	1	0
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
DATA LENGTH (DTL)							

Execution Phase: Data read from the disk drive is transferred to the system in DMA or non-DMA mode.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

RECALIBRATE COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	1
0	0	0	0	0	0	DS1	DS0

Execution Phase: Disk drive head is stepped out to track 0.

Result Phase: None

RELATIVE SEEK COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
1	DIR	0	0	1	1	1	1
0	0	0	0	0	HDS	DS1	DS0
RELATIVE CYLINDER NUMBER (RCN)							

Execution Phase: The disk drive head is stepped in or out a programmable number of tracks.

Result Phase: None

SCAN EQUAL COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	SK	1	0	0	0	0
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
SECTOR INCREMENT (SI)							

Execution Phase: Controller compares floppy disk data to data received from the host.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

SCAN HIGH OR EQUAL COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	SK	1	1	1	0	1
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
SECTOR INCREMENT (SI)							

Execution Phase: Controller compares floppy disk data to data received from the host.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

SCAN LOW OR EQUAL COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	SK	1	1	0	0	1
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
SECTOR INCREMENT (SI)							

Execution Phase: Controller compares floppy disk data to data received from the host.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

SEEK COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1
0	0	0	0	0	HDS	DS1	DS0
NEW CYLINDER NUMBER (NCN)							

Execution Phase: The disk drive head is stepped in or out to a programmable track.

Result Phase: None

SENSE DRIVE STATUS COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
0	0	0	0	0	HDS	DS1	DS0

Execution Phase: Disk drive status information is detected and reported in Status Register 3.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 3							

SENSE INTERRUPT STATUS COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0

Execution Phase: Status is reported to Status Register 0 at the end of each seek operation.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
PRESENT CYLINDER NUMBER (PCN)							

SPECIFY COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
SRT				HUT			
HEAD LOAD TIME (HLT)							DMA

Execution Phase: The internal register is read or written.

Result Phase: None

VERIFY COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	SK	1	0	1	1	0
EC	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
DTL/SC							

Execution Phase: Data is read from the disk but is not transferred to the system.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

VERSION COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	0

WRITE DATA COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	0	0	0	1	0	1
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
DATA LENGTH (DTL)							

Execution Phase: Data is transferred from the system to the controller in DMA or non-DMA mode and is written to the disk.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

WRITE DELETED DATA COMMAND

Command Phase:

Data Bus							
7	6	5	4	3	2	1	0
MT	MFM	0	0	1	0	0	1
0	0	0	0	0	HDS	DS1	DS0
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							
EOT SECTOR NUMBER							
INTERSECTOR GAP LENGTH (GPL)							
DATA LENGTH (DTL)							

Execution Phase: Data is transferred from the system to the controller in DMA or non-DMA mode and is written to the disk.

Result Phase:

Data Bus							
7	6	5	4	3	2	1	0
STATUS REGISTER 0							
STATUS REGISTER 1							
STATUS REGISTER 2							
CYLINDER NUMBER (C)							
HEAD NUMBER (HDS)							
SECTOR NUMBER (R)							
BYTES PER SECTOR (N)							

DATA TRANSFER COMMAND DESCRIPTIONS

All of the READ DATA, WRITE DATA, and VERIFY type of commands use the same parameter bytes and return the same type of result data. The only difference is the coding of bits 4:0 in the first byte.

An implied SEEK is executed if the EIS feature is enabled by means of the CONFIGURE command. This seek is completely transparent to the user. During the seek portion of the command, the Drive Busy bit for the drive (Main Status Register) goes active. If the seek portion fails, the failure is reflected in the result status, which is normally returned for a READ/WRITE DATA command. Status Register 0 (ST0) contains the error code, and Cylinder Number (C) contains the number of the cylinder on which the seek failed.

READ DATA Command

A set of nine bytes is required to place the controller in the read data mode. After the READ DATA command has been issued, the controller loads the head, if required, waits the specified head setting time (defined in the SPECIFY command), and begins reading ID address marks and ID fields. When the sector address read off the diskette matches the sector address specified in the command, the controller reads the sector's data field and transfers the data to the FIFO.

When the read from the current sector is completed, the sector address is incremented by one, and the data from the next logical sector is read and output via the FIFO. This continuous read function is called a *multisector read operation*.

Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the controller stops sending data but continues to read data from the current sector and check CRC bytes. At the end of the sector, the controller terminates the READ DATA command.

Sector sizes are listed in the following table. If N, the number of bytes per sector, is set to 00H, the sector size is set to 128 bytes. The Data Length (DTL) value determines the number of bytes to be transferred. If DTL is less than 128 bytes, the controller transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for any CRC errors. For writes, it completes the 128-byte sector, filling in zeros. If N is not set to 00H, then DTL is invalid and should be set to FF hex. (This has no impact on the number of bytes transferred.)

SECTOR SIZES, READ DATA MODE

Number of Bytes per Sector, N (hex)	Sector Size (bytes)
00	128
01	256
02	512
03	1024
04	2048
—	—
07	16k

The amount of data that can be handled with a single command to the controller depends upon the multitrack (MT) and the number of Bytes per Sector (N), as shown in the following table. MT is bit 7 of the first command byte.

MAXIMUM DATA HANDLING PER READ DATA COMMAND

MT	N	MaximumTransfer Capacity (bytes)	Final Sector Read From Disk
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

The multitrack function (MT) allows the controller to read data from both sides of the diskette. For a particular cylinder, data is transferred starting at sector 1, side 0, and is completed at the last sector of the same track on side 1.

If the host terminates a read or write operation in the controller, then the ID information in the result phase is dependent upon the state of the MT bit and the End of Track (EOT) byte (see the Result Phase table on the following page).

At the completion of the READ DATA command, the head is not unloaded until the Head Unload interval (specified in the SPECIFY command) has elapsed. If the host issues another command before the head unloads, then the head setting time may be saved between subsequent reads.

If the controller twice detects a pulse on the INDEX pin without finding the specified sector, it sets the IC code in Status Register 0 (ST0) to 01 (abnormal termination), sets the DMA bit in register ST1 to 1 (sector not found), and terminates the READ DATA command. The controller could fail to find the specified sector if the diskette's index hole passes through the index detect logic in the drive.

After reading the ID and data fields in each sector, the controller checks the CRC bytes. If a CRC error occurs in the ID or data field, the controller sets the IC code in register ST0 to 01 (abnormal termination), sets the CE bit flag in register ST1 to 1, sets the CD bit in register ST2 to 1 (if CRC is incorrect in the ID field), and terminates the READ DATA command.

The skip flag (SK) is bit 5 of the first command byte. When this bit is set to 1, sectors containing a Deleted Data Address (DDA) mark are automatically skipped during execution of the READ DATA command. If READ DELETED DATA is executed, only sectors with a DDA mark are accessed. When the SK flag is set to 0, these sectors are read.

The following table shows the effect of the SK bit on execution of the READ DATA command. Except where noted in this table, the Cylinder Number (C) or Sector Number (R) of the sector address is automatically incremented (see the Result Phase table on the following page).

EFFECT OF SKIP BIT ON READ DATA COMMAND

SK Bit Value	Data Address Mark	Sector Read?	CM Bit of ST2 Set?	Result
0	Normal Data	Yes	No	Normal termination
0	Deleted Data	Yes	Yes	Address not incremented; next sector not searched for
1	Normal Data	Yes	No	Normal termination
1	Deleted Data	No	Yes	Normal termination; sector skipped

READ DELETED DATA RESULT PHASE

MT	HDS	Final Sector Transferred to Host	ID Information at Result Phase			
			Cylinder No. (C)	HDS	Sector No. (R)	Bytes/Sector (N)
0	0	Less than EOT	No change	No change	R+1	No change
0	0	Equal to EOT	C + 1	No change	01	No change
0	1	Less than EOT	No change	No change	R+1	No change
0	1	Equal to EOT	C + 1	No change	01	No change
1	0	Less than EOT	No change	No change	R+1	No change
1	0	Equal to EOT	No change	LSB	01	No change
1	1	Less than EOT	No change	No change	R+1	No change
1	1	Equal to EOT	C + 1	LSB	01	No change

Notes: “No change” means the value is the same as it was at the start of command execution.
The LSB of HDS (head number) is complemented.

READ DELETED DATA Command

This command is the same as READ DATA, but it operates on sectors that contain a Deleted Data Address (DDA) mark at the beginning of a data field. The following table shows the effect of the SK bit on execution of the READ DELETED DATA command.

EFFECT OF SKIP BIT ON READ DELETED DATA COMMAND

SK Bit Value	Data Address Mark	Sector Read?	CM Bit of ST2 Set?	Result
0	Normal Data	Yes	Yes	Address not incremented; next sector not searched for
0	Deleted Data	Yes	No	Normal termination
1	Normal Data	No	Yes	Normal termination; sector skipped
1	Deleted Data	Yes	No	Normal termination

Except as noted in the above table, the Cylinder Number (C) or Sector Number (R) of the sector address is automatically incremented. This is shown in the Result Phase table.

READ TRACK Command

This command is similar to the READ DATA command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the IDX pin, the controller reads all the data fields on the track as continuous blocks of data, without regard to logical sector numbers. If the controller finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command.

The controller compares the ID information read from each sector with the specified value in the command, and sets the No Data flag of Status Register 1 (ST1) to 1 if there is no comparison. Multitrack or skip operations are not allowed with this command. The MT and SK bits (bits 7 and 5 of the first command byte, respectively) should always be set to 0.

This command terminates when the EOT specified number of sectors has been read. If the controller does not find an ID address mark on the diskette after the second occurrence of a pulse on the INDEX pin, it sets the IC code in register ST0 to 01 (abnormal termination), sets the MA bit (missing address mark) in register ST1 to 1, and terminates the command.

WRITE DATA Command

After the WRITE DATA command has been issued, the controller loads the head (if in Head Unload state), waits the specified Head Load time (as defined in the SPECIFYcommand), and begins reading ID fields. When the sector address read from the diskette matches the Sector Number specified in the command, the controller reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the controller computes the CRC value and writes it into the CRC field at the end of the sector transfer. The second number stored in Sector Number is incremented by 1, and the controller continues writing to the next data field. The FDC continues this multisector write operation. Upon receipt of a terminal count signal, or the occurrence of a FIFO over/underrun while a data field is being written, the controller fills the remainder of the data field with zeros.

The controller reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 (ST0) to 01 (abnormal termination), sets the CE bit of register ST1 to 1, and terminates the WRITE DATA command.

The WRITE DATA command operates in much the same manner as the READ DATA command. The definition of items like End of Track, No Data, and Data Length are the same. Refer to the READ DATA command for details.

WRITE DELETED DATA Command

This command is almost the same as the WRITE DATA command except that a Deleted Data Address Mark is written at the beginning of the data field instead of the normal Data Address mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

VERIFY Command

The VERIFY command is used to verify the data stored on a disk. This command functions like a READ DATA command except that no data is transferred to the host. Data is read from the disk, and the CRC is computed and checked against the previously stored value.

Because no data is transferred to the host, TC cannot be used to terminate this command. An implicit TC will be issued to the controller if the EC bit is set to 1. This implicit TC will occur when the Sectors per Cylinder (SC) value has decremented to 0. An SC value of 0 will verify 256 sectors.

This command can also be terminated by setting the EC bit to 0 and the EOT value equal to the final sector to be checked. If EC is set to 0, the Data Length(DTL)/Sectors per Cylinder (SC) should be programmed to 0FFH. Refer to the following table for MT and EC values versus SC and EOT values.

VERIFY COMMAND RESULT PHASE

MT Val.	EC Val.	SC and EOT Values	Termination Result
0	0	SC = DTL and EOT < sectors per side	Successful; result phase valid
0	0	SC = DTL and EOT > sectors per side	Unsuccessful; result phase valid
0	1	SC < remaining sectors and EOT < sectors per side	Successful; result phase valid
0	1	SC > remaining sectors or EOT > sectors per side	Unsuccessful; result phase valid
1	0	SC = DTL and EOT < sectors per side	Successful; result phase valid
1	0	SC = DTL and EOT > sectors per side	Unsuccessful; result phase valid
1	1	SC < remaining sectors and EOT < sectors per side	Successful; result phase valid
1	1	SC > remaining sectors or EOT > sectors per side	Unsuccessful; result phase valid

Notes: SC = Sectors per Cylinder, EOT = End of Track, DTL = Data Length; sectors per side = number of formatted sectors per each side of the disk; sectors remaining = number of formatted sectors left to read, including side 1. If MT is set to 1 and SC is greater than the number of remaining formatted sectors on side 0, verification continues on side 1.

FORMAT TRACK Command

The FORMAT TRACK command allows an entire track to be formatted in IBM, ISO, or perpendicular format. The figure on the following page shows the IBM, perpendicular, and ISO formats supported by the FORMAT TRACK command.

After a pulse from the INDEX pin is detected, the controller starts writing data on the disk, including the Gap, Address Marks, ID, and Data fields, using the IBM system 34 or 3740 format (MFM or FM, respectively).

The values written to the gap and data fields are controlled by the values programmed into Bytes per Sector (N), Sectors per Cylinder (SC), Intersector Gap Length (GPL), and Data Pattern, which are specified by the host during the command phase. The sector data field is filled with the specified data byte.

The sector ID field is supplied by the host. For this field the controller needs four data bytes per sector for Cylinder Number (C), Head Number (HDS), Sector Number (R), and Bytes per Sector (N).

After formatting each sector, the host must send the controller new values for Cylinder Number , Head Number, Sector Number, and Bytes per Sector for the next sector on the track during the execution phase.

Sector Number is the only value that the host must change after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). The incrementing and formatting continues for the whole track until the controller again encounters a pulse on the INDEX pin and terminates the command.

The following tables contain typical values for gap fields that depend upon the size of the sector and the number of sectors on each cylinder. Actual values can vary due to drive electronics.

TYPICAL GAP LENGTH VALUES FOR FORMATTING

Format	Sector Size (dec.)	Bytes/ Sector, N (hex)	Sectors/ Cylinder (hex)	GPL1 (hex)	GPL2 (hex)
FM 5.25inch	128	00	12	07	09
	128	00	10	10	19
	512	02	08	18	30
	1024	03	04	46	87
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM 5.25inch	256	01	12	0A	0C
	256	01	10	20	32
	512*	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
FM 3.5inch	128	0	0F	07	1B
	256	1	09	0F	2A
	512	2	05	1B	3A
MFM 3.5inch	256	1	0FF	0E	36
	512*	2	09	1B	54
	1024	3	05	35	74

Notes: GPL1 = suggested intersector gap length in read/write commands to avoid a splice point between the data and ID fields of contiguous sections. GPL2 = suggested intersector gap length in the FORMAT TRACK command.

*PC/AT typical values.

TYPICAL VALUES FOR PC-COMPATIBLE DISKETTE MEDIA

Media	Sector Size (dec.)	Bytes/ Sector, N (hex)	Sectors/ Cylinder (hex)	GPL1 (hex)	GPL2 (hex)
360k	512	02	09	2A	50
1.2M	512	02	0F	1B	54
720k	512	02	09	1B	50
1.44M	512	02	12	1B	53
2.88M	512	02	24	1B	53

Notes: GPL1 = suggested intersector gap length in read/write commands to avoid a splice point between the data and ID fields of contiguous sections. GPL2 = suggested intersector gap length in the FORMAT TRACK command.

IBM Format (MFM)

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		TRACK	HEAD	SECTOR	# BYTES	CRC	GAP 2	SYNC	DATA AM		DATA	CRC	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE						22x	12x	3x	FB				
4E	00	C2		4E	00	A1							4E	00	A1	F8				

Note: IAM is 3 bytes of C2 data pattern, clock pattern of 14.
AM is 3 bytes of A1 data patern, clock pattern of 0A.

IBM Format (FM)

GAP 4a	SYNC	IAM	GAP 1	SYNC	IDAM	TRACK	HEAD	SECTOR	# BYTES	CRC	GAP 2	SYNC	DATA AM	DATA	CRC	GAP 3	GAP 4b
40x	6x	FC	26x	16x	FE						11x	6x	FB or F8				
FF	00		FF	00							FF	00					

Note: IAM is 3 bytes of FC data pattern, clock pattern of D7.
AM is 3 bytes of FE data pattern, clock pattern of C7.
Data AM is 3 bytes of FB or F8 data pattern, clock pattern of C7.

Perpendicular Format

GAP 4a	SYNC	IAM		GAP 1	SYNC	IDAM		TRACK	HEAD	SECTOR	# BYTES	CRC	GAP 2	SYNC	DATA AM		DATA	CRC	GAP 3	GAP 4b
80x	12x	3x	FC	50x	12x	3x	FE						41x	12x	3x	FB				
4E	00	C2		4E	00	A1							4E	00	A1	F8				

Note: IAM is 3 bytes of C2 data pattern, clock pattern of 14.
AM is 3 bytes of A1 data pattern, clock pattern of 0A.

Note: All byte counts are in decimal; all byte values are in hex.
CRC uses standard polynomial x16 + x12 + x5 + 1.
Perpendicular Format GAP2 = 41 bytes is only for the 1Mbps data rate; otherwise it is 22 bytes.

Formats Supported by the 82C735 Chip

CONTROL COMMAND DESCRIPTIONS

Control commands differ from the other commands in that no data transfer takes place. The READ ID, RECALIBRATE, and SEEK commands generate an interrupt; the remaining control commands do not. The RECALIBRATE and SEEK commands generate an interrupt upon completion and do not return any result bytes. Therefore, it is highly recommended that these control commands be followed by the SENSE INTERRUPT STATUS command; otherwise, valuable interrupt status information will be lost.

READ ID Command

The READ ID command is used to find the present position of the recording heads. The controller stores the values from the first readable ID field into its registers. If the controller does not find an ID address mark on the diskette after the second occurrence of a pulse on the INDEX pin, it sets the IC code of Status Register 0 (ST0) to 01 (abnormal termination), sets the MA bit in register ST1 to 1, and terminates the command.

RECALIBRATE Command

Upon power up, the software must issue a RECALIBRATE command for proper initialization of all drives and the controller. This command causes the read/write head within the controller to retract to the track 0 position. The controller clears the contents of the Present Cylinder counter, and checks the status of the TRK0 pin from the floppy drive.

As long as the TRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the TRK0 pin goes high, the Seek End (SE) bit in Status Register 0 (ST0) is set to a 1 and the command is terminated. If the TRK0 pin is still low after 79 step pulses have been issued, the controller sets the SE and EC (Equipment Check) bits of ST0 to 1 and terminates the command.

Disks capable of handling more than 80 tracks per side may require more than one RECALIBRATE command to return the head to physical track 0.

During the command phase of the RECALIBRATE operation, the controller is in the busy state, but during the execution phase it is in nonbusy state. At this time another RECALIBRATE command may be issued, and parallel recalibrate operations may be done on up to four drives at once.

The RECALIBRATE command does not have a result phase; therefore, a SENSE INTERRUPT STATUS command must be issued after RECALIBRATE to terminate the command and verify the head position (Present Cylinder Number or PCN). If a SENSE INTERRUPT STATUS is not issued, the drive will continue to be busy and may affect the operation of the next command.

SEEK Command

The read/write head within the drive is moved from track to track under the control of the SEEK command. The FDC compares the Present Cylinder Number (PCN), which is the current head position, with the New Cylinder Number (NCN). If PCN is not equal to NCN, the direction signal to drive is set to 1 (step in) and step pulses are issued.

The rate at which step pulses are issued is controlled by the Step Rate Time (SRT) parameter. After each step pulse is issued, NCN is compared to PCN. If they are equal , the SE bit in Status Register 0 (ST0) is set to 1 and the command is terminated.

During the command phase of a SEEK or RECALIBRATE operation, the FDC is in Busy state, but during the execution phase it is in Nonbusy state.

Note that if implied seek is not enabled, the read and write commands should be preceded by the following control commands:

1. SEEK command: Step to proper track.
2. SENSE INTERRUPT STATUS command: Terminate the SEEK command.
3. READ ID command: Verify that the head is on the proper track.

Since the SEEK command does not have a result phase, the user must immediately follow it with a SENSE INTERRUPT STATUS command to terminate the command and verify the head position (Present Cylinder number or PCN). The HDSEL bit in ST0 always returns 0. If a SENSE INTERRUPT STATUS is not issued, the drive will continue to be busy and may affect the operation of the next command.

SENSE INTERRUPT STATUS Command

The 82C735 generates an interrupt signal on the FINTRQ pin for one of the following reasons:

- Entering the result phase of one of the following commands:

  READ DATA
  READ TRACK
  READ ID
  READ DELETED DATA
  WRITE DATA
  FORMAT TRACK
  WRITE DELETED DATA
  VERIFY

- End of SEEK, RELATIVE SEEK, or RECALIBRATE command
- FDC requires a data transfer during the execution phase in the non-DMA mode.

The SENSE INTERRUPT STATUS command resets the interrupt signal and identifies the cause of the interrupt via the IC code and SE bit of Status Register 0 (see the following table).

SENSE INTERRUPT STATUS CODES

SE Bit	IC Code	Cause of Interrupt
0	11	Polling
1	00	Normal termination of SEEK or RECALIBRATE command
1	01	Abnormal termination of SEEK or RECALIBRATE command

If a SENSE INTERRUPT STATUS command is issued when no active interrupt condition is present, Status Register 0 (ST0) will return a value of 80H (invalid command). A SENSE INTERRUPT STATUS command must be issued immediately after a SEEK, RELATIVE SEEK, or RECALIBRATE command, since these commands have no result phase. The SENSE INTERRUPT STATUS command terminates these commands and verifies the head position (Present Cylinder Number or PCN). The HDSEL bit in ST0 always returns 0. If a SENSE INTERRUPT STATUS is not issued, the drive will continue to be busy and may affect the operation of the next command.

SENSE DRIVE STATUS Command

SENSE DRIVE STATUS obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. Status Register 3 (ST3) contains the drive status information.

SPECIFY Command

The SPECIFY command sets the initial values for each of the three internal timers, as shown in the table on the next page. The Head Unload Time (HUT) defines the interval from the end of the execution phase of a read or write command to the head unload state. The Step Rate Time (SRT) defines the interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the spacing between the remaining step pulses.

The Head Load Time (HLT) defines the interval between the time the Head Load signal goes high and the start of the read or write operation. The values, shown in the table on the next page, change with the data rate speed selection. The values are the same for MFM and FM.

SPECIFY COMMAND DRIVE CONTROL DELAYS

	Head Unload Time (msec)			
	1M	**500k**	**300k**	**250k**
0	128	256	426	512
1	8	16	26.7	32
——	——	——	——	——
E	112	224	373	448
F	120	240	400	480
	Step Rate Time (msec)			
	1M	**500k**	**300k**	**250k**
0	8.0	16	26.7	32
1	7.5	15	25.0	30
——	——	——	——	——
E	1.0	2	3.33	4
F	0.5	1	1.67	2
	Head Load Time (msec)			
	1M	**500k**	**300k**	**250k**
00	128	256	426	512
01	1	2	3.3	4
02	2	4	6.7	8
——	——	——	——	——
7E	126	252	420	504
7F	127	254	423	508

The choice of DMA or non-DMA operations is made by the DMA bit. When this bit is 1, the non-DMA mode is selected; when it is 0, the DMA mode is selected. In the DMA mode, data transfers are signaled by the DRQ pin. Non-DMA mode uses the RQM bit and the FINTR pin to signal data transfers.

CONFIGURE Command

CONFIGURE is issued to select the special features of the controller. A CONFIGURE command need not be issued if the default values of the controller meet the following system requirements:

- EIS—No implied seeks
- EFIFO—FIFO disabled
- POLL—Polling enabled
- FIFOTHR—FIFO threshold set to 1 byte
- PRETAK—Precompensation set to Track 0

EIS: Enable Implied Seek—When set to 1, the controller performs a SEEK operation before executing a read or write command. EIS defaults to “no implied seek”.

EFIFO: FIFO Enable—A 1 puts the FIFO into the 765A compatible mode in which the FIFO is disabled (default). This means data transfers are asked for on a byte-by-byte basis. The threshold defaults to 1.

POLL: Drive Polling—POLL defaults to 0, polling enabled. In this state, a single interrupt is generated after a RESET. No polling occurs during Head Load and Head Unload delays.

FIFOTHR: FIFO Threshold—FIFOTHR is the FIFO threshold in the execution phase of a read or write command. It is programmable from 1 to 16 bytes, with a default of one byte. A 00 selects one byte; FF selects 16 bytes.

PRETRK: Precompensation Start Track Number— PRETRK is programmable from track 0 to 255 and defaults to track 0. A 00 selects track 0; FF selects track 255.

VERSION Command

The VERSION command checks to see if the controller is an enhanced type or the older type (765A). If an enhanced FDC is used, a value of 90H is returned as the result byte. No interrupts are generated.

RELATIVE SEEK Command

This command is coded the same as SEEK, except for the MSB of the first byte and the DIR bit.

DIR bit	Head Step Direction Control 0 = Step head out 1 = Step head in
RCN	Relative Cylinder Number. RCN determines how many tracks to step the head in or out from the current track number.

The RELATIVE SEEK command differs from the SEEK command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The SEEK command is good for drives that support a maximum of 256 tracks.

RELATIVE SEEK commands cannot be overlapped with other RELATIVE SEEKs. Only one RELATIVE SEEK can be active at a time. Bit 4 (EC) of Status Register 0 (ST0) sets if a RELATIVE SEEK attempts to step outward beyond track 0.

As an example, assume that a floppy drive has 300 usable tracks, that the host needs to read track 300, and that the head is on any track (0 to 255). If a SEEK command is issued, the head will stop at track 255.

If a RELATIVE SEEK command is issued, the controller will move the head the specified number of tracks, regardless of the internal cylinder position register (but would increment the register). The maximum count that the head can be moved with a single RELATIVE SEEK command is 256 (D). If the head is on track 40 (D) when the RELATIVE SEEK is issued, the controller will move the head to track 296 (D) maximum, which is the initial track plus 256 (D). Functionally, the controller starts counting from 0 again as the track number goes above 255 (D). As the cylinder number crosses track 255, the internal register Present Cylinder Number (PCN) will overflow and contain 40 (D). The resulting PTR value will thus be [(NCN+PCN) mod 256].

The user must compensate for controller functions when accessing tracks greater than 255 (precompensation track number). The controller does not know that it is working in an "extended track area" (greater than 255).

Any command except RECALIBRATE uses the current PCN value. RECALIBRATE only looks for the Track 0 signal and will return an error if the head is positioned farther than 79 steps, since it is limited to issuing a maximum of 80 step pulses. In this case, a second RECALIBRATE command should be issued.

The SEEK command and the implied seeks function correctly within the 44(D) track area (299 to 255) of the "extended track area". Do not issue a new track position that would exceed the maximum track present in the extended area. To return to the standard floppy range of tracks (0-255), issue a RELATIVE SEEK to cross the track 255 boundary.

A RELATIVE SEEK can be used instead of the normal SEEK, but the host is required to calculate the difference between the current head location and the new target head location. This may require the host to issue a READ ID command to ensure that the head is physically on the track that the software assumes it to be on. Different controller commands return different cylinder results, and it may be difficult for the software to track them without the READ ID command.

DUMPREG Command

The DUMPREG command is designed to support system run time diagnostics and application software development and debugging.

PERPENDICULAR MODE Command

The PERPENDICULAR MODE command should be issued prior to executing read/write/format commands that access a disk drive with perpendicular recording capability. With this command, the length of the GAP2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives.

The table on the following page describes the effects of the WG and GAP bits for the PERPENDICULAR MODE command. Upon a reset, the controller will default to the conventional mode (WG = 0, GAP= 0). Selection of the 500kbps and 1Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register (DRSR). The user must ensure that the two data rates remain consistent.

The GAP2 and VCO timing requirements for perpendicular recording drives are dictated by the design of the read/write head. In the design of this head, a pre-erase precedes the normal read/write head by a distance of 200 micrometers. This is about 38 bytes at a 1Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head, since it has not been activated. To accommodate this head activation and deactivation time, the GAP2 field is expanded to a length of 41 bytes.

When the controller reads back, it must begin synchronization at the beginning of the Sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the GAP2 field. But when the controller operates in the 1Mbps perpendicular mode (WG = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased GAP2 field size. For both cases, an approximate two-byte cushion is maintained from the beginning of the Sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For write data, the controller activates the Write Gate signal at the beginning of the Sync field in the conventional mode. Then it writes a new Sync field, Data Address Mark, Data Field, and CRC in IBM format MFM (see the preceding table titled "Formats Supported by the 82C735"). With the pre-erase head of the perpendicular drive, the write head must be activated in the GAP2 field to insure a proper write of the new sync field. In the 1Mbps perpendicular mode (WG = 1, GAP = 1), the controller writes 38 bytes in the GAP2 space. In the 500kbps perpendicular mode (WG = 1, GAP = 0), where the bit density is proportional to the data rate, the controller writes19 bytes in the GAP2 field.

Note that none of the alterations in GAP2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. From the user's viewpoint, the software behavior of the controller does not change when the PERPENDICULAR MODE command is invoked.

EFFECTS OF WG AND GAP ON PERPENDICULAR MODE COMMAND

GAP Bit	WG Bit	Mode	VCO Low Time After Index Pulse (bytes)	Length of GAP2 Format Field (bytes)	Part of GAP2 Written by Write Data (bytes)	GAP2 VCO Low Time for Read (bytes)
0	0	Conventional	33	22	0	24
0	1	500 kbps Perpendicular	33	22	19	24
1	0	Reserved	33	22	0	24
1	1	1Mbps Perpedicular	18	41	38	43

SCAN Commands

The controller recognizes three SCAN commands: SCAN EQUAL, SCAN LOW OR EQUAL, and SCAN HIGH OR EQUAL. These commands enable the FDC to compare data read from a diskette with data supplied by the CPU or DMA controller. The FDC uses ones complement arithmatic (00 = lowest number, FF = highest number) to make the comparison.

Note: An overrun will occur (OR bit in ST1 sets) and the SCAN command will terminate if the FDC does not receive the data from the CPU or DMA controller within 27µs in FM mode or 13µs in MFM mode.

The controller scans each byte in a sector of data for one of the following conditions:

- Scan equal: $D_{fdc} = D_{cpu}$
- Scan low or equal: $D_{fdc} \leq D_{cpu}$
- Scan high or equal: $D_{fdc} \geq D_{cpu}$

where D_{fdc} is floppy disk data and D_{cpu} is processor data.

If the sector does not meet the conditions of the SCAN command, the controller increments the sector number by one and proceeds to the next sector. Scanning continues until the controller finds a sector that satisfies the conditions (a *hit*), reaches End of Track (EOT), or receives a Terminal Count signal from the host.

If the controller has a hit, it sets the Scan Hit (SH) bit of Status Register 2 (ST2) to 1 and terminates the SCAN command. If it does not have a hit before reaching EOT, it sets the Scan Not Satisfied (SN) bit of ST2 to 1 and terminates the SCAN command. Receiving a Terminal Count signal from the CPU or DMA also causes the controller to end the command, but the controller first completes scanning of the current byte.

The following table gives SN and SH bit values for all conditions of the SCAN command.

SN AND SH BIT VALUES FOR SCAN CONDITIONS

Scan Command	Scan Conditions	ST2 BitValues	
		SN	SH
Scan Equal	$D_{fdc} = D_{cpu}$	0	1
	$D_{fdc} \neq D_{cpu}$	1	0
Scan Low or Equal	$D_{fdc} = D_{cpu}$	0	1
	$D_{fdc} < D_{cpu}$	0	0
	$D_{fdc} \ngtr D_{cpu}$	1	0
Scan High or Equal	$D_{fdc} = D_{cpu}$	0	1
	$D_{fdc} > D_{cpu}$	0	0
	$D_{fdc} \nless D_{cpu}$	1	0

The setting of the SCAN command's SK bit determines FDC response in the event it encounters a Deleted Data Address mark (DDA) on one of the sectors. If the SK bit is 0, the controller sets the Control Mark (bit 6) of register ST2 to 1 (high) and ends the SCAN command. If SK is 1, the controller skips the sector containing the DDA mark, sets the CM bit to 1 to show that it has encountered a deleted sector, and proceeds to scan the next sector.

When Multitrack (MT) or Sector Increment (SI) is used, it is important to remember that *the controller must read the last sector of the track.* Hence, the first and last sectors to be read must be consistent with the setting of MT and SI. Suppose, for example, that alternate sector reads are programmed (SI = 02 and MT = 0), that the first sector to be read is sector 23, and that the last sector to be read is 28. The controller will read sectors 23, 25, and 27, skip EOT on sector 28, and terminate the SCAN command abnormally at the index hole. If the first sector had been 22 or the last sector had been 27, the controller would have reached EOT and completed the SCAN command normally.

Functional Description

This section provides a functional description of the following principal components of the 82C735 controller chip:

- Serial port: NS16550 compatible UART
- Integrated drive electronics interface (IDE)
- 4MB floppy disk controller (FDC)
- Bidirectional parallel port interface (Printgine)
- Power management circuitry
- Mouse port logic

Refer to the following figure for a graphic representation of the 82C735. For register information see "Registers" and the specific register descriptions, e.g., “Serial Port Registers.”

SERIAL PORT (UART)

The 82C735 supports two UARTs for serial to parallel conversion of data characters received from the CPU. The UARTs are equivalent to the PC16555OC/NS1655OAF, which is an improved version of the original NS16450 UART. These UARTs are functionally identical to the NS16450 on powerup, or they can be reset to NS16450 mode under software control.

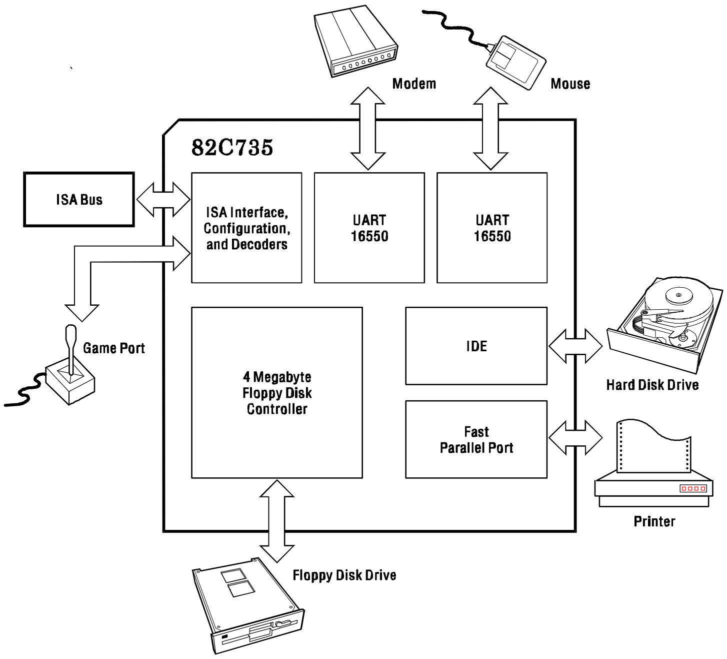
The UARTs can also be put into FIFO mode to relieve the CPU of excessive software overhead. In FIFO mode, the internal FIFOs are activated, allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. FIFO mode is described on the following page.

Each of these serial ports functions as a serial data I/O interface in a microcomputer system and is completely independent. The functional configuration of the UARTs is under system software control.

The CPU can access UART status at any time by reading the appropriate 82C735 status register. The status information reported includes the type and condition of the transfer operation being performed by the UART, as well as error conditions like parity, overrun, framing, or break interrupt.

The UARTs have a programmable baud rate generator that is capable of dividing the internal reference clock by divisors of 1 to (2^{16} - 1) and producing a 16x clock for driving the transmitter logic. This 16x clock can also be used to drive the receiver logic. For a description of the baud rate generator, see “Serial Port Registers.”

The UARTs have complete modem control and a prioritized interrupt system. Interrupts can be programmed to the user’s requirements to minimize the computing required to handle the communications link.



82C735 System Organization

FIFO Interrupt Mode Operation

Each serial channel has two 16-byte FIFOs associated with it. The operational description that follows is applicable to the FIFOs of both channels.

When the RCVR FIFO and Received Data Available Interrupt bits are enabled (FCR0 = 1, IER0 = 1) Received Data Available interrupts occur. The Received Data Available interrupt is issued to the CPU when the number of bytes in the RCVR FIFO equals the programmed trigger level. It is cleared as soon as the number of bytes in the RCVR FIFO drops below the trigger level.

The Received Data Available indication from the Interrupt Identification Register also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

The Receiver Line Status interrupt (IIR = 06), as before, has higher priority than the Received Data Available interrupt (IIR = 04).

The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the RCVR FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO Timeout interrupts can occur if the following conditions exist:

- At least one character is in the RCVR FIFO.
- The most recent serial character was received more than four continuous character times ago. (If two stop bits are programmed, the second one is included in this time delay.)
- The most recent CPU read of the RCVR FIFO was received more than four continuous character times ago.

The maximum time between a received character and a timeout interrupt is 160ms at 300 baud, with a 12-bit receive character (i.e., 1 START, 8 DATA, 1 PARITY and 2 STOP bits). Character times are calculated by using the baud rate generator clock as the the clock signal. This makes the delay proportional to the baud rate.

A timeout interrupt is cleared and the timer reset when the CPU reads one character from the RCVR FIFO. When the timeout interrupt indication is inactive, the timeout indication timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

Transmit (XMIT) interrupts can occur when the XMIT FIFO interrupts are enabled (FCR0 = 1, IER1 = 1). The Transmitter Holding Register Empty (THRE) interrupt occurs when the XMIT FIFO is empty. It is cleared as soon as the IIR register is read or the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while this interrupt is being serviced).

Transmitter FIFO empty indications are delayed one character time minus the last stop bit time whenever THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. This delay prevents the UART from issuing a second THRE interrupt as soon as it transfers the first character into the transmitter shift register. The first THRE interrupt occurs immediately after FCR0 is changed, assuming FCR0 is enabled.

Character Timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt. XMIT FIFO Empty has the same priority as the current THRE interrupt.

FIFO Polled Operation

With FCR0 = 1, resetting any or all of bits 3-0 of the Interrupt Enable Register puts the associated serial channel in the FIFO polled mode of operation. Since the receiver and transmitter are controlled seperately, either one or both can be in the polled mode of operation. In this mode, the program will check receiver and transmitter status via the LSR.

- LSR0 is set as long as there is one byte in the RCVR FIFO.
- LSR1 to LSR4 specifies which error(s) has occurred. Character error status is handled the same way as in the interrupt mode.
- LSR5 indicates when the XMIT FIFO is empty.
- nLSR6 indicates that both the XMIT FIFO and shift register are empty.
- LSR7 indicates whether there are any errors in the RCVR FIFO.

In the FIFO polled mode, no trigger level reached or timeout condition is indicated; however, the RCVR and XMIT FIFOs are otherwise functional.

INTEGRATED DRIVE ELECTRONICS INTERFACE (IDE)

The 82C735 supports AT and XT embedded controller hard disk drives. The chip provides the following control signals for the IDE interface and the IDE buffers:

- IDEENLO#: Low byte buffer enable (AT and XT)
- IDEENHI#: High byte buffer enable (AT only)
- HDCS0#: Primary hard disk chip select. Task file register access
- HDCS1#: Secondary hard disk chip select (AT and XT)
- IOCS16#: I/O channel select 16. 16-bit I/O transfer indication (AT only).
- IDED7: IDE data bit 7. This bit is directly connected to data bit D7 of the IDE interface connector (AT only).
- HDACK#: Hard disk DMA acknowledge (XT only)

The 82C735 IDE interface operates in XT and AT modes. AT mode supports programmed I/O only (8 and 16 bits). XT mode supports only 8-bit DMA and 8-bit programmed I/O.

In AT mode, the IDE interface supports both the primary and secondary address ranges in a PC/AT system. The address is selected by means of Configuration Register CR05H, bit 4. The following table lists the addresses supported by the IDE interface.

IDEENLO# becomes active when the 82C735 decodes the addresses shown in the following table in AT mode, or 320-323H and DMA transfers (HDACK# = 0) in XT mode.

IDEENHI# becomes active only when IOCS16# is active in the address range 1F0H-1F7H (primary) or 170H-177H (secondary) in AT mode (CR00H, bit1=1).

IOCS16# is generated by the hard disk controller when it requires a 16-bit transfer.

IDED7 should be connected directly to data bit D7 of the IDE interface.

IOCS16#/HDACK# is a multiplexed pin. IOCS16# is valid in AT mode and HDACK# in XT mode.

IDE INTERFACE ADDRESS SUPPORT

System	Type	Addresses	Setup
AT	Primary	1F0-1F7H, 3F6-3F7H	CR05H=0
AT	Secondary	170-177H, 376-377H	CR05H=1
XT	Primary only	320H-323H	—

AT Mode

In AT mode, the normal transfer mode is 8-bit. Transfers of 16 bits are performed using the 16-bit data register when IOCS16# is active. Both IDEENLO# (low buffer enable) and IDEENHI# (high buffer enable) are active during 16-bit transfers.

HDCS0# is active whenever the 82C735 decodes I/O addresses 1F0-1F7H (primary range) or 170-177H (secondary range).

IDEENLO# is active on all AT mode addresses. On the low byte buffer, only seven bits (0-6) are connected to the data bus. Bit 7 is a special case; it is driven by the 82C735 to the host interface. On the IDE interface, IDED7 is connected directly to the connector.

Normally, the 82C735 functions as a buffer for bit 7, but upon reading 3F7H (377H in secondary), the chip tristates bits 0-6, enables IDEENLO# to transfer bits 0-6 from the IDE host, and supplies bit 7 to the host via the floppy disk interface.

XT Mode

In XT mode, the IDE interface supports only 8-bit programmed I/O or DMA; it does not support 16 bits. Normally, DMA transfer is done from the data register (320H) only. During a DMA cycle (indicated by active AEN and HDACK#), pin IDEENLO# is active, allowing the data to flow through the low byte buffer. The XT mode decodes I/O address range 320H-323H.

FLOPPY DISK CONTROLLER

The 82C735 contains an enhanced floppy disk controller (FDC) that is suitable for PC/AT, EISA, and general-purpose applications. The core is compatible with the NEC uPD72065B and is software compatible with the 82077SL. Key features include a 16-byte FIFO, which allows better system performance in multi-master systems; support for perpendicular recording (4MB floppy support); and a high-performance digital data separator.

In addition, the FDC contributes to the overall power management features of the 82C735 through a direct powerdown mode controlled by software. This feature achieves powerdown without dependence on external factors and is designed to be transparent to all application software.

Precompensation Circuitry

The FDC supports data rates of 250Kb/s, 300Kb/s, 500Kb/s, and 1Mb/s. The 1Mb/s data rate is applicable to the high performance tape and floppy disk drives on today's market. The FDC programmable write precompensation circuitry defaults to 125ns for the 250, 300 and 500Kb/s data rates and to 41.67ns for the 1Mb/s data rate.

Perpendicular Recording Support

The new 2.88MB and 4MB floppy drives, which run at 1MB/s, employ perpendicular recording, a new format that is fully supported by the FDC. Unlike the traditional longitudinal method, perpendicular recording orients the magnetic bits vertically to achieve higher bit densities.

Digital Data Separator

The 82C735 has a high-performance on-chip digital data separator (DDS), which consists of a digital phase lock loop, phase detector, a ROM lookup table, and a programmable fractional counter. The data separator needs no external components and is compatible with the strict data separator requirements of floppy and tape drives.

The function of the data separator is to lock onto the incoming serial read data. When lock is achieved, the serial front-end logic of the FDC is provided with a clock, which is synchronized with the read data. The synchronized clock, called a *data window*, is used to sample the serial data internally. One state of the data window samples the data portion of the bit cell; the alternate state samples the clock portion. Serial-to-parallel conversion logic separates the read data into clock and data bytes.

The 24MHz reference clock is divided by N to provide a 16x clock to the pulse recognition logic. This clock is the reference for the speed tracking circuit. The adjustment logic uses a lookup table to provide a correction of +/- 1/8 of the reference clock. The comparator will correct incoming pulses in five ranges: normal, late, very late, early, and very early.

Pulse counts in the normal range are not changed. Pulse counts in the early and late ranges are corrected by +/- 1/8 of the clock at the end of the count. Pulse counts in the very early and very late ranges are immediately corrected by +/- 1/8 of the clock.

Powerdown Mode

Direct powerdown results in immediate powerdown of the FDC section of the 82C735, without regard to the current state of the part. Powerdown is conducted via bit 6 of the DSR register. Programming this bit high powers down the FDC after the part is internally reset. All current status is lost when the powerdown mode is invoked.

Powerdown mode can be exited only by a hardware or software reset. After reset, the FDC goes through a normal drive status initialization sequence. The FIFO mode is set to default unless the LOCK command has blocked it (see “FDC Command Set”). After a delay, the polling interrupt is issued.

Integrated Circuity

The AT bus interface circuitry is completely integrated with the 82C735 circuitry with 24mA drive capability, thus no external logic is required. In addition, 48mA floppy interface buffers allow direct connection of the 82C735 to the floppy drive.

Drive Interface

All drive outputs have 40mA drive capability, and all inputs use a receive buffer with hysterisis. The internal digital data separator requires no external components, yet it permits an extremely wide capture range with high levels of read-data jitter and instantaneous speed variations. The drive signals can be directly connected to a floppy drive.

PARALLEL PORT INTERFACE (PRINTGINE)

The parallel port interface operates in the following modes:

- Standard: ISA style Centronics unidirectional
- Bi-di: PS/2 style bidirectional
- Fast Centronics: high-speed bidirectional
- EPP: enhanced bidirectional
- ECP: extended capabilities bidirectional

The ISA-style Centronics mode features a single-byte unidirectional output port. It is fully compatible with ports in IBM PC, XT, AT, and compatible machines. The PS/2 style mode features a bidirectional single-byte port. Read access to peripherals is possible in this mode. These two modes operate without a FIFO and maintain compatibility with existing printing protocols. Data transfers are controlled through interrupts or polling.

The fast Centronics, EPP, and ECP protocols operate with a FIFO for high performance. These modes are capable of data transfer rates from 200Kb/sec for the fast Centronics mode to 2MB/s for the EPP and ECP modes.

High-speed performance improvements result from the following design enhancements:

- Protocols are implemented in hardware to eliminate the significant overhead of parallel port protocols.
- DMA is used to offload the processor from data transfer overhead and interrupt service, if interrupt driven.
- A FIFO is used to reduce processor/DMA bus utilization.

The 82C735 parallel port can be disabled or configured as LPT1:, LPT2:, or LPT3:. The parallel port protocols are fully controlled by software. All the data, status, control, and extended control registers are direct CPU I/O space ports. The 82C735 is capable of driving the parallel interface directly with no external buffers.

Operation in Standard Mode

In standard mode, the interface functions as a unidirectional parallel port and is normally used to connect a printer or plotter. The 82C735 selects the printer by asserting SLCTIN#. If a device is connected and the selection is properly made, the device asserts SLCT to confirm the selection. The 82C735 then asserts INIT# to initialize the printer. If an error is encountered during initialization or normal operation, the printer asserts ERROR# . The printer or plotter can also notify the controller that it is out of paper by asserting PE.

During normal operation, the printer asserts BUSY (high) when it is not ready to receive data from the controller. When it has finished processing the data, the printer asserts ACK# (low) and deasserts BUSY (low). If interrupts are enabled, deasserting ACK# (high) generates an interrupt, and the corresponding interrupt service routine functions as a parallel port driver. If interrupts are disabled, the parallel port software must poll the status register to determine when the ACK# is pulsed.

The parallel port driver outputs valid data on the printer data pins and asserts STROBE# after an appropriate data stabilization interval. STROBE# is deasserted after a sufficient setup time has elapsed. Valid data can then be read from the port after a hold time has elapsed.

Operation in Bi-Di Mode

A write operation in bi-di mode is similar to that in standard mode except that data can be read (input) from the parallel port. During a parallel port read cycle, data available on the parallel port bus is driven on to the system bus.

Operation in Fast Centronics Mode

Fast Centronics mode has standard protocols as well as bidirectional capability. It achieves significantly higher performance by implementing some of the software controlled handshaking in hardware, and by using a FIFO to reduce the system overhead.

When the parallel port driver outputs valid data on the printer data pins, the hardware automatically asserts STROBE#. The printer then asserts BUSY to indicate that it is not ready to receive data. Once the printer deasserts BUSY, the hardware automatically deasserts STROBE# and is ready for the printer driver to output another byte of data.

If the FIFO is used, the parallel port driver can deposit up to 128 bytes in the FIFO and wait for it to be emptied before coming back to provide another chunk of data. All other operations are the same as in standard mode.

Operation in EPP Mode

The Enhanced Parallel Port (EPP) mode is a high-speed bidirectional protocol. It differs slightly from standard mode in attempting to achieve a SCSI-like (multiple device) capability, sharing the existing parallel port signals. The EPP protocol requires significant modifications to the existing software drivers. The software layer on top of the physical layer has been defined.

In EPP mode initialization, printer selection and error reporting work the same as in standard mode. The difference is that the SLCTIN# and AUTOFD# signals are automatically generated and become address strobe (ASTRB#) and data strobe (DSTRB#), respectively, enabling direct access to the parallel port devices. An automatic address strobe is generated when data is read or written to the address port of the EPP interface; an automatic data strobe is generated when data is read or written to the data port. Thus, the parallel port devices can be accessed without the software loops required for standard implementations.

The output drivers on the control port are made to be TTL drivers, driving both up and down. The TTL drivers enable the port to run faster than the open-drain drivers of the standard port.

Operation in ECP Mode

The Extended Capabilities Parallel Port mode (ECP) is another high-speed bidirectional protocol that is implemented in hardware to reduce software and system overhead. This protocol uses a fully asynchronous handshake to complete data transfers.

In ECP mode, initialization, printer selection, and error reporting work the same as in standard mode. However, during data transfers, signals HOSTCLK and PERACK are used to handshake for a write operation, and PERCLK and HOSTACK are used to handshake for a read operation. ECP mode also uses the FIFO and DMA to improve throughput of the parallel port.

FIFO Implementations

All high-speed protocols use the FIFO. The parallel port interface implements a FIFO that allows bytes to be transferred between memory and the parallel port. This reduces the processor (programmed I/O) memory access and bus arbitration (DMA) overhead.

The 82C735 implementation uses a 128-byte FIFO. Management and control of the FIFO depends on the data transfer mechanism employed and the direction of transfer. The FIFO can operate during a write or a read operation, but only in one direction at a time. For a description of forward and reverse operations, see "ECP Parallel Port FIFO Timing" in the section "Electrical Specifications."

DMA Uses

DMA can be used to sequence the memory and I/O cycles required to transfer data between system memory and the parallel port. It must be initialized (starting address, transfer length, mode, etc.) prior to enabling the DMA handshake in the parallel port sequencer.

All ISA DMA transfers employ a 128-byte FIFO. The FIFO improves ISA bus utilization by allowing burst (demand) mode operation.

POWER MANAGEMENT CIRCUITRY

Power management functions are achieved with the PWRGD signal and configuration register bits. The configuration and register data can be retained during sleep mode with minimum current drain, which makes the 82C735 ideal for laptop environments. In addition, the configuration registers can be programmed to disable or power down each port of the 82C735. This feature enhances the flexibility of the chip in system integration.

For any system, the three typical power management operating modes are active, sleep, and powerdown. Applications of these modes are discussed in the following sections.

Active Mode

In active mode the 82C735 is powered down by a power supply (through an AC outlet), or by a main battery (NiCd) if the chip is used in a laptop application. The configuration registers are initialized by the system BIOS. The software BIOS can be used to power off selected resources when needed to reduce total power consumption.

Sleep Mode

In a laptop application, the main battery has a life of 4 to 12 hours. To save battery energy, the system can be put in sleep mode, which draws minimum current.

The 82C735 supports sleep mode through the PWRGD pin and bits 5 and 6 of configuration register CR00H. These bits are the serial port and floppy oscillator enable and function as follows:

Bit 6	Bit 5	
0	0	Oscillator is always ON regardless of the PWRGD state (default).
0	1	Oscillator is ON when PWRGD is high, otherwise it is OFF (tristated).
1	0	Oscillator is ON when PWRGD is high, otherwise it is OFF (tristated).
1	1	Oscillator is always OFF.

To implement sleep mode, program bits 5 and 6 of CR00H as either 0,1 or 1,0 so that the oscillator will turn off when PWRGD is deasserted. This will minimize the current drawn by the serial and FDC ports. PWRGD is deasserted by user-designed sleep mode circuitry.

In sleep mode the 82C735 isolates itself from the rest of the system. All outputs are tristated, all inputs are disabled, and all commands are ignored until PWRGD is restored to the active state (wake up).

Powerdown Mode

Power is completely removed from the system when the 82C735 is in powerdown mode. The programmed configuration register data is not retained. The configuration registers are restored by the system BIOS.

The enable/disable and powerup/powerdown bits for each port are summarized below.

Serial Port 1: CR02H

Bit 3	1 = Power up (default) 0 = Power down
Bit 2	1 = Enabled (default) 0 = Disabled

Serial Port 2: CR02H

Bit 7	1 = Power up (default) 0 = Power down
Bit 6	1 = Enabled (default) 0 = Disabled

Parallel Port: CR01H

Bit 2	1 = Power up (default) 0 = Power down
Bits 1:0	0,0 = Disabled 0,1 = Enabled 1,0 = Enabled 1,1 = Enabled

Floppy Port: CR00H

Bit 4	1 = Enabled (default) 0 = Disabled
Bit 3	1 = Power up (default) 0 = Power down

IDE Port: CR00H

Bit 0	1 = Enabled (default) 0 = Disabled

Mouse Port: CR06H

Bit 1	1 = Enabled 0 = Disabled (default)
Bit 0	1 = Powerdown (default) 0 = Power up

Note: Serial Port 2 has to be disabled and powered down for the mouse to operate.

MOUSE PORT

From a hardware perspective, the 82C735 mouse port looks like a PS/2 mouse port. The base address for the mouse port registers are set up using configuration register CR07H. On power up, this register comes up as CR00H, which disables the mouse port. The mouse port is enabled only when an address is written to it (see "Mouse Port Registers").

The following paragraphs contain software support specifications for the mouse.

Adding Extended BIOS Data Area

To run a PS/2 mouse in a PC environment, add the following extended BIOS data area to the standard BIOS:

```
Bios_Data_Area      SEGMENT AT 40H
Extended_BDA        DW ?       ;OE  Extended BDA
                               ;segment
Bios_Data_Area      ENDS
```

The extended BIOS data area contains variables that are used by the various BIOS functions. The location and content of the variables must be consistent with the IBM BIOS for complete compatibility. Refer to the following Extended BIOS Data Area table.

The extended area starts at the segment indicated by the Extended_BDA variable in the BIOS data area. This segment is usually the highest 1K of RAM; however, it is best to use the variable to refer to the extended BIOS data area and not make assumptions about its location.

The extended area supports the interrupt 15 function called C2. This function and its subfunctions (01 to 07) are discussed under "Function C2—Pointing Device Interface."

Function C2—Pointing Device Interface

AL must be in the range 00-07 or this routine should return AH = 01 and carry set. If AL is in this range, follow the procedures outlined below for the C2 subfunctions.

EXTENDED BIOS DATA AREA

Ex_BIOS_Data_Area	Segment	Paragraph	Description
EXBDA_size	DW	?	00 Size of Extended_BDA
	DB	21H DUP(?)	02 Reserved
Variables			
Pointer_Driver	DD	?	22 Pointer support routine
Pointer_Info1	DB	?	26 Pointer flag 0
Pointer_Info2	DB	?	27 Pointer flag 1
Pointer_Data	DB	8 DUP(?)	28 Reserved
	DB	0BH DUP(?)	30 Reserved
Keyboard_Type	DB	?	3B Keyboard type byte
BAT_Flag	DB	?	3C BAT complete flag

Subfunction 00: Enable/Disable Pointer

Entry:	AL = 00	;Enable/disable pointer
	BH = 00	;Disable
	BH = 01	;Enable
Exit:	AH	;Status returned
	CF	;Error status returned

If BH is neither 00 nor 01, return with AH = 01 and carry set. If BH is 00 (disable), set the Command in Progress bit of Pointer_info1 and then send a POINTER DISABLE command (F5) to the pointer (see "Sending a Command to the Pointer").

If BH is 01 (enabled), test to see if the user call is installed (bit 7 of Pointer_Info2). If this bit is not set, return AH = 05 with carry set (no driver installed). Otherwise, send a POINTER ENABLE command (F4) to the pointer.

Set the Pointing Device Interrupt Enable bit (bit 4) in the mouse status/control port (refer to "Mouse Port Registers").

Subfunction 01: Reset Pointing Device

Entry:	AL = 01	;Reset pointing device
Exit:	AH	;Status returned
	CF	;Error status returned
	BH	;Device ID

Send a DISABLE POINTER command (F5) to the pointer (see "Sending a Command to the Pointer"). If the command is sent without error, send a RESET command (FF) to the pointer. If an error occurs, read two bytes from the pointer (see "Receiving Data From the Pointer").

Return AL containing the first returned byte (Pointer_Data) and BH containing the second byte (Pointer_Data + 1).

Subfunction 02: Set Sample Rate

Entry:	AL = 02	;Set sample rate
	BH	;Sample rate
Exit:	AH	;Status returned
	CF	;Error status returned

If BH is greater than 06, return AH = 02 with carry set. Otherwise, set the Command in Progress bit of Pointer_info1 and then send a SET SAMPLE RATE command (F1) to the pointer (see "Sending a Command to the Pointer"). If no error occurs, set the Command in Progress bit again and then write the reports-per-second value of the pointer as shown in the following table.

POINTER REPORTS/SECOND VALUES

Sample Rate	Reports/Second
00	0A
01	14
02	28
03	3C
04	50
05	64
06	C8

Subfunction 03: Set Resolution

Entry:	AL = 03	;Set resolution
	BH	;Resolution value
Exit:	AH	;Status returned
	CF	;Error status returned

If the resolution value is above 03, return AH = 02 with carry set. Otherwise, set the Command in Progress bit of Pointer_Info1 and then send a SET RESOLUTION command (E8) to the pointer (see "Sending a Command to the Pointer"). If no error occurs, set the Command in Progress bit again and then write the resolution value to the pointer.

Subfunction 04: Read Device Type

Entry:	AL = 04	;Read device type
Exit:	AH	;Status returned
	CF	;Error status returned
	BH	;Device ID

Send a READ DEVICE TYPE command (F2) to the pointer (see "Sending a Command to the Pointer"). If an error occurs, return AH = 0F with carry set. If no error occurs, read the byte from the pointer (see "Receiving Return Data From the Pointer"). Return BH containing the first byte returned (Pointer_Data).

Subfunction 05: Pointer Device Init

Entry:	AH = 05	;Pointer device initialization
	BH	;Data package size
Exit:	AH	;Status returned
	CF	;Error status returned
	BH	;Device ID

If the package size on entry is above 8 (see the following package size table), return AH = 02 with carry set. Reset bits 0-2 in Pointer_Info2 and replace with the package size bits (BH = 1). Reset the pointer, using the method described in "Subfunction 01: Reset Pointing Device."

Subfunction 06: Extended Functions

Entry:	AL = 06	;Extended commands
	BH = 00	;Return status
	BH = 01	;Set scaling to 1:1
	BH = 02	;Set scaling to 2:1
Exit:	AH	;Status returned
	CF	;Error status returned
	BL	;Status byte 1 (BH = 00)
	CL	;Status byte 2 (BH = 00)
	DL	;Status byte 3 (BH = 00)

If BH is above 02 on entry, return AH = 01 with carry set. If BH = 00 on entry, return the pointer status by sending a READ ID command (E9) to the pointer (see “Sending a Command to the Pointer”). If an error occurs, return AH = 0F and carry set.

Read three bytes from the pointer (see “Receiving Return Data From the Pointer”). Return BH = 00, BI = Pointer_Data, CL = Pointer_Data + 1, DH = 00, and DL = Pointer_Data + 2.

If BH is 01 on entry, set the scaling to 1:1 by sending the printer a SET SCALING TO 1:1 command (E6).

If BH is 02 on entry, set the scaling to 2:1 by sending the printer a SET SCALING TO 2:1 command (E7).

PACKAGE SIZE

Stack Offset	Package Size (bytes)							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0	00	00	00	00	00	00	[03]	[04]
1	00	00	00	00	00	00	Ldata	Ldata
2	00	00	Ldata	Ldata	[02]	[03]	[02]	[03]
3	00	00	00	00	Ldata	Ldata	[05]	[06]
4	00	00	[01]	[02]	[01]	[02]	[01]	[02]
5	00	00	00	00	[03]	[04]	[04]	[05]
6	Ldata	[00]	[00]	[00]	[00]	[00]	[00]	[00]
7	00	Ldata	00	[01]	00	[01]	00	[01]

Notes: Ldata = the last data byte read from the pointer.
[*nn*] = the *n*th byte of the data package (at Pointer_Data) stored in the Extended_BDA.
00 = store zero.

Subfunction 07: Device Driver FAR CALL Initialization

Entry:	AL = 07	;Device driver FAR CALL init
	ES:BX	;Address of routine
Exit:	AH	;Status returned
	CF	;Error status returned.

Place the value of ES:BX in Pointer_Device. If the value in ES:BX is zero, reset the Pointer Device Installed flag. If ES:BX is not zero, set the Pointer Device Installed flag (bit 7) of Pointer_Info2. Return AH = 00 with carry set.

Sending a Command to the Pointer

Configuration register CR07H indicates the data port address for the pointer. This address should be the standard default address for COM2. The value at this location determines the mouse data port and mouse status/control port locations.

Use the following procedure to send a command byte to the pointer device:

1. Set the package size to 7 (see the Package Size table).
2. Set the Pointer Device flag (bit 7) of Pointer_Info2.
3. Reset the Packet Count (bits 0-2 of Pointer_Info1).
4. Set the Command in Progress bit and reset the ACK# and Resend bits of Pointer_Info1.
5. Reset the interface by setting the Mouse Enable (bit 7) and Pointing Device Reset (bit 3) of the mouse status/control port.
6. Reset the Pointing Device Reset (bit 3).
7. Wait until the Pointing Device XMIT Idle bit (bit 2) of the mouse status control port has set.
8. Send the command byte to the mouse by writing the data to the mouse data port.
9. Wait about 250 msec for either the ACK# or Resend bit to set in Pointer_Info1.
10. If the Resend bit is set or a timeout occurs, repeat steps 3 through 8. Three retries are allowed.
11. If ACK# is set and no data is to be returned, restore Pointer_Info2, reset the package count to zero, and exit.
12. If ACK# is set and data is to be returned, follow the procedure in “Receiving Return Data From the Pointer.”

Receiving Return Data from the Pointer

After the command byte has been sent to the pointer, wait until the package count (Pointer_Info1) is equal to the number of bytes requested. Then proceed as follows:

1. Restore Pointer_Info2.
2. Reset the package count to zero (Pointer_Info1).
3. Exit.

Pointer IRQ Handler (Interrupt 73) Procedure

Read the data byte from the mouse data port and check that the Command in Progress flag (bit 7) of Pointer-Info1 is set. Then follow procedure 1, 2 or 3, depending on the byte read and the package size.

1. If the byte read was an Error (FC), ACK# (FA), or Resend (FE), proceed as follows:
   a. Set the corresponding flag (bit 4, 5 or 6) in Pointer_Info1.
   b. Reset the Command in Progress flag (bit 7).
   c. Clear interrupts.
   d. Exit.

2. If the byte read was not an Error, ACK#, or Resend and the current package size (bits 0-2 of Pointer_Info2) is *not* equal to the package count (bits 0-2 of Pointer_Info1), proceed as follows:
   a. Place the byte read in the Extended_BDA of (OFFSET Pointer Data + Pointer_Info1 and 7). This is the current index for the data read.
   b. Increment Pointer_Info1.
   c. Clear interrupts.
   d. Exit.

3. If the byte read was not an Error, ACK#, or Resend and the current package size (bits 0-2 of Pointer_Info2) *is* equal to the package count (bits 0-2 of Pointer_Info1), proceed as follows:
   a. Reset the package count to zero.
   b. Create a stack frame of eight bytes for the data from the Package Size table (given above).
   c. Perform a long call to the user's interrupt routine at Pointer_Device.
   d. On return, remove the stack frame data.
   e. Clear interrupts.
   f. Exit.

Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Minimum	Maximum
Supply Voltage	V_{CC}	3.0V	7.0V
Input Voltage	V_I	-0.5V	5.5V
Operating Temperature (ambient)	T_A	0°C	70°C
Storage Temperature	T_{STG}	-40°C	125°C

Caution: Permanent damage to the device could result if the absolute maximum ratings are exceeded.

Use a clamp circuit if there is danger that voltage spikes may occur on the power supply output, or that voltage transients on the AC power line may appear on the DC output.

CAPACITANCE

T_A = 25°C; V_{CC} = 5V

Parameter	Symbol	Maximum Limit (pF)	Test Condition
Clock Input Capacitance	C_{CLKIN}	20	All pins except the pin under test are tied to AC ground.
Input Capacitance	C_{IN}	10	
Output Capacitance	C_{OUT}	20	

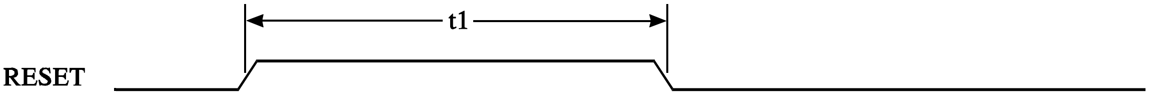
DC ELECTRICAL CHARACTERISTICS

T_A= 0°C to 70°C; V_{CC} = 5V ±0.5V

Buffer	Parameter	Symbol	Min.	Max.	Typical	Unit	Test Condition
I TTL Input	Low Input Voltage Level	V_{ILI}	—	0.8	—	V	
	High Input Voltage Level	V_{IHI}	2.0	—	—	V	
IS Schmitt-trigger Input	Low Input Voltage Level	V_{ILS}	—	0.8	—	V	
	High Input Voltage Level	V_{IHS}	2.2	—	—	V	
	Schmitt-Trigger Hysteresis	HYS	—	—	250	mV	
I_{CLK} Clock Input	Low Input Voltage Level	VILCK	—	0.4	—	V	
	High Input Voltage Level	V_{IHCK}	3.0	—	—	V	
I, IS, I_{CLK}	Input Leakage Current	I_{IL}	-10	20	—	μA	V_I = 0.4V to V_{CC}
O 4mA TTL Output	Low Output Voltage Level	V_{OL}	—	0.4	—	V	I_{OL} = 4mA
	High Output Voltage Level	V_{OH}	2.4	—	—	V	I_{OH} = -1mA
	Output Leakage Current	I_{OL}	-10	20	—	μA	V_O = 0.4V to V_{CC}
OC 16-24mA Open-drain Output	Low Output Voltage Level	V_{OL}	—	0.4	—	V	I_{OL} = 24mA or 16mA
	High Output Voltage Level	V_{OH}	2.4	—	—	V	I_{OH} = -10μA
	Output Leakage Current	I_{OL}	-10	20	—	μA	V_O = 0.4V to V_{CC}
OD 48mA High-current Open-drain Output	Low Output Voltage Level	V_{OL}	—	0.4	—	V	I_{OL} = 48mA
	High Output Voltage Level	V_{OH}	2.4	—	—	V	I_{OH} = -10μA
	Output Leakage Current	I_{OL}	-10	20	—	μA	V_O = 0.4V to V_{CC}
OH 24mA High-current TTL Output	Low Output Voltage Level	V_{OL}	—	0.4	—	V	I_{OL} = 24mA
	High Output Voltage Level	V_{OH}	2.4	—	—	V	I_{OH} = -12mA
	Output Leakage Current	I_{OL}	-10	20	—	μA	V_O = 0.4V to V_{CC}
T 24mA Tristate TTL Output	Low Output Voltage Level	V_{OL}	—	0.4	—	V	I_{OL} = 24mA
	High Output Voltage Level	V_{OH}	2.4	—	—	V	I_{OH} = -12mA
	Output Leakage Current	I_{OL}	-10	20	—	μA	V_O = 0.4V to V_{CC}
	Supply Current Active	I_{CC}	—	40	—	mA	
	Supply Current Standby	I_{STBY}	—	250	—	μA	PWRGD low

RESET TIMING

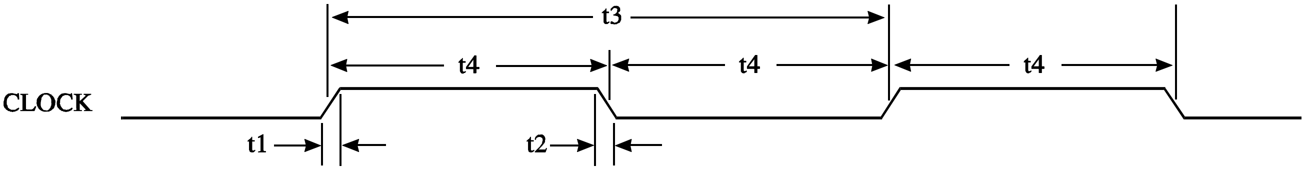
Time	Parameter	Minimum (ns)	Maximum (ns)	Typical (ns)
t1	RESET width	500	—	—



Reset Timing

CLOCK TIMING

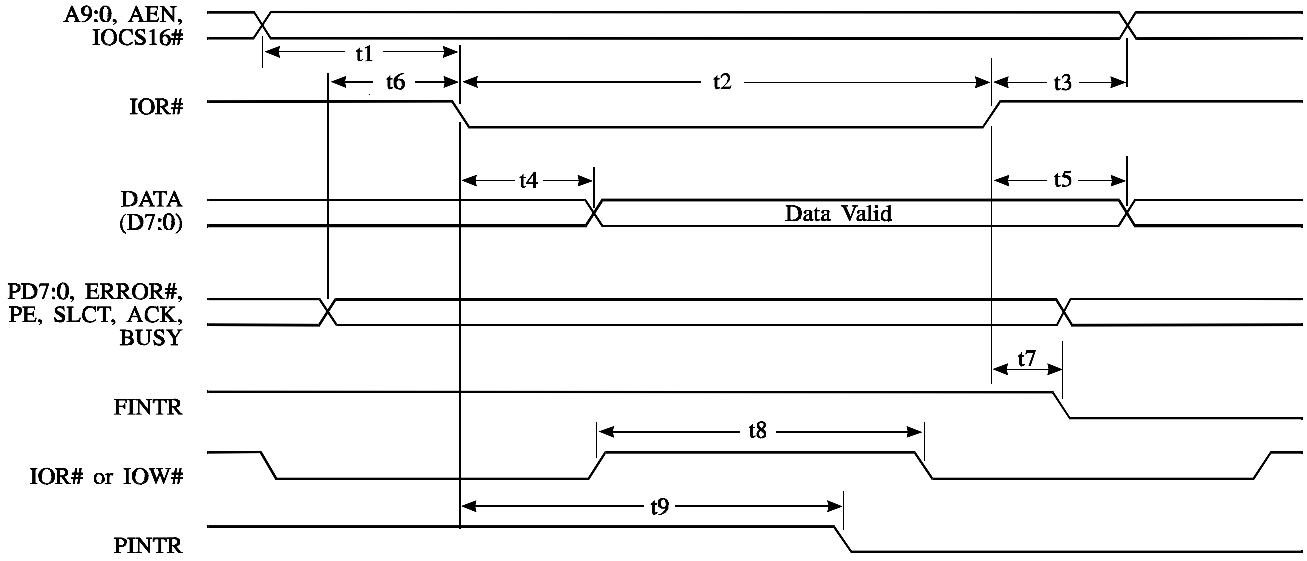
Time	Parameter	Minimum (ns)	Maximum (ns)	Typical (ns)
t1	Clock rise time (V_{IN} = 0.4 to 3.0)	—	5	—
t2	Clock fall time (V_{IN} = 3.0 to 0.4)	—	5	—
t3	Clock period	40	—	41.67
t4	Clock active (high or low)	14	—	—



Clock Timing

MICROPROCESSOR READ TIMING

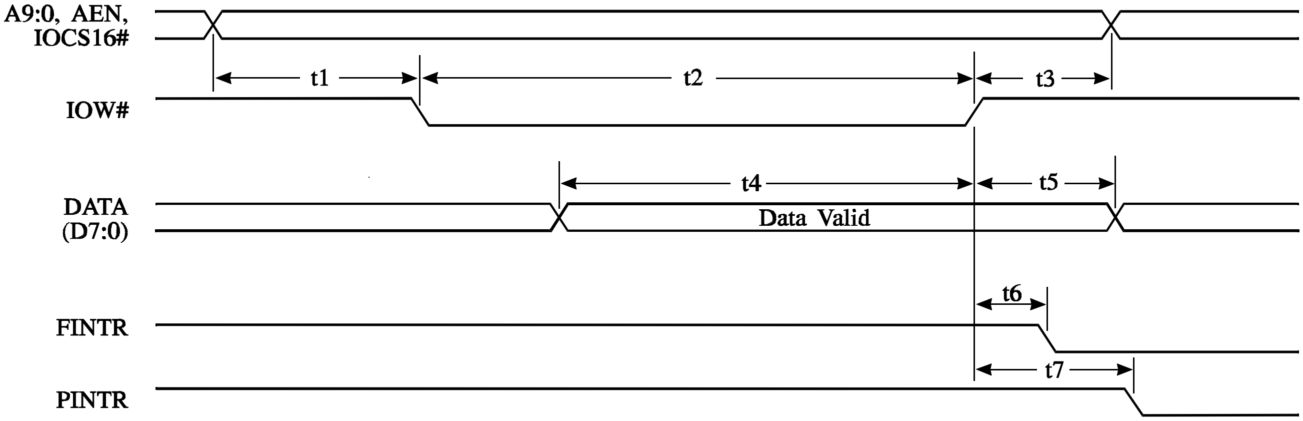
Time	Parameter	Minimum (ns)	Maximum (ns)	Typical (ns)
t1	A9:0, AEN, IOCS16# setup to IOR# low	40	—	—
t2	IOR# width	150	—	—
t3	A9:0, AEN, IOCS16# hold from IOR# high	10	—	—
t4	Data access time from IOR# low	—	100	—
t5	Data to float delay from IOR# high	10	60	—
t6	Port setup	—	—	20
t7	Read strobe to clear FINTR	—	55	40
t8	IOR# or IOW# inactive for transfers to and from ECP FIFO	150	—	—
t9	IOR# active to PINTR inactive	—	260	—



Microprocessor Read Timing

MICROPROCESSOR WRITE TIMING

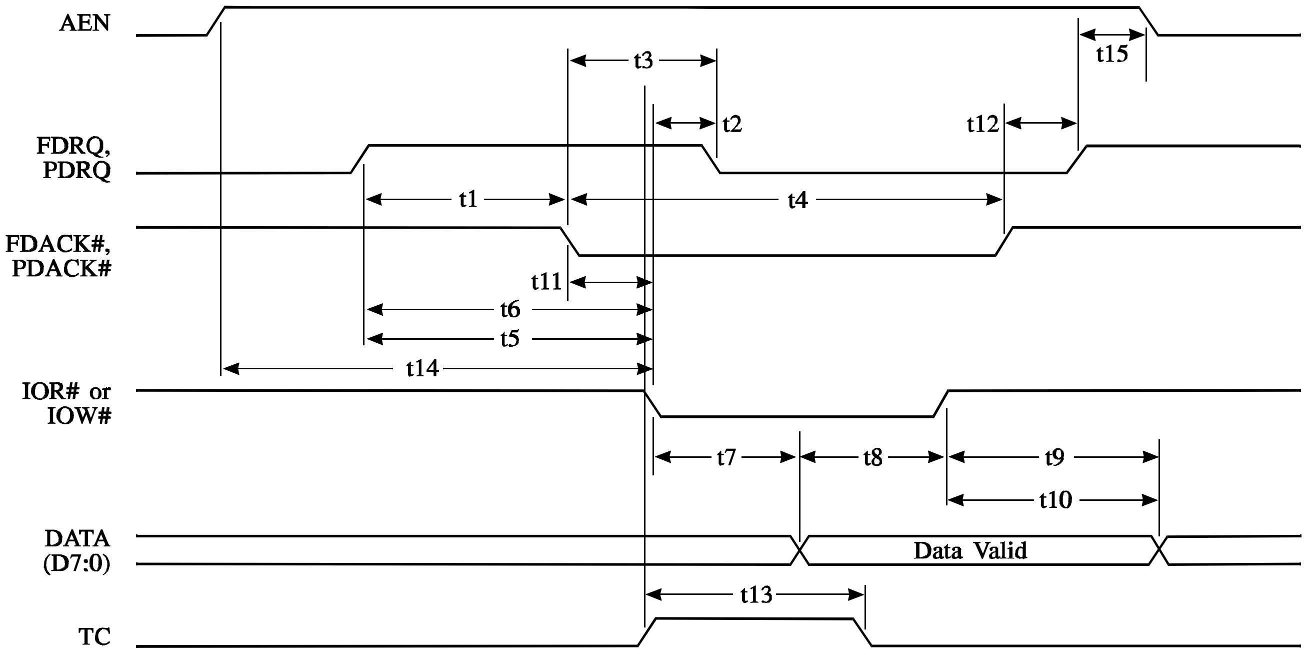
Time	Parameter	Minimum (ns)	Maximum (ns)	Typical (ns)
t1	A9:0, AEN, IOCS16# setup to IOW# low	40	—	—
t2	IOW# width	150	—	—
t3	A9:0, AEN, IOCS16# hold from IOW# high	10	—	—
t4	Data setup time to IOW# high	40	—	—
t5	Data hold time from IOW# high	10	—	—
t6	Write strobe to clear FINTR	—	55	40
t7	IOW# inactive to PINTR inactive	—	260	—



Microprocessor Write Timing

DMA TIMING

Time	Parameter	Minimum (ns)	Maximum (ns)	Typical (ns)
t1	DACK# delay time from DRQ high	0	—	—
t2	DRQ reset delay from IOR# or IOW#	—	118	—
t3	DRQ reset delay from DACK# low	—	118	—
t4	DACK# width	150	—	—
t5	IOR# delay from DRQ high	0	—	—
t6	IOW# delay from DRQ high	0	—	—
t7	Data access time from IOR# low	—	100	—
t8	Data setup time to IOW# high	40	—	—
t9	Data to hold time from IOR# high	10	60	—
t10	Data hold time from IOW# high	10	—	—
t11	DACK# setup to IOW#/IOR# low	5	—	—
t12	DACK# hold after IOW#/IOR# high	10	—	—
t13	TC pulse width	60	—	—
t14	AEN setup to IOR#/IOW#	40	—	—
t15	AEN hold from DACK#	10	—	—



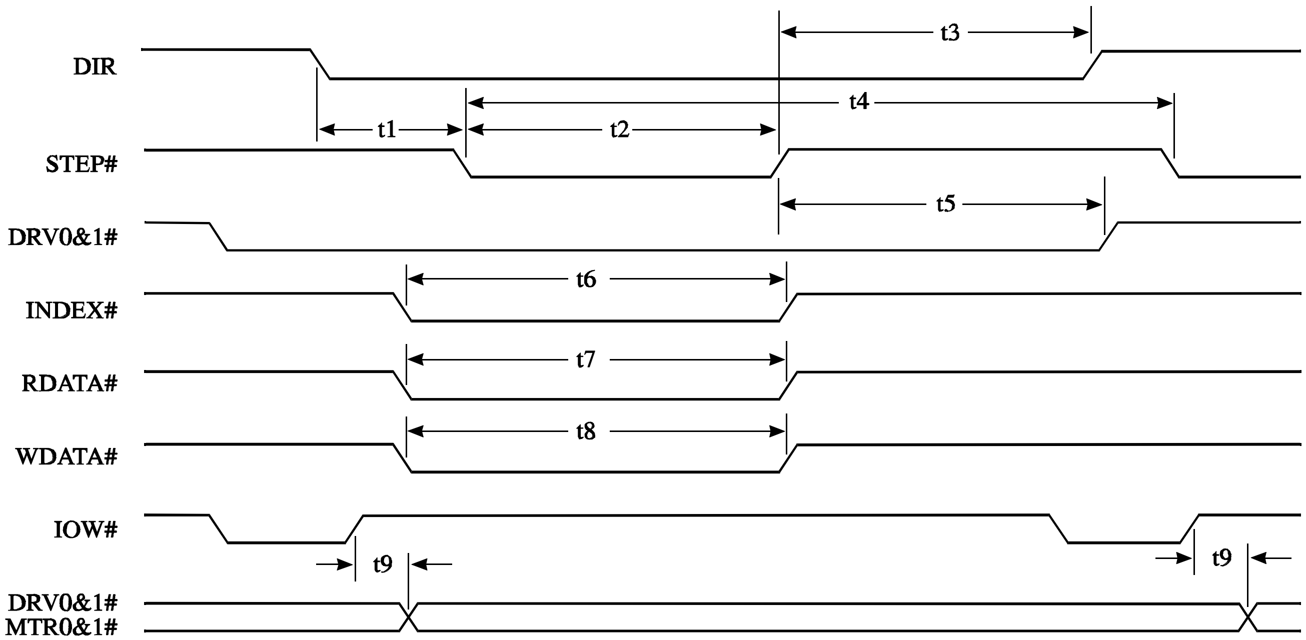
DMA Timing

FLOPPY DISK DRIVE TIMING

Time	Parameter	Minimum	Maximum	Typical	Units
t1	DIR setup to STEP# low	—	—	4	A (see Note 1)
t2	STEP# active time low	—	—	24	A
t3	DIR hold time after STEP#	—	—	96	A
t4	STEP# cycle time	—	—	132	A
t5	DRV0&1# hold time from STEP# low	—	—	20	A
t6	INDEX pulse width	—	—	2	A
t7	RDATA# active time low	—	—	40	ns
t8	WDATA# write data width low	—	—	0.5	B (see Note 2)
t9	DRV0&1# and MTR0&1# from end of IOW# (see Note 3)	—	—	25	ns

Notes:

1. A specifies one FCLK (FDC clock) period: 4MHz at 250kb/s; 4.8MHz at 300kb/s, 8MHz at 500kb/s; 16MHz at 1Mb/s.
2. B specifies one WCLK period, where WCLK is 2 x data rate.
3. DRV0&1# = Drive Select 0 and 1 active low signals; MTR0&1# = Motor Select 0 and 1 active low signals.

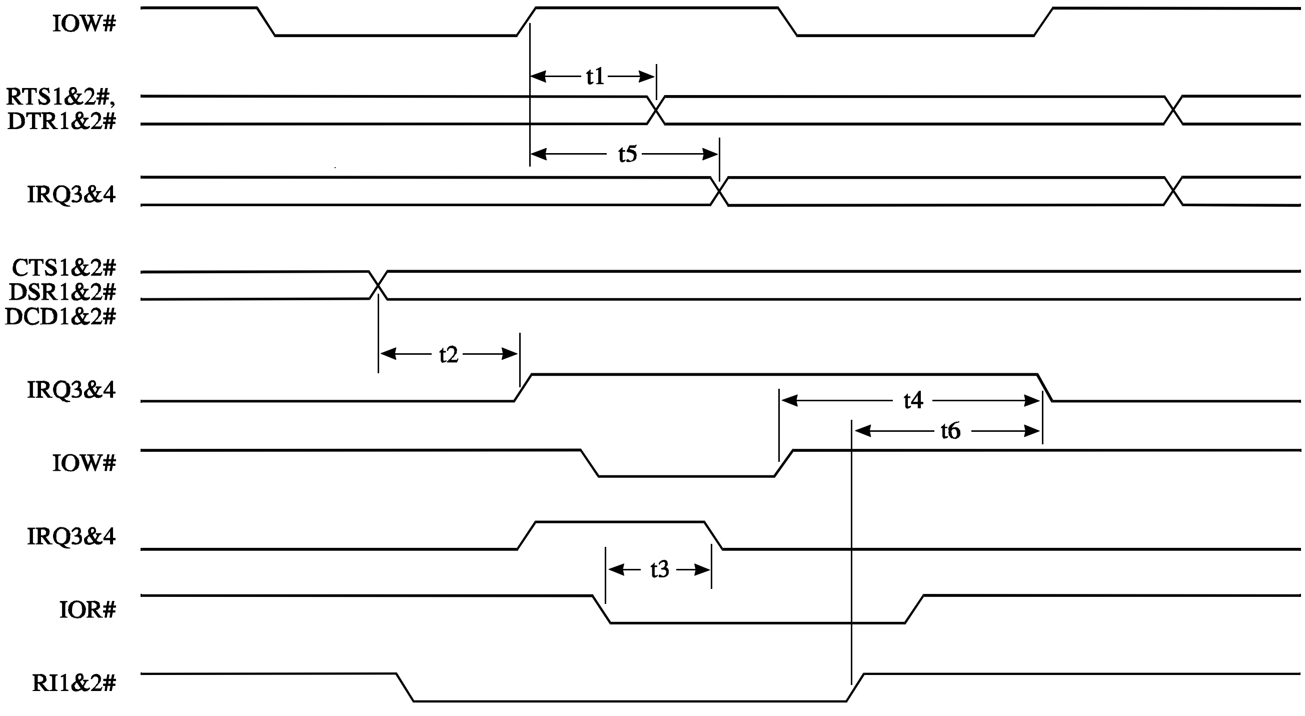


Floppy Disk Drive Timing

SERIAL PORT TIMING

Time	Parameter	Min. (ns)	Max. (ns)	Comments
t1	RTS1#/RTS2# and DTR1#/DTR2# delay from IOW#	—	200	See Note
t2	IRQ3/IRQ4 active delay from CTS1#/CTS2# , DSR1#/DSR2#, and DCD1#/DCD2#	—	100	See Note
t3	IRQ3/IRQ4 inactive delay from IOR# (leading edge)	—	120	
t4	IRQ3/IRQ4 inactive delay from IOW# (trailing edge)	—	125	
t5	IRQ3/IRQ4 inactive delay from IOW#	10	100	
t6	IRQ3/IRQ4 active delay from RI1#/RI2#	—	100	See Note

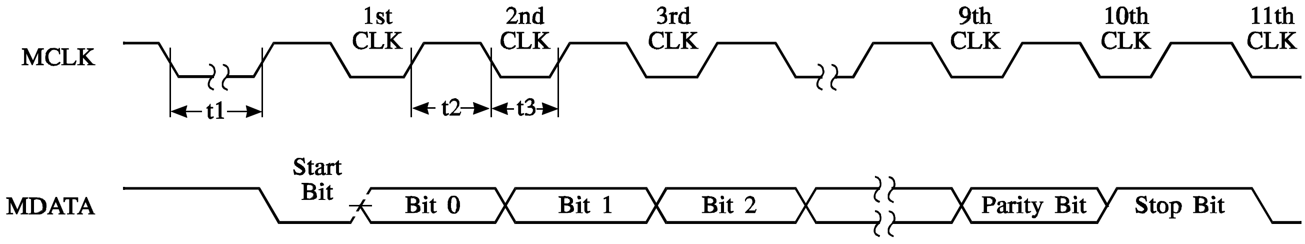
Note: 1 and 2 designate the primary and secondary serial ports, respectively.



Serial Port Timing

MOUSE TRANSMIT TIMING

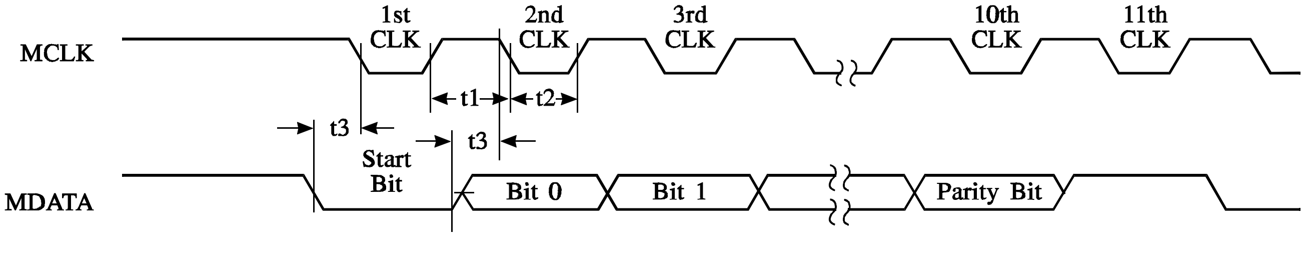
Time	Parameter	Minimum (ns)	Maximum (ns)
t1	MCLK line inactive while CPU prepares to send data	110	115
t2	Duration of MCLK active	30	50



Mouse Transmit Timing

MOUSE RECEIVE TIMING

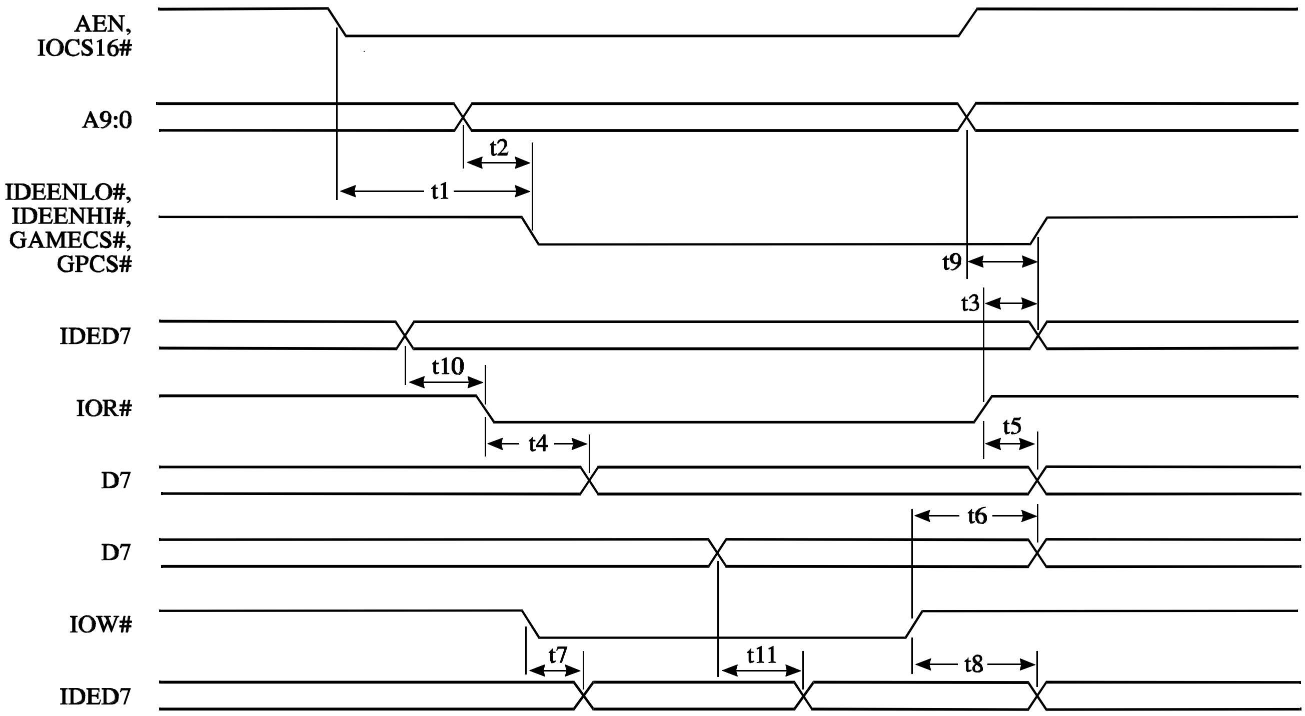
Time	Parameter	Minimum (ns)	Maximum (ns)
t1	Duration of MCLK inactive	30	50
t2	Duration of MCLK active	30	50
t3	Time from MDATA transition to falling edge of MCLK	5	25



Mouse Receive Timing

IDE INTERFACE TIMING

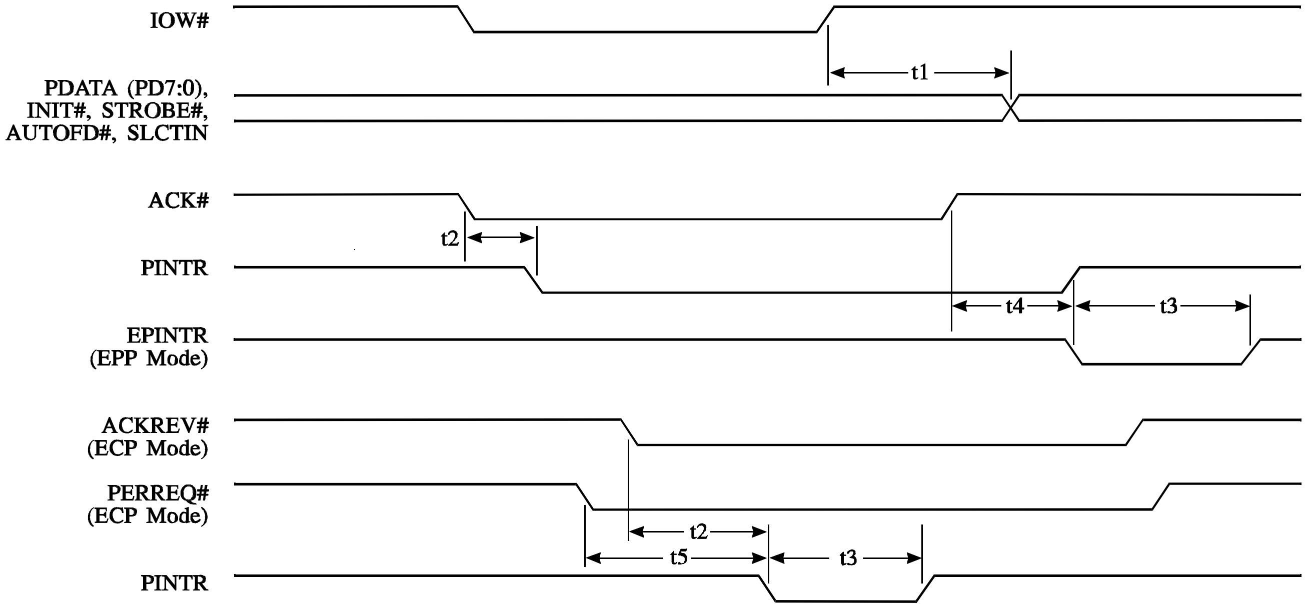
Time	Parameter	Minimum (ns)	Maximum (ns)
t1	IDEENLO#, IDEENHI#, GAMECS#, and GPCS# delay from AEN and IOCS16#	—	40
t2	IDEENLO#, IDEENHI#, GAMECS#, and GPCS# delay from A9:0	—	40
t3	IDED7 hold time after IOR#	10	—
t4	D7 delay time from IOR#	—	100
t5	D7 hold time from IOR#	10	60
t6	D7 hold time from IOW#	10	—
t7	IDED7 delay from data bus IOW# active	—	50
t8	IDED7 inactive delay from IOW#	10	50
t9	IDEENLO# and IDEENHI# delay from IOCS16# and AEN	—	40
t10	IDED7 setup time before IOR#	40	—
t11	IDED7 delay from D7	—	25



IDE Interface Timing

PARALLEL PORT TIMING

Time	Parameter	Minimum (ns)	Maximum (ns)
t1	PDATA (PD7:0), INIT#, STROBE#, AUTOFD# delay from IOW#	—	100
t2	PINTR delay from ACK#, ACKREV# (ECP mode)	—	60
t3	EPINTR active low in EPP mode	200	300
t4	PINTR delay from ACK#	—	105
t5	PERREQ# active to PINTR active	—	105



Parallel Port Timing

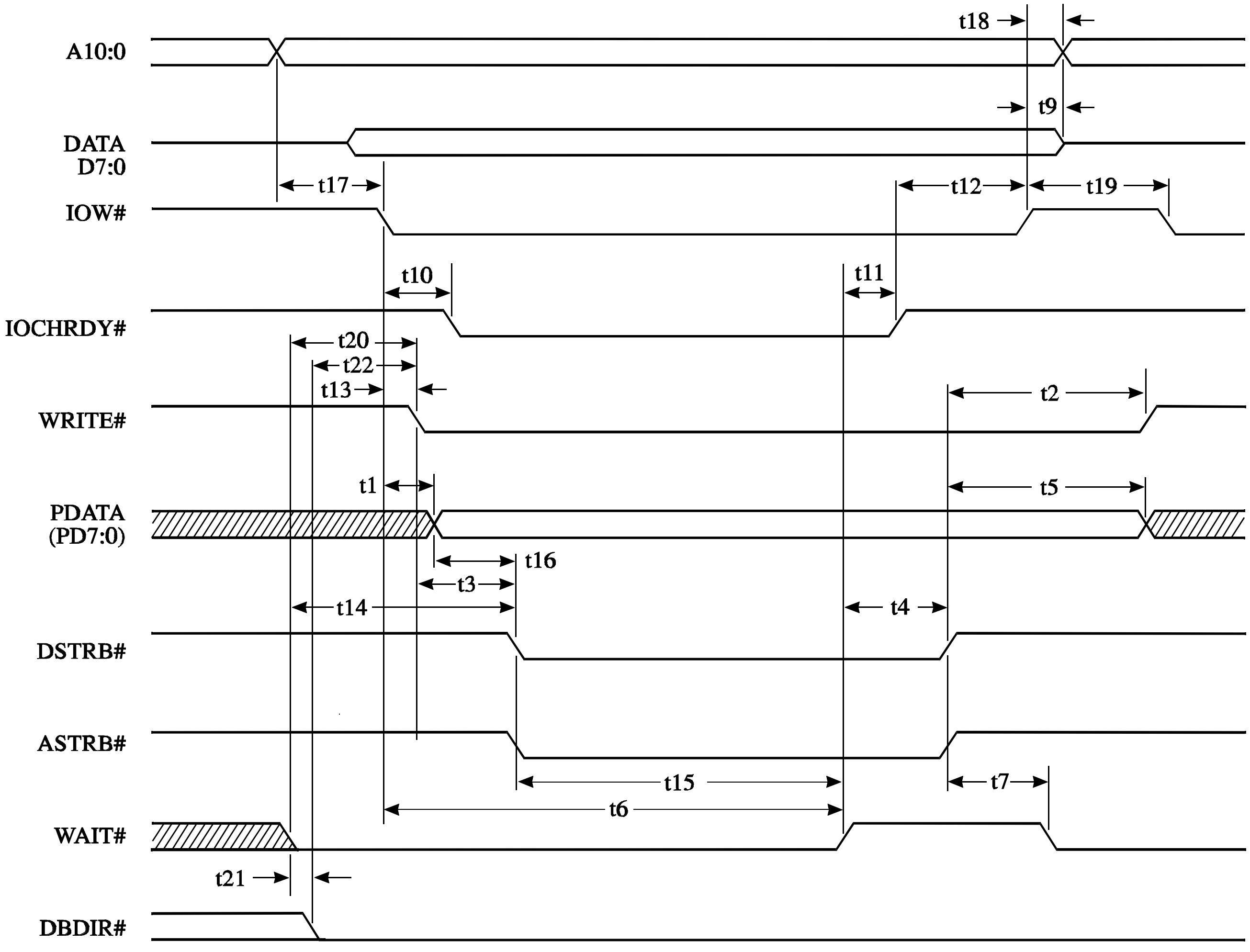
EPP DATA OR ADDRESS WRITE CYCLE

Time	Parameter	Minimum (ns)	Maximum (ns or as specified)	Comments
t1	IOW# asserted to PDATA valid	0	100	
t2	Command deasserted to WRITE# change	40	160	See Note 1
t3	WRITE# to command asserted	20	—	
t4	WAIT# deasserted to command deasserted	80	200	See Note 1
t5	Command deasserted to PDATA invalid	60	140	See Notes 1, 2
t6	Timeout	—	2.7µs	
t7	Command deasserted to WAIT# asserted	0	—	
t9	IOW# deasserted to D7:0 invalid	0	—	
t10	IOW# asserted to IOCHRDY# asserted	0	100	WAIT low
t11	WAIT# deasserted to IOCHRDY# deasserted	0	60	
t13	IOW# asserted to WRITE# asserted	0	50	
t15	Command asserted to WAIT# deasserted	—	2.6µs	
t16	PDATA valid to command asserted	40	—	

Notes:

1. WAIT# must be filtered to compensate for ringing on the parallel bus cable. WAIT# is considered to have settled after it does not transition for a minimum of 50nsec.

2. The maximum time only applies if another cycle is pending. If no other cycle is pending, the da ta is held indefinitely.



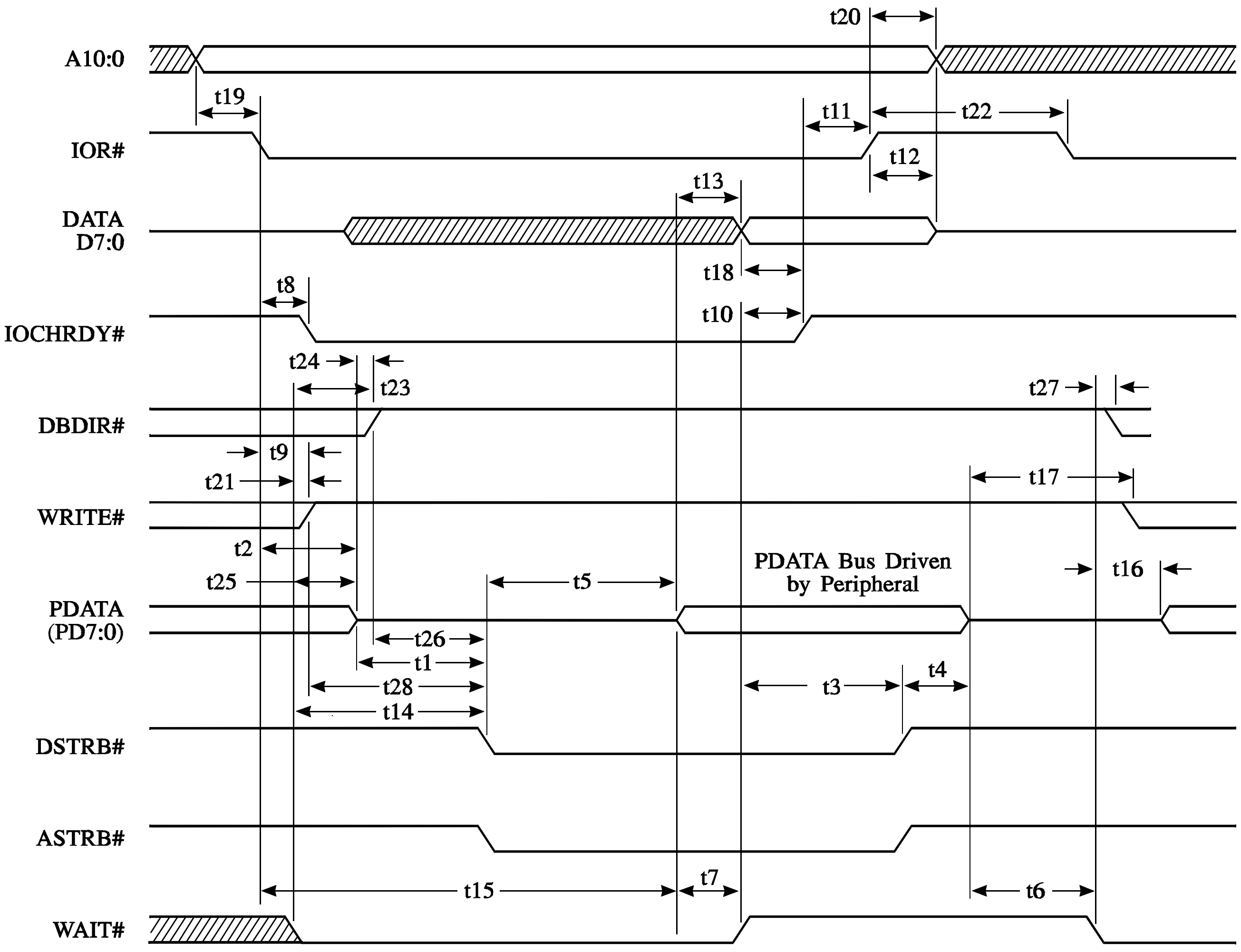
EPP Data or Address Write Cycle

EPP DATA OR ADDRESS READ CYCLE

Time	Parameter	Minimum (ns)	Maximum (ns)	Comments
t1	PDATA hi-Z to command asserted	0	—	
t2	IOR# asserted to PDATA hi-Z	0	60	
t3	WAIT# deasserted to command deasserted	80	200	See note 1
t4	Command deasserted to PDATA hi-Z	0	—	
t5	Command asserted to PDATA valid	—	250	No WAIT
t7	PDATA valid to WAIT# deasserted	0	—	
t8	IOR# asserted to IOCHRDY# asserted	0	100	WAIT low
t9	WRITE# deasserted to IOR# asserted	0	—	See note 2
t10	WAIT# deasserted to IOCHRDY# deasserted	0	60	
t13	PDATA valid to D7:0 valid	0	75	
t17	Command deasserted to WRITE# change	40	160	
t28	WRITE# deasserted to command	40	—	

Notes:

1. WAIT# is considered to have settled when it does not transition for a minimum of 50ns.
2. When not executing a write cycle, WRITE# is inactive high.



EPP Data or Address Read Cycle

ECP PARALLEL PORT FIFO OPERATION

In ECP FIFO operation, the standard parallel port is run at or near the peak 500kb/sec allowed for operation in the forward direction using DMA. The state machine does not examine PERCLK (Peripheral Clock) and begins the next data transfer based on PERACK (Peripheral Acknowledge). See the ECP Parallel Port FIFO Timing diagram on the following page.

ECP parallel port FIFO timing is designed to allow operation at approximately 2MB/sec over a 15-foot cable. If a shorter cable is used, the bandwidth increases.

Forward Operation

In the Forward Idle phase of ECP operation, when there is no data to send, the host keeps HOSTCLK high and the peripheral device leaves PERCLK low. The data transfer phase can be entered from this state.

In the Forward Data Transfer phase, the interface transfers data and commands from the host to the peripheral device using interlocked PERACK and HOSTCLK signals. If the peripheral device wants to reverse the procedure and send data to the host, it can asynchronously assert PERREQ# to request that the channel be reversed.

When it is ready to send data, the host sets HOSTCLK high. The data must be stable for the specified setup time prior to the falling edge of HOSTCLK. The peripheral device sets PERACK high to acknowledge the handshake. The host then sets HOSTCLK high and transfers the data. After accepting the data, the peripheral device sets PERACK low to complete the transfer. This sequence is shown in the ECP Parallel Port Forward Timing diagram.

The timing is designed to provide three cable roundtrip times for data setup if PDATA (PD7:0) is driven simultaneously with HOSTCLK.

Reverse Operation

In the Reverse Idle phase, when the peripheral device has no data to send, the peripheral keeps PERCLK high. The idle host keeps HOSTACK low. The data transfer phase can be entered from the idle state.

In the Reverse Data Transfer phase, the peripheral device sets PERCLK low to signal that it has data to send. The data must be stable for the specified setup time prior to the falling edge of PERCLK. When the host is ready to accept a byte, it sets HOSTACK high to acknowledge the handshake. The peripheral device then sets PERCLK high and transfers the data. After accepting the data, the host sets HOSTACK low, completing the transfer. This sequence is shown in the ECP Parallel Port Reverse Timing diagram.

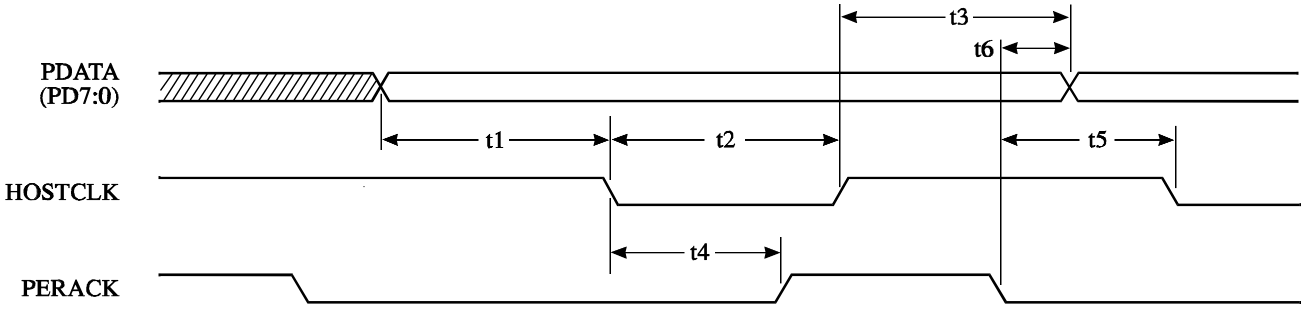
Output Drivers

Higher performance data transfers are achieved by using balanced CMOS active drivers for the critical ECP signals: PDATA, HOSTACK, HOSTCLK, PERACK, and PERCLK. The drivers are dynamically changed from open-collector (the traditional control-signal specification) to totem-pole to avoid the compatibility problems that active drivers can present. The timing for the dynamic driver change is specified in the Microsoft *Extended Capabilities Port Protocol and ISA Interface Standard*, Rev. 1.11, February 10, 1993. This standard is available from Microsoft Corporation. The dynamic driver change must be implemented properly to prevent glitching of the outputs.

ECP PARALLEL PORT FIFO TIMING

Time	Parameter	Minimum (ns)	Maximum (ns)	Comments
t1	PDATA valid to HOSTCLK active	500	—	
t2	HOSTCLK active pulse width	500	—	
t3	PDATA hold from HOSTCLK inactive	500	—	See Note
t4	HOSTCLK active to PERACK active	—	900	
t5	PERACK inactive to HOSTCLK active	500	—	
t6	PERACK inactive to PDATA invalid	80	—	See Note

Note: If no other data transfer is pending, the data is held indefinitely. If another data transfer is pending, the data is held until PERAK goes inactive or for time t3, whichever is longer.



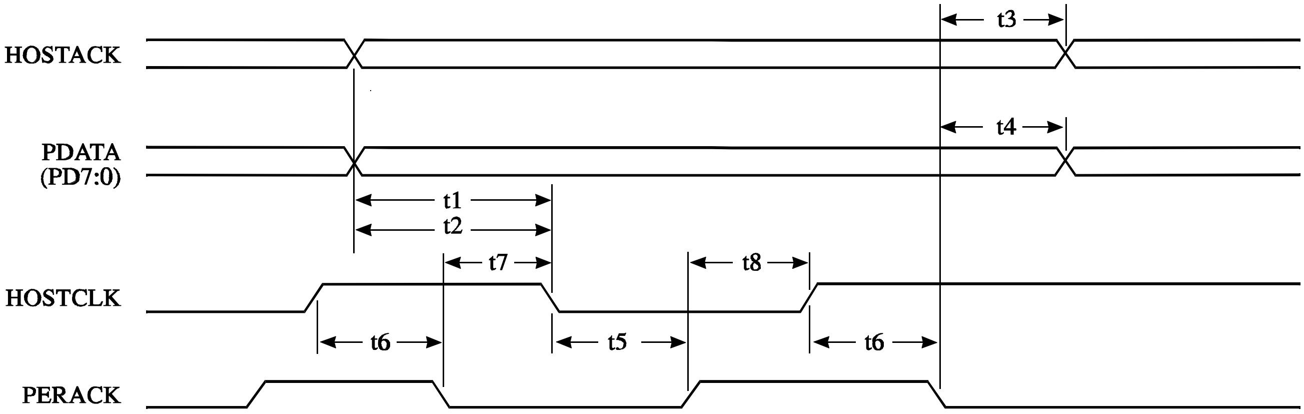
ECP Parallel Port FIFO Timing

ECP PARALLEL PORT FORWARD TIMING

Time	Parameter	Minimum (ns)	Maximum (ns)	Comments
t1	HOSTACK valid to HOSTCLK asserted	0	60	
t2	PDATA valid to HOSTCLK asserted	0	60	
t3	PERACK deasserted to HOSTACK changed	80	180	See Notes 1 and 2
t4	PERACK deasserted to PDATA changed	80	180	See Notes 1 and 2
t5	HOSTCLK asserted to PERACK asserted	0	—	
t6	HOSTCLK deasserted to PERACK deasserted	0	—	
t7	PERACK deasserted to HOSTCLK asserted	80	200	See Notes 1 and 2
t8	PERACK asserted to HOSTCLK deasserted	80	180	See Note 2

Notes:

1. Maximum value only applies if the FIFO is holding data to be written out.
2. PERACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130ns.



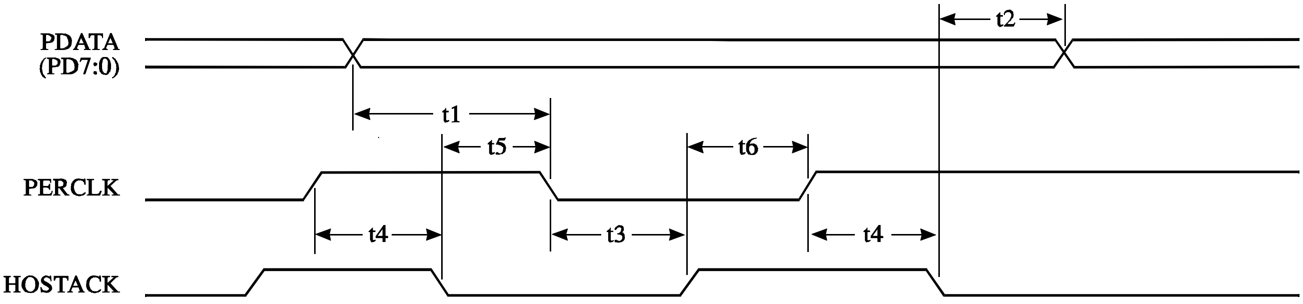
ECP Parall Port Forward Timing

ECP PARALLEL PORT REVERSE TIMING

Time	Parameter	Minimum (ns)	Maximum (ns)	Comments
t1	PDATA valid to PERCLK asserted	0	—	
t2	HOSTACK deasserted to PDATA changed	0	—	
t3	PERCLK asserted to HOSTACK deasserted	80	200	See Notes 1 and 2
t4	PERCLK deasserted to HOSTACK asserted	80	200	See Note 2
t5	HOSTACK asserted to PERCLK asserted	0	—	
t6	HOSTACK deasserted to PERCLK deasserted	0	—	

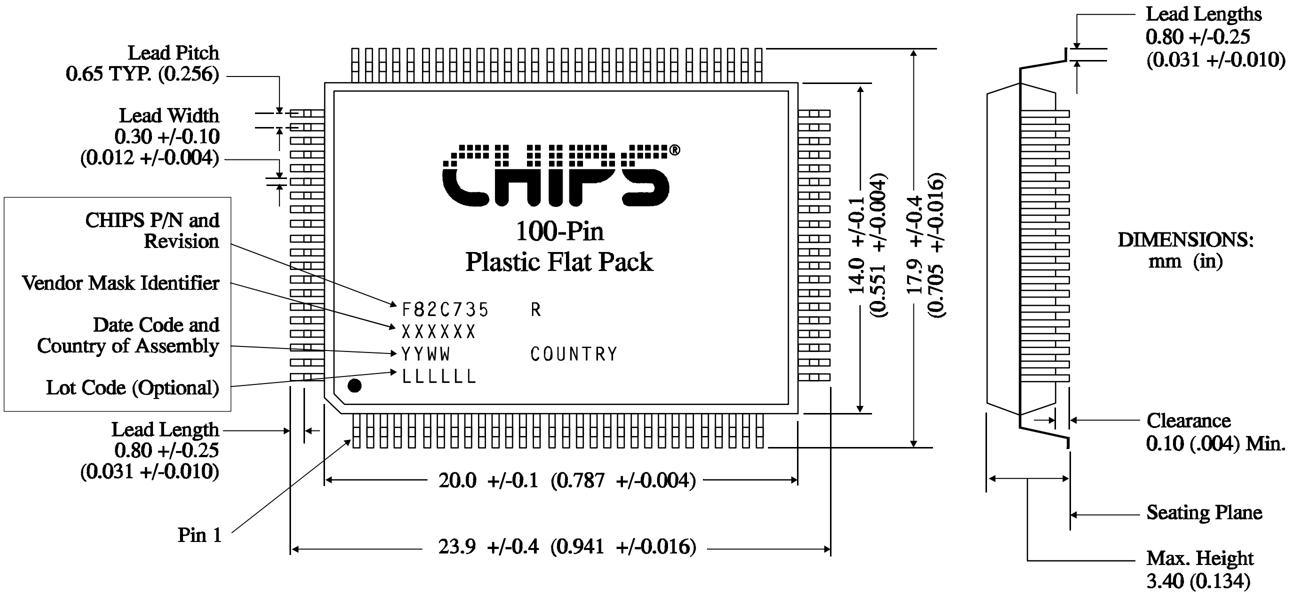
Notes:

1. Maximum value only applies if there is room in the FIFO. Host can stall by keeping HOSTACK low.
2. PERCLK is not considered asserted or deasserted until it is stable for a minimum of 50ns.



ECP Parallel Port Reverse Timing

Mechanical Specifications



CHIPS®

Chips and Technologies, Inc.
3050 Zanker Road
San Jose, California 95134
Phone: 408-434-0600
Telex: 272929 CHIPS UR
FAX: 408-434-6452

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