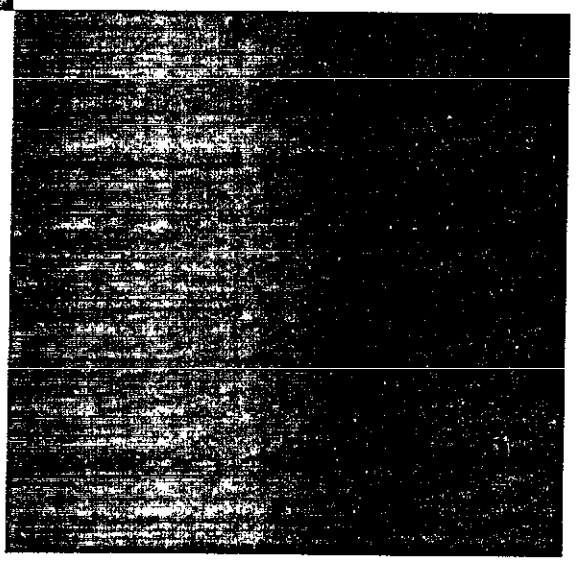
82C710

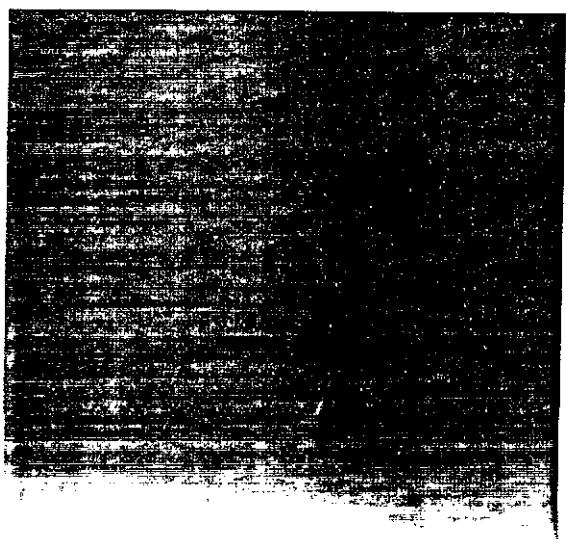


Universal Peripheral Controller

Data Sheet

August 1990

P R E L I M I N A R Y



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82C710
UNIVERSAL PERIPHERAL CONTROLLER

- Low Power CMOS, 100 pin PQFP Package
- On Chip Power Management Features, Controllable Through Hardware and/or Software
- 100% IBM PC-XT/AT Compatibility.
- 24 mA AT/XT Bus Interface Buffers
- Schmitt Trigger Input on Reset Pin
- 1 x 16450 Compatible UART
- 1 IBM PC-XT/AT Compatible Enhanced (Bi-Directional) Parallel Port
- 24 mA Parallel Port Output Drivers
- PS/2 Style Mouse Port Logic with BIOS & Driver Support
- IDE Interface (For Embedded AT & XT Hard Drives)
- General Purpose Chip Select
- Real Time Clock Chip Select
- Fully μPD72065B and IBM-BIOS Compatible Floppy Controller
  - —Licensed NEC design
  - —48 mA floppy drive interface buffers
  - —Data rate and drive control registers
  - —Two pin programmable precompensation modes
  - —Supports two floppy drives directly and up to four drives with an external decoder
  - —DMA enable logic
- On-chip Precision Analog Data Separator
  - —±380 ns at 500K bps
  - —±740 ns at 250K bps
  - —Automatically selects one of three filters
  - —Supports 250 Kb/s, 300 Kb/s, 500 Kb/s & 1 Mb/s data rates
  - —Programmable recompensation modes
- Single 24 MHz Crystal/Oscillator for UART and Floppy Disk Controller

The 82C710 Universal Peripheral Controller (UPC) is a single chip controller offering the complete I/P solution for the PC-XT & PC-AT environments. The chip is an LSI implementation of the most commonly used peripheral devices found in an IBM PC, XT or AT. It features 24 mA drivers for the output buffers, including the host data bus and parallel port data bus. It incorporates one 16450 compatible UART, one enhanced parallel port (with bi-directional capability), an IDE compatible hard disk interface, a μPD72065B compatible floppy disk controller, PS/2 type mouse logic, and various chip selects. Decoding logic and support for main, auxiliary and standby power supplies and software configurable base addresses for these devices, operational modes and interrupts are also included. Power management aspects of the 82C710 includes modular power down for each port, and software oscillator disable. The hardware power management is done through the PWRGD pin. When the chip is powered down (i.e. when PWRGD is inactive) the current drawn is less than 250 microAmps, all the inputs are disabled, and all outputs are tri-stated. The contents of all the registers are preserved, as long as power supply to the 82C710 is maintained.

The host interface is PC compatible, (i.e. D0-D7, A0-A9, $\overline{IOR}$, $\overline{IOW}$, AEN, MINTR, FINTR, PINTR, SINTR, and RESET), and can be connected directly to the bus. The data buffers (D0-D7, PD0-PD7, IDED7) are capable of sinking 24 mA @ 0.5V, the parallel port control signals are open collector with internal pull up, and are capable of sinking 24 mA @ 0.5V.

The UART implements a fully functional serial link. Programmable character length, parity generation and detection, stop-bit generation

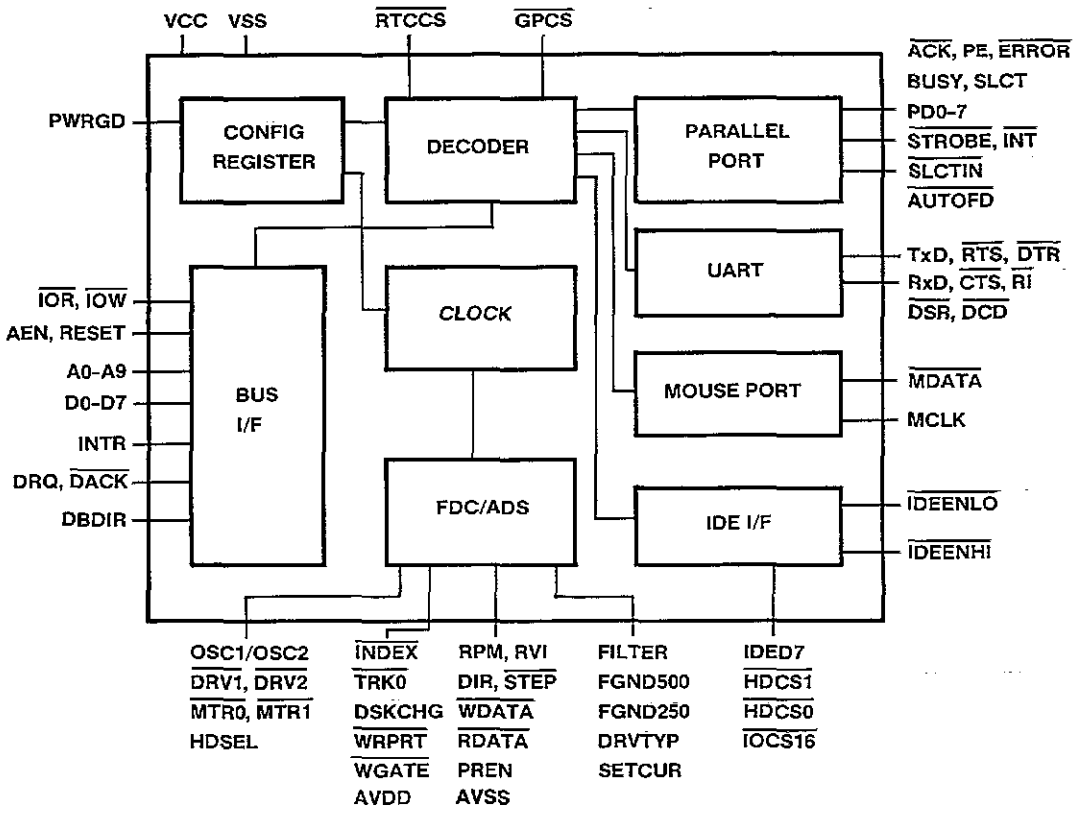


Figure 1. 82C710 Block Diagram

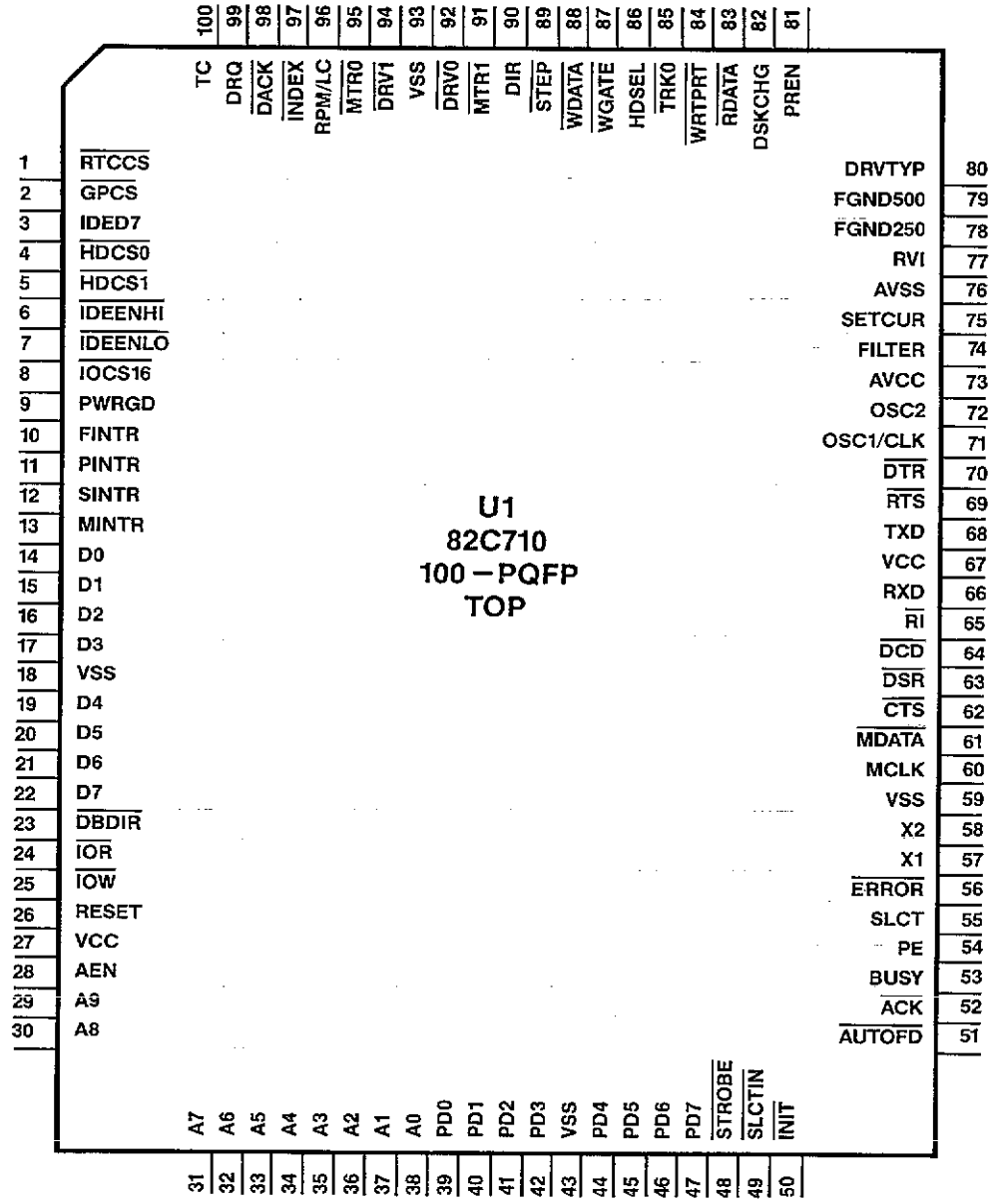
and baud rate generation are provided. Double buffering is used so that precise synchronization is unnecessary. Status information is accessible to the CPU by reading internal registers. MODEM control lines are provided, as are internal diagnostic functionality and interrupt prioritization.Support for an auxiliary power system (such as that derived from a telephone line or RS232 link) permits a UPC in a battery-powered device to consume no battery power until an incoming character is detected.

The parallel port can be configured for output only (printer application) or input and output (scanner application). The necessary control signals are provided for use as a Centronics-compatible (output only) parallel port. For scanner applications, a Centronics-like interface is used. Such an interface is utilized by the RICOH IS30 scanner.

The configuration RAM and circuitry support programmable base addresses for all registers internal to the UPC. This permits creation of a menu-driven program for system configuration. Selection of sources for interrupts, enabling and configuring of on-chip subsystems (UARTs, parallel port, etc.) and control of the configuration process itself are also handled with this RAM and its associated circuitry.

The remainder of this data sheet will consider each of the aforesaid subsystems individually. Sections containing more general design data for the chip as a whole are at the end along with electrical and physical characteristics.

Figure 1 depicts the subsystems present in the 82C710.


U1
82C710
100 – PQFP
TOP
1 RTCCS
2 GPCS
3 IDED7
4 HDCS0
5 HDCS1
6 IDEENHI
7 IDEENLO
8 IOCS16
9 PWRGD
10 FINTR
11 PINTR
12 SINTR
13 MINTR
14 D0
15 D1
16 D2
17 D3
18 VSS
19 D4
20 D5
21 D6
22 D7
23 DBDIR
24 IOR
25 IOW
26 RESET
27 VCC
28 AEN
29 A9
30 A8
31 A7
32 A6
33 A5
34 A4
35 A3
36 A2
37 A1
38 A0
39 PD0
40 PD1
41 PD2
42 PD3
43 VSS
44 PD4
45 PD5
46 PD6
47 PD7
48 STROBE
49 SLCTIN
50 INIT
51 AUTOFD
52 ACK
53 BUSY
54 PE
55 SLCT
56 ERROR
57 X1
58 X2
59 VSS
60 MCLK
61 MDATA
62 CTS
63 DSR
64 DCD
65 RI
66 RXD
67 VCC
68 TXD
69 RTS
70 DTR
71 OSC1/CLK
72 OSC2
73 AVCC
74 FILTER
75 SETCUR
76 AVSS
77 RVI
78 FGND250
79 FGND500
80 DRVTYP
81 PREN
82 DSKCHG
83 RDATA
84 WRTPRT
85 TRK0
86 HDSEL
87 WGATE
88 WDATA
89 STEP
90 DIR
91 MTR1
92 DRV0
93 VSS
94 DRV1
95 MTR0
96 RPM/LC
97 INDEX
98 DACK
99 DRQ
100 TC

1.0 82C710 Pin Description

1.1 Host Interface (30 pins)

Pin No.	Symbol	Buffer Type	Description
13	MINTR	T	Mouse port Interrupt Request (programmable polarity), 24 mA driver. The interrupt is enabled/disabled via bit 4 of the Mouse control port.
10	FINTR	T	Floppy controller Interrupt Request (programmable polarity), 24 mA driver. This interrupt is enabled/disabled via bit 3 of the Drive Control Register. The active output is used to get the attention of the CPU. The required action depends on the current function of the controller.
12	SINTR	T	Serial port Interrupt Request (programmable polarity), 24 mA driver. The appropriate interrupt is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset.
11	PINTR	T	Parallel port Interrupt Request (programmable polarity), 24 mA driver. The interrupt is enabled/disabled via bit 4 of the Parallel Control Register. If enabled, the interrupt is generated following the $\overline{ACK}$ signal input.
23	$\overline{DBDIR}$	O	Host Data Bus Buffer Direction. Active low signal indicates read cycle for 82C710 internal accesses: Parallel port, Serial port, FDC and Mouse port. Also goes low if IDE, Real Time Clock Chip Select ($\overline{RTCCS}$) and General Purpose Chip Select ($\overline{GPCS}$) are active and their buffer modes are enabled (through configuration register).
38..29	A0-A9	I	Host address bit 0-9. These address bits are latched internally at the beginning of $\overline{IOR}$ or $\overline{IOW}$.
28	AEN	I	Active high Address Enable indicates DMA activity. Normally, this signal is used with A0-A9, $\overline{IOW}$, $\overline{IOR}$ to decode I/O address ports.
24	$\overline{IOR}$	I	Active low I/O read from host.
25	$\overline{IOW}$	I	Active low I/O write from host.
26	RESET	IS	Active high Reset from host (Schmitt-trigger input). RESET has to be valid for a minimum of 500 nanosecond. This resets the serial port, parallel port, mouse and the FDC. The effect of hardware reset is shown in the functional description of each port. The configuration registers are not affected. They come up in the default condition only on power up.
14..17 19..22	D0-D7	I/0H	Host data bus, 24 mA driver. This bi-directional data bus is used to transfer information between the CPU and 82C710.
98	$\overline{DACK}$	I	Active low input to acknowledge the DMA request. This signal normally is used to enable DMA read or write.
99	DRQ	OH	Active high DMA request output signal to the host, 24 mA driver.
100	TC	I	Active high input signal indicates termination of DMA transfer, qualified by $\overline{DACK}$ before use on chip.

1.2 Parallel Port Controller (17 pins):

Pin No.	Symbol	Buffer Type	Description
39..42 44..47	PD0-PD7	I/OH	The bi-directional parallel data bus is used to transfer information between CPU and peripherals. These signals have high current drive and capable of sinking 24 mA @ 0.5V
48	$\overline{\text{STROBE}}$	OC	This active low output indicates to the peripheral that the data at the parallel port is valid. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
49	$\overline{\text{SLCTIN}}$	OC	This active low output selects the printer when it is low. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
50	$\overline{\text{INIT}}$	OC	This active low output initializes (reset) the printer when it is low. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
51	$\overline{\text{AUTOFD}}$	OC	When this output is low the printer automatically adds one line feed after printing. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
52	$\overline{\text{ACK}}$	I	Active low Acknowledge input. Low indicates that data has been received and the printer is ready to accept more data.
53	BUSY	I	Active high Busy input. The high input signal indicates the printer can not accept additional data.
54	PE	I	Active high Paper End input. The high input signal indicates the printer is out of paper.
55	SLCT	I	Active high device Select input. The input is set high by the printer when it is selected.
56	$\overline{\text{ERROR}}$	I	Active low Error input. This input is set low by the printer when it detects the error.

1.3 Serial Port Interface (10 Pins):

62	$\overline{\text{CTS}}$	I	Active low Clear to Send input. Handshake signal which notifies the UART that the MODEM is ready to receive data. The CPU can monitor the status of $\overline{\text{CTS}}$ signal by reading bit 4 of Modem Status Register (MSR). A $\overline{\text{CTS}}$ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{CTS}}$ changes state. The $\overline{\text{CTS}}$ signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of $\overline{\text{CTS}}$.
63	$\overline{\text{DSR}}$	I	Active low Data Set Ready input. Handshake signal which notifies the UART that the MODEM is ready to establish the communication link. The CPU can monitor the status of $\overline{\text{DSR}}$ signal by reading bit 5 of Modem Status Register. A $\overline{\text{DSR}}$ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DSR}}$ changes state. Note: Bit 5 of MSR is the complement of $\overline{\text{DSR}}$

1.3 Serial Port Interface (10 pins) (Continued)

Pin No.	Symbol	Buffer Type	Description
64	$\overline{DCD}$	I	Active low Data Carrier Detect input. Handshake signal which notifies the UART that carrier signal is detected by the MODEM. The CPU can monitor the status of $\overline{DCD}$ signal by reading bit 7 of Modem Status Register (MSR). A $\overline{DCD}$ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{DCD}$ changes state. Note: Bit 7 of MSR is the complement of $\overline{DCD}$.
65	$\overline{RI}$	I	Active low Ring Indicator input. Handshake signal which notifies the UART that the telephone ring signal is detected by the MODEM. The CPU can monitor the status of $\overline{RI}$ signal by reading bit 6 of Modem Status Register (MSR). A $\overline{RI}$ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{RI}$ changes state. Note: Bit 6 of MSR is the complement of $\overline{RI}$.
66	RXD	I	Active high receive serial data input from communication link.
69	$\overline{RTS}$	O	Active low Request To Send output. Handshake output signal notifies MODEM that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{RTS}$ signal to inactive mode (high). Forced inactive during loop mode operation.
70	$\overline{DTR}$	O	Active low Data Terminal ready output. Handshake output signal notifies MODEM that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the $\overline{DTR}$ signal to inactive mode (high). Forced inactive during loop mode operation.
68	TXD	O	Active high transmit serial data output to the communication link.
57, 58	NC	—	No Connect

1.4 IDE Interface and Chip Selects (9 Pins):

Pin No.	Symbol	Buffer Type	Description
9	PWRGD	I	Active high Power Good indication. The 82C710 is fully functional when PWRGD is active; when PWRGD is inactive and Vcc is still valid, the 82C710 is isolated from the rest of the circuit. All accesses are ignored, all inputs are disabled, and all outputs are tri-stated. However, contents of all registers are preserved, and the current drain drops to Istby.
8	$\overline{\text{IOCS16}}$	O	Active low 16 bit I/O indication, AT hard disk mode. The hard disk interface generates $\overline{\text{IOCS16}}$ to inform the host and the 82C710 that 16 bit I/O transfers are about to begin. $\overline{\text{IOCS16}}$ is active only when transferring data words in AT mode. Low = 16 bit, high = 8 bit (AT mode).
	($\overline{\text{HDACK}}$)	I	Active Low HDC DMA Acknowledge, XT hard disk mode.
3	IDED7	I/OH	IDE Data Bit 7, AT hard disk mode. IDED7 transfers data at I/O addresses 1F0H-1F7H (R/W), 3F6H (R/W), 3F7(W). IDED7 should be connected to the IDE data bit 7. Normally, the 82C710 functions as a buffer, transferring data bit 7 between the IDE device and the host. During read of I/O address 3F7H, IDED7 is FDC Disk Change bit 7.
	Reserved	N/A	Not used in the XT hard disk mode.
4	$\overline{\text{HDCS0}}$	OH	Active low Hard Disk Chip Select 0 for IDE interface, AT/XT hard disk mode. This decodes the address space 1F0H-1F7H (default) if configured in AT mode (CR#06H<6> = 0) or 320H-323H if configured in XT mode (CR#06H<6> =1).
5	$\overline{\text{HDCS1}}$	OH	Active low Hard Disk Chip Select 1 for IDE interface, AT/XT hard disk mode. This decodes the address space 3F0-3F7H.
6	$\overline{\text{IDEENHI}}$	O	Active low High Data Buffer Enable, AT hard disk mode. $\overline{\text{IDEENHI}}$ is active only when $\overline{\text{IOCS16}}$ is active, I/O address 1F0H-1F7H, and AT mode is selected.
	Reserved	N/A	Not used in the XT hard disk mode.
7	$\overline{\text{IDEENLO}}$	O	Active low Low Data Buffer Enable, AT/XT hard disk mode. $\overline{\text{IDEENLO}}$is active when accessing I/O address 1F0H-1F7H and 3F6H-3F7H (AT mode) or 320H-323H (XT mode: 8 bit DMA or programmed I/O).
1	$\overline{\text{RTCCS}}$	O	Active low Real Time Clock chip select, AT/XT mode. $\overline{\text{RTCCS}}$ decodes I/O addresses 70H and 71H for the 146818 compatible RTC
2	$\overline{\text{GPCS}}$	O	Active low General Purpose Chip Select. The address is specified in the Configuration register #09H and #0AH with the mask bit specified in Configuration register #0AH decoded to generate this chip select signal.
	(OUT1)	O	OUT1 output from the serial port, when Conf. register #0BH<0> = 1

1.5 Floppy Interface (24 pins):

Pin No.	Symbol	Buffer Type	Description
71	X1/CLK	fclk	The external connection for parallel resonant 24 MHz crystal input. A CMOS compatible oscillator is required if a crystal is not used.
72	X2	O	24 MHz crystal. If an external clock is used, this pin should not be connected.
83	$\overline{\text{RDATA}}$	IS	The active low signal reads raw data from the disk. This is Schmitt input.
88	$\overline{\text{WDATA}}$	OD	This active low signal writes precompensated serial data to the selected drive. This is a high open current drain output and is not gated internally with the Write gate.
92,94	$\overline{\text{DRV0, 1}}$	OD	These active open drain outputs select drive 0-3. Two drives can be supported directly. An external decoder (2 to 4) is needed to select four drives.
82	DSKCHG	IS	This Diskette Change signal notifies the FDC that the disk drive door has been opened. This Schmitt latched input is inverted and read via bit 7 of I/O address 3F7H.
87	$\overline{\text{WGATE}}$	OD	This active low open drain signal enables the head to write onto the disk.
90	DIR	OD	This open drain output signal controls the head movement direction. (Low = Step in; High = Step out)
89	$\overline{\text{STEP}}$	OD	This active low output signal supplies the step pulse, at a programmable rate, to move the head for seek operation.
86	HDSEL	OD	This open drain output selects the head on the selected drive. (Low = side 0; High = side 1)
85	$\overline{\text{TRK0}}$	IS	This active low Schmitt input indicates that the head is in track 0 of the selected drive.
84	$\overline{\text{WRPRT}}$	IS	This active low Schmitt input indicates that the disk is write-protected. Any Write command is ignored.
97	$\overline{\text{INDEX}}$	IS	This active low Schmitt input indicates the beginning of a track.
95, 91	$\overline{\text{MTR0, 1}}$	OD	This active low open drain output selects motor drivers 0-3. Two motor drivers are supported directly. An external decoder (2 to 4) is needed to select four motor drivers. The motor enable bits are software controllable via the Digital Output Register (DOR).
74	FILTER	I/O	This signal is the output of the charge pump and the input to the VCO. PLL filter circuitry is connected to this pin, FGND250, FGND500 and analog ground.
79	FGND500	OL	This low impedence output signal is connected to 500 Kb/s (MFM) PLL filter circuitry.
78	FGND250	OL	This low impedence output signal is connected to 250 Kb/s (MFM) PLL filter circuitry.

1.5 Floppy Interface (Continued)

Pin No.	Symbol	Buffer Type	Description
81	PREN	I	This input selects precompensation mode: Low = Normal, High = Alternate. Precompensation values (shown in Floppy section) depend on the selected data rate and precompensate mode.
80	DRVTYP	I	When this input is low, the dual speed spindle motor driver is used. If 300Kb/s is selected via Data Rate register, the PLL actually runs at 250Kb/s. When this input is high (standard AT), the single speed spindle motor driver is used. The PLL runs at 300Kb/s when data rate is selected at 300Kb/s.
75	SETCUR	I	This signal is connected to the Analog ground via an external resistor to set the charge pump current for PLL filter.
96	RPM/LC	OD	Depending on DRVTYP input, this open drain output signal can function in two modes: 1. When DRVTYP is LOW (dual speed spindle), this output selects either 300RPM or 360RPM. This output is low when 250/300Kb/s is selected and high when 500Kb/s selected. 2. When DRVTYP is HIGH (single speed spindle), the output goes high when 500Kb/s is selected (high density media). It is also used to indicate when to reduce write current.
77	RVI	I	An external resistor connects this pin to Analog ground for PLL filter.
1.6 Mouse Port (2 pins):			
60	MCLK	IS/OB	This is a bi-directional PS/2 mouse port clock signal, open drain, 24 mA Driver
61	$\overline{\text{MDATA}}$	IS/OB	This is a bi-directional PS/2 mouse port data signal, open drain, 24 mA Driver
1.7 Power and Ground (8 pins):			
27,67	Vcc (2)		+5V Digital supply pins
18,43, 59,93	Vss (4)		0V Reference for the FDC digital, CPU interface, serial port, parallel port, and disk interface output drive circuitry, respectively.
73	AVcc		Analog +5V for PLL.
76	AVss		Analog ground for PLL

Buffer Types:

I = TTL input
IS = Schmitt-trigger input
O = TTL output
OH = High current TTL output
OB = Mid current open drain output
OC = Open Drain
OD = High current open drain output
OL = Low current open drain output
T = Tri-state TTL output, 24 mA
Iclk = Clock Input

2.0 SERIAL PORT (UART)

2.1 Introduction

One equivalent NS16450 UART is implemented on the 82C710. The serial port is fully compatible to the 16450 ACE registers. The programmable features allow data rates ranging from 50 baud to 115.2 Kbaud; 5 to 8 bit character size with 1 start and 1, 1.5, 2 stop bits; even, odd, sticky, or no parity; and prioritized interrupts. An interrupt from the UART is enabled or disabled (tri-stated) using the OUT2 bit. If a 1 is written to OUT2, UART, interrupt is enabled. Writing 0 tri-states the interrupt. OUT1 of the Serial Port can be selected to become an output. This pin can be configured to be either OUT1 of the Serial Port or a General Purpose Chip Select depending upon CR#0BH<0>. If CR#0BH=0, then pin 2 is $\overline{\text{GPCS}}$ (default); if CR#0BH=1, pin 2 becomes the OUT1 pin of the Serial Port. The serial port base address is relocated by writing different values to Config. Reg. #04H. An on-chip baud rate generator divides the input clock or crystal frequency by a number from 1 to 65535. This frequency is used for both receiving and transmitting serial data.

Serial-to-parallel conversion is performed on received data and parallel-to-serial conversion is performed on transmitted data. Status of the UART is available at any time. To access it, the CPU reads the appropriate status register in the UPC. The current state and type of a transfer are contained in this status information as are details regarding any errors encountered. The conditions under which the processor will be interrupted and the interrupt line to be used are programmable.

Control lines are provided to permit interfacing to a MODEM. Internal diagnostics are supported that permit simulation of break, parity, overrun and framing error conditions as well as operation in loopback mode.

2.2 Serial Port Registers

Addressing of the accessible UART registers is shown in Table 2.0 below. The base address of all registers is software programmable during the configuration sequence (see the section entitled "82C710 Configuration"). UART registers are located at sequentially increasing addresses above this base address. A UPC contains a single UART which contains one set of the registers described below.

Table 2.0 Addressing of UART Registers

Drab	A2	A1	A0	Offset	Register Name
0	0	0	0	0H	Received Buffer Register (R)
0	0	0	0	0H	Transmit Buffer Register (W)
0	0	0	1	1H	Interrupt Enable Register (R/W)
X	0	1	0	2H	Interrupt Flag Register (R/W)
X	0	1	1	3H	Byte Format Register (R/W)
X	1	0	0	4H	Modem Control Register (R/W)
X	1	0	1	5H	Line Status Register (R/W)
X	1	1	0	6H	Modem Status Register (R/W)
X	1	1	1	7H	Scratch Pad Register (R/W)
1	0	0	0	0H	Divisor LSB (R/W)
1	0	0	1	1H	Divisor MSB (R/W)

Where:

X = Don't Care
MSB = Most Significant Byte
LSB = Least Significant Byte
DRAB = Divisor Register Address Bit (Bit 7 of Byte Format Register)

BIT DEFINITIONS OF SERIAL PORT REGISTERS

2.2.1 *Receive Buffer (RB)*
Offset = 0H, Read only, DRAB = 0

This register holds the incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the UPC. This scheme uses an additional shift register (the Receive Shift Register; not user accessible) to assemble the incoming byte before it is loaded into the Receive Buffer.

2.2.2 *Transmit Buffer (TB)*
Offset=0H, Write only, DRAB=0

This register holds the data byte to be sent. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the UPC. This scheme uses a shift register (the Transmit Shift Register; not user accessible) which is loaded from the Transmit Buffer. The transmitted byte is then shifted out of the Transmit Shift Register to the TXD pin.

2.2.3 *Interrupt Enable Register (IER)*
Offset=1H, Read/Write, DRAB = 0

The low order 4 bits of this register control the enabling of each of the four possible types of interrupts. Setting a bit to a logic 1 enables the corresponding interrupt. It is possible to enable all, none, or some of the interrupt sources. Disabling all interrupts means that the interrupt flag register content is not valid and that none of the interrupt signals output by the UPC can be triggered by a UART. All other portions of the UART are unaffected by the disabling of interrupts. The individual bit definitions are as follows:

Bit 0: A logic 1 here causes an interrupt when the Receive Buffer contains valid data.

Bit 1: A logic 1 here causes an interrupt when the Transmit Buffer is empty.

Bit 2: A logic 1 here causes an interrupt when an error (Overrun, Parity, Framing or Break) has been encountered. The Line Status register must be read to determine the type of error.

Bit 3: A logic 1 here causes an interrupt when one of the bits in the MODEM Status register changes state.

Bits 4-7: These four bits are set to 0.

2.2.4 *Interrupt Flag Register (IFR)*
Offset = 2H, Read/Write, DRAB = X

When accessed, this register reports the highest pending interrupt. By reading it, the CPU can determine the source of the interrupt and can act accordingly. The Interrupt Flag Register (IFR) records the highest pending interrupt in bits 0 through 2. Other interrupts are temporarily disregarded (they are internally saved by the UPC) until the highest priority one is serviced.

Four levels of prioritized interrupts exist. In descending order of priority they are:

1. Line Status (highest priority)
2 Receive Buffer full
3. Transmit Buffer empty
4. MODEM Status (lowest priority)

Bit definitions for the IFR are as follows:

Bit 0: If this bit is a zero, an interrupt is pending and bits 1 and 2 can be read to determine the source of the interrupt. When this bit is a logic 1, no interrupts are pending. Note that this bit can be used in a polled environment to determine if an interrupt is pending. It can also be used for the same purpose with a hardwired interrupt priority scheme. In the latter case, bits 1 and 2 of this register act as a pointer to an interrupt service routine.

Bits 1 and 2: As indicated in Table 2.2, these two bits specify the type and source of the interrupt.

Bits 3-7: These five bits are set to 0.

2.2.5 *Byte Format Register (BFR)*
Offset = 3H, Read/Write, DRAB = X

This read/write register contains format information for the serial line. Since it can be read, a separate copy of its content need not be kept in system memory. Bit definitions are as follows:

Bits 0 and 1: These specify the word length for received and transmitted characters. Start, stop and parity bits are not included in the word length value. The word lengths are:

Bit 0	Bit 1	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: The combination of this bit and Bits 0 and 1 of this register determine the number of stop bits used with each transmitted character. The table below summarizes this information. Note that the receiver will ignore additional stop bits beyond the first regardless of the number of stop bits used when transmitting.

Bit 2	Word Length	Number of Stop Bits
0	—	1
1	5 Bits	1 1/2
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

Bit 3: A logic 1 in this bit enables parity generation (during transmission) and checking (during receipt). The parity bit is always after the last data bit but before the first stop bit. If enabled, a parity bit of the proper state (0 or 1) is generated such that the sum (carry ignored) of all data bits plus the parity bit produces either an even (even parity) or odd (odd parity) value.

Bit 4: This Even Parity bit controls parity sense. It is ignored unless Bit 3 is a logic 1. If Bits 3 and 4 are logic 1s (even parity), an even number of logic 1s will be transmitted and a parity error will be generated each time an odd number is received. If Bit 3 is a 1 and Bit 4 is a 0 (odd parity), an odd number of logic 1s will be transmitted and a parity error will be generated each time an even number is received.

Bit 5: This is the Force Parity bit. It ensures that the parity bit and sense (even or odd) match regardless of the sum normally used to determine parity. Thus if BFR Bits 3, 4 and 5 are all logic 1s (even parity), the parity bit transmitted will always be a 0 and a parity error will be detected if a logic 1 parity bit is received. If Bits 3 and 5 are 1 and Bit 4 is 0, the parity bit transmitted will always be a 1 and a parity error will be detected if a 0 parity bit is received.

Bit 6: This BREAK bit, when set to a logic 1, forces the transmitted data output pin TXD to a Spacing or logic 0 condition. This BREAK condition is terminated when Bit 6 is set to a 0. The operation of the transmitter logic is unaffected by the value of this bit; only the value of the TXD pin is affected. A BREAK condition is typically used to alert a terminal in a communications system. To prevent the transmission of erroneous data, follow the steps below:

1. Load a NULL character (all zeroes) into the Transmit Buffer.
2. Load Bit 6 (BREAK bit) after the next Transmit Buffer Empty (TBE) occurs.
3. Time the length of the BREAK condition by continuing to load NULL characters into the Transmit Buffer and counting the number loaded.
4. Clear the BREAK condition only after a Transmitter Empty (TEMT) condition occurs.

Bit 7: This Divisor Register Address Bit (DRAB) must be a logic 1 to permit access to the Divisor Registers. Access to all other internal UART registers requires that this bit be 0.

2.2.6 *Modem Control Register (MCB)*
Offset = 4H, Read/Write, DRAB = X

This byte-wide register is used to manage the connection to an external MODEM or data set. Bit definitions are as follows:

Bit 0: This $\overline{DTR}$ bit determines the state of the $\overline{DTR}$ output pin. Setting Bit 0 to a logic 1 forces $\overline{DTR}$ to its active state (logic 0). If Bit 0 is a logic 0, $\overline{DTR}$ will be inactive (logic 1). An external inverting buffer is typically used (to insure the proper polarity of $\overline{DTR}$) when connecting a UPC $\overline{DTR}$ output to a MODEM or data set.

Bit 1: This $\overline{RTS}$ bit determines the state of the corresponding $\overline{RTS}$ UPC output pin in a fashion identical to Bit 0 (see above).

Bit 2: This bit is used to control the OUT1 pin when Configuration Register B, bit 0, is set to 1 (the $\overline{OUT1}$ pin is multiplexed with $\overline{GPCS}$ pin through Register B). If Bit 2 is set to 0, the $\overline{OUT1}$ pin is 1; if it is set to 1, the $\overline{OUT1}$ pin is 0.

Bit 3: This bit is used to control the OUT2 pin. When OUT2 = 0 (default), the serial interrupt is forced into high impedance. When OUT1 = 1 the serial interrupt output is enabled.

Note: OUT2 is an internal chip signal.

In the normal mode (no loopback), this bit is OUT2. When OUT2 = 0 (default), the serial interrupt is forced into a high impedance. When OUT2 = 1, the interrupt output is enabled.

Bit 4: This Loopback bit is used for self-diagnostic purposes. If it is a logic 1:

1. The TXD UPC output pin is set to a logic 1 (Marking state) and it is disconnected from the output of the Transmit Shift Register.
2. The RXD UPC input pin is disconnected from the Receive Shift Register.
3. The input to the Receiver Shift Register is internally connected to the output of the Transmit Shift Register.
4. All MODEM control input pins ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected from the internal circuitry.
5. MODEM control output pins $\overline{DTR}$ and $\overline{RTS}$ are forced to their inactive state (logic 1).
6. MODEM control output $\overline{DTR}$ is connected internally to MODEM control input $\overline{DSR}$, MODEM control output $\overline{RTS}$ is internally connected to input $\overline{CTS}$, and MODEM Control Register (MCR) bit 2 determines the state of bit 6 of the MODEM Status Register (MSR). Bit 3 of the MCB controls bit 7 of the MSR.
7. Data which is transmitted will immediately be received, permitting the CPU to verify the data paths internal to the UPC and its connection to the CPU.

While operating in diagnostic loopback mode, interrupts are disabled. Interrupts are controlled by the Interrupt Enable register. Interrupts which are due to MODEM signals operate as documented, although the source is now the lower 4 bits of the MODEM Control Register rather than the MODEM input pin signals.

Bits 5, 6 and 7: These bits are set to 0.

Table 2.2 UART Interrupt Specifications (Interrupt Flag Register)

Bit 2	Bit 1	Bit 0	Priority	Type	Source	Servicing The Interrupt
0	0	1		NO INTERRUPT PENDING		
1	1	0	Highest	Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Read Line Status Register
1	0	0	Second	Receive Buffer Full	Receive Data	Read Receive
0	1	0	Third	Transmit Buffer Empty	Transmit Buffer	Read IFR or Write transmit buffer
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Carrier	Read MODEM Status Register

2.2.7 *Line Status Register (LSR)*
Offset = 5H, Read Only, DRAB = X

This byte-wide register supplies serial link status information to the CPU. A Receive Line Status interrupt is caused by one of the conditions flagged by Bits 1 through 4 of this register. It is read-only. Writes to it are used at the factory for testing purposes and are not recommended. Bit definitions are as follows:

Bit 0: This Receive Buffer Full (RBF) bit is set to a logic 1 when an incoming character has been transferred from the Receive Shift Register to the Receive Buffer. Reading the Receive Buffer resets it to a logic 0.

Bit 1: This Overrun Error bit is set to a logic 1 when a new character is transferred into the Receive Buffer before the previously received character was read by the CPU. The previously received character is lost. When the CPU reads the LSR, the Overrun Error bit is reset to a 0.

Bit 2: This Parity Error bit is set to a logic 1 whenever a parity error is detected (received character has a parity other than that selected). Reading the LSR resets this bit to a 0.

Bit 3: This Framing Error bit is set to a logic 1 when an incoming character has no stop bit after the last data bit or (if parity is enabled) after the parity bit. A valid stop bit is the presence of a Mark condition (logic 1) in the proper time slot after the last data bit or the parity bit. Reading the LSR resets this bit to a 0.

Bit 4: This Break Interrupt bit will be a logic 1 if a Space condition (logic 0) is present on the RXD line for an entire character time (start bit time, plus data bit times, plus parity bit time, plus stop bit time). Reading the LSR resets this bit to a 0.

Bit 5: This Transmit Buffer Empty (TBE) bit is set to a logic 1 when an outgoing character is loaded from the Transmit Buffer (TB) into the Transmit Shift Register. If the TBE interrupt is enabled, an interrupt will be generated when this bit is set. Writing a character to the TB resets this bit to a 0.

Bit 6: This Transmitter Empty (TEMT) bit will be set to a logic 1 when both the Transmit Buffer and the Transmit Shift Register are empty. When either of these two registers contains a character, this bit will be reset to a 0.

Bit 7: This bit is set to 0.

2.2.8 *MODEM Status Register (MSR)*
Offset = 6H, Read/Write, DRAB = X

This byte-wide register holds the current value of the MODEM control lines. It also sets a bit (to a logic 1) each time one of these control lines changes state. Reading the MSR resets all of the Change bits to 0. A MODEM Status Interrupt is generated (if it is enabled) when Bit 0, 1, 2 or 3 is set to a 1. Bit definitions are:

Bit 0: This is the Clear To Send Changed bit. It is set to a 1 if the $\overline{CTS}$ line has changed state since the last time the MSR was read.

Bit 1: This is the Data Set Ready Changed bit. It is set to a 1 if the $\overline{DSR}$ line has changed state since the last time the MSR was read.

Bit 2: This is the Rising Edge of Ring Indicator bit. It is set to a 1 if the $\overline{RI}$ line has changed from a logic 0 to a logic 1 since the last time the MSR was read.

Bit 3: This is the Data Carrier Detect Changed bit. It is set to a 1 if the $\overline{DCD}$ line has changed state since the last time the MSR was read.

Bit 4: This is the Clear To Send bit. It is the complement of the $\overline{CTS}$ pin. When in diagnostic loopback mode, this bit is identical to the $\overline{RTS}$ bit in the MODEM Control Register (MCR).

Bit 5: This is the Data Set Ready bit. It is the complement of the $\overline{DSR}$ pin. When in diagnostic loopback mode, this bit is identical to the $\overline{DTR}$ bit in the MCR.

Bit 6: This is the Ring Indicator bit. It is the complement of the $\overline{RI}$ pin. In diagnostic loopback mode, it is controlled by Bit 2 of the MCR.

Bit 7: This is the Data Carrier Detect bit. It is the complement of the $\overline{DCD}$ pin. In diagnostic loopback mode, it is controlled by Bit 3 of the MCR.

2.2.9 *Scratchpad Register*
Offset = 7H, Read/Write, DRAB = X

This byte-wide register has no effect on the UART within which it is located. It can be used for any purpose by the programmer.

2.3 Effects of Hardware Reset

Table 2.3 details the effect of a hardware RESET on the UART located in a UPC. Note that the UPC has a configuration option which permits only a part of the UART to be reset when a hardware RESET is applied. This option is useful when the UPC will monitor a serial link and wake up the CPU upon receipt of an incoming character. Bit 7 in UPC Configuration Register 1 controls this option. When Bit 7 is a 0, all registers in the UART except the Receive Buffer, Transmit Buffer and the Divisor Registers (LSB and MSB) will be reset when a hardware RESET occurs. If Bit 7 is a 1, none of the registers in the UART will be reset. See the Configuration section for more details. Table 2.3 assumes that Bit 7 of the UPC Configuration register is a zero.

Table 2.3 Action of a Hardware Reset on the 82C710 UART

Register or Signal	Cause of Reset	Reset State
Interrupt Enable Register	Hardware RESET	All bits = logic 0
Interrupt Flag Register	Hardware RESET	Bit 0 = logic 1 Other bits = logic 0
Byte Format Register	Hardware RESET	All bits = logic 0
MODEM Control Register	Hardware RESET	All bits = logic 0
Line Status Register	Hardware RESET	Bits 5, 6 = logic 1 Other bits = logic 0
MODEM Status Register	Hardware RESET	Bits 0-3 = logic 0 Bits 4-7 = Input Signal
TXD2 and TXD1	Hardware RESET	logic 1 (high)
Receive Line Status Interrupt	Hardware RESET or Read LSR	logic 0 (low)
Receive Buffer Full Interrupt	Hardware RESET or Read RB	logic 0 (low)
Transmit Buffer Empty Interrupt	Hardware RESET or Read TB	logic 0 (low)
MODEM Status Interrupt	Hardware RESET or Read MSR	logic 0 (low)
$\overline{RTS2}$ and $\overline{RTS1}$	Hardware RESET	logic 1 (high)
$\overline{DTR2}$ and $\overline{DTR1}$	Hardware RESET	logic 1 (high)

2.4 Baud Rate Generation

The UART contains a programmable Baud Generator. The 24 MHz crystal oscillator frequency input is divided by 13 to provide a frequency of 1.8462 MHz. This is sent to the Baud Rate Generator and divided by the divisor for the UART. The output frequency of the Baud Rate Generator is 16 x the baud rate, [(divisor # = (frequency input) ÷ (baud rate x 16)]. The output of the Baud Rate Generator drives the transmitter and receiver sections of the serial channel. Two 8-bit latches store the divisor in a 16-bit binary format. This Divisor Latch must be loaded during initalization to ensure proper operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded.

Table 2.4 lists decimal divisors to use with a crystal frequency of 24 MHz. The oscillator input to the chip should always be 24 MHz to ensure that the Floppy Disk Controller timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

3.0 PARALLEL PORT

3.1 Introduction

The Parallel Port is compatible to the IBM XT/AT Parallel Port, plus PS/2 like extended mode for bi-directional mode. When the parallel port is disabled via the configuration register, all outputs are disabled, and register contents are preserved. Upon power up, the control signals are inactive. The status register reflects the status signals.

3.2 Printer Interface Accessible Registers

Table 3.1 depicts the registers and I/O ports which are accessible for the parallel printer port. These are compatible with the IBM PC parallel port. Bit definitions for each of these registers are given after the diagram. All addresses for the parallel port are offsets from the base address specified during the UPC configuration process.

Table 2.4 Divisors, Baud Rates and Clock Frequencies

	1.8462 MHz Clock	
Divisor for Baud Rate	**Decimal Divisor for 16 X Clock**	**Percent Error (Note 1)**
50	2304	0.001
75	1536	
110	1047	
134.5	857	0.004
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.005
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	0.030

Note 1: The percent error for all Baud Rates, except where indicated otherwise, is 0.002%.

3.2.1 *Data Latch (Port A)*
***Offset** = 00H*

This read/write register is located at an offset of 0H from the base address of the parallel port. Data written to this register is transmitted to the printer. Data read from this port is identical to that which was last written.

3.2.2 *Printer Status Register (Port B)*
***Offset** = 01H*

This read-only register is located at an offset of 1H from the base address of the parallel port. Bit definitions are as follows:

Bit 7: $\overline{\text{Busy}}$. This bit reflects the state of the UPC $\overline{\text{BUSY}}$ input pin. A 0 means that the printer is busy and cannot accept data. A 1 indicates that the printer is ready to accept data.

Bit 6: $\overline{\text{ACK}}$. This bit reflects the state of the $\overline{\text{ACK}}$ input pin. A 0 means that the printer has received a character and is ready to accept another. A 1 means that it is still reading the last character sent or data has not been received.

Bit 5: PE-Paper Empty. This bit reflects the state of the UPC PE input pin. A 1 indicates a paper end condition. A 0 indicates the presence of paper.

Bit 4: SLCT. This bit reflects the state of the UPC SLCT input pin. A 1 means the printer is online. A 0 means it is not selected.

Bit 3: $\overline{\text{ERROR}}$. This bit reflects the inverted state of the UPC $\overline{\text{ERROR}}$ input pin. A 0 means that an error condition has been detected. A 1 indicates no errors.

Bits 2-0: Reserved.

3.2.3 *Printer Controls Register (Port C)*
***Offset** = 02H*

This read/write register is located at an offset of 02H from the base address of the parallel port. Bit definitions are:

Bits 7-6: Reserved. Reset to 0.

Bit 5: Parallel Control Direction, valid in extended mode only (CR#1 <6>=1). In printer mode, the direction is always out, regardless of the state of this bit. In the extended mode, a 0 means an output/write condition. A 1 means an input/read condition.

Bit 4: IRQEN. This bit is used to enable or disable interrupts resulting from the printer $\overline{\text{ACK}}$ signal. A 1 generates interrupts when $\overline{\text{ACK}}$ changes from active to inactive. The CPU will be interrupted on the IRQ line specified in the UPC configuration RAM. A 0 means that IRQ is disabled.

Bit 3: $\overline{\text{SLCTIN}}$ (pin 49). Used to drive the UPC $\overline{\text{SLCTIN}}$ output pin. A 1 selects the printer. A 0 means the printer is not selected.

Bit 2: $\overline{\text{INIT}}$ (pin 50). Used to control the UPC $\overline{\text{INIT}}$ output pin. A 0 (active low) starts the printer (50 μs pulse minimum). A 0 initializes the printer.

Bit 1: $\overline{\text{AUTOFD}}$ (pin 51). Used to control the UPC $\overline{\text{AUTOFD}}$ output pin. A 1 causes the printer to generate a line feed after each line is printed. A 0 means no autofeed.

Bit 0: $\overline{\text{STROBE}}$ (pin 48). Used to control the UPC $\overline{\text{STROBE}}$ output pin. A 1 in this bit generates the active low pulse (0.5 μs pulse minimum) which is required to clock data into the printer. There is a 0.5 μs data setup time requirement before $\overline{\text{STROBE}}$ can be asserted. A 0 means there will be no strobe.

3.3 Parallel Port Connector

The parallel port connector is a DB-25 female connector. The 82C710 parallel port signals are connected directly to the parallel port connector. Typically the signals are assigned to the pins as shown below:

Pin	I/O	Name
1	O	$\overline{\text{STROBE}}$
2-9	I/O	PD0-PD7
10	I	$\overline{\text{ACK}}$
11	I	BUSY
12	I	PE
13	I	SLCT
14	O	$\overline{\text{AUTOFD}}$
15	I	$\overline{\text{ERROR}}$
16	O	$\overline{\text{INT}}$
17	O	$\overline{\text{SLCTIN}}$

Table 3.1 Summary of Accessible Parallel Port Registers

		7	6	5	4	3	2	1	0
A	XX0H	DATA							
B	XX1H	BUSY	$\overline{\text{ACK}}$	PE	$\overline{\text{SCLTIN}}$	$\overline{\text{ERROR}}$	R	R	R
C	XX2H	R	R	DIR	IRQEN	$\overline{\text{SLCTIN}}$	$\overline{\text{INT}}$	$\overline{\text{AUTOFD}}$	$\overline{\text{STROBE}}$

Note: R means Reserved

DATA LATCH (PORT A)

STATUS (PORT B)

CONTROL (PORT C)

3.4 Hardware Reset

The hardware reset is performed by applying the logic 1 to the 82C710 RESET pin. The table below shows the value of the parallel port registers after the hardware reset.

Parallel Register	Reset Value
Data Register	Don't care
Status Register	80H
Control Register	00H

4.0 INTEGRATED DRIVE ELECTRONICS INTERFACE

4.1 Introduction

The IDE interface allows users to utilize hard disks with imbedded controller (AT and XT interface). The 82C710 provides the control signals for the IDE interface and the IDE buffers, as shown below:

$\overline{\text{IDEENLO}}$: Low Byte Buffer Enable (AT and XT).

$\overline{\text{IDEENHI}}$: High Byte Buffer Enable (AT only).

$\overline{\text{HDCS0}}$: Primary Hard Disk Chip Select used to access the Task File Registers decodes 1F0H-1F7H (AT) or 320H-323H (XT).

$\overline{\text{HDCS1}}$: Secondary Hard Disk Chip Select, decodes 3F0H-3F7H (AT and XT).

$\overline{\text{IOCS16}}$: When active it indicates 16 bit I/O transfer (AT only).

$\overline{\text{IDED7}}$: D7 of the IDE interface should be connected to this pin (AT only).

$\overline{\text{HDACK}}$: Hard Disk DMA Acknowledge (XT only).

$\overline{\text{IDEENL}}$ becomes active when the 82C710 decodes addresses 1F0H-1F7H, 3F6H, and 3F7H in the AT mode, or 320H-323H and DMA transfers ($\overline{\text{HDACK}}$=0) in the XT mode. $\overline{\text{IDEENHI}}$ becomes active only when $\overline{\text{IOCS16}}$ is active and address range 1F0H-1F7H, and in AT mode (CR#0CH<6>=1). $\overline{\text{IOCS16}}$ is generated by the Hard Disk Controller when it requires a 16 bit transfer. IDED7 should be connected directly to data bit 7 of the IDE interface. The AT mode supports programmed I/O only (8 and 16 bit). XT mode supports only 8 bit DMA and 8 bit programmed I/O. The $\overline{\text{IOCS16}}$/$\overline{\text{HDACK}}$ pin is multiplexed, in the AT mode it is $\overline{\text{IOCS16}}$, in the XT mode it is $\overline{\text{HDACK}}$ signal.

4.2 AT/XT modes in IDE interface

There are 2 IDE interface modes:

AT mode: 8/16 bit programmed I/O only (no DMA). AT mode decodes addresses 1F0H-1F7H, 3F6H and 3F7H. Normal transfer is 8 bit; 16 bit transfer is performed when $\overline{\text{IOCS16}}$ is active and on data register (1F0H). Both $\overline{\text{IDEENLO}}$ (low buffer enable) and $\overline{\text{IDEENHI}}$ (high buffer enable) are active during 16 bit transfer. $\overline{\text{HDCS0}}$ is active whenever the 82C710 decodes programmed I/O address 1F0H-1F7H. $\overline{\text{IDEENLO}}$ is active on all AT mode addresses. On the low byte buffer, only 7 bits (D0-D6) are connected to the data bus. Bit 7 is a special case; it is sourced from the 82C710. On the IDE interface, IDED7 is connected directly to the connector. D7 of the 82C710 provides data bit 7 to the host interface. Normally the 82C710 functions as a buffer for D7, but, when reading 3F7H, D0-D6 of the 82C710 are tri-stated and $\overline{\text{IDEENLO}}$ is enabled to transfer data bits D0-D6 from the IDE to the host; D7 should be supplied by the Floppy Disk Interface.

XT mode: 8 bit programmed I/O or DMA (no 16 bit). Normally DMA transfer is done from the data register (320H) only. During a DMA cycle (indicated by active AEN and HDACK) IDEENLO is active, allowing the data to flow through the low byte buffer. XT mode decodes I/O address range 320H-323H.

4.3 Hard Disk Register

Below is the short summary description and bit definition of the hard disk registers. More information can be obtained from IBM AT Technical Reference.

4.3.1 *Task File Registers*

Data Register (1F0H, R/W)

Read and Write to sector buffer. Accessed only when Read or Write command is executed.

Error Register (1F1H, R)

This register contains the status of the last executed command.

Bit 0: Set 1 if Data Address Mark not found.
Bit 1: Set 1 if track 0 is error.
Bit 2: Set 1 if command is aborted.
Bit 3: Not used.
Bit 4: Set 1 if ID is not found.
Bit 5: Not used.
Bit 6: Set 1 if Data ECC error.
Bit 7: Set 1 if bad block detect.

Write Compensation Register (1F1H, W)

This register contains the starting cylinder value divided by 4.

Sector Count Register (1F2H, R/W)

This register contains the number of sectors during a Verify, Read, Write or Format command. Note that a 0 value means 256 sector transfer.

Sector Number Register (1F3H, R/W)

This register contains the target's logical sector number of Read, Write and Verify command.

Cylinder Number Register (R/W)
1F4H = Low, 1F5H = High

These registers contain LSB and MSB of the first cylinder number where the disk is to be accessed for Read, Write, Seek and Verify command.

Drive/Head Register (1F6H, R/W)

Bit 7, 5: Set to 1
Bit 6: Set to 0
Bit 4: Drive select. Primary = 0, Secondary = 1

Bit 3-0: 4 bit binary represents the head number (bit 3:MSB and bit 0:LSB)

Status Register (1F7H, R)

This register contains the status of the drive:

Bit 7: Set to 1 if the drive is busy.
Bit 6: Set to 1 if the drive is ready to accept command.
Bit 5: Set to 1 if write fault condition occurred.
Bit 4: Set to 1 if seek command is completed.
Bit 3: Set to 1 if drive is ready to transfer data.
Bit 2: Set to 1 if data correction is sucessful.
Bit 1: Set to 1 if index mark is detected.
Bit 0: Set to 1 if error occur from last command.

Command Register (1F7H, W)

This register contains command op code for fixed disk operation.

4.3.2 Other Registers

Digital Input Register Definition (3F7H, R)

Bit 7: Diskette Change, Diskette interface status (FDC)
Bit 6: Write Gate (HDC)
Bit 5: Head Select 3/Reduced Write Current (HDC)
Bit 4: Head Select 2 (HDC)
Bit 3: Head Select 1 (HDC)
Bit 2: Head Select 0 (HDC)
Bit 1: Drive Select 1 (HDC)
Bit 0: Drive Select 0 (HDC)

Fixed Disk Register (3F6H, W)

Bits 7-4: Not Used
Bit 3: HEAD3EN
Bit 2: RESET
0 = Normal operation, default
1 = Generate reset to HDC
Bit 1: $\overline{\text{IRQEN}}$
0 = Enabled interrupt
1 = Disable interrupt, default
Bit 0: Reserved

5.0 FLOPPY DISK CONTROLLER (FDC)

5.1 Introduction

The 82C710 contains a fully compatible NEC μPD72065B Floppy Disk Controller (FDC), an on-chip precision Analog Data Separator (ADS) and many other enhancement features. The XT/AT bus interface circuitry is completely integrated with the 82C710 and requires no external logic when interfaced with the XT/AT bus. The licensed 765 core guarantees the compatibility. The on-chip Data Separator supports 250/300/500Kb/s and 1Mb/s. Depending on the selected data rate, up to 3 external filters are automatically switched in. This provides optimum performance in the PC environment which uses 250/300 and 500Kb/s data rates. The 48 mA Floppy interface buffer allows the 82C710 to connect directly to the disk drive.

5.2 Floppy Disk Register Description

The 82C710 contains 5 registers which may be accessed by the main system processor. The description of each register is shown below:

Main Status Register (3F4H, Read only)

The Main Status Register contains the information for the FDC, and may be accessed any time.

Bit 7: Request for Master (RQM). This bit indicates that the data register is ready to send or receive data to or from the CPU. Both bits DIO and RQM should be used to perform the handshaking function of "ready" and "direction" to the CPU.

Bit 6: Data Direction (DIO). This bit indicates the direction of data transfer between the FDC and the data register. If DIO=1, then data is transferred from the data register to the CPU. If DIO=0, then transfer is from the CPU to the data register.

Bit 5: Execution Mode (EXM). This bit is set only when the execution phase is in the non DMA mode. When this bit goes low, the execution phase has ended and the result phase has begun. This bit operates only in the non DMA mode.

Bit 4: Command in progress. Set high when the Read or Write command is in progress. The FDC will not accept any other command.

Bit 3: Drive 3 seeking. Set high when drive 3 is in the Seek mode. The FDC will not accept any other command.

Bit 2: *Drive 2 seeking. Set high when drive 2* is in the Seek mode. The FDC will not accept any other command.

Bit 1: *Drive 1 seeking.* Set high when drive 1 is in the Seek mode. The FDC will not accept any other command.

Bit 0: Drive 0 seeking. Set high when drive 0 is in the Seek mode. The FDC will not accept any other command.

Note: Some softwares write to this register instead of register 3F5H. For some NMOS 765 FDCs, a write to register 3F4H acts the same as a write to register 3F5H. For all CMOS 765s and the 82C710, a write to register 3F4H is ignored.

Data Register (3F5H, Read/ Write)

All Commands, Status, and Data transferred between the CPU and the FDC flows through this register. The command is loaded into this register based on the Request for Master and Data Direction bits (bits 7 and 6 of Main Status Register).

During the Command phase, all information required to perform a particular operation is written into the Data Register.

During the Result phase, the Result Status is read from the Data Register (it actually consists of four status registers, ST0-ST3, in the stack with only one presented to the bus at a time).

Status Register 0 (ST0)

Bits 7-6: Interrupt Code (IC)

b7,	b6	
0	0	Normal termination of program completed.
0	1	Abnormal Termination of command. (AT)
1	0	Invalid Command issued.
1	1	Ready signal changed during execution.

Bit 5: Seek End (SE). Set high to indicate the completion of Seek command.

Bit 4: Equipment Check (EC). Set high to indicate track 0 signal failed or Fault signal received.

Bit 3: Not Ready. Always set to 0.

Bit 2: Head Select (HS). Set high to indicate the state of head at interrupt.

Bit 1: Unit Select 1 (US1). This flag indicates a drive unit number at interupt.

Bit 0: Unit Select 0 (US0). This flag indicates a drive unit number at interrupt.

Status Register 1 (ST1)

Bit 7: End of cylinder (EN). Set high to indicate that the FDC has tried to access a sector beyond the final sector of a cylinder.

Bit 6: Not used. Always set to 0.

Bit 5: *Data Error (DE). Set high to indicate* the FDC detects a CRC error in ID field or data field.

Bit 4: *Overrun* (OR). Set high to indicate the FDC is not serviced by the CPU during the data transfer within a certain time interval.

Bit 3: Not used. Always set to 0.

Bit 2: No Data (ND). Set high to indicate: 1) The FDC can not find the sector specified in Internal Data Register (IDR) during the execution of READ DATA, WRITE DELETED or SCAN command.

2) The FDC read ID field without an error during the execution of READ ID command.

3) The FDC can not find the starting sector during the execution of READ A CYLINDER.

Bit 1: Not writable (NW). Set high to indicate the Write Protect signal is detected during execution of WRITE DATA, WRITE DELECTED DATA, FORMAT A CYLINDER commands.

Bit 0: Missing Address Mark (MA). Set high to indicate that the FDC can not detect Data Address Mark or Deleted Data Address Mark.

Status Register 2 (ST2)

Bit 7: Not used. Always set to 0.

Bit 6: Control Mark (CM). Set high to indicate the FDC encountered a sector which contains a Deleted Data Address Mark during the execution of READ DATA or SCAN command.

Bit 5: Data Error (DE). Set high to indicate FDC detects a CRC error in the data field.

Bit 4: Wrong Cylinder (WC). Set high to indicate the content of the cylinder is different from that stored in the Internal Data Register (IDR).

Bit 3: Scan Equal Hit (SH). Set high to indicate the condition "equal" has been satisfied during the execution of SCAN command.

Bit 2: Scan Not Satisfied (SN). Set high to indicate the FDC can not find a sector on the cylinder which meets the specified condition during the execution of SCAN command.

Bit 1: Bad cylinder (BC). Set high to indicate the content of the cylinder on the medium is different from that stored in IDR and the content of the cylinder is FFH.

Bit 0: Missing Address Mark (MD). Set high to indicate that the FDC can not find the Data Address Mark or Deleted Data Address Mark when reading the drive.

Status Register 3 (ST3)

Bit 7: Fault (F). Indicates the status of the Fault signal from the Floppy Disk Drive (FDD).

Bit 6: Write Protected (WP). Indicates the status of the Write Protected signal from the FDD.

Bit 5: Ready (RY). Indicates the status of the Ready signal from the FDD.

Bit 4: Track 0 Cylinder (T0). Indicates the status of theTrack 0 signal from the FDD.

Bit 3: Two Side (TS). Indicates the status of the Two Side signal from the FDD.

Bit 2: Head Address (HD). Indicates the status of the Side Select signal to the FDD.

Bit 1: Unit Select 1 (US1). Indicates the status of the Unit Select 1 signal to the FDD.

Bit 0: Unit Select 0 (US0). Indicates the status of the Unit Select 0 signal to the FDD.

NOTE: μPD765 internal drive select bits US0 and US1 are not used.

Digital Output Register (Drive Control Register) (3F2H Write only)

This 8-bit write only register controls the drive select, motor enable, DMA enable and reset functions.

Bit 7:	Motor Enable 3.
Bit 6:	Motor Enable 2.
Bit 5:	Motor Enable 1.
Bit 4:	Motor Enable 0.
Bit 3:	Enable DMA (DRQ and $\overline{\text{DACK}}$) and interrupt (IRQ).
Bit 2:	Reset floppy controller.
Bits 1,0:	Drive selects.

Below is the Drive/Motor activation table.

Table 5.1 Drive/Motor Selection

b7	b6	b5	b4	b1	b0	Driver
			1	0	0	0
		1		0	1	1
	1			1	0	2
1				1	1	3

Configuration Control Register (Data Rate Register) (3F7H Write only)

This is a two bit register that controls the data rate the controller uses. This register feeds the logic that selects the data rates by programming a prescaler that divides the crystal or clock input by either 3, 5 or 6. This causes either 4MHz, 4.8 MHz and 8MHz to be input as the master clock for the controller core.

Bits 7-2:	Not used.
Bits 1,0:	Data Rate select (determined as shown in Table 5.8 in the PLL filter section).

Fixed Disk Register (3F7H, Read only)

Bit 7:	Disk Changed. This bit is the complement of the Disk Changed input pin.
Bit 6-0:	These bits are used by the Hard Disk Controller. They are tri-stated when reading this register.

5.3 Command Sequence

The 82C710 FDC is capable of generating 17 different commands. Each command is initiated by a multi-byte transfer from the CPU, and the result after execution may also be multi-byte transferred back to the CPU. Most commands involve three phases:

COMMAND PHASE: The FDC receives all information required to perform a particular operation.

EXECUTION PHASE: The FDC performs the instructed command.

RESULT PHASE: After completion of the operation, status and other housekeeping information is made available to the CPU.

5.4 Modes of Operation

DMA Mode

If the DMA mode is selected, a DMA request is initiated in the Execution phase when a byte is ready to be transferred. The DMA mode is enabled via the DMA bit in the SPECIFY command, and the DMA signals are enabled via the Drive Control Register. After the last byte is transferred, an interrupt is generated to indicate the beginning of the Result phase.

Interrupt Mode (Non-DMA)

If Non-DMA is selected, an interrupt is generated in the Execution phase when a byte is ready to be transferred. The Main status register is read to verify that the interrupt is for data transfer. When data is read or written to the Data Register, the interrupt will be cleared. When the last byte is transferred, the interrupt is also generated to indicate the beginning of Result phase.

5.5 Command Description

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation". The Read Data Command may be terminated by the receipt of a Terminal Count (TC) signal. TC should be issued at the same time that the DACK for the last byte to data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 5.2 below shows the Transfer Capacity.

The "multitrack" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

Table 5.2 Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field,), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, then the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 microsec in the FM Mode, and every 13 microsec in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 5.3 shows the value for C, H, R, and N, when the processor terminates the Command.

Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

Table 5.3

		Final Sector Transferred to Processor	ID Information at Result Phase			
MT	HD		C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
0	0	Equal to EOT	C + 1	NC	R = 01	NC
0	1	Less than EOT	NC	NC	R + 1	NC
0	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
1	0	Equal to EOT	NC	LSB	R = 01	NC
1	1	Less than EOT	NC	NC	R + 1	NC
1	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N = 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 microsec in the FM mode, and every 13 microsec in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read A Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDE HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command. This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDE HOLE for the second time, then it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA 9 (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette. Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3470 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (Number of bytes/sector), SC (Sectors/Cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively. Table 5.4 shows the relationship between N, SC, and GPL for various sector sizes.

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of

Table 5.4

Mode	Sector Size	N	SC	GPL(1)	GPL(2,3)
	8" Drives (360 RPM, 500 Kb/s)				
RM	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	0G	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
	5 1/4" DRIVES (300 RPM, 250 KB/S)				
RM	129	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
	3 1/2" DRIVES (300 RPM, 250 KB/S)				
RM	128	00	0F	07	1B
	256	01	09	09	2A
	512	02	05	1B	3A
MFM	256	01	0F	0E	36
	512	02	09	1B	54
	1024	03	05	35	74

Notes:
1. Suggested values of GPL in Read or Write command to avoid splice point between data field and ID field of contiguous sections.
2. Suggested value of GPL in Format command.
3. All values except sector size and hexidecimal.
4. In MFM mode the FDC cannot perform a Read/Write/Format operation with 128 bytes/sector (N=00)

data which meets the conditions of DFDD = D PROCESSOR, DFDD < D PROCESSOR, OR DFDD > D PROCESSOR. The hexidecimal byte of FF either from memory for FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP —> R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 5.5 shows the status of bits SH and SN under various conditions of SCAN.

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

Table 5.5 SH and SN Status

COMMAND	STATUS REGISTER 2		COMMENT
	BIT2=SN	BIT3=SH	
Scan Equal	0	1	DFDD=DCPU
	1	0	DFDD< >DCPU
Scan Low or Equal	0	1	DFDD=DCPU
	0	0	DFDD<DCPU
	1	0	DFDD>DCPU
Scan High or Equal	0	1	DFDD=DCPU
	0	0	DFDD>DCPU
	1	0	DFDD<DCPU

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 microsec (FM Mode) or 13 microsec (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number) and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued.
(Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued.
(Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB0-DB3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in the process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 microsec, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 do not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms...OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the HeadLoad signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms...7F = 254 ms).

The time intervals mentioned above are a direct function of the clock. Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC765 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high (1) indicating to the processor that the FDC is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Version

The Version command was added to distinguished the μPD765B from the μPD765A. The response to this command is the same as the Invalid command except that a processor read of Status Register 0 returns 90 Hex instead of 80 Hex.

5.6 Analog Data Separator

The 82C710 on-chip Analog Data Separator (ADS) consists of an analog Phase Lock Loop (PLL) and its associated circuitry. The PLL is composed of four main components: the phase comparator, filter, Voltage Control Oscillator (VCO) and programmable divider. The phase comparator detects the phase difference between the raw data read from the disk and the divider's output. The phase difference is converted into a current which either charges or discharges the filter. The VCO varies due to the voltage changes of the filter. This reduces the phase difference until the divider output frequency matches the average frequency of the data read from the disk. The block diagram of the Data Separator is shown in Figure 5.1 .

Table 5.6

STATUS REGISTER 0

SEEK END BITS 5	INTERRUPT CODE BIT 6	INTERRUPT CODE BIT 7	CAUSE
0	1	1	Ready Line changed state, either polarity
1	1	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

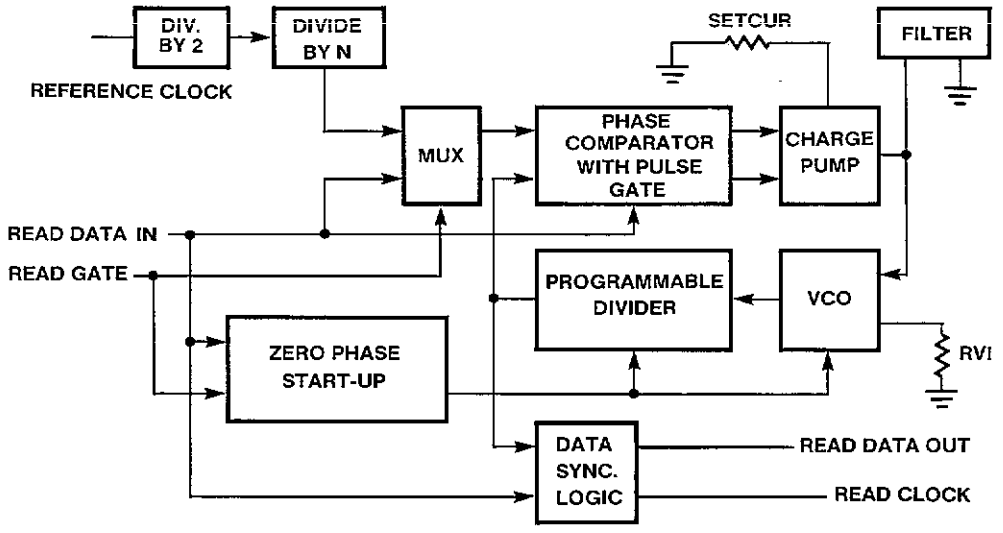


Figure 5.1 Analog Data Separator Block Diagram

PLL Filter

The 82C710 Analog Data Separator requires an external filter in order to run at different data rates. This filter functions as the current sink and source when the phase difference is converted to a current. Figure 5.2 is a typical 250/300/500 Kb/s filter configuration with recommended values (Table 5.7).

Filter component tolerances are:
R1, R2 = ± 1%
R3, R4 = ± 5%
C1, C2, C3 = ± 10%

Table 5.7: Filter Values

R1	R2	R3	R4	C1	C2	C3
18K	6.8K	560	560	0.027	0.047	1500
	ohms			pF	pF	pF

5.7 Drive Polling

After the reset has been sent to 82C710, the FDC will automatically go into the polling mode. In between command, the FDC polls all the drives looking for a change in ready line from any of the drives. If the ready line changes state (usually due to a door opening or closing), then the FDC will generate an interrupt. When the Status Register 0 (ST0) is read (after the Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the ready line by the FDC occurs continuously between commands, thus notifying the CPU which drives are on and off line. Each drive is polled every 1.024ms except during Read/Write command. When used 4MHz clock for interfacing minifloppies, the polling is 2.048ms.

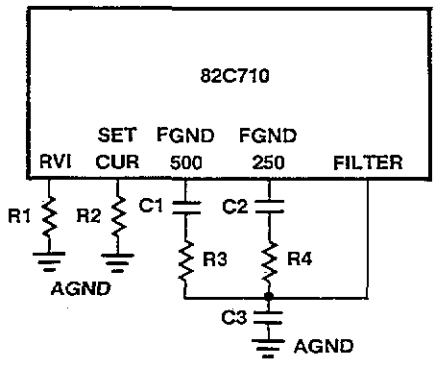


Figure 5.2 Filter Configuration

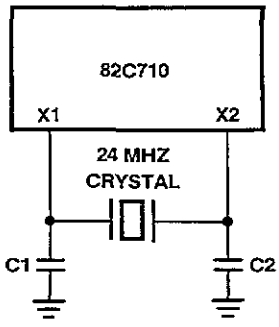


Figure 5.3 Crystal Circuit

Typical values for C1 and C2 are 20pF.

Crystal Specification:
Frequency: 24 Mhz
Mode: Parallel Resonant
Fundamental mode.
Shunt capacitance: Less than 5pF.
Series resistance: Less than 40 ohms.

5.8 Crystal/Clock

The 24 MHz crystal clock can be supplied by either crystal or MOS level oscillator. The typical crystal circuit with recommended values is shown in figure 5.3.

Table 5.8: Data Rate and Precompensation Values

D1 D0 **	DRVTYP Pin	Data Rate MFM (Kb/s)	Normal Precomp* (ns)	Alternate Precomp* (ns)	FGND pin Enabled	RPM/LC Pin Level
0 0	X	500	125	125	FGND500	High
0 1	0	250	125	250	FGND250	Low
0 1	1	300	208	208	FGND250	Low
1 0	0	250	125	250	FGND250	Low
1 0	1	250	125	250	FGND250	Low
1 1	0	1000	63	83	None	High
1 1	1	1000	83	83	None	Low

* Normal values when PUMP/PREN pin set low; Alternate values when PUMP/PREN pin set high.
** D0 and D1 are Data Rate Control Bits.

5.9 Instruction Set Table

The following pages are Command symbol description and μP756 instruction sets.

Table 5.9: Instruction Set Table

SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
C	Cylinder	The current/selected cylinder (track) number 0 through 76 of the medium.
D	Data	The Data pattern which is going to be written into a Sector.
D7-D0	Data Bus	8-Bit Data bus. D7 is a most significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the Data Length which users are going to read out or write into the Sector.
EOT	End Of Track	The final Sector number of the Cylinder. During R/W, the FDC stops data transfer after a sector # equal to EOT.
GPL	Gap Length	The length of Gap 3. During R/W command, this value determines the # of bytes that VCO will stay low after CRC bytes. During Format, it determines the size of Gap 3.
H	Head Address	Head Number 0 or 1 as specified in ID field.
HD	Head	Selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	Head Load Time in the FDD (2 to 254 ms in 2ms steps).
HUT	Head Unload Time	Head Unload time after Read/Write operation (16 to 240ms in 16ms increments).
MF	FM or MFM mode	If MF is low, FM mode is selected. High is MFM mode.
MT	Multi-Track	If MT is high, multi-track operation is performed. If MT = 1 after finishing the R/W on side 0, FDC automatically starts searching for sector 1 on side 1.

Table 5.9: Instruction Set Table (Continued)

SYMBOL	NAME	DESCRIPTION
N	Number	Number of Data Bytes written into a sector.
NCN	New Cylinder Num.	New Cylinder Number which is reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA mode	Operation in non-DMA mode.
PCN	Present Cyl. Num.	Cylinder number at the completion of SENSE INTERRUPT. Status command. Position of Head at the present time.
R	Record	Sector number which will be read or written.
R/W	Read/Write	Read or Write signal.
SC	Sector	Number of Sectors per Cylinder.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	Stepping rate of FDD. (1 to 16ms in 1 ms increments.) Stepping rate applied for all drivers (F = 1 ms, E = 2ms)
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Four registers store the status information after a command is executed. This information is available during the result phase and read only after a command has been executed.
STP		During SCAN operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from CPU; and if STP = 2, the alternate sectors are read and compared.
US0, US1	Unit Select	Selected drive number 0 or 1. Programmed in commands. Not used for external drive selection, which is based on Digital Output Register.

82C710 Instruction Set

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Format A Track										
Command	W	0	MF	0	0	1	1	0	1	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				N	----------			Bytes/Sector
	W	----------				SC	----------			Sectors/Track
	W	----------				GPL	----------			Gap 3
	W	----------				D	----------			Filter Byte
Execution										
Result	R	----------				ST 0	----------			Status
	R	----------				ST 1	----------			Information after
	R	----------				ST 2	----------			Command
	R	----------				C	----------			Execution
	R	----------				H	----------			ID information
	R	----------				R	----------			has no meaning
	R	----------				N	----------			
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command Code
Execution	W	X	X	X	X	X	0	US1	US0	Head retracted to Track 0
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				NCN	----------			
Execution										Head is positioned over proper cylinder on diskette.
Invalid										
Command	W	----------				Invalid Codes				Invalid Code FDC in standby
Result	R	----------				ST 0	----------			ST 0 = 80H

82C710 Instruction Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command Code
	W	X	X	X	X	X	*HD*	*US1*	*US0*	
Execution										The first correct ID information on cylinders stored in Data Register
Result	R	----------				ST 0			----------	Status
	R	----------				ST 1			----------	information after
	R	----------				ST 2			----------	the execution
	R	----------				C			----------	
	R	----------				H			----------	Sector ID read
	R	----------				R			----------	during exection
	R	----------				N			----------	phase
Sense Interrupt Status										
	W	0	0	0	0	1	0	0	0	Command Code
Result	R	----------				STO			----------	Status
Command	R	----------				PCN			----------	information at the end of Seek operation about FDC
Sense Drive Interrupt										
	W	0	0	0	0	0	1	0	0	Command code
	W	X	X	X	X	X	HD	US1	US0	
Result Command	R	----------				ST 3			----------	Status information about the FDC
Specify										
Command	W	0	0	0	0	0	0	1	1	Command code
	W	----------		SAT		----------		----------	HUT	
	W	HLT	----------			----------		----------	ND	
Version										
Command	W	X	X	X	1	0	0	0	0	Invalid Code FDC in standby
Result	R	----------				ST 0			----------	ST 0 = 90H

82C710 Instruction Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read A Track										
Command	W	0	MF	SK	0	0	0	1	0	Command Code
	W	X	X	X	X	X	HD	US1	US0	Sector ID
	W	----------				C	----------			information prior
	W	----------				H	----------			to Command
	W	----------				R	----------			execution.
	W	----------				N	----------			
	W	----------				EOT	----------			Data transfer
	W	----------				GPL	----------			between CPU
	W	----------				DTL	----------			and FDD FDC
Execution										reads all data fields from index hole to EOT
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				C	----------			Sector ID
	W	----------				H	----------			information prior
	W	----------				R	----------			to Command
	W	----------				N	----------			execution.
	W	----------				EOT	----------			
	W	----------				GPL	----------			
	W	----------				DTL	----------			Data compared
Execution										between FDD and CPU
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			

82C710 Instruction Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				C	----------			Sector ID
	W	----------				H	----------			information prior
	W	----------				R	----------			to Command
	W	----------				N	----------			execution.
	W	----------				EOT	----------			
	W	----------				GPL	----------			
	W	----------				DTL	----------			
Execution										Data compared between FDD and CPU
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				C	----------			Sector ID
	W	----------				H	----------			information prior
	W	----------				R	----------			to Command
	W	----------				N	----------			execution.
	W	----------				EOT	----------			
	W	----------				GPL	----------			
	W	----------				DTL	----------			
Execution										Data compared between FDD and CPU
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			

82C710 Instruction Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				C	----------			Sector ID
	W	----------				H	----------			information prior
	W	----------				R	----------			to Command
	W	----------				N	----------			execution. The 4
	W	----------				EOT	----------			bytes are
	W	----------				GPL	----------			commanded
	W	----------				DTL	----------			against header.
Execution										Data transfer between CPU and FDD
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				C	----------			Sector ID
	W	----------				H	----------			information prior
	W	----------				R	----------			to Command
	W	----------				N	----------			execution. The 4
	W	----------				EOT	----------			bytes are
	W	----------				GPL	----------			commanded
	W	----------				DTL	----------			against header.
Execution										Data transfer between CPU and FDD
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			

82C710 Instruction Set (Continued)

Phase	R/W	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				C	----------			Sector ID
	W	----------				H	----------			information prior
	W	----------				R	----------			to Command
	W	----------				N	----------			execution. The 4
	W	----------				EOT	----------			bytes are
	W	----------				GPL	----------			commanded
	W	----------				DTL	----------			against header.
Execution										Data transfer between CPU and FDD
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command Code
	W	X	X	X	X	X	HD	US1	US0	
	W	----------				C	----------			Sector ID
	W	----------				H	----------			information prior
	W	----------				R	----------			to Command
	W	----------				N	----------			execution. The 4
	W	----------				EOT	----------			bytes are
	W	----------				GPL	----------			commanded
	W	----------				DTL	----------			against header.
Execution										Data transfer between CPU and FDD
Result	R	----------				ST 0	----------			
	R	----------				ST 1	----------			STATUS and
	R	----------				ST 2	----------			Sector ID
	R	----------				C	----------			information after
	R	----------				H	----------			Command
	R	----------				R	----------			execution
	R	----------				N	----------			

6.0 MOUSE PORT CONTROLLER

6.1 Introduction

The mouse port of the 82C710 looks like a PS/2 mouse port from a hardware standpoint. The base address for the mouse port registers are setup through the configuration register 0DH. On power up, this register comes up as 00H, which disables the mouse port. It becomes enabled only when some address is written into it.

6.2 Mouse Port Register Description

Mouse Data Port (Offset =*00H, R/W*)

Bits 7-0: Serial data bits 0-7

Mouse Status Control Port (Offset=*1H,R/W*)

This port contains both status and control bits for the mouse (pointing) device.

Bit 7: Mouse Device Enable
0 - Disables clocking for pointing device
1 - Enables clocking for pointing device
Bit 6: Pointing Device Clear
Bit 5: Pointing Device Error
Bit 4: Pointing Device Interrupt
0 - Disables pointing device interrupt
1 - Enables pointing device interrupt
Bit 3: Pointing Device Reset
0 - Normal operation mode
1 - Sets pointing device in the reset conditions (default)
Bit 2: Pointing device XMIT Idle
Bit 1: Pointing Device Character received
Bit 0: Pointing Device Idle

6.3 Mouse Software Support Specifications

In order to run a PS/2 Mouse in a PC environment, an extended BIOS system, which supports interrupt 15 function called C2, should be added in the standard BIOS. The following section describes the PS/2 mouse function C2 and its subfunctions.

6.3.1 *BIOS Data Area*

```
Bios_Data_Area  SEGMENT AT 40H
Extended_BDA    DW ?  ;OE Extended
                      BDA segment
Bios_Data_Area  ENDS
```

6.3.2 *Extended BIOS Data Area*

The extended BIOS data area contains additional variables that are used by the various BIOS functions. The location and contents of these variables must be consistent with the IBM BIOS for complete compatibility. The extended BIOS data area starts at the segment indicated by the Extended_BDA variable in the BIOS data area. This segment will usually be the highest 1K of RAM. However, BIOS routines should use the Extended_BDA variable to refer to the extended BIOS data area and not make assumptions about its location.

The following is an assembly language description of the variables with the name with which they will be referred throughout this document.

6.3.3. *Function C2 - Pointing Device Interface*

AL must be in the range 00-07 or this routine should return AH = 01 and carry set. If AL is in this range, the procedure outlined below for each of the different subfunctions should be followed.

Table 5.3.2: Extended BIOS Data Area

EX_BIOS_DATA_AREA	SEGMENT PARA		
EXBDA_SIZE	DW	?	;00 Size of Extended BDA
	DB	21H DUP(?)	;02 Reserved
;Pointing device variables			
Pointer_Driver	DD	?	;22 Pointer support routine
Pointer_Info 1	DB	?	;26 Pointer flag 0
Pointer_Info2	DB	?	;27 Pointer flag 1
Pointer_Data	DB	8 DUP(?)	;28 Reserved
	DB	0BH DUP(?)	;30 Reserved
Keyboard_Type	DB	?	;3B Keyboard type byte
BAT_Flag	DB	?	;3C BAT complete flag

6.3.4 *Subfunction 00 - Enable/disable pointer*

Entry: AL = 00 Enable/disable pointer
BH= 00 Disable
BH= 01 Enable

Exit: AH- Status returned
CF- Error status returned

If BH is not either 00 or 01, return with AH = 01 and carry set. If BH is 00 (disable), set the command in progress bit of **Pointer_Info1** and then set a pointer disable (F5) to the controller as described below.

If BH is 01 (enable), test to see if the user call is installed (bit 7 of **Pointer_Info2**). If this bit is not set, return AH = 05 with carry set (no driver installed). Otherwise, send a pointer enable (F4) to the controller using the method described below. Set the Pointing Device Interrupt Enable (bit 4) in the Mouse Status/Control Port.

6.3.5 *Subfunction 01 - Reset Pointing Device*

Entry: AL = 01 Reset pointing device

Exit: AH- Status returned
CF- Error status returned
BH- Device ID

Send a disable pointer command (F5) to the pointer using the method described below. If the command was sent to the controller without error, send an FF to the pointer (reset) using the method outlined below. If an error occurs, read two byte from the controller using the method described below.

Return AL containing the first returned (**Pointer_Data**) and BH containing the second byte (**Pointer_Data + 1**).

6.3.6 *Subfunction 02 - Set Sample Rate*

Entry: AL = 02 Set sample rate
BH- Sample rate

Exit: AH- Status returned
CF- Error status returned

If BH is greater than 06, return AH = 02 with carry set. Otherwise, set the command in progress bit of **Pointer_Info1** and then send a set sample rate (1F) command to the pointer using the method described below. If no error occurs, set the command in progress bit again and then write the reports per second value of the pointer as presented in the table below.

Sample Rate	Reports Per Second
00	0A
01	14
02	28
03	3C
04	50
05	64
06	C8

6.3.7 *Subfunction 03 - Set Resolution*

Entry: AL = 03 Set resolution
BH- Resolution value

Exit: AH- Status returned
CF- Error status returned

If the resolution value is above 03, return AH = 02 with carry set. Otherwise, set the command in progress bit of **Pointer_Info1** and then send a set resolution (E8) command to the pointer using the method described below. If no error occurs, set the command in progress bit again and then write the resolution value to the pointer.

6.3.8 *Subfunction 04 - Read Device Type*

Entry: AL = 04 Read device type

Exit: AH- Status returned
CF- Error status returned
BH- Device ID

Send an F2 to the pointer (read device type) using the method outlined below. If an error occurs, return AH = OF and carry set. If no error occurs, read the byte from the controller using the method described below.

Return BH containing the first byte returned **(Pointer_Data).**

6.3.9 *Subfunction 05 - Pointer Device Init*

Entry: AL = 05 Pointer device init
BH- Data package size

Exit: AH- Status returned
CF- Error status returned
BH- Device ID

If the package size on entry is above 8, return AH = 02 with carry set. Reset bits 0-2 in **Pointer_Info2** and replace with the package size bits (BH-1). Reset the pointer as specified above (see subfunction 01 above.)

6.3.10 *Subfunction 06 - Extended Functions*

Entry: AL = 06 Extended commands
BH= 00 Return status
BH= 01 Set scaling to 1:1
BH= 02 Set scaling to 2:1

Exit: AH- Status returned
CF- Error status returned
BL- Status byte 1 (BH= 00)
CL- Status byte 2 (BH= 00)
DL- Status byte 3 (BH= 00)

If BH is above 02 on entry, return AH = 01 with carry set. If BH = 00 on entry, return the pointer status. This is done by sending an E9 to the pointer (read ID) using the method outlined below. If an error occurs, return AH = 0F and carry set.

Read three bytes from the controller using the method outlined below. Return BH = 00, Bl = **Pointer_Data,** CL = **Pointer_Data + 1,** DH = 00, and DL = **Pointer_Data + 2.**

If BH is 01 on entry, set the scaling to 1:1. This is done by sending a set scaling to 1:1 (E6) command to the pointer using the method described below.

If BH is 02 on entry, set the scaling to 2:1. This is done by sending a set scaling to 2:1 (E7) command to the pointer using the method described below.

6.3.11 *Subfunction 07 - Device Driver FAR CALL Init*

Entry: AL- 07 Device driver FAR CALL init
ES:BX Address of routine
Exit: AH- Status returned
CF- Error status returned

Place the value in ES:BX into **Pointer_Device**. Set the pointer device installed flag (bit 7) of **Pointer_Info2** if the value in ES:BX is not zero and reset the pointer device installed flag otherwise. Return AH = 00 with carry set.

6.3.12 *Send Command to Pointer*

The following procedure is used to send a *command byte to the pointer device.* Configuration Register 0DH indicates the data port address for the pointer (This should be the standard default address for COM2). The value at this location determines the Mouse Data Port and Mouse Status/Control Port locations. Set the package size to 07 and the pointer device flat (bit 7) of **Pointer_Info2**. Reset the packet count (bit 0-2 of **Pointer_Info1**).

Set the command in progress bit and rest the ACK and Resend bits of **Pointer_Info1**. Reset the interface by setting the Mouse Enable (bit 7) and the pointing Device Reset (bit 3) of the Mouse Status/Control Port. Then, reset the Pointing Device Reset (bit 3) of the Mouse Status Control Port. Wait for the pointing device XMIT idle bit (bit 2) to become set. Once the interface is reset, and the device is idle send the command byte to the mouse by writing the data to the Mouse Data Port.

Wait for about 250 milliseconds for either the ACK or resend bits to be set in **Pointer_Info1.** If the resend bit is set or a timeout occurs, repeat the process in the paragraph above (up to three retries). If th ACK bit is set, and no data is to be returned, restore **Pointer_Info2**, reset the package count to zero and exit. If data is to be returned, do the procedure below.

6.3.13 *Get Return Data From Pointer*

After the command byte is sent to the pointer, wait until the package count **(Pointer_Info1)** is equal to the number of bytes requested. *When they are equal, restore* **Pointer_Info2,** reset the package count to zero **(Pointer_Info1)** and exit.

6.3.14 *Pointer IRQ Handler (Interrupt 73)*

Read the data byte from the Mouse Data Port. If the command in progress flag (bit 7) of **Pointer_Info1** is set, the following should be done: If the byte read was an error (FC), ACK (FA), or resend (FE), set the corresponding flag (bit 4,5,or 6) in **Pointer_Info1**, reset the command in progress flag (bit 7), clear interrupts, and then exit. If it is none of these three bytes proceed with the processing below.

Stack Offset	**Package Size**							
	1	2	3	4	5	6	7	8
0	00	00	00	00	00	00	[03]	[04]
1	00	00	00	00	00	00	Ldata	Ldata
2	00	00	Ldata	Ldata	[02]	[03]	[02]	[03]
3	00	00	00	00	Ldata	Ldata	[05]	[06]
4	00	00	[01]	[02]	[01]	[02]	[01]	[02]
5	00	00	00	00	[03]	[04]	[04]	[05]
6	Ldata	[00]	[00]	[00]	[00]	[00]	[00]	[00]
7	00	Ldata	00	[01]	00	[01]	00	[01]

If the current package size (bits 0-2 of **Pointer_Info2**) is not equal to the package count (bits 0-2 of **Pointer_Info1**), place the byte read into the extended BIOS data area of (OFFSET *Pointer Data* + ***Pointer_Info1*** *and* 7). This is the current index for the data read. Increment **Pointer_Info1**, clear interrupts and exit.

If the package count is equal to the package size, reset the package count to zero and then do the following: Create a stack frame of eight bytes which will contain the information from the table below (based on the package size). Note that in the table below that L Data is the last data byte read from the pointer. [nn] indicates that the n'th byte of the data package (at **Pointer_Data**) stored in the extended BIOS data area. 00 indicates zero should be stored.

After the stack frame is created, perform a long call to the user's interrupt routine at **Pointer_Device.** On return, remove the stack frame data, clear interrupts, and exit.

6.4 Mouse Connector

The PS/2 Mouse connector uses a 6-pin miniature DIN connector. Figure 6.1 shows the connector and figure 6-2 shows the voltages and signals assigned to the PS/2 Mouse connector pins.

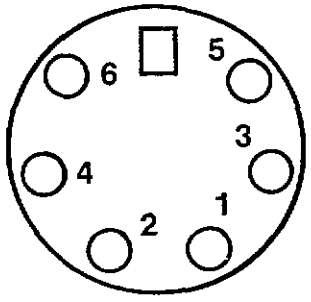


Figure 6.1. The PS/2 Mouse Connector

Pin	I/O	Signal Name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5 Vdc
5	I/O	Clock
6	NA	Reserved

Figure 6.2 Signal Assessment

7.0 THE 82C710 CONFIGURATION

7.1 Introduction

A significant portion of the 82C710 circuitry is used for configuration, all of which can be performed under software control. This permits user-friendly (probably menu-driven) UPC configuration using setup utilities provided with the card or system containing the UPC. DIP switches and jumpers can thus be eliminated meaning that it should no longer be necessary to open the chassis to change the configuration of a peripheral.

Since the UPC is software configured, a setup program must be run any time configuration is changed. This process entails placing the UPC in configuration mode and setting the on-chip configuration registers.

7.2 Configuration Sequence

In order to setup or change the configuration of the UPC, two consecutive I/O addresses (one even and one odd; these should not conflict with any existing devices) are used to select and access the internal configuration registers. The configuration sequence is intentionally complicated to prevent accidental changes to the UPC configuration by an errant program. Any deviation from the sequence described below will cause the configuration state machine to return to its initial idle state.

By IBM PC convention, I/O addresses 3F8-3FFH and 28F-2FFH are reserved for COM1 and COM2 respectively. The Interrupt Flag Register (IFR), located by default at 2FAH or 3FAH in each UPC, is normally read only. Writes to these locations are tolerated by the UPC, and they should present no problem for resident NS16450 or INS8250A UART's. Note that there are special considerations when using more than one UPC in a single system.

The configuration sequence is divided into three steps:

1) Entering the configuration mode
2) Configuring the 82C710
3) Escaping the configuration mode

The description of each step with examples is as follows:

7.2.1 *Enter configuration mode*

Before doing this step, you must select two consecutive port addresses (CRI and CAP) which will be used to access and write data to the configuration registers. CRI (Configuration Register Index) is located in the EVEN and LOWER address and is used to access the configuration register. CAP (Configuration Access Port) is the CRI address plus 1 (ODD and UPPER) and is used to write data to the selected register. Make sure your selected address does not conflict with other adapter's I/O address.

Assuming 390H is selected for CRI, the following sequence is used to get into the configuration mode

—I/O write 55H to 2FAH port address
—I/O write AAH to 3FAH port address (AAH is the complement of 55H)
—I/O write 36H to 3FAH port address
—I/O write E4H to 3FAH port address. (E4H is 390H divided by 4)
—I/O write 1BH to 2FAH port address (1BH is the complement of E4H)

In configuration mode, ready to be configured

Note that any deviation from the above sequence will cause the configuration state machine to return to its initial idle state.

7.2.2 *Configuring the 82C710*

To access and write data to any of the configuration registers, two I/O writes are needed:

—I/O write <Pointer> to CRI where
Pointer = bit 3-0: is the pointer to the configuration register. 0 value is to access register 0, 1 to access register 1 and so on. Bits 7-4 should be set to 0.

—I/O write <data>to CAP where
<data> = data needed to write into accessed register.

Examples:

To access register 0 to turn on the oscillator and enable all ports:
—I/O write 00H to 390H (Point to register 0H)
—I/O write 0FH to 391H (set necessary bits)

To access register 4 to set the serial port address to 2F8H:
—I/O write 04H to 390H
—I/O write 7EH to 391H (7EH is 2F8H div. 4)

7.2.3 *Escaping configuration mode*

To escape configuration mode, write any value into the configuration register 15 (FH)
—I/O write 0FH to 390H
—I/O write BBH to 391H (write any value)

7.2.4 *Configuration example*

The below sample configuration program is written in the 8086 assemply language.

```
************************************************
      Entering the configuration mode
************************************************

MOV   DX,02FAH ;Write 55H to I/O 2FAH
MOV   AL,55H
OUT   DX,AL

MOV   DX,3FAH  ;Write AAH to I/O 2FAH
MOV   AL,0AAH
OUT   DX,AL

MOV   AL,36H   ;Write 36H to I/O 3FAH
OUT   DX,AL

MOV   AL,0E4H  ;Write E4H to I/O 3FAH
OUT   DX,AL    ;Set CRI to 390H

MOV   DX,2FAH  ;Write 1BH to I/O 2FAH
MOV   AL,36H   ;
OUT   DX,AL

************************************************
      Configuring the 82C710
************************************************

MOV   DX,390H  ;Set DX to CRI
MOV   AL,0CH   ;point to register 0CH
OUT   DX,AL

INC   DX       ;Set DX to CAP
IN    AL,DX    ;Get current value
OR    AL,80H   ;Enable IDE
AND   AL,0BFH  ;Select AT interface
AND   AL,0FEH  ;Set mouse port in normal
OUT   DX,AL

DEC   DX       ;Set DX to CRI
MOV   AL,0DH   ;Point to 0D register
OUT   DX,AL

INC   DX       ;Set DX to CAP
MOV   AL,0C4H  ;Set mouse address=310H
OUT   DX,AL    ;0C4H = 310 div by 4

************************************************
      Escaping the configuration mode
************************************************

MOV   DX,390H  ;Set DX to CRI
MOV   DX,0FH   ;Point to register FH
OUT   DX,AL

INC   DX       ;Set DX to CAP
OUT   DX,AL    ;any data
```

7.3 Configuration Register Description

There are 16 configuration registers in the 82C710 which must be initialized. Settings are retained as long as standby power is maintained.

These registers are not affected by the RESET signal and are set to their default state only upon power up. Table 7-1 depicts the configuration registers in the 82C710 with the default values upon power up. The definitions for each of the bits in the 82C710 configuration registers are shown below.

Configuration Register 00H (R/W)

This read/write register is located at CRI offset 00H. Bit definitions are as follows:

Bit 7: Valid Configuration. This bit indicates that a valid configuration cycle has taken place. The configuration software should set this bit to 1 after it has initialized the required configuration registers.

Value	Function
0	Invalid Configuration. Indicates that power has been applied to the UPC but the configuration registers have not yet been fully initialized. A reset from the RESET pin has no effect on this bit.
1	Valid Configuration. Indicates that the configuration software has initialized all necessary configuration registers since the last time power was applied to the UPC.

Bits 6-5: Serial Port and Floppy Oscillator Enable.

Value		Function
b6	b5	
0	0	Oscillator always ON, default
0	1	Oscillator is ON when PWRGD is active, otherwise it is OFF (tri-state)
1	0	Oscillator is ON when PWRGD is active, otherwise it is OFF (tri-state)
1	1	Oscillator always OFF

Value	Description
0	Oscillator ON, BR Generator Clock ENABLED. In this state the oscillator and Baud Rate Generator Clock are always enabled and are not shut off due to removal of the main power supply (PWRGD pin becoming active). The presence of a power supply other than a (low capacity) battery is assumed. This is due to the fact that serial port operation (in particular the oscillator) consumes more power than many of the other 82C710 circuits.
1	Oscillator ON, BR Generator Clock ENABLED. In this state, the oscillator and BR Generator Clock are ON and ENABLED respectively as long as the PWRGD pin is inactive. When PWRGD becomes active, these two are shut down.
2	Oscillator ON, BR Generator Clock DISABLED. In this state the oscillator is ON as long as the PWRGD pin is inactive. When PWRGD becomes active, the oscillator is shut off. The BR Generator Clock is always disabled.
3	Oscillator OFF, BR Generator Clock DISABLED.

Bit 4: Reserved (read only)

Bit 3: Enable Parallel Port; Read/Write. A 1 in this bit enables the Parallel Port. The default is enabled upon power up.

Bit 2: Enable UART; Read/Write. A 1 in this bit enables UART. The default is enabled upon power up.

Bits 1,0: Reserved (read/write).

Configuration Register 01H (R/W)

This read/write register is located at CRI offset 01H. Bit definitions are as follows:

Bit 7: Reset Control. This bit determines the manner in which the RESET pin affects the serial port. Default is normal RESET.

Value	Function
0	Normal RESET. The UPC RESET input will cause a reset of all registers in the serial port excluding the Receive Buffer, Transmit Buffer and Divisor Registers.
1	Restricted RESET. The RESET input will not reset the serial port. This is used in applications where the UPC remains powered from an external supply while power to the remainder of the system is shut off. When the system power is restored, (most likely due to an interrupt when a character is received) it is desirable to have the state of the serial port remain unchanged.

Value	Function
0	Normal, for printer only. In this mode, the data read from the Parallel Data Latch register is identical to that which was last written.

1 Bi-directional. In this mode, write data to Parallel Data Latch register will latch the data and be sent to the parallel connector when the DIR bit (bit 5 of Parallel Control Register) is set to Write direction. The DIR bit should be set to Read direction in order to read the connector data. Otherwise the latched data is read.

Bit 5: Force UART $\overline{CTS}$ active. A 1 in this bit forces the UPC internal $\overline{CTS}$ signal low. Default is not forced and the output is dependent on the programmed Modem Control Register valve.

Bit 4: Force UART $\overline{DSR}$ active. A 1 in this bit forces the UPC internal $\overline{DSR}$ signal low. Default is not forced and the output is dependent on the programmed Modem Control Register valve.

Bit 3: Force UART $\overline{DCD}$ active. A 1 in this bit forces the UPC internal $\overline{DCD}$ signal low. Default is not forced and the output is dependent on the programmed Modem Control Register valve.

Bits 2-0: Reserved (read only).

Configuration Register 02H (R/W)

This read/write register is located at CRI offset 02H. Bit definitions are as follows:

Bit 7: Reserved = 0 (read/write).

Bit 6: UART Divider. Divide UART clock by 2 or 4.

Value	Function
0	Divide by 2 (default)
1	Divide by 4

Bit 5: UART RX Clock Select.

Value	Function
0	Use baud rate generator output (default)
1	Use divider output (see bit 6)

Bit 4: UART TX Clock Select.

Value	Function
0	Use baud rate generator output (default)
1	Use divider output (see bit 6)

Bit 3: Reserved (default = 1, readable as 1 only)

Bits 2-0: Reserved (default = 0, readable as 0 only)

Configuration Register 03H
Reserved

Configuration Register 04H (R/W)
(UART base address)

This read/write register holds the base address of the UART . It is located at CRI offset 04H. The high order seven bits in this one byte register are compared with SAD<09:03> when the UPC is in normal operating mode to determine if the UART is being addressed. Nominal settings are 2F8H (COM2) or 3F8H (COM1). Default upon power up in FEH: address 3F8H (COM1).

Bits 7-1: The MSB of the Primary Serial Port Address (bits 9-3)

Bit 0: Reserved = 0 (If read will be zero)

Configuration Register 06H (R/W)
(Parallel base address)

This read/write register holds the base address of the parallel port. It is located at CRI offset 06H. The eight bits in it are compared with SAD<09:02> when the UPC is in normal operating mode to determine if the Parallel Port is being addressed. Nominal settings are 278H (LPTC) or 378H (LPTB). Default is 278H. (LPTA is assumed to be on the monochrome adapter).

Configuration Register 07H
Reserved

Configuration Register 08H
Reserved

Configuration Register 09H (R/W)
(General Purpose Chip Select address)

This read/write register is located at CRI offset 09H. Bit definitions are as follows:

Bits 7-0: A9-A2 Address Decode

Configuration Register 0AH (R/W)

This read/write register is located at CRI offset 0AH. Bit definitions are as follows

Bits 7-5: $\overline{\text{GPCS}}$ mask for address bit 3 to bit 1.

Value	Function
0	No mask
1	Mask (not used in decoding)

Bit 4: Reserved.

Bit 3: $\overline{\text{GPCS}}$ A1 address decode

Bit 2: $\overline{\text{IDEENLO}}$ Buffer Enable

Value	Function
0	Disabled (default)
1	Enabled. $\overline{\text{IDEENLO}}$ qualifies BDIR

Bit 1: $\overline{\text{GPCS}}$ Enable.

Value	Function
0	Disabled (default).
1	Enable $\overline{\text{GPCS}}$ output.

Bit 0: $\overline{\text{GPCS}}$ Buffer Enable.

Value	Function
0	Disabled (default).
1	Enabled. $\overline{\text{GPCS}}$ qualifies BDIR.

Configuration Register 0BH (R/W)

This read/write register is located at CRI offset 0BH. Bit definitions are as follows:

Bit 7: Mouse Interrupt Polarity Select (MINTR).

Value	Function
0	Active high (default)
1	Active low. Tri-stated when inactive.

Bit 6: Floppy Interrupt Polarity Select (FINTR).

Value	Function
0	Active high (default)
1	Active low. Tri-stated when inactive.

Bit 5: Serial Interrupt Polarity Select (SINTR).

Value	Function
0	Active high (default).
1	Active low. Tri-stated when inactive.

Bit 4: Parallel Interrupt Polarity Select (PINTR)

Value	Function
0	Active high (default)
1	Active low. Tri-stated when inactive.

Bit 3: Serial Port Power Down.

Value	Function
0	Normal Mode (default).
1	Power Down Mode.

Bit 2: Reserved.

Bit 1: Parallel Port Power Down

Value	Function
0	Normal Mode (default)
1	Power Down Mode. All outputs (PD0-7, STROBE, SLCTIN, INT, AUTOFD) are tri-stated. All inputs (ACK,BUSY,PE,SLCT,ERROR) are disabled.

Bit 0: GPCS/OUT1 Pin Function Select.

Value	Function
0	GPCS is selected as output pin. (default)
1	OUT1 of UART (MCR) is selected as output pin.

Configuration Register 0CH (R/W)

This read/write register is located at CRI offset 0CH. Bit definitions are as follows:

Bit 7: IDE Enable.

Value	Function
0	IDE disabled. HDCS0, HDCS1, IDEENLO, IDEENHI are always high.
1	IDE Enabled (default). HDCS0, HDCS1, IDEENLO, IDEENHI are active.

Bit 6: IDE AT/XT Select.

Value	Function
0	IDE AT interface (default) 8/16 bit programmed I/O transfers. IDEENLO is active during I/O 3F6H, 3F7H, 1F0H-1F7H. IDEENHI is active during programmed I/O 1F0H-1F7H and HDCS1 is active during PIO 3F0H-3F7H.
1	IDE XT interface. 8 bit DMA and PIO transfers. IDEENLO is active during PIO 320H-323H or DMA (HDACK active). HDCS0 is active only during programmed I/O (PIO) 320H-323H.

Bit 5: FDC Enable

Value	Function
0	FDC Disabled

Note: The FDC must also be powered down.

1	FDC Enabled (default) Floppy chip select is active for I/O address 3F0H-3F7H.

Bit 4: FDC Power Down

Value	Function
0	Normal Mode (default)
1	Power Down Mode. All outputs are tri-stated. All inputs are disabled. All FDC Write registers are accessible. Read only registers produce undetermined value when read.

Bit 3: RTCCS Enable

Value	Function
0	RTCCS Disabled (default)
1	RTCCS Enabled. RTCCS is active for I/O 70H and 71H.

Bit 2: RTCCS Buffer Enable

Value	Function
0	RTCCS Buffer Disabled (default)
1	RTCCS Enabled. RTCCS qualifies DBIR.

Bit 1: Reserved (Read/Write).

Bit 0: Mouse Port Power Down.

Value	Function
0	Normal Mode (default)
1	Power Down Mode

Configuration Register 0DH (R/W)

This register contains the base address of Mouse port

b7-b0: The 8 most significant bits of the mouse port. Default on power up is 00H which implies the mouse port is disabled. When an address is written into this register, the mouse port is enabled.

Configuration Register 0EH (R/W)

This read/write register is located at CRI offset 0EH. Bit definitions are as follows:

Bit 7: Reserved.

Bit 6: Serial Port Test enabled.

Value	Function
0	Normal mode. Test disabled (default)
1	Test enabled. TXD outputs the Rx clock.

Bit 5: Reserved. (readable as 0).

Bits 4-3: Floppy Test Enable.

Value b4	Value b3	Function
0	0	Normal mode. Test disabled
0	1	The Data Separator signals can be observed on the output pins: $\overline{WGATE}$ = PUMPDN (Pump Down) HDSE = PUMPUP (Pump Up) $\overline{DIR}$ = RDD $\overline{STEP}$ = RDW
1	0	The parallel port input pads are used as inputs to the floppy as shown below. The floppy output pads are used to observed the internal signals. $\overline{INPUTS}$: $\overline{BUSY}$ = WCLK765 $\overline{ACK}$ = RDD765 PE = CLK765 SLCT = RDW765 $\overline{OUTPUTS}$: $\overline{MTR0}$ = MFM $\overline{MTR1}$ = VCOSYNC (VCO from 765) DRV0 = RWSEEK DRV1 = WDA765
1	1	The Floppy inputs pads are used to force data separator signals and observe results on the outputs. $\overline{INPUTS}$: $\overline{WRPRT}$ = PDOWN INDEX = PUP DSKCHG = VCOSYNC (To charge Pump RDGATE) $\overline{OUTPUTS}$: $\overline{WGATE}$ = PUMPDN HDSEL = PUMPUP DIR = RDD STEP = RDW

Bit 1,0: Reserved (readable as 0).

Configuration Register 0FH (R)

This register contains the Configuration Register Index address divided by 4.

Configuration Register 0FH (W)

Writing any value into this register will bring the 82C710 out of configuration mode.

Table 7-1. The 82C710 Bit Definition Summary with Default Values

Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
00H	Valid C	OSC. Enable		R	P. En	S. En	RESERVED		0CH
01H	Reset	Pr/Bi	F-CTS	F-DSR	F-DCD	RESERVED			00H
02H	R	S. Clk	Rx Src	Tx Src.	RESERVED				0XH
03H	RESERVED								XXH
04H	UART Port Address Div. by 4							N/A	FEH
05H	RESERVED								XXH
06H	Parallel Port Address Div. by 4								9EH
07H	RESERVED								XXH
08H	RESERVED								XXH
09H	General Port Chip Select (Bit 9-2) $\overline{GPCS}$								B0H
0AH	$\overline{GPCS}$ Mask			R	$\overline{GPCS}$A1	IDEBEN	$\overline{GPCS}$EN	$\overline{GPCS}$BEN	00H
0BH	MINTRP	FINTRP	SINTRP	PINTRP	SPDWN	R	PPDWN	$\overline{GPCS}$/OUT	00H
0CH	IDEEN	IDEAT/XT	FDCEN	FPDWN	RTCCSEN	RTCBEN	R	MDDWN	A0H
0DH	Mouse Port Base Address (Bit 7-0)								00H
0EH	R	STEn	R	FTEn1	FTEn2	DSTEn	0	0	00H
0FH	Configuration Index Div. 4								XXH

8.0 82C710 POWER MANAGEMENT

8.1 Introduction

Power management functions are achieved using PWRGD pin (hardware) and Configuration Register bits (software). The 82C710 configurations and register data can be retained during sleep mode with minimum current drain. This makes the 82C710 ideal for laptop environments. Each port of the 82C710 can also be disabled or powered down through configuration registers. This feature enhances the 82C710's flexibility in system integration. The section below discusses the power management of the 82C710.

8.2 Power Management Application

There are three typical operating modes for any system.

1) Active mode
2) Sleep mode
3) Power Down mode

Active mode:

In this mode, the 82C710 will be powered by a power supply (through AC outlet) or in a laptop by a main battery (NiCd). The configuration registers will be initialized by the System BIOS. In Active mode, software (BIOS) can power off selected resources when needed to reduce total power consumption.

Sleep mode:

In a Laptop application, the power source is the main battery which can last from 4-12 hours. To save battery energy, the system should be put in sleep mode which draws a minimum current when it is not used. The 82C710 supports this sleep mode feature through PWRGD pin and bits 6 and 5 of configuration register 0H (CR#0H<6,5>). Below is a detailed description of these bit functions.

b6,b5	Serial Port & Floppy Oscillator Enable.
0 0	Oscillator always ON regardless of PWRGD, default.
0 1	Oscillator is ON when PWRGD is high, otherwise it is OFF (tri-state).
1 0	Oscillator is ON when PWRGD is high, otherwise it is OFF (tri-state).
1 1	Oscillator is always OFF

To implement the sleep mode, the CR#0H<6,5> should be programmed as 0,1 or 1,0. This turns off the oscillator and minimizes the current drawn by the serial and floppy ports. The PWRGD signal is controlled by user designed sleep mode circuitry. When the system is put in the sleep mode, the sleep mode circuitry will assert PWRGD. The 82C710 isolates itself from the rest of the system; all outputs are tri-stated, all inputs are disabled and all commands are ignored until the PWRGD is restored to the active state (wake up). This is why CRD is set to 0,1 or 1,0.

Power Down mode

In this mode, the power is completely removed from the system. The programmed configuration register data will not be retained. This should not be the issue since the configuration registers will be restored by the system BIOS.

Note: In any mode, the 82C710 should not be powered by the RTC backup battery (Lithium).

8.3 Enabled and Power Down Register Values

This section summarizes the Enabled/Disabled and Power Up/Down bits for each port.

Serial Port

CR#00H<2> = 0	Enabled (default)
CR#00H<2> = 1	Disabled

CR#0BH<3> = 0	Power Up (default)
CR#0BH<3> = 1	Power Down.

Parallel Port

CR#00H<3> = 0	Enabled (default)
CR#00H<3> = 1	Disabled

CR#0BH<1> = 0 Power Up (default)
CR#0BH<1> = 1 Power Down.

Floppy Port

CR#0CH<5> = 0 Disabled
CR#0CH<5> = 1 Enabled (default)

CR#0CH<4> = 0 Power Up (default)
CR#0CH<4> = 1 Power Down.

Note: In order to completely disable the FDC portion (for an external floppy drive), the FDC needs to be disabled and powered down at the same time.

IDE port

CR#0CH<7> = 0 Disabled
CR#0CH<7> = 1 Enabled (default)

RTCCS (Real Time Clock Chip Select)

CR#0CH<3> = 0 Disabled (default)
CR#0CH<3> = 1 Enabled

GPCS (General Purpose Chip Select)

CR#0AH<1> = 0 Disabled
CR#0AH<1> = 1 Enabled (default)

9.0 REAL TIME CLOCK CHIP SELECT ($\overline{RTCCS}$) AND GENERAL PURPOSE CHIP SELECT ($\overline{GPCS}$)

9.1 Introduction

The 82C710 provides the Real Time Clock Chip Select ($\overline{RTCCS}$) which is decoded at I/O addresses 70H and 71H and the General Purpose Chip Select ($\overline{GPCS}$) whose address is programmable. The following section describes the application of these two signals.

9.2 The 82C710 RTC Application

The typical Real Time Clock circuit is shown in Figure 10.2.

9.3 The 82C710 With Second Serial Port

The 82C710 provides only one serial port. For applications which require two serial ports, the 82C710 General Purpose Chip Select is used to implement this application with minimum additional logic. Since the $\overline{GPCS}$ address is programmable via the 82C710 configuration registers, the second serial port address can be put in any location. Typical second serial port circuitry is shown in figure 10.2.

Note that the $\overline{GPCS}$ signal can also be used to implement the Game Port Application as shown in figure 10.3.

10.0 PC/AT DESIGN APPLICATION

10.1 Introduction

This section describes the 82C710 in a PC/AT Motherboard application. With the 82C710, the complete serial port, parallel port, floppy disk port, IDE interface and PS/2 Mouse port can be embedded in the motherboard with minimal board space and some cost saving. Figure 10.1 shows a typical motherboard application of the 82C710.

10.2 I/O Address Map for the PC/AT

Serial Port

Below is a table of standard PC/AT serial port addresses and the corresponding interrupts.

Physical Address	Interrupt	Logical Name
3F8H	IRQ4	COM1
2F8H	IRQ3	COM2
338H/3E8H 2E8H/220H	IRQ4	COM3
238H/2E8H 2E0H/228H	IRQ3	COM4

Note that the logical name has no bearing on the address assignment. For instance, COM1 logical name is assigned to the first serial port found by the ROM BIOS, regardless of the IRQ and address assignment. However, the address is paired with the assigned interrupt. Also, there is a sequence of the addresses the BIOS will search for.

By default, the 82C710 serial port is set at the 3F8H address, and the interrupt should be hard wired to the IRQ4.

Parallel Port

Physical Address	Interrupt	Logical Name
3BCH	IRQ5	LPTA
378H	IRQ7	LPTB
278H	IRQ5	LPTC

Note that the logical name has no bearing on the address assignment. For instance, LPT3 logical name is assigned to the first serial port found by the ROM BIOS, regardless of the IRQ and address assignment. However, the address is paired with the assigned interrupt. Also, there is a sequence of the addresses the BIOS will search for.

The IBM PC/AT allows installation of up to 3 parallel ports. These ports have logical names: LPT1, LPT2, LPT3. The printer port on the Monochrome/Printer Adaptor, which is addressed at 3BCH, will be LPT1 when it is installed, then the LPTC (278H) on 82C710 (if configured) will be LPT2.

By default, the 82C710 serial port is set at 278H address, and the interrupt should be hard wired to the IRQ3.

Floppy Disk Controller

The 82C710 integrates an entire PC/AT floppy controller design. The I/O address is mapped into 3F0H-3F7H; there is no need for an external address decoder. The 82C710 is connected directly to the floppy disk interface because of the on-chip 48 mA output buffer.

The open collector outputs from the floppy disk interface should be terminated at the 82C710 with a 150 ohm resistor. The external 250/300/500 Kb/s PLL filter is connected to the 82C710 via FILTER, FGND250, FGND500 and AGND pins. This filter configuration allows the 82C710 to operate at different data rates. The floppy interrupt is connected to IRQ6 as PC/AT standard. Below is the table of I/O address maps and drive/media formats.

I/O Address Map for Floppy

I/O Address	Access Type	Description
3F0H	----	Unused
3F1H	----	Unused
3F2H	Write	Digital Output Register
3F3H	----	Unused
3F4H	Read	Main Status Reg.
3F5H	R/W	Data Register
3F6H	----	Unused
3F7H	Write	Data Rate Select Reg.
3F7H	Read	Digital Input Register

The description of these registers can be found in the Floppy Section.

Drive and Media for PC/AT

Drive Speed (RPM)	Capacity (Kbyte)	Data Rate (Kbps)	Sector	Cyl.
300	360	250	9	40
360*	360	300	9	40
360	1.2Mbyte	500	15	80

*When a 360Kbyte diskette is in the 1.2 Mbyte drive.

IDE Interface

The 82C710 integrates the complete IDE interface into a single chip. The 82C710 IDE signals connect directly to the IDE connector. Two transceivers whose direction signals are controlled by $\overline{\text{IDEENLO}}$ and $\overline{\text{IDEENHI}}$ are required for the low byte and the high byte data.

PC/AT Task File Registers

I/O Address	Type Access	Description
1F0H	R/W	Data Register
1F1H	R	Error Register
	W	Write Precomp.
1F2H	R/W	Sector Count
1F3H	R/W	Sector Number
1F4H	R/W	Cylinder Low
1F5H	R/W	Cylinder High
1F6H	R/W	Drive/Head
1F7H	R	Status Register
	W	Command Reg.

PC/AT Alternate Registers

I/O Address	Type Access	Description
3F6H	W	Fixed Disk
3F7H	R	Digital Input

The description of these registers can be found in the IDE interface section.

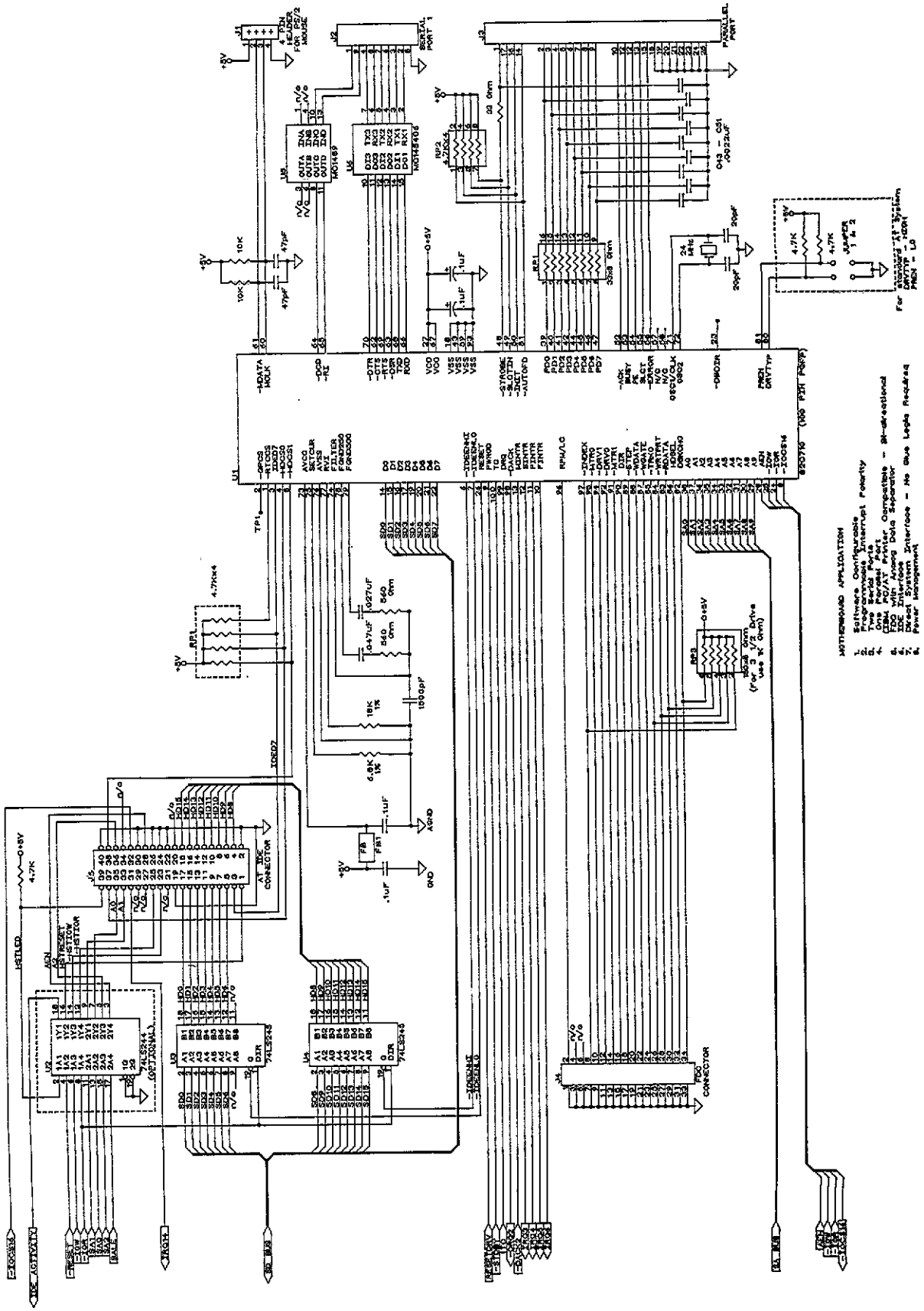


Figure 10.1 82C710 Motherboard Application

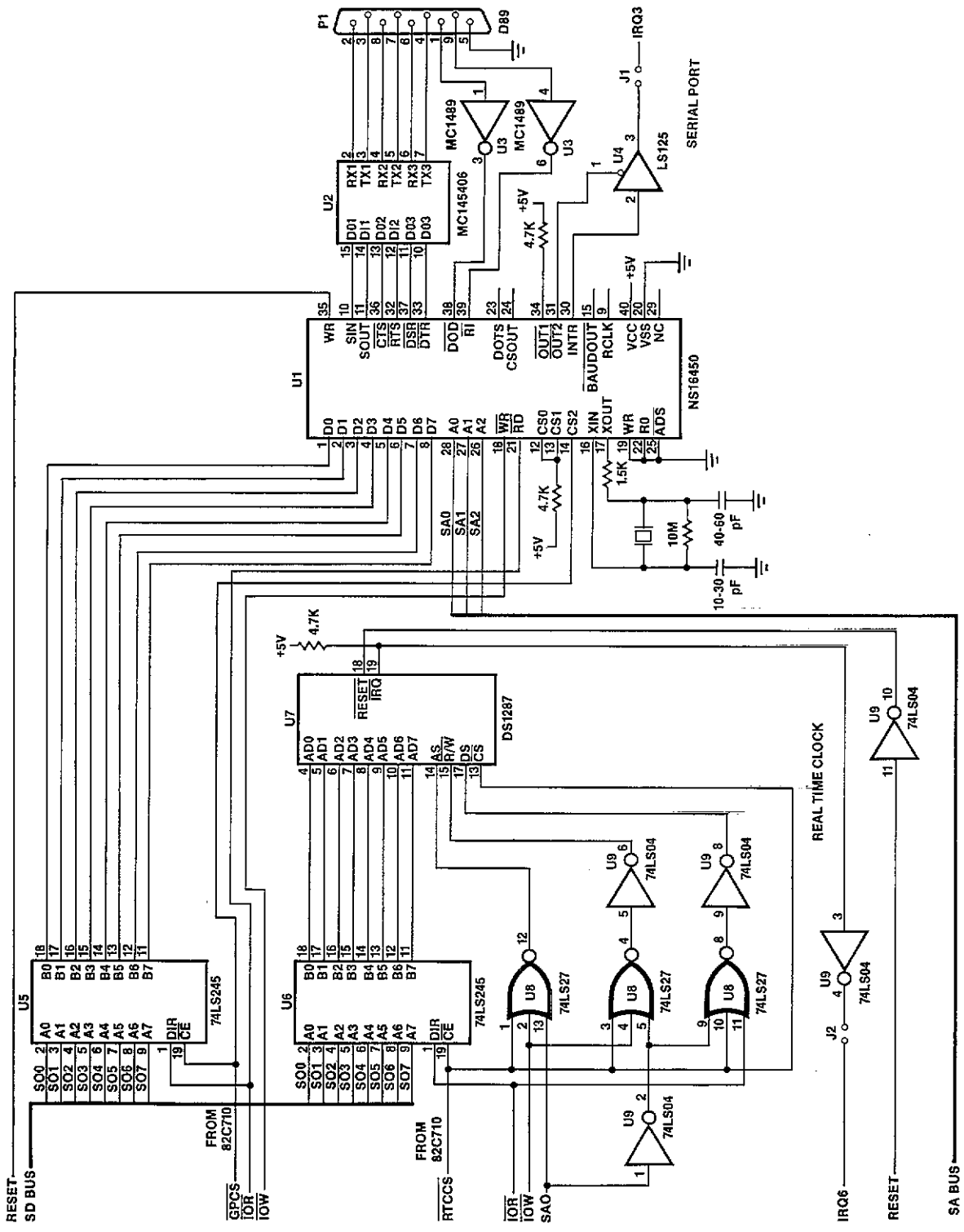


Figure 10.2 $\overline{\text{RTCSS}}$ & $\overline{\text{GPCS}}$ Application

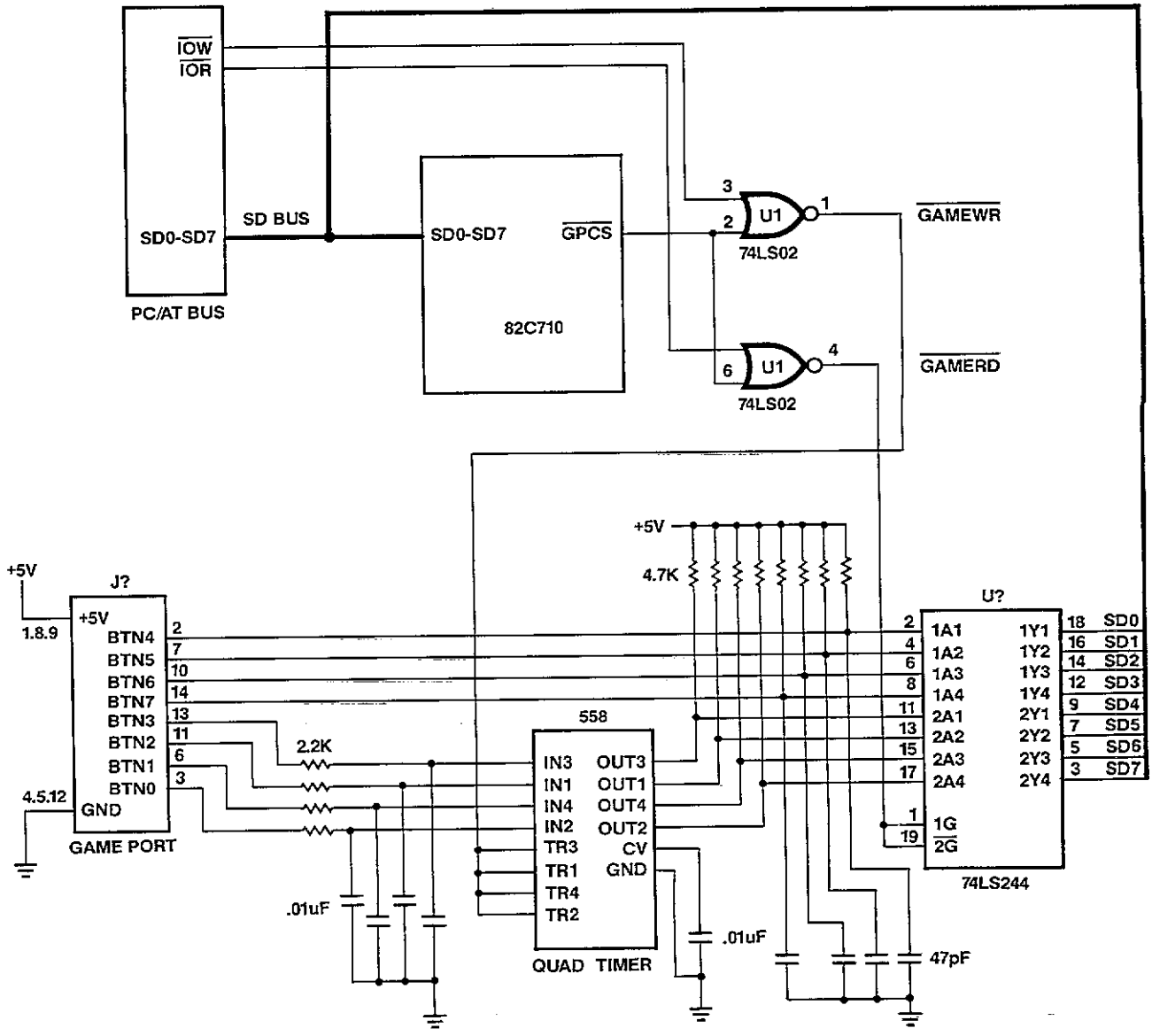


Figure 10.3 82C710 Game Port Application

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0		7.0	Volts
VI	Input Voltage	-0.5		5.5	Volts
TA	Operating Temperature	0		70	°C
Tstg	Storage Temperature	-40		125	°C

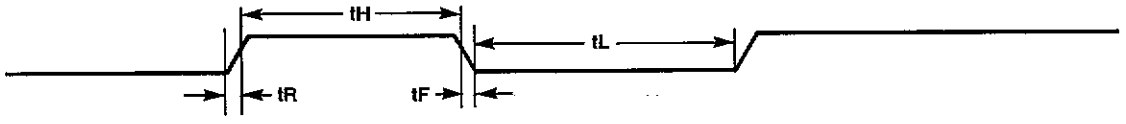
DC Characteristics Vcc = 5.0 ± 0.5V, Temp = 0°C to 70°C (Operating)

Type	Symbol	Min	Typ	Max	Units	Test Condition
	V_{CC}	4.5	5.0	5.5	V	
O	I_{OL}			4.0	mA	$V_{OL\ MAX}$ = 0.4V
	I_{OH}			-1.0	mA	$V_{OL\ MIN}$ = 2.4V
OH	I_{OL}			24	mA	$V_{OL\ MAX}$ = 0.5V
	I_{OH}			-12	mA	$V_{OL\ MIN}$ = 2.4V
OB	I_{OL}			24	mA	$V_{OL\ MAX}$ = 0.5V
	I_{OH}			-10	mA	$V_{OL\ MIN}$ = 2.4V
OC	I_{OL}			24	mA	$V_{OL\ MAX}$ = 0.5V
	I_{OH}			-50	μA	$V_{OL\ MIN}$ = 2.4V
OD	I_{OL}			48	mA	$V_{OL\ MAX}$ = 0.5V
	I_{OH}			-10	μA	$V_{OL\ MIN}$ = 2.4V
OL	I_{OL}			8	mA	$V_{OL\ MAX}$ = 0.5V
	I_{OH}			-10	μA	$V_{OL\ MIN}$ = 2.4V
I	I_{IL}			-0.2	mA	$V_{CC\ MAX}$, V_{IL} = 0.4V
	I_{IH}			20	μA	$V_{CC\ MAX}$, V_{IH} = 2.7V
	V_{IL}			0.8	V	
	V_{IH}	2.0			V	
ICLK	I_{IL}			-0.2	mA	$V_{CC\ MAX}$, V_{IL} = 0.4V
	I_{IH}			20	μA	$V_{CC\ MAX}$, V_{IH} = 2.7V
	V_{IL}			0.4	V	
	V_{IH}	3.0			V	
IS	I_{IL}			-0.2	mA	$V_{CC\ MAX}$, V_{IL} = 0.4V
	I_{IH}			20	μA	$V_{CC\ MAX}$, V_{IH} = 2.7V
	V_{IL}			0.8	V	
	V_{IH}	2.2			V	
	hys		250		mV	
I_{STBY}				250	μA	
T	I_{OL}			24	mA	$V_{OL\ MAX}$ = 0.4V
	I_{OH}			-12	mA	$V_{OL\ MIN}$ = 2.4V
I_{CC}			10	40	mA	

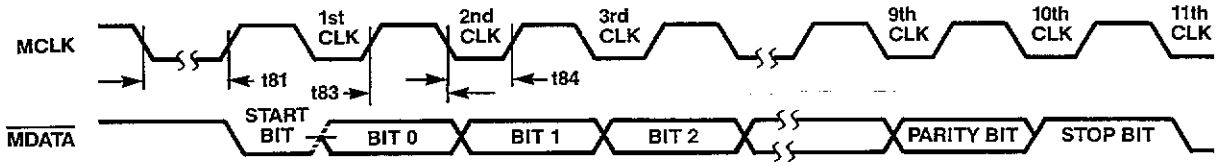
AC ELECTRICAL CHARACTERISTICS

Symbol	Description	Min	Max	Units
Host Interface Timing				
t1	RESET width	500		ns
t2	$\overline{IOR}$, $\overline{IOW}$ width	150		ns
t3	AEN,$\overline{IOCS16}$ setup time to $\overline{IOR}$,$\overline{IOW}$	40		ns
t4	AEN,$\overline{IOCS16}$ hold time from $\overline{IOR}$,$\overline{IOW}$	10		ns
t5	Address bus setup time to $\overline{IOR}$,$\overline{IOW}$	40		ns
t26	Address bus hold time from $\overline{IOR}$,$\overline{IOW}$	10		ns
t27	Data setup time to $\overline{IOW}$	40		ns
t6	Data hold time from $\overline{IOW}$	10		ns
t7	Data bus delay from $\overline{IOR}$		100	ns
t8	Data bus hold time from $\overline{IOR}$	10	60	ns
t9	DBDIR active delay from $\overline{IOR}$,$\overline{IOW}$		40	ns
t10	DBDIR inactive delay from $\overline{IOR}$,$\overline{IOW}$		80	ns
t11	$\overline{CS}$ delay from AEN, Address bus		40	ns
Parallel Port Timing				
t12	PD0-PD7,$\overline{INT}$,$\overline{STROBE}$,$\overline{AUTOFD}$,$\overline{SLCTIN}$ delay from Data bus		100	ns
t13	INTR delay from $\overline{ACK}$		60	ns
IDE Interface Timing				
t14	$\overline{IDEENLO}$,$\overline{IDEENHI}$ delay from AEN,$\overline{IOCS16}$		40	ns
t15	$\overline{IDEENLO}$,$\overline{IDEENHI}$ delay from address bus		40	ns
t16	IDED7 to DATA bus bit 7 delay (READ cycle)		60	ns
t17	DATA bus bit 7 to IDED7 delay		50	ns
DMA Interface Timing				
t18	$\overline{DACK}$ setup time to $\overline{IOR}$,$\overline{IOW}$	40		ns
t19	$\overline{DACK}$ hold time from $\overline{IOR}$,$\overline{IOW}$	40		ns
t20	$\overline{DACK}$ to $\overline{IDEENLO}$,$\overline{IDEENHI}$ delay		40	ns
t21	AEN,$\overline{IOCS16}$ to $\overline{IDEENLO}$,$\overline{IDEENHI}$ delay		40	ns
Serial Port Timing				
t28	$\overline{IOW}$ to $\overline{RTS}$,$\overline{DTR}$,$\overline{OUT1}$ delay		200	ns
t22	$\overline{IOW}$ to SINTR tri-state delay	10	100	ns
t23	SINTR active delay from $\overline{CTS}$,$\overline{DSR}$,$\overline{DCD}$		100	ns
t24	SINTR inactive delay from $\overline{IOR}$ (leading edge)		120	ns
t25	SINTR inactive delay from $\overline{IOW}$ (trailing edge)		125	ns
Mouse Transmit				
t81	Time for MCLK line to be inactive while CPU is preparing to send data	110	115	ns
t83	Duration of MCLK active	30	50	ns
t84	Duration of MCLK inactive	30	50	ns
Mouse Receive				
t86	Duration of MCLK inactive	30	50	ns
t87	Duration of MCLK active	30	50	ns
t89	Time from DATA transition to falling edge MCLK	5	25	ns

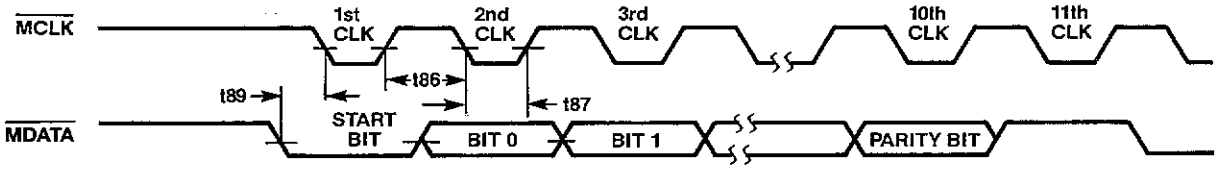
CLOCK TIMING



MOUSE TRANSMIT



MOUSE RECEIVE



AC ELECTRICAL CHARACTERISTICS (Continued)

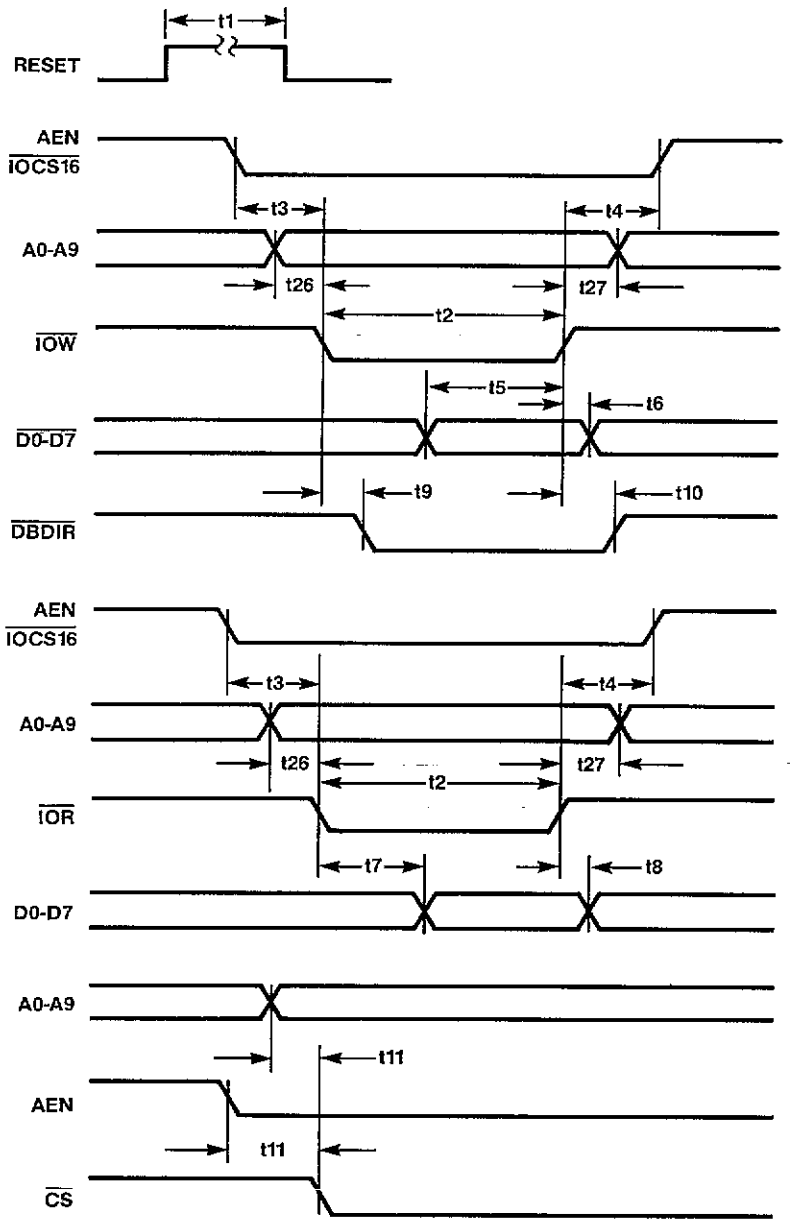
Symbol	Description	Min	Typ	Max	Units	Test Condition
Write Clock						
t30 (1)	Floppy Clock cycle		125		ns	8 MHz
	Derived from 24 MHz source		208.3		ns	4.8 MHz
			250		ns	4 MHz
t31 (1)	Write clock active high		2		t30	
t32 (1)	Delay from rising FCLK to rising WCLK	0		40	ns	
t33 (1)	Delay from rising FCLK to falling WCLK	0		40	ns	
Read Operation						
t34	Read data active high	40			ns	
t35 (1)	Window hold time to read data	15			ns	
t36 (1)	Window hold time from read data	15			ns	
Write Operation						
t38 (1)	Write clock cycle		16		t30	MFM+0, 5 1/4"
			8		t30	MFM=1, 5 1/4"
			8		t30	MFM=0, 8"
			4		t30	MFM=1, 8"
			8		t30	MFM=0, 3 1/2"
			4		t30	MFM=1, 3 1/2"
t39 (1)	Write clock rise/fall time			20	ns	
t40	FCLK to $\overline{\text{WGATE}}$ delay	10		80	ns	
t41 (1)	Preshift delay from rising WCLK	10		80	ns	
t42	$\overline{\text{WDATA}}$ delay from rising FCLK	10		80	ns	
t43	$\overline{\text{WDATA}}$ width	t30-50			ns	
Seek Operation						
t44 (1)	$\overline{\text{DRV0}}$, 1 hold time to RW/seek	12			us	8 MHz CLK (2)
t45 (1)	RW/Seek hold time to DIR	7			us	8 MHz CLK (2)
t47 (1)	$\overline{\text{SEEK}}$ hold time to DIR	30			us	8 MHz CLK (2)
t48	$\overline{\text{STEP}}$ active time	6	7	8	us	8 MHz CLK (2)
t50	DIR hold time after $\overline{\text{STEP}}$	24			us	8 MHz CLK (2)
t51	DIR hold time to $\overline{\text{STEP}}$	10			us	8 MHz CLK (2)
t52	$\overline{\text{STEP}}$ cycle time	33			us	8 MHz CLK (2)

NOTE:
1. These are internal signals.
2. Double these values for a 4 MHz clock period.

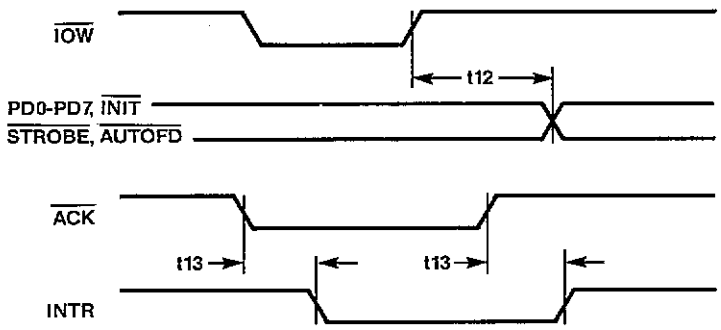
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Description	Min	Max	Units
Clock Timing				
tH	Clock high	17		ns
tL	Clock low	17		ns
tR				

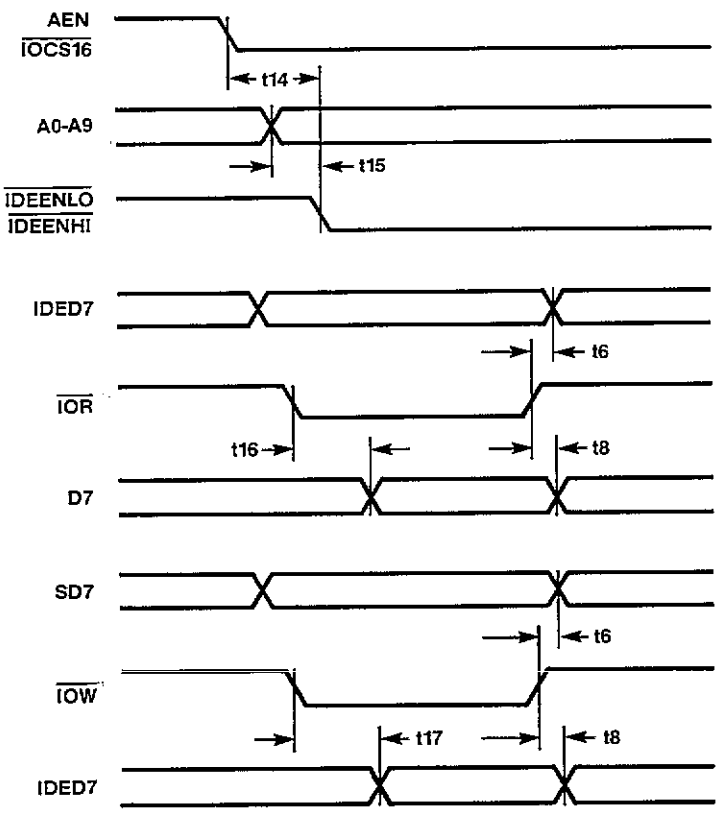
HOST INTERFACE TIMING



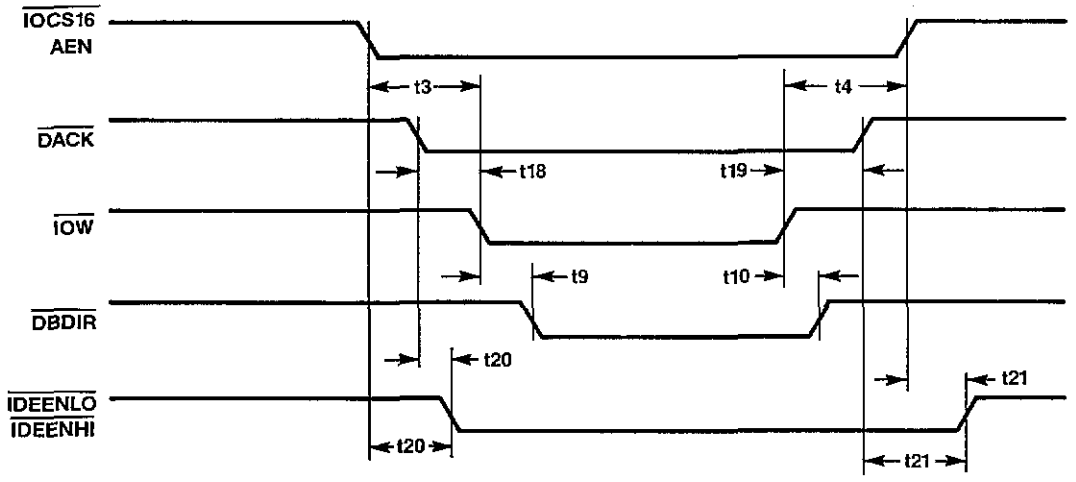
PARALLEL PORT TIMING



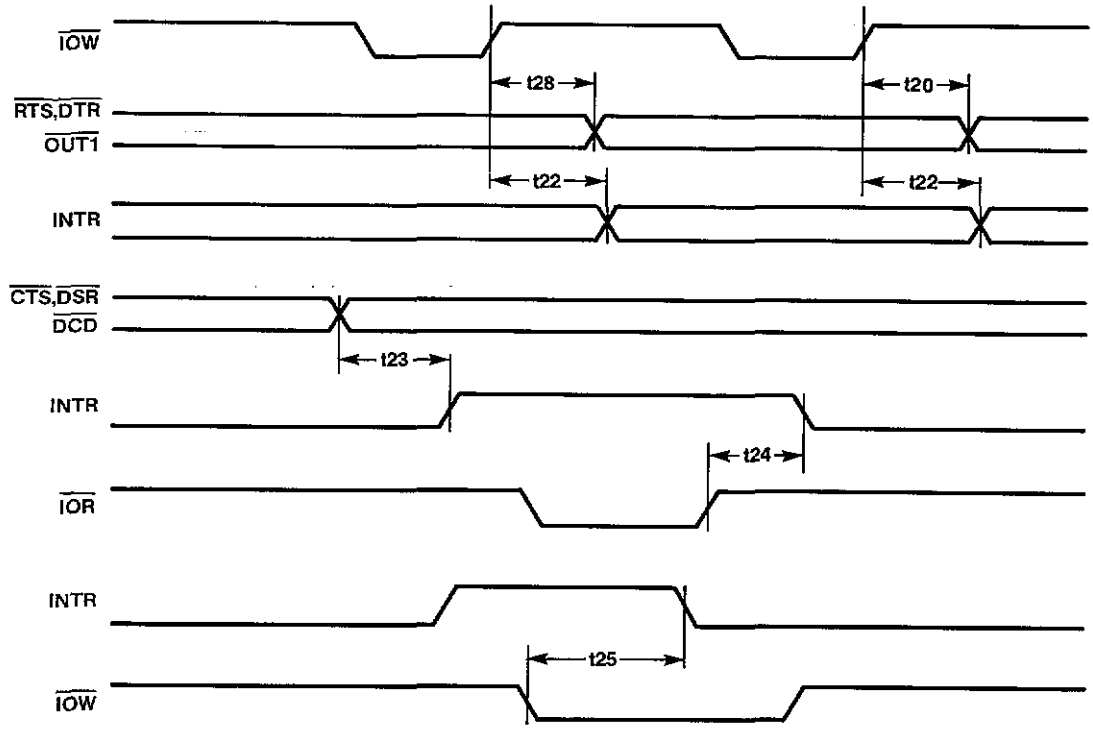
IDE INTERFACE TIMING



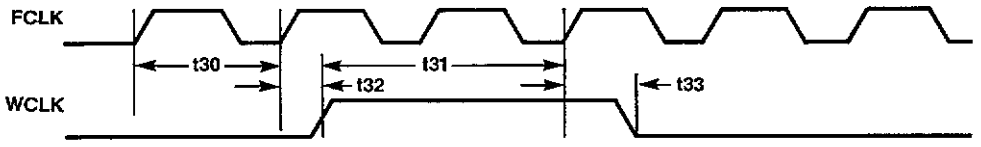
DMA TIMING



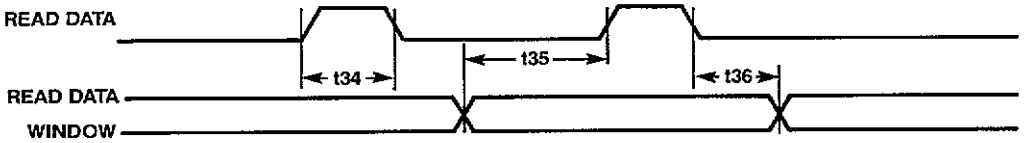
SERIAL PORT TIMING



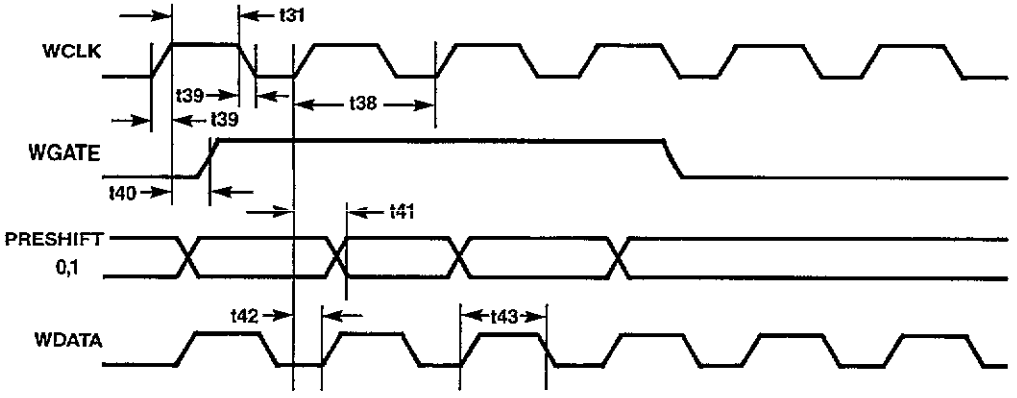
WRITE CLOCK



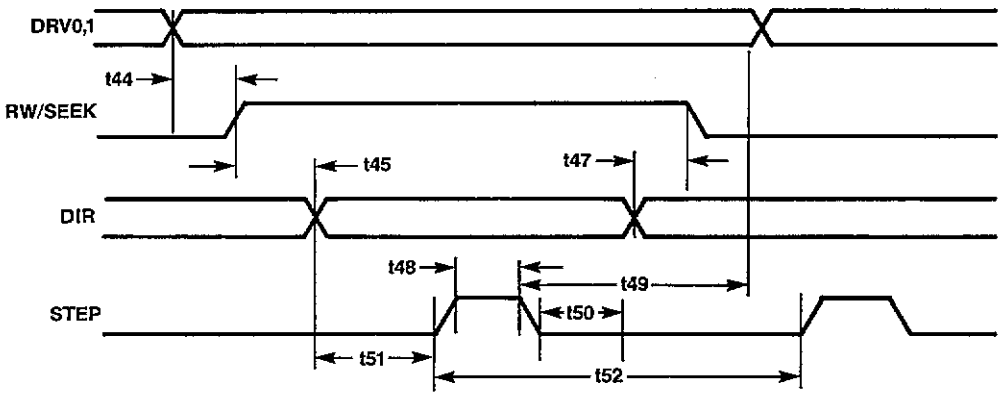
FDD READ OPERATION



FDD WRITE OPERATION



SEEK OPERATION

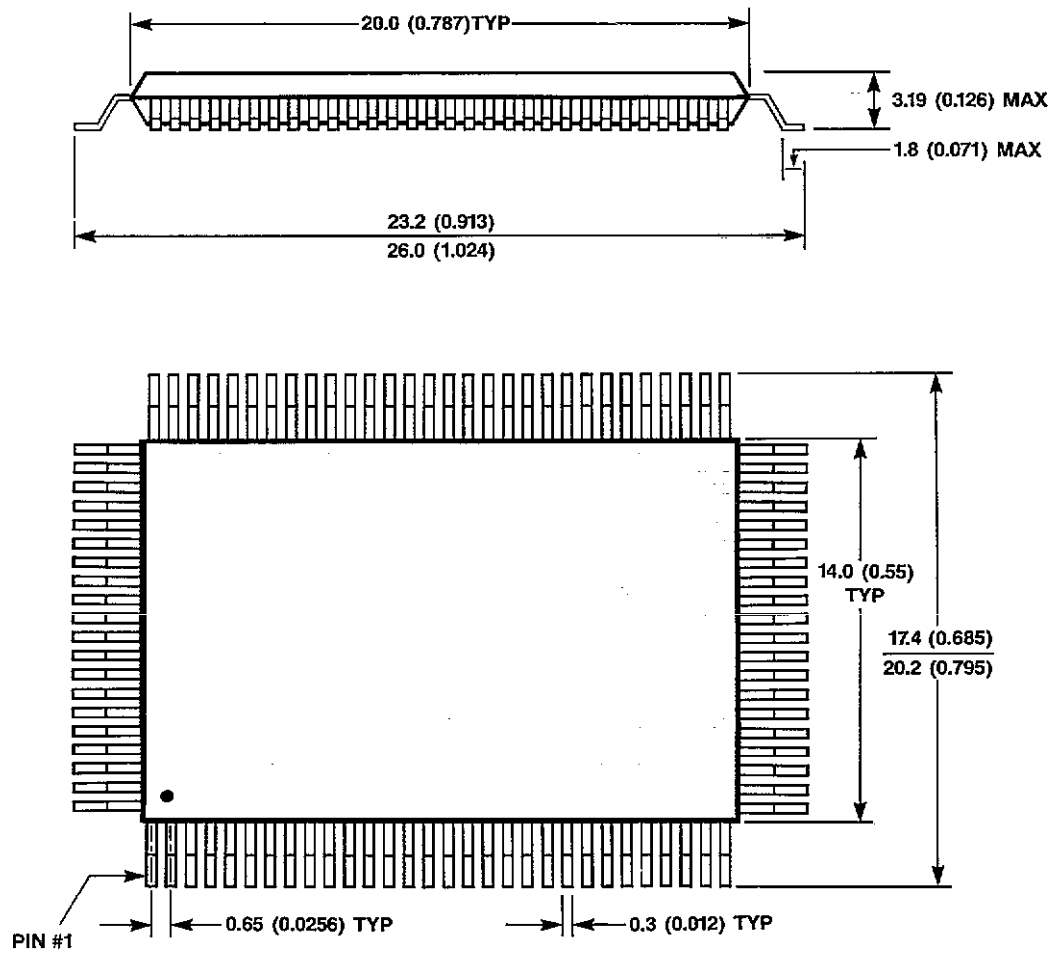


F82C710 (PQFP) PINOUT — 100 PINS

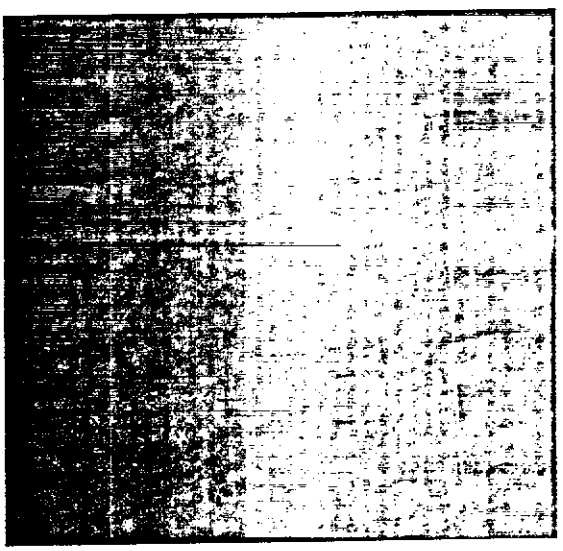
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	$\overline{\text{RTCCS}}$	31	A7	51	$\overline{\text{AUTOFD}}$	81	PREN
2	$\overline{\text{GPCS}}$	32	A6	52	$\overline{\text{ACK}}$	82	DSKCHG
3	IDED7	33	A5	53	BUSY	83	$\overline{\text{RDATA}}$
4	$\overline{\text{HDCS0}}$	34	A4	54	PE	84	$\overline{\text{WRTPRT}}$
5	$\overline{\text{HDCS1}}$	35	A3	55	SLCT	85	$\overline{\text{TRK0}}$
6	$\overline{\text{IDEENHO}}$	36	A2	56	$\overline{\text{ERROR}}$	86	HDSEL
7	$\overline{\text{IDEENLO}}$	37	A1	57	N/C	87	$\overline{\text{WGATE}}$
8	IOCS16	38	A0	58	N/C	88	$\overline{\text{WDATA}}$
9	PWRGD	39	PD0	59	Vss	89	$\overline{\text{STEP}}$
10	FINTR	40	PD1	60	MCLK	90	DIR
11	PINTR	41	PD2	61	$\overline{\text{MDATA}}$	91	$\overline{\text{MTR1}}$
12	SINTR	42	PD3	62	$\overline{\text{CTS}}$	92	$\overline{\text{DRV0}}$
13	MINTR	43	Vss	63	$\overline{\text{DSR}}$	93	Vss
14	D0	44	PD4	64	$\overline{\text{DCD}}$	94	$\overline{\text{DRV1}}$
15	D1	45	PD5	65	$\overline{\text{RI}}$	95	$\overline{\text{MTR0}}$
16	D2	46	PD6	66	RXD	96	RPM/LC
17	D3	47	PD7	67	Vcc	97	$\overline{\text{INDEX}}$
18	Vss	48	$\overline{\text{STROBE}}$	68	TXD	98	$\overline{\text{DACK}}$
19	D4	49	$\overline{\text{SLCTIN}}$	69	$\overline{\text{RTS}}$	99	DRQ
20	D5	50	INIT	70	$\overline{\text{DTR}}$	100	TC
21	D6			71	OSC1/CLK		
22	D7			72	OSC2		
23	$\overline{\text{DBDIR}}$			73	AVcc		
24	$\overline{\text{IOR}}$			74	FILTER		
25	$\overline{\text{IOW}}$			75	SETCUR		
26	RESET			76	AVss		
27	Vcc			77	RVI		
28	AEN			78	FGND 250		
29	A9			79	FGND 500		
30	A8			80	DRVTYP		

F82C710 (PQFP) PINOUT — 100 PINS

SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN
A0	38	$\overline{\text{DACK}}$	98	$\overline{\text{IOCS16}}$	8	RESET	26
A1	37	$\overline{\text{DBDIR}}$	23	$\overline{\text{IOR}}$	24	RI	65
A2	36	$\overline{\text{DCD}}$	64	$\overline{\text{IOW}}$	25	RPM/LC	96
A3	35	DIR	90	MCLK	60	$\overline{\text{RTCCS}}$	1
A4	34	DSKCHG	82	$\overline{\text{MDATA}}$	61	$\overline{\text{RTS}}$	69
A5	33	DRQ	99	MINTR	13	RVI	77
A6	32	$\overline{\text{DRV0}}$	92	$\overline{\text{MTR0}}$	95	RXD	66
A7	31	$\overline{\text{DRV1}}$	94	$\overline{\text{MTR1}}$	91	SETCUR	75
A8	30	DRVTYP	80	N/C	57	SINTR	12
A9	29	$\overline{\text{DSR}}$	63	N/C	58	SLCT	55
$\overline{\text{ACK}}$	52	$\overline{\text{DTR}}$	70	OSC1/CLK	71	$\overline{\text{SLCTIN}}$	49
AEN	28	$\overline{\text{ERROR}}$	56	OSC2	72	$\overline{\text{STEP}}$	89
$\overline{\text{AUTOFD}}$	51	FGND250	78	PD0	39	$\overline{\text{STROBE}}$	48
AVcc	73	FGND500	79	PD1	40	TC	100
AVss	76	FILTER	74	PD2	41	$\overline{\text{TRK0}}$	85
BUSY	53	FINTR	10	PD3	42	TXD	68
$\overline{\text{CTS}}$	62	$\overline{\text{GPCS}}$	2	PD4	44	Vcc	27
D0	14	$\overline{\text{HDCS0}}$	4	PD5	45	Vcc	67
D1	15	$\overline{\text{HDCS1}}$	5	PD6	46	Vss	18
D2	16	HDSEL	86	PD7	47	Vss	43
D3	17	IDED7	3	PE	54	Vss	59
D4	19	$\overline{\text{IDEENHI}}$	6	PINTR	11	Vss	93
D5	20	$\overline{\text{IDEENLO}}$	7	PREN	81	$\overline{\text{WDATA}}$	88
D6	21	$\overline{\text{INDEX}}$	97	PWRGD	9	$\overline{\text{WGATE}}$	87
D7	22	$\overline{\text{INIT}}$	50	$\overline{\text{RDATA}}$	83	$\overline{\text{WRPRT}}$	84



DIMENSIONS: mm (in)



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