82C607
Multifunction Controller

- **Single Chip UART and Analog Data Separator**
- **100% functionally compatible to the IBM PS/2 model 50, 60, and 80**
- **Fully compatible NS16550 Asynchronous Communications Element**
- **16 bytes FIFO for transmitter and receiver buffers**
- **Easy interface to the industry standard floppy disk controllers (765A/765B/8272A)**
- **Supports multiple data rates (250K, 300K, and 500Kbps)**
- **High drive, 48 mA output buffer**
- **Schmitt trigger inputs**
- **Low power advanced CMOS technology**
- **68 pin PLCC or 80 pin Flat Pack**

The 82C607 Multifunction Controller incorporates a single channel UART, an analog floppy disk data separator and the host interface logic compatible with IBM PS/2 model 50, 60, and 80 personal computers.

The UART is functionally compatible to NS16550 Asynchronous Communications Element. The data separator contains a self-calibrated analog phase locked loop (PLL), write precompensation circuit, and the logic interface to the industry standard 765A/765B/8272A floppy disk controller. It supports three standard data rates: 250K, 300K, and 500K bits per second, each selectable by software.

Together with 765A/765B/8272A, the 82C607 provides a very cost effective and high performance implementation for the serial port and the floppy disk sub-system for systems compatible to the PS/2 environment.

The 82C607 is implemented using advanced CMOS technology; available in 68 pin PLCC or 80 pin Flat Pack packages.

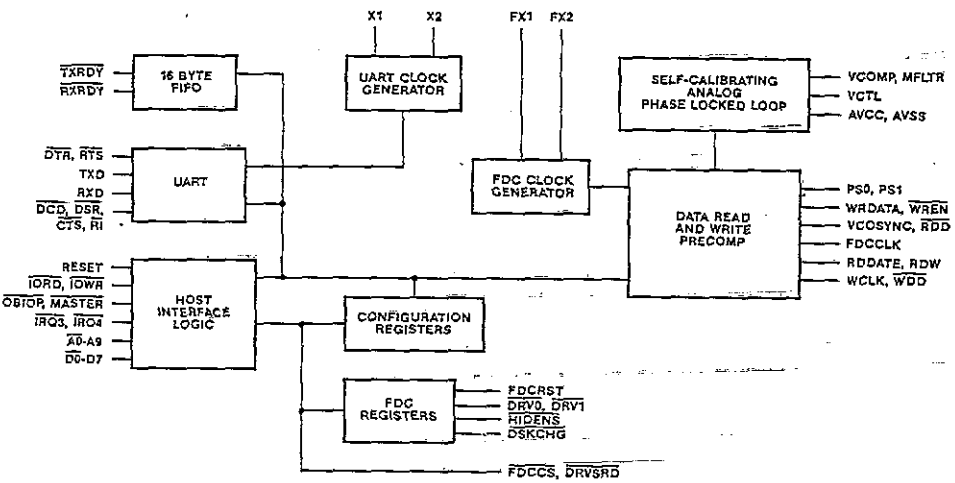


Figure 1. 82C607 Block Diagram

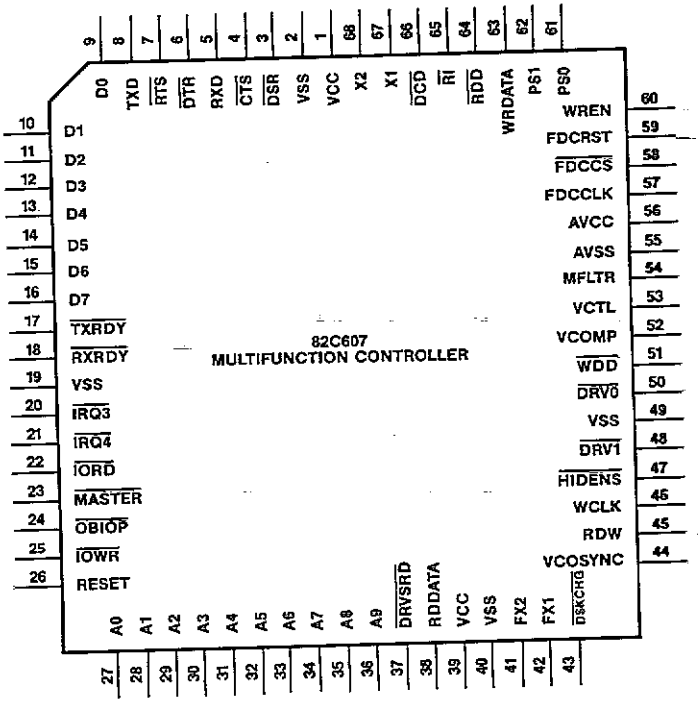


Figure 2. 82C607 Pin PLCC Pinout

82C607 68 PLCC Package Pin Description

Pin No.	Pin Type	Symbol	Description
System Bus Interface			
9-16	I/O	D0-D7	Three state, bidirectional Data Bus. These bits are connected to the system data bus. They should be connected to the peripheral (XD) bus (82C226 pins 31-24).
22	I	$\overline{\text{IORD}}$	Active low, I/O Read strobe. It should be connected to $\overline{\text{XIORD}}$ (82C221 pin 2).
23	I	$\overline{\text{MASTER}}$	Active low, MASTER signal. $\overline{\text{MASTER}}$ is an indication that an external bus master device is using the bus. When $\overline{\text{MASTER}}$ is active, I/O Read or I/O Write to addresses 0000H to 0099H is inhibited.
24	I	$\overline{\text{OBIOP}}$	Active low, On Board IO Peripheral Select. $\overline{\text{OBIOP}}$ is active when the system is addressing the first 1K of I/O space (I/O address range 0000H-03FFH). Normally, it is connected to 82C222 pin 57.
25	I	$\overline{\text{IOWR}}$	Active low, I/O Write strobe. It should be connected to $\overline{\text{XIOW}}$ (82C221 pin 3)
26	I	RESET	Active high, RESET. RESET initializes the 82C607, and should be valid for a minimum of 500 ns. It is a TTL level Schmitt trigger input.
27-36	I	A0-A9	Input, address bits 0 to 9. These addresses are decoded to access the internal registers.
Serial Port Interface			
3	I	$\overline{\text{DSR}}$	Active low, Data Set Ready. When active, it tells the CPU that the MODEM or Data Set is ready to transfer data. It can be monitored by reading bit 5 of the Modem Status Register (MSR). A change in the state of $\overline{\text{DSR}}$ signal since the last read will cause bit 1 of the Modem Status Register to go high. An interrupt will be generated when bit 5 of the Modem Status Read changes state, if the MODEM Status interrupt is enabled (bit 3 of the Interrupt Enable Register).

82C607 68 PLCC Package Pin Description (continued)

Pin No.	Pin Type	Symbol	Description
4	I	$\overline{CTS}$	*Active low, Clear To Send.* A handshake signal which notifies the UART that the MODEM is ready to receive data. The CPU can monitor this signal by reading bit 4 of the MODEM Status Register (MSR). Bit 0 of the MODEM Status Register indicates a change of state in the corresponding $\overline{CTS}$ signal since the last read of the MODEM Status Register. This signal does not affect the UART transmitter. A change in the state of bit 4 of the MODEM Status Register ($\overline{CTS}$) will cause the CPU to be interrupted if bit 3 (MODEM Status) of the Interrupt Enable Register is set.
5	I	RXD	Serial Data input (Receiver Data).
6	O	$\overline{DTR}$	Active low, Data Terminal Ready. When active, it notifies the MODEM or Data Set that the UART is ready to transfer data. It can be activated by writing a 1 to bit 0 of the MODEM Control Register. This output stays inactive after RESET or during internal loop-back mode.
7	O	$\overline{RTS}$	Active low, Request To Send. Handshake signal that notifies the MODEM or Data Set that the UART is ready to transmit data. This output can be changed by writing to bit 1 of the MODEM Control Register. This output stays inactive (high) after RESET or during internal loopback mode.
8	O	TXD	Serial Data output (Transmitter Data). It is reset to a 1 (Marking State) upon RESET.
17	O	$\overline{TXRDY}$	Active low, Transmit Ready. For MODE 0 (Interleaved DMA) operation, $\overline{TXRDY}$ will go active if there is no more data in the XMIT FIFO or in the Transmit Holding Register. It will become inactive after the first character is loaded into the XMIT FIFO. Only MODE 0 is allowed in Character Mode. For MODE 1 (Burst DMA) operation, $\overline{TXRDY}$ will become active if there is at least one unfilled position in the XMIT FIFO. It will go inactive when the XMIT FIFO is completely *full.*

82C607 68 PLCC Package Pin Description (continued)

Pin No.	Pin Type	Symbol	Description
18	O	$\overline{\text{RXRDY}}$	Active low, Receive Ready. For MODE 0 (Interleaved DMA) operation, $\overline{\text{RXRDY}}$ will go active if there is at least one character in the RCV FIFO or in the Receive Holding Register. It will become inactive if there are no characters in the RCV FIFO or Receive Holding Register. Only MODE 0 is allowed in Character Mode. For MODE 1 (Burst DMA) operation, $\overline{\text{RXRDY}}$ will become active if it has reached the RCV FIFO trigger level or the timeout timer has expired. It will go inactive if there are no more data in the RCV FIFO or in the Receive Holding Register.
20	OD	$\overline{\text{IRQ3}}$	Active low, Interrupt Request 3. Level triggered $\overline{\text{IRQ3}}$ is used if the UART is programmed as Serial Port 2. The output is open drain driver and requires a 4.7K pull-up resistor.
21	OD	$\overline{\text{IRQ4}}$	Active low, Interrupt Request 4. Level triggered $\overline{\text{IRQ4}}$ is used if the UART is programmed as Serial Port 1. The output is open drain driver and requires a 4.7K pull-up resistor.
65	I	$\overline{\text{RI}}$	Active low, Ring Indicator signal. When active, it notifies the UART that a telephone ringing signal has been detected by a MODEM or Data Set. It can be monitored by reading bit 6 of the MODEM Status Register. When this signal goes from an active to an inactive state, bit 2 of the MODEM Status Register will be set. If MODEM Status Interrupt is enabled, activation of this signal will generate an interrupt at the trailing edge of $\overline{\text{RI}}$.
66	I	$\overline{\text{DCD}}$	Active low, Data Carrier Detect. When active, it notifies the UART that a carrier signal has be detected by the MODEM or Data Set. The CPU can monitor this signal by reading bit 7 of MODEM Status Register. A change in the state of this signal since the last read of the MODEM Status Register will cause bit 3 of the MODEM Status Register to go high. It has no effect on the UART receiver. An interrupt will be generated when bit 7 of the MODEM Status Register changes state if MODEM Status Interrupts are enabled (bit 3 of the Interrupt Enable Register).
67	I	X1	UART Crystal input, 1.8432 MHz, 3.075 MHz, or 8.0 MHz.
68	O	X2	UART Crystal output. This clock is used by the UART to generate the baud rates. A fundamental frequency parallel resonant crystal should be connected to this pair. Alternately, an external clock generator can be connected to X1; X2 should be left unconnected.

82C607 68 PLCC Package Pin Description (continued)

Pin No.	Pin Type	Symbol	Description
Floppy Disk Controller Interface			
37	O	$\overline{\text{DRVSRD}}$	Active low, Drive Status Register Read. $\overline{\text{DRVSRD}}$ goes active when the 82C607 decodes an I/O read of address 03F0H.
38	O	RDATA	Active high, Read Data output. RDATA is synchronized with RDW, it contains data and clock bits. The FDC will separate the clock and data bits.
42 41	I O	FX1 FX2	24 MHz crystal oscillator input. 24 MHz crystal oscillator output. This clock is used by the data separator. A fundamental frequency parallel resonant crystal should be connected to this pair. Alternately, an external clock generator can be connected to FX1; FX2 should be left unconnected.
43	I	$\overline{\text{DSKCHG}}$	Active low, Disk Change signal. An input from the from the floppy disk drive. It goes active when a diskette is removed from the drive. This pin has a Schmitt trigger input buffer.
44	I	VCOSYNC	Active high, Read Enable control signal from FDC. When active, it indicates that FDC is in read operation and allows the PLL to lock onto the input data. When inactive, the read operation is inhibited and the PLL ignores the incoming data on $\overline{\text{RDD}}$ pin.
45	O	RDW	Active high, Read Data Window. This signal is used by the FDC to sample the clock and data bits of RDATA.
46	O	WCLK	Write Clock for FDC.
47	O	$\overline{\text{HIDENS}}$	Active low, High Density Disk. It is active when the data rate is programmed to 500K bps high density mode. A 48 mA current sinking capability driver is provided by this pin.
48 50	O O	$\overline{\text{DRV1}}$ $\overline{\text{DRV0}}$	Active low, Drive Select 1. Active low, Drive Select 0. When active, it selects the floppy disk drive and enable the motor. This pin is capable of sinking 48 mA current and can be connected to the disk drive cable directly.
51	O	$\overline{\text{WDD}}$	Active low, Precompensated Write Data. $\overline{\text{WDD}}$ is connected to the floppy drive, capable of sinking 48 mA.
52	I/O	VCOMP	Compensation voltage for the dual PLL. An external capacitor connected to this pin to provide reference for PLL filter.
53	I	VCTL	VCO Control Voltage for the main PLL.

82C607 68 PLCC Package Pin Description (continued)

Pin No.	Pin Type	Symbol	Description
54	I/O	MFLTR	Main PLL Filter. A external RC filter network is connected to this pin.
55	I	AV_{SS}	Analog ground.
56	I	AV_{CC}	Analog power supply.
57	O	FDCCK	Clock output to FDC.
58	O	$\overline{FDCCS}$	Active low, FDC Chip Select signal. $\overline{FDCCS}$ is a decoded signal for I/O address range 3F0H-3F7H.
59	O	FDCRST	Active high, FDC Reset signal.
60	I	WREN	Active high, Write Enable control signal from FDC.
61,62	I	PS0, PS1	From the FDC for Precompensation Select.

PS0	PS1	Precompensation
0	0	No Shift
0	1	125 ns late
1	0	125 ns early
1	1	Undefined

63	I	WDATA	Active high, Uncompensated Write Data from the FDC.
64	I	$\overline{RDD}$	Active low, Raw Read Data from the disk drive. A Schmitt trigger input buffer is used in this pin to provide higher noise margin.
1,39		V_{CC}	Digital power supply.
2,19,40,49		V_{SS}	Digital ground.

Notes:
I = Input
O = Output
OD = Open Drain
B = Bidirectional
T = Tristate

82C607 Functional Description

The 82C607 consists of a NS16550 compatible Asynchronous Communications Elements with a FIFO like that used in the IBM PS/2 model 50/60/80, a Data Separator for 765A/765B/8272A compatible Floppy Disk Controller, and the interface logic for the PS/2 applications.

Each of the subsystems is described in detail in the subsequent chapters. The 82C607 is best suited when used with the CS8250/CS8280 PS/2 model 50/60/80 compatible chipset.

Figure 1. shows the internal block diagram for the 82C607.

The System Interface Logic includes: Setup/Enable Mode register, Enable register, Internal Configuration register, decoding logic, and self test features. Additionally the 82C607 allow flexibility in configuring the device within a PS/2 compatible environment by software. Through bit manipulations: serial port and floppy interface can be enabled or disabled, the serial port can be configured as Serial 1 (address 3F8H-3FFH) or Serial 2 (address 2F8H-2FFH), and test features can be enabled or disabled.

Upon power up, the UART defaults to 16450 (non-FIFO) mode. After programmed to the enhanced mode, the internal FIFOs are enabled, allowing 16 bytes of data to be stored in each transmit or receive mode (plus 3 error bits per byte in receive mode). The FIFO lessen CPU interactions during fast transfers, thus minimize systems overhead and maximize the overall efficiency.

The high performance, CMOS Data Separator contains a self-calibrated analog phase locked loop, write precompensation circuitry, and the FDC interface. The self-calibrating feature eliminates the costly adjustments of external components, at the same time provides accurate data recovery. The write precompensation circuit shifts the bit patterns written to the disk as determined by the FDC. The 82C607 supports three standard data rates: 250K, 300K, and 500K bits per second; this option is software selectable.

SYSTEMS INTERFACE

The systems interface function is to simplify the 82C607 connection to any PS/2 environment, namely the Programmable Option Select (POS) registers. POS eliminates hardware switches by using programmable registers.

I/O port 0022H and 0023H are the Configuration Index (CIR) and Configuration Data registers (CDR) respectively. Configuration registers also support chip enable and internal test enable/disable features. I/O port 0094H is the System Board Enable/Setup Register, and I/O port 0102H (POS Register 2) is System Board I/O register. This register set enables/disables and select the Serial port and the Floppy Disk Interface functions.

0022H - Write Only: Configuration Index Register (CIR)

CIR is the address to the configuration registers, it can be written only when MASTER = 1 and $\overline{\text{OBIOP}}$ = 0. For each access to the CDR, a value of **A8H** has to be written to CIR.

Index A8H: To access CDR

0023H - Read/Write: Configuration Data Register (CDR)

It can be accessed only when CIR is equal to **A8H** , MASTER = 1 and $\overline{\text{OBIOP}}$ = 0.

0023H Read Only: System Status

Bit 7:	State of bit 7 of the Enable register (94H). 0: Setup Mode 1: Enable Mode. Default.
Bit 6:	Data Separator Test Control. 0: Disable Test. Default. 1: Enable Test
Bit 5:	UART Test Control. 0: Disable Test. Default. 1: Enable Test.
Bit 4:	Reserved. The state of this bit depends on the pattern written into bit 4 of the control register.
Bit 3:	Serial Port Select. 0: Not selected. Default. 1: Serial port selected.
Bit 2:	Enable Serial Port. 0: Disabled. Default. 1: Enabled.
Bit 1:	Enable Diskette Drive Interface. 0: Disabled. Default. 1: Enabled.
Bit 0:	Peripheral Enable. 0: Disabled. Default. 1: Enabled.

0023H Write Only: Test Mode Enable.

Bit 7:	Reserved, should be 0.
Bit 6:	Enable Data Separator Test. 0: Disable Test. Default. 1: Enable Internal Data Separator Test Function.
Bit 5:	Enable UART Test. 0: Disable Test. Default. 1: Enable Internal UART Test Function.
Bit 4-0:	Reserved, should be written as 0.

Bit 6-5 are reset to "0" when RESET goes active.

0094H - Write Only: System Setup/Enable Mode.

Selects either Setup or Enable mode. Can be written only if MASTER = 1 and OBIOP = 0. Bit 7 is forced to "1" upon RESET.

Bit 7:	Function Mode. 0: Setup mode. 1: Enable mode. Default.
Bit 6-0:	Reserved, should be 0.

0102H - Write only: System IO Byte Register (POS Reg. 2).

It can be written only when OBIOP = 0 and bit 7 of register 94 = 0. All the bits are reset to 0 (disabled) upon RESET.

Bit 7-4:	Reserved, should be 0.
Bit 3:	Serial Port Select. 0: Serial port = Serial 2 (address 278H). Default. 1: Serial port = Serial 1 (address 3F8H).
Bit 2:	Enable Serial Port. 0: Disable serial port. Default. 1: Enables the serial port if Bit 0 is "1".
Bit 1:	Enable Floppy Drive Interface. 0: Disable floppy drive interface. Default. 1: Enables the floppy drive interface if b0 is 1.
Bit 0:	Peripheral Enable. 0: Serial port and FDI are disabled. Default. 1: Allows bit 1 and bit 2 to be enabled.

To install the 82C607:

1. Write A8H to CIR (port 0022H).
2. Read CDR (port 0023H), it should read 80H (Enable mode).
3. Write 00H to port 0094H to setup the 82C607.
4. Write 05H to POS Reg. 2 (port 0102H) to enable Serial 2 (2F8H-2FFH), or 0DH to enable Serial 1 (address 3F8H-3FFH).
5. Write 80H to port 0094H to enable the 82C607.

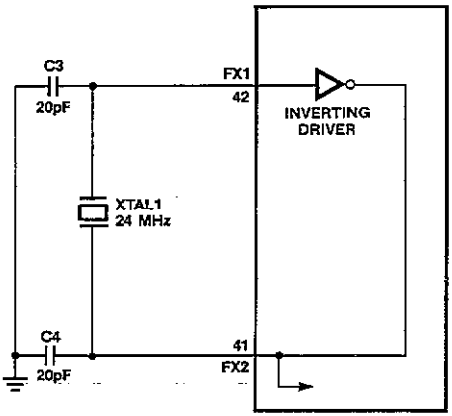


Figure 3A. Clock Provided by a Crystal

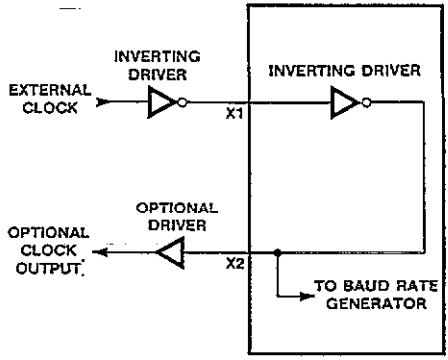


Figure 3B. Clock Provided by an External Clock

Table 1 Typical Resistor and Capacitor Values for Oscillator Network

Xtal Freq	R1	C1	C2
1.8432 MHz	2 M	20 pF	20 pF
3.072 MHz	2 M	20 pF	20 pF
8.0 MHz	2 M	20 pF	20 pF

Note (1): No resistor needed.

Table 2 Baud Rate Divisor Values

Baud	1.8 MHz			3.1 MHz			8.0 MHz		
Rate	Dec	Hex	% Err	Dec	Hex	% Err	Dec	Hex	% Err
50	2304	0900	—	3840	0F00	—	10000	2710	—
75	1536	0600	—	2560	0A00	—	6667	1A0B	.005
110	1047	0417	.026	1745	06D1	.026	4545	11C1	.010
134.5	857	0359	.058	1428	0594	.034	3717	0E85	.013
150	768	0300	—	1280	0500	—	3333	0D05	.010
300	284	011C	—	640	0280	—	1667	0683	.020
600	192	00C0	—	320	0140	—	833	0341	.040
1.2 K	96	0060	—	160	00A0	—	417	01A1	.080
1.8 K	64	0040	—	107	006B	.312	277	0115	.080
2.0 K	58	003A	.69	96	0060	—	250	00FA	—
2.4 K	48	0030	—	80	0050	—	208	00D0	.160
3.6 K	32	0020	—	53	0035	.628	139	008B	.080
4.8 K	24	0018	—	40	0028	—	104	0068	.160
7.2 K	16	0010	—	27	001B	1.23	69	0045	.644
9.6 K	12	000C	—	20	0014	—	52	0034	.160
19.2 K	6	0006	—	10	000A	—	26	001A	.160
38.4 K	3	0003	—	5	0005	—	13	000D	.160
56 K	2	0002	2.86				9	0009	.790
128 K							4	0004	2.34
256 K							2	0002	2.34

UART

The UART implemented is NS16550 compatible, which is NS16450 compatible in character mode. In the FIFO mode, a 16 byte FIFO for each transmit and receive buffers are enabled. The oscillator pins 67 (X1) and 68 (X2) should be connected to a crystal circuit as shown in figure 3A. In place of a crystal, a clock oscillator can be connected to pin X1 (and leaving X2 unconnected), as shown in figure 3B. Values for the external components for 1.8432 MHz, 3.072 MHz, and 8 MHz are tabulated in Table 1. The baud rate generator divides this frequency to produce 16X the baud rate clock, using a 16 bit value stored in the divisor registers. Table 2 lists the divisors for commonly used baud rates.

RESET

Various UART registers and signals are reset to their default values when RESET (26) signal is applied to the 82C607. Also certain reads and writes effect some register contents. Table 3 below summarizes RESET controls and effects.

Table 3 Reset Control and Reset Effect

Register/Signal	Reset Control	Reset Effect
Interrupt Enable Register	H/W Reset	All bits = 0
Interrupt Flag Register	H/W Reset	Bits 0 = 1, bits 1-7 = 0
Modem Control Register	H/W Reset	All bits = 0
Line Status Register	H/W Reset	All Bits = 0 <60>
Modem Status Register	H/W Reset	Bits 0-3 = 0, bits 4-7 = inputs
TXD	H/W Reset	High (1)
Line Status Interrupt	H/W Reset or Read LSR	Low (0)
Receive Buffer Full Interrupt	H/W Reset or Read RB	Low (0)
Transmit Buffer Empty Interrupt	H/W Reset Read IFR Write TB	Low (0)
Modem Status Interrupt	H/W Reset or Read MSR	Low (0)
$\overline{RTS}$	H/W Reset	High (1)
$\overline{DTR}$	H/W Reset	High (1)
RCV FIFO	H/W Reset or FCR0 and FCR1 or FCR0 = 0	All bits = 0
XMIT FIFO	H/W Reset or FCR0 and FCR2 or FCR0 = 0	All bits = 0
FIFO Control	H/W Reset	All bits = 0

Accessing UART Registers

To access the UART registers the 82C607 has to be enabled, and the UART has to be enabled. See the above SYSTEMS INTERFACE section to enable the UART and the 82C607. Table 4 below lists the accessible UART registers.

Table 4 UART Registers Addresses

Serial 1	Serial 2	DRAB	R/W	Register Name
03F8H	02F8H	0	R	Receive Buffer
03F8H	02F8H	0	W	Transmit Buffer
03F9H	02F9H	0	R/W	Interrupt Enable Register
03F8H	02F8H	1	R/W	Divisor (LSB)
03F9H	02F9H	1	R/W	Divisor (MSB)
03FAH	02FAH	X	R	Interrupt Flag Register
03FAH	02FAH	X	W	FIFO Control
03FBH	02FBH	X	R/W	Byte Format Register
03FCH	02FCH	X	R/W	Modem Control Register
03FDH	02FDH	X	R/W	Line Status Register Write for Testing Only
03FEH	02FEH	X	R/W	Modem Status Register
03FFH	02FFH	X	R/W	Scratch Pad Register

Note:
X = Don't Care
MSB = Most Significant Byte
LSB = Least Significant Byte
DRAB = Divisor Register Address Bit

BIT DEFINITIONS OF ACCESSIBLE REGISTERS

I/O addresses 03F8H-03FFH are for Serial 1, and 02F8H-02FFH for Serial 2 registers. They can be accessed only when OBIOP = 0.

0xF8H - R: Receive Buffer (RB)

The incoming serial bit pattern is encoded and filtered from the Start, Stop, and the Parity bits into the Receive Shift Register (not user accessible). The bits are assembled into a byte, then loaded into the Receive Buffer (double buffering method). In FIFO mode, the byte is loaded onto the top of FIFO, then the FIFO is pushed down (if FIFO is not full).

0xF8H - W: Transmit Buffer (TB)

For the transmit buffer, the procedure is reversed. A byte pattern from Transmit Holding Register is appended with the Start, Stop, and Parity bit, loaded into Transmit Shift Register (not user accessible), then shifted out to the TXD pin clocked by the transmit clock. In FIFO mode, the byte is loaded from top of FIFO, then the next character is popped into top of the FIFO (if FIFO is not empty).

0xF9H - R/W: Interrupt Enable Register (IER)

The lower 4 bits (bits 0-3) enables four types of interrupts, the higher 4 bits are 0. When all the bits are 0 the INTR output, and the Interrupt Flag Register (IFR) are inhibited. Any of the interrupt bits can be selectively enabled (set to 1). If this condition is met, an interrupt will be generated (INTR will be high), and the corresponding IFR bits will be set. The bit definitions are as follows:

Bit 0: Generates interrupt when Receive Buffer is filled (or a timeout condition in FIFO mode).

Bit 1: Generates interrupt when Transmit Register is empty.

Bit 2: Generates interrupt when any error (Overrun, Parity, Framing, or Break) occurs in the Line Status Register. The LSR should be read to determine the error.

Bit 3: Generates interrupt when any bits in the Modem Status Register changes state.

Bit 4-7: These bits are always set to 0.

0xFAH - R: Interrupt Flag Register (IFR)

IFR indicates if an interrupt has occurred, the type of interrupt, and sets the priority. It freezes the highest level, allows no other interrupt to change IFR value, until it is serviced by the system. Bit definitions:

Bit 0: 0 - Interrupt Pending
1 - No Interrupt.

Bit 1,2: These bits indicates the highest pending interrupt as shown in Table 5.

Bit 3: This bit is always 0 in Character mode. In FIFO mode, it indicates Timeout Interrupt is pending, if bit 2 is also set.

Bit 4-6: These bits are always set to 0.

Bit 7: This bit is set when FCR0 = 1 (in FIFO mode)

Table 5 Interrupt Types and Priorities

b3	b2	b1	b0	Level	Type	Source	Reset
0	0	0	0	—	None	—	
0	1	1	0	Highest	Line Status	Overrun, Parity, Framing, or Break	Read LSR, or FCR1 = 1, or H/W Reset
0	1	0	0	Second	RB full	Data Received, or Reached Trigger Level	Read RB, or FIFO Dropped Below Trig. Level, or FCR1 = 1, or H/W Reset
1	1	0	0	Second	Timeout	No Data Removed from FIFO or no inputs to RCV FIFO for the last 4 character times and RCV FIFO is not empty during this time	Read RB, or FCR1 = 1, or H/W Reset
0	0	1	0	Third	TB Empty	TB Empty	Read IFR or Write TB
0	0	0	0	Fourth	Modem Status	CTS,DSR,RI,DCD	Read MSR

Note: b3-b0 in the above table 5 corresponds to bits 3-0 of the Interrupt Flag register (IFR @ 0xFA)

0xFAH - W: FIFO Control Register (FCR)

The FIFO Control Register enables, resets, and/or sets trigger for FIFO operations, and selects DMA type. Bit definitions are as follows:

Bit 0: Enable FIFO Mode (FCR0)

Value	Function
0	Disable FIFO, also clears both FIFOs.
1	Enable both XMIT and RCV FIFOs. FIFOs are automatically cleared when changing modes (Character to FIFO, and vice versa), thus they need not be cleared manually.

Bit 1: Clear RCV FIFO (FCR1)

Value	Function
0	Normal Operation.
1	Clear RCV FIFO All the bytes in RCV FIFO are cleared, and the FIFO counter is reset to 0, but the shift register is not cleared. This bit resets itself to 0.

Bit 2: Clear XMIT FIFO (FCR2)

Value	Function
0	Normal Operation.
1	Clear XMIT FIFO All bytes in XMIT FIFO are cleared, and the FIFO counter is reset to 0, but the shift register is not cleared. This bit resets itself to 0.

Bit 3: DMA Mode Select (FCR3)

Value	Function
0	Interleave Mode DMA A single character is transferred between CPU cycles.
1	Burst Mode DMA Characters are continuously transferred until RCV FIFO is empty or XMIT FIFO is full.

Bit 4, 5: Reserved, should be set to 0

Bit 6, 7: RCV FIFO Trigger Level (FCR6, FCR7) These bits are used to set the trigger level for RCV FIFO interrupt. FCR6 is the LSB, FCR7 is the MSB.

Table 5 RCV FIFO Trigger Level

FCR6	FCR7	Trigger Level
0	0	1 Byte
0	1	4 Bytes
1	0	8 Bytes
1	1	14 Bytes

0xFBH - R/W: Byte Format Register (BFR)

The Byte Format Register specifies the format of the data exchange. Bit definitions are as follows:

Bit 0, 1: These bits specify the number of bits per character transmitted or received.

Bit 2: This bit with bits 0 and 1 determines the number of stop bits used for each transmitted character.

Table 6 Word Length and Number of Stop Bits

Bit 2	Bit 0	Bit 1	Word Length	Stop Bits
0	X	X	X Bits	1 Bit
1	0	0	5 Bits	1½
1	0	1	6 Bits	2
1	1	0	7 Bits	2
1	1	1	8 Bits	2

Note: X's are don't cares.

Bit 3: Enable Parity Bit.

Value	Function
0	Parity Disabled.
1	Parity Enabled. Parity is generated (transmit), and checked (receive) between the last data bit and Stop bit.

Bit 4: Even Parity Bit

Value	Function
0	Odd Parity, if parity enabled (bit 3 is 1). Odd number of 1's of the data word and Parity bit is transmitted or checked.
1	Even parity, if parity enabled (bit 3 is 1). Even number of 1's of data word and Parity bit is transmitted or checked.

Bit 5: Forced Parity Bit

Value	Function
0	Disable Forced Parity
1	Enable Forced Parity. Always ensures correct parity sense. When bits 3, 4, and 5 are 1's (even parity) the Parity bit is sent and checked as 0 . If bits 3 and 5 are 1's and bit 4 is 0 (odd parity) the Parity bit is sent and checked as 1.

Bit 6: Break Enable Bit

Value	Function
0	Break Disabled.
1	Break Enabled, TXD is forced to 0 (Spacing State). Break is used to get attention of a terminal. The following sequence ensures no errors or extra characters: 1. Load 0's to Transmit Buffer, when empty. 2. Enabled Break after the next empty Transmit Buffer. The transmitter can be used to time the character, and correct the baud rate. 3. Wait for idling transmitter (TE = 1). 4. Disable Break when normal transmission has been restored.

Bit 7: Divisor Register Access Bit

Value	Function
0	Normal Operation. Used to access the Receive Buffer, the Transmit Buffer, and the Interrupt Enable Register.
1	Divisor Register Access. Used to access the Divisor Latches of the Baud Generator.

0xFCH – R/W: Modem Control Register (MCR)

Modem Control register sets the modem interface, and enables an internal loopback feature for diagnostics. Definitions of the individual bits:

Bit 0: Data Terminal Ready ($\overline{DTR}$)

Value	Function
0	$\overline{DTR}$ output is set to 1
1	$\overline{DTR}$ output is reset to 0

Bit 1: Request To Send ($\overline{RTS}$)

Value	Function
0	$\overline{RTS}$ output is set to 1
1	$\overline{RTS}$ output is reset to 0

Bit 2: Output 1 ($\overline{OUT1}$)
No external connection, for diagnostic purposes only.

Bit 3: Output 2 ($\overline{OUT2}$).
No external connection. $\overline{OUT2}$ used to control INTR output.

Value	Function
0	INTR output is high impedance
1	INTR is Enabled.

Bit 4: Loopback Mode

Value	Function
0	Normal Mode
1	Loopback Mode, the following occur: ■ Serial Output (TXD) is set to a 1 (Marking State) ■ Serial Input (RXD) is disabled ■ Transmit Shift Register is looped back to the Receive Shift Register. ■ Modem inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disabled ■ Modem outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are looped back to the Modem inputs, and also forced inactive (high). The connections are as follows: $\overline{RTS}$ to $\overline{CTS}$ $\overline{DTR}$ to $\overline{DSR}$ $\overline{OUT1}$ to $\overline{DCD}$ $\overline{OUT2}$ to RI In this diagnostic mode, the interrupts are fully functional. Interrupts from Modem Control are also functional. The Interrupt Enable Register controls the interrupt enable/disable functions.

Bit 5-7: These bits are set to 0.

0xFDH - R/W: Line Status Register (LSR)

Line Status Register provides information about the data received and the status of the Transmit Buffer and Transmit Shift Register. If any of the bits 0-4 of the Line Status Register are set (error and/or data ready indication), and the corresponding interrupts in the interrupt Enable register (0xF9) are enabled (set to 1), then an interrupt will be generated. Definition of the bits are as follows:

Bit 0: Data Ready (DR)

Value	Function
0	No Data or Receive Buffer/RCV FIFO was Read.
1	Data Available in Receive Buffer/ RCV FIFO. This bit is reset to 0 after reading all the data in the RCV FIFO or the Receive Buffer.

Bit 1: Overrun Error indicator (OE)

Value	Function
0	Normal Condition, no Overrun Error.
1	Overrun Error has occurred. In Character mode, it indicates that the current character overwrote the previous one, because the data in the Receive Buffer has not been transferred. The OE bit is reset to 0 after reading this register (LSR @ 0xFD).In FIFO mode, it indicates that the FIFO is full and the character is received in the shift register. If more data is still received, then the previous character in the shift register is overwritten, but not transferred to the FIFO.

Bit 2: Parity Error indicator (PE)

Value	Function
0	Normal Condition, no Parity Error
1	Parity Error has occurred. In Character mode, it means an incorrect parity bit was received, it does not match with the parity bit generated. The PE bit is reset to 0 after reading this register (LSR @ 0xFD).In FIFO mode, it indicates Parity error in the data at the top of the FIFO.

Bit 3: Framing Error indicator (FE)

Value	Function
0	Normal Condition, no Framing Error.
1	Framing Error. Framing Error indicates invalid Stop bit was received (the Stop bit following the last data bit or parity bit is a "0"). The FE bit is reset to 0 after reading this register (LSR @ 0xFD). In FIFO mode, it means a Framing Error for the data at the top of the FIFO.

Bit 4: Break Interrupt indicator (BI)

Value	Function
0	Normal Condition, no Break detected
1	Break Condition detected. The number of 0's received is more than the full word length (Start + data + Parity + Stop). The BI bit is reset to 0 after reading this register (LSR @ 0xFD).In FIFO mode, it means Break condition with the data at the top of the FIFO. Only one Break character is loaded into the FIFO. Data transfer into the FIFO is disabled until the next received bit is 1 and the next valid Start bit is received.

Bit 5: Transmit Buffer Empty (TBE)

Value	Function
0	Transmit Buffer or XMIT FIFO is not empty
1	Transmit Buffer or XMIT FIFO is empty It indicates that the UART is ready to receive the next data to be sent out. It indicates that the data is loaded from the Transmit Buffer to the Transmit Shift Register. An interrupt will be generated if Transmit Buffer Empty Interrupt is set to 1. This bit is reset to 0 when data is transferred to the Transmit Buffer. In FIFO mode, this bit is set to 1 if the XMIT FIFO is empty; and reset to 0 after the first character is loaded into the XMIT FIFO.

Bit 6: Transmitter Empty indicator (TE)

Value	Function
0	Data in the Transmit Buffer or in the Transmit Shift Register
1	Both Transmit Buffer and Transmit Shift Register are empty. In FIFO mode, it indicates that both XMIT FIFO and Transmit Shift Register are empty. This bit is reset to 0 when either Transmit Buffer or Transmit Shift Register loaded with data.

Bit 7: FIFO Error indicator (LSR7)

Value	Function
0	In Character mode or no FIFO Errors
1	At least one error in the FIFO. Indicates Parity error, Framing error, or break condition in any of the data in the FIFO. LSR7 is reset to 0 after reading this register (LSR - 0xFD), and there is no other error in the FIFO.

0xFEH - R/W: Modem Status Register (MSR)

Modem Status Register reflects the status of the modem lines ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$). The lower nibble records the changes of the modem status. If any of bits 0-3 is set to 1, Modem Status Interrupt will go active. The upper nibble reflects the status of the input pins.

Bit 0: Delta Clear To Send (DCTS)

Value	Function
0	$\overline{CTS}$ has not changed
1	$\overline{CTS}$ has changed state since the last read

Bit 1: Delta Data Set Ready (DDSR)

Value	Function
0	$\overline{DSR}$ has not changed
1	$\overline{DSR}$ has changed state since the last read

Bit 2: Trailing Edge of Ring Indicator (TERI)

Value	Function
0	$\overline{RI}$ has not changed
1	$\overline{RI}$ changed from low to high

Bit 3: Delta Data Carrier Detect (DDCD)

Value	Function
0	$\overline{DCD}$ has not changed
1	$\overline{DCD}$ has changed state since the last read

Bit 4: Clear To Send (CTS)
CTS bit reflects the inverse of $\overline{CTS}$ pin. In loopback mode, CTS is the same as RTS in MCR (0xFCH).

Bit 5: Data Set Ready (DSR)
DSR bit reflects the inverse of $\overline{DSR}$ pin. In loopback mode, DSR is the same as DTR in MCR (0xFCH).

Bit 6: Ring Indicator (RI)
RI bit reflects the inverse of $\overline{RI}$ is the same as RTS in OUT1 (0xFCH).

Bit 7: Data Carrier Detect (DCD)
DCD bit reflects the inverse of $\overline{DCD}$ pin. In loopback mode, DCD is the same as OUT2 in MCR (0xFCH).

0xFFH – R/W: Scratchpad Registers

Scratchpad register is general purpose register for temporary storage. It does not control any function of the UART.

RCV Interrupts in FIFO Mode

The following conditions should be observed for RCV interrupts:

1. FIFO is enabled (FCR0 @ 0xFAH = 1), and Data Available Interrupt is enabled (IER0 @ 0xF9H = 1)
2. Data Available interrupt is set when FIFO reaches the trigger level, and it is reset when FIFO goes below the trigger level (see FIFO Control Register @ 0xFAH bits 6,7 for trigger level setting).
3. Interrupt Flags are set to indicate that data is available, and are reset to 0 whenever FIFO goes below trigger level.
4. Line Status interrupt is always higher priority than Data Available interrupt.
5. Data Available bit (LSR @ 0xFDH bit 0) is set to 1 after data is loaded from shift register to RCV FIFO, and reset to 0 when FIFO is empty.

Timeout Interrupts in FIFO Mode

The following conditions should be observed for Timeout interrupts:

1. FIFO is enabled (FCR0 @ 0xFAH = 1) and Data Available interrupt is enabled (IER0 @ 0xF9H = 1).
2. A timeout interrupt occurs because the timeout timer expires. It is cleared by reading RCV FIFO. Timeout timer duration is 4x character times. The timer is reset after a new character is received or after RCV FIFO is read.

Timeout timer duration is calculated as follows:

Char_Len = Start + data + Parity + Stop
Char_Time = Char_Len * RCLK
Timer duration = 4 * Char_Time

Example:
Assuming 9600 Baud, 7 bits/character, Start bit, 1 Stop bit, Odd Parity, 1.8432 MHz

Char_Len = 1 + 7 + 1 + 1= 10 bits

RCLK = 1.8423 / (16*12) = 9.6 KHz (104.17 μS)

Timer duration = 4 * 10 * 104.17 = 4.17 mS

The following conditions activates Timeout interrupts:

a. *FIFO is not empty, and*
b1. Data has not received for the last 4 character times, or
b2. FIFO has not been read for the last 4 character times.

XMIT Interrupts in FIFO Mode

For XMIT interrupts to occur, the following conditions must be met:

1. FIFO is enabled (FCR0 @ 0xFAH = 1) and Transmit Buffer Empty interrupt is enabled (IER1 @ 0xF9H = 1).
2. Transmit Buffer interrupt occurred because XMIT FIFO is empty. This interrupt can be cleared after writing to Transmit Buffer (0xF8H) or after reading Interrupt Flag register (0xFAH).

XMIT FIFO indication will be delayed under the following conditions:

- Transmit Buffer is empty (IER1 @ 0xF9H = 1), and
- XMIT FIFO has 1 byte or is empty since the last empty Transmit Buffer (IER1=1)

The delay will be 1 character time.

Polling in FIFO Mode

To put the UART in polled FIFO mode:

1. Set FCR0 (0xFA bit 0) to 1 and
2. Disables all interrupts (IER @ 0xF9 = 0)

Under polled FIFO mode, LSR (0xFD) becomes status of:

- LSR0 is set if RCV FIFO is not empty
- LSR1-LSR4 specifies error type
- LSR5 indicates Empty XMIT FIFO
- LSR6 indicates Empty XMIT FIFO and Empty Shift Register
- LSR7 indicates Error in RCV FIFO

Timeout condition or Trigger condition will not occur in polled FIFO operation.

Table 6A Summary of UART Registers (Part 1 of 2)

Bit No	0xFAH (R) Interrupt Flag	0xFAH (W) FIFO Control	0xFBH Byte Format	0xFCH MODEM Control	0xFDH Line Status
7	FIFO (1) Enable	RCV FIFO Trigger 1	Divisor Reg Access Bit	0	RCV FIFO Error (1)
6	0	RCV FIFO Trigger 0	Set Break	0	Transmitter Empty
5	0	Reserved	Forced Parity	0	Transmit Buffer Empty
4	0	Reserved	Even Parity Select	Loopback Mode	Break Interrupt
3	Int ID 2 (1)	DMA Mode Select	Parity Enable	Out 2	Framing Error
2	Int ID 1	XMIT FIFO Reset	# Stop Bits	Out 1	Parity Error
1	Int ID 0	RCV FIFO Reset	Word Length Select 1	RTS	Overrun Error
0	0 = Int Pending	FIFO Enable	Word Length Select 0	DTR	Data Available

Note (1): These bits are 0's in the Character mode.

Table 6B Summary of UART Registers (Part 2 of 2)

		DRAB/BFR7 = 0			DRAB/BFR7 = 1		
Bit	0xFEH	0xFFH	0xF8H R	0xF8H R	0xF9h	0xF8H	0xF9H
Bit No	Modem Status	Scratch	Rcv Buffer	Xmit Buffer	Interrupt Enable	Divisor (LSB)	(MSB)
7	Delta CTS	D7	D7	D7	0	D7	D15
6	Delta DSR	D6	D6	D6	0	D6	D14
5	Trailing Edge Ring Indicator	D5	D5	D5	0	D5	D13
4	Delta DCD	D4	D4	D4	0	D4	D12
3	CTS	D3	D3	D3	MODEM Status Interrupt	D3	D11
2	DSR	D2	D2	D2	Line Status Interrupt	D2	D10
1	RI	D1	D1	D1	Transmit Buffer Empty	D1	D9
0	DCD	D0	D0	D0	Data Available	D0	D8

Floppy Disk Interface:

The Floppy Interface consists of two blocks:

i) The System Interface.
ii) The Disk Clock and Data Recovery.

i) System Interface:

The system interface decodes the addresses, the control signals, and includes the registers required to implement PS/2 compatible Floppy Disk Controller (FDC), using the NEC D765/ 72065 or 8272 chip.

ii) Disk Clock and Data Recovery:

Clock Generator

The clock generator circuitry consists of a 24 MHZ fundamental mode crystal. Figure 3A shows the connections of the oscillator and the specifications of the crystal. The 24 MHZ clock is used to generate the CLK, (The FDC clock) and the WCK (FDC write clock).

Table 7 Data Rate Selection Table

RS1	RS0	Data Rate	CLK	WCK	RDW
0	0	500 K bps	8 MHz	1 MHZ	500 KHz
0	1	300 K bps	4.8 MHz	600 KHz	300 KHz
1	0	250 K bps	4 MHz	500 KHz	250 KHz
1	1	500 K bps	8 MHz	1 MHz	500 KHz

Resonant Frequency: 24.0 MHz
Frequency Accuracy: 0.1%
Crystal Operation: Fundamental Mode Parallel Resonance
Series Resistance: Rs = 8 Ohm
Motional Inductance: L = 2.2 mH
Motional Capacitance: C = 0.02 pF
Shunt Capacitance: Co=4.5 pF

Data Rate Control Logic

The 82C607 supports three standard data rates:

- 250 K bps
- 300 K bps
- 500 K bps

The data rate is software programmable by the system using the FDC configuration control register Register 03F7H.

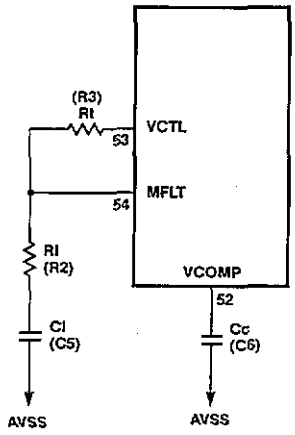


Figure 4. Phase Locked Loop Configuration

Data Separator

The data separator section consists of two analog phase locked loops; A reference PLL and the Main PLL, read data (RDD) and read data window (RDW) generators.

The function of main PLL is to recover the clock and data from the data stream so that the data may be decoded by the FDC. It tracks the drive motor rotational speed variation and pulse jitter. The second PLL adjusts itself to the power supply, temperature, process parameter variations and proportionally adjusts the main PLL.

The Phase Locked Loop (PLL) contains the phase/frequency comparator, charge-pump generator, loop filter and the Voltage Controlled Oscillator (VCO) as shown in Figure 5. For the reference PLL a simple capacitor C1 low pass filter is used. For the main PLL a more sophisticated second order external loop filter is used. Figure 4 shows the configuration of these filters.

Table 9 Data Separator Component Values

Symbol	Value	Description
(R2)	1.0 K	Loop resistor
(C5)	3300 pF	Loop Capacitor
(C6)	0.047 F	Compensation Capacitor
(R3)	3.9 K	Main Filter Resistor

During the idle period, VCOSYNC input is low and the main PLL locks onto the local reference clock. When the read operation begins and the VCOSYNC goes high the main PLL switches from reference clock to the incoming data stream. During an acquisition period (SYNC FIELD), the fast capture mode with low internal acquisition resistor (R_C)and high pumping current is used.

After lock the main PLL switches to tracking mode with high Rt and low pump current which reduces the loop gain. This method ensures that PLL will lock in fast (within 32 bit time) and tolerate 15% bit cell width jitter. At 500 Kbps bit rate a phase error of 380 ns or less (760 ns for 250 Kbps, 630 ns for 300 Kbps) will still keep PLL in lock.

Write Precompensation

The write pre-compensation circuit adjusts the data pulse position when writing to the disk. The purpose is to minimize bit shifts when reading data back from the diskette.

The FDC monitors the bit stream being sent to the 82C607, and depending on bit pattern activates the PS0 and PS1 signals. The 82C607 responds accordingly.

Precompensation Values

PS0	PS1	MFM
0	0	No Shift
0	1	125 ns Late
1	0	125 ns Early
1	1	Not Defined

Floppy Disk Controller Registers:

03F0H – Read Only: Status Register A.

Bit 7:	Interrupt Pending 0: No Interrupt pending. 1: Interrupt pending.
Bit 6:	2nd Drive Installed 0: Second drive installed 1: No second drive.
Bit 5:	Step 0: No step 1: Step
Bit 4:	Track 0 0: Current track is 0 1: Current track is not 0
Bit 3:	Head Select 0: Head 0 selected 1: Head 1 selected
Bit 2:	Index, status of INDEX signal 0: Index detected 1: No index detected
Bit 1:	Write Protect 0: Diskette is write protected 1: Diskette is not write protected
Bit 0:	Direction 0: Toward the inner track 1: Away from the inner track

03F1H – Read Only: Status Register B.

Bit 7-6:	Reserved, they are 0's.
Bit 5:	Drive Select 0: Drive 0 select 1: Drive 1 select
Bit 4:	Write Data A positive transition of WR DATA toggles this bit
Bit 3:	Read Data A positive transition of -RD DATA toggles this bit
Bit 2:	Write Enable 0: Write operation inactive 1: Write operation active
Bit 1:	Motor Enable 1 0: Drive 1 motor off 1: Drive 1 motor on
Bit 0:	Motor Enable 0 0: Drive 0 motor off 1: Drive 0 motor on

03F2H - Write Only: Digital Output Register.

Bit 7-6:	Reserved
Bit 5:	Motor Enable 1 0: Turn off motor of drive 1, if selected 1: Turn on motor of drive 1, if selected
Bit 4:	Motor Enable 0 0: Turn off motor of drive 0, if selected 1: Turn on motor of drive 0, if selected
Bit 3:	Reserved, should be 0
Bit 2:	FDC Select 0: FDC Software 1: FDC reset on software reset off
Bit 1:	Reserved, should be 0
Bit 0:	Drive Select 0: Drive 0 selected 1: Drive 1 selected

03F4H - Read Only: FDC Status Register.

Bit 7:	Request for Master
Bit 6:	Data Direction 0: Output mode, from CPU to FDC 1: Input mode, from FDC to CPU
Bit 5:	Non-DMA Mode 0: DMA mode 1: Non-DMA mode
Bit 4:	FDC Busy 0: Ready to accept command 1: Busy with command execution
Bit 3, 2:	Reserved
Bit 1:	Drive 1 Busy 0: Ready 1: Drive 1 is in seek mode
Bit 0:	Drive 0 Busy 0: Ready 1: Drive 0 is in seek mode

03F5H - Read/Write: FDC Data Register.

This I/O port is used to send commands, to receive status, and to receive/send data of the Floppy Disk Controller.

03F7H - Read Only: Digital Input Register.

Bit 7:	Diskette change 0: No diskette change 1: Diskette was changed
Bit 6-1:	Reserved, unknown when read.
Bit 0:	High Density diskette 0: High density 1: Low density

03F7H - Write only: FDC Configuration Control Register.

Bit 7-2:	Reserved, should be 0
Bit 1,0:	Data Rate Controls (DRC1, RDC0)

DRC1	DRC0	Data Rate
0	0	500 K bits/second
0	1	300 K bits/second
1	0	250 K bits/second
1	1	Reserved

Applications Diagram

Figure 5 gives a complete Logic diagram showing how the 82C607 can be used to interface to the system bus and to the floppy disk controller.

82C607 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Power Dissipation	P_D		1.0	W
Supply Voltage	V_{CC}	-0.5	7.0	V
Input Voltage	V_I	-0.5	V_{CC}+0.5	V
Output Voltage	V_O	-0.5	V_{CC}+0.5	V
Operating Temperature	T_{OP}	-25	85	°C
Storage Temperature	T_{STG}	-40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

82C607 Normal Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_A	0	70	°C

82C607 DC Characteristics

Parameter	Symbol	Min.	Max.	Units
Power Supply Current	I_{CC}		40	mA
Input High Voltage	V_{IH}	2.0	V_{CC}+0.5	V
for X1, FX1		3.5	V_{IH-MAX}	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Output Low Voltage	V_{OL}			V
under the following I_{OL} conditions:				
Output Low Current:	I_{OL}			
WDD, DRV0, DRV1, HIDENS		0.5		mA
IRQ3, IRQ4		24	0.4	mA
D0-D7		-8.0		mA
all other pins		2.4		mA
Output High Voltage	V_{OH}	2.4		V
under the following I_{OI} conditions:				
WDD, DRV0, DRV1, HIDDSK				µA
open drain		-400		µA
all other pins		-400		µA
Input Low Current	I_{IL}		-200	µA
Input High Current	I_{IH}		10	mA
Input Capacitance @ F_C = 1MHz	C_{IN}		15	pF
Output Capacitance @ F_C = 1MHz	C_{OUT}		15	pF

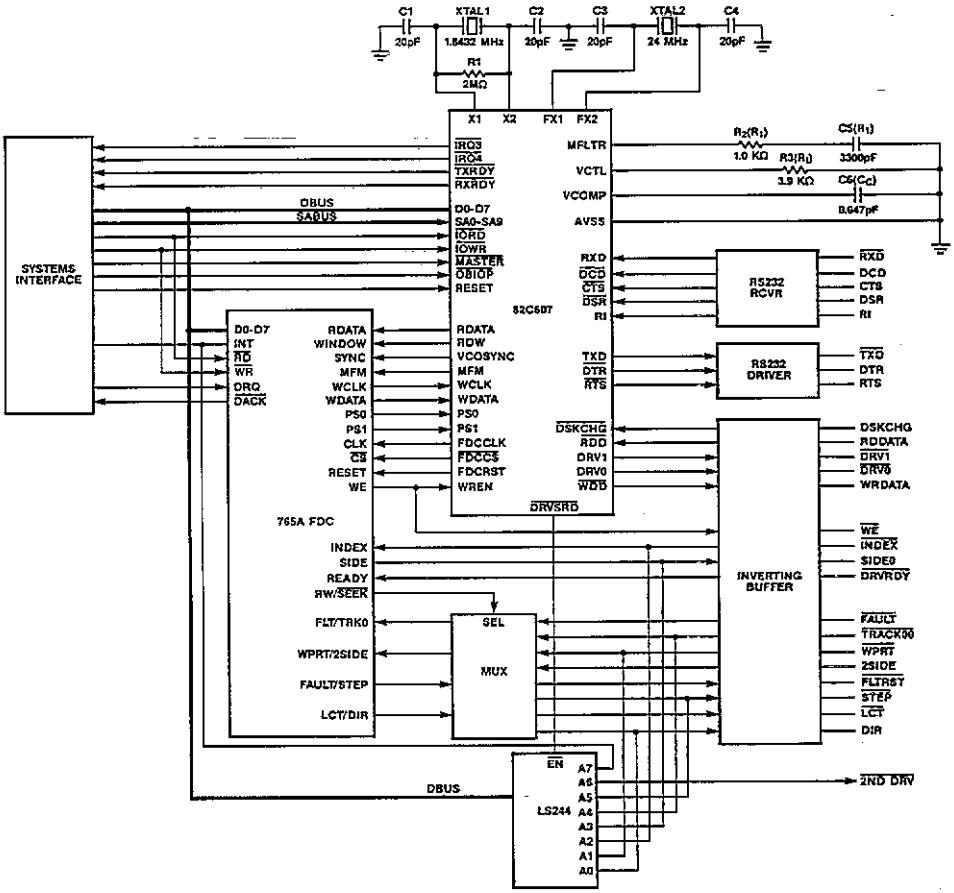


Figure 5. Applications Block Diagram Showing Interconnect Among Floppy Disk Controller, 82C607, Systems Interface and Floppy Disk.

82C607 AC Characteristics (under normal operating conditions)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

Sym	Parameter	Min	Typ	Max	Units
Host Interface Timing					
t1	$\overline{IORD}$, $\overline{IOWR}$ pulse width	100			ns
t2	Address Set-Up to Command Active	40			ns
t3	Address Hold from Command Active	20			ns
t4	Data Delay from $\overline{IORD}$ Active			100	ns
t5	Data Hold time from $\overline{IORD}$ Inactive	0			ns
t6	Data Setup time to $\overline{IOWR}$ Active	80			ns
t7	Data Hold time from $\overline{IOWR}$ Inactive	20			ns
t8	MASTER, OBIOP setup to $\overline{IORD}$/$\overline{IOWR}$ active	40			ms
t9	MASTER, OBIOP hold from $\overline{IORD}$/$\overline{IOWR}$ active	20			ms
t10	RESET inactive to $\overline{IORD}$/$\overline{IOWR}$ active	1			µs
t11	RESET pulse width	7			t21
Floppy Disk Interface Timing					
t12	RDW width				
	500K bps	0.9	1.0	1.1	µs
	300K bps	1.56	1.66	1.76	µs
	250K bps	1.9	2.0	2.1	µs
t13	RW, WCLK rise time, except for CLK			10	ns
t14	RW, WCLK fall time, except for CLK	10			ns
t15	RDATA width	6580		95	ns
t16	RDW to RDATA set up	15			ns
t17	RDW to RDATA hold	15			ns
t18	RDD width from drive	30		t12-50	ns
t19	CLK rise/fall time			10	ns
t20	CLK high time	40			ns
t21	CLK cycle time				
	500K bps	124.87	125	125.12	ns
	300K bps	208.12	208.33	208.54	ns
	250K bps	249.75	250	250.25	ns
t27	WCLK high width	t28/ 4-10	t28/4	t28/ 4+10	ns

82C607 AC Characteristics
(under normal operating conditions)(continued)

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%)

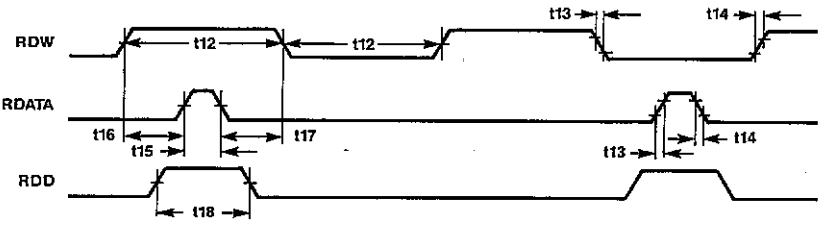
Sym	Parameter	Min	Typ	Max	Units
t23	CLK to WCLK delay	0		40	ns
t24	WDATA, WREN, PS1, PS0 delay from WCK	20		10*t23	
t25	WDATA data width	t21-50			ns
t26	WDD width	t24-10	t24	t24+10	ns
t28	WCLK cycle time				
	500K bps	9995	1000	1005	ns
	300K bps	1662	1667	1672	ns
	250K bps	1995	2000	2005	ns
UART Timing					
t29	$\overline{IOR}$ (LSR, RBR) to INTR low			1.0	µs
t30	$\overline{IOW}$ (TB) to INTR low			175	ns
t31	Initial TB $\overline{IOW}$ to INTR (6)	16		32	TCLK
t32	Initial INTR reset to TXD (6)	8		24	TCLK
t33	Stop to INTR (6)	8		8	TCLK
t34	$\overline{IOR}$ IFR to INTR low			250	ns
t35	$\overline{IOW}$ MCR to output			200	ns
t36	$\overline{IOW}$ MCR to INTR float			250	ns
t37	Modem input to INTR high			250	ns
t38	$\overline{IOR}$ MSR to INTR low			250	ns
t39	Start to TXRDY high (6)			8	TCLK
t40	$\overline{IOW}$ to TXRDY low			200	ns

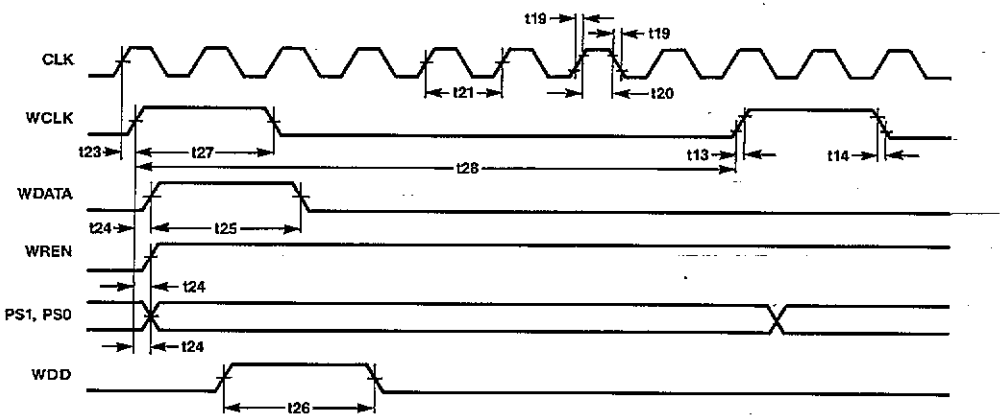
Loading: 60 pF for all pins

Conditions for AC measurements:

1. TTL high is 1.8 V and higher.
2. TTL low is .4 V and lower.
3. Rise/Fall time is between 0.6 and 1.8 V.
4. AC loading for all output is 100 pF to ground.
5. Input swings between 0.4 and 2.4 V with 3-10 ns rise/fall time.
6. TCLK frequency = UART OSC divided by Divisor Register Value.

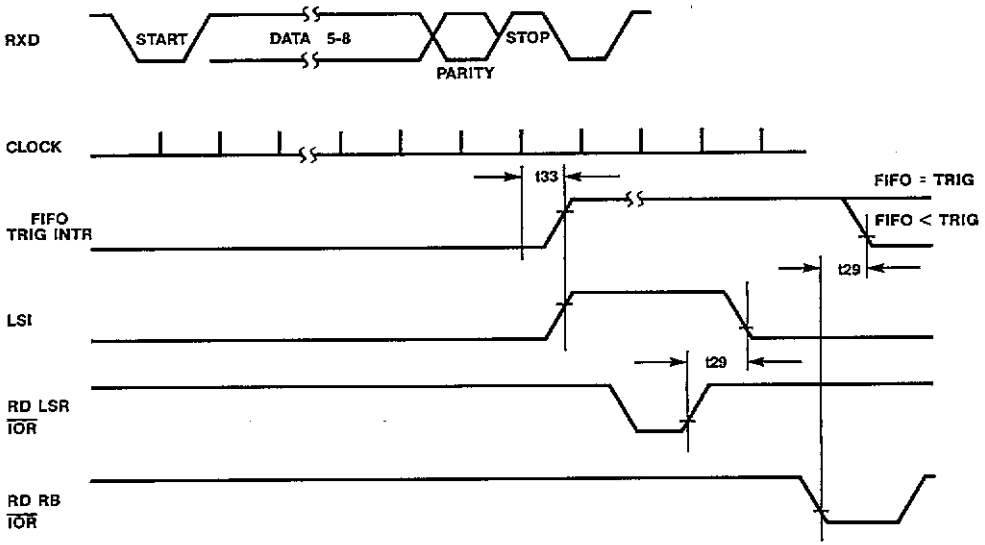
82C607 Timing Diagrams

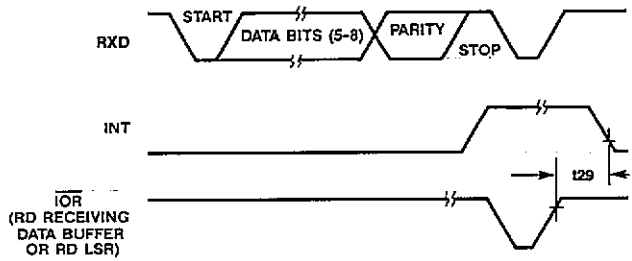




82C607 Timing Diagrams (continued)

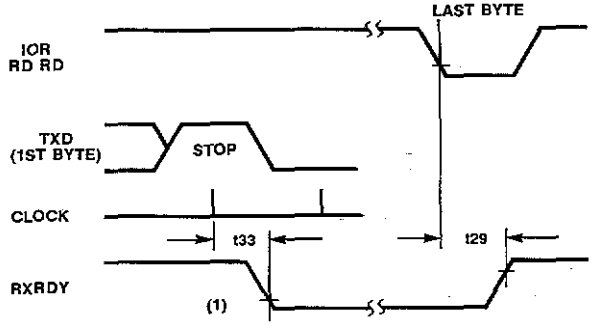
RCV FIFO 1ST BYTE (SET LSR0)





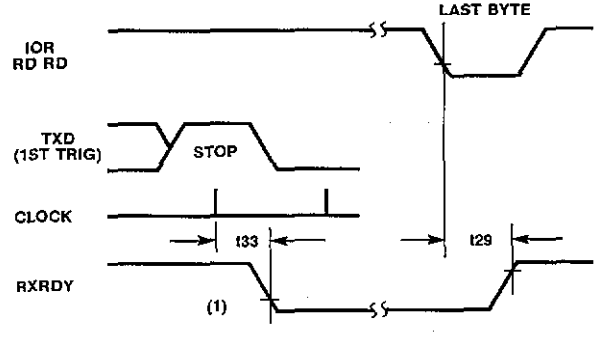
82C607 Timing Diagrams (continued)

FCR0 = 0 OR FCR0 = 1 & FCR3 = 0 (MODE0, INTERLEAVE DMA)



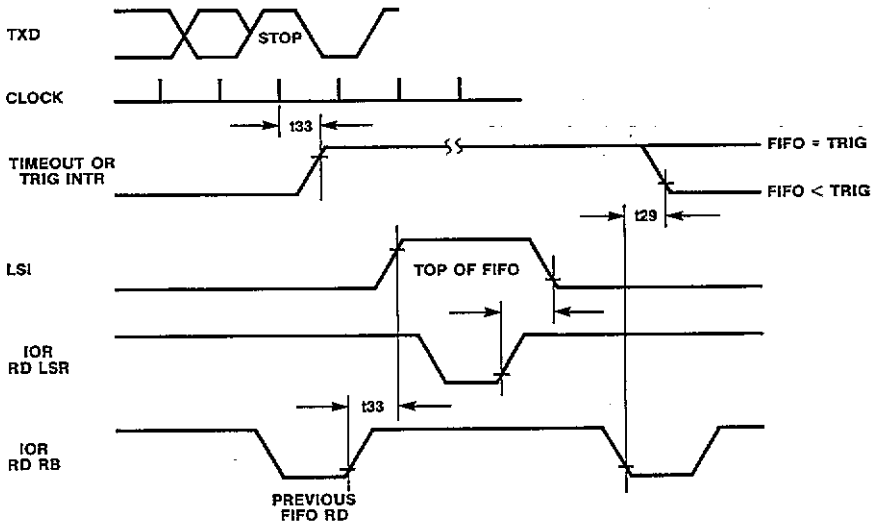
Note 1: If FCR0 = 1, t33 = 9 × RCLK

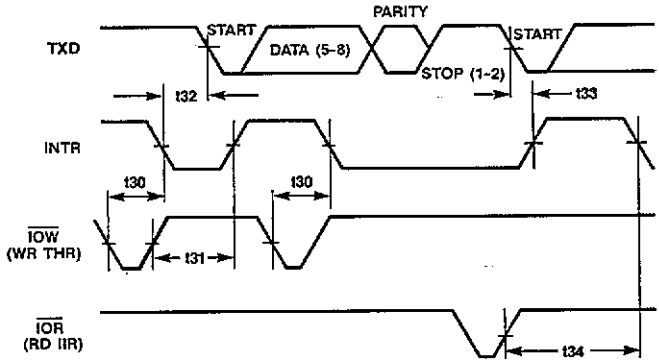
FCR0 = 1 & FC3 = 1 (MODE1, BURST DMA)



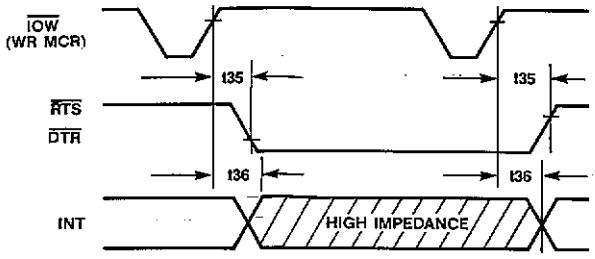
82C607 Timing Diagrams (continued)

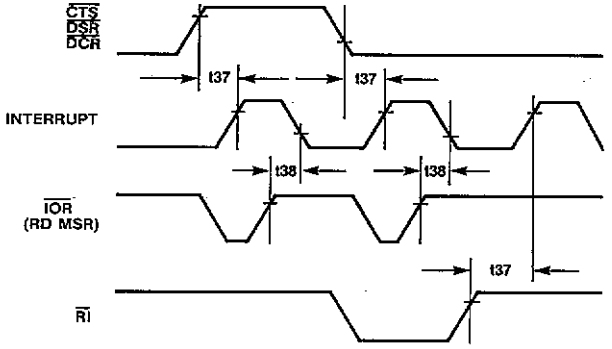
RCV FIFO NOT 1ST BYTE (LSR0 IS ALREADY SET)



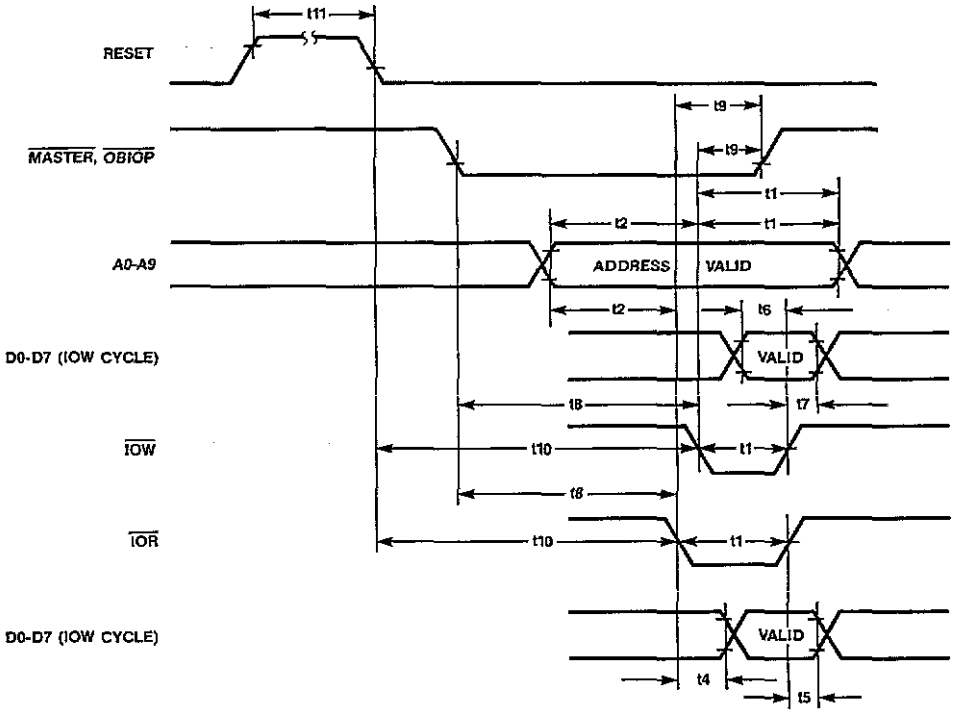


82C607 Timing Diagrams (continued)



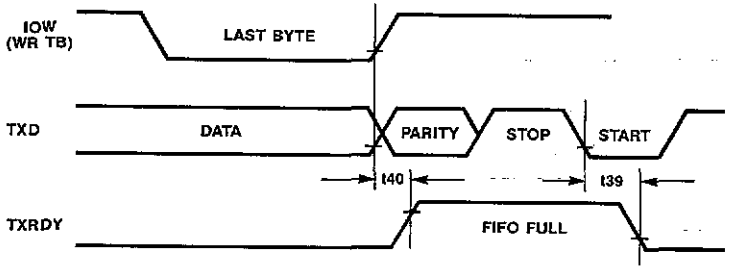


82C607 Timing Diagrams (continued)

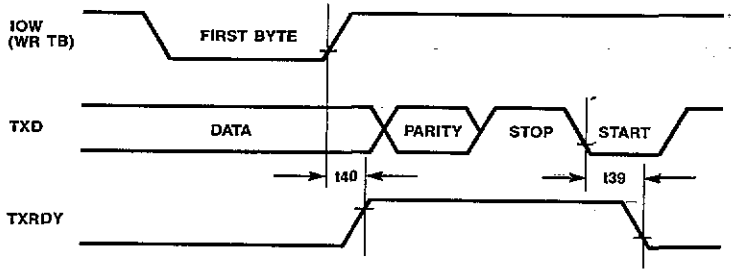


82C607 Timing Diagrams (continued)

FCR0 = 1 & FCR3 = 1 (MODE1, BURST DMA)



FCR0 = 0 OR FCR0 = 1 & FCR3 = 0 (MODE0, INTERLEAVE DMA)



Glossary of Terms:

BFR	Byte Format Register
BI	Break Interrupt
CDC	Data Carrier Detect
CDR	*Configuration Data Register*
CIR	Configuration Index Register
CTS	Clear To Send
DCTS	Delta Clear To Send
DDCD	Delta Data Carrier Detect
DDSR	Delta Data Set Ready
DR	Data Ready
DRAB	Divisor Register Access Bit
DSR	Data Set Ready
FCR	FIFO Control Register
FDC	Floppy Disk Controller
FE	Framing Error
IER	Interrupt Enable Register
IFR	Interrupt Flat Register
LSR	Line Status Register
MSR	MODEM Status Register
OE	Overrun Error
PE	Parity Error
POS	Programmable Option Select
RB	Receive Buffer
RI	Ring Indicator
RTS	Request To Send
TB	Transmit Buffer
TBE	Transmit Buffer Empty
TE	Transmitter Empty
TERI	Trailing Edge of Ring Indicator

List of Figures:

List of Tables:

CANADA DISTRIBUTORS

Electro Source, Inc.
Gateway Business Park
300 March Road
Suite 205
Kanata, Ontario
Canada K2K 2E2
Phone: 613-592-3214

Electro Source, Inc.
230 Galaxy Blvd.
Suite 303
Rexdale, Ontario
Canada M9W 5R8
Phone: 416-675-4490

Electro Source, Inc.
6600 TransCanada Hwy.
Suite 420
Pointe Claire, Quebec
Canada H9R 4S2
Phone: 514-630-7846

ITT Rae Electronics
300 North Riverfmede Road
Concord (Toronto) Ontario
Canada L4K 2Z4
Phone: 416-736-1144

Valtrie Marketing Inc.
910 Rowndtree Dairy Road
Unit 12
Woodbridge, Ontario
Canada L4L48
Phone: 416-851-0355

U.S. DISTRIBUTORS

ALABAMA
Quality Components
4900 University Square
Suite 20
Huntsville, AL 35816
Phone: 205-830-1881

Hall-Mark
4900 Bradford Drive
Huntsville, AL 35816
Phone: 205-837-8700

ARIZONA
Anthem
1727 East Webber Drive
Tempe, AZ 85281
Phone: 602-966-6600

Hall-Mark
4637 S. 36th Place
Phoenix, AZ 85040
Phone: 602-437-1200

CALIFORNIA
Anthem
20640 Bahama Street
Chatsworth, CA 91311
Phone: 818-700-1000

Anthem
One Oldfield Drive
Irvine, CA 92718-2809
Phone: 714-768-4444

Anthem
4700 Northgate Boulevard
Sacramento, CA 95834
Phone: 916-922-6800

Anthem
9369 Carroll Park Drive
San Diego, CA 92121
Phone: 619-453-9005

Anthem
1040 East Brokaw
San Jose, CA 95131
Phone: 408-295-4200

Hall-Mark
8130 Remmet Avenue
Canoga Park, CA 91304
Phone: 818-716-7300

Hall-Mark
6341 Auburn Blvd., Suite D
Citrus Heights, CA 95610
Phone: 916-722-8600

Hall-Mark
3878 Ruffin Rd., Suite B
San Diego, CA 92123
Phone: 619-268-1201

Hall-Mark
1110 Ringwood Ct.
San Jose, CA 95131
Phone: 408-946-0900

Hall-Mark
19220 S. Normandie Avenue
Torrance, CA 90502
Phone: 213-217-8400

Hall-Mark
14831 Franklin Avenue
Tustin, CA 92680
Phone: 714-669-4100

COLORADO
Anthem
373 Inverness Dr. South
Englewood, CO 80112
Phone: 303-790-4500

Hall-Mark
6950 S. Tucson Way
Englewood, CO 80112
Phone: 303-790-1662

CONNECTICUT
Lionex
170 Research Parkway
Meriden, CT 06450
Phone: 203-237-2282

Hall-Mark
33 Village Lane
Wallingford, CT 06492
Phone: 203-269-0100

FLORIDA
Hall-Mark
15302 Roosevelt Blvd.
Suite 303
Clearwater, FL 33520
Phone: 813-530-4543

Hall-Mark
7648 Southland Blvd.
Suite 100
Orlando, FL 32809
Phone: 407-855-4020

Hall-Mark
3161 S.W. 15th Street
Pompano Beach, FL
33069-4806
Phone: 305-971-9280

Quality Components
Florida
Phone: 800-241-0037

GEORGIA
Hall-Mark
6410 Atlantic Blvd.
Suite 115
Norcross, GA 30071
Phone: 404-447-8000

Quality Components
6145-B Northbelt Parkway
Norcross, GA 30071
Phone: 404-449-9508

ILLINOIS
Anthem
180 Crossen
Elk Grove Village, IL 60007
Phone: 312-640-6066

INDIANA
Hall-Mark
4275 W. 96th Street
Indianapolis, IN 46268
Phone: 317-872-8875
800-423-6638 (INDIANA)
800-772-0112 (KENTUCKY)

KANSAS
Hall-Mark
10809 Lakeview Drive
Lenexa, KS 66215
Phone: 913-888-4747

MASSACHUSETTS
Hall-Mark
6 Cook Street
Bilerica, MA 01821
Boston 617-935-9777
Phone: 617-667-0902

Lionex
36 Jonspin Road
Wilmington, MA 01887
Phone: 617-657-5170

MARYLAND
Hall-Mark/Baltimore
10240 Old Columbia Road
Columbia, MD 21046
Phone: 301-988-9800

Anthem
9020A Mendenhall Court
Columbia, MD 21045
Phone: 301-964-6640

MICHIGAN
Hall-Mark
38027 Schoolcraft Road
Livonia, MI 48150
Phone: 313-462-1205

MINNESOTA
Anthem
10025 Valley View Rd. #160
Eden Prairie, MN 55344
Phone: 612-944-5454

Hall-Mark
10300 Valley View
Suite 101
Eden Prairie, MN 55344
Phone: 612-941-2600

MISSOURI
Hall-Mark
13750 Shoreline Drive
Earth City, MO 63045
Phone: 314-291-5350

NORTH CAROLINA
Hall Mark
5237 N. Blvd.
Raleigh, NC 27604
Phone: 919-872-0712

Quality Components
3029-105 Stoneybrook Dr.
Raleigh, NC 27604
Phone: 919-876-7767

NEW JERSEY
Anthem
311 Route 46 West
Fairfield, NJ 07006
Phone: 201-227-7960

Hall-Mark
107 Fairfield Road Ste. 1B
Fairfield, NJ 07006
Phone: 201-575-4415

Hall-Mark
11000 Midlantic Drive
Mt. Laurel, NJ 08054
Phone: 609-235-1900

NEW YORK
Anthem
400 Oser Avenue
Hauppauge, NY 11788
Phone: 516-273-1660

Hall-Mark
101 Comac Loop
RonKonKoma, NY 11779
Phone: 516-737-0600

Hall-Mark
80 Rockwood Place
Rochester, NY 14610
Phone: 716-244-9290

OHIO
Hall-Mark
5821 Harper Road
Solon, OH 44139
Phone: 216-349-4632

Hall-Mark
400 E. Wilson Bridge Road
Suite 3
Worthington, OH 43085
Phone: 614-888-3313

OKLAHOMA
Hall-Mark
2500 No. Hemlock Lane
Broken Arrow, OK 74012
Phone: 1-800-327-9989

Quality Components
3158 S. 108th East Ave.
Suite 274
Tulsa, OK 74146
Phone: 918-664-8812

OREGON
Anthem
9705 SW Sunshine Ct. #900
Beaverton, OR 97005
Phone: 503-643-1114

PENNSYLVANIA
Lionex
101 Rock Road
Horsham, PA 19044
Phone: 215-443-5150

TEXAS
Hall-Mark
1221 Technology Blvd.
Austin, TX 78727
Phone: 512-258-8848

Hall-Mark
11420 Page Mill Road
Dallas TX 75243
Phone: 214-553-4300

Hall-Mark
8000 Westglen
Houston, TX 77063
Phone: 713-781-6100

Quality Components
4257 Kellway Circle
Addison, TX 75001
Phone: 214-733-4300

Quality Components
2120-M West Braker Lane
Austin, TX 78758
Phone: 512-835-0220

Quality Components
1005 Industrial Boulevard
Sugar Land, TX 77478
Phone: 713-240-2255

UTAH
Anthem
1279 West 2200 South
Suite A
Salt Lake City, UT 84119
Phone: 801-973-8555

UTAH (con't)
Hall-Mark
2265 S. 1300 West
West Valley, UT 84119
Phone: 801-972-1008

WASHINGTON
Anthem
5020 148th Avenue N.E.
Redmond, WA 98052
Phone: 206-881-0850

WISCONSIN
Hall-Mark
16255 W. Lincoln Avenue
New Berlin, WI 53151
Phone: 414-797-7844

FAR EAST DISTRIBUTORS

American MITAC Corporation
3385 Viso Court
Santa Clara, CA 95054
U.S.A.
Phone: 408-988-0258
Telex: 9103382201 MECTEL
Fax: 408-980-9742

AUSTRALIA
R&D Electronics
4 Florence Street
Burwood, Victoria
Australia 3125
Phone: 61-3-288 8911
Fax: 61-3-2889168

HONG KONG
Wong's Kong King Ltd.
8/F, Sime Darby Ind. Centre
420 Kwun Tong Road
Kwun Tong, Kowloon Hong Kong
Phone: 852 3-450121
Telex: 36810 WKKL HX
Fax: 852 3-7551128

Technology Research Co.
4/F, Block C, Watson's Estate
North Point, Hong Kong
Phone: 011852 5-8073323
Telex: 80554 TRC HX
Fax: 852 5-8073031

INDIA
Silicon Electronics
3350 Scott Blvd. #1201
Santa Clara, CA 95054
U.S.A.
Phone: 408-988-4408

ISRAEL
Hitek Ltd.
5 Haarad St.
TEL-AVIV, ISRAEL
Phone: 972 03/472005
Telex: 922371984HTK1
Fax: 972 3-493074

JAPAN
ASCII Corporation
SAT-I Bldg., 3F
2-20-4, Minami Aoyamo
Minato-ku
Tokyo 107 Japan
Phone: 03-470-0486
Telex: J28764ASCII
Fax: 03-740-0522

KOREA
Kortronics Enterprises
Rm. 307 9-Dong B-Block
#604-1 Guro-Dong, Guro-Gu
Seoul, Korea
Phone: 82 2 635-1043
Fax: 82 2 675-0514

SINGAPORE
Chartered Telmos Design PTE Ltd.
249 Jalan Boonlay
Singapore 261
Phone: 656607359
Fax: 652614913

TAIWAN, R.O.C.
Chips & Technologies, Inc.
Room A, 8th Floor
687 Ming Sheng East Road
Taipei, Taiwan, R.O.C.
Phone: 011 886 2 717-5595
Fax: 011 886 2 717-5646

Union Technology Corp.
3rd Floor
585 Ming Sheng East Rd.
Taipei, Taiwan, R.O.C.
Phone: 886-2-5018170
Fax: 886-2-5056609

EUROPEAN DISTRIBUTORS

BELGIUM
Auriema Belgium S.A./N.V.
Rue Brogniezstraat 172-A
B-1070 Bruxelles
Belgium
Phone: (02) 523-62-95
Telex: 21646
Fax: (02) 520-14-57

FINLAND
OY Fintronic AB
Melkonkatu 24A
SF-00210
Helsinki, Finland
Phone: 358 06926022
Telex: 857124224 FTRON SF
Fax: 358 0 674886

FRANCE
A2M
6. Av. du General De Gaulle
78150 Le Chesnay
France
Phone: 33 39.54.91.13
Telex: 842698376 F
Fax: 331 39.54.30.61

GERMANY
Rein Elektronik GmbH
Loetscher Weg 66
Postfach 5160
D-4054 Nettetal 1
West Germany
Phone: 49 (02153) 733-0
Telex: 841854203B REIN D
(or 854251B REIN D)
Fax: 49 02153-733110

ITALY
Maxel S.r.l.
Via C. Frova 34
20092 Cinisello Balsamo (MI)
Italy
Phone: 39 (02) 61.29.052
Telex: 352045 MOXMI I
Fax: 39 (02) 61.72.582

NETHERLANDS
Auriema Nederland B.V.
Doornakkersweg 26
5642 MP Eindhoven
Netherlands
Phone: 31 (0) 40-816565
Telex: 84451992
Fax: 31 (0) 40-811815

SPAIN
Compania Electronica de Tecnicas Aplicadas, S.A. (Comelta) (Main Branch)
Emilio Munoz, num. 41
Mave 1-1-2
28037 Madrid, Spain
Phone: 34-1-754-3001
Telex: 83142007 CETA E
Fax: 34-1-754-2151

SPAIN (cont'd)
Compania Electronica de Tecnicas Aplicadas, S.A. (Comelta)
Pedro IV, num. 84-5
planta
08005 Barcelona, Spain
Phone: 34-3-300-7712
Telex: 83151934 CETA E

SWEDEN (Nordic Countries)

Nordisk Elektronik A.B. (Main Branch)
Torshamnsgatan 39, 7th Floor
Box 36 S-164 93 Kista
Sweden
Phone: 46 08 703 46 47
Fax: 46 08 703 98 45
Telex: 85410547 NORTRON S

Nordisk Eletronik A/S
P.O. Box 123
Smedsvingen 4
1364 Hvalstad
Norway
Phone: 47 02 84 62 10
Fax: 47 02 84 65 45
Telex: 85677546 NENASN

Nordisk Elektronik A/S
Transformervej 17
DK-2730 Herlev
Denmark
Telex: 85535200 NORDEL DK
Phone: 45-284-20-00
Fax: 45-2-92-15-52

SWITZERLAND
DataComp
Silbernstrasse 10
CH-9853 Dietikon
Switzerland
Phone: 41 01 740 51 40
Telex: 827750 DACO
Fax: 41 1-7413423

UNITED KINGDOM
Katakana Limited
Manhattan House
Bridge Road
Maidenhead, Berkshire
SL6 8DB
United Kingdom
Phone: Maidenhead 44 (0628) 75641
Telex: 846775 KATKAN G
Fax: 44 (0628) 782812

CANADA SALES REPRESENTATIVES

Electro Source, Inc.
Gateway Business Park
300 March Road
Suite 205
Kanata, Ontario
Canada K2K 2E2
Phone: 613-592-3214

Electro Source, Inc.
230 Galaxy Blvd.
Suite 303
Rexdale, Ontario
Canada M9W 5R8
Phone: 416-675-4490

Electro Source, Inc.
6600 TransCanada Hwy.
Suite 420
Pointe Claire, Quebec
Canada H9R 4S2
Phone: 514-630-7846

ITT Rae Electronics
300 North Rivermede Road
Concord (Toronto) Ontario
Canada L4K 2Z4
Phone: 416-851-0355

Valtrie Marketing Inc.
910 Rowndtree Dairy Road
Unit 12
Woodbridge, Ontario
Canada L4L48
Phone: 416-851-0355

U.S. SALES REPRESENTATIVES

ALABAMA
The Novus Group, Inc.
2905 Westcorp Blvd.
Suite 120
Huntsville, AL 35805
Phone: 205-534-0044

ARIZONA
Reptronix
4625 So. Lakeshore Dr.
Tempe, AZ 85203
Phone: 602-345-4580

CALIFORNIA
Chips & Technologies, Inc.
18201 Von Karman Ave.
Suite 310
Irvine, CA 92715
Phone: 714-852-8721

Chips & Technologies, Inc.
2055 Gateway Place
Suite 220
San Jose, CA 95110
Phone: 408-437-8877

Magna Sales
3333 Bowers Avenue
Suite 251
Santa Clara, CA 95054
Phone: 408-727-8753

S.C. Cubed
468 Pennsfield Place
Suite 101A
Thousand Oaks, CA 91360
Phone: 805-496-7307

S.C. Cubed
17862 17th St. East Building
Suite 207
Tustin, CA 92680
Phone: 714-731-9206

COLORADO
Wescom Marketing, Inc.
4851 Independence Street
Suite 159
Wheat Ridge, CO 80033
Phone: 303-422-8957

FLORIDA
Dyne-A-Mark Corporation
500 E. Semoran Blvd. Ste. 15A
Casselberry, FL 32707
Phone: 407-831-2822

Dyne-A-Mark Corporation
573 South Duncan Avenue
Clearwater, FL 33516
Phone: 813-441-4702

Dyne-A-Mark Corporation
1001 Northwest 62nd Street
Suite 108
Ft. Lauderdale, FL 33309
Phone: 305-771-6501

GEORGIA
Chips & Technologies, Inc.
136 Mae Belle Way
Lawrenceville, GA 30244
Phone: 404-921-0292

The Novus Group, Inc.
4556 Canda Drive
Liburn, GA 30247
Phone: 404-381-1015

ILLINOIS
Chips & Technologies
450 E. Devon Ave.
Suite 280
Itasca, IL 60143
Phone: 312-250-0075

Micro-Tex, Inc.
2400 West Central Road
Hoffman Estates, IL 60196
Phone: 312-382-3001

INDIANA
Giesting & Associates
101 East Carmel Drive
Suite 210
Carmel, IN 46032
Phone: 317-844-5222

Giesting & Associates
1246 Sowles Bay Road
RR#2 Box 505
Angola, IN 46703
Phone: 219-833-1960

MARYLAND
Micro-Comp, Inc.
1421 South Caton Ave.
Baltimore, MD 21227-1082
Phone: 301-644-5700

MASSACHUSETTS
Chips & Technologies, Inc.
One Wall Street
Burlington Office Park
Burlington, MA 01803
Phone: 617-273-3500

Mill-Bern Associates, Inc.
2 Mack Road
Woburn, MA 01801
Phone: 617-932-3311

MICHIGAN
Giesting & Associates
5654 Wendzel Drive
Coloma, MI 49038
Phone: 616-468-4200

Giesting & Associates
34441 Eight Mile Road
Suite 113
Livonia, MI 48152
Phone: 313-478-8106

MINNESOTA
High Technology Sales Assoc.
11415 Valley View Road
Eden Prairie, MN 55344
Phone: 612-944-7274

NEW JERSEY
T.A.I.
12 South Blackhorse Pike
Bellmawr, NJ 08031
Phone: NJ: 609-933-2600
PA: 215-627-6615

NEW MEXICO
Reptronix
237-C Eubank Blvd. NE
Albuquerque, NM 87123
Phone: 505-292-1718

NEW YORK
ERA, Incorporated
351 Veterans Memorial Hwy.
Commack, NY 11725
Phone: 516-543-0510

L-Mar Associates
349 W. Commercial St.
Suite 2285
Rochester, NY 14445
Phone: 716-381-9100

NORTH CAROLINA
The Novus Group, Inc.
5337 Trestlewood Lane
Raleigh, NC 27610
Phone: 919-833-7771

OHIO
Giesting & Associates
2854 Blue Rock Road
P.O. Box 39398
Cincinnati, OH 45239
Phone: 513-385-1105

Giesting & Associates
26250 Euclid Avenue
Suite 521
Cleveland, OH 44132
Phone: 216-261-9705

OREGON
L-Squared Limited
15234 NW Greenbrier Pkwy.
Beaverton, OR 97006
Phone: 503-629-8555

PENNSYLVANIA
Giesting & Associates
471 Walnut Street
Pittsburgh, PA 15238
Phone: 412-963-5832

TEXAS
OM Sales
13915 Burnet Road
Suite 301
Austin, TX 78728
Phone: 512-388-1151

Chips & Technologies, Inc.
15415 Katy Freeway
Suite 209
Houston, TX 77094
Phone: 713-579-9633

OM Sales
10500 Richmond Avenue
Suite 115
Houston, TX 77042
Phone: 713-789-4426

OM Sales
2323 N. Central Expwy.
Suite 150
Richardson, TX 75080
Phone: 214-690-6746

UTAH
Wescom Marketing, Inc.
3499 S. Main, Suite 5
Salt Lake City, UT 84115
Phone: 801-269-0419

WASHINGTON
L-Squared Limited
105 Central Way
Suite 203
Kirkland, WA 98033
Phone: 206-827-8555

WISCONSIN
Micro-Tex, Inc.
22660 Broadway
Suite 3B
Waukesha, WI 53186
Phone: 414-542-5352

NOTES

NOTES

NOTES

NOTES

NOTES

Chips and Technologies, Incorporated
3050 Zanker Road, San Jose, CA 95134 408-434-0600 Telex 272929 CHIP UR