64200
(Wingine™)

High Performance
'Windows™ Engine'

Data Sheet

July 1992

P R E L I M I N A R Y

CHIPS®

CHIPS®

64200 (Wingine™)
High Performance 'Windows™ Engine'

■ Cost effective Windows™ Accelerator

■ Interfaces directly with X86 SX/DX/DX2 Systems

■ Interfaces directly with ISA486 CHIPSet

■ High performance achieved via direct access frame buffer Memory Bus Architecture

■ Direct linear mapping of entire video memory anywhere in system memory space

■ Flexible video memory configurations: 8, 16, or 32-bit wide VRAM (256KB–2MB)

■ Supports the following display modes with 1MB of VRAM:

  • 8bpp up to 1024x768 (interlaced or non-I/L)
  • 16bpp up to 800x600 (with Sierra RAMDAC)
  • 24bpp up to 640x480 (with Bt484 or equiv)

■ Supports higher resolution display modes with 2MB VRAM:

  • 8bpp up to 1280x1024 (non-interlaced)
  • 16bpp up to 1024x768 (interlaced or non-I/L)
  • 24bpp up to 800x600 (non-interlaced)

■ Highly integrated design (non-multiplexed system bus, direct bus drive, minimum external glue logic)

■ All video shifting performed on-chip to allow use of low-cost VGA RAMDACs (allows video rates to 80 MHz)

■ Compatible with high-resolution color palette RAMDACs such as the Bt484 and TI 34075 having separate 8-bit and 32-bit parallel inputs for direct connection to VRAM serial data (allows video rates to 135 MHz)

■ Full VGA compatibility

■ Interfaces directly with the 82C481 True-Color Graphics Accelerator

■ Direct interface to 82C404 programmable clock

■ In-Circuit Testability Features

■ Small low-cost package: EIAJ-standard 160-pin plastic flat pack

■ Chip pinouts optimized for PCB layout
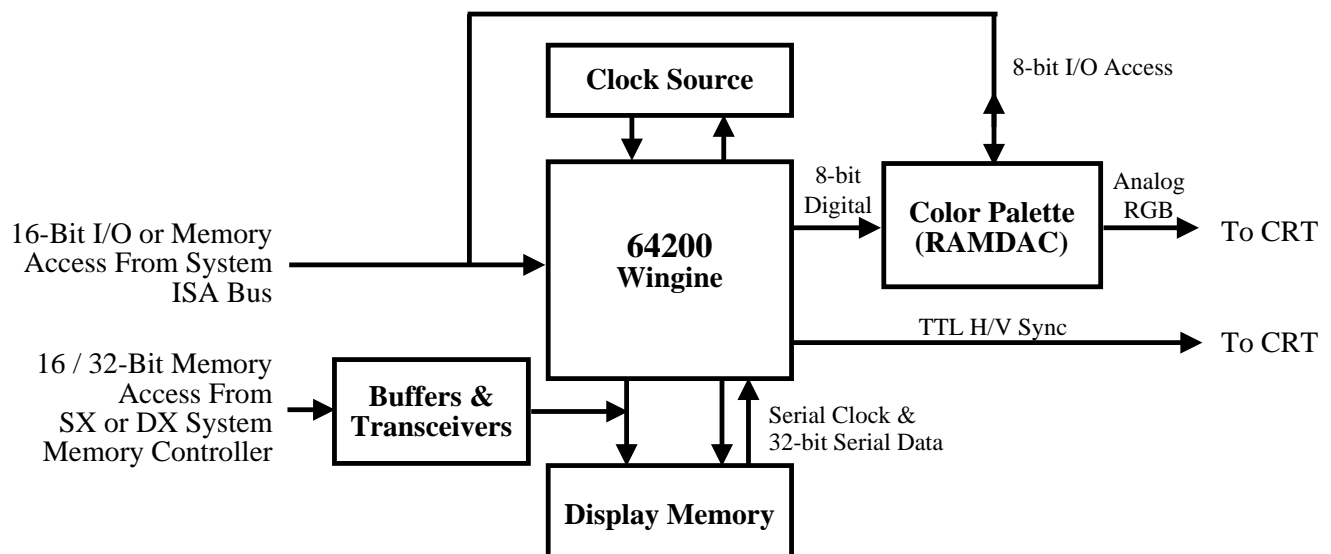
System Diagram - Memory Bus Architecture

Revision History

Revision	Date	By	Comment
0.2	10/10/91	DH	Changed pinouts Modified & expanded application schematics Updated register bit definitions Added Introduction section Added Electrical specifications section Added support for Bt484 & MU color palette chips
0.21	11/4/91	DH	Changed Bt484 application schematic hookup Added 82C481 connection application schematic
0.3	11/19/91	DH	Rewrote introduction section Added 'NDA Required' disclaimer for protection until chip announcement Changed part number for chip to 64200 Changed chip pinouts to group P0-7, PCLK, and BLANK/ together Moved TOUT from VSYNC to VGA pin to keep next to TCLK Added NCLK output on pin 98 (moved DSF to reserved pin 137) Memory interface now remains tristated until 1st write to Master Ctrl reg Inverted Master Control register bit-6 (XREQ/ Divide control) Added Master Control register bit-7 (XREQ/ Direction control) Added XR3D bit-4 (word swap) for selection of 16-bit shiftout from CD (to allow DX 512K option for lower half of VRAMs to be optional) Moved the memory configuration bit from XR01 bit-3 to XR3D bit-5 Fixed the documentation to reflect 2MB VRAM support Added description of XR28 Video Interface Register
0.4	2/12/92	ST/DH	Added missing register definitions Increased drive specifications on various pins Swapped DSF and WE/ pinouts (documentation error) Fixed bus reference specifications Changed electrical specs for 80MHz video frequencies Fixed bit definitions (XR03[6], XR3D[5]) and added MEM/ config bit Added 64201 interface diagrams and updated 481 intfc block diagram
0.5	4/92	VS	Added table of supported resolutions Added information on interfacing to CS4021 system chipset Added more information on interfacing to CS82310 system chipset Added Winglue information Removed XR02 bits 0,2 (always 16-bit access) Removed XR04 bits 6-7 (not implemented) Added XR3D bit 3 (481 mode) Removed XR44 (not implemented) Removed generic bus interface timing
0.6	7/92	VS/ST	Modified Memory Timing Removed XR03 bits 2-3 (not implemented) Added description of how to support external VGA Release Data Sheet to Marcom

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Introduction

The concept behind the 64200 'Windows Engine' (Wingine) is the implementation of video display memory as a bank (or banks) of system memory. The idea is that the system CPU (typically at least a 386-class processor) can manipulate pixels on the screen quickly if the display memory bottleneck is removed. The video memory is accessed directly by the system CPU as a frame buffer through the VRAM random access port while the display is continuously being refreshed via the VRAM serial data port.

Wingine is basically a standard 16-bit VGA with extensions. The primary extension is to allow the system to directly access VRAM display memory as system memory. Wingine operates in two modes: 'Windows Acceleration' mode and 'VGA' mode. In 'VGA' mode, Wingine drives the video memory. Wingine uses the VRAMs as DRAMs in VGA mode (no special capabilities of the VRAMs are required or used); all VGA operations are implemented via the VRAM random access port. (Wingine pinouts are defined such that future implementations may be extended to take advantage of the VRAM serial port in VGA mode.) In 'Windows Acceleration' mode, the VRAM random access ports are driven by the system memory controller; the Wingine chip does not have access to the VRAMs, but performs all VRAM serial data shift operations and provides HSYNC and VSYNC for the display monitor. In 'Windows Acceleration' mode, the system performs all data transfer operations based on information provided from the Wingine chip.

The result is very high performance, since the entire random port bandwidth is available for CPU access and the VRAMs may always be accessed at full memory speed. In addition, memory may be accessed at the full width of system memory (16 or 32 bits). The frame buffer may be accessed as a linear array of pixels (in 'packed-pixel' format) anywhere in the system memory space.

Another major advantage is the ability to accept 32 bits of serial data from the VRAMs and convert it into an 8-bit video data stream compatible with a standard low-cost VGA RAMDAC. This capability removes the <u>requirement</u> for an expensive RAMDAC, allowing implementation of cost effective, high performance graphics system.

Wingine directly supports 4bpp (nibble) and 8bpp (byte) modes <u>with standard VGA 8-bit RAMDACs</u> which are available up to 80 MHz. 16bpp mode may be supported with an extended capability RAMDAC such as a Sierra SC11482, 483, or 484. Wingine can also support various types of high performance and extended capability RAMDACs with 32-bit parallel data input ports. These RAMDACs typically support pixel rates to 135 MHz and modes of 1bpp, 2bpp, 4bpp, 8bpp, 16bpp, and / or 24bpp. All known RAMDACs support these modes lsb first (e.g., nibble modes shift the first pixel out of bits 0-3 of the first byte in memory, the second pixel out of bits 4-7, etc). All of these modes up to 16bpp are also supported in the XGA ('lsb first' is referred to as 'Intel order' in IBM's XGA documentation). Therefore, for compatibility, pixel shift order is always lsb first and <u>pixels are always stored in Wingine memory as a linear array of n-sized elements starting with bit-0 of byte 0</u>.

DISPLAY MEMORY CONFIGURATIONS

The VRAM frame buffer may be implemented with two, four, or eight 256Kx4 (1Mb) or two or four 256Kx8 (2Mb) VRAMs, accessed as 1 bank of 32-bit memory in 386 DX or 486 systems or as 2 banks of 16-bit memory in 386 SX systems. This provides 1MB of display memory, which is adequate for support of 1024x768 at 8bpp (256-color). This amount of memory, using split buffer VRAMs and a Sierra RAMDAC (or equivalent), will also support 16bpp modes up to 800x600.

Wingine allows 512KB upgradable to 1MB of display memory in 386 <u>SX</u> (16-bit) systems by <u>optionally populating the upper bank</u>. The 512KB configuration supports 1024x768 at 4bpp (16-color) and 640x480 at 8bpp (256-color). If word interleaving is done in 16-bit systems, the memory map is identical between 16 and 32 bit systems (and the same drivers may be used). Wingine is designed to also handle non-word-interleaved 2 bank 16-bit memory maps, if word interleaving is not implemented by the system.

If <u>256Kx4 VRAMs</u> are used, 512KB of display memory (upgradable to 1MB) may also be implemented by <u>optionally populating the upper nibble</u> of each byte. In this configuration, the

system would always manipulate display memory assuming 8bpp; screen display would be 16-color with 4 VRAMs installed and 256-color with 8 VRAMs installed (the RAMDAC pixel mask register would be set to mask out the upper 4 bits of video data in 4-VRAM mode).

Wingine will support 24bpp modes up to 640x480 in 1MB configurations, but a RAMDAC must be used which allows packing R, G, & B every 3 bytes and AT &T 206491 RAMDACs. The Bt482 support this type of pixel packing. However Wingine will support 24bpp modes up to 640x400 if the RAMDAC ignores one byte out of every four. Many 32-bit input RAMDACs (Bt484 / 485, TI 34075 / 34076) support 24bpp mode in this fashion (by ignoring the upper byte of the 32-bit input). Since only one pixel is input to the RAMDAC every shift clock, the maximum pixel rate in this mode is limited by the VRAM shift clock rate: 33 MHz for '-10' (100nS) VRAMs and 40 MHz for '-8' (80nS) VRAMs).

Wingine supports interlaced displays at 1024x768 resolution. Wingine maintains a linear address mapping scheme so that software drivers are independent of whether the display is interlaced or not.

Wingine is compatible with VRAM memory configurations larger than 1MB, if implemented by the system as either multiple banks of 32-bit memory using '256K x N' VRAMs or single banks of 32-bit memory using '512K x N' or '1M x N' VRAMs. These configurations would typically be implemented with 32-bit input extended-function, high-performance RAMDACs and support high resolutions (e.g., 1280x1024) and/or high-color modes (16bpp and 24bpp).

SYSTEM SUPPORT REQUIREMENTS

To implement a Wingine-based Graphics sub-system, the system memory controller must be able to map a bank (or banks) of VRAMs into the system memory space. The memory controller must be aware of the differences between VRAMs and DRAMs for random access port control (the VRAM serial port is controlled by Wingine). Wingine support exists in the CS4021 486 CHIPSet. Chips and Technologies plans to provide Wingine support in all future Systems Logic CHIPSets™ and SYSTEMSets™ to allow Wingine to interface directly to those products. Extensions are also planned for all current CHIPSets™ and SYSTEMSets™.

MEMORY INTERFACE

Two types of memory subsystems can be designed with Wingine. In the first type, 2 or 4 DRAMs can be used for VGA compatible modes. For Wingine modes, separate VRAMs are used. In this implementation, VGA memory and 'Wingine mode' memory are separate. No external buffers are required to isolate the two memory buses.

In the second type of memory subsystem, a shared memory bus is used for a cost effective implementation. In this case, only VRAMs are used. In VGA mode, Wingine controls video memory. In 'Wingine' mode, the system memory controller has control over video memory. External buffers are required to isolate the two buses - the Wingine memory bus and the system memory bus. Refer to the following section for additional details.

Wingine can support up to 2 Mbytes of display memory. It can also support 256 Kbyte and 512 Kbyte memory configurations. The following table shows a matrix of resolution and memory requirements. This table assumes a shared memory architecture. It is **important** to buffere SCLK with a fast buffer when 2 Mbyte configuration is used.

	Resolution	Memory
VGA Mode	640x480 16 Colors	256 Kbytes
	800x600 16 Colors	256 Kbytes
	640x480 256 Colors	512 Kbytes
	1024x768 16 Colors	512 Kbytes
Wingine Mode	640x480 256 Colors	512 Kbytes
	800x600 256 Colors	512 Kbytes
	1024x768 256 Colors	1 Mbyte
	640x480 16 bits/pixel	1 Mbyte
	640x480 24 bits/pixel	1 Mbyte
	800x600 16 bits/pixel	1 Mbyte *
	1024x768 16 bits/pixel	2 Mbyte**
	1280x1024 256 colors	2 Mbytes

 * Requires Split - Buffer VRAMs.
** Requires Bt484 compatible DAC.

RECOMMENDED MEMORY CHIPS

	Standard	Split Buffer
Micron		MT42C4256
Mitshubishi		442256
Toshiba	524256	
NEC	42273	

SYSTEM INTERFACE

The 64200 Wingine chip is tightly coupled to system chipsets from Chips and Technologies. This tight coupling between Wingine and the system chipset results in a very high performance Windows architecture. The Wingine graphics controller can be interfaced to two high performance CHIPSets from Chips & Technologies - the CS4021 and CS82310 chipsets.

Wingine/CS4021 Interface

CS4021 (also called the ISA486 chipset) is CHIPS' next generation high end chipset. This chipset can support both 386 and 486 designs. Special features are provided in the ISA486 chipset for a simple and elegant interface to the Wingine subsystem. Figure 1 and Figure 2 show the Wingine/ISA486 interface.

Figure 1 shows the data path between the ISA486 memory controller and Wingine memory. In VGA mode, Wingine interfaces to the ISA bus. In this mode, display memory is controlled by Wingine. The CPU accesses video memory through Wingine. In VGA mode, up to 512 Kbytes of video memory is supported. In this mode, the VGA pin from Wingine is high to isolate the data bus from ISA486. As Wingine has 17 address lines, it is necessary to qualify memory read and memory writes with a valid VGA address. The external PAL decodes the upper address (LA17 -LA23) from the ISA bus for a valid VGA access (0A0000 - 0BFFFFh) and qualifies the MEMR/ and MEMW/ signals to Wingine.

When the 64200 is switched to 'Windows Accelerator' (or Wingine) mode, the ISA486 chipset can access video memory directly for much higher video performance. In this mode up to 2 Mbytes of display memory can be supported. Figure 1 shows a 1MB implementation. In 'Wingine' mode the full 32 bit memory bus can be utilized for accessing display memory. In this mode, Wingine tristates its memory bus and pulls the VGA pin low. The two data buffers on the upper 16 bits of the memory bus are enabled allowing the ISA486 memory controller to access video memory directly. The direction of the data buffers is controlled by an external signal derived from the RAS/, CAS/, and WE/ signals from ISA486. For Write operations, data is driven onto the video memory data lines. During read cycles, the buffers are turned around to drive the data onto the system memory bus.

The XREQ/ signal from Wingine is used to request a transfer cycle from the system memory controller. The memory controller will perform a transfer cycle to the video RAMs when XREQ/ goes active. Figure 2 shows the interface for address and control

lines. During VGA modes, the ISA486 memory controller is isolated from video memory by pulling the VGA pin high. The addresses and control signals for video memory are generated by Wingine.

In 'Wingine' mode, the VGA pin goes low and the system memory controller drives the address and control lines. The Wingine memory bus is tristated during this mode.

Wingine/CS82310 Interface

The CS82310 (also called the PEAK/DM chipset) is another high end chipset that can support Wingine. To simplify the interface to PEAK/DM, a companion chip "64201 (Winglue)" has been designed. Winglue interfaces between PEAK/DM and Wingine.

Figure 3 shows the data bus interface for PEAK/DM. The external data buffers are controlled by Winglue. Wingine uses the VGA pin to indicate if it is in VGA or 'Wingine' mode. In VGA mode, the VOE/ pin from Winglue is high thus tristating the data buffers on the upper data bus. For a 16 bit VGA interface, the external PAL generates MEMCS16/ for the AT bus. The same signal is used by Winglue to qualify VMEMR/ and VMEMW/ to Wingine for valid VGA cycles.

In 'Wingine' mode, Winglue pulls the VOE/ pin low to enable the data buffers. The MDINP pin from Winglue controls the direction of the data buffers for read/write cycles. Winglue performs the transfer cycles to the video RAMs based on the XREQ/ input from Wingine. Winglue also arbitrates with the system memory controller for control of the memory bus during transfer cycles using the HLD/HLDA protocol.

Figure 4 shows the interface for address and control signals. During VGA mode, the VOE/ pin is high to disable the address/control buffers. In 'Wingine' mode, VOE/ goes low to allow the memory controller to drive the address and control lines. Wingine tristates its memory bus during 'Wingine' mode.

EXTERNAL VGA SUPPORT

An external VGA can be supported in Wingine system. The motherboard Wingine can be disabled by disconnecting the AEN signal to Wingine. This will prevent Wingine from being initialized. An external VGA can then reside in the system without any conflict with Wingine. MEMCS16/ from the Wingine subsystem should also be disabled to allow 8 bit VGA cards. Two jumpers can be used on the AEN and MEMCS16/ lines. Refer to Figure 1 and Figure 3.
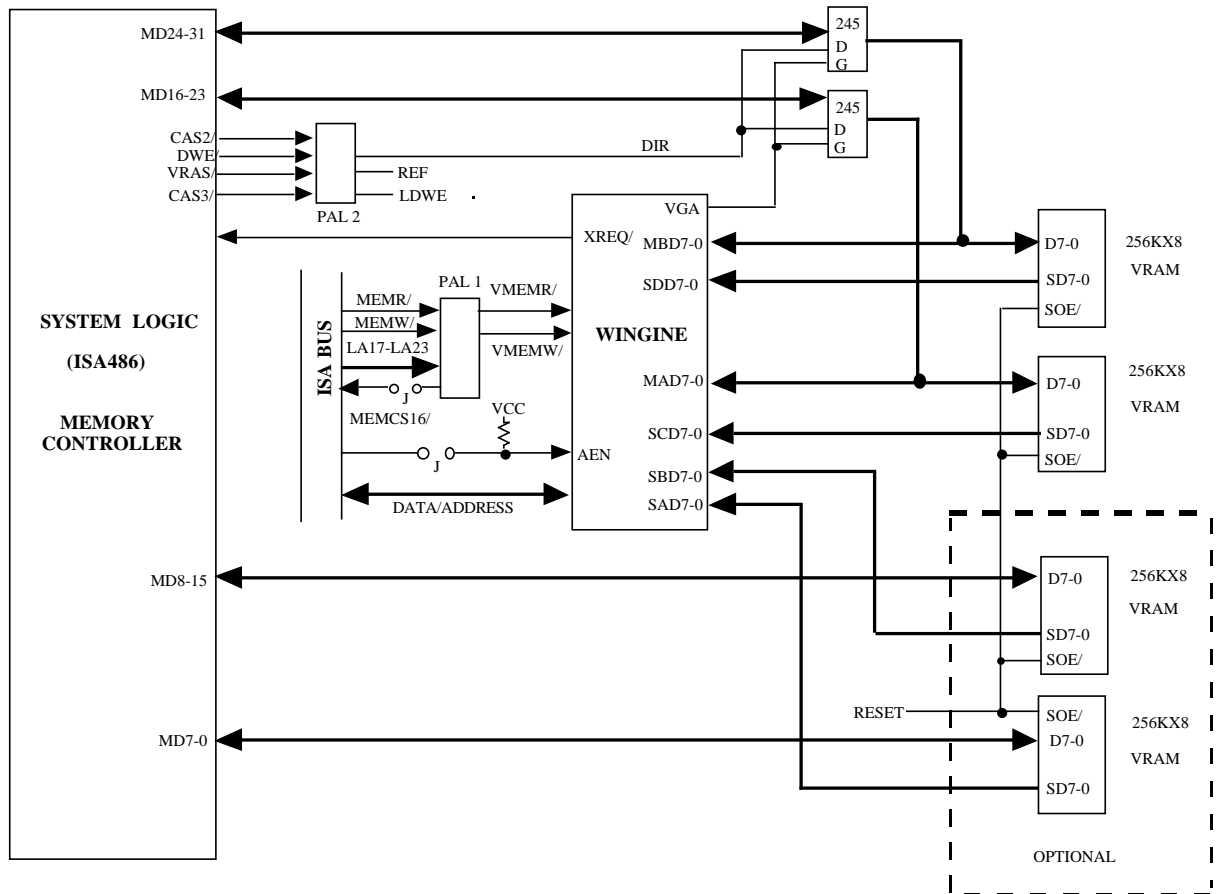
Figure 1 - Wingine Interface to ISA486 (Data)

PAL EQUATIONS:

PAL 1

RAMADD = !LA23 & !LA22 & !LA21 & !LA20 & LA19 & !LA18 & LA17;

VMEMR = MEMR & RAMADD;

VMEMW = MEMW & RAMADD;

MEMCS16.OE = RAMADD;

MEMCS16 = 'B' 1;

PAL 2

CASS   =   CAS2 # CAS3;

REF   =   CAS2 & !VRAS # REF & CAS2 # REF & VRAS;

LDWE   =   DWE & !CASS # LDWE & CASS # LDWE & DWE;

DIR   =   CASS & VRAS & !REF & !LDWE;

Where

REF - Indicates a valid memory refresh cycle

LDWE - Latched write enable with CAS.
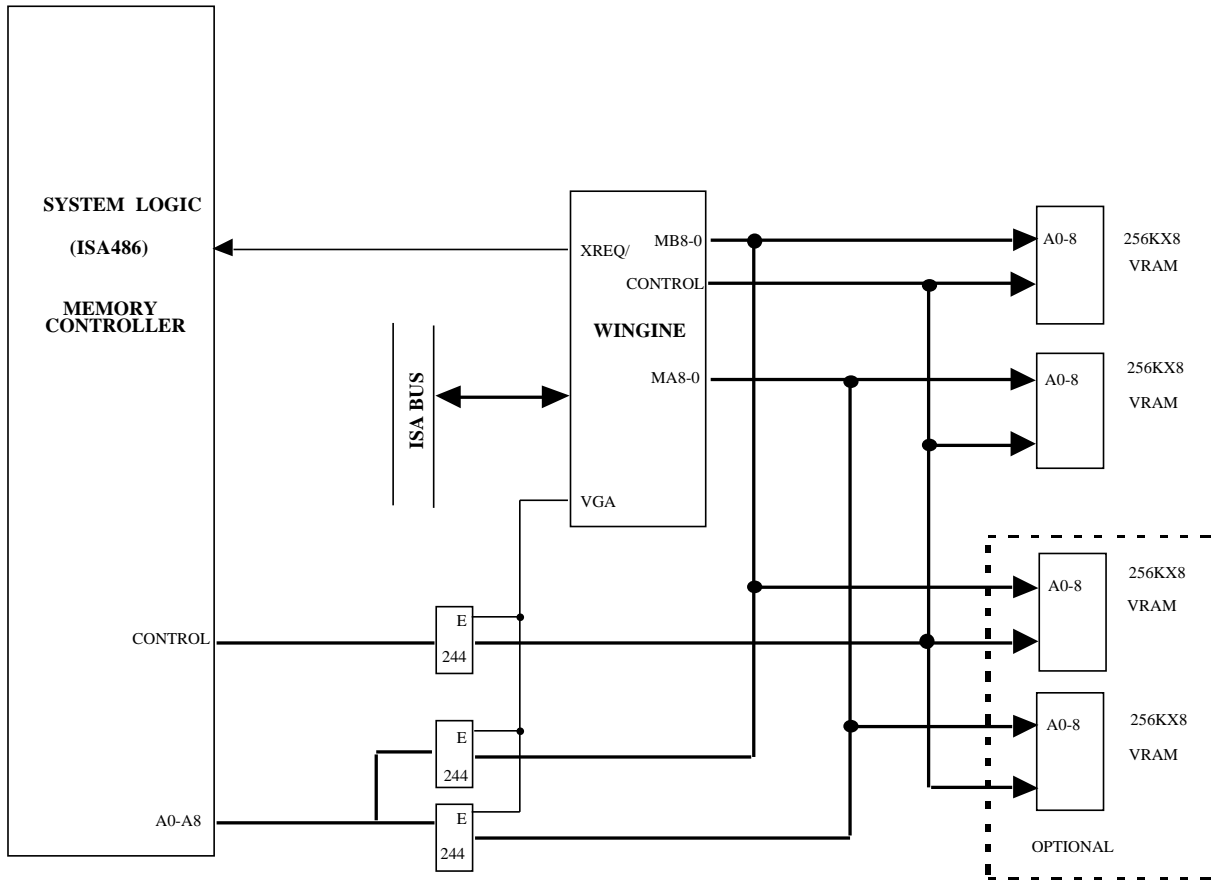
Figure 2 - Wingine Interface to ISA486 (Address/Control)
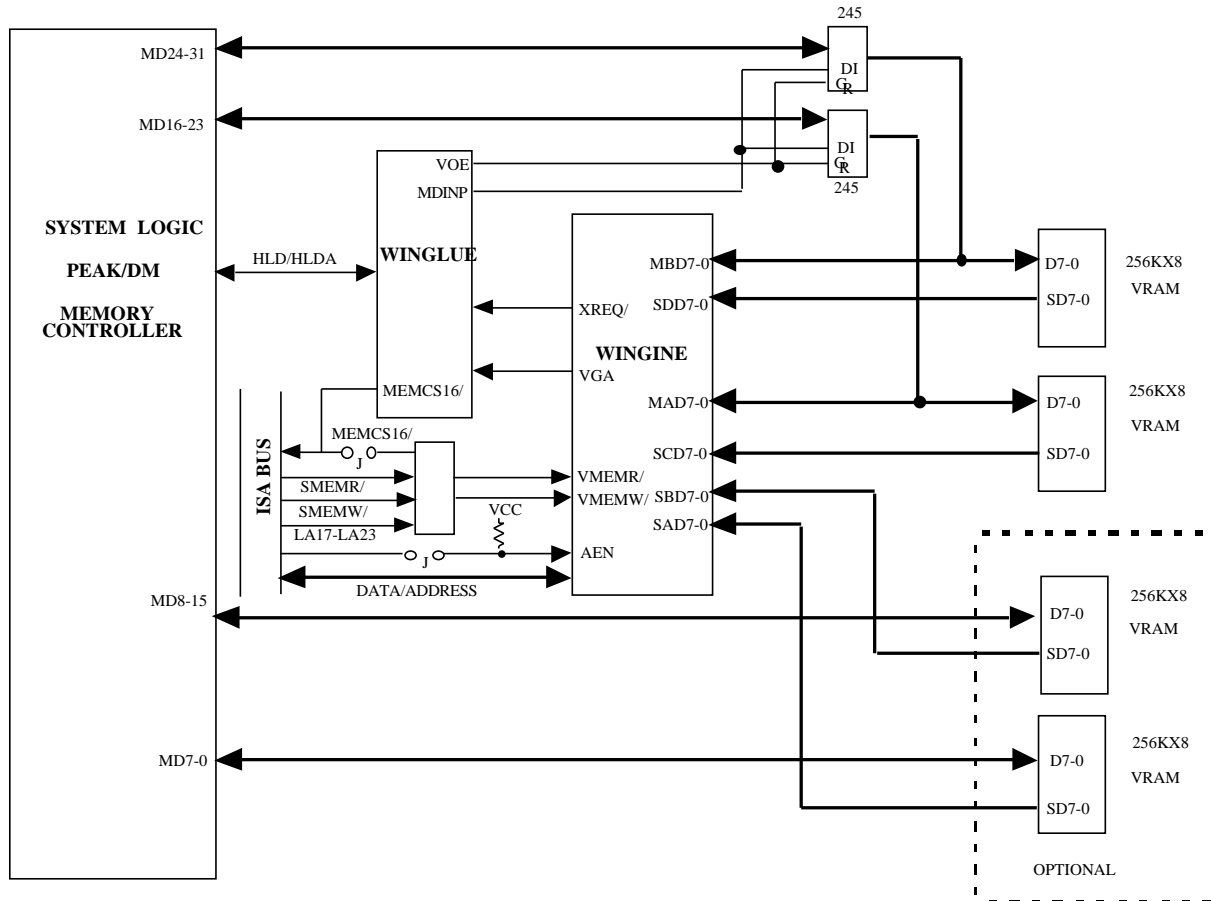
Figure 3 - Wingine Interface to PEAK/DM (Data)

PAL EQUATION:

RAMADD = ! LA23 & !LA22 & !LA21 & !LA20 & LA19 & !LA18 & LA17;

VMEMR = MEMR & RAMADD;

VMEMW = MEMW & RAMADD;

MEMCS16 .OE. = RAMADD;

MEMCS16 . = 'b' 1 ;

Figure 4 - Wingine Interface to PEAK/DM (Address/Control)

Top pins (left to right):
MBD5 MBD6 MBD7 SAD4 SBD4 SCD4 SDD4 SAD5 SBD5 SCD5 SDD5 SAD6 SBD6 SCD6 SDD6 SAD7 SBD7 SCD7 SDD7 GND **VCC** SCLK NCLK VGA CLK3 CLK2 CLK1 CLK0 MCLK GND BLANK/ PCLK P0 P1 P2 P3 P4 P5 P6 P7

(TOUT) (TCLK)

Top pin numbers: 120 119 118 117 116 115 114 113 112 111 110 109 108 107 106 105 104 103 102 101 100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81

Top alternate functions: (BUS0)(CFG0) (BUS1)(CFG1) (OSC/)(CFG2) (MEM/)(CFG3) (CFG4) (CFG5) (CFG6) (CFG7) (FLD)(MUX)(CSEL2) (CSEL1) (CSEL0) (CLKIN)

Left side:
Pin	Name		Pin	Name
121	MBD4			
122	MBD3			
123	MBD2			
124	MBD1 (ICT1/)			
125	MBD0 (TSE1/)			
126	BA8			
127	BA7			
128	BA6			
129	BA5			
130	**GND**			
131	BA4			
132	BA3			
133	BA2			
134	BA1			
135	BA0			
136	DTOEB/			
137	WE/			
138	CASB/			
139	RASB/			
140	VCC			
141	GND			
142	RASA/			
143	CASA/			
144	DSF			
145	DTOEA/			
146	AA0			
147	AA1			
148	AA2			
149	AA3			
150	**GND**			
151	AA4			
152	AA5			
153	AA6			
154	AA7			
155	AA8			
156	MAD0 (ICT0/)			
157	MAD1 (TSE0/)			
158	MAD2			
159	MAD3			
160	MAD4			

64200
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Right side:
Pin	Name
80	GND
79	SENSE
78	PALWR/
77	PALRD/
76	VSYNC
75	HSYNC
74	XREQ/
73	IRQ
72	RESET
71	VCC
70	**GND**
69	D15
68	D7
67	D14
66	D6
65	GND
64	D13
63	D5
62	D12
61	D4
60	VCC
59	GND
58	D11
57	D3
56	D10
55	D2
54	GND
53	D9
52	D1
51	D8
50	**GND**
49	VCC
48	D0
47	IOCS16/
46	A16
45	A15
44	A14
43	A13
42	A12
41	A11

Note:
Pin names shown indicate ISA (PC/AT) bus connections
Pin names in parentheses (...) indicate alternate function

Bottom pin numbers: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40

Bottom pin names: MAD5 MAD6 MAD7 SAD0 SBD0 SDD0 SAD1 SBD1 SCD1 SDD1 SAD2 SBD2 SCD2 SDD2 SAD3 SBD3 SCD3 SDD3 VCC GND RDY/ IORD/ IOWR/ VMEMR/ VMEMW/ RFSH/ AEN BHE/ A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10

Pin Name	Pin #	Dir	Drive
A00	30	In	--
A01	31	In	--
A02	32	In	--
A03	33	In	--
A04	34	In	--
A05	35	In	--
A06	36	In	--
A07	37	In	--
A08	38	In	--
A09	39	In	--
A10	40	In	--
A11	41	In	--
A12	42	In	--
A13	43	In	--
A14	44	In	--
A15	45	In	--
A16	46	In	--
AA0	146	Out	4mA
AA1	147	Out	4mA
AA2	148	Out	2mA
AA3	149	Out	2mA
AA4	151	Out	2mA
AA5	152	Out	2mA
AA6	153	Out	2mA
AA7	154	Out	2mA
AA8	155	Out	2mA
AEN	28	In	--
BA0	135	Out	4mA
BA1	134	Out	4mA
BA2	133	Out	2mA
BA3	132	Out	2mA
BA4	131	Out	2mA
BA5	129	Out	2mA
BA6	128	Out	2mA
BA7	127	Out	2mA
BA8	126	Out	2mA
BHE/	29	In	--
BLANK/ (DE)	90	Out	4mA
CASA/	143	Out	4mA
CASB/	138	Out	4mA
CLK0 (CLKIN)	93	In	--
CLK1 (CSEL0)	94	I/O	4mA
CLK2 (CSEL1)	95	I/O	4mA
CLK3 (CSEL2)	96	I/O	4mA
(TCLK) (FLD) (MUX)			
D00	48	I/O	24mA
D01	52	I/O	24mA
D02	55	I/O	24mA
D03	57	I/O	24mA
D04	61	I/O	24mA
D05	63	I/O	24mA
D06	66	I/O	24mA
D07	68	I/O	24mA
D08	51	I/O	24mA
D09	53	I/O	24mA
D10	56	I/O	24mA
D11	58	I/O	24mA
D12	62	I/O	24mA
D13	64	I/O	24mA
D14	67	I/O	24mA
D15	69	I/O	24mA
DSF	144	Out	2mA

Pin Name	Pin #	Dir	Drive
DTOEA/	145	Out	2mA
DTOEB/	136	Out	2mA
GND	21	--	--
GND	50	--	--
GND	54	--	--
GND	59	--	--
GND	65	--	--
GND	70	--	--
GND	80	--	--
GND	91	--	--
GND	101	--	--
GND	130	--	--
GND	141	--	--
GND	150	--	--
HSYNC	75	Out	24mA
IOCS16/	47	I/O	24mA
IORD/	23	In	--
IOWR/	24	In	--
IRQ	73	I/O	24mA
MAD0 (TSE0/)	156	I/O	2mA
MAD1 (ICT0/)	157	I/O	2mA
MAD2	158	I/O	2mA
MAD3	159	I/O	2mA
MAD4	160	I/O	2mA
MAD5	1	I/O	2mA
MAD6	2	I/O	2mA
MAD7	3	I/O	2mA
MBD0 (TSE1/)	125	I/O	2mA
MBD1 (ICT1/)	124	I/O	2mA
MBD2	123	I/O	2mA
MBD3	122	I/O	2mA
MBD4	121	I/O	2mA
MBD5	120	I/O	2mA
MBD6	119	I/O	2mA
MBD7	118	I/O	2mA
MCLK	92	In	--
NCLK	98	Out	4mA
P0	88	Out	4mA
P1	87	Out	4mA
P2	86	Out	4mA
P3	85	Out	4mA
P4	84	Out	4mA
P5	83	Out	4mA
P6	82	Out	4mA
P7	81	Out	4mA
PALRD/	77	Out	2mA
PALWR/	78	Out	2mA
PCLK	89	Out	4mA
RASA/	142	Out	4mA
RASB/	139	Out	4mA
RDY	22	Out	24mA
RESET	72	In	--
RFSH/	27	In	--
SAD0	4	In	--
SAD1	8	In	--
SAD2	12	In	--
SAD3	16	In	--
SAD4	117	In	--
SAD5	113	In	--
SAD6 (CFG0) (BUS0)	109	In	--
SAD7 (CFG4)	105	In	--
SBD0	5	In	--

Pin Name	Pin #	Dir	Drive
SBD1	9	In	--
SBD2	13	In	--
SBD3	17	In	--
SBD4	116	In	--
SBD5	112	In	--
SBD6 (CFG1) (BUS1)	108	In	--
SBD7 (CFG5)	104	In	--
SCD0	6	In	--
SCD1	10	In	--
SCD2	14	In	--
SCD3	18	In	--
SCD4	115	In	--
SCD5	111	In	--
SCD6 (CFG2) (OSC/)	107	In	--
SCD7 (CFG6)	103	In	--
SCLK	99	Out	4mA
SDD0	7	In	--
SDD1	11	In	--
SDD2	15	In	--
SDD3	19	In	--
SDD4	114	In	--
SDD5	110	In	--
SDD6 (CFG3) (MEM/)	106	In	--
SDD7 (CFG7)	102	In	--
SENSE	79	In	--
VCC	20	--	--
VCC	49	--	--
VCC	60	--	--
VCC	71	--	--
VCC	100	--	--
VCC	140	--	--
VGA (TOUT)	97	Out	2mA
VMEMR/	25	In	--
VMEMW/	26	In	--
VSYNC	76	Out	24mA
XREQ/	74	I/O	4mA
WE/	137	Out	4mA
(BUS0,BUS1)	See SAD6,SBD6		
(CFG0-7)	See SxD6,SxD7		
(CLKIN)	See CLK0		
(CLKSEL0-2)	See CLK1-3		
(DE)	see BLANK/		
(FLD)	See CLK3		
(ICT0/)	See MAD1		
(ICT1/)	See MBD1		
(MEM/)	See SDD6		
(MUX)	See CLK3		
(OSC/)	See SCD6		
(TSE0/)	See MAD0		
(TSE1/)	See MBD0		
(TCLK)	See CLK3		
(TOUT)	See VGA		

PIN DESCRIPTIONS

System Bus Interface

Pin #	Pin Name	Type	Active	Description
48	D0	I/O	High	System Data Bus
52	D1	I/O	High	
55	D2	I/O	High	
57	D3	I/O	High	
61	D4	I/O	High	
63	D5	I/O	High	
66	D6	I/O	High	
68	D7	I/O	High	
51	D8	I/O	High	
53	D9	I/O	High	
56	D10	I/O	High	
58	D11	I/O	High	
62	D12	I/O	High	
64	D13	I/O	High	
67	D14	I/O	High	
69	D15	I/O	High	
30	A0	In	High	System Address Bus
31	A1	In	High	
32	A2	In	High	(Note: upper addresses are decoded external to the chip
33	A3	In	High	and used to qualify the VMEMR/ and VMEMW/
34	A4	In	High	inputs)
35	A5	In	High	
36	A6	In	High	
37	A7	In	High	
38	A8	In	High	
39	A9	In	High	
40	A10	In	High	
41	A11	In	High	
42	A12	In	High	
43	A13	In	High	
44	A14	In	High	
45	A15	In	High	
46	A16	In	High	

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Pin #	Pin Name	Type	Active	Description
72	RESET	In	High	Reset. Connect directly to the bus reset signal. Note: the VRAM SOE/ pins should also be connected to RESET.
27	RFSH/	In	Low	This pin is an active low signal indicating a Refresh cycle. When this pin is low, memory is not accessible.
29	BHE/	In	Low	Byte High Enable. BHE/ low indicates the high order byte at the current word address is being accessed.
28	AEN	In	Both	Indicates valid I/O address: 0 = valid I/O address, 1 = invalid I/O address (IORD/ and IOWR/ will be ignored).
73	IRQ	Out	Both	Frame Interrupt Output. Interrupt polarity is programmable. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller.
47	IOCS16/	Out	Low	I/O Select 16. Indicates 16-bit I/O access.
23	IORD/	In	Low	I/O Read Strobe
24	IOWR/	In	Low	I/O Write Strobe
25	VMEMR/	In	Low	Memory Read Strobe qualified with upper address bits
26	VMEMW/	In	Low	Memory Write Strobe qualified with upper address bits
22	RDY	Out	High	Ready. Driven low to indicate that the current cycle should be extended with wait states. This signal is driven high at the end of the cycle, then tristated.

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name		Type	Active	Description
146	AA0		Out	High	DRAM address bus for planes 0-1
147	AA1		Out	High	
148	AA2		Out	High	
149	AA3		Out	High	
151	AA4		Out	High	
152	AA5		Out	High	
153	AA6		Out	High	
154	AA7		Out	High	
155	AA8		Out	High	
135	BA0		Out	High	DRAM address bus for planes 2-3
134	BA1		Out	High	
133	BA2		Out	High	
132	BA3		Out	High	
131	BA4		Out	High	
129	BA5		Out	High	
128	BA6		Out	High	
127	BA7		Out	High	
126	BA8		Out	High	
142	RASA/		Out	Low	Row address strobe for memory planes 0-1
139	RASB/		Out	Low	Row address strobe for memory planes 2-3
143	CASA/		Out	Low	Column address strobe for planes 0-1
138	CASB/		Out	Low	Column address strobe for planes 2-3
137	WE/		Out	Low	Write enable for memory all planes
145	DTOEA/		Out	Low	VRAM data transfer output enable for planes 0-1
136	DTOEB/		Out	Low	VRAM data transfer output enable for planes 2-3
144	DSF		Out	High	VRAM Special Function (block write, etc.)
156	MAD0	(TSE0/)	I/O	High	Display memory data bus for planes 0 and 1
157	MAD1	(ICT0/)	I/O	High	
158	MAD2		I/O	High	(see clock pins page for explanation of the TSE and
159	MAD3		I/O	High	ICT features)
160	MAD4		I/O	High	
1	MAD5		I/O	High	
2	MAD6		I/O	High	
3	MAD7		I/O	High	
125	MBD0	(TSE1/)	I/O	High	Display memory data bus for planes 2 and 3
124	MBD1	(ICT1/)	I/O	High	
123	MBD2		I/O	High	
122	MBD3		I/O	High	
121	MBD4		I/O	High	
120	MBD5		I/O	High	
119	MBD6		I/O	High	
118	MBD7		I/O	High	

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Display Memory Interface (continued)

Pin #	Pin Name			Type	Active	Description
4	SAD0	(SD0)		I/O	High	Serial data for bits 0-7 (pixel A)
8	SAD1	(SD1)		I/O	High	
12	SAD2	(SD2)		I/O	High	
16	SAD3	(SD3)		I/O	High	
117	SAD4	(SD4)		I/O	High	
113	SAD5	(SD5)		I/O	High	
109	SAD6	(SD6)	(CFG0)	I/O	High	CFG0 is also called BUS0 (see config register XR01)
105	SAD7	(SD7)	(CFG4)	I/O	High	
5	SBD0	(SD8)		I/O	High	Serial data for bits 8-15 (pixel B)
9	SBD1	(SD9)		I/O	High	
13	SBD2	(SD10)		I/O	High	
17	SBD3	(SD11)		I/O	High	
116	SBD4	(SD12)		I/O	High	
112	SBD5	(SD13)		I/O	High	
108	SBD6	(SD14)	(CFG1)	I/O	High	CFG1 is also called BUS1 (see config register XR01)
104	SBD7	(SD15)	(CFG5)	I/O	High	
6	SCD0	(SD16)		I/O	High	Serial data for bits 16-23 (pixel C)
10	SCD1	(SD17)		I/O	High	
14	SCD2	(SD18)		I/O	High	
18	SCD3	(SD19)		I/O	High	
115	SCD4	(SD20)		I/O	High	
111	SCD5	(SD21)		I/O	High	
107	SCD6	(SD22)	(CFG2)	I/O	High	CFG2 is also called OSC/ (see config register XR01)
103	SCD7	(SD23)	(CFG6)	I/O	High	
7	SDD0	(SD24)		I/O	High	Serial data for bits 24-31 (pixel D)
11	SDD1	(SD25)		I/O	High	
15	SDD2	(SD26)		I/O	High	
19	SDD3	(SD27)		I/O	High	
114	SDD4	(SD28)		I/O	High	
110	SDD5	(SD29)		I/O	High	
106	SDD6	(SD30)	(CFG3)	I/O	High	CFG3 is also called MEM/ (see config register XR01)
102	SDD7	(SD31)	(CFG7)	I/O	High	
99	SCLK			Out	High	VRAM shift clock. Inactive during H/V blanking.
74	XREQ/			I/O	Low	Transfer Request. Used as an <u>output</u> to signal that a VRAM data transfer cycle needs to be performed (i.e., VRAM shift registers need to be filled). Used as an <u>input</u> to signal that a data transfer has been performed (i.e., VRAM shift registers are ready to be shifted out). Tristate if Wingine mode is disabled (default). Internal pullup. Direction is controlled by XR03 bit-7.
97	VGA	(TOUT)		Out	High	VRAM Control Select. High indicates the Wingine chip is driving the VRAM address, data, and control lines. Low indicates Wingine's VRAM address, data, and control pins are tri-stated. Controlled by XR03 (Master Control register, port 22-23h index E0h) bit-0 inverted.

Also becomes the test output in ICT mode. See the clock pins page for an explanation of ICT

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Video Interface

Pin #	Pin Name		Type	Active	Description
81	P7		Out	High	8-bit video data output
82	P6		Out	High	
83	P5		Out	High	
84	P4		Out	High	
85	P3		Out	High	
86	P2		Out	High	
87	P1		Out	High	
88	P0		Out	High	
76	VSYNC		Out	Both	Horizontal Sync (polarity is programmable: MSR bit-7)
75	HSYNC		Out	Both	
89	PCLK		Out	High	Vertical Sync (polarity is programmable: MSR bit-6)
					Pixel clock for video data. In 16-bit/pixel mode, the rising edge may be used externally to latch the 'upper' data byte and the following falling edge used to transfer the 'lower' byte.
90	BLANK/	(DE)	Out	Both	Blanking signal for the external color palette chip (polarity is programmable: see XR28 bit-0). This pin may also be redefined as a Display Enable signal (see XR28 bit-1).
78	PALWR/		Out	Low	I/O write strobe for the external color palette chip (IMSG176, BT47x, or compatible). Asserted when the chip is enabled and an I/O Write occurs to addresses 3C6-3C9h (or 43Cx, 83Cx, and C3Cx if enabled by XR02).
77	PALRD/		Out	Low	I/O read strobe for an external color palette chip (IMSG176, BT47x, or compatible). Asserted when an I/O Read occurs from addresses 3C6h, 3C8h, or 3C9h (or 43Cx, 83Cx, and C3Cx if enabled by XR02). The chip responds directly for reads from 3C7h.
79	SENSE		In	High	Monitor sense input. Normally connected to the outputs of an LM339 comparator on the external color palette chip analog RGB outputs (or directly to the color palette chip if this function is built in such as in the BT475). The state of this pin may read as bit-4 of Input Status Register 0 (port 3C2h). See also extension register XR1F (Virtual Switch Register).

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Clock, Power, and Ground

Pin #	Pin Name		Type	Active	Description
92	MCLK		In	High	Memory Clock. 50 MHz for 100ns RAM's, 56 MHz for 80 ns RAM's, or 65 MHz for 70ns RAM's.
93	CLK0	(CLKIN)	In	High	If <u>external</u> clock selection is enabled (default), CLKIN is the input dotclock for all pixel clock frequencies and
94	CLK1	(CSEL0)	I/O	High	CLK0-1 become clock select outputs driven by Misc Output Register (MSR at port 3C2h) bits 2 and 3
95	CLK2	(CSEL1)	I/O	High	(CSEL 0 and 1, respectively). The CLK3 pin can be programmed (via FCR port 3BA/3DA bits 0-1) to be
96	CLK3	(CSEL2) (FLD) (MUX) (TCLK)	I/O	High	low or high (CSEL2), an odd/even field indicator for interlace mode (FLD), or PCLK÷2 (MUX). CLK3 is also used as the test clock (TCLK) in ICT mode (see the description of ICT mode at bottom of page).
					If <u>internal</u> clock selection is enabled (see configuration pin 'OSC/' and config register XR01), CLK0, CLK1, CLK2, and CLK3 are inputs for external discrete oscillators. One of the four is selected as the input dotclock per Misc Output Register (MSR port 3C2h) bits 2-3.
98	NCLK		Out	High	PCLK ÷ 4 or ÷ 8 (free-running version of SCLK).
20	VCC		VCC	--	Power
49	VCC		VCC	--	
60	VCC		VCC	--	
71	VCC		VCC	--	
100	VCC		VCC	--	
140	VCC		VCC	--	Ground
21	GND		GND	--	
50	GND		GND	--	
54	GND		GND	--	
59	GND		GND	--	
65	GND		GND	--	
70	GND		GND	--	
80	GND		GND	--	
91	GND		GND	--	
101	GND		GND	--	
130	GND		GND	--	
141	GND		GND	--	
150	GND		GND	--	

<u>ICT Mode</u>: If <u>ICT0/ and ICT1/ are low</u> with <u>RESET high</u>, a <u>rising edge on CLK3</u> will put the chip into 'In Circuit Test' mode. In ICT mode, all digital signal pins become inputs which are part of a long path starting at NCLK (pin 98) and proceeding to higher pin numbers around the chip to pin 160 then to pin 1 and ending at CLK3 (pin 96). If all pins in the path are high, the VGA output will be high. If any pin is low, the VGA output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time (CLK3 last) and observing the effect on VGA. CLK3 must be toggled last because rising edges on CLK3 with ICT1/ or ICT2/ high or RESET low will <u>exit ICT mode</u>. As a side effect, ICT mode effectively 3-states all pins except VGA.

If <u>TSE0/ and TSE1/ are low</u> with <u>RESET high</u>, a <u>rising edge on CLK3</u> will <u>3-state all pins</u>. A CLK3 rising edge without the enabling conditions exits 3-state.

Note: Pin names in parentheses (...) indicate alternate functions

REGISTER SUMMARY - CGA, MDA, AND HERCULES MODEs

Register	Register Name	Bits	Access	I/O Port - MDA/Herc	I/O Port - CGA	Comment
ST00 (STAT)	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	RW	3B8	3D8	
COLOR	CGA Color Select	6	RW	n/a	3D9	
			RW	3D6-3D7 index 7E	3D6-3D7 index 7E	XR7E
HCFG	Hercules Configuration	2	W	3BF	n/a	
			RW	3D6-3D7 index 14	3D6-3D7 index 14	XR14
RX, R0-11	'6845' Registers	0-8	RW	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MSR	Miscellaneous Output	7	W	3C2	3C2	
FCR	Feature Control	4	W	3BA	3DA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MASTER	Master Control	8	W	22-23h index E0h	22-23h index E0h	R/W Copy in System
			RW	3D6-3D7 index 03	3D6-3D7 index 03	XR03
VSE	Video Subsystem Enable	1	RW	3C3 if PI	3C3 if PI	Disabled by XR70 bit-6
SETUP	Setup Control	2	W	46E8 if ISA	46E8 if ISA	Disabled by XR70 bit-7
ENABLE	Global Enable	1	RW	102 if ISA	102 if ISA	Setup Only
MSR	Miscellaneous Output	7	W	3C2	3C2	
			R	3CC	3CC	
FCR	Feature Control	4	W	3BA	3DA	
			R	3CA	3CA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	6	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
DACMASK	Color Palette Pixel Mask	8	RW	3C6, 83C6	3C6, 83C6	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	
DACWX	Color Palette Write-Mode Index	8	RW	3C8, 83C8	3C8, 83C8	
DACDATA	Color Palette Data 0-FF	3x6 or 3x8	RW	3C9, 83C9	3C9, 83C9	
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - INDEXED REGISTERS (VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	RW	RW	3C4
SR0	Reset	2	VGA/EGA	RW	RW	3C5
SR1	Clocking Mode	6	VGA/EGA	RW	RW	3C5
SR2	Plane Mask	4	VGA/EGA	RW	RW	3C5
SR3	Character Map Select	6	VGA/EGA	RW	RW	3C5
SR4	Memory Mode	3	VGA/EGA	RW	RW	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	RW	RW	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	0	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	RW	RW	3CE
GR0	Set/Reset	4	VGA/EGA	RW	RW	3CF
GR1	Enable Set/Reset	4	VGA/EGA	RW	RW	3CF
GR2	Color Compare	4	VGA/EGA	RW	RW	3CF
GR3	Data Rotate	5	VGA/EGA	RW	RW	3CF
GR4	Read Map Select	2	VGA/EGA	RW	RW	3CF
GR5	Mode	6	VGA/EGA	RW	RW	3CF
GR6	Miscellaneous	4	VGA/EGA	RW	RW	3CF
GR7	Color Don't Care	4	VGA/EGA	RW	RW	3CF
GR8	Bit Mask	8	VGA/EGA	RW	RW	3CF
ARX	Attribute Controller Index	6	VGA/EGA	RW	RW	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	RW	RW	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	RW	RW	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	RW	RW	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	RW	RW	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	RW	RW	3C0 (3C1)
AR14	Color Select	4	VGA	RW	n/a	3C0 (3C1)

EXTENSION REGISTER SUMMARY: 00–2F

Chips' VGA Product Family

Reg	Register Name	Bits	Access	Port	Reset	450	451	452	453	455	456	457	64200	65530
XRX	**Extension Index Register**	7	R/W	3D6	- x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR00	**Chip Version**	8	R/O	3D7	1 0 1 0 r r r r	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR01	**Configuration**	8	R/O	3D7	d d d d d d d d	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR02	**CPU Interface Control**	5	R/W	3D7	0 0 0 0 0 - - -	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR03	**Master Control** *(ROM Interface)*	6	R/W	3D7	0 0 0 0 - - 0 0	.	✓	✓	✓	.	.	✓	✓	.
XR04	**Memory Control**	3	R/W	3D7	- - 0 - - 0 - 0	✓	✓	✓	.	✓	✓	✓	✓	✓
XR05	*(Clock Control)*	--	--	3D7		.	.	✓	✓	.	.	✓	.	.
XR06	*(Color Palette Control / DRAM Intfc)*	--	--	3D7		.	.	✓	.	.	.	.	.	✓
XR07	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR08	*(General Purpose Output Select B)*	--	--	3D7		.	✓	✓	.	✓	✓	✓	.	.
XR09	*(General Purpose Output Select A)*	--	--	3D7		.	✓	✓	.	✓	✓	✓	.	.
XR0A	*(Cursor Address Top)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR0B	**CPU Paging**	3	R/W	3D7	- - - - - 0 0 0	✓	.	✓	✓	✓	✓	✓	✓	✓
XR0C	**Start Address Top**	1	R/W	3D7	- - - - - - - 0	✓	.	✓	✓	.	.	.	✓	✓
XR0D	**Auxiliary Offset**	2	R/W	3D7	- - - - - - 0 0	✓	✓	✓	.	✓	✓	✓	✓	✓
XR0E	**Text Mode Control**	2	R/W	3D7	- - - - 0 0 - -	✓	.	✓	.	.	.	.	✓	✓
XR0F	*(Configuration Register 2)*	--	--	3D7		.	.	.	.	.	.	.	.	✓
XR10	**Single/Low Map Register**	8	R/W	3D7	x x x x x x x x	✓	.	✓	✓	.	.	.	✓	✓
XR11	**High Map Register**	8	R/W	3D7	x x x x x x x x	✓	.	✓	✓	.	.	.	✓	✓
XR12	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR13	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR14	**Emulation Mode**	8	R/W	3D7	0 0 0 0 h h 0 0	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR15	**Write Protect**	8	R/W	3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR16	*(Trap Enable)*	--	--	3D7		.	✓	✓	✓	✓	✓	✓	.	.
XR17	*(Trap Status)*	--	--	3D7		.	✓	✓	✓	✓	✓	✓	.	.
XR18	**Alternate H Disp End**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR19	**Alternate H Sync Start / Half-line**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1A	**Alternate H Sync End**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1B	**Alternate H Total**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1C	**Alternate H Blank Start** *(H Panel Size)*	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1D	**Alternate H Blank End**	8	R/W	3D7	0 x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1E	**Alternate Offset**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1F	**Virtual EGA Switch Register**	5	R/W	3D7	0 - - - x x x x	✓	.	.	.	.	.	.	✓	✓
XR20	-reserved- *(453 Interface II)/(SUD)*	--	--	3D7		.	.	✓	✓	.	.	.	.	.
XR21	-reserved- *(Sliding Hold A)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR22	-reserved- *(Sliding Hold B)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR23	-reserved- *(SHC)/(WBM Ctrl)*	--	--	3D7		.	.	✓	✓	.	.	.	.	.
XR24	*(FP AltMaxScanline/SHD/WBM Patt)*	--	--	3D7		.	.	✓	✓	.	.	.	.	✓
XR25	*(FP AltGrHVirtPanel Size/453PinDefn)*	--	--	3D7		.	.	✓	✓	.	.	.	.	✓
XR26	-reserved- *(453 Config)*	--	--	3D7		.	.	.	.	.	✓	.	.	.
XR27	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR28	**Video Interface**	7	R/W	3D7	0 0 0 0 - 0 0 0	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR29	-reserved- *(Function Control)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR2A	-reserved- *(Frame Intrpt Count)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR2B	**Default Video**	8	R/W	3D7	0 0 0 0 0 0 0 0	✓	✓	✓	.	✓	✓	✓	✓	✓
XR2C	*(FP Vsync (FLM) Delay/Force H High)*	--	--	3D7		.	.	✓	.	.	.	.	.	✓
XR2D	*(FP Hsync (LP) Delay / Force H Low)*	--	--	3D7		.	.	✓	.	.	.	.	.	✓
XR2E	*(FP Hsync (LP) Delay / Force V High)*	--	--	3D7		.	.	✓	.	.	.	.	.	✓
XR2F	*(FP Hsync (LP) Width / Force V Low)*	--	--	3D7		.	.	✓	.	.	.	.	.	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)   − = Not implemented (always reads 0)
 d = Set from the corresponding data bus pin on falling edge of RESET   r = Chip revision # (starting from 0000)
 h = Read-only Hercules Configuration Register Readback bits   0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 & 64xxx VGAs drive CRTs, 455–457 & 655x0 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 30-5F

Chips' VGA Product Family

Reg	Register Name	Bits	Access	Port	Reset	450	451	452	453	455	456	457	**64200**	65530
XR30	*(Graphics Cursor Start Address High)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR31	*(Graphics Cursor Start Address Low)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR32	*(Graphics Cursor End Address)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR33	*(Graphics Cursor X Position High)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR34	*(Graphics Cursor X Position Low)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR35	*(Graphics Cursor Y Position High)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR36	*(Graphics Cursor Y Position Low)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR37	*(Graphics Cursor Mode)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR38	*(Graphics Cursor Mask)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR39	*(Graphics Cursor Color 0)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR3A	*(Graphics Cursor Color 1)*	--	--	3D7		.	.	✓	.	.	.	.	.	.
XR3B	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR3C	**Serial / Row Count**	6	R/W	3D7	- - x x x x x x	.	.	.	.	.	.	.	✓	.
XR3D	**Multiplexer Mode**	5	R/W	3D7	- - - x x x x x	.	.	.	.	.	.	.	✓	.
XR3E	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR3F	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR40	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR41	*(Virtual EGA Switch Register)*	--	--	3D7		.	.	.	✓	.	.	.	.	.
XR42	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR43	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR44	*(Software Flag Register)*	--	--	3D7		.	.	.	✓	.	.	.	.	✓
XR45	*(Software Flag Register 2 / FG Color)*	--	--	3D7		.	.	.	✓	.	.	.	.	.
XR46	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR47	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR48	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR49	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR4A	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR4B	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR4C	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR4D	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR4E	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR4F	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR50	*(Panel Format)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR51	*(Display Type)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR52	*(Power Down Control / Panel Size)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR53	*(Line Graphics Override)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR54	*(FP Interface / Alternate Misc Output)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR55	*(H Compensation / Text 350_A Comp)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR56	*(H Centering / Text 350_B Comp)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR57	*(V Compensation / Text 400 Comp)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR58	*(V Centering / Graphics 350 Comp)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR59	*(V Line Insertion/Graphics 400 Comp)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR5A	*(V Line Replication/FP VDisp St 400)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR5B	*-reserved- (FP VDisp End 400)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	.
XR5C	*(Weight Control Clock A)*	--	--	3D7		.	.	.	.	✓	✓	.	.	.
XR5D	*(Weight Control Clock B)*	--	--	3D7		.	.	.	.	✓	✓	.	.	.
XR5E	*(ACDCLK Control)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR5F	*(Power Down Mode Refresh)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)   − = Not implemented (always reads 0)
d = Set from the corresponding data bus pin on falling edge of RESET   r = Chip revision # (starting from 0000)
h = Read-only Hercules Configuration Register Readback bits   0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 & 64xxx VGAs drive CRTs, 455–457 & 655x0 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 60-7F

Chips' VGA Product Family

Reg	Register Name	Bits	Access	Port	Reset	450	451	452	453	455	456	457	**64200**	65530
XR60	*(Blink Rate Control)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR61	*(SmartMap™ Control)*	--	--	3D7		.	.	.	.	✓	✓	.	.	✓
XR62	*(SmartMap™ Shift Parameter)*	--	--	3D7		.	.	.	.	✓	✓	.	.	✓
XR63	*(SmartMap™ Color Mapping Control)*	--	--	3D7		.	.	.	.	✓	✓	.	.	✓
XR64	*(FP Alternate Vertical Total)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR65	*(FP Alternate Overflow)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR66	*(FP Alternate Vertical Sync Start)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR67	*(FP Alternate Vertical Sync End)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR68	*(FP V Panel Size / FP Alt V DE End)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	✓
XR69	*(FP V Display Start 350)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	.
XR6A	*(FP V Display End 350)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	.
XR6B	*(FP V Overflow 2)*	--	--	3D7		.	.	.	.	✓	✓	✓	.	.
XR6C	*(Weight Control Clock C)*	--	--	3D7		.	.	.	.	✓	✓	.	.	.
XR6D	*(FRC Control)*	--	--	3D7		.	.	.	.	.	✓	✓	.	.
XR6E	*(Polynomial FRC Control)*	--	--	3D7		.	.	.	.	.	.	✓	.	✓
XR6F	*(Frame Buffer Control)*	--	--	3D7		.	.	.	.	.	.	.	.	✓
XR70	**Setup / Disable Control**	1	R/W	3D7	0 - - - - - - -	✓	.	.	.	.	.	.	✓	✓
XR71	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR72	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR73	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR74	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR75	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR76	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR77	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR78	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR79	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR7A	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR7B	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR7C	-reserved-	--	--	3D7		.	.	.	.	.	.	.	.	.
XR7D	*(FP Compensation Diagnostic)*	--	--	3D7		.	.	.	.	.	.	.	.	✓
XR7E	**CGA/Hercules Color Select**	6	R/W	3D7	- - x x x x x x	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	8	R/W	3D7	0 0 x x x x 0 0	✓	✓	✓	.	✓	✓	✓	✓	✓

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Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
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Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register is used to enable or disable the VGA. It is also used to place the VGA in normal or setup mode.

The Global and Extension Enable Registers are accessible only during Setup mode. The Global ID Register contains the ID number that identifies the 64200 as a Chips & Technologies product.

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space*. Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, the 64200 decodes the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin, pending CRT interrupt, display enable/HSYNC output, and vertical retrace/video output. The Feature Control Register selects the VSYNC function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and video SYNC polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The

Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4/16/32KBytes, Odd/Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND EXTERNAL COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen. External color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Some of the registers are located external to the 64200 in the external color palette. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 64200 uses several additional registers to support new features that are not available in an ordinary VGA. No new bits are defined and no reserved/unused bits are used in the regular VGA registers.

These extended 64200 registers and the functions they control are disabled on reset. The extended registers can be accessed by two sets of control bits (disabled on reset). Access to 64200 extended registers is accomplished by putting the 64200 in VGA setup mode and setting bit-D7 of the register at I/O address 103h. Once access is enabled, extended registers can be addressed using the index/data pair of registers at I/O address 3B6h / 3B7h or 3D6h / 3D7h.

In the 64200, a new extended register, 46E8 Register Override (XR70) has been implemented. When set, this register write protects setup register 103 (Extension Enable Register). This forces the extended registers to stay enabled no matter what is written to port 46E8 or the setup registers.

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. <u>Miscellaneous</u> Registers include the 64200 Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.

2. <u>General Purpose</u> Registers handle video blanking and the video default color.

3. <u>Backwards Compatibility</u> Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.

4. <u>Alternate Horizontal and Vertical</u> Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.

Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 64200 (Extension Registers) are summarized in the Extension Register Table.

Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
–	Setup Control	–	W	46E8h	–	29
–	Global Enable	–	RW	102h & Setup mode	–	29

SETUP CONTROL REGISTER
Write only at I/O Address 46E8h
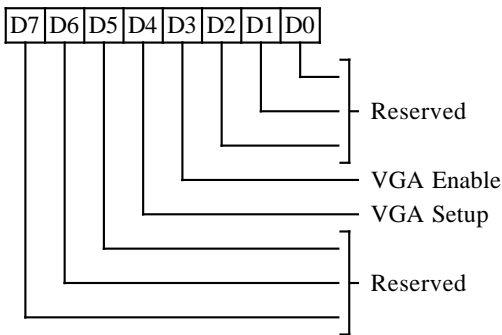
This register is cleared by RESET.

2-0   **Reserved (0)**

3   **VGA Enable**

    0   VGA is disabled
    1   VGA is enabled

4   **Setup Mode**

    0   VGA is in Normal Mode
    1   VGA is in Setup Mode

7-5   **Reserved (0)**

GLOBAL ENABLE REGISTER
Read/Write at I/O Address 102h
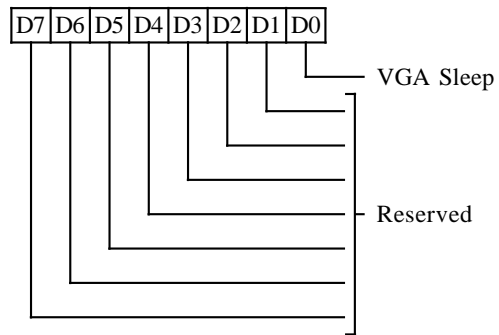
This register is only accessible in Setup Mode. It is cleared by RESET.

0   **VGA Sleep**

    0   VGA is disabled
    1   VGA is enabled

7-1   **Reserved (0)**

General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	31
ST01	Input Status 1	–	R	3BAh/3DAh	–	31
FCR	Feature Control	–	W	3BAh/3DAh	5	32
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	32
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)
Read only at I/O Address at 3C2h
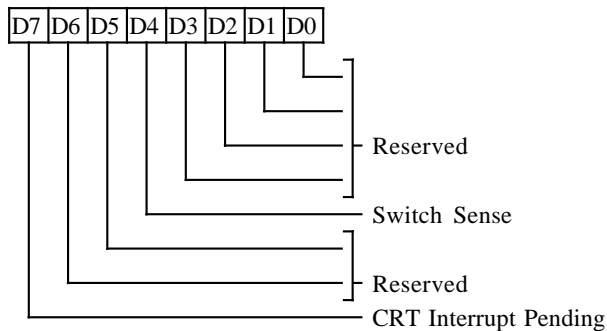
3-0 **Reserved (0)**

4 **Switch Sense**

This bit returns the Status of the SENSE pin.

6-5 **Reserved (0)**

7 **CRT Interrupt Pending**

    0 Indicates no CRT interrupt is pending

    1 Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)
Read only at I/O Address 3BAh/3DAh
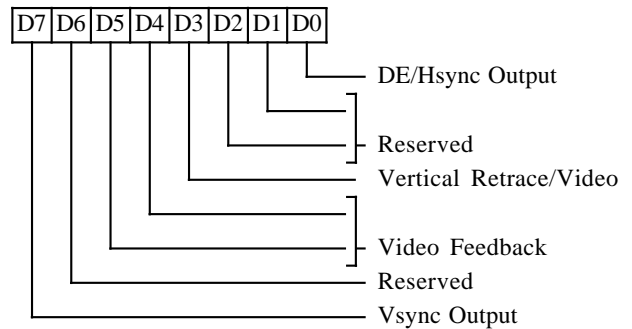
0 **Display Enable/HSYNC Output**

The functionality of this bit is controlled by the Emulation Mode register (XR14[4]).

    0 Indicates DE or HSYNC <u>inactive</u>
    1 Indicates DE or HSYNC <u>active</u>

2-1 **Reserved (0)**

3 **Vertical Retrace/Video**

The functionality of this bit is controlled by the Emulation Mode register (XR14[5]).
    0 Indicates VSYNC or video <u>inactive</u>
    1 Indicates VSYNC or video <u>active</u>

5-4 **Video Feedback 1, 0**

These are diagnostic video bits which are selected via the Color Plane Enable Register.

6 **Reserved (0)**

7 **Vsync Output**

The functionality of this bit is controlled by the Emulation Mode register (XR14[6]). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)
Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection
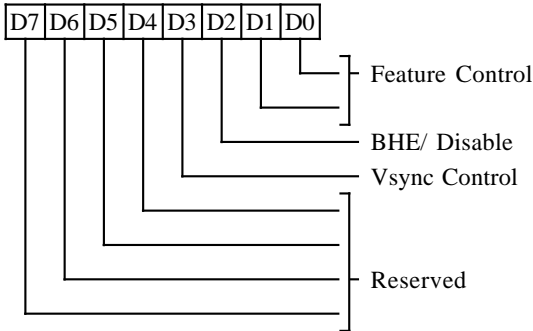
1-0 Feature Control

When the 'OSC/' configuration bit is high (see XR01) indicating CLK1-3 are outputs, these bits determine the CLK3 (CSEL2) pin function as follows:

FCR1:0 = 00 = CLK3 pin low
FCR1:0 = 01 = CLK3 pin high
FCR1:0 = 10 = CLK3 is Field (0=even)
FCR1:0 = 11 = CLK3 is PCLK÷ 2

'10' is for interface to the BT484 'FLD' pin which indicates the odd or even field for the hardware cursor in interlace mode. '11' is for interface with the Music Semiconductor RAMDAC 'MUX' pin. '00' and '01' may be used to control the Sierra Semiconductor RAMDAC 'HICOLOR/' pin. Use of the CLK3 pin for RAMDAC control assumes an 82C404 programmable clock chip is being used and therefore CLK3 is not needed for clock selection.

2 BHE/ Disable

This bit may be set to disable 16-bit operations to the chip (the chip will always treat the BHE/ input as high regardless of the state of the pin if this register bit is set).

3 Vsync Control

0 VSync output on the VSYNC pin (default)
1 Logical 'OR' of VSync and Display Enable output on the VSYNC pin

This capability is not typically very useful, but is provided for IBM compatibility.

7-4 Reserved (0)

MISCELLANEOUS OUTPUT REGISTER (MSR)
Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection
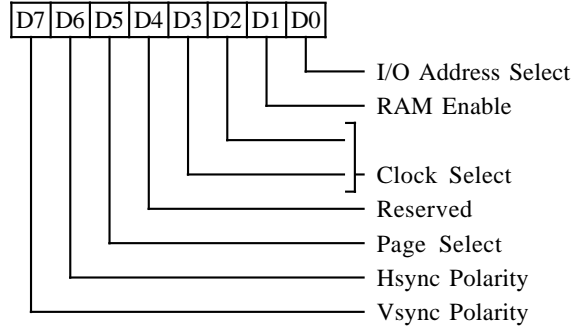
This register is cleared by RESET.

0 I/O Address Select.
This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0 Select 3Bxh I/O address
1 Select 3Dxh I/O address

1 Enable RAM

0 Prevent CPU access to display memory
1 Allow CPU access to display memory

3-2 Clock Select.
These bits usually select the dot clock source for the CRT interface:

MSR3:2 = 00 = Select CLK0
MSR3:2 = 01 = Select CLK1
MSR3:2 = 10 = Select CLK2
MSR3:2 = 11 = Select CLK3

See extension register XR01 bits 2-3 (Configuration) and FCR bits 0-1 for variations of the above clock selection mapping. See also XR1F (Virtual Switch Register) for additional functionality potentially controlled by these bits.

4 Reserved (0)

5 Page Select.
In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64K byte page in display memory for CPU access: 1=select lower page; 0=select upper page.

6 CRT Hsync Polarity. 0=pos, 1=neg

7 CRT Vsync Polarity. 0=pos, 1=neg

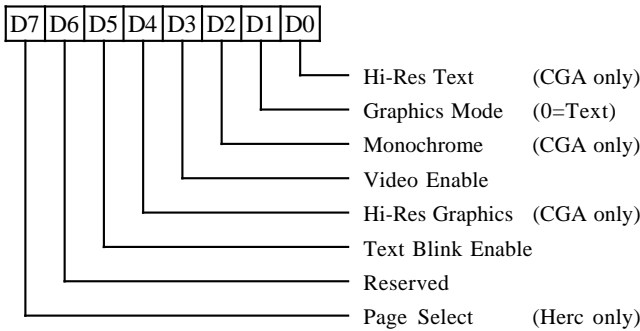(Blank pin polarity can be controlled via the Video Interface Register, XR28)

CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	33
COLOR	CGA Color Select	–	RW	3D9h	–	34
HCFG	Hercules Configuration	–	RW	3BFh	–	35

CGA / HERCULES MODE CONTROL REGISTER (MODE)
Read/Write at I/O Address 3B8h/3D8h

D7	D6	D5	D4	D3	D2	D1	D0

Hi-Res Text   (CGA only)
Graphics Mode   (0=Text)
Monochrome   (CGA only)
Video Enable
Hi-Res Graphics   (CGA only)
Text Blink Enable
Reserved
Page Select   (Herc only)

This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0   CGA 80/40 Column Text Mode

0   Select 40 column CGA text mode
1   Select 80 column CGA text mode

1   CGA/Hercules Graphics/Text Mode

0   Select text mode
1   Select graphics mode

2   CGA Mono/Color Mode

0   Select CGA color mode
1   Select CGA monochrome mode

3   CGA/Hercules Video Enable

0   Blank the screen
1   Enable video output

4   CGA High Resolution Mode

0   Select 320x200 graphics mode
1   Select 640x200 graphics mode

5   CGA/Hercules Text Blink Enable

0   Disable character blink attribute (blink attribute bit-7 used to control background intensity)
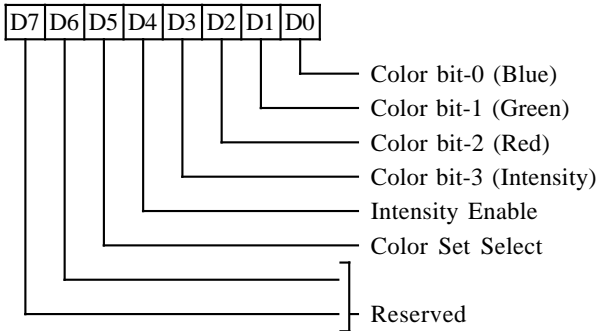1   Enable character blink attribute

6   Reserved (0)

7   Hercules Page Select

0   Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
1   Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER
Read/Write at I/O Address 3D9h

D7	D6	D5	D4	D3	D2	D1	D0

- Color bit-0 (Blue)
- Color bit-1 (Green)
- Color bit-2 (Red)
- Color bit-3 (Intensity)
- Intensity Enable
- Color Set Select
- Reserved

This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET.

3-0   Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (the color displayed when the pixel value is 0) is black.

4   Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

5   Color Set Select

This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:
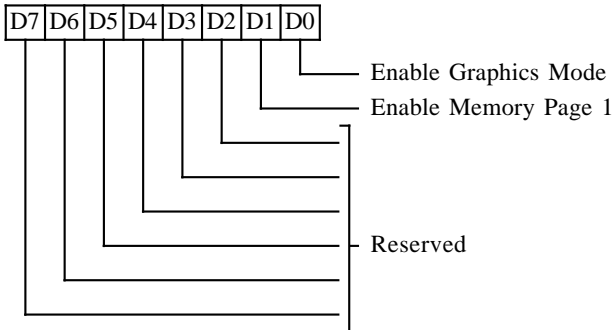
Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6   Reserved (0)

**HERCULES CONFIGURATION
REGISTER (HCFG)**
Write only at I/O Address 3BFh

D7 D6 D5 D4 D3 D2 D1 D0

— Enable Graphics Mode
— Enable Memory Page 1

— Reserved

This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14 bits 2 & 3. It is cleared by RESET.

0   Enable Graphics Mode

0   Lock the 64200 in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh (in text mode the same area of display memory wraps around 8 times within this range such that B0000 accesses the same display memory location as B1000, B2000, etc.).

1   Permit entry to Hercules Graphics mode.

1   Enable Memory Page 1

0   Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.

1   The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.
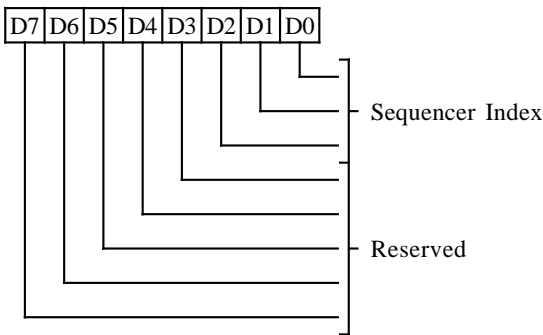
7-2   Reserved (0)

Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	37
SR00	Reset	00h	RW	3C5h	1	37
SR01	Clocking Mode	01h	RW	3C5h	1	38
SR02	Plane/Map Mask	02h	RW	3C5h	1	38
SR03	Character Font	03h	RW	3C5h	1	39
SR04	Memory Mode	04h	RW	3C5h	1	40
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	40

SEQUENCER INDEX REGISTER (SRX)
Read/Write at I/O Address 3C4h

This register is cleared by RESET.

2-0   Sequencer Index

These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.
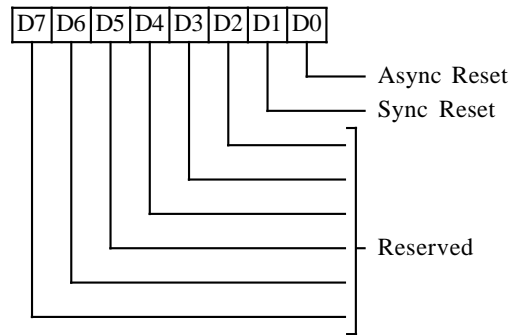
7-3   Reserved (0)

SEQUENCER RESET REGISTER (SR00)
Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection

0   Asynchronous Reset

0   Force asynchronous reset
1   Normal operation

Display memory data will be corrupted if this bit is set to zero.

1   Synchronous Reset

0   Force synchronous reset
1   Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).
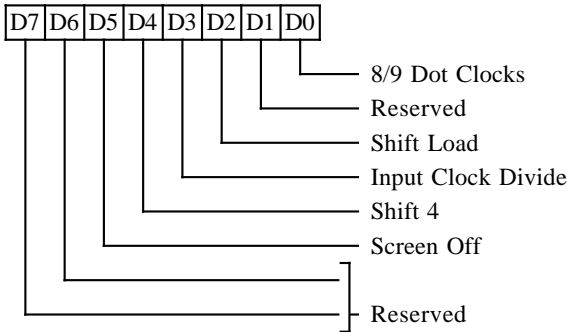
7-2   Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)
Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection

0   8/9 Dot Clocks

This bit determines whether a character clock is 8 or 9 dot clocks long.

    0   Select 9 dots/character clock
    1   Select 8 dots/character clock

1   Reserved (0)

2   Shift Load

    0   Load video data shift registers <u>every</u> character clock
    1   Load video data shift registers <u>every other</u> character clock

Bit-4 of this register must be 0 for this bit to be effective.

3   Input Clock Divide

    0   Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
    1   Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4   Shift 4

    0   Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
    1   Load shift registers every 4th character clock.

5   Screen Off

    0   Normal Operation
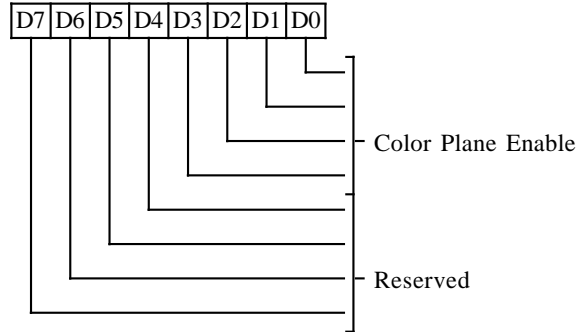   1   Disable video output and assign all display memory bandwidth for CPU accesses

7-6   Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)
Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection

3-0   Color Plane Enable

    0   Write protect corresponding color plane
    1   Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.
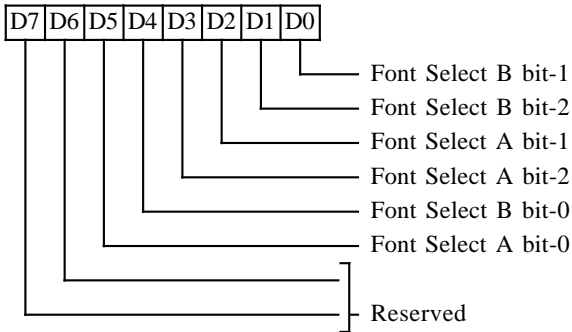
7-4   Reserved (0)

**CHARACTER FONT SELECT
REGISTER (SR03)**
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection

D7	D6	D5	D4	D3	D2	D1	D0

Font Select B bit-1
Font Select B bit-2
Font Select A bit-1
Font Select A bit-2
Font Select B bit-0
Font Select A bit-0

Reserved

In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B

3-2 High order bits of Character Generator Select A

4 Low order bit of Character Generator Select B

5 Low order bit of Character Generator Select A

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.
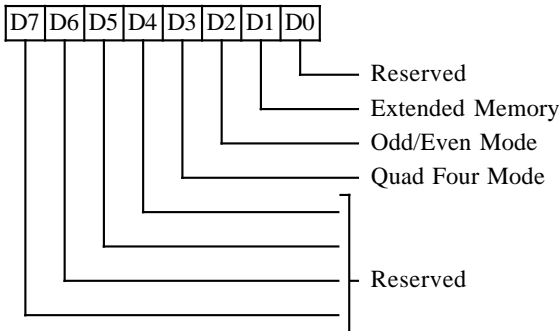
**SEQUENCER MEMORY MODE
REGISTER (SR04)**
Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0

- Reserved
- Extended Memory
- Odd/Even Mode
- Quad Four Mode

- Reserved

0   Reserved (0)

1   Extended Memory

   0   Restrict CPU access to 4/16/32 Kbytes
   1   Allow complete access to memory

   This bit should normally be 1.

2   Odd/Even Mode

   0   CPU accesses to Odd/Even addresses
        are directed to corresponding odd/even
        planes
   1   All planes are accessed simultaneously
        (IRGB color)

   Bit-3 of this register must be 0 for this bit to
   be effective. This bit affects only CPU <u>write</u>
   accesses to display memory.

3   Quad Four Mode

   0   CPU addresses are mapped to display
        memory as defined by bit-2 of this
        register
   1   CPU addresses are mapped to display
        memory modulo 4.   The two low
        order CPU address bits select the dis-
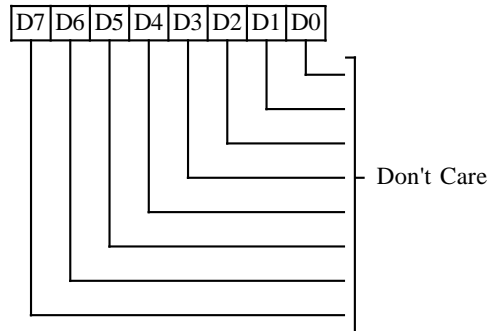   play memory plane.

   This bit affects both CPU reads and writes
   to display memory.

7-4   Reserved (0)

**SEQUENCER HORIZONTAL CHARACTER
COUNTER RESET (SR07)**
Read/Write at I/O Address 3C5h
Index 07h

D7 D6 D5 D4 D3 D2 D1 D0

- Don't Care

Writing to SR07 with any data will cause the
horizontal character counter to be held reset
(character counter output = 0) until a write to any
other sequencer register with any data value. The
write to any index in the range 0-6 clears the latch
that is holding the reset condition on the character
counter.

The vertical line counter is clocked by a signal
derived from horizontal display enable (which does
not occur if the horizontal counter is held reset).
Therefore, if the write to SR07 occurs during vertical
retrace, the horizontal and vertical counters will both
be set to zero. A write to any other sequencer
register may then be used to start both counters with
reasonable synchronization to an external event via
software control.

*This is a standard VGA register which was not
documented by IBM.*

CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	42
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	42
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	42
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	43
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	43
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	44
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	44
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	45
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	45
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	46
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	46
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	47
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	47
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	48
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	48
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	48
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	48
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	49
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	49
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	49
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	49
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	50
CR13	Offset	13h	RW	3B5h/3D5h	3	50
CR14	Underline Row	14h	RW	3B5h/3D5h	3	50
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	51
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	51
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	52
CR18	Line Compare	18h	RW	3B5h/3D5h	3	53
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	54
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	54
CR3x	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	54

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B4h-3B5h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D4h-3D5h by setting Misc Output Register bit-0 to 1.

Note 2: In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 bit-7) of whether the vertical sync or light pen registers are readable at indices 10-11.
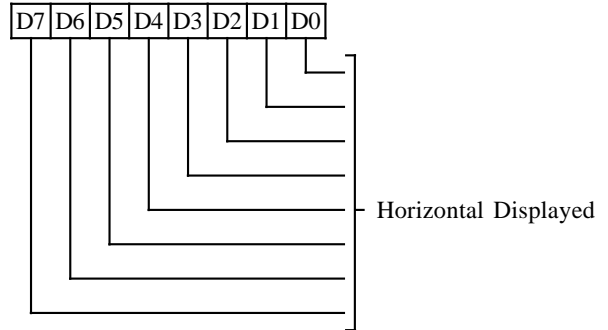
CRTC INDEX REGISTER (CRX)
Read/Write at I/O Address 3B4h/3D4h
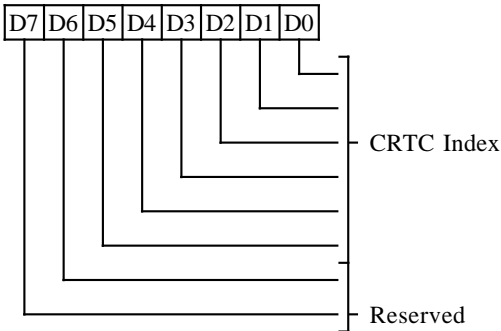
5-0   CRTC data register index

7-6   Reserved (0)

HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 protection

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   Horizontal Total

Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
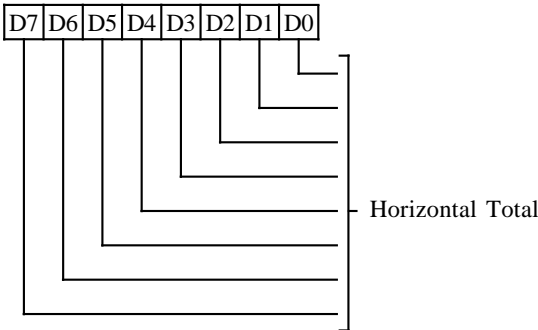*Index 01h*
Group 0 protection

This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   Horizontal Displayed

This register should be programmed to hold the number of characters displayed per scan line – 1.

**HORIZONTAL BLANK START
REGISTER (CR02)**
Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
— H Blank Start

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   Horizontal Blank Start

These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

**HORIZONTAL BLANK END
REGISTER (CR03)**
Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 protection

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```
— H Blank End
— DE Skew Control
— Light Pen Reg. Enable

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0   Horizontal Blank End

These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] and 1Fh. The most significant bit is programmed in CR05 bit-7. This bit = [(CR02 + W) and 20h]/20h.

6-5   Display Enable Skew Control

Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7   Light Pen Register Enable

Must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.
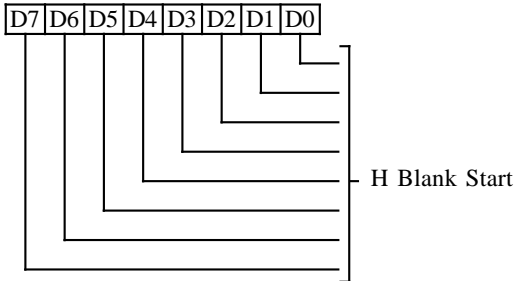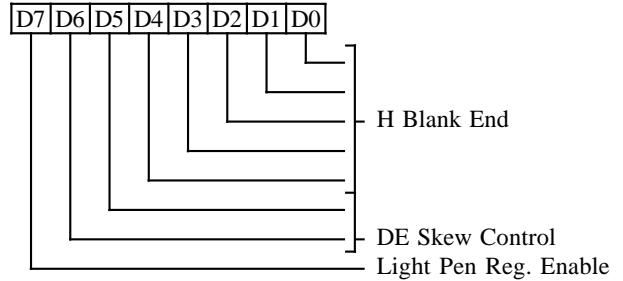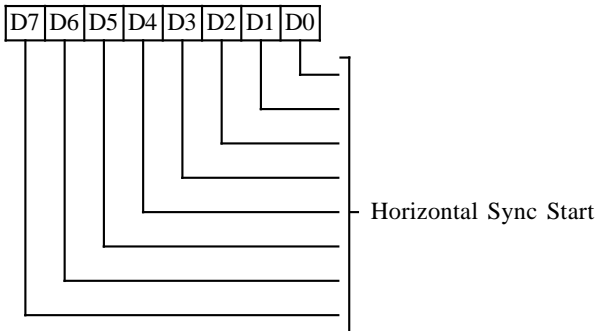
**HORIZONTAL SYNC START
REGISTER (CR04)**
Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 protection

This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0   Horizontal Sync Start

These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

**HORIZONTAL SYNC END
REGISTER (CR05)**
Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 protection
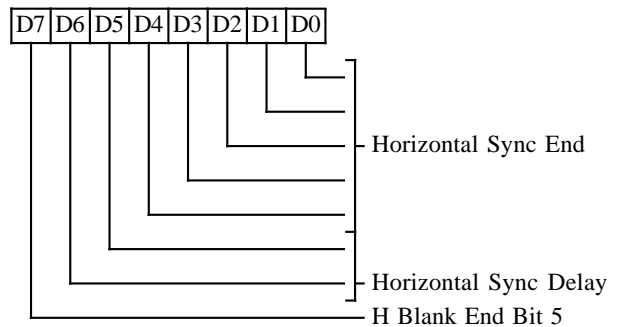
This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0   Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) and 1Fh.

6-5   Horizontal Sync Delay

These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7   Horizontal Blank End Bit 5

Sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)
Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 protection

```
D7 D6 D5 D4 D3 D2 D1 D0
```
V Total (Scan Lines)
(Lower 8 Bits)
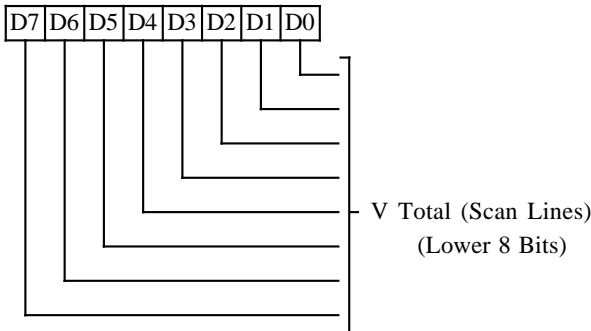
This register is used in all modes.

7-0   Vertical Total

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count – 2

OVERFLOW REGISTER (CR07)
Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 protection on bits 0-3 and bits 5-7
Group 3 protection on bit 4

```
D7 D6 D5 D4 D3 D2 D1 D0
```
V Total Bit 8
V DE End Bit 8
V Sync Start Bit 8
V Blank Start Bit 8
Line Compare Bit 8
V Total Bit 9
V DE End Bit 9
V Sync Start Bit 9
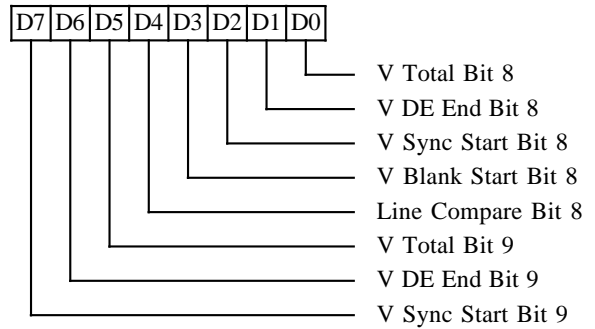
This register is used in all modes.

0   Vertical Total Bit 8

1   Vertical Display Enable End Bit 8

2   Vertical Sync Start Bit 8

3   Vertical Blank Start Bit 8

4   Line Compare Bit 8

5   Vertical Total Bit 9

6   Vertical Display Enable End Bit 9

7   Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)
Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection

MAXIMUM SCAN LINE REGISTER (CR09)
Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 protection on bits 0-4
Group 4 Protection on bits 5-7

D7	D6	D5	D4	D3	D2	D1	D0

- Start Row Scan Count
- Byte Panning Control
- Reserved

D7	D6	D5	D4	D3	D2	D1	D0

- Scan Lines Per Row
- V Blank Start Bit 9
- Line Compare Bit 9
- Double Scan
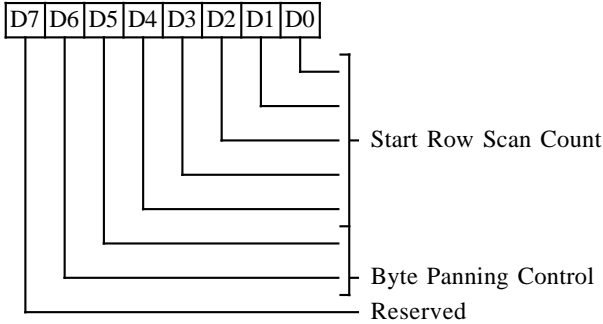
4-0   Start Row Scan Count

These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

6-5   Byte Panning Control

These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7   Reserved (0)

4-0   Scan Lines Per Row

These bits specify the number of scan lines in a row: Number of scan lines per row = value + 1.

5   Bit 9 of the Vertical Blank Start register

6   Bit 9 of the Line Compare register

7   Double Scan

    0   Normal Operation
    1   Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

**CURSOR START SCAN LINE
REGISTER (CR0A)**
Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection
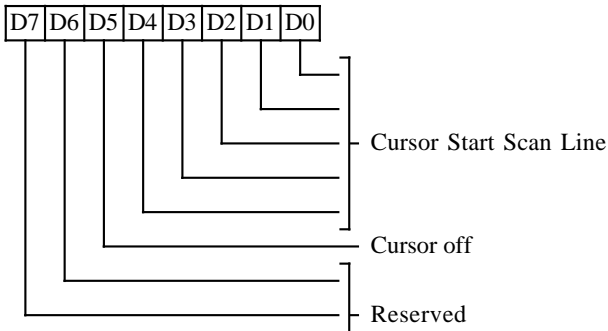
4-0   Cursor Start Scan Line

These bits specify the scan line of the
character row where the cursor display
begins.

5   Cursor Off

0   Text Cursor On
1   Text Cursor Off

7-6   Reserved (0)

**CURSOR END SCAN LINE
REGISTER (CR0B)**
Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 protection
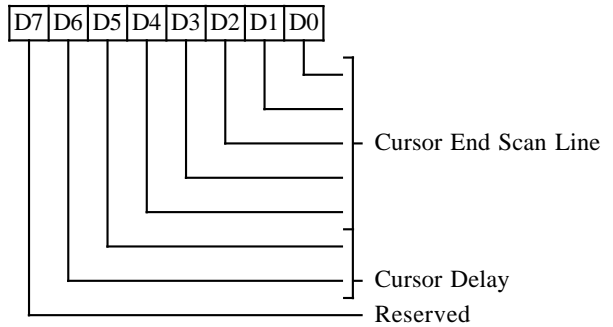
4-0   Cursor End Scan Line

These bits specify the scan line of a character
row where the cursor display ends: Last
scan line for the block cursor = Value + 1.

6-5   Cursor Delay

These bits define the number of character
clocks that the cursor is delayed to
compensate for internal pipeline delay.

7   Reserved (0)

Note: If the Cursor Start Line is greater than the
Cursor End Line, then no cursor is generated.

START INDEX HIGH REGISTER (CR0C)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Display Start Index High
(Upper 8 bits)
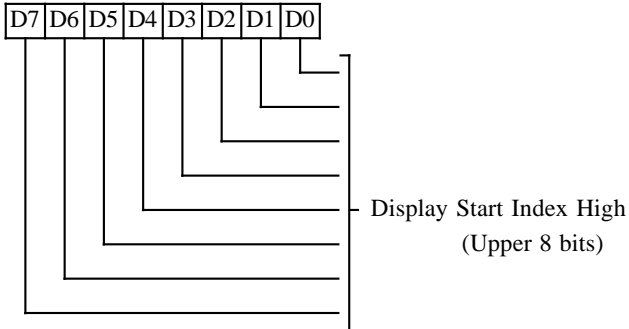
7-0   Display Start Index High

Upper 8 bits of display start address. In
CGA/MDA/Hercules modes, this register
wraps around at the 16, 32, and 64 Kbyte
boundaries respectively.

**CURSOR LOCATION HIGH
REGISTER (CR0E)**
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Mem. Index
ρper 8 bits)
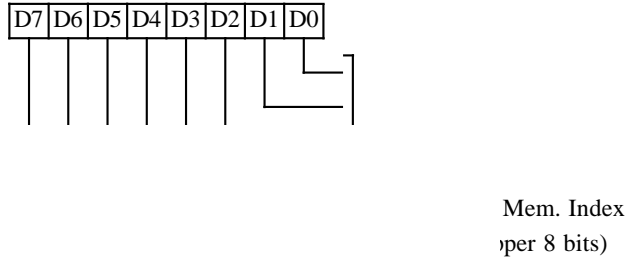
7-0   Text Cursor Memory Index High

Upper 8 bits of the memory address where
the text cursor is active.   In
CGA/MDA/Hercules modes, this register
wraps around at 16, 32, and 64 Kbyte
boundaries respectively.

START INDEX LOW REGISTER (CR0D)
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Display Start Index Low
(Lower 8 bits)

7-0   Display Start Index Low

Lower 8 bits of the display start address.
The display start address points to the
memory address corresponding to the top
left corner of the screen.

**CURSOR LOCATION LOW
REGISTER (CR0F)**
Read/Write at I/O Address 3B5h/3D5h
Index 0Fh

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Text Cursor Mem. Index
(Lower 8 bits)
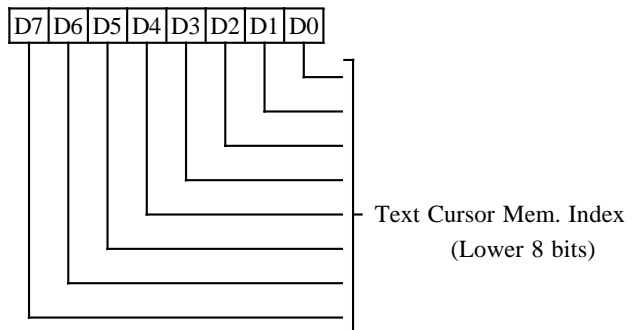
7-0   Text Cursor Memory Index Low

Lower 8 bits of the memory address where
the text cursor is active.   In
CGA/MDA/Hercules modes, this register
wraps around at 16, 32, and 64 Kbyte boun-
daries respectively.

LIGHTPEN HIGH REGISTER (CR10)
Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

LIGHTPEN LOW REGISTER (CR11)
Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)
Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

V Sync Start
(Lower 8 bits)
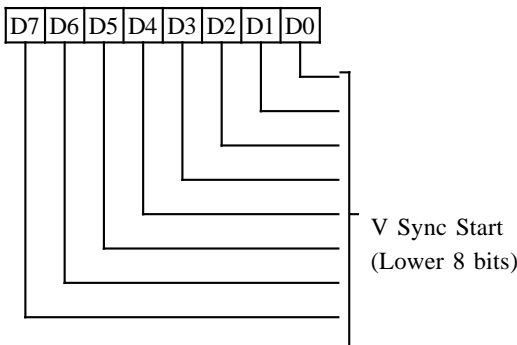
This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 bit-7=1.

7-0   Vertical Sync Start

The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)
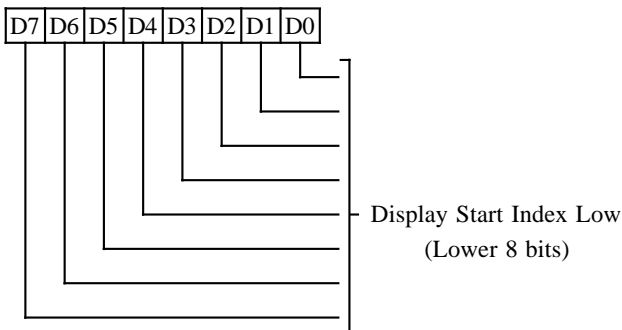*Read/Write at I/O Address 3B5h/3D5h*
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6 and 7

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

V Sync End
V Interrupt Clear
V Interrupt Enable
Select Refresh Type
Protect CRTC (Group 0)
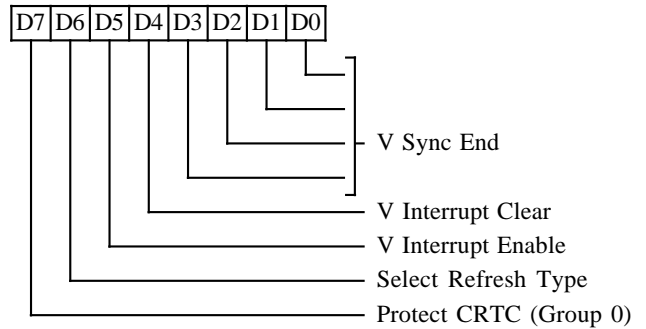
This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 bit-7=1.

3-0   Vertical Sync End

Lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4   Vertical Interrupt Clear

0   Clear vertical interrupt generated on the IRQ output (default on reset)
1   Normal operation

5   Vertical Interrupt Enable

0   Enable vertical interrupt (default)
1   Disable vertical interrupt

6   Select Refresh Type

0   3 refresh cycles per scan line
1   5 refresh cycles per scan line

7   Group Protect 0

This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0   Enable writes to CR00-CR07
1   Disable writes to CR00-CR07

CR07 bit-4 (Line Compare bit-9) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)
Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 protection
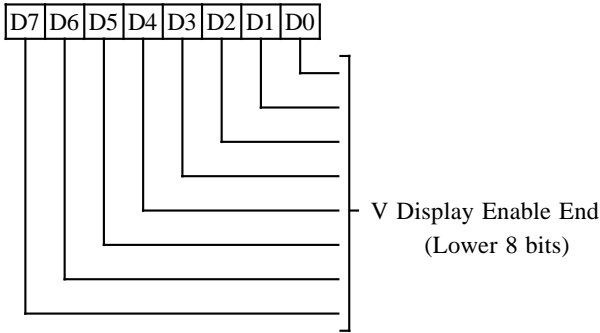
7-0   Vertical Display Enable End

These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 protection
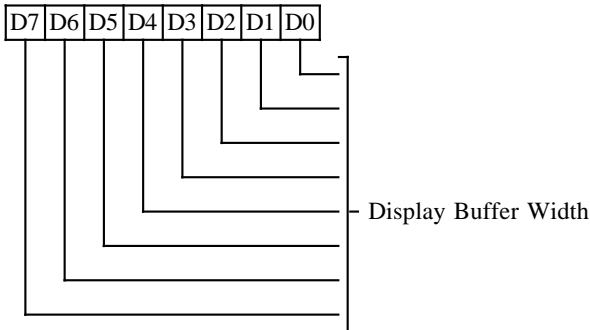
7-0   Display Buffer Width

The byte starting address of the next display row = Byte Start Address for current row + K * (CR13 + Z/2), where Z = bit defined in XR0D and K = 2 in byte mode, K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)
Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 protection
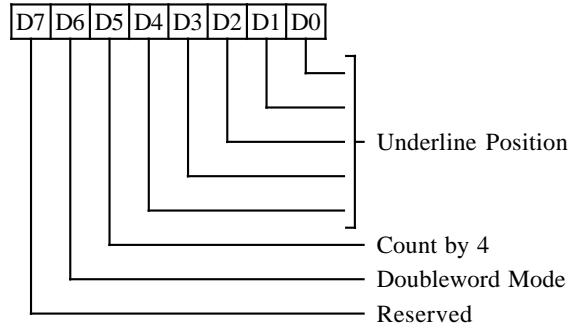
4-0   Underline Position

These bits specify the underline's scan line position within a character row. Value = Actual scan line number - 1.

5   Count by 4 for Doubleword Mode

0 Display Memory Address is incremented by 1 or 2
1 Display Memory Address is incremented by 4 or 2

See CR17 bit-3 for further details.

6   Doubleword Mode

0 Display Memory Address is a byte or word address
1 Display Memory Address is a doubleword address

This bit is used in conjunction with CR17 bit-6 to select the display memory addressing mode.

7   Reserved (0)

VERTICAL BLANK START REGISTER (CR15)
Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 protection
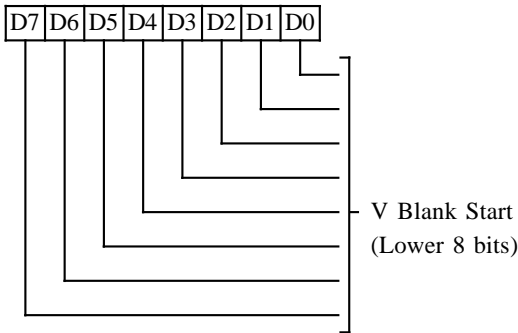
This register is used in all modes.

7-0   Vertical Blank Start

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)
Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 protection
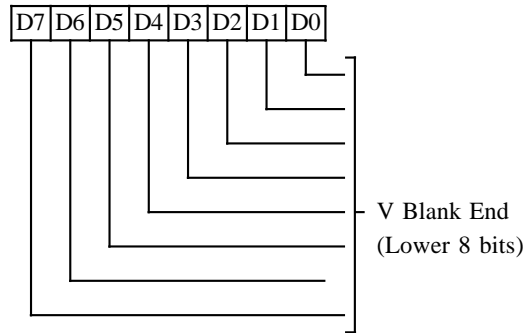
This register is used in all modes.

7-0   End Vertical Blank

These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)
Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0,1 and 3-7
Group 4 Protection for bit 2.

D7	D6	D5	D4	D3	D2	D1	D0

Compatibility Mode
Select Row Scan Ctr
Vsync Select
Count by 2
Reserved
Address Wrap
Word/Byte Mode
CRTC Reset
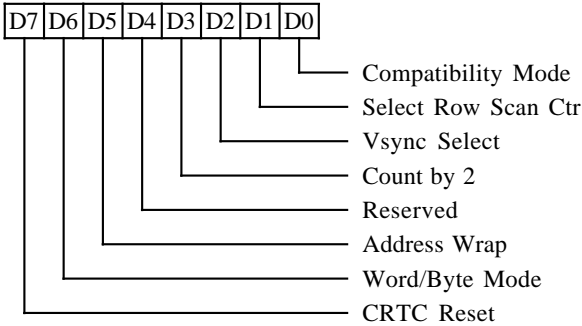
0   Compatibility Mode Support

This bit allows compatibility with the IBM CGA two-bank graphics mode.

0   The character row scan line counter bit 0 is substituted for memory address bit 13 during active display time.
1   Normal operation, no substitution takes place.

1   Select Row Scan Counter

This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

0   Substitute character row scan line counter bit 1 for memory address bit 14 during active display time.
1   Normal operation, no substitution takes place.

2   Vertical Sync Select

This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3   Count By Two

0   Memory address counter is incremented every character clock.
1   Memory address counter is incremented every two character clocks, used in conjunction with bit-5 of 0Fh.

Note: This bit is used in conjunction with CR14 bit-5. The net effect is as follows:

		Increment Addressing
CR14 bit-5	CR17 bit-3	Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, the address inrements every two clocks.

4   Reserved (0)

5   Address Wrap

This bit is effective only in word mode.

0   Wrap display memory address at 16 Kbytes. This is used in IBM CGA mode.
1   Normal operation (extended mode)

6   Word Mode or Byte Mode

0   Select Word Mode. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output.
1   Select Byte Mode

Note: This bit is used in conjunction with CR14 bit-6 to select byte, word, or double word memory addressing as follows:

CR14 bit-6	CR17 bit-6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7   Hardware Reset

This bit is cleared by RESET

0   Force HSYNC and VSYNC to be inactive. No other registers or outputs are affected.
1   Normal Operation

Display memory addresses are affected by CR17 bit-6 as shown in the table below:

Logical Memory Address	Physical Memory Address		
	Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * not CR17 bit-5 + A15 * CR17 bit-5
Note 2 = A12 xor (A14 * XR04 bit-2)
Note 3 = A13 xor (A15 * XR04 bit-2)

LINE COMPARE REGISTER (CR18)
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Line Compare Target
(Lower 8 bits)
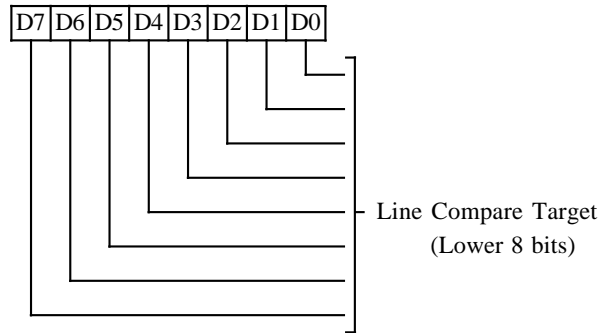
7-0 Line Compare Target

These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 bit-7).

MEMORY DATA LATCH REGISTER (CR22)
Read only at I/O Address 3B5h/3D5h
Index 22h

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └── Data Latch n Bit 7
                  └───── Data Latch n Bit 6
               └──────── Data Latch n Bit 5
            └─────────── Data Latch n Bit 4
         └────────────── Data Latch n Bit 3
      └───────────────── Data Latch n Bit 2
   └──────────────────── Data Latch n Bit 1
└─────────────────────── Data Latch n Bit 0
```
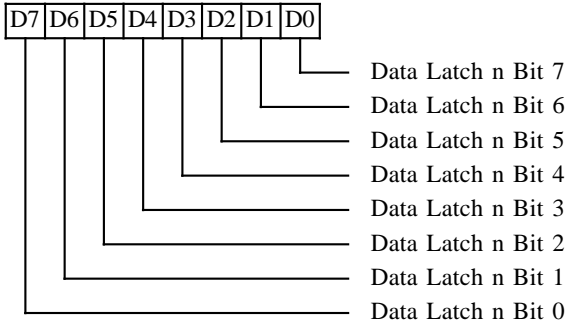
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 bits 0&1) and is in the range 0-3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)
Read only at I/O Address 3B5h/3D5h
Index 24h

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └── Index (0) / Data (1)
                  └───── Reserved
               └──────── Palette Address Source
            └─────────┐
         └──────────┐ │  Attribute
      └───────────┐ │ │  Controller
   └────────────┐ │ │ │  Index
└─────────────────────┘
```
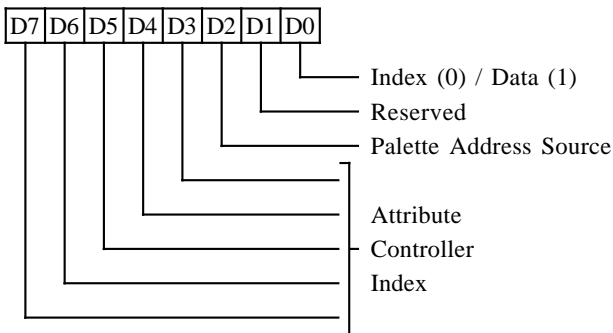
This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

CLEAR VERTICAL DISPLAY ENABLE FFh (CR3X)
Write only at I/O Address 3B5h/3D5h
Index 3xh

```
D7 D6 D5 D4 D3 D2 D1 D0
                     └── Clear Vert Disp Ena FF
            └─────────┐
         └──────────┐ │
      └───────────┐ │ │  Ignored
   └────────────┐ │ │ │
└─────────────────────┘
```
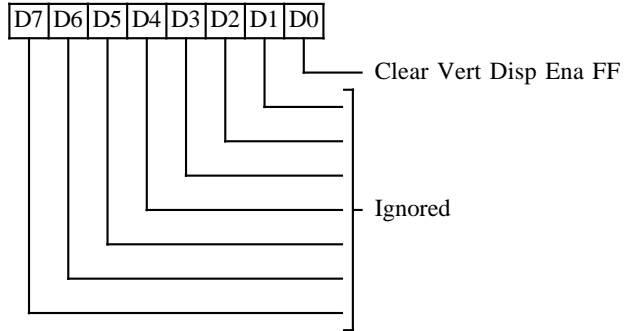
Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

Reads from this register are not decoded and will return indeterminate data.

This is a standard VGA register which was not documented by IBM.

Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	RW	3CEh	1	55
GR00	Set/Reset	00h	RW	3CFh	1	55
GR01	Enable Set/Reset	01h	RW	3CFh	1	56
GR02	Color Compare	02h	RW	3CFh	1	56
GR03	Data Rotate	03h	RW	3CFh	1	57
GR04	Read Map Select	04h	RW	3CFh	1	57
GR05	Graphics mode	05h	RW	3CFh	1	58
GR06	Miscellaneous	06h	RW	3CFh	1	60
GR07	Color Don't Care	07h	RW	3CFh	1	60
GR08	Bit Mask	08h	RW	3CFh	1	61

GRAPHICS CONTROLLER INDEX REGISTER (GRX)
Write only at I/O Address 3CEh
Group 1 Protection
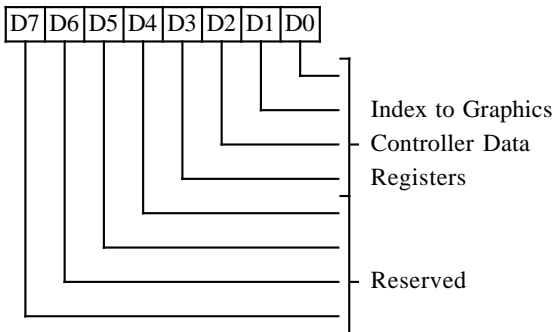
3-0   Graphics Controller Index

4-bit index to Graphics Controller registers

7-4   Reserved (0)

SET/RESET REGISTER (GR00)
Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection
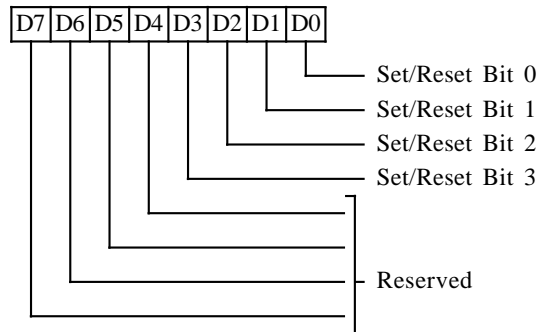
The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

3-0   Set / Reset

When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Rest register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4   Reserved (0)

ENABLE SET/RESET REGISTER (GR01)
Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
— Enable Set/Reset Bit 0
— Enable Set/Reset Bit 1
— Enable Set/Reset Bit 2
— Enable Set/Reset Bit 3
— Reserved
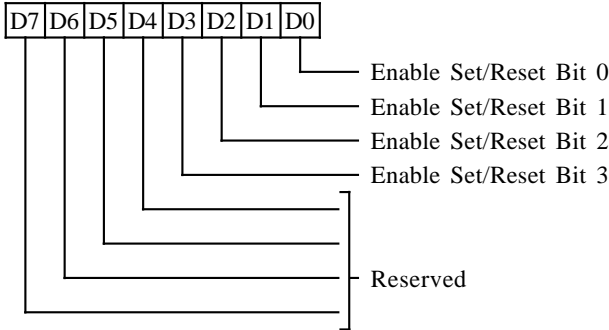
3-0   Enable Set / Reset

This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

   0   The corresponding plane is written with the data from the CPU data bus
   1   The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4   Reserved (0)

COLOR COMPARE REGISTER (GR02)
Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection

D7 D6 D5 D4 D3 D2 D1 D0
— Color Compare (Plane 0)
— Color Compare (Plane 1)
— Color Compare (Plane 2)
— Color Compare (Plane 3)
— Reserved
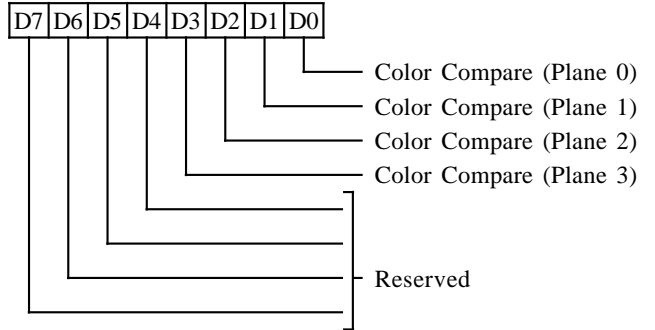
3-0   Color Compare

This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3.   The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit, a mis-match returns a logical 0.

7-4   Reserved (0)

DATA ROTATE REGISTER (GR03)
Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection

2-0   Rotate Count

These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3   Function Select

These bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

7-5   Reserved (0)

READ MAP SELECT REGISTER (GR04)
Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection

2-0   Rotate Count

This register is also used to 'reduced' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits selected the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	1	Plane 2
1	1	Plane 3

7-2   Reserved (0)

DATA ROTATE REGISTER (GR03)
Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection

```
D7 D6 D5 D4 D3 D2 D1 D0
                      └──── Rotate Count 0
                   └─────── Rotate Count 1
                └────────── Rotate Count 2
          └──────────────── Function Select
    └──────────────────────── Reserved
```

2-0   Rotate Count

These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3   Function Select

These bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

7-5   Reserved (0)

READ MAP SELECT REGISTER (GR04)
Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection

```
D7 D6 D5 D4 D3 D2 D1 D0
                      └──── Map Select 0
                   └─────── Map Select 1
          └──────────────── Reserved
```

1-0   Map Select

This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2   Reserved (0)

GRAPHICS MODE REGISTER (GR05)
Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection

```
D7 D6 D5 D4 D3 D2 D1 D0
```

Write Mode
Reserved
Read Mode
Odd/Even Mode
Shift Register Mode
Reserved
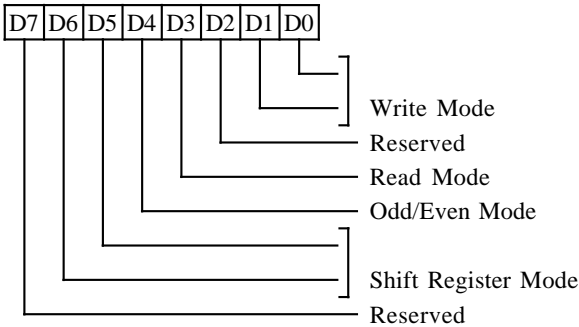
1-0   Write Mode

(For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data.)

Bit 1 Bit 0 Write Mode
0   0   **Write mode 0**. Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.

0   1   **Write mode 1**. Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.

1   0   **Write mode 2**. The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0

in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.

1   1   **Write mode 3**. The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value.

A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches.

A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register.

The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2   Reserved (0)

3   Read Mode

0   The CPU reads data from one of the planes as selected in the Read Map Select register.

1   The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4   Odd/Even Mode

0   All CPU addresses sequentially access all planes

1   Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for IBM CGA-compatible memory organization.

6-5   Shift Register Mode

These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If the data bits in the memory planes (0-3) are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

Bit 65	Last Bit Shifted Out			Shift ⟶ Direction			1st Bit Shifted Out	Output to:
00	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit3
01	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit3
1x	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit1
	M3D2	M2D6	M3D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit3

Note: If the Shift Register is not loaded every character clock (see SR01 bits 2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

7   Reserved (0)

MISCELLANEOUS REGISTER (GR06)
Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

— Graphics/Text Mode
— Chain Odd/Even Planes

— Memory Map Mode

— Reserved
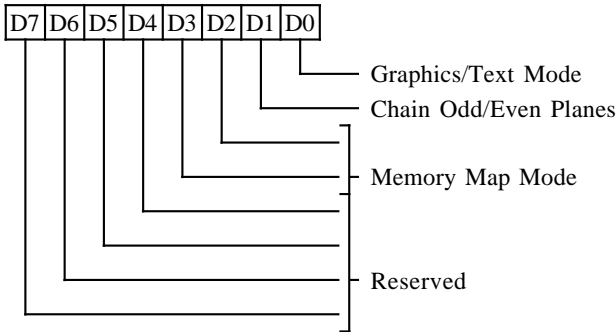
0   Graphics/Text Mode

  0   Text Mode
  1   Graphics mode

1   Chain Odd/Even Planes

This mode can be used to double the address space into display memory.

  1   CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:
      A0 = 0 select planes 0 and 2
      A0 = 1 select planes 1 and 3
  0   A0 not replaced

3-2 Memory Map mode

These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)
Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

— Ignore Color Plane 0
— Ignore Color Plane 1
— Ignore Color Plane 2
— Ignore Color Plane 3

— Reserved
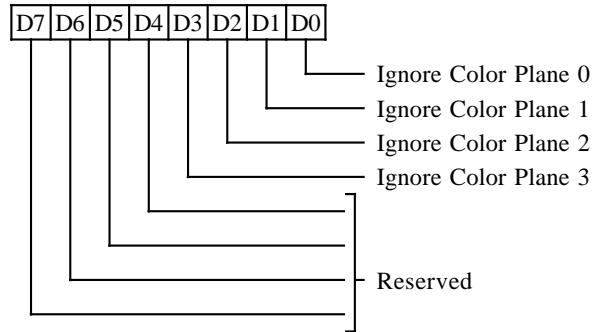
3-0 Ignore Color Plane (0-3)

  0   This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.
  1   The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

0=Immune to change
1=Change permitted
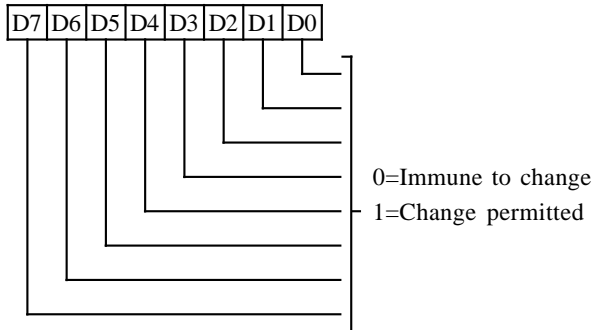
7-0   Bit Mask

The bit mask is applicable to any data writ-
ten by the CPU, including that subject to a
rotate, logical function (AND, OR, XOR),
Set/Reset, and No Change. In order to
execute a proper read-modify-write cycle
into displayed memory, each byte must first
be read (and latched by the VGA), the Bit
Mask register set, and the new data then
written. The bit mask applies to all four
planes simultaneously.

0   The corresponding bit in each of the
four memory planes is written from
the corresponding bit in the latches.

1   Unrestricted manipulation of the
corresponding data bit in each of the
four memory planes is permitted.

Attribute Controller
and Color Palette Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	63
AR00-AR0F	Internal Color Palette Data	00-0Fh	RW	3C0h/3C1h	1	64
AR10	Mode Control	10h	RW	3C0h/3C1h	1	64
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	65
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	65
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	66
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	66
DACMASK	External Color Palette Pixel Mask	–	RW	3C6h	6	67
DACSTATE	DAC State	–	R	3C7h	–	67
DACRX	External Color Palette Read-Mode Index	–	W	3C7h	6	68
DACX	External Color Palette Index (for 3C9h)	–	RW	3C8h	6	68
DACDATA	External Color Palette Data	00-FFh	RW	3C9h	6	68

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection
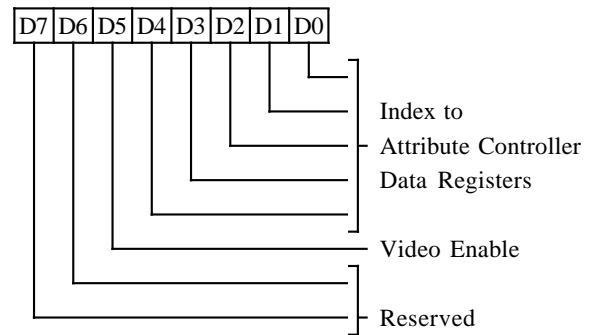
4-0   Atribute Controller Index

These bits point to one of the internal registers of the Attribute Controller.

5   Enable Video

    0   Disables the video, allowing the Attribute Controller color registers to be accessed by the CPU.

    1   Enables the video and causes the Attribute Controller Color registers (AR00-AR0F) to be inaccessible by the CPU.

7-6   Reserved (0)

ATTRIBUTE CONTROLLER COLOR PALETTE DATA REGISTERS (AR00-AR0F)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63D6

D7	D6	D5	D4	D3	D2	D1	D0

- Blue
- Green
- Red
- Secondary Blue
- Secondary Green
- Secondary Red
- Reserved
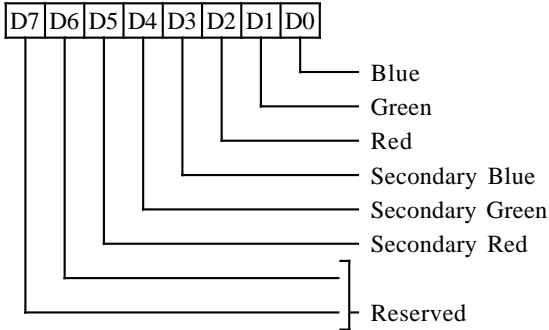
5-0   Color Data

These bits are the color value in the respective palette register as pointed to by the index register.

7-6   Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection

D7	D6	D5	D4	D3	D2	D1	D0

- Text/Graphics Mode
- Mono/Color Display
- Enable Line Graphics
- Select Background
- Reserved
- Horizontal Split Screen
- 256 Color
- Video Output 4-5 Select
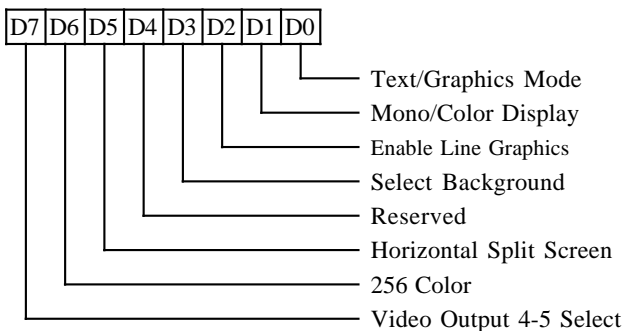
0   Text/Graphics Mode

- 0   Select text mode
- 1   Select graphics mode

1   Monochrome/Color Display

- 0   Select color display attributes
- 1   Select mono display attributes

2   Enable Line Graphics Character Codes

This bit is dependent on bit 0 of the Override register.

- 0   Make the ninth pixel appear the same as the background
- 1   For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3   Enable Blink/Select Background Intensity

The blink counter is clocked by VSYNC

- 0   Disable Blinking and enable text mode background intensity
- 1   Enable the blink attribute in text and graphics modes.

4   Reserved (0)

5   Split Screen Horizontal Panning Mode

- 0   Scroll both screens horizontally as specified in the Pixel Panning register
- 1   Scroll horizontally only the top screen as specified in the Pixel panning register

6   256 Color Output Assembler

- 0   6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock
- 1   Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

7   Video Output 5-4 Select

- 0   Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers
- 1   Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
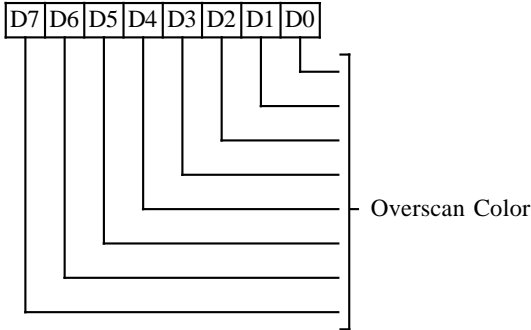
— Overscan Color

7-0　Overscan Color

These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

— Color Plane 0 Enable
— Color Plane 1 Enable
— Color Plane 2 Enable
— Color Plane 3 Enable
— Display Status Select
— Reserved
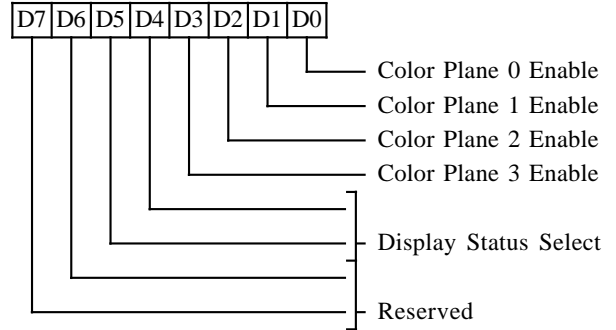
3-0　Color Plane (0-3) Enable

　0　Force the corresponding color plane pixel bit to 0 before it addresses the color palette
　1　Enable the plane data bit of the corresponding color plane to pass

5-4　Display Status Select

These bits select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6　Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)
Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection
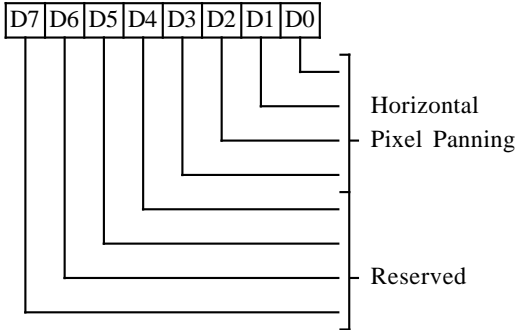
3-0   Horizontal Pixel Panning

These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixels/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixels/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 bit-6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
	9-dot	8-dot	256-color
AR13	Mode	Mode	Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4   Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)
Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection
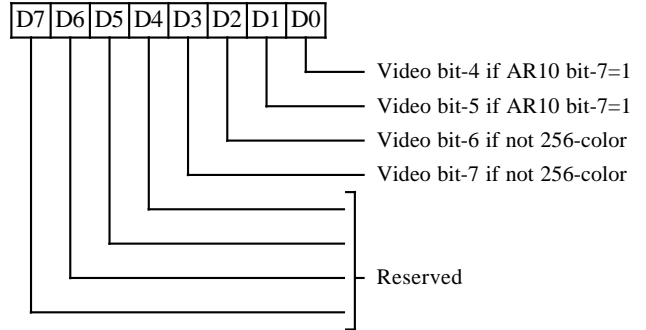
1-0   Pixel Pad 5-4

These bits are output as video bits 5 and 4 when AR10 bit-7 = 1. They are disabled in the 256 color mode.

3-2   Pixel Pad 7-6

These bits are output as video bits 7 and 6 in all modes except 256-color mode.

7-4   Reserved (0)

**EXTERNAL COLOR PALETTE
PIXEL MASK REGISTER (DACMASK)**
Read/Write at I/O Address 3C6h
Group 6 Protection

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Pixel Mask Bit-0
Pixel Mask Bit-1
Pixel Mask Bit-2
Pixel Mask Bit-3
Pixel Mask Bit-4
Pixel Mask Bit-5
Pixel Mask Bit-6
Pixel Mask Bit-7
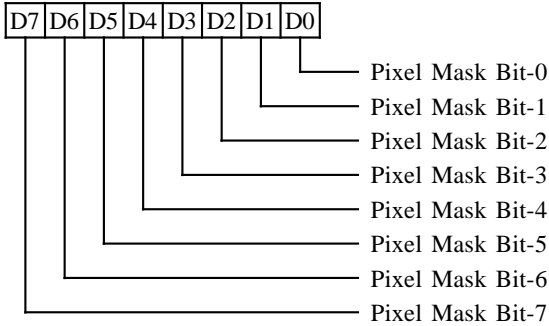
7-0   Pixel Mask

The contents of this register are logically ANDed with the 8 bits of video data coming into the external color palette. Zero bits in this register therefore cause the corresponding address input to the external color palette to be zero. For example, if this register is programmed with 7, only external color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located in the external color palette chip (used for displaying analog data to the CRT). Reads from this I/O location cause the PALRD/ pin to be asserted. Writes to this I/O location cause the PALWR/ pin to be asserted. The functionality of this port is determined by the external palette chip.

**EXTERNAL COLOR PALETTE
STATE REGISTER (DACSTATE)**
Read only at I/O Address 3C7h

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Palette State 0
Palette State 1
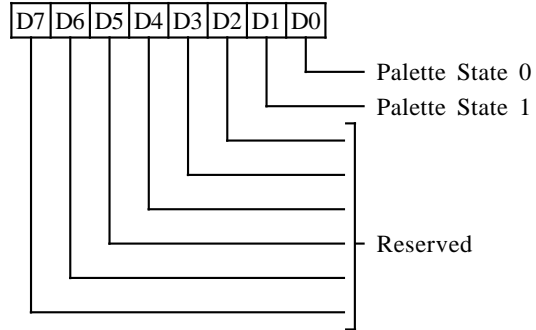
Reserved

1-0   Color Palette State

Status bits indicate the I/O address of the last CPU write to the external DAC/Color Palette:

00   The last write was to 3C8h (write mode)
11   The last write was to 3C7h (read mode)

7-2   Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the external color palette chip automatically increments its index register differently depending on whether the index is written at 3C7h or 3C8h.

This register is physically located in the 64200 chip (PALRD/ is *not* asserted for reads from this I/O address).

**EXTERNAL COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)**
Write only at I/O Address 3C7h
Group 6 Protection

**EXTERNAL COLOR PALETTE
INDEX REGISTER (DACX)**
Read/Write at I/O Address 3C8h
Group 6 Protection

D7	D6	D5	D4	D3	D2	D1	D0

Color Palette Index 0
Color Palette Index 1
Color Palette Index 2
Color Palette Index 3
Color Palette Index 4
Color Palette Index 5
Color Palette Index 6
Color Palette Index 7
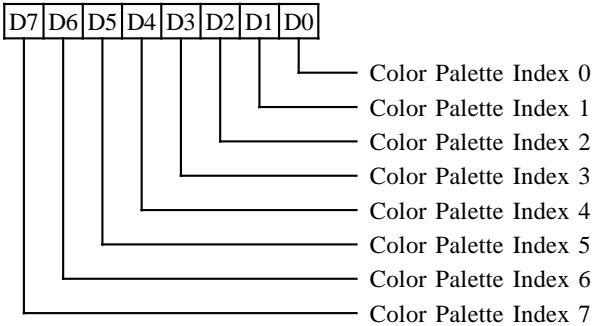
**EXTERNAL COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)**
Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection

D7	D6	D5	D4	D3	D2	D1	D0

	Access	
1st	2nd	3rd
Red 0	Green 0	Blue 0
Red 1	Green 1	Blue 1
Red 2	Green 2	Blue 2
Red 3	Green 3	Blue 3
Red 4	Green 4	Blue 4
Red 5	Green 5	Blue 5
(Red 6)	(Green 6)	(Blue 6)
(Red 7)	(Green 7)	(Blue 7)
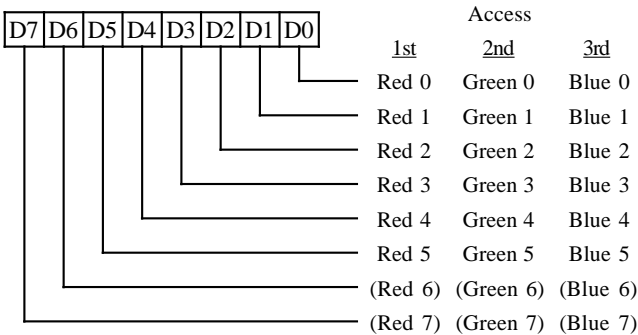
The color palette index and data registers are physically located in the external color palette chip. The index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette chip).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register internal to the color palette chip. The save register (not the index register) is used internally by the palette chip to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette chip. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette chip internal RGB sequence counter.

The palette chip internal save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The 64200 therefore saves the state of which port (3C7h or 3C8h) was last written and returns that information on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and not on reads from 3C7h). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted.

The functionality of the index and data ports is determined by the external palette chip.

Extension Registers

Register Mnemonic	Register Group	Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	--	Extension Index	--	RW	3D6h	- x x x x x x x	70
XR00	Misc	Chip Version	00h	R	3D7h	1 0 1 0 r r r r	70
XR01	Misc	Configuration	01h	R	3D7h	d d d d d d d d	71
XR02	Misc	CPU Interface	02h	RW	3D7h	0 0 0 0 0 - - -	72
XR0D	Misc	Auxiliary Offset	0Dh	RW	3D7h	- - - - - - 0 0	76
XR0E	Misc	Text Mode Control	0Eh	RW	3D7h	- - - - 0 0 - -	76
XR28	Misc	Video Interface	28h	RW	3D7h	- - 0 - - 0 0 0	84
XR2B	Misc	Default Video	2Bh	RW	3D7h	0 0 0 0 0 0 0 0	84
XR70	Misc	Setup / Disable Control	70h	RW	3D7h	0 - - - - - - -	86
XR7F	Misc	Diagnostic	7Fh	RW	3D7h	0 0 x x x x 0 0	87
XR04	Mapping	Memory Mapping	04h	RW	3D7h	- - 0 - - 0 - 0	74
XR0B	Mapping	CPU Paging	0Bh	RW	3D7h	- - - - - 0 0 0	75
XR0C	Mapping	Start Address Top	0Ch	RW	3D7h	- - - - - - - 0	75
XR10	Mapping	Single/Low Map	10h	RW	3D7h	x x x x x x x x	77
XR11	Mapping	High Map	11h	RW	3D7h	x x x x x x x x	77
XR14	Compatibility	Emulation Mode	14h	RW	3D7h	0 0 0 0 h h 0 0	78
XR15	Compatibility	Write Protect	15h	RW	3D7h	0 0 0 0 0 0 0 0	79
XR1F	Compatibility	Virtual EGA Switch	1Fh	RW	3D7h	0 - - - x x x x	83
XR7E	Compatibility	CGA Color Select	7Eh	RW	3D7h	- - x x x x x x	86
XR18	Alternate	Alternate Horizontal Display End	18h	RW	3D7h	x x x x x x x x	80
XR19	Alternate	Alt H Sync Start / Half Line Compare	19h	RW	3D7h	x x x x x x x x	80
XR1A	Alternate	Alternate Horizontal Sync End	1Ah	RW	3D7h	x x x x x x x x	81
XR1B	Alternate	Alternate Horizontal Total	1Bh	RW	3D7h	x x x x x x x x	81
XR1C	Alternate	Alternate Horizontal Blank Start	1Ch	RW	3D7h	x x x x x x x x	82
XR1D	Alternate	Alternate Horizontal Blank End	1Dh	RW	3D7h	0 x x x x x x x	82
XR1E	Alternate	Alternate Offset	1Eh	RW	3D7h	x x x x x x x x	83
XR03	Wingine™	Master Control	03h	RW	3D7h	0 0 0 0 - - 0 0	73
XR3C	Wingine™	Serial / Row Count	3Ch	RW	3D7h	- - x x x x x x	85
XR3D	Wingine™	Multiplexer Mode	3Dh	RW	3D7h	- - x x x x x x	85

Reset Codes: x = Not changed by RESET (indeterminate on power-up)   - = Not implemented (always reads 0)
d = Set from the corresponding data bus pin on falling edge of RESET   r = Chip revision # (starting from 0000)
h = Read-only Hercules Configuration Register Readback bits   0/1 = Reset to 0/1 by falling edge of RESET

EXTENSION INDEX REGISTER (XRX)
Read/Write at I/O Address 3D6h

D7	D6	D5	D4	D3	D2	D1	D0

Index to
Extension Registers
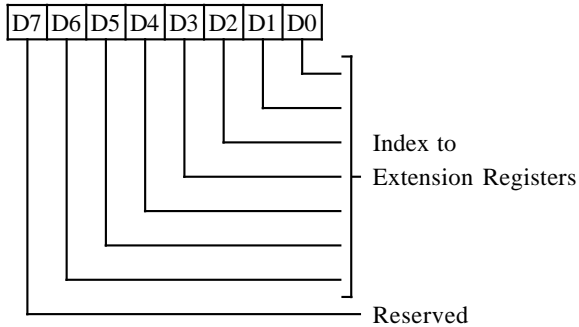
Reserved

6-0   Extensions Index

Index value used to access the extension registers

7   Reserved (0)

CHIPS VERSION REGISTER (XR00)
Read only at I/O Address 3D7h
Index 00h

D7	D6	D5	D4	D3	D2	D1	D0
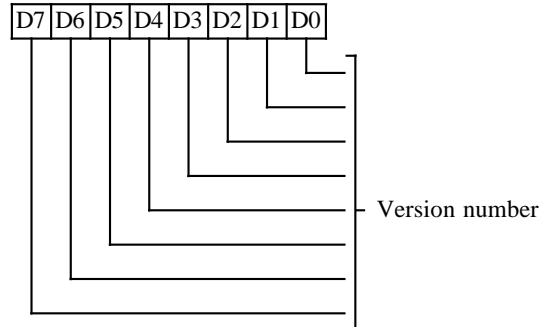
Version number

This register contains the version number for the 64200. Values start at A0h and are incremented for every silicon step.

3-0   Chip Type

These bits always read 1010b.

7-4   Chip Revision

Values in these bits start at 0000b and are incremented for every silicon step.

CONFIGURATION REGISTER (XR01)
Read only at I/O Address 3D7h Index 01h

D7	D6	D5	D4	D3	D2	D1	D0

BUS/: Bus Type
OSC/: Pixel Clock Source
MEM/: Memory Config
CFG4: Configuration Bit-4
CFG5: Configuration Bit-5
CFG6: Configuration Bit-6
CFG7: Configuration Bit-7
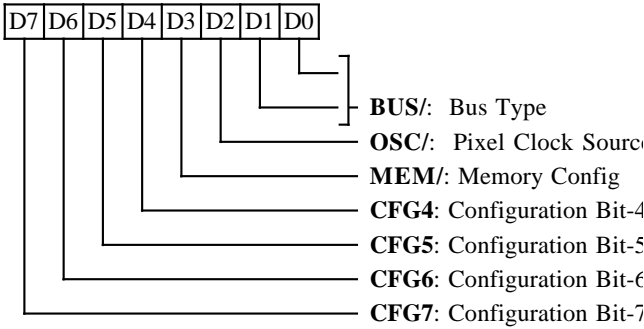
These bits latch the state of configuration bits 0-7 (selected serial data inputs: see pin description section) on the falling edge of RESET. The state of bits 0-3 after RESET effect chip internal logic as indicated below; bits 4-7 have no hardware effect on the chip. The configuration inputs have internal on-chip high-valued pullups and will float high if not driven otherwise during RESET so that the default state of all bits is 'one'.

This register is not related to the Virtual EGA Switch register (XR1F).

1-0 CPU Bus Type

00 Reserved (Future PI bus)
01 Reserved (Future MC Bus)
10 Reserved (Future Local Bus)
11 ISA bus

2 Pixel Clock Source (OSC/)

0 Oscillator Configuration

CLK0-CLK3 are pixel clock inputs (internally selected by MSR bits 2-3)

1 Clock Chip Configuration

CLK0 pin is pixel clock input
CLK1 pin is CSEL0 output
CLK2 pin is CSEL1 output
CLK3 pin is CSEL2 output

Note: Actual pixel clock frequencies generated (and how the CSEL2-0 outputs are driven) is determined as follows:

- CSEL0 is driven by MSR bit-2
- CSEL1 is driven by MSR bit-3
- CSEL2 is driven by FCR bit-0 if FCR bit-1 is 0. If FCR bit-1 is 1, CSEL2 becomes either an interlace odd/even field indicator (FLD) or PCLK÷2 (MUX) (see FCR register bits 0-1 for details).

3 Memory Configuration (MEM/)

0 The display memory interface pins are always driven, independent of the state of the MASTER register 'Wingine™' bit (XR03 bit-0). In this configuration, VGA memory is an independent bank of DRAMs separate from the Wingine™ VRAMs.

The 64200 provides VGA display memory refresh for the DRAMs at all times. The system provides refresh of the separate Wingine™ VRAMs at all times. XR03 bit-0 still controls the state of the 'VGA' pin (pin 97), but would normally be programmed to 1 (Wingine™ mode) at all times after reset.

1 The display memory interface pins are driven only when the MASTER register 'Wingine™' bit (XR03 bit-0) is 0 (VGA mode). The memory pins (RAS/, CAS/, WE/, DTOE/, DSF, AA, BA, MAD, and MBD) are tri-stated when XR03 bit-0 is set.

In this configuration, VGA memory is shared with the Wingine™ VRAMs. The 64200 provides display memory refresh in VGA mode and the system provides display memory refresh in Wingine™ mode.

7-4 Configuration bits 7-4 (CFG7-4)

Latched from CFG7-4 (Serial Data Inputs) on the falling edge of RESET and readable, but otherwise have no hardware effect.

CPU INTERFACE REGISTER (XR02)
Read/Write at I/O Address 3D7h Index 02h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

Reserved

Attribute Controller

Mapping

10-Bit I/O Address Decode

83C6-83C9 Palette Decode

Attribute FF Status (R/O)
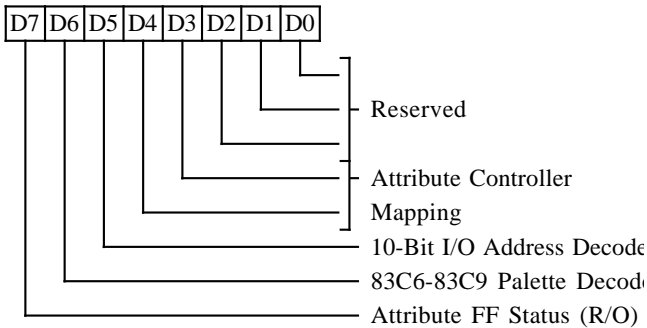
2-0   Reserved (0)

4-3   Attribute Controller Mapping

  00 Write Index and Data at 3C0h. (8-bit access only) (default - VGA mapping)
  01 Write Index at 3C0h and Data at 3C1h (8-bit or 16-bit access). Attribute flip-flop (bit-7) is always reset in this mode (16-bit mapping)
  10 Write Index at 3C0h and Data at 3C0h or 3C1h (EGA mapping, 8-bit access only)
  11 Reserved

5   I/O Address Decoding

  0 Decode all 16 bits of I/O address (default)
  1 Decode only lower 10 bits of I/O address. This affects the following addresses only: 3B4h, 3B5h, 3B8h, 3BAh, 3BFh, 3C0h, 3C1h, 3C2h, 3C4h, 3C5h, 3CEh, 3CFh, 3D4h, 3D5h, 3D8h, 3D9h, and 3DAh.

  Note: This bit does not effect the VGA color palette (X3C6-X3C9).

6   Palette Address Decoding

  0 External palette registers can be accessed only at 3C6h-3C9h (default)
  1 External palette registers can be accessed at 3C6h-3C9h and 83C6h-83C9h (for extended-function color palette chips with 8 internal registers).

  Note: For Bt484 or other RAMDACs which have 16 internal registers use XR03 bit-1 to select the 8 additional registers at 02C6-02C9h and 82C6-82C9h.

7   Attribute Flip-flop Status (read only)

  0 Index
  1 Data

MASTER CONTROL REGISTER (MASTER/XR03)
Write-Only at I/O Address 22-23h Index E0h
Read/Write at I/O Address 3D7h Index 03h

D7	D6	D5	D4	D3	D2	D1	D0

Wingine™ / VGA Select
Alt Palette Port Address
Reserved
Reserved
Alt VGA Port Address
XREQ/ Mode
XREQ/ Divide
XREQ/ Direction
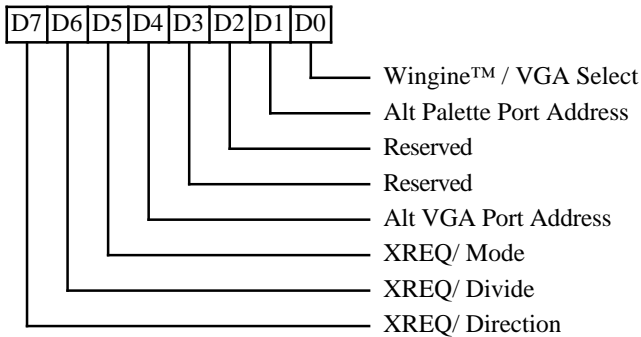
This register write-only on the graphics chip, but a read/write copy exists in systems with built-in Wingine™ support. This register is cleared by RESET.

0   Wingine™ / VGA Select

  0   VGA (Wingine™ drives the memory)
  1   Wingine™ (memory pins are 3-state)

  Note: The memory pins are 3-stated after RESET until this register is written for the first time. If CFG3 (MEM/) is 0, the memory pins are always driven independent of the state of this bit.

  This bit is output inverted on 'VGA' pin 97.

1   Alternate Palette Port Address

  0   VGA Palette is at z3C6-z3C9
  1   VGA Palette is at z2C6-z2C9

  Note: z is don't care or zero per XR02 bit-6

2   Reserved

3   Reserved

4   Alternate VGA Port Address

  0   VGA Registers are at z3[b:d]x
  1   VGA Registers are at z2[b:d]x

5   XREQ/ Mode

  0   XREQ/ is Display Enable (DE) only (interlaced if XR28 bit-5=1)
  1   XREQ/ indicates split-buffer VRAM transfer cycle timing (count is in XR3C, multiplexer mode is in XR3D)

6   XREQ/ Divide

  0   XREQ/ is DE for all lines
  1   XREQ/ is high during even-numbered display line blank times

7   XREQ/ Direction

  0   XREQ/ is an input from the system
  1   XREQ/ is an output to the system

MEMORY CONTROL REGISTER (XR04)
Read/Write at I/O Address 3D7h Index 04h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                        └── Memory Configuration
                     └───── Reserved
                  └──────── Memory Wraparound Ctrl
            └────────────── Reserved
         └───────────────── Write Buffer Enable
   └──────────────────────── Reserved
```
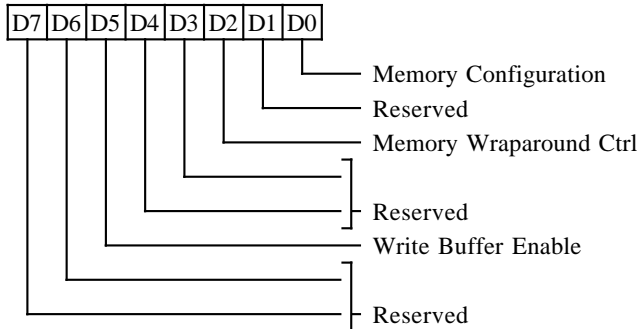
0   Memory Configuration

	Data Path	# of RAMs	Config	RAM Type	Total Memory
0	8-bit	2	256Kx4	D	256KB
1	16-bit	4	256Kx4	D	512KB

1   Reserved (0)

2   Memory Wraparound Control

This bit enables bit-17 of the CRT Controller address counter (default = 0 on reset).

   0   Disable CRTC address counter bit-17
   1   Enable CRTC address counter bit-17

4-3   Reserved (0)

5   CPU Memory Write Buffer

   0   Disable CPU memory write buffer
   1   Enable CPU memory write buffer

7-6   Reserved (0)

CPU PAGING REGISTER (XR0B)
Read/Write at I/O Address 3D7h
Index 0Bh
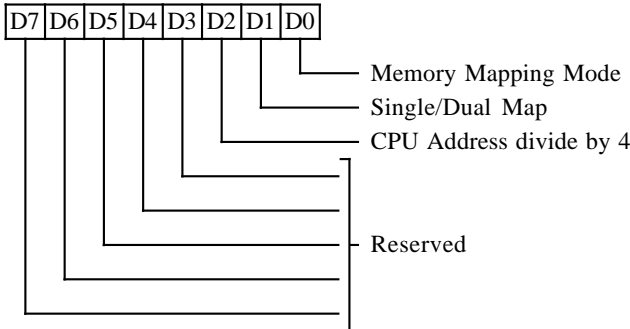
0   Memory Mapping Mode

    0   Normal Mode (VGA compatible)
    1   Extended Mode (mapping for 512 KByte VGA memory configuration

1   Single/Dual Map

    0   CPU uses only a single map to access the extended video memory space. The base address for this map is defined in the Single Map Register (XR10).
    1   CPU uses two maps to access the extended video memory space. The base addresses for the two maps are defined in the Low and High Map Registers (XR10 and XR11).

2   CPU address divide by 4

    0   Disable divide by 4 (normal mode)
    1   Enable divide by 4 for CPU addresses. This allows VGA video memory to be accessed sequentially in VGA mode 13. In addition, all VGA video memory is available in VGA mode 13 by setting this bit.

7-3   Reserved (0)

Note: Registers XR0B and XR0C control memory mapping for VGA modes only. Memory mapping in Wingine™ mode is controlled by XR3D.

START ADDRESS TOP REGISTER (XR0C)
Read/Write at I/O Address 3D7h
Index 0Ch
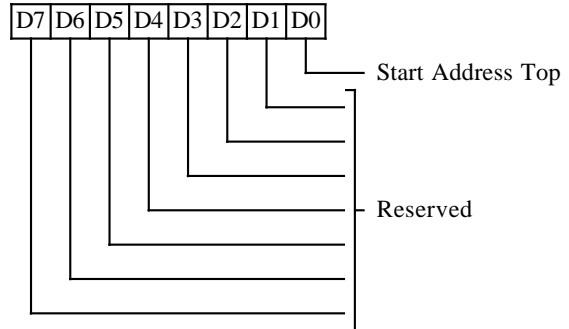
0   Start Address Top

This bit defines the high order bit for the Display Start Address when 512KB of VGA display memory is used.

7-1   Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)
Read/Write at I/O Address 3D7h
Index 0Dh

D7 D6 D5 D4 D3 D2 D1 D0

Lsb of Offset (CR13)
Lsb of Alt Offset (XR1E)

Reserved
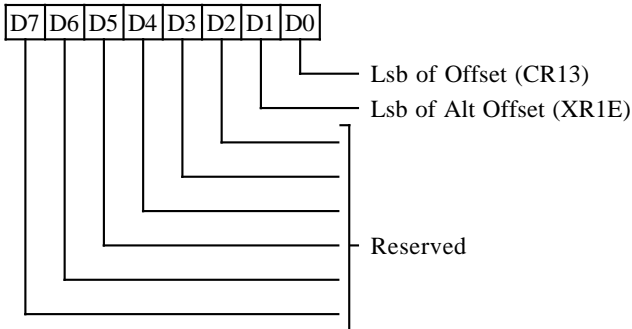
0   Offset Lsb

This bit provides finer granularity to the Offset when the Chain (Odd/Even) and Chain 4 modes are used. This bit is used with the regular Offset register (CR13).

1   Alternate Offset Lsb

This bit provides finer granularity to the Offset when the Chain (Odd/Even) and Chain 4 modes are used. This bit is used with the Alternate Offset register (XR1E).

7-2   Reserved (0)

TEXT MODE CONTROL REGISTER (XR0E)
Read/Write at I/O Address 3D7h
Index 0Ch

D7 D6 D5 D4 D3 D2 D1 D0

Reserved

Cursor Blink Disable
Cursor Style
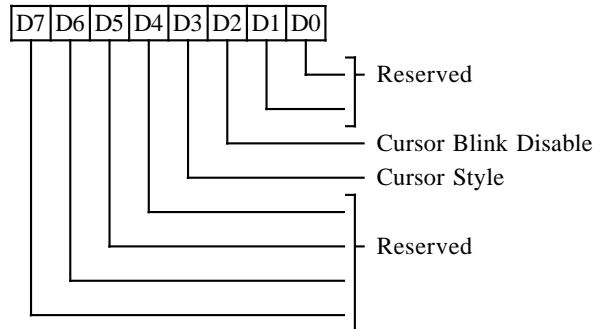
Reserved

1-0   Reserved (0)

2   Cursor Blink Disable

    0   Blinking
    1   Non-blinking

3   Cursor Style

    0   Replace
    1   Exclusive-Or

7-4   Reserved (0)

SINGLE/LOW MAP REGISTER (XR10)
Read/Write at I/O Address 3D7h
Index 10h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

┤ Single or Lower Map
  Base address bits 12-17
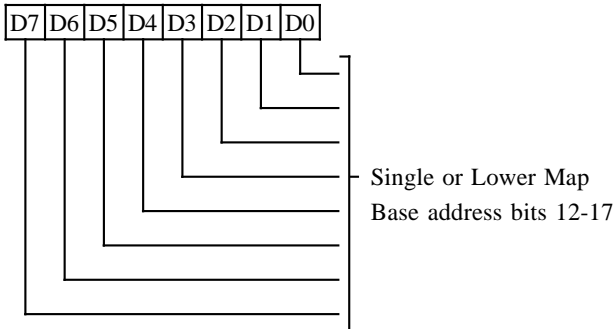
HIGH MAP REGISTER (XR11)
Read/Write at I/O Address 3D7h
Index 11h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
```

┤ Higher Map
  Base address bits 12-17
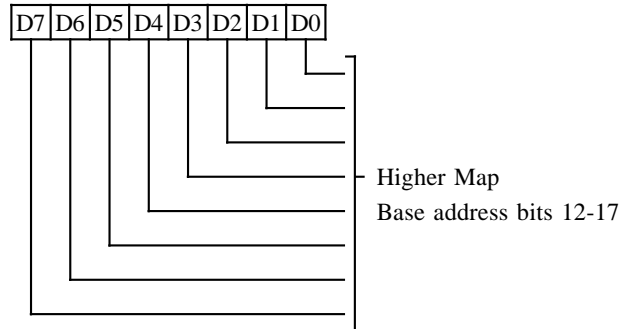
7-0   Single or Lower Map Base Address

These eight bits define the Single or Lower
Map (in Dual Map Mode) base address bits
17-12. The map starts on a 1K boundary in
planar modes and on a 4K boundary in
packed pixel modes.   In case of dual
mapping this register controls the CPU
window into the display memory based on
the contents of GR06 bits 2-3 as follows:

GR06	Low Map
0	0A0000-0AFFFFh
1	0A0000-0A7FFFh
2	0B0000-0B7FFFh
3	0B8000-0BFFFFh

Dual mapping is not allowed in the last two
cases. In the last two cases the CPU uses
single mapping.

7-0   Higher Map Base Address

These eight bits define the Higher Map (in
Dual Map Mode) base address bits 17-12.
The map starts on a 1K boundary in planar
modes and on a 4K boundary in packed
pixel modes. This register maps the CPU
window into display memory based on the
contents of GR06 bits 2-3 as follows:

GR06	Low Map
0	0B0000-0BFFFFh
1	0A8000-0AFFFFh
2	Don't care
3	Don't care

EMULATION MODE REGISTER (XR14)
Read/Write at I/O Address 3D7h
Index 14h
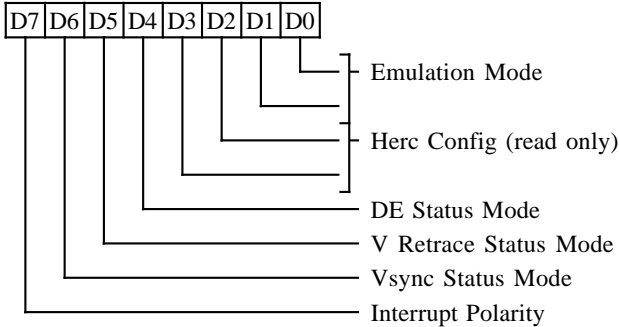
1-0   Emulation Mode

1	0	Mode
0	0	VGA
0	1	CGA
1	0	MDA / Hercules
1	1	EGA

3-2   Hercules Configuration Register (3BFh) Readback (read only)

4   Display Enable Status Mode

   0   Select <u>Display Enable</u> status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh). Normally used for CGA, EGA, and VGA modes.

   1   Select <u>Hsync</u> status to appear at bit 0 of Input Status register 1 (I/O Address 3xAh). Normally used for MDA / Hercules mode.

5   Vertical Retrace Status Mode

   0   Select <u>Vertical Retrace status</u> to appear at bit 3 of Input Status register 1 (I/O Address 3xAh). Normally used for CGA, EGA, and VGA modes.

   1   Select <u>Video</u> to appear at bit 3 of Input Status register 1 (I/O Address 3xAh). Normally used for MDA / Hercules mode.

6   Vsync Status Mode

   0   Prevent Vsync status from appearing at bit 7 of Input Status register 1 (I/O Address 3xAh). Normally used for CGA, EGA, and VGA modes.

   1   Enable Vsync status to appear at bit 7 of Input Status register 1 (I/O Address 3xAh). Normally used for MDA / Hercules mode.

7   Interrupt Output Function

This bit controls the function of the IRQ/ output.

Interrupt State	XR14[7]=0	XR14[7]=1
Disabled	3-state	3-state
Enabled, Inactive	3-state	Low
Enabled, Active	3-state	High

WRITE PROTECT REGISTER (XR15)
Read/Write at I/O Address 3B7h/3D7h Index 15h

```
┌──┬──┬──┬──┬──┬──┬──┬──┐
│D7│D6│D5│D4│D3│D2│D1│D0│
└──┴──┴──┴──┴──┴──┴──┴──┘
                      └───── Wr Protect Group 1 regs
                   └──────── Wr Protect Group 2 regs
                └─────────── Wr Protect Group 3 regs
             └────────────── Wr Protect Group 4 regs
          └───────────────── Wr Protect Group 5 regs
       └──────────────────── Wr Protect Group 6 regs
    └─────────────────────── Wr Protect Group 0 regs
 └────────────────────────── Wr Protect AR11
```
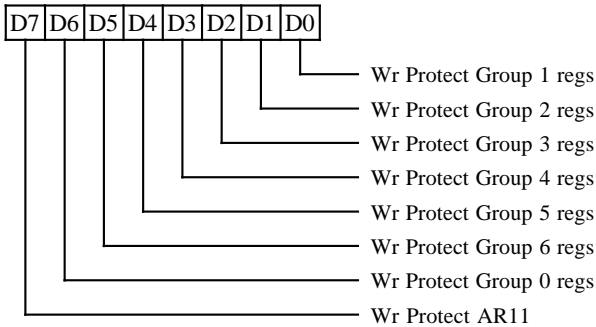
This register controls write protection for various groups of registers as shown. 0 = unprotected, 1= protected.

0   Write Protect Group 1 Registers

Sequencer (SR00-SR04)
Graphics Controller (GR00-GR08)
Attribute Controller (AR00-14)

1   Write Protect Group 2 Registers

Cursor Size register (CR09) bits 0-4
Character Height regs (CR0A, CR0B)

2   Write Protect Group 3 Registers

CRT Controller CR07 bit-4
CRT Controller CR08
CRT Controller CR11 bits 4 and 5
CRT Controller CR13 and CR14
CRT Controller CR17 bits 0, 1, & 3-7
CRT Controller CR18

(Split screen, smooth scroll, & CRTC mode control registers)

3   Write Protect Group 4 Registers

CRT Controller CR09 bits 5-7
CRT Controller CR10
CRT Controller CR11 bits 0-3 & 6
CRT Controller CR12, CR15, CR16
CRT Controller CR17 bit-2

4   Write Protect Group 5 Registers

Miscellaneous Output (3C2h)
Feature Control (3BA/3DAh)

5   Write Protect Group 6 Registers

I/O Addresses 3C6-3C9h

The PALRD/ and PALWR/ output signals are disabled and the 64200 DAC state register is write protected.

6   Write Protect Group 0

Auxiliary Write Protect for CRT Controller registers CR00-CR07 except CR07 bit-4. This bit is logically ORed with CR11 bit-7.

7   Write Protect AR11

This bit is ORed with bit-0, therefore writing to AR11 is possible only if both bit-0 and bit-7 are 0.

**ALTERNATE HORIZONTAL
DISPLAY ENABLE END (XR18)**
Read/Write at I/O Address 3D7h Index 18h
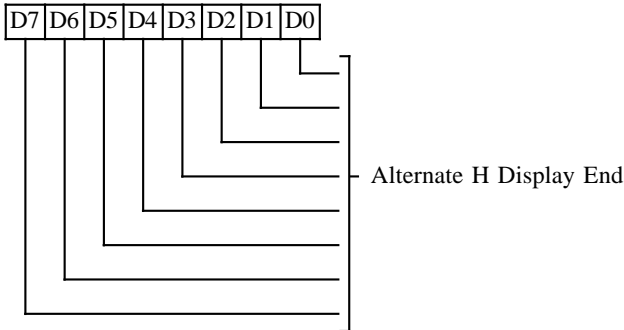
- Alternate H Display End

This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0   Alternate Horizontal Display Enable End

The value in this register defines the number of characters to be displayed per horizontal line. The programmed value is the number of characters displayed per scan line – 1.

**ALTERNATE HORIZONTAL SYNC START
/ HALF LINE COMPARE (XR19)**
Read/Write at I/O Address 3D7h Index 19h
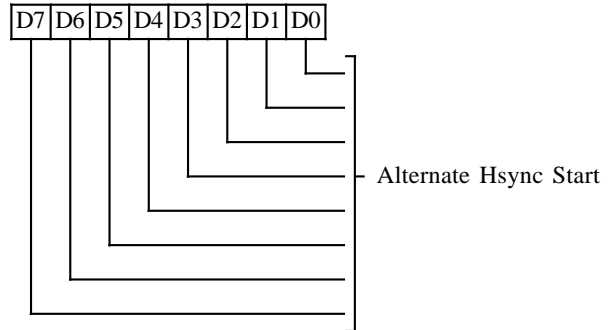
- Alternate Hsync Start

This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0   Alternate Horizontal Sync Start or Half Line Compare

XR28 bit-3 = 0 (Non-interlaced Video)
When the alternate register set is in effect, the value in this register defines the beginning of Horizontal Sync in terms of character clocks from the beginning of the display scan. This controls the centering of the display on the screen.

XR28 bit-3 = 1 (Interlaced Video)
The value in this register is used to generate the 'half-line compare' signal that controls the positioning of the Vsync for odd frames.

ALTERNATE HORIZONTAL SYNC END (XR1A)
Read/Write at I/O Address 3D7h Index 1Ah
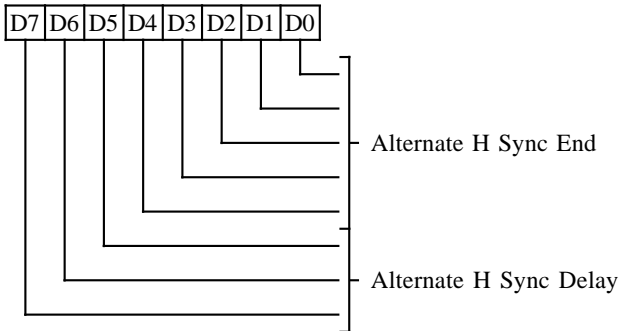
D7 D6 D5 D4 D3 D2 D1 D0

Alternate H Sync End

Alternate H Sync Delay

This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

4-0   Alternate Horizontal Sync End

Lower 5 bits of the character count that defines the end of Horizontal Sync.

The value programmed into bits 0-4 of this register is the lower 5 bits of the sum of the value in Horizontal Sync Start register plus the desired Horizontal Sync Width.

6-5   Alternate Horizontal Sync Delay

The value in these bits defines the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7   Alternate Horizontal Blank End bit-5

Sixth bit of the Horizontal Blank End register (CR03).

ALTERNATE HORIZONTAL TOTAL (XR1B)
Read/Write at I/O Address 3D7h Index 1Bh
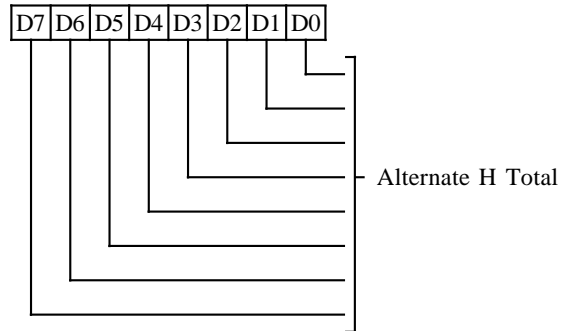
D7 D6 D5 D4 D3 D2 D1 D0

Alternate H Total

This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0   Alternate Horizontal Total

This register defines the total number of character times in a scan line including both displayed characters and retrace. The programmed value is the number of character clocks per scan line minus 5 for VGA mode and minus 2 for EGA mode.

ALTERNATE HORIZONTAL BLANK START (XR1C)
Read/Write at I/O Address 3D7h Index 1Ch
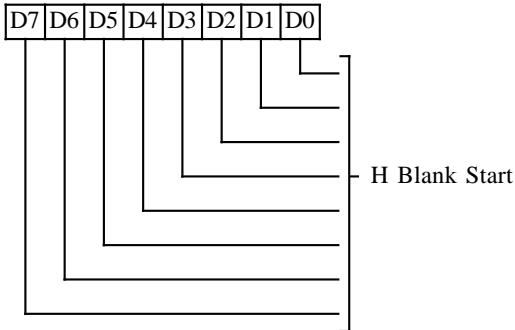
D7 D6 D5 D4 D3 D2 D1 D0

H Blank Start

This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0   Alternate Horizontal Blank Start

This register defines the beginning of Horizontal Blanking in terms of character clocks. The period between horizontal display enable end and horizontal blanking start is the right side border on the screen.

ALTERNATE HORIZONTAL BLANK END (XR1D)
Read/Write at I/O Address 3D7h Index 1Dh
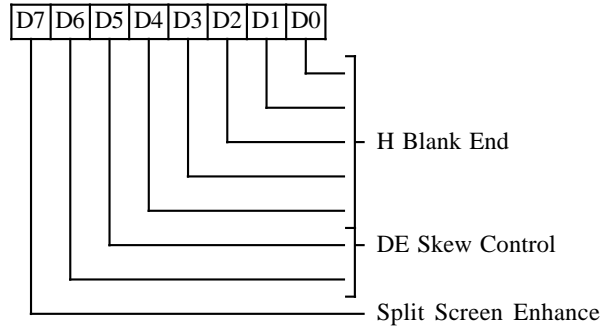
D7 D6 D5 D4 D3 D2 D1 D0

H Blank End

DE Skew Control

Split Screen Enhance

This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

4-0   Alternate Horizontal Blank End

These bits are programmed with the lower 5 bits of the character count that defines the end of horizontal blanking. The interval between the end of horizontal blanking and the beginning of the display (count 0) is the left side border on the screen. The programmed value is calculated by adding the value in the horizontal blanking start register to the desired horizontal blanking width. The lower 5 bits of the result is programmed into this register and the sixth bit is programmed into CR05.

6-5   Display Enable Skew Control

These bits define the number of character clocks (0-3) that the Display Enable signal is delayed to compensate for internal pipeline delays.

7   Split Screen Enhancement

0   IBM VGA compatible operation
1   Enhances split-screen functionality. Also, this bit should be set to '1' for Hercules graphics mode (720x348 resolution).

This bit defaults to 0.

ALTERNATE OFFSET (XR1E)
Read/Write at I/O Address 3D7h Index 1Eh
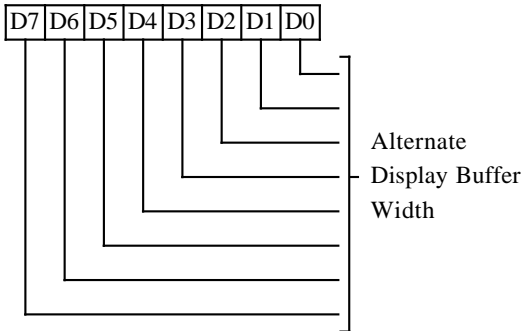
D7	D6	D5	D4	D3	D2	D1	D0

Alternate
Display Buffer
Width

This register is used in low resolution (320-pixel) CGA modes and Hercules graphics modes.

7-0   Alternate Offset

The byte starting address of the next display row is 'Byte start address of the current row plus (K times the contents of the Offset Register)' where K = 2 in byte mode and 4 in word mode.

To provide finer granularity in offset, an additional bit is defined in the Auxiliary Offset Register in the extended I/O space. This additional bit essentially adds a least significant bit to the Offset.

The byte or word mode for the memory address is selected by the CRT mode control Register bit-6. The 400-line register bit-2 allows byte/word resolution to the display buffer width.

VIRTUAL SWITCH REGISTER (XR1F)
Read/Write at I/O Address 3D7h Index 1Fh

D7	D6	D5	D4	D3	D2	D1	D0

Virtual EGA Switches

Reserved
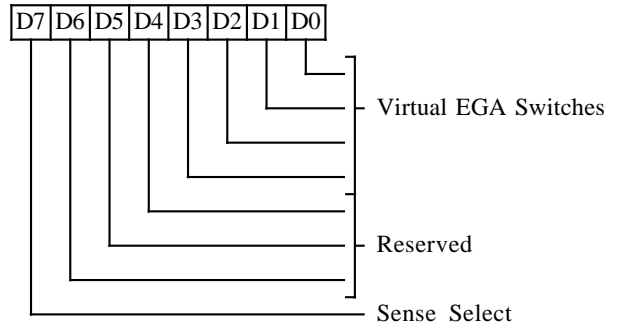
Sense Select

3-0   Virtual EGA Switches

If bit-7 of this register is '1', then one of these four bits is read back in Input Status Register 0 bit-4. The bit selected is determined by Misc Output Register (3C2h) bits 2-3.

6-4   Reserved (0)

7   Sense Select

0   Select the SENSE pin for readback in Input Status Register 0 bit-4.

1   Select one of bits 0-3 of this register for readback in Input Status Register 0 bit-4. The selected bit is read back as follows:

Misc 3-2	XR1F Bit Selected
00	bit-3
01	bit-2
10	bit-1
11	bit-0

VIDEO INTERFACE REGISTER (XR28)
Read/Write at I/O Address 3D7h Index 28h

D7	D6	D5	D4	D3	D2	D1	D0

- Blank/DE Polarity
- Blank/DE Output Select
- Shut Off Video
- Reserved (0)
- 256-Color Video Path
- Interlace Mode
- 8-Bit Video Pixel Panning
- Reserved (R/W)

0   Blank / Display Enable Polarity

   0   Negative
   1   Positive

1   Blank / Display Enable Select

   0   BLANK/ pin outputs BLANK/
   1   BLANK/ pin outputs DE

Bit-0 polarity selection is applicable to either

2   Shut off Video

   0   Video forced to border / overscan color (AR11) during blank time when screen not blanked (video is forced to 0 when screen is blanked)
   1   Video forced to default video (XR2B) when screen blanked or during blank time when screen not blanked

3   Reserved (always reads 0)

4   256-Color Video Path

   0   4-bit internal video data path (default)
   1   8-bit internal video data path; effective when AR10 bit-6=1 (256-color mode)

5   Interlace Mode

   0   Non-interlaced video
   1   Interlaced video

In interlace mode, XR19 holds the half-line compare value which controls Vsync positioning for odd frames. ***Interlace may be used in graphics modes only.***

6   8-Bit Video Pixel Panning

   0   AR13 bits 2-1 used to control panning
   1   AR13 bits 2-0 used to control panning

Effective when bit-4=1 (256-Color Video Path) and AR10 bit-6=1 (256-color mode)

7   Reserved (R/W but no internal function)

DEFAULT VIDEO REGISTER (XR2B)
Read/Write at I/O Address 3D7h Index 2Bh

D7	D6	D5	D4	D3	D2	D1	D0

- Color displayed when screen is blanked

7-0   Default Video Color

These bits specify the color to be displayed when the screen is forced to the blank state using SR1 bit-5.

SERIAL / ROW COUNT REGISTER (XR3C)
Read/Write at I/O Address 3D7h Index 3Ch

```
D7 D6 D5 D4 D3 D2 D1 D0
```

— Serial Count
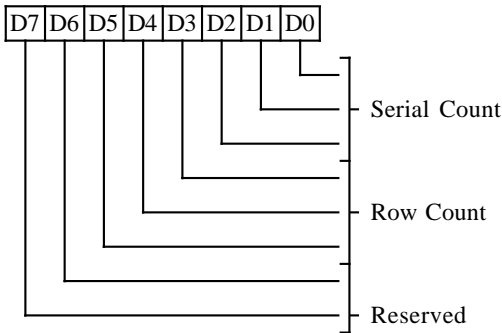
— Row Count

— Reserved

2-0   Serial Count

000	64 Serial Clocks
001	128
010	256
011	512
1x0	1024
1x1	2048

5-3   Row Count

000	64 Transfer Cycles
001	128
010	256
011	512
1x0	1024
1x1	2048

7-6   Reserved (0)

MULTIPLEXER MODE REGISTER (XR3D)
Read/Write at I/O Address 3D7h Index 3Dh

```
D7 D6 D5 D4 D3 D2 D1 D0
```

— Multiplexer Mode

— 481 Mode

— Word Swap
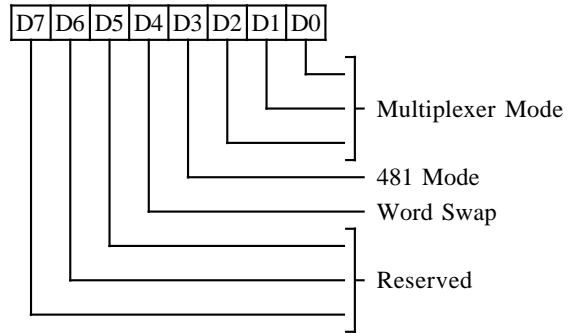
— Reserved

2-0   Multiplexer Mode   (bpp = Bits Per Pixel)

	Input	Output	NCLK
000	32 bits (A-D)	8 bpp	÷ 4
001	16 bits (AB or CD)	8 bpp	÷ 2
010	reserved	reserved	
011	reserved	reserved	
100	16 bits (AB or CD)	4 bpp	÷ 4
101	reserved	reserved	
110	32 bits (A-D)	4 bpp	÷ 8
111	reserved	reserved	

Pixel Output Order - 8 bpp Modes

| A | B | A | B | A | … |

or

| A | B | C | D | A | B | C | D | A | … |
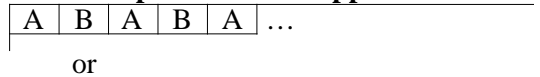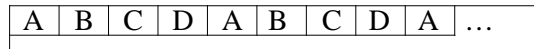
Pixel Output Order - 4 bpp Modes

| AL | AH | BL | BH | AL | … |

or

| AL | AH | BL | BH | CL | CH | DL | DH | AL | … |
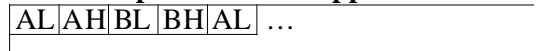
3   481 Mode

0   Blank/ is generated by the internal Wingine CRTC parameters. This mode is used for Wingine operation.

1   Blank/ is generated based on the state of the XREQ/ signal. This should be selected when an external device such as the 481 is generating data transfers and CRT timing.

4   Word Swap

0   In 16 bit mux mode, shift from AB till end of first bank then switch to CD

1   16 bit shift from CD only

7-5   Reserved (0)

SETUP / DISABLE CONTROL REGISTER (XR70)
Read/Write at I/O Address 3D7h Index 70h

D7 D6 D5 D4 D3 D2 D1 D0

Reserved (0)

3C3/46E8 Register Disable
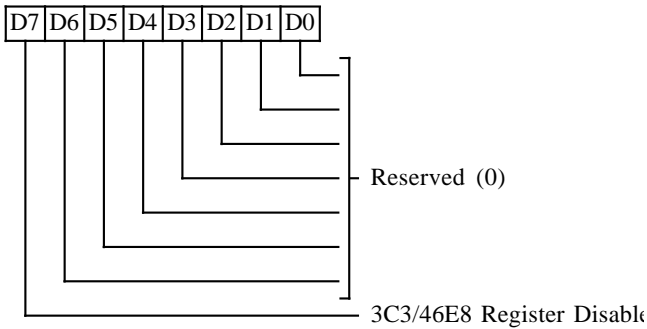
6-0   Reserved (0)

7   3C3 / 46E8 Register Disable

0   In the PI bus, port 3C3h works as defined to provide control of VGA disable. In the PC bus, port 46E8h works as defined to provide control of VGA disable and setup mode.

1   In the PI bus, writes to I/O port 3C3 have no effect. In the PC bus, writes to I/O port 46E8h have no effect (the VGA remains enabled and will not go into setup mode).

Note: Writes to register 46E8 are only effective in PC bus configurations (46E8 is ignored in PI bus configurations independent of the state of this bit). Writes to 3C3 are only effective in PI bus configurations (3C3 is ignored in PC bus configurations independent of the state of this bit).

Reads from ports 3C3 and 46E8h have no effect independent of the programming of this register (both 3C3 and 46E8h are write-only registers).

This register is cleared by RESET.

CGA COLOR SELECT (XR7E)
Read/Write at I/O Address 3B7h/3D7h Index 7Eh

D7 D6 D5 D4 D3 D2 D1 D0

Color bit-0 (Blue)
Color bit-1 (Green)
Color bit-2 (Red)
Color bit-3 (Intensity)
Intensity Enable
Color Set Select
Reserved (0)
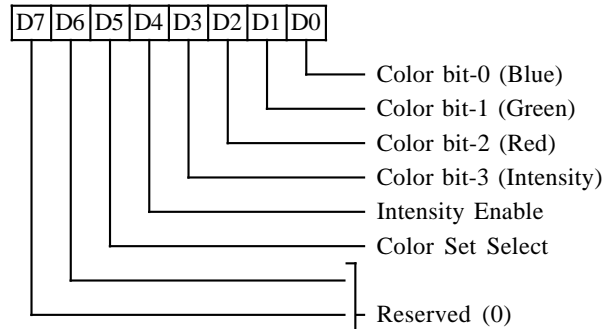
This register is a copy of the CGA color select register 3D9h. Writes to this register will change the copy at 3D9h. It is effective in CGA emulation mode. The copy at 3D9h is visible only in CGA emulation mode. The copy at XR7E is always visible.

DIAGNOSTIC REGISTER (XR7F)
Read/Write at I/O Address 3D7h Index 7Fh
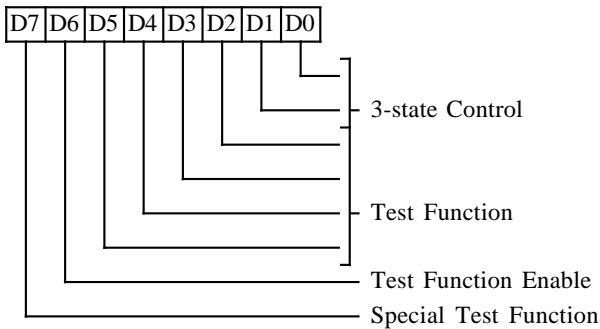
0   3-State Control Bit 0

>   0   Normal outputs (default on Reset)
>   1   3-state output pins: RDY, IOCS16/, IRQ, PALRD/, PALWR/, P7-0, PCLK, HSYNC, VSYNC, BLANK/, XREQ/, VGA, NCLK, and SCLK.

1   3-State Control Bit 1

>   0   Normal outputs (default on Reset)
>   1   3-state output pins: RASA/, RASB/, CASA/, CASB/, WE/, DTOE/, DSF, AA0-8 and BA0-8.

>   Note: Configuration bit XR01 bit-2 may be used to tri-state the clock select pins

5-2   Test Function

These bits are used for internal testing of the chip when bit-6 = 1.

6   Test Function Enable

This bit enables bits 5-2 for internal testing.

>   0   Disable test function bits (default)
>   1   Enable test function bits

7   Special Test Function

This bit is used for internal testing and should be set to 0 (default to 0 on reset) for normal operation.

Application Schematic Examples

This section includes schematic examples showing how to connect the Wingine chip. The schematics are broken down into four main groups for discussion:

1) **System Bus Interface**

   - ISA Bus

2) **Display Memory Interface**

   - DX
   - 386SX
   - 386SX minimum system (2 256Kx4 VRAMs)
   - 386SX with separate DRAMs for theVGA
   - 82C481 True-Color Graphics Accelerator
   - Peak/DM interface using the 64201

3) **Video Interface**

   - Standard VGA RAMDAC (BT475)
   - Extended VGA RAMDAC (MU9C1715)
   - Extended VGA RAMDAC (SC11482)
   - Hi-Res Support - BT484 RAMDAC

4) **Clock Interface**

   - 82C404 Clock Chip
   - Discrete Oscillators

To design a Wingine-based video subsystem, select one option from each of the above groups and combine the schematics from the following pages.

CHIPS®

Pin	Signal		Pin	
B02	RESET		72	RESET
C01	BHE/		29	BHE/
A11	AEN		28	AEN
A10	RDY		22	RDY
B28	ALE	n/c		
B13	IOWR/		24	IOWR/
B14	IORD/		23	IORD/
B08	0WS/	n/c		
B19	RFSH/		27	RFSH/
B04	IRQ9		73	IRQ
D02	IOCS16/		47	IOCS16/
B30	14.31818 MHz	To Clock Chip		
B20	BUSCLK	n/c		
A01	NMI/	n/c		

If the system provides upper address decoding (e.g., LOMEGCS/) the circuit below may be simplified

Wingine

Pin	Signal	
D01	MEMCS16/	
B11	SMEMW/	To ISA Bus
B12	SMEMR/	To ISA Bus
System	MEMW/	From System
System	MEMR/	From System
C02	LA23	
C03	LA22	
C04	LA21	
C05	LA20	
C06	LA19	
C07	LA18	
C08	LA17	

PAL 16L8

Pin	
1	I
2	I
3	I
4	I / 19 O
5	I / 18 O
6	I / 17 I/O
7	I / 16 I/O
8	I / 15 I/O
9	I / 14 I/O
11	I / 13 I/O
	12 O

| 26 | VMEMW/ |
| 25 | VMEMR/ |

Unconnected PAL pins above may be used for other system functions

Pin	Signal		Pin	
A12	A19	n/c		
A13	A18	n/c		
A14	A17	n/c		
A15	A16		46	A16
A16	A15		45	A15
A17	A14		44	A14
A18	A13		43	A13
A19	A12		42	A12
A20	A11		41	A11
A21	A10		40	A10
A22	A9		39	A9
A23	A8		38	A8
A24	A7		37	A7
A25	A6		36	A6
A26	A5		35	A5
A27	A4		34	A4
A28	A3		33	A3
A29	A2		32	A2
A30	A1		31	A1
A31	A0		30	A0

+5V = B3, B29, D16

Pin	Signal		Pin	
C18	D15		69	D15
C17	D14		67	D14
C16	D13		64	D13
C15	D12		62	D12
C14	D11		58	D11
C13	D10		56	D10
C12	D09		53	D9
C11	D08		51	D8

GND = B1, B10, B31, D18

Pin	Signal		Pin	
A02	D07		68	D7
A03	D06		66	D6
A04	D05		63	D5
A05	D04		61	D4
A06	D03		57	D3
A07	D02		55	D2
A08	D01		52	D1
A09	D00		48	D0

Wingine ISA Bus Circuit Example
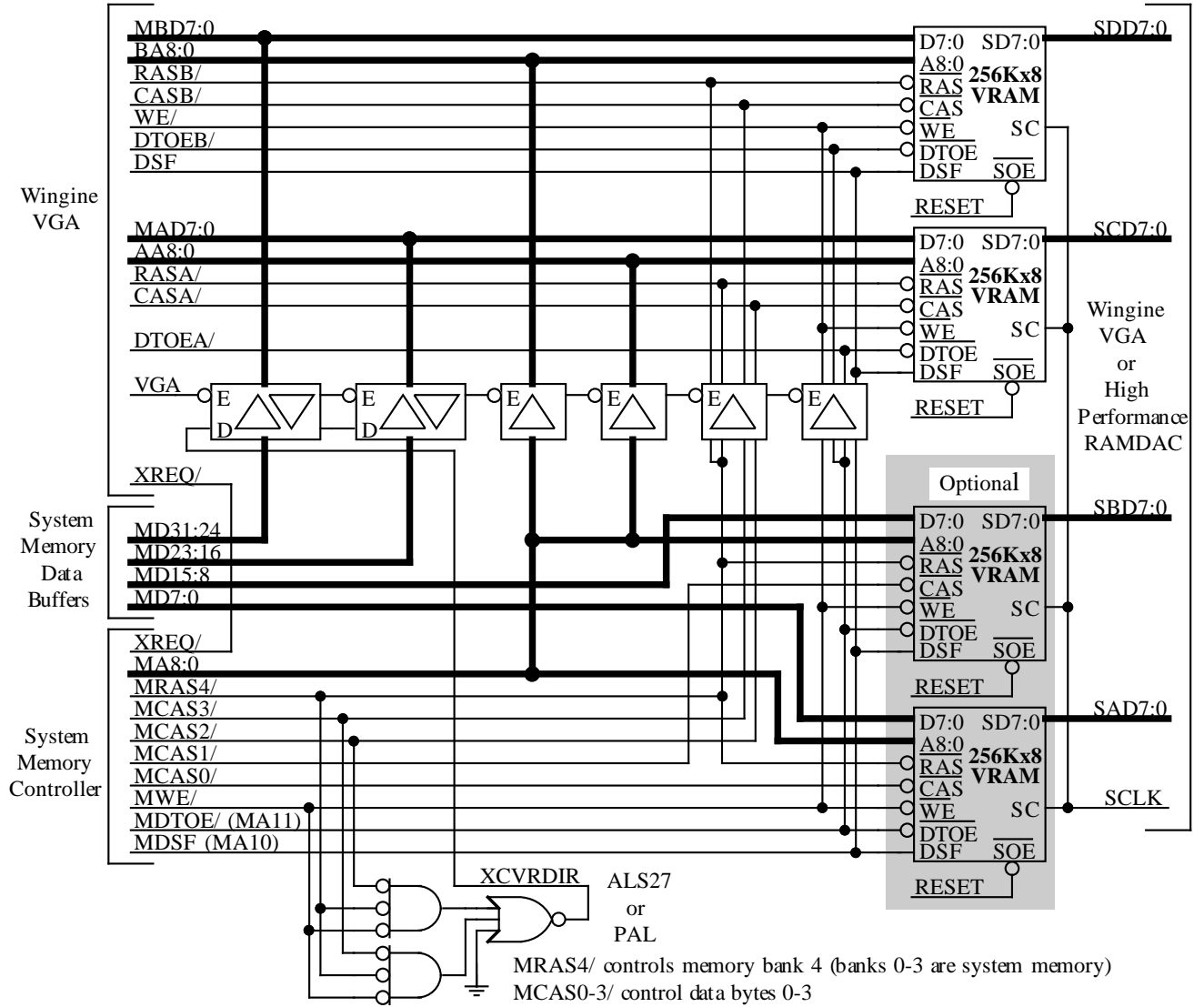
Wingine Display Memory Interface Circuit Example - DX System
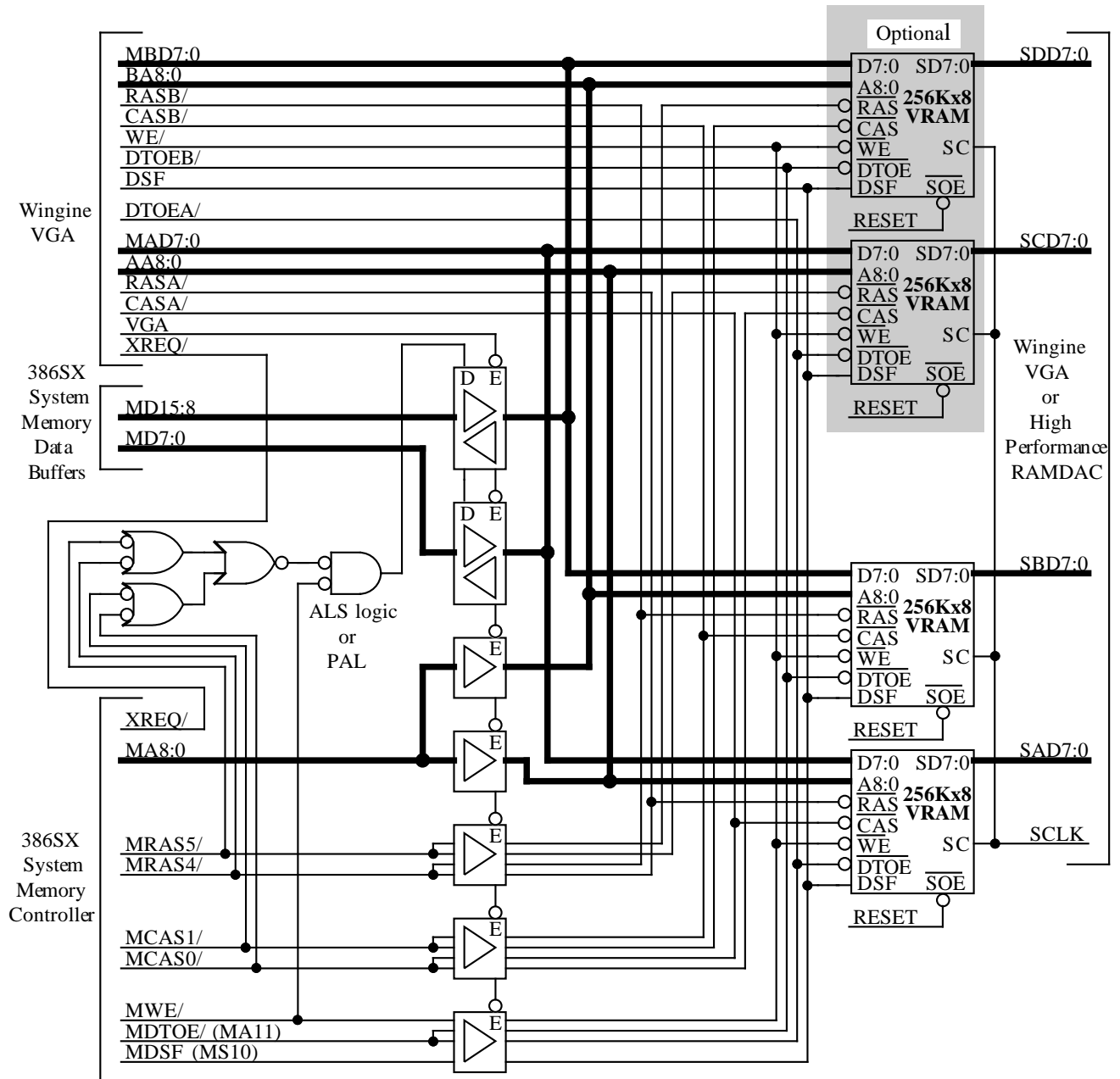
MRAS4-5/ control memory banks 4-5 (banks 0-3 are system memory)

MCAS0-1/ control data bytes 0-1

Actual tri-state buffers may not be required if the system chip memory interface pins may be tristated using 'VGA'

Wingine Display Memory Interface Circuit Example - 386SX System

MBD7:4 — n/c
MBD3:0
BA8:0
RASB/
CASB/
WE/
DTOEB/
DSF

**Wingine
VGA**

MAD7:4 — n/c
MAD3:0
AA8:0
RASA/
CASA/
DTOEA/
VGA
XREQ/

n/c — SDD7:0

n/c — SCD7:0

**Wingine
VGA**

**386SX
System
Memory
Data
Buffers**

MD15:12
MD11:8
MD7:4
MD3:0

D E

XREQ/

n/c — SBD7:4
n/c — SAD7:4

SBD3:0

D3:0 SD3:0
A8:0 **256Kx4**
RAS **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

RESET

ALS logic
or
PAL

E

**386SX
System
Memory
Controller**

MA8:0

E

SAD3:0

D3:0 SD3:0
A8:0 **256Kx4**
RAS **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

RESET

E

SCLK

MRAS5/
MRAS4/ — n/c

MCAS1/
MCAS0/

E

MWE/
MDTOE/ (MA11)
MDSF (MS10)

E
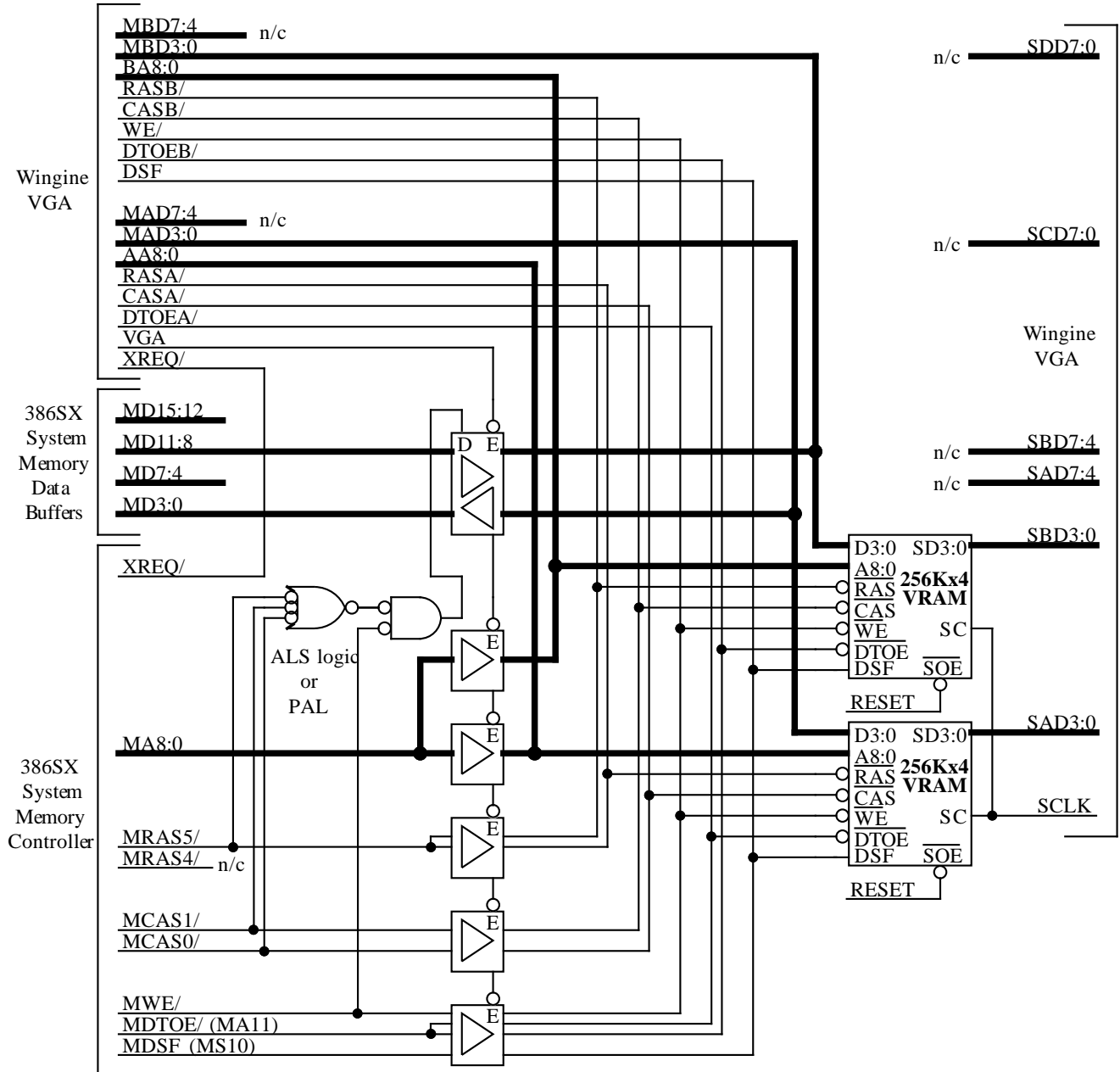
MRAS4-5/ control memory banks 4-5 (banks 0-3 are system memory)
MCAS0-1/ control data bytes 0-1

Actual tri-state buffers may not be required if the system chip memory interface pins may be tristated using
'VGA'
With this memory configuration, 8BPP (8 bit per pixel) mode is assumed but only 16 colors are available

Wingine Display Memory Interface Circuit Example - Minimum System (2 VRAMs)

CHIPS®

Wingine VGA

MBD7:4
MBD3:0
BA8:0
RASB/
CASB/
DTOEB/

D3:0
A8:0 **256Kx4**
RAS **DRAM**
CAS
WE
OE

Optional

D3:0
A8:0 **256Kx4**
RAS **DRAM**
CAS
WE
OE

MAD7:4
MAD3:0
AA8:0
RASA/
CASA/
WE/
DTOEA/
DSF

VGA

XREQ/

D3:0
A8:0 **256Kx4**
RAS **DRAM**
CAS
WE
OE

Optional

D3:0
A8:0 **256Kx4**
RAS **DRAM**
CAS
WE
OE

Optional

D7:0   SD7:0
A8:0 **256Kx8**
RAS **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

RESET

SDD7:0

D7:0   SD7:0
A8:0 **256Kx8**
RAS **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

RESET

SCD7:0

Wingine
VGA
or
High
Performance
RAMDAC

386SX
System
Memory
Data
Buffers

MD15:8
MD7:0

XREQ/
MRAS5/
MRAS4/

D7:0   SD7:0
A8:0 **256Kx8**
RAS **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

RESET

SBD7:0

386SX
System
Memory
Controller

MA8:0
MCAS1/
MCAS0/
MWE/
MDTOE/ (MA11)
MDSF (MA10)

D7:0   SD7:0
A8:0 **256Kx8**
RAS **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

RESET

SAD7:0

SCLK

MRAS4-5/ control memory banks 4-5 (banks 0-3 are system memory)
MCAS0-1/ control data bytes 0-1

Wingine Display Memory Interface Circuit Example - 386SX System with Separate VGA

Wingine VGA

82C481 Graphics Accelerator
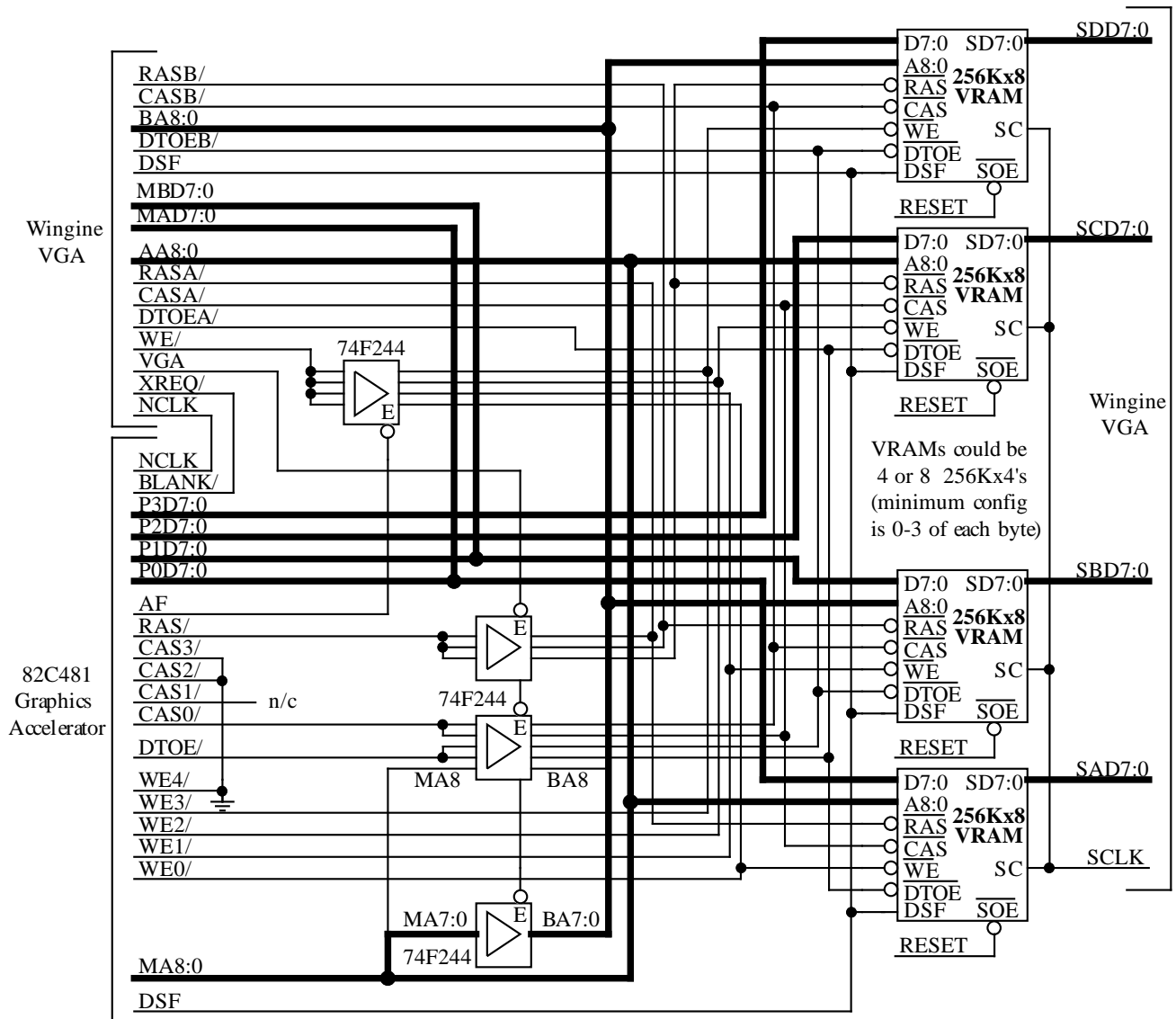
- 82C481 MCLK may be 50 MHz (100nS VRAMs)
- 82C481 NCLK is 1/4 or 1/8 of the video frequency
  (NCLK is essentially a free-running version of SCLK)
- 82C481 PALRD/ and PALWR/ are used for RAMDAC control
- SENSE should be connected to both the VGA and the 82C481
- If 256Kx4 VRAMs are used, all 8 write enables in the 82C481 could
  alternately be used to implement 4bpp modes up to 2048x1024
- To configure Wingine for 82C481 compatibility, the CFG4 pin
  (SAD7, also called '481/') must be tied low through a 4.7K resistor

The VGA H/V SYNC signals connect
to the 82C481 VHSYNC and VVSYNC
inputs and the 82C481 H/V SYNC
outputs are used to drive the monitor

The 82C404 MCLK output connects
to both Wingine and the 82C481; The
82C404 VCLK output connects to Wingine
(Wingine controls CLKSEL0 and CLKSEL1)

Wingine Display Memory Interface Circuit Example - 82C481 Graphics Accelerator
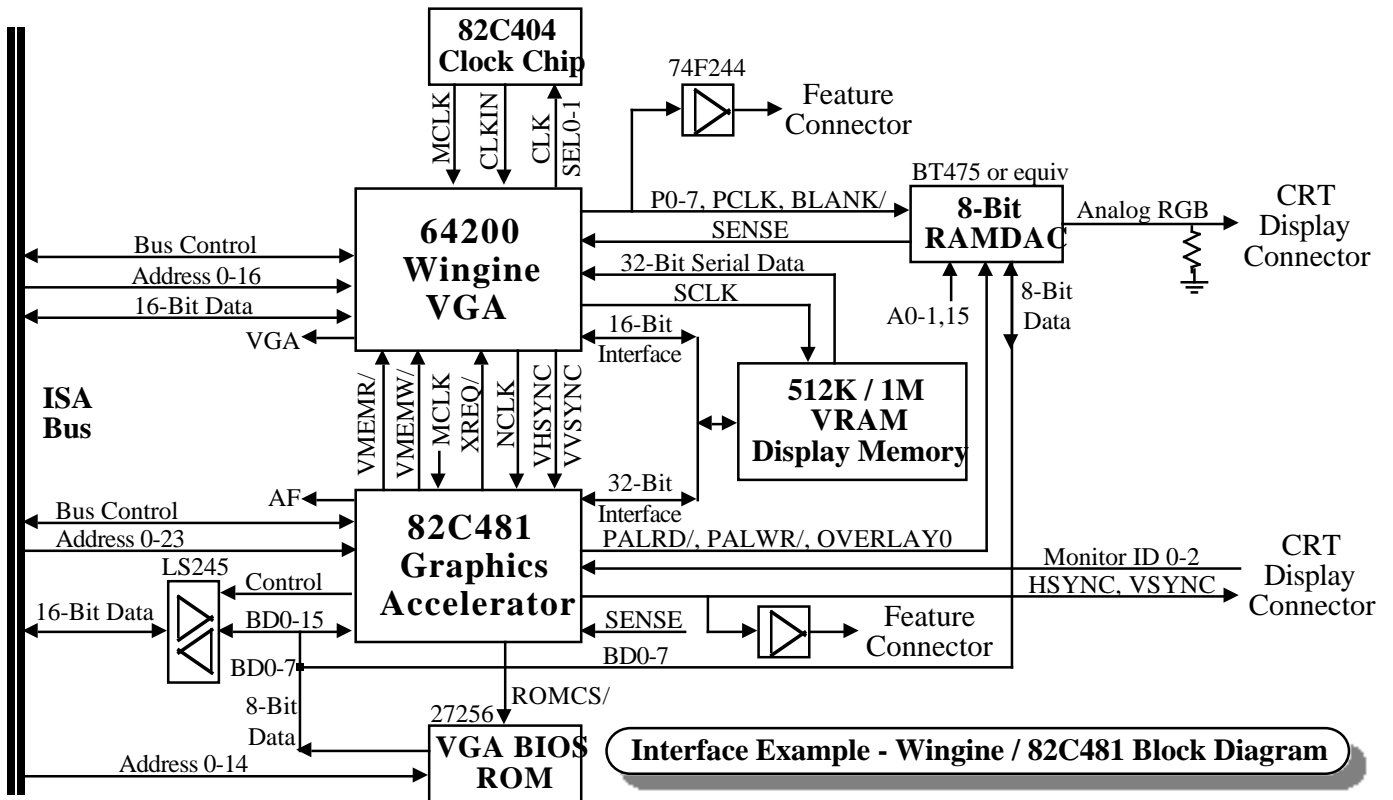
Interface Example - Wingine / 82C481 Block Diagram
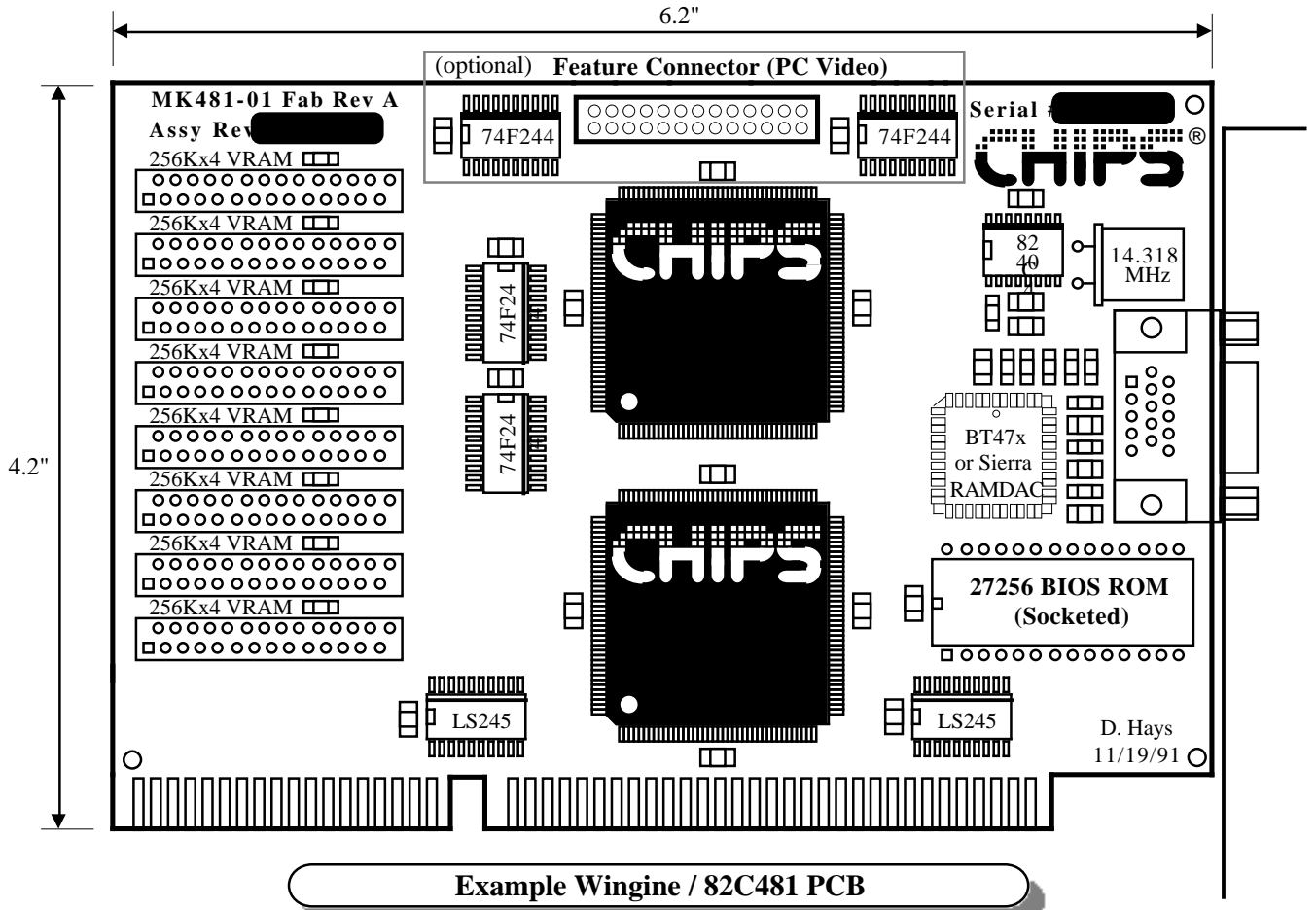
Example Wingine / 82C481 PCB

Block Diagram - Wingine Interface to Peak/DM

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Peak/DM 82C351 Memory Controller

MA10	99
MA9	98
MA8	97
MA7	96
MA6	95
MA5	93
MA4	92
MA3	91
MA2	90
MA1	88
MA0	87

74F244

MA0-10 — 33 — To A0-10 of System DRAM (Four or Eight 4MB SIMMs)

E

From Wingine & WinGlue AA0-8
From Wingine & WinGlue BA0-8

74F244

MA0-8 — 33 — To VAA0-8 (A0-8 of VRAMs A and C)
To VBA0-8 (A0-8 of VRAMs B and D)

E

VOE/

DWE/	101	DWE/
RAS7/	135	n/c
RAS6/	134	n/c	PCASE/
RAS5/	133	CASE2/
RAS4/	132	RAS2/
RAS3/	131	
RAS2/	129	RAS1/
RAS1/	128	
RAS0/	127	RAS0/
CAS3/	119	
CAS2/	118	
CAS1/	117	
CAS0/	116	

CASE1/
CASE0/

74F32

CAS3/	72	CAS03/
CAS2/	71	CAS02/
CAS1/	70	CAS01/
CAS0/	69	CAS00/

74F32

CAS13/
CAS12/
CAS11/
CAS10/

74F32

CAS23/
CAS22/
CAS21/
CAS20/

Peak/DM 82C355 Data Buffer

MD31	To SIMM byte-3 bit-7 banks 0 & 1
MD30	To SIMM byte-3 bit-6 banks 0 & 1
MD29	To SIMM byte-3 bit-5 banks 0 & 1
MD28	To SIMM byte-3 bit-4 banks 0 & 1
MD27	To SIMM byte-3 bit-3 banks 0 & 1
MD26	To SIMM byte-3 bit-2 banks 0 & 1
MD25	To SIMM byte-3 bit-1 banks 0 & 1
MD24	To SIMM byte-3 bit-0 banks 0 & 1
MD23	To SIMM byte-2 bit-7 banks 0 & 1
MD22	To SIMM byte-2 bit-6 banks 0 & 1
MD21	To SIMM byte-2 bit-5 banks 0 & 1
MD20	To SIMM byte-2 bit-4 banks 0 & 1
MD19	To SIMM byte-2 bit-3 banks 0 & 1
MD18	To SIMM byte-2 bit-2 banks 0 & 1
MD17	To SIMM byte-2 bit-1 banks 0 & 1
MD16	To SIMM byte-2 bit-0 banks 0 & 1
MD15	To SIMM byte-1 bit-7 banks 0 & 1
MD14	To SIMM byte-1 bit-6 banks 0 & 1
MD13	To SIMM byte-1 bit-5 banks 0 & 1
MD12	To SIMM byte-1 bit-4 banks 0 & 1
MD11	To SIMM byte-1 bit-3 banks 0 & 1
MD10	To SIMM byte-1 bit-2 banks 0 & 1
MD9	To SIMM byte-1 bit-1 banks 0 & 1
MD8	To SIMM byte-1 bit-0 banks 0 & 1
MD7	To SIMM byte-0 bit-7 banks 0 & 1
MD6	To SIMM byte-0 bit-6 banks 0 & 1
MD5	To SIMM byte-0 bit-5 banks 0 & 1
MD4	To SIMM byte-0 bit-4 banks 0 & 1
MD3	To SIMM byte-0 bit-3 banks 0 & 1
MD2	To SIMM byte-0 bit-2 banks 0 & 1
MD1	To SIMM byte-0 bit-1 banks 0 & 1
MD0	To SIMM byte-0 bit-0 banks 0 & 1

ENA DIR
245

19	VOE/
1	MDINP
11	MBD7
12	MBD6
13	MBD5
14	MBD4
15	MBD3
16	MBD2
17	MBD2
18	MBD0

H →
⟷
A B

| 9 | | 8 | | 7 | | 6 | | 5 | | 4 | | 3 | | 2 |

ENA DIR
245

19	
1	
11	MAD7
12	MAD6
13	MAD5
14	MAD4
15	MAD3
16	MAD2
17	MAD1
18	MAD0

H →
⟷
A B

To VRAM B Data Bits 0-7

MBDx connects to VRAM D & Wingine
MADx connects to VRAM C & Wingine

To VRAM A Data Bits 0-7

Wingine / Peak/DM Memory Interface Circuit

MBD0-7
BA0-8
RASB/
RASA/
WE/
DTOEB/
DTOEA/
DSF

Wingine
VGA

MAD0-7
AA0-8
CASB/
CASA/
VSYNC
HSYNC
VGA
XREQ/

XREQ/
VGA
HSYNC
VSYNC
DSF
VWE/
BA0-8
AA0-8
DTOEB/
DTOEA/
VCAS3/
VCAS2/
VCAS1/
VCAS0/
SOE0/

WinGlue
Support
Chip

To
CRT

D7:0   SD7:0   SDD7:0
A8:0   **256Kx8**
RAS   **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

D7:0   SD7:0   SCD7:0
A8:0   **256Kx8**
RAS   **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

D7:0   SD7:0   SBD7:0
A8:0   **256Kx8**
RAS   **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

Wingine
VGA
or High
Performance
RAMDAC

D7:0   SD7:0   SAD7:0
A8:0   **256Kx8**
RAS   **VRAM**
CAS
WE   SC
DTOE
DSF   SOE

SCLK

VOE/
MDINP
CASE2/
PCASE/

PCASE/
CASE2/
MDINP
VOE/

CAS23/
CAS22/
CAS21/
CAS20/
RAS2/
RAS1/
RAS0/
DWE/

Peak/DM
Memory
Controller
&
Data
Buffers

E

33

E

33

E

33

To All 4 Bank 1 SIMMs
To All 4 Bank 0 SIMMs
To All SIMMs Both Banks

74F244

RASA/   To 64201
RASB/   (WinGlue)

**Wingine / WinGlue /
VRAM**

CAS13/   33   To Bank 1 Byte 3 SIMM
CAS12/   To Bank 1 Byte 2 SIMM
CAS11/   To Bank 1 Byte 1 SIMM
CAS10/   To Bank 1 Byte 0 SIMM

CAS03/   To Bank 0 Byte 3 SIMM
CAS02/   To Bank 0 Byte 2 SIMM
CAS01/   To Bank 0 Byte 1 SIMM
CAS00/   To Bank 0 Byte 0 SIMM

VBA0-8

VAA0-8

MBD0-7
MAD0-7
MD8-15
MD0-7

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J3 = Feature (PC-Video Interface) Connector
(ribbon connector: numbers in parentheses
indicate component and
solder--side #'s if
card-edge connector
implemented)
(card edge pin 1 is
closest the bracket)

+5V
4.7uH

47uF   0.1   0.047

Digital Ground

Analog Ground

J3-1 (C13)
J3-26(S1)
J3-24(S2)
J3-22(S3)
J3-12(S8)
J3-10(S9)
J3-8 (S10)
J3-6 (S11)

44 OL3   AVCC 4
43 OL2   AVCC 20
42 OL1   AVCC 21
41 OL0   AVCC 22
5 SYNC   OPA 30
2 8/6   COMP 29
          VREF 31

0.1

1K

J1 = VGA Analog
Video Connector

1%
Rset   0.1

Key — J1-9

MS3 — J1-15
MS2 — J1-4
MS1 — J1-12
MS0 — J1-11

**Wingine
Video**

P7 81
P6 82
P5 83
P4 84
P3 85
P2 86
P1 87
P0 88

J3-11(C8)   39 C7
J3-13(C7)   38 C6
J3-15(C6)   37 C5
J3-17(C5)   36 C4
J3-19(C4)   35 C3
J3-21(C3)   34 C2
J3-23(C2)   33 C1
J3-25(C1)   32 C0

28 IREF
23 SETUP
3 AGND
24 AGND

R 25
G 26
B 27

J1-1
J1-2
J1-3

BLANK/ 90
PCLK 89
SENSE 79
(FLD) CLK3 96   n/c
PALWR/ 78
PALRD/ 77

J3-7(C10)   7 BLANK
J3-9(C9)   40

1 SENSE

16 WR   **BT475
RAM
DAC**

6 RD

D7 15 11   245   9 D0
D6 14 12   8 D1
D5 13 13   H   7 D2
D4 12 14   6 D3
D3 11 15   5 D4
D2 10 16   B A 4 D5
D1 9   17   3 D6
D0 8   18   E D 2 D7

150, 2%
R_L

J1-6
J1-7
J1-8

J1-10
J1-5

HSYNC 75
VSYNC 76

J3-5(C11)   19 RS2
J3-3(C12)   18 RS1
             17 RS0

19

.001

A15
A1
A0

PLCC-44

FB

HSYNC
VSYNC

J1-13
J1-14

D0-7

(**Wingine Video Interface Circuit Example - Standard VGA Color Palette**)

J3 = Feature (PC-Video Interface) Connector
(ribbon connector: numbers in parentheses
indicate component and
solder--side #'s if
card-edge connector
implemented)
(card edge pin 1 is
closest the bracket)

J3-1 (C13)
J3-26(S1)
J3-24(S2)
J3-22(S3)
J3-12(S8)
J3-10(S9)
J3-8 (S10)
J3-6 (S11)

Wingine Video

P7 81 — J3-11(C8)
P6 82 — J3-13(C7)
P5 83 — J3-15(C6)
P4 84 — J3-17(C5)
P3 85 — J3-19(C4)
P2 86 — J3-21(C3)
P1 87 — J3-23(C2)
P0 88 — J3-25(C1)

BLANK/ 90 — J3-7(C10)
PCLK 89 — J3-9(C9)
SENSE 79
(FLD) CLK3 96
PALWR/ 78
PALRD/ 77
HSYNC 75 — J3-5(C11)
VSYNC 76 — J3-3(C12)

A15
A1
A0

D0-7

+5V
4.7uH
47uF
0.1
0.047
Digital Ground
Analog Ground

44 OL3 AVCC 4
43 OL2 AVCC 21
42 OL1 AVCC 22
41 OL0
5 SYNC
2 8/6
OPA 30
COMP 29
VREF 31
0.1
1K
1% 0.1
Rset
IREF 28
SETUP 23
AGND 3
AGND 24

39 C7
38 C6
37 C5
36 C4
35 C3
34 C2
33 C1
32 C0

R 25
G 26
B 27

7 BLANK
40 1
SENSE
20 HICOLOR
16 WR
6 RD
SC11 482 RAM DAC
19 RS2
18 RS1
17 RS0
PLCC-44

D7 15 11 9 D0
D6 14 12 8 D1
D5 13 13 7 D2
D4 12 14 6 D3
D3 11 15 5 D4
D2 10 16 4 D5
D1 9 17 3 D6
D0 8 18 2 D7
245
H
B A
E D
19 1

J1 = VGA Analog Video Connector

Key — J1-9
MS3 — J1-15
MS2 — J1-4
MS1 — J1-12
MS0 — J1-11

J1-1
J1-2
J1-3
150, 2%
R_L

J1-6
J1-7
J1-8
J1-10
J1-5

HSYNC — J1-13
VSYNC — J1-14

Wingine Video Interface Circuit Example - Extended VGA Color Palette (Sierra

Note: The only difference in connection between the Sierra RAMDACs and the BT475 is pin 20 (HICOLOR/).
In addition to standard VGA color palette features, the Sierra RAMDACs (SC11482, SC11483, and
SC11484) provide 16-bit / pixel ('HiCOLOR') format (5-5-5 Targa-compatible for 32,768 colors per
pixel). HiCOLOR information may be loaded by one of two programmable methods: 1) LSB on the
PCLK rising edge followed by the MSB on the falling edge or 2) LSB on PCLK rising edge followed by
the MSB on the next rising edge (synchronized by BLANK/: the 1st byte latched after BLANK/ goes
high is the LSB).

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J3 = Feature (PC-Video Interface) Connector
(ribbon connector: numbers in parentheses
indicate component and
solder--side #'s if
card-edge connector
implemented)
(card edge pin 1 is
closest the bracket)

J3-1 (C13)
J3-26(S1)
J3-24(S2)
J3-22(S3)
J3-12(S8)
J3-10(S9)
J3-8 (S10)
J3-6 (S11)

+5V   4.7uH

47uF   0.1   0.047   Digital Ground

Analog Ground

44 PAL3   VCC 4
43 PAL2   VCC 20
42 PAL1
41 PAL0   AVCC 21
5 SYNC   AVCC 22
2
3 DGND
   DGND

NC 29
NC 30
NC 31

IREF 28

SETUP 23
AGND 24

220Ω
Rset
22.1Ω
1%

Ferrite Bead

LM334Z   1N4148

J1 = VGA
Analog Video
Connector

J1-6
J1-7
J1-8

J1-10
J1-5

Wingine Video

P7 81   J3-11(C8)   39 C7
P6 82   J3-13(C7)   38 C6
P5 83   J3-15(C6)   37 C5
P4 84   J3-17(C5)   36 C4
P3 85   J3-19(C4)   35 C3
P2 86   J3-21(C3)   34 C2
P1 87   J3-23(C2)   33 C1
P0 88   J3-25(C1)   32 C0

R 25
G 26
B 27

J1-1
J1-2
J1-3

BLANK/ 90   J3-7(C10)   7 BLANK
PCLK 89   J3-9(C9)   40
SENSE 79   1 MUX
(FLD) CLK3 96
PALWR/ 78   16 WR   **MU9C**
PALRD/ 77   6 RD   **1715**
                             RAM
HSYNC 75   J3-5(C11)   19 RS2 **DAC**
VSYNC 76   J3-3(C12)   18 RS1
                         17 RS0

D7 15 11   9 D0
D6 14 12   8 D1
D5 13 13   7 D2
D4 12 14   6 D3
D3 11 15   5 D4
D2 10 16   4 D5
D1 9   17   3 D6
D0 8   18   2 D7

245
H
B A
E D
19

150, 2%
R_L

Key   J1-9

A15
A1
A0

D0-7

PLCC-44

MS3   J1-15
MS2   J1-4
MS1   J1-12
MS0   J1-11

HSYNC   J1-13
VSYNC   J1-14

+5V   LM339   +5V
4.7K   4.7K

SENSE

340
1%
0.1

Wingine Video Interface Circuit Example - Extended VGA Color Palette

Note: The primary difference in connection between the Music Semiconductor RAMDAC and the BT475 is pin 1 (SENSE output in the BT475 and MUX input in the MU9C1715). The Music RAMDAC has no internal comparator circuit so an LM339 must be provided externally; there is also no internal voltage reference (pins 29-31 are no-connects), so an external current reference circuit must be provided. However, the MU9C1715 provides four different 16-bit / pixel mappings (including both a 5-5-5 Targa-compatible format like the Sierra SC1148x plus XGA 5-6-5 format) in addition to standard VGA color palette features. The Music RAMDAC also provides a nibble mode which allows the loading of two 4-bit pixels on every input clock with the effective pixel rate twice that frequency for high resolution display support (nibble mode requires driving the MUX pin at 1/2 the PCLK rate).

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Left side pin labels (to BT484):

Signal	Pin	BT484
SDD7	32	PD7
SDD6	31	PD6
SDD5	30	PD5
SDD4	29	PD4
SDD3	28	PD3
SDD2	27	PD2
SDD1	26	PD1
SDD0	25	PD0
SCD7	24	PC7
SCD6	23	PC6
SCD5	22	PC5
SCD4	21	PC4
SCD3	20	PC3
SCD2	19	PC2
SCD1	18	PC1
SCD0	17	PC0
SBD7	16	PB7
SBD6	15	PB6
SBD5	14	PB5
SBD4	13	PB4
SBD3	12	PB3
SBD2	11	PB2
SBD1	10	PB1
SBD0	9	PB0
SAD7	8	PA7
SAD6	7	PA6
SAD5	6	PA5
SAD4	5	PA4
SAD3	4	PA3
SAD2	3	PA2
SAD1	2	PA1
SAD0	1	PA0
SCLK	83 (n/c)	SCLK

Power/analog pins:

AVCC 79, AVCC 77, AVCC 75, AVCC 45, AVCC 42, AVCC 40
47uF 0.1 0.047 FB +5V
Digital Ground
Analog Ground
CSYNC 64
COMP 41 0.1
VREFO 44
VREFIN 43 0.1
FSADJ 33 Rset 1%
GND 84
GND 82
GND 80
GND 38
GND 36
GND 34

BT484 Pixel Output Order (BPP = Bits Per Pixel)

4BPP	8BPP	16BPP	16BPP	16BPP	24BPP
PA7:4	PA7:0	PA:B7:0	PA:B7:0	PC:D7:0	PA:C7:0
PA3:0	PB7:0	PC:D7:0	repeats	repeats	repeats
PB7:4	PC7:0	repeats			
PB3:0	PD7:0		**5-5-5**	**5-6-5**	
PC7:4	repeats		**Targa**	**XGA**	
PC3:0			**16BPP**	**16BPP**	**24BPP**
PD7:4			R=14:10	R=15:11	R=PC7:0
PD3:0			G=9:5	G=10:5	G=PB7:0
repeats			B=4:0	B=4:0	B=PA7:0

VGA Mode: program BT484 to use PCLK0 for pixel clock
Wingine Mode: program BT484 to use PCLK1 for pixel clock
Both: BT484 uses LCLK for load clock
(In Wingine mode, PCLK is '÷n' and BT484 ignores PCLK0)

PCLK0 = VGA Pixel Clock
              and Load Clock
PCLK1 = Px0-7 Pixel Clock
LCLK = Px0-7 Load Clock
SCLK = VRAM Shift Clock

Wingine Video (left block):

Signal	Pin
SCLK	99
P7	81
P6	82
P5	83
P4	84
P3	85
P2	86
P1	87
P0	88
PCLK	89
BLANK/	90
SENSE	79
(FLD) CLK3	96
PALWR/	78
PALRD/	77
HSYNC	75
VSYNC	76

BT484 RAM DAC pins:

LCLK 81
VGA7 74
VGA6 73
VGA5 72
VGA4 71
VGA3 70
VGA2 69
VGA1 68
VGA0 67
PCLK0 78
BLANK 65
CDE 63
SENSE 46
FLD 62
WR 48
RD 49
PORTSEL 66
PCLK1 76
RESET 47
RS3 53
RS2 52
RS1 51
RS0 50

PLCC-84

R 35 FB
G 37 FB
B 39 FB
150 2% 220pF
R_L

RESET — LS04
A15
A8
A1
A0
VGA — LS04
CLKIN (from 82C404)
D7:0

245 buffer:
D7 61/11 9 D0
D6 60/12 8 D1
D5 59/13 7 D2
D4 58/14 6 D3
D3 57/15 5 D4
D2 56/16 4 D5
D1 55/17 3 D6
D0 54/18 2 D7
H, B A, E D, 19, 1

J1 = VGA Analog Video Connector
J1-1
J1-2
J1-3
Key — J1-9
MS3 — J1-15
MS2 — J1-4
MS1 — J1-12
MS0 — J1-11
J1-6
J1-7
J1-8
.001
J1-10
J1-5
FB
HSYNC J1-13
VSYNC J1-14

Wingine Video Interface Circuit Example - Hi-Res VGA Color Palette

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Wingine VGA

14.318 MHz	6	XTAL IN	MCLK	8	92	MCLK
n/c	7	XTAL OUT	CLK	9	93	CLK0 (CLKIN)
See	12	MCLKSEL0	(Clk)CLKSEL0	1	94	CLK1 (CLKSEL0)
Table	14	MCLKSEL1	(Data)CLKSEL1	2	95	CLK2 (CLKSEL1)
				n/c	96	CLK3 (CLKSEL2)(FLD

82C404 Programmable Clock Chip

10	FPMODE
16	PWRDN
4	OUTDIS
15	INTCLK
11	FEATCLK
13	DVCC

AVCC 3
SO-16
DIP-16
GND 5

0.1 22-47 uF

MCLK Defaults

| 00 = 32.500 MHz |
| 01 = 40.000 MHz |
| 10 = 50.350 MHz |
| 11 = 56.644 MHz |

0.1

+5V   22 ohm

Default MCLK	Default 00	CLK Selections 01	1x
00	25.175	28.644	28.644
01	25.175	28.644	28.644
10	40.000	28.644	28.644
11	40.000	50.350	25.175

Wingine Clock Circuit Example - 82C404

82C404

+5V		
22Ω		
0.1uF		
22-47uF		

1	CSel0	Pwrdn/	16
2	CSel1	IntClk	15
3	**AVcc**	MSel1	14
4	ODis/	**DVcc**	13
5	**Gnd**	MSel0	12
6	Xin	FClk	11
7	Xout	FM/	10
8	MClk	Clk	9

0.1uF

+5V

X Indicates direct connection to power/ground distribution plane

82C404 Recommended PCB Layout

| 80nS VRAMs: | 56.644 MHz |
| 100nS VRAMs: | 50.350 MHz |

47 Ω

Wingine VGA

92	MCLK
93	CLK0 (CLKIN)
94	CLK1 (CLKSEL0)
95	CLK2 (CLKSEL1)
96	CLK3 (CLKSEL2)(FLD

| 25.175 MHz |
| 28.322 MHz |
| 44.900 MHz |
| 65.000 MHz |

Note: To use discrete oscillators selected via the Wingine internal clock multiplexer, the OSC/ pin (SCD6) must also be connected to ground through a 4.7K resistor

Wingine Clock Circuit Example - Discrete Oscillators

A0-19, Status
(RFSH/, AEN)

T_{ASC} T_{CPW} T_{NXT}

Command Strobe
(I/O: IORD/, IOWR/)
(Mem: MEMR/, MEMW/)

T_{SSC} T_{AHA} T_{SHA}

PALRD/, PALWR/ (I/O)

T_{PAL} T_{PAL}

T_{RLC}

T_{RPW} T_{CHR}

RDY (Mem)

T_{RSR} T_{RDZ}

T_{RDS} T_{RDH}

Data (Read)

T_{WDD} T_{WDH}

Data (Write)

Bus Cycle Timing

AC TIMING CHARACTERISTICS - DRAM TIMING

Symbol	Parameter	Min	Max	Units
T_{RC}	Read/Write Cycle Time	TBD	–	nS
T_{RAS}	RAS/ Pulse Width	TBD	–	nS
T_{RP}	RAS/ Precharge	4Tm	–	nS
T_{CRP}	CAS/ to RAS/ precharge	.5Tm	–	nS
T_{CSH}	CAS/ Hold from RAS/	5Tm	–	nS
T_{RCD}	RAS/ to CAS/ delay	3Tm	–	nS
T_{RSH}	RAS/ Hold from CAS/	2Tm	–	nS
T_{CP}	CAS/ Precharge	Tm	–	nS
T_{CAS}	CAS/ Pulse Width	2Tm	–	nS
T_{ASR}	Row Address Setup to RAS/	Tm	–	nS
T_{ASC}	Column Address Setup to CAS/	Tm	–	nS
T_{RAH}	Row Address Hold from RAS/	2Tm	–	nS
T_{CAH}	Column Address Hold from CAS/	Tm	–	nS
T_{CAC}	Data Access Time from CAS/	–	Tm	nS
T_{RAC}	Data Access Time from RAS/	–	4Tm	nS
T_{DS}	Write Data Setup to CAS/	Tm	–	nS
T_{DH}	Write Data Hold from CAS/	2Tm	–	nS
T_{WS}	WE/ Setup to RAS/	TBD	–	nS
T_{WP}	WE/ Hold from RAS	TBD	–	nS
T_{PC}	CAS Cycle Time	3Tm	–	nS
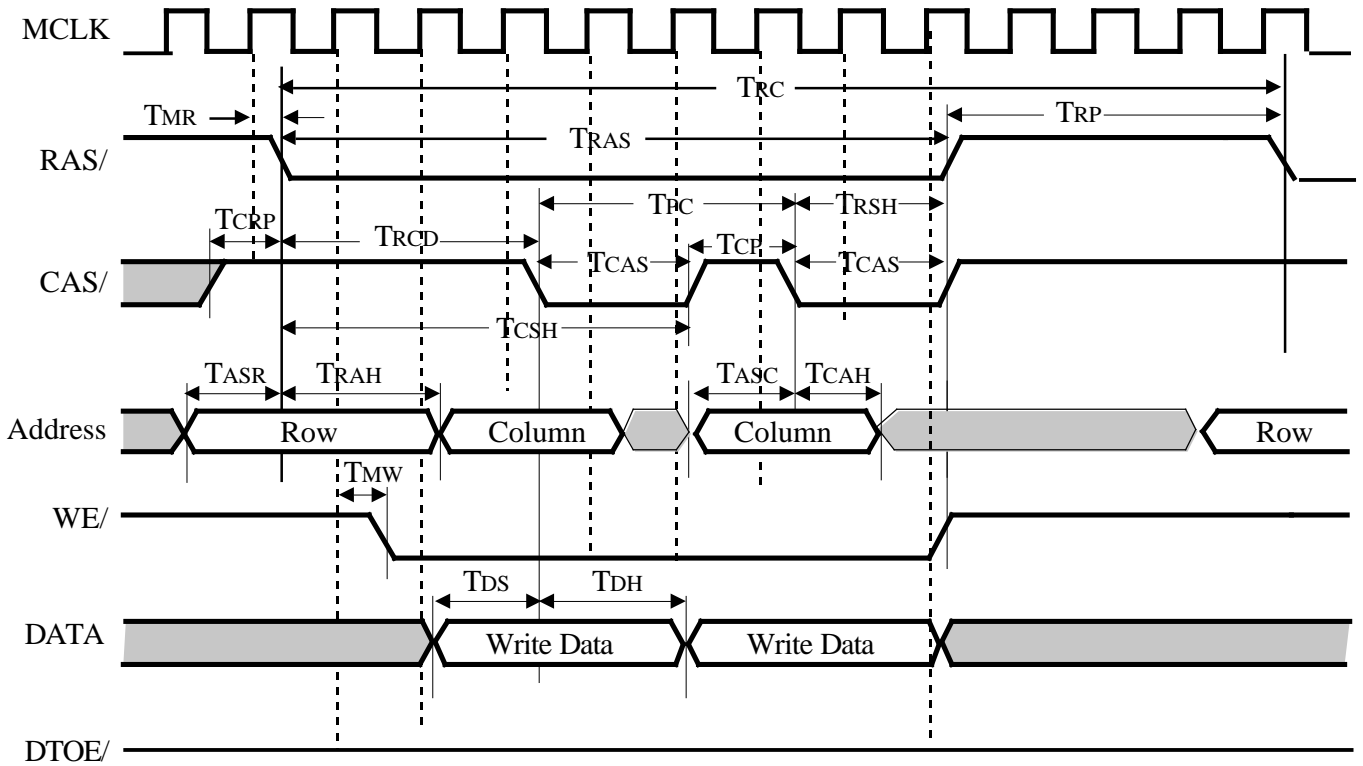
DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode write cycle.
The number of actual CAS cycles may vary between 0 and 4.
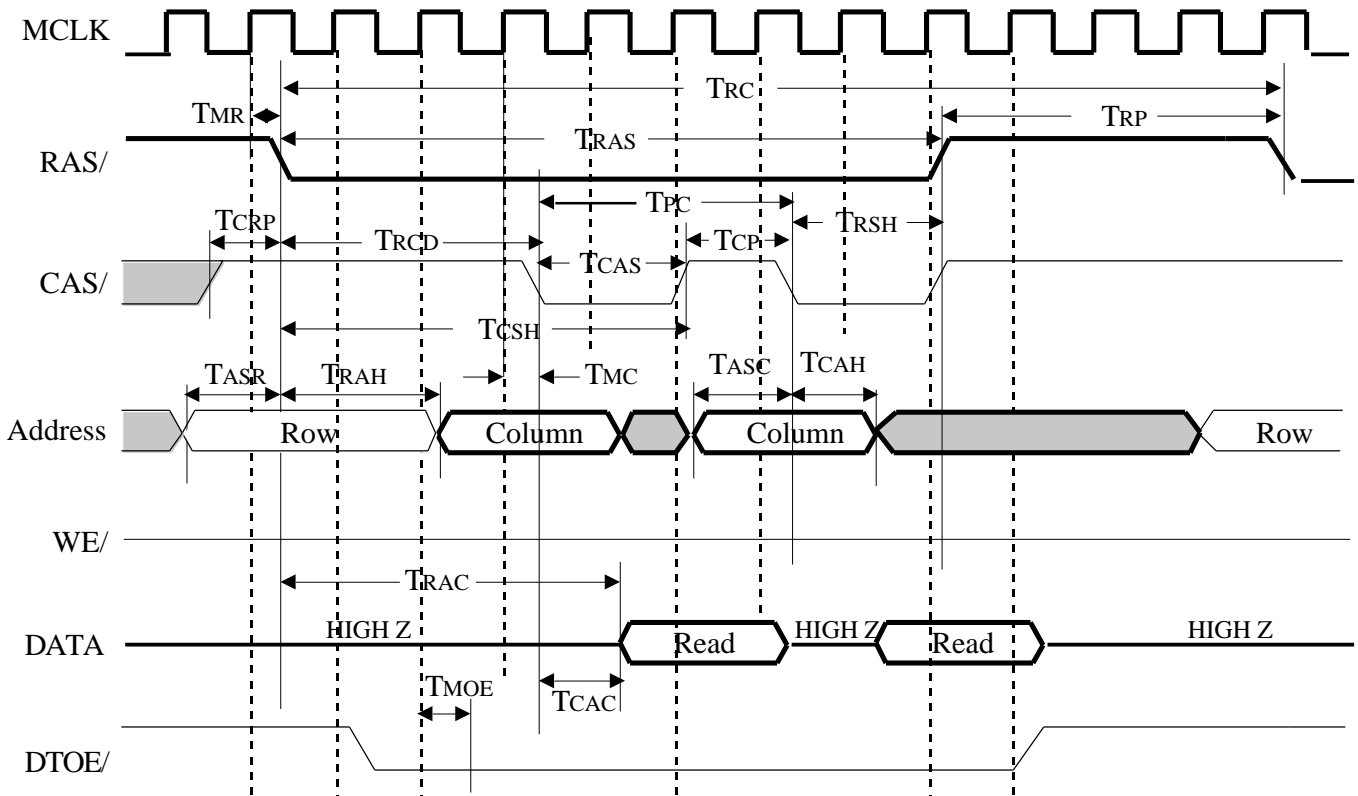
DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary. The maximum number of CAS cycles allowed is 32 (when the FIFO is being filled).