M1543C

South Bridge
Pentium/Pentium II Chip
Set with Super I/O & FIR

Version 1.00

M1543C : PCI-to-ISA Bus Bridge with Super I/O & Fast IR

Section 1 : Introduction

1.1 Features

- **Provides a highly integrated bridge (with Super I/O & Fast IR) between PCI and ISA bus for both Pentium and Pentium II systems**
- **PCI 3.3V/5V Tolerance Interface**
  - Supports PCI Master and Slave Interface
  - Supports PCI Master and Slave Initiated Termination
  - Concurrent PCI Architecture
  - PCI spec. 2.1 Compliant (Delayed Transaction & Passive Release Support)
- **Buffers Control**
  - 8-byte Bi-directional Line Buffers for DMA/ISA Memory Read/Write Cycles to PCI Bus
  - 32-bit Posted Write Buffer for PCI Memory Write and I/O Data Write (for Sound Card) to ISA Bus
- **Provides Steerable PCI Interrupts for PCI device Plug-and-Play**
  - Up to 8 PCI Interrupts Routing
  - Level to Edge Trigger Transfer
- **Enhanced DMA Controller**
  - Provides 7 Programmable Channels, 4 for 8-bit Data Size, 3 for 16-bit Data Size
  - 32-bit Addressability
  - Provides Compatible DMA Transfers
  - Provides Type F Transfers
- **Interrupt Controller**
  - Provides 14 Interrupt Channels
  - Independent Programmable Level/Edge Triggered Channels
- **Counter/Timers**
  - Provides 8254 Compatible Timers for System Timer, Refresh Request, Speaker Output Use
- **Supports Distributed DMA**
  - 7 DMA Channels can be Arbitrarily Programmed as Distributed Channels
- **Supports Serialized IRQ**
  - Quiet/Continuous Mode
  - Programmable (Default 21) IRQ/DATA Frames
  - Programmable START Frame Pulse Width
- **Supports Plug-and-Play**
  - 1 Programmable Chip Select
  - 2 Steerable Interrupt Request Lines
- **Built-in Keyboard Controller**
  - Built-in PS2/AT Keyboard and PS2 Mouse Controller
- **Supports up to 256 KB ROM Size Decoding**
- **Supports Positive/Subtractive Decode for ISA Device**
- **PMU Features**
  - Full Support for ACPI and OS Directed Power Management
  - CPU SMM Legacy Mode and SMI Feature Supported
  - Supports Programmable STPCLKJ : Throttle/CKONSTP/CKOFFSTP Control
  - Supports I/O Trap for I/O Restart Feature
  - PMU Operation States :
    -- ON
    -- Standby
    -- Sleep (Power On Suspend)
    -- Suspend (Suspend to DRAM)
    -- Suspend to HDD
    -- Soft-Off
    -- Mechanical Off
  - APM State Detection and Control Logic Supported
  - Global and Local Device Power Control Logic
  - 3 Programmable Timers : Standby/ APMA/ Global_Display
  - Provides System Activity and Display Activity Monitorings, including
    -- Video
    -- Audio
    -- Hard Disk
    -- Floppy Disk
    -- Serial Ports
    -- Parallel Port
    -- Keyboard
    -- 1 Programmable I/O Group
    -- 1 Programmable Memory Space

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- Provides Hot Plugging Events Detection
  -- Docking Insert
- Multiple External Wakeup Events of Standby Mode
  -- Power Button (Hotkey)
  -- Modem Ring
  -- RTC Alarm
  -- DRQ2
- Suspend Wakeup Detected
  -- Modem Ring
  -- RTC Alarm
  -- Docking Insert
  -- Power Button (Hotkey)
  -- USB Events
  -- IRQ
  -- ACPWR
- Thermal Alarm Supported
- Clock Generator Control Logic Supported
  -- CPUCLK Stop Control
  -- PCICLK Stop Control
- L2 Cache Power Down Control Logic Supported
- 6 General Purpose Input Signals, 10 General Purpose Output Signals
- 16 Extended General Purpose Input Signals and 16 Extended General Purpose Output Signals
- All Registers Readable/Restorable for Proper Resume from Suspend State

■ **Built-in PCI IDE Controller**

- Supports Ultra 33 DMA Mode Transfers up to Mode 2 Timing (33 Mbytes/sec)
- Supports PIO Modes up to Mode 4 Timings, and Multiword DMA Mode 0,1,2 with Independent Timing of up to 4 Drives
- Integrated 16 x 32-bit Read Ahead & Posted Write Buffers for each channel (Total : 32 DWords)
- Dedicated pins of ATA Interface for each channel
- Supports tri-state IDE signals for Swap Bay

■ **USB Interface**

- One Root Hub with three USB ports based on OpenHCI 1.0a specification
- Supports FS (12Mbits/sec) and LS (1.5Mbits/sec) Serial Transfer
- Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse

■ **Super I/O Interface**

- Supports Windows 95 Plug-and-Play
- Supports 2 Serial/ 1 Parallel/ FDC/ 1 IR Functions
- Supports 16-bit Address Decoder
- 2.88 MB (Formatted) Floppy Disk Controller
  -- Software Compatible with 82077 and Supports 16-byte Data FIFOs
  -- High Performance Internal Data Separator
  -- Supports Standard 1 Mbps/ 500 Kbps/ 300 Kbps/ 250 Kbps Data Transfer Rate
  -- Supports 3 modes of 3.5“ FDD (720K/1.2M/ 1.44MB)
  -- Swappable Drives A and B
  ~~-- Programmable 7-bit I/O Base Address~~
- Various modes of Parallel Port
  -- Supports ECP/ EPP / PS/2 / SPP and 1284 Compliance
  -- Standard Mode
  ~~-- Programmable 8-bit I/O Base Address~~
  -- Multiplexing of FDC signals through Parallel Port pins
  -- 12 IRQ Channel Options
  -- 4 8-bit DMA Channel Options
  -- IBM PC/XT, PC/AT and PS/2 Compatible Bi-directional Parallel Port
  -- Enhanced Mode
  - Enhanced Parallel Port (EPP) Compatible
  - EPP Is Compatible with EPP1.9 (IEEE 1284 Compliant), also supports EPP1.7 of Xircom specification
  -- High Speed Mode
  - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) Compatible
  - IEEE 1284 Compatible ECP
  - Includes protection circuit against damage caused when printer is powered up, or operated at higher voltages
- Serial Ports
  -- Two high performance ~~16450~~/16550 compatible UARTs with Send/Receive 16-byte FIFOs
  -- Programmable Baud Rate Generator
  -- MIDI (Musical Instrument Digital Interface) Compatible
  -- Option between ~~programmable 7-bit I/O base addresses~~, 12 IRQs, ~~and 4 DMA channels~~ for each device
- Wireless Communications
  -- Dedicated pins and COM Port for Infrared Transmission
  -- Supports IrDA 1.0 (SIR) and IrDA 1.1 (MIR and FIR)
  -- Supports Sharp-IR
  -- Option between ~~programmable 7-bit I/O base addresses~~, 12 IRQs, and 4 DMA channels for each device
- High Performance Power Management for FDC, UART And Parallel Port

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- **SMBus Interface**
  - System Management Bus Interface meets the V1.0 specification
- **Hotkey for Power on Button function through Keyboard**
- **328-pin (27mmx27mm) BGA package**

* Underlined words indicate difference with M1543

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1.2 Functions

The M1543C is a high integration bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. The M1543C has integrated the following functions :

(1) Super I/O with Fast IR : 1 Floppy Disk Controller, 1 Parallel Port, 2 Serial Ports, 1 Dedicated Pins of COM Port for Infrared Transmission to support IrDA 1.0 (SIR), IrDA 1.1 (MIR and FIR), and Sharp-IR specification.
(2) System Peripherals (ISP) (2 x 82C59, 1 x 82C54), advanced features (Type F) in the DMA controller (2 X 82C37).
(3) Serial Interrupt & Distributed DMA protocol support.
(4) 2 Steerable IRQs and 1 Programmable Chip Select for Plug-and-Play Support.
(5) 2-channel dedicated IDE Master Controller with Ultra-33 specification.
(6) The ACPI (Advanced Configuration and Power Interface) specification support.
(7) Deep flexible green function and provides the best solution for the best green system.
(8) PS2 Keyboard/Mouse controller with Hotkey support.
(9) System Management Bus (SMB).
(10) 3 OpenHCI 1.0a USB ports for best AGP system support.
(11) Dedicated and extended GPIO signals support.
(12) PCI 2.1 (Delayed Transaction & Passive Release) specification support.

M1543C can connect to the ALi Pentium North Bridge (M1521/M1531/M1541) and also the ALi Pentium II North Bridge (M1621) to provide the best system solution. The following includes more function description.

The built-in Mega I/O in M1543C is the most advanced Super I/O controller solution to basic IBM PC, XT, AT peripherals. It incorporates three full function universal asynchronous receiver/ transmitters (UARTs) (Two for COM1/COM2 and One is dedicated for IR support), a Parallel Port with various mode support, and a Floppy Disk Controller (FDC) incorporating high performance internal data separator with send/receive 16 bytes FIFOs. The serial ports support two high performance ~~16450~~/16550 compatible UARTs with send/receive 16 bytes FIFOs and a programmable baud rate generator. For the complete system architecture and specification, M1543C has the dedicated pins and COM port for the IR support, which means, the motherboard still can support two serial ports outside and have the IR support at the same time. The wireless communications supported by M1543C includes IrDA 1.0 (SIR), IrDA 1.1 (MIR and FIR), and Sharp-IR. The Parallel Port features basic functions such as standard mode, enhanced mode, and high speed mode and is compliant to SPP, PS/2, EPP, ECP, and 1284 standard. The Parallel Port also includes protection circuit against damage caused when printer is powered up, or is operated at higher voltages. The Floppy Disk Controller can support up to 1 Mbps data transfer, three-mode driver, and swappable drives A & B. Furthermore, M1543C also has high performance power management for FDC, UARTs and Parallel Port to meet green requirement.

One eight byte bi-directional line buffer is provided for ISA/DMA Master memory read/write. One 32-bit wide posted write buffer is provided for PCI memory write & I/O write (for Audio) cycles to the ISA bus. M1543C also provides a PCI to ISA IRQ routing table, and level to edge trigger transfer. Furthermore, M1543C supports Serial Interrupt and Distributes DMA for Open Architecture Specification.

The chip provides 2 extra IRQ lines and 1 programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts.

The on-chip IDE controller supports two separate IDE connectors for up to 4 IDE devices providing an interface for IDE hard disks and CD ROMs. The Ultra DMA specification (which supports the 33M bytes per second transfer rate) has been implemented in this IDE controller. The ATA bus pins & the smart deep Buffer (16 x 32-bit Read Ahead and Posted Write) are all dedicated for separate channel to improve the reliability and the performance of IDE Master. Dedicated Pins and Buffers are also the best implementation for today's concurrent OS and application to reduce overhead and achieve the best performance. The IDE controller also supports Tri-state IDE signals for Swap Bay support.

The M1543C supports Super Green for Intel and Intel compatible CPUs. It implements SMI or SCI (System Controller Interrupt) to meet the ACPI specification. It also meets the requirement for Microsoft's OnNow Design Initiative. The M1543C supports powerful power management for power saving including On, Standby, Sleeping, Suspend, Soft Off, Mechanical Off state. To control the CPU power consumption, it provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control. Also, the M1543C can support the most flexible system clock design : it can be programmed to stop the CPU Clock, and PCI Clock. The PBSRAM (Pipelined Burst SRAM) doze mode is also supported.

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The M1543C is a highly integrated chip including PS2 Keyboard/Mouse with Hotkey support, SM Bus, 3 OpenHCI 1.0a USB ports (One can be used for AGP slot, and the other two for external connections), and the dedicated and extended GPIO (General Purpose Input/Output) pins. M1543C supports the Hotkey function in the keyboard. Users can define the special function key to make the system entering or leaving different operation mode, for example, put the system into sleep or wake up the system, even force the system into Soft-Off mode. For the best AGP system implementation, M1543C has a dedicated USB port to connect to AGP slot and supports two AGP IRQ inputs to route to any available ISA interrupt pins. Also, for the more demanding GPIO pins in modern motherboard design, M1543C supports extended GPIO pins through external logic. It can extend up to 16 GPI signals and 16 GPO signals. For the best system performance, M1543C supports all the PCI 2.1 specification including Delayed Transaction & Passive Release. The system designer can use this chip to implement the best green and cost/performance system.

1.3 System Architecture & Functional Block Diagram

Figure 1.1 shows the system block diagram of Aladdin-V with M1543C. Aladdin-V is the best socket-7 chipset which can support 100MHz CPU bus and 2X AGP to achieve the best system & 3D Graphic performance. Through the high integration of M1543C, user can build a motherboard with the features of Super I/O (FDC, Parallel Port, and COM Ports), IR (SIR, MIR, FIR, and Sharp-IR), USB, Ultra-33 IDE, PS2 Keyboard/Mouse, Hotkey function, ACPI, GPIO , and deep green function with the minimized cost.

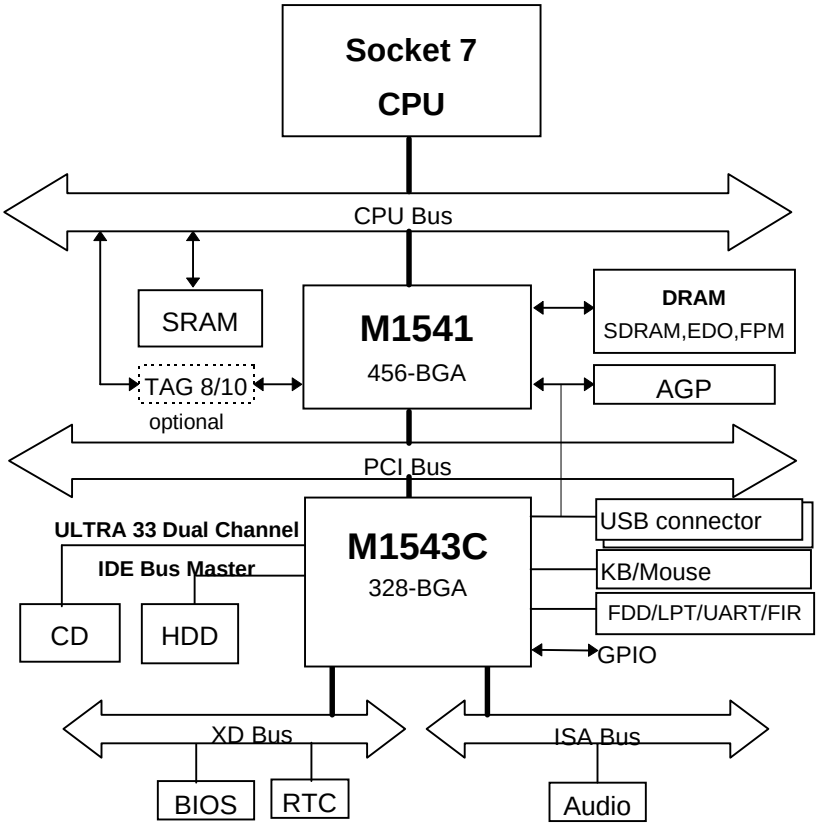

Figure 1.1 Aladdin V System Block Diagram with M1543C

Figure 1.2 shows the system block diagram of Aladdin Pro II with M1543C. Aladdin Pro II is the best Pentium II chipset which can support 100MHz CPU bus and 2X AGP to achieve the best system & 3D Graphic performance. Through the high integration of M1543C, user can build a motherboard with the features of Super I/O (FDC, Parallel Port, and COM Ports), IR (SIR, MIR, FIR, and Sharp-IR), USB, Ultra-33 IDE, PS2 Keyboard/Mouse, Hotkey function, ACPI, GPIO, and deep green function with the minimized cost.

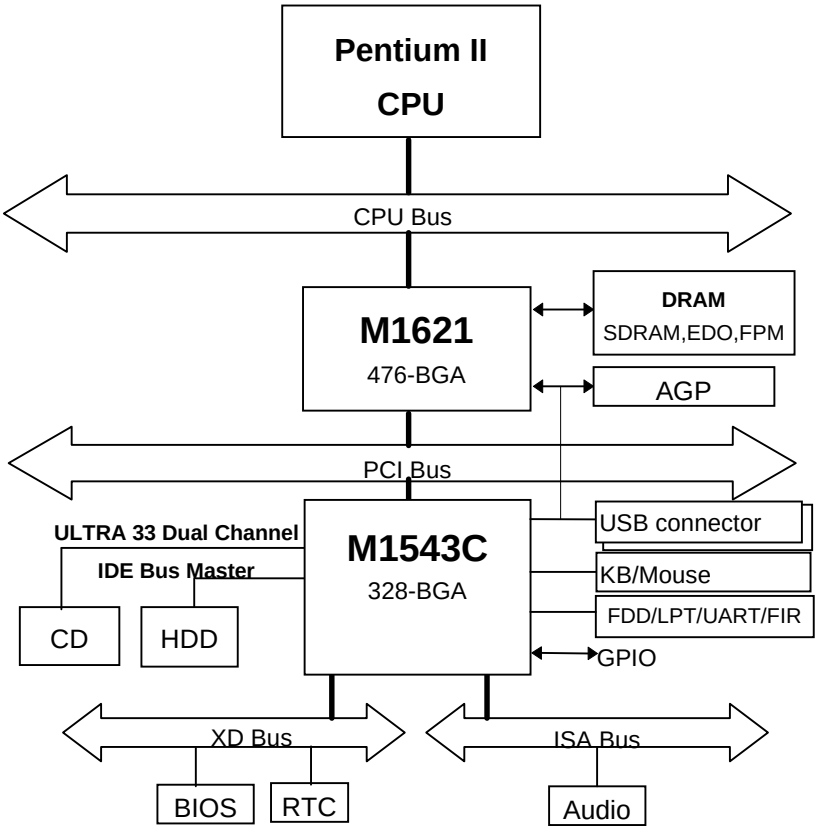

Figure 1.2 Aladdin Pro II System Block Diagram with M1543C

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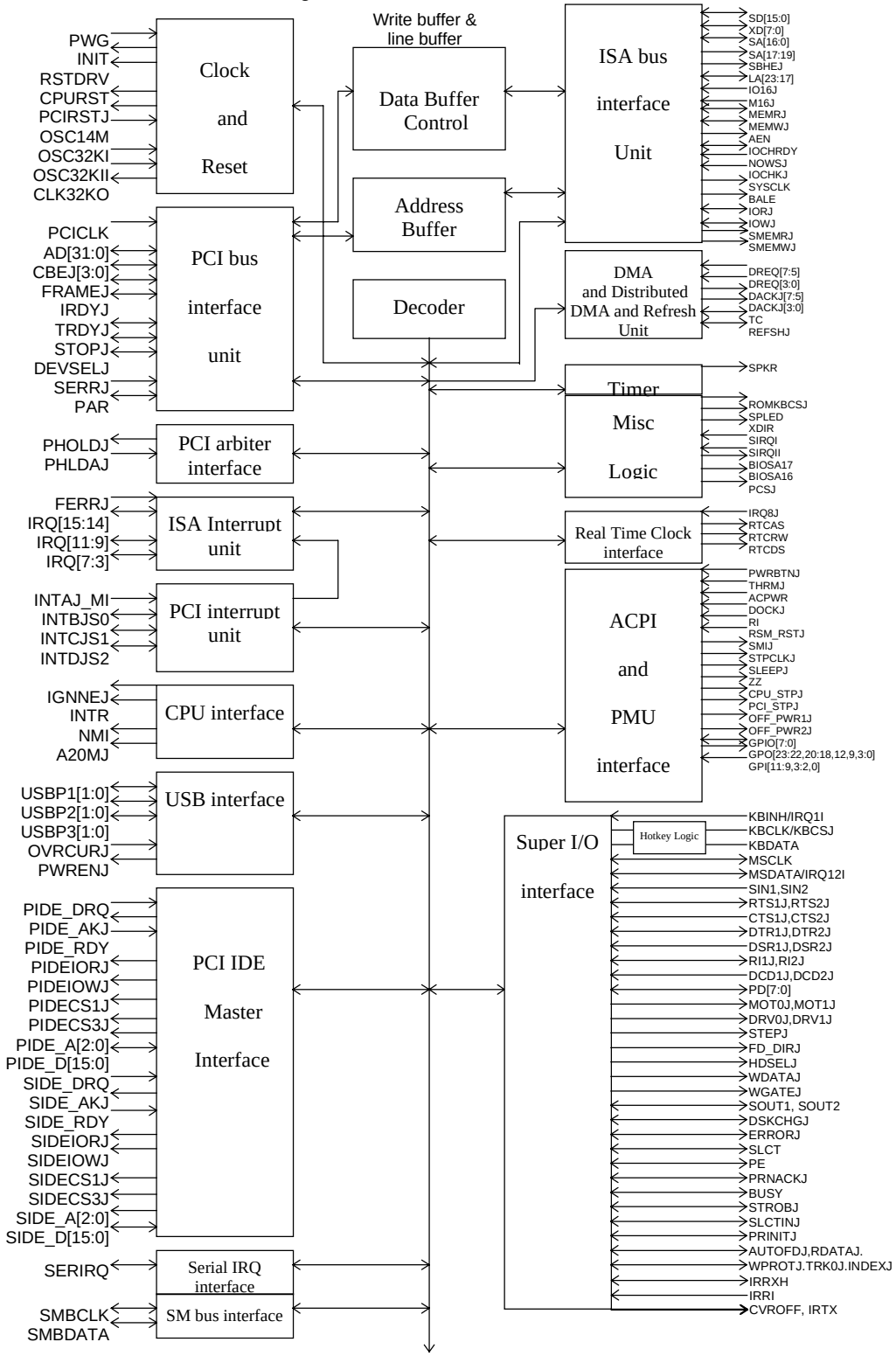
Figure 1.3 shows the internal function block diagram of M1543C.



1.4 Differences between M1543C and M1543

This section summarizes the differences between M1543C and M1543. Table below lists the major function differences :

Function	**M1543C**	**M1543**
Extended GPIO	16 GPIs & 16 GPOs	None
IDE Smart Buffer Size	32 DWords	20 DWords
USB Ports	3 Ports	2 Ports
COM Ports	3 Ports	2 Ports
IR Support	SIR, MIR, FIR, and Sharp-IR	SIR only
Keyboard Hotkey Function	Yes	No

The following show the more detailed information regarding the differences :

(1) Pin I/O Change :

Signal Name (Location)	**M1543**	**M1543C**
DSKCHGJ (T3)	I	I/O
SOUT1 (W6)	O	I/O
CLK32KO (M19)	O	I/O

(2) New Hardware Setting Pins :

Signal Name (Location)	**Pull-High**	**Pull-Low**
CLK32KO (M19)	32K test mode, this mode is only for test only.	Normal mode, this mode must be used in normal operation.
PCSJ (D15)	Normal mode	Hotkey enable, this mode is programmed as Power PC mode in M1543.

(3) SD/GPIO[7:0] Usage When TC is Pull-high :
When TC is pull-high, GPIO[7:0] are chosen. But it can be assigned as another function through register programming. Please refer to the following table :

Signal Name (Location)	**As Function**	**Register Setting**
SD/GPIO[7] (Y11)	PWR_EN (O)	M1543C Index-72h Bit6 = 1
	GPIO[7] (I/O)	M1543C Index-72h Bit6 = 0
SD/GPIO[6] (W11)	Reserved	M1543C Index-75h Bit6 = 1
	GPIO[6] (I/O)	M1543C Index-75h Bit6 = 0
SD/GPIO[5] (Y12)	USBP2- (I/O)	M5237 Index-40h Bit26 = 1
	GPIO[5] (I/O)	M5237 Index-40h Bit26 = 0
SD/GPIO[4] (W12)	USBP2+ (I/O)	M5237 Index-40h Bit26 = 1
	GPIO[4] (I/O)	M5237 Index-40h Bit26 = 0
SD/GPIO[3] (Y13)	CVROFF (O)	M1543C Index-6Dh Bit4 = 1
	GPIO[3] (I/O)	M1543C Index-6Dh Bit4 = 0
SD/GPIO[2] (W13)	IRRX (I)	M1543C Index-6Dh Bit4 = 1
	GPIO[2] (I/O)	M1543C Index-6Dh Bit4 = 0
SD/GPIO[1] (U13)	IRRXH (I/O)	M1543C Index-6Dh Bit4 = 1
	GPIO[1] (I/O)	M1543C Index-6Dh Bit4 = 0
SD/GPIO[0] (T13)	IRTX (O)	M1543C Index-6Dh Bit4 = 1
	GPIO[0] (I/O)	M1543C Index-6Dh Bit4 = 0

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(4) AGP Interrupts Inputs :
User can connect AGP two Interrupts (AGP_INTAJ and AGP_INTBJ) pins to IRQ[14]/AGP_INTAJ(G17) & IRQ[15]/AGP_INTBJ(H17) pins and use M1543C Index-4Bh Bits[7:0] to route these two interrupts to any available ISA Interrupts. The following table shows the register setting for pin function selection :

Signal Name (Location)	**M1543C Index-78h Bit0 = 0**	**M1543C Index-78h Bit0 = 1**
IRQ[14]/AGP_INTAJ (G17)	IRQ[14]	AGP_INTAJ
IRQ[15]/AGP_INTBJ (H17)	IRQ[15]	AGP_INTBJ

(5) Suspend Region:
Put two pins: IRQ[10]/KBDATA (N18), LA[21]/KBCLK (M17)into Suspend region for Hotkey support.

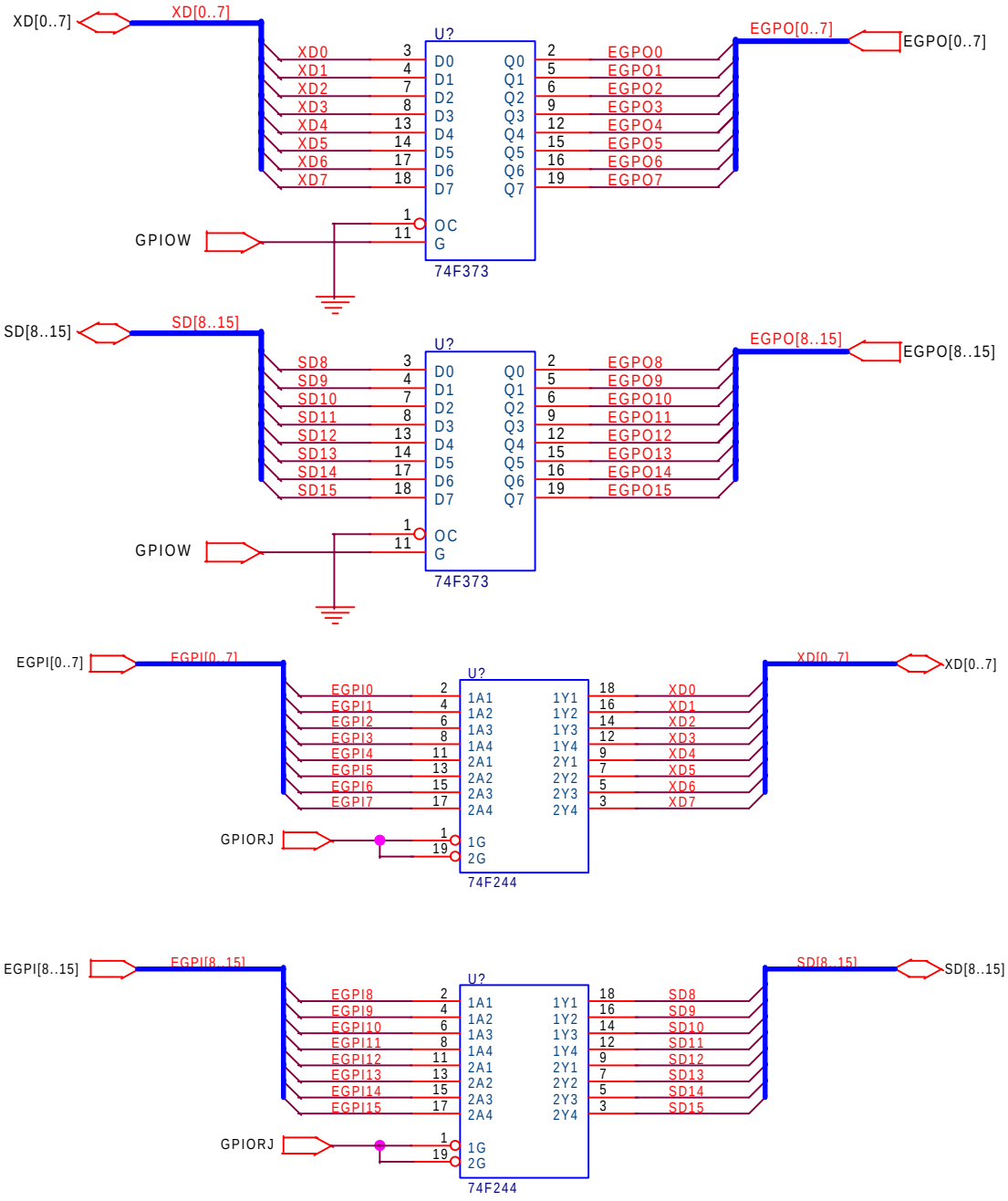
(6) Hotkey Function:
When PCSJ is pull-low, the Hotkey function is enabled. IRQ[10]/KBDATA (N18) and LA[21]/KBCLK (M17) will become KBDATA and KBCLK for the Hotkey function support. KBDATA/IRQ[10] (U12) and LA[21]/KBCLK (M17) will become IRQ[10] and LA[21] for ISA slot. That is why M1543C puts these two pins into Suspend region. The following table shows the pin function difference :

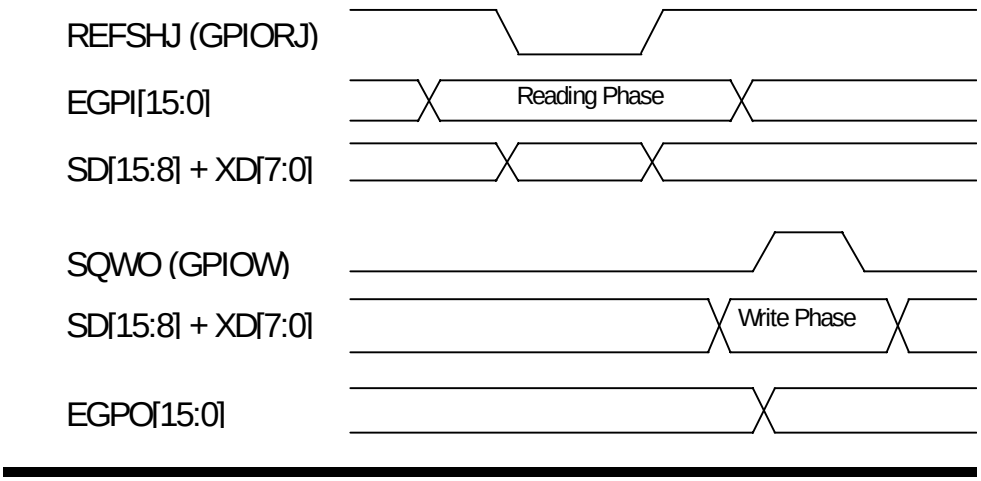
Signal Name (Location)	**PCSJ pull-high** (Hotkey function is disabled)	**PCSJ pull-low** (Hotkey function is enabled)
IRQ[10]/KBDATA (N18)	IRQ[10]	KBDATA
LA[21]/KBCLK (M17)	LA[21]	KBCLK
KBDATA/IRQ[10] (U12)	KBDATA	IRQ[10]
KBCLK/LA[21] (U11)	KBCLK	LA[21]

(7) Extended GPIO Pins (16 Bits Input and 16 Bits Output):
For this function support, external two F373s and two F244s must be used. And pin REFRSHJ is used as GPIORJ function (no register setting needed) to control F244 output enable, SQWO must be chosen as GPIOW function (through register setting) to control F373 Latch input. The following table shows the SQWO pin function selection:

M1543C register Index-5Ah Bits[9:8]	Pin SQWO/GPIOW/GPO[9] (E15) function selection
00	SQWO
01	GPIOW
10	GPO[9]
11	GPO[9]

The following figure shows the external circuit implementation and timing for extended GPIO :





(8) M1543C can release IRQ12 resource when PS2 Mouse is not enabled (Internal Keyboard is enabled as AT Keyboard only). M1543 cannot release IRQ12 at the same configuration.

Section 2 : Pin Description

2.1 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	AD 21	AD 20	AD 19	AD 16	IRDY J	SER RJ	AD 14	AD 10	AD6	AD1	PHO LDJ	PCIR EQJ	USB P1-	RTC DS	ROMK BCSJ	XD2	XD5	SD 15	SD 14	SD 13
B	CBE J3	AD 23	AD 22	AD 17	FRA MEJ	STO PJ	AD 15	AD 11	AD7	AD2	PHL DAJ	USB CLK	USB P0+	RTC RW	XD0	XD3	XD6	SD 12	DRE Q7	SD 11
C	AD 26	AD 25	AD 24	AD 18	CBE J2	DEV SELJ	CBE J1	AD 12	CBE J0	AD3	PCI_ STPJ	OVC RJ	USB P0-	RTC AS	XD1	XD4	XD7	DAC KJ7	SD 10	DRE Q6
D	AD 29	AD 28	AD 27	AD 30	AD 31	TRD YJ	PAR	AD 13	AD8	AD4	CPU_ STPJ	SIRQ I	BIOS A17	XDIR	PCS J	SER IRQ	SPK R	SD9	DAC KJ6	SD8
E	PIDE CS3J	PIDE CS1J	PIDE A2	INTA J_MI	INTB JS0	INTC JS1	PCI RSTJ	PCI CLK	AD9	AD5	AD0	USB P1+	SIRQ II	BIOS A16	SQW O	THR MJ	SPL ED	DRE Q5	MEM WJ	DAC KJ5
F	PIDE A0	PIDE A1	PIDE DAKJ	INTD JS2	PIDE RDY	VCC _B					**M1543C**			VCC _A	VCC _E	KBIN H	MEM RJ	DRE Q0	LA17	DAC KJ0
G	PIDE IORJ	PIDEI OWJ	PIDE DRQ	PIDE D15	PIDE D0	VCC _A									VCC _ 3C	LA 18	IRQ 14	INIT	A20 MJ	FER RJ
H	PIDE D14	PIDE D1	PIDE D13	PIDE D2	PIDE D12											LA 19	IRQ 15	SMIJ	NMI	INTR
J	PIDE D3	PIDE D11	PIDE D4	PIDE D10	PIDE D5				GND	GND	GND	GND				LA 20	SLE EPJ	STP CLKJ	IGN NEJ	CPU RST
K	PIDE D9	PIDE D6	PIDE D8	PIDE D7	SIDE CS3J				GND	GND	GND	GND				ZZ	OFF_ PWR 1	RSM_ RSTJ	SUST AT1J	ACP WR
L	SIDE CS1J	SIDE A2	SIDE A0	SIDE A1	SIDE DAKJ				GND	GND	GND	GND				SMB DATA	OFF_P WR2	DOC KJ	IRQ8 J	PWR BTNJ
M	SIDE RDY	SIDE IORJ	SIDE IOWJ	SIDE DRQ	SIDE D15				GND	GND	GND	GND				SMB CLK	LA21	RI	CLK3 2KO	PWG
N	SIDE D0	SIDE D14	SIDE D1	SIDE D13	SIDE D2										VDD _5S	IRQ 11	LA22	IRQ 10	OSC 32KII	OSC 32KI
P	SIDE D12	SIDE D3	SIDE D11	SIDE D4	DIRJ	VCC _A									VCC _C	LA23	IO16 J	SBH EJ	M16J	OSC 14M
R	SIDE D10	SIDE D5	SIDE D9	MOT 1J	DRV 0J	VDD _5	VCC _A							VCC _3A	VCC _A	BAL E	TC	SA0	SA1	SA2
T	SIDE D6	SIDE D8	DSK CHGJ	DRV 1J	MOT 0J	DEN SEL	DCD 1J	PD3	ACK J	RST DRV	MS CLK	MS DATA	SD0	SA19	DAC KJ3	DAC KJ2	SA6	SA3	SA4	SA5
U	SIDE D7	HD SELJ	RDA TAJ	INDE XJ	DCD 2J	DSR 1J	STR OBJ	PD4	BUS Y	ERR ORJ	KB CLK	KB DATA	SD1	SME MRJ	SA17	IRQ3	IRQ5	SA8	SA7	IRQ4
V	WPR OTJ	TRK 0J	WGA TEJ	DTR 2J	RI1J	DTR 1J	PD0	PD5	PE	INITJ	IRQ9	DRE Q2	NO WSJ	AEN	IORJ	SA15	DRE Q1	SA10	IRQ6	SA9
W	WDA TAJ	STE PJ	RTS2 J	SOU T2	CTS 1J	SOU T1	PD1	PD6	SLC T	SLC TINJ	SD6	SD4	SD2	SME MWJ	SA18	DRE Q3	SA14	SYS CLK	SA11	IRQ7
Y	RI2J	CTS 2J	DSR 2J	SIN2	RTS 1J	SIN1	PD2	PD7	AUTO FDJ	IOCH KJ	SD7	SD5	SD3	IOCH RDY	IOW J	SA16	DAC KJ1	SA13	REFR SHJ	SA12

Figure 2-1. Pinout Diagram (Top View)

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	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	SD 13	SD 14	SD 15	XD5	XD2	ROMK BCSJ	RTC DS	USB P1-	PCIR EQJ	PHO LDJ	AD1	AD6	AD 10	AD 14	SER RJ	IRD YJ	AD 16	AD 19	AD 20	AD 21
B	SD 11	DRE Q7	SD 12	XD6	XD3	XD0	RTC RW	USB P0+	USB CLK	PHL DAJ	AD2	AD7	AD 11	AD 15	STO PJ	FRA MEJ	AD 17	AD 22	AD 23	CBE J3
C	DRE Q6	SD1 0	DAC KJ7	XD7	XD4	XD1	RTC AS	USB P0-	OVC RJ	PCI_ STPJ	AD3	CBE J0	AD 12	CBE J1	DEV SELJ	CBE J2	AD 18	AD 24	AD 25	AD 26
D	SD8	DAC KJ6	SD9	SPK R	SER IRQ	PCS J	XDI R	BIOS A17	SIR QI	CPU_ STPJ	AD4	AD8	AD 13	PAR	TRD YJ	AD 31	AD 30	AD 27	AD 28	AD 29
E	DAC KJ5	MEM WJ	DRE Q5	SP LED	THR MJ	SQ WO	BIOS A16	SIR Q II	USB P1+	AD0	AD5	AD9	PCI CLK	PCI RSTJ	INTC JS1	INTB JS0	INTA J_MI	PID E A2	PIDE CS1J	PIDE CS3J
F	DAC KJ0	LA1 7	DRE Q0	ME MRJ	KBI NH	VCC _E	VCC _A			**M1543C**					VCC _B	PIDE RDY	INTD JS2	PIDE DAKJ	PID E A1	PIDE A0
G	FER RJ	A20 MJ	INIT	IRQ 14	LA1 8	VCC _ 3C									VCC _A	PID E D0	PIDE D15	PIDE DRQ	PIDE IOWJ	PIDE IORJ
H	INT R	NMI	SMIJ	IRQ 15	LA1 9											PIDE D12	PID ED2	PIDE D13	PID E D1	PIDE D14
J	CPU RST	IGN NEJ	STP CLKJ	SLE EPJ	LA2 0				GND	GND	GND	GND				PID E D5	PIDE D10	PID E D4	PIDE D11	PIDE D3
K	ACP WR	SUST AT1J	RSM_ RSTJ	OFF_P WR1	ZZ				GND	GND	GND	GND				SIDE CS3J	PID E D7	PID E D8	PID ED6	PIDE D9
L	PWR BTNJ	IRQ 8J	DOC KJ	OFF_P WR2	SMB DATA				GND	GND	GND	GND				SIDE DAKJ	SID EA1	SID E A0	SID E A2	SIDE CS1J
M	PW G	CLK3 2KO	RI	LA 21	SMB CLK				GND	GND	GND	GND				SIDE D15	SIDE DRQ	SIDE IOWJ	SIDE IORJ	SIDE RDY
N	OSC 32KI	OSC 32KII	IRQ 10	LA2 2	IRQ 11	VDD _5S										SID ED2	SIDE D13	SID E D1	SIDE D14	SIDE D0
P	OSC 14M	M16 J	SBH EJ	IO16 J	LA 23	VCC _C									VCC _A	DIRJ	SID ED4	SIDE D11	SID ED3	SIDE D12
R	SA2	SA1	SA0	TC	BAL E	VCC _A	VCC _3A							VCC _A	VDD _5	DRV 0J	MOT 1J	SID E D9	SID ED5	SIDE D10
T	SA5	SA4	SA3	SA6	DAC KJ2	DAC KJ3	SA1 9	SD0	MS DATA	MS CLK	RST DRV	ACK J	PD3	DCD 1J	DEN SEL	MOT 0J	DRV 1J	DSK CHGJ	SID E D8	SIDE D6
U	IRQ 4	SA7	SA8	IRQ 5	IRQ 3	SA 17	SME MRJ	SD1	KB DATA	KB CLK	ERR ORJ	BUS Y	PD4	STR OBJ	DSR 1J	DCD 2J	IND EXJ	RDA TAJ	HD SELJ	SIDE D7
V	SA9	IRQ 6	SA 10	DRE Q1	SA 15	IORJ	AEN	NO WSJ	DRE Q2	IRQ 9	INIT J	PE	PD5	PD0	DTR 1J	RI1J	DTR 2J	WGA TEJ	TRK 0J	WPR OTJ
W	IRQ 7	SA 11	SYS CLK	SA1 4	DRE Q3	SA1 8	SME MW J	SD2	SD4	SD6	SLC TINJ	SLC T	PD6	PD1	SOU T1	CTS 1J	SOU T2	RTS 2J	STE PJ	WDA TAJ
Y	SA 12	REFR SHJ	SA 13	DAC KJ1	SA 16	IOW J	IOCH RDY	SD3	SD5	SD7	IOC HKJ	AUT OFDJ	PD7	PD2	SIN1	RTS 1J	SIN2	DSR 2J	CTS 2J	RI2J

Figure 2-2. Bottom View

2.2 Pin Description Table :

Pin Name	Type	Description
Clock & Reset Interface :		
PWG	I Group C Schmitt	**Power-Good Input.** This signal comes from the power supply to indicate that power is available and stable. M1543C will use this signal to generate reset sequence for the system. The de-assertion of this input will enable the leakage control circuit between Soft-off (Suspend to Disk) resume circuit and no power circuit.
PCICLK	I Group B	**PCI Clock for Internal PCI Interface.** This is an input PCI clock, it should always be running at ON, STANDBY, SLEEP (Power-On Suspend) state. When CLKRUNJ is active, this clock should always be running. Internal PCI state machine and ISA state machine will use this clock.
OSC14M	I Group C	**14.318Mhz Clock Input.** This input clock will be used for Power Management timer, M8254 timer, SM Bus base frequency and ISA state machine. M1543C has moved this pin to Group C.
OSC32KI	I Group C	**32 KHz Oscillator Input 1.** This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The M1543C will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to DRAM Suspend Refresh Circuit in North Bridge. If a Crystal is not used, an external 32 Khz clock input should be connected to this pin.
OSC32KII	I Group C	**32 KHz Oscillator Input 2.** This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The M1543C will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to DRAM Suspend Refresh Circuit in North Bridge. If a Crystal is not used, this pin should be floated.
CLK32KO	I/O Group C 2.4/2.4 mA	**32 KHz Clock Output for DRAM Refresh.** At ON, STANDBY, SLEEP (Power On Suspend), SUSPEND (Suspend to DRAM) states, the output will send to Memory controller in North Bridge to support DRAM refresh clock. At Soft off and Suspend to Disk states, the output will drive low to avoid leakage current. This pin is also used as 32K test mode when pulled high. In normal operation, it must not be pulled high. This pin has a 40K internal pull-low resistor.
USBCLK	I Group B	**48 MHz USB Clock Input.** This clock will send to USB state machine to generate USB signals.
PCI Bus Interface :		
PCIRSTJ	O-Group B 12/16 mA	**PCI Bus Reset.** This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.
AD[31:0]	I/O Group B 12/16 mA	**Address and Data Multiplexed Bus.** During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBEJ[3:0]	I/O-Group B 12/16 mA	**Bus Command and Byte Enable.** During address phase, CBEJ[3:0] define the Bus Command. During the data phase, CBEJ[3:0] define the Byte Enables.
FRAMEJ	I/O -Group B 12/16 mA	**Cycle Frame.** Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.
TRDYJ	I/O -Group B 12/16 mA	**Target Ready.** Target Ready indicates the target's ability to complete the current data phase of the transaction.
IRDYJ	I/O-Group B 12/16 mA	**Initiator Ready.** Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
STOPJ	I/O-Group B 12/16 mA	**Cycle Stop Request.** Cycle Stop indicates the target is requesting the master to stop the current transaction.
DEVSELJ	I/O Group B 12/16 mA	**Device Select.** This signal indicates that the target device has decoded the address as its own cycle. This pin is an output pin when M1543C acts as a PCI slave, has decoded address as its own cycle including subtractive decoding.

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Pin Description Table (continued) :

Pin Name	Type	Description
PCI Bus Interface :		
SERRJ	I -Group B	**System Error.** This signal may be pulsed active by any agent that detects a system error condition. When SERRJ is sampling low, M1543C will assert NMI to generate non-maskable interrupt to CPU.
PAR	I/O Group B 12/16 mA	**Parity Signal.** PAR is an Even Parity and is calculated on AD[31:0] and CBEJ[3:0]. When M1543C acts as a PCI master, it drives PAR one PCI clock after address phase for read/write transaction and one PCI clock after data phase for write transaction. When the M1543C acts as a target, it drives PAR one PCI clock after data phase for PCI master read transaction.
PHLDAJ	I Group B	**PCI Bus Ownership Acknowledge.** When PCI bus arbiter asserts this pin, M1543C has owned the PCI bus.
PHOLDJ	I/O Group B 7.2/7.2 mA	**PCI Bus Ownership Request.** M1543C requests the ownership of the PCI bus from the PCI bus arbiter on the North Bridge. M1543C will assert this signal on behalf of the ISA Master, DMA Device, IDE Master, and the USB Master. This signal is also used as USB test mode when it is pulled low. In normal operation, it must be pulled high.
INTAJ_MI	I Group B	**PCI INTA.** PCI interrupt input A or PCI interrupt polling input. M1543C can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it connects to PCI INTAJ when 4 PCI Interrupts are supported, or connects to the 74F181 encoded output to support the 8 PCI Interrupts polling mode.
INTBJS0	I/O Group B Schmitt 4/4 mA	**PCI INTB.** PCI interrupt input B or polling select_0 output. M1543C can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it connects to PCI INTBJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 0 to support the 8 PCI Interrupts polling mode.
INTCJS1	I/O Group B Schmitt 4/4 mA	**PCI INTC.** PCI interrupt input C or polling select_1 output. M1543C can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it connects to PCI INTCJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 1 to support the 8 PCI Interrupts polling mode.
INTDJS2	I/O Group B Schmitt 4/4 mA	**PCI INTD.** PCI interrupt input D or polling select_2 output. M1543C can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it connects to PCI INTDJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 2 to support the 8 PCI Interrupts polling mode.
CPU interface :		
INIT	O Group E 2.4/2.4 mA	**CPU Initialize Interrupt.** CPU cold & warm reset. When CPU is Pentium II (XDIR is pulled low), this signal is low active. Otherwise (XDIR is pulled high), this signal is high active. When power on, KBC RC, port 92 RC, shutting down all will trigger INIT active.
CPURST	O-Group E 2.4/2.4 mA	**CPU Cold Reset.** When power turns on, this reset signal will be asserted, and then will become de-asserted until 4 ms after PWG becomes high.
IGNNEJ	O-Group E 2.4/2.4 mA	**Ignore Error.** This pin is used as the ignore numeric coprocessor error and connects to CPU.
INTR	O-Group E 2.4/2.4 mA	**Interrupt Request to CPU.** This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt.
NMI	O-Group E 2.4/2.4 mA	**Non-maskable Interrupt to CPU.** This is generated by the ISA Parity error (IOCHKJ assertion), PCI Parity error or DRAM Parity error (SERRJ assertion), and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt.
A20MJ	O-Group E 2.4/2.4 mA	**CPU A20 Mask.** This is the CPU Address line A20 mask signal.
FERRJ/ IRQ13	I Group E	**Floating Point Error.** FERRJ input to generate IRQ13. When coprocessor interface is disabled through configuration register Index-43h bit 6 setting, the function of this pin is IRQ13.

Pin Description Table (continued) :

Pin Name	Type	Description
ISA Bus Interface :		
IRQ[15]/ AGP_INTBJ, IRQ[14]/ AGP_INTAJ, IRQ[11], IRQ[9], IRQ[7:3]	I/O Group A Schmitt 9.6/9.6 mA	**Interrupt Request.** The Interrupt Request lines are directly from the ISA Bus, from the PCI Interrupt Routing, or from the steerable Interrupt pins. IRQ14 & IRQ15 can be connected to AGP two Interrupts AGP_INTAJ and AGP_INTBJ. Through M1543C register Index-4Bh Bits[7:0], they can also route to any available Interrupt lines.
IRQ[10]/ KBDATA	I/O Group C Schmitt 9.6/9.6 mA	**Interrupt Request Line 10 or Keyboard Data.** This pin is a multi-function pin. When pin PCSJ is pulled high which means Hotkey function is disabled, this pin is IRQ[10] as the Interrupt Request Line 10. When pin PCSJ is pulled low which means Hotkey function is enabled, this pin will become KBDATA and should connect to Keyboard. (please see 5.4.1)
RSTDRV	O-Group A 12/16mA	**ISA Bus Reset.** This output is used to reset the ISA Bus and the system device. This pin will be active if the system reset is needed.
SD[15:8]	I/O-Group A 12/12 mA	**ISA High Byte Slot Data Bus.** These pins should connect to the ISA High Byte Slot Data Bus. These pins can also be used to extend GPI. Please refer to section 1.4 for more detailed information.
XD[7:0]	I/O Group A 12/12 mA	**XD Data Bus.** When the SD[7:0] pins are defined as GPIO[7:0] pins, these pins can be used to drive SD[7:0] if TTL LS245 is used as a buffer. The M1543C signal XDIR will control this buffer. Also these pins can also be used to extend GPIO signals. Please refer to section 1.4 for more detailed implementation.
SD[7]/ GPIO[7]/ PWR_EN	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 7 or General Purpose I/O or USB Power Enable.** This pin is a multi-function pin selected by hardware and software setting. When pin TC is pulled low, SD[7] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[7]/PWR_EN functions are selected. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL. GPIO[7] or PWR_EN are chosen through M1543C register Index-72h bit6 setting. When this bit is reset as 0, GPIO[7] is chosen for green or system event control. When this bit is set as 1, PWR_EN is chosen to control the USB Power enable.
SD[6]/ GPIO[6]	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 6 or General Purpose I/O.** This pin is a multi-function pin selected by hardware setting. When pin TC is pulled low, SD[6] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[6] is selected for green or system event control. M1543C register Index-75h bit6 must be reset as 0 for GPIO[6] support. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL.
SD[5]/ GPIO[5]/ USBP2-	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 5 or General Purpose I/O or USB Port2 Data Signal.** This pin is a multi-function pin selected by hardware and software setting. When pin TC is pulled low, SD[5] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[5]/USBP2- functions are selected. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL. GPIO[5] or USBP2- are chosen through M5237 register Index-40h bit26 setting. When this bit is reset as 0, GPIO[5] is chosen for green or system event control. When this bit is set as 1, USBP2- is chosen to support USB Port2 data signal.
SD[4]/ GPIO[4]/ USBP2+	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 4 or General Purpose I/O or USB Port2 Data Signal.** This pin is a multi-function pin selected by hardware and software setting. When pin TC is pulled low, SD[4] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[4]/USBP2+ functions are selected. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL. GPIO[4] or USBP2+ are chosen through M5237 register Index-40h bit26 setting. When this bit is reset as 0, GPIO[4] is chosen for green or system event control. When this bit is set as 1, USBP2+ is chosen to support USB Port2 data signal.

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Pin Description Table (continued) :

Pin Name	Type	Description
ISA Bus Interface :		
SD[3]/ GPIO[3]/ CVROFF	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 3 or General Purpose I/O or Infrared Mode Switching.** This pin is a multi-function pin selected by hardware and software setting. When pin TC is pulled low, SD[3] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[3]/CVROFF functions are selected. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL. GPIO[3] or CVROFF are chosen through M1543C register Index-6Dh bit4 setting. When this bit is reset as 0, GPIO[3] is chosen for green or system event control. When this bit is set as 1, CVROFF is chosen to support Infrared. This pin is used in IBM like module to control the speed of the module.
SD[2]/ GPIO[2]/ IRRX	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 2 or General Purpose I/O or Infrared Receive.** This pin is a multi-function pin selected by hardware and software setting. When pin TC is pulled low, SD[2] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[2]/IRRX functions are selected. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL. GPIO[2] or IRRX are chosen through M1543C register Index-6Dh bit4 setting. When this bit is reset as 0, GPIO[2] is chosen for green or system event control. When this bit is set as 1, IRRX is chosen to support Infrared. This pin is used as Infrared serial data input signal.
SD[1]/ GPIO[1]/ IRRXH	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 1 or General Purpose I/O or Infrared Control Signal.** This pin is a multi-function pin selected by hardware and software setting. When pin TC is pulled low, SD[1] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[1]/IRRXH functions are selected. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL. GPIO[1] or IRRXH are chosen through M1543C register Index-6Dh bit4 setting. When this bit is reset as 0, GPIO[1] is chosen for green or system event control. When this bit is set as 1, IRRXH is chosen to support Infrared. In HP like transceiver module, this is the high speed receiver signal input (1 to 4 Mb/s). In IBM like transceiver module, this is an output signal to control the SD/MODE signal which will control the speed of the module.
SD[0]/ GPIO[0]/ IRTX	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus Line 0 or General Purpose I/O or Infrared Transmit.** This pin is a multi-function pin selected by hardware and software setting. When pin TC is pulled low, SD[0] is selected. No external LS245 TTL is required to support SD[7:0] bus. When pin TC is pulled high, GPIO[0]/IRTX functions are selected. In this hardware configuration, external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL. GPIO[0] or IRTX are chosen through M1543C register Index-6Dh bit4 setting. When this bit is reset as 0, GPIO[0] is chosen for green or system event control. When this bit is set as 1, IRTX is chosen to support Infrared. This pin is used as Infrared serial data output signal.
SA[19:17]	O-Group A 12/12 mA	**ISA Slot Address Bus A19-A17.** These pins should connect to the ISA System Address Bus.
SA[16:0]	I/O-Group A 12/12 mA	**ISA Slot Address Bus A16-A0.** These pins should connect to the ISA System Address Bus.
SBHEJ	I/O -Group A 12/12 mA	**ISA Byte High Enable.** This pin should connect to the ISA System Byte High Enable pin.

Pin Description Table (continued) :

Pin Name	Type	Description
ISA Bus Interface :		
LA[23:22], LA[20:17]	I/O-Group A 12/12 mA	**ISA Latched Address Bus.** They are inputs during ISA master cycle and should connect to ISA Slot Latch Address Bus.
LA[21]/ KBCLK	I/O-Group C 12/12 mA	**ISA Latched Address Bus Line 21 or Keyboard Clock.** This pin is a multi-function pin. When pin PCSJ is pulled high which means Hotkey function is disabled, this pin is LA[21] as the ISA Latched Address Bus Line 21. When pin PCSJ is pulled low which means Hotkey function is enabled, this pin will become KBCLK and should connect to Keyboard. (Please see 5.4.1)
IO16J	I -Group A	**ISA 16 Bit I/O Device Indicator.** This is an input and will be driven by the device if the ISA I/O cycle is a 16-bit access.
M16J	I/O-Group A 12/20 mA	**ISA 16 Bit Memory Device Indicator.** This pin will be driven by the device or by the M1543C if the ISA Memory cycle is a 16-bit access.
MEMRJ	I/O-Group A 12/12 mA	**ISA Memory Read.** This signal is an output when the M1543C is the ISA Bus master, or an input during ISA master cycle.
MEMWJ	I/O -Group A 12/12 mA	**ISA Memory Write.** This signal is an output when the M1543C is the ISA Bus master, or an input during ISA master cycle.
AEN	O-Group A 12/12 mA	**ISA I/O Address Enable.** This signal will become active high during DMA cycle to prevent I/O device to decode DMA cycles as valid I/O cycles.
IOCHRDY	I/O-Group A 12/20 mA	**ISA System Ready.** This signal is an output during ISA master cycle, or an input when the M1543C is the ISA Bus master .
NOWSJ	I-Group A	**ISA Zero Wait-State for Input.** This input signal will terminate the CPU to ISA command instantly.
IOCHKJ	I-Group A	**ISA Parity Error.** M1543C will generate NMI to CPU when this signal is asserted.
SYSCLK	O-Group A 12/12 mA	**ISA System Clock.** This output is generated by the PCI clock or OSC14M clock and is used as the ISA system clock.
BALE	O-Group A 12/12 mA	**Bus Address Latch Enable.** BALE will be asserted throughout DMA, ISA master, and the Refresh cycles. Otherwise, it will only assert half the SYSCLK before the ISA command is asserted.
IORJ	I/O-Group A 12/16 mA	**ISA I/O Read.** This signal is an input during ISA master cycle, and an output when the M1543C is the ISA Bus master.
IOWJ	I/O-Group A 12/12 mA	**ISA I/O write.** This signal is an input during ISA master cycle, and an output when the M1543C is the ISA Bus master.
SMEMRJ	O-Group A 12/12 mA	**ISA System Memory Read.** This signal indicates that the memory read command is below 1M Byte address.
SMEMWJ	O-Group A 12/12 mA	**ISA System Memory Write.** This signal indicates that the memory write command is below 1M Byte address.
DREQ[7:5], DREQ[3:0]	I-Group A Schmitt	**DMA Request Signals.** These are inputs from the DMA Device or ISA Master Request. The M1543C will combine the DMA request, ISA Master request, IDE Bus Master request, and USB Master request to generate the PHOLDJ to the PCI Arbiter.
DACKJ[7:5], DACKJ[3:0]	O-Group A 9.6/9.6 mA	**DMA Acknowledge Signals.** After the M1543C has acquired the PCI Bus grant (PHLDAJ), the internal arbiter will assert the DMA acknowledge signal to the DMA Device Request.
TC	I/O-Group A 12/12 mA	**DMA End of Process.** This signal will be asserted after the DMA Device has ended the transaction. This pin is also used as hardware configuration to select SD bus function. Please refer to section 1.4 for more detailed information.
REFRSHJ	I/O Group A 12/20 mA	**ISA Refresh Cycle.** This signal is an input during ISA master cycle, and an output when the M1543C is the ISA Bus master.

Pin Description Table (continued) :

Pin Name	Type	Description
Miscellaneous Logic :		
SPKR	I/O Group A 4.8/4.8 mA	**Speaker Output.** This pin is used to control the Speaker Output and should connect to the Speaker. This pin is also used as hardware configuration to enable Super I/O test mode. In normal operation, it must be pulled high.
RTCAS	O-Group A 4.8/4.8 mA	**RTC Address Strobe.** This pin is used as the RTC Address Strobe and should connect to the RTC.
RTCRW	O-Group A 4.8/4.8 mA	**RTC Write Strobe.** This pin is used as the RTC Read/Write Command and should connect to the RTC. The M1543C will drive the RTC command through dedicated pin instead of the 74F32 decode to save the system cost.
RTCDS	O-Group A 4.8/4.8 mA	**RTC Data Strobe.** This pin is used as the RTC Data Strobe and should connect to the RTC.
SPLED	I/O-Group A 4.8/4.8 mA	**Speed LED Output.** This pin is used to control the Speed LED Output and should be connected to LED. This pin is also used as hardware configuration to support 256KB ROM (Pull Low) or 128KB ROM (Pull High).
ROMKBCSJ	O-Group A 4.8/4.8 mA	**ROM/Keyboard Chip Select.** This pin is the ROM chip select and is the Keyboard chip select also when internal KBC is disabled. This pin is also used as hardware configuration to enable M1543C test mode. In normal operation, it must be pulled high.
SERIRQ/ GPI[2]	I/O Group A 12/16 mA	**Serial Interrupt Request or General Purpose Input.** This pin is used to support the serial interrupt protocol or as a General Purpose Input. The pin function is selected by M1543C register Index-59h bit2 setting. Value 0 is used to select GPI[2], and value 1 is used to select SERIRQ.
SIRQI	I -Group A	**Steerable IRQ Input1.** This is a steerable Interrupt input, M1543C will provide a Routing Mechanism to route this Interrupt to any 8259 input.
SIRQII	I -Group A	**Steerable IRQ Input2.** This is a steerable Interrupt input, M1543C will provide a Routing Mechanism to route this Interrupt to any 8259 input.
IRQ8J	I -Group C	**RTC Interrupt Input.** This is the RTC Interrupt input. This pin belongs to the Power Group C, and it can support the RTC Alarm function during Soft-off or Suspend state.
XDIR/ GPO[12]	I/O Group A 4.8/4.8 mA	**XD Bus Direction Control or General Purpose Output.** When external XD bus is designed to generate SD[7:0] bus on motherboard (TC is pulled high), this pin is X-bus direction control. Otherwise (TC is pulled low), this pin is a general purpose output. This pin is also used as hardware configuration to choose Pentium II CPU (Pull Low) or Pentium CPU (Pull High).
KBINH/ IRQ1I	I/O Group A 12/24 mA	**Keyboard Inhibit or Interrupt One Input.** This pin will be the Keyboard Inhibit input when internal KBC is enabled (RTS2J is pulled high). Otherwise (RTS2J is pulled low), it will be the IRQ1 input.
KBCLK/ LA[21]/ GPI[9]	I/O Group A 12/24 mA	**Keyboard Clock or ISA Latched Address Bus Line 21 or General Purpose Input.** This pin is the Keyboard interface Clock when internal KBC is enabled & Hotkey function is disabled (RTS2J is pulled high & PCSJ is pulled high). This pin is ISA Latched Address Bus line 21 when internal KBC is enabled & Hotkey function is enabled (RTS2J is pulled high & PCSJ is pulled low). Otherwise (RTS2J is pulled low), it is a general purpose input. (Please see 5.4.1)
KBDATA/ IRQ10/ GPI[10]	I/O Group A 12/24 mA	**Keyboard data or ISA Interrupt Request Line 10 or General Purpose Input.** This pin is a KB interface DATA when internal KBC is enabled & Hotkey function is disabled (RTS2J is pulled high & PCSJ is pulled high). This pin is ISA Interrupt Request line 10 when internal KBC is enabled & Hotkey function is enabled (RTS2J is pulled high & PCSJ is pulled low). Otherwise (RTS2J is pulled low), this pin is a general purpose input. (Please see 5.4.1)
MSCLK/ GPI[11]	I/O Group A 12/24 mA	**Mouse Clock or General Purpose Input.** This pin is a mouse clock when internal PS2 Keyboard is enabled (DTR2J is pulled high). Otherwise (DTR2J is pulled low), this pin is a general purpose input.
MSDATA/ IRQ12I	I/O Group A 12/24 mA	**Mouse Data or Interrupt Line 12 Input.** This pin is mouse data when internal PS2 Keyboard is enabled (DTR2J is pulled high). Otherwise (DTR2J is pulled low), this pin is the IRQ12 input.

Pin Description Table (continued) :

Pin Name	Type	Description
Miscellaneous Logic :		
BIOSA17/ GPO[19]	O-Group A 4.8/4.8 mA	**ROM Address 17 or General Purpose Output.** This pin is the ROM A17 control when 2M ROM is used, or it is a general purpose output.
BIOSA16/ GPO[18]	O-Group A 4.8/4.8 mA	**ROM Address 16 or General Purpose Output.** This pin is the ROM A16 control when 2M ROM is used, or it is a general purpose output.
PCSJ/ GPO[0]/ APICCSJ	I/O Group A 4.8/4.8 mA	**Programmable Chip Select or General Purpose Output or APIC chip select.** This pin can be selected as a programmable Chip Select, or as a general purpose output. The pin function is selected by M1543C register Index-5Ah bit0 setting. Value 0 is used to select PCSJ, and value 1 is used to select GPO[0]. This pin is also used as the hardware configuration to enable the Hotkey function (Pull Low).
IDE interface :		
PIDEDRQ	I-Group A	**Primary IDE DMA Request for IDE Master.** This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.
SIDEDRQ	I-Group A	**Secondary IDE DMA Request for IDE Master.** This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.
PIDEDAKJ	O Group A 9.6/9.6 mA	**Primary IDE DACKJ for IDE Master.** This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.
SIDEDAKJ	O Group A 9.6/9.6 mA	**Secondary IDE DACKJ for IDE Master.** This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.
PIDERDY	I-Group A	**Primary IDE Ready.** This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different function. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by M5229 to strobe the input data. In write cycle, this pin is used by IDE device to notify M5229 as DMA Ready (DDMARDYJ).
SIDERDY	I-Group A	**Secondary IDE Ready.** This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions. In read cycle, IDE device will drive this signal as Data Strobe (DSTROBE) to use by M5229 to strobe the input data. In write cycles, this pin is used by IDE device to notify M5229 as DMA Ready (DDMARDYJ).
PIDEIORJ	O-Group A 12/12 mA	**Primary IDE IORJ Command.** This is the IORJ command output pin to notify the Primary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions. In read cycle, this pin is used by M5229 to notify IDE device as DMA Ready (DDMARDYJ). In write cycle, M5229 will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.
SIDEIORJ	O-Group A 12/12 mA	**Secondary IDE IORJ Command.** This is the IORJ command output pin to notify the Secondary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different function. In read cycle, this pin is used by M5229 to notify IDE device as DMA Ready (DDMARDYJ). In write cycle, M5229 will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.
PIDEIOWJ	O-Group A 12/12 mA	**Primary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Primary IDE device that the available Write Data is already asserted by M5229 in PIO and DMA mode. In Ultra-33 mode, this pin is driven by M5229 to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.
SIDEIOWJ	O-Group A 12/12 mA	**Secondary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Secondary IDE device that the available Write Data is already asserted by M5229 in PIO and DMA mode. In Ultra-33 mode, this pin is driven by M5229 to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.

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Pin Description Table (continued) :

Pin Name	Type	Description
IDE interface :		
PIDECS1J	O-Group A 12/12 mA	**IDE Chip Select 1 for Primary Channel 0.** This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3J	O-Group A 12/12 mA	**IDE Chip Select 3 for Primary Channel 1.** This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
SIDECS1J	O-Group A 12/12 mA	**IDE Chip Select 1 for Secondary Channel 0.** This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3J	O-Group A 12/12 mA	**IDE Chip Select 3 for Secondary Channel 1.** This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
PIDEA[2:0]	O-Group A 12/12 mA	**Primary IDE ATA Address Bus.** These are the Address pins connected to Primary Channel.
SIDEA[2:0]	O-Group A 12/12 mA	**Secondary IDE ATA Address Bus.** These are the Address pins connected to Secondary Channel.
PIDED[15:0]	I/O- Group A 9.6/9.6 mA	**Primary IDE ATA Data Bus.** These are the Data pins connected to Primary Channel.
SIDED[15:0]	I/O-Group A 9.6/9.6 mA	**Secondary IDE ATA Data Bus.** These are the Data pins connected to Secondary Channel.
Power Management Unit :		
RSM_RSTJ	I-Group C Schmitt	**Resume Circuit Initial Reset Input.** This input is used to initialize the resume circuit.
SMIJ	O-Group E 4/4 mA	**SMM Interrupt Output.** This output should be connected to CPU SMM Interrupt input.
STPCLKJ	O-Group E 4/4 mA	**Stop CPU Internal Clock Output.** This output is used to stop the CPU internal clock and should be connected to CPU STPCLKJ input.
SLEEPJ/ GPO[20]	O-Group E 4/4 mA	**Pentium II Sleep State or General Purpose Output.** This output will force Pentium II CPU to enter Sleep State, or as a general purpose output. The pin function is selected by the Hardware Configuration of pin XDIR. When XDIR is pulled low, SLEEPJ is selected. Otherwise, GPO[20] is selected.
ZZ/ GPO[1]	O-Group E 4/4 mA	**PBSRAM Power Saving Mode or General Purpose Output.** This output is used to control L2 cache entering power saving mode, or as a general purpose output. The pin function is selected by M1543C register Index-5Ah bit1 setting. Value 0 is used to select ZZ, and value 1 is used to select GPO[1].
CPU_STPJ/ GPO[2]	O-Group B 4/4 mA	**Clock Cell CPU Clock Stop or General Purpose Output.** This output is used to stop the CPU Clock of the clock generator, or as a general purpose output. The pin function is selected by M1543C register Index-5Ah bit2 setting. Value 0 is used to select CPU_STPJ, and value 1 is used to select GPO[2].
PCI_STPJ/ GPO[3]	O-Group B 4/4 mA	**Clock Cell PCI Clock Stop or General Purpose Output.** This output is used to stop the PCI Clock of the clock generator, or as a general purpose output. The pin function is selected by M1543C register Index-5Ah bit3 setting. Value 0 is used to select PCI_STPJ, and value 1 is used to select GPO[3].
SUSTAT1J	O-Group C 4/4 mA	**Suspend Status for North Bridge.** This output is used to notice the north bridge to control DRAM suspend refresh circuit.
PWRBTNJ	I-Group C Schmitt	**Power Button Input.** This input is used to support the ACPI Power Button function.
PCIREQJ/ GPI[3]	I-Group B	**PCI Bus Request Event Input or General Purpose Input.** This input comes from the North Bridge or external circuit to notice M1543C there is PCI request pending. This pin can also be programmed as a general purpose input. The pin function is selected by M1543C register Index-59h bit3 setting. Value 0 is used to select PCIREQJ, and value 1 is used to select GPI[3].

Pin Description Table (continued) :

Pin Name	Type	Description
Power Management Unit :		
SQWO/ GPIOW/ GPO[9]	O-Group A 4/4 mA	**Square Wave Output or Extended GPIO Write or General Purpose Output.** This output can be used to output Square Wave with 1Hz or 2Hz, or as the extended GPIO Write command, or as a general purpose output. The pin function is selected by M1543C register Index-5Ah bits[9:8] setting. Value 00 is used to select SQWO, value 01 is used to select GPIOW, and value 1X is used to select GPO[9].
OFF_PWR1/ GPO[22]	O-Group C 4/4 mA	**Remove All Circuit Power Except Internal Suspend Circuit and External DRAM or General Purpose Output.** OFF_PWR1 and OFF_PWR2 can be used to support Suspend to DRAM system state. OFF_PWR1 is used to control the Power plan of DRAM circuit. In Suspend to DRAM state, OFF_PWR1 will not become active high to enable DRAM circuit to do Suspend Refresh. The pin is multi-functional and is selected by M7101 register Index-C6h bit1 setting. Value 0 is used to select OFF_PWR1, and value 1 is used to select GPO[22].
OFF_PWR2/ GPO[23]	O-Group C 4/4 mA	**Remove All Circuit Power Except Internal Suspend Circuit or General Purpose Output.** OFF_PWR2 and OFF_PWR1 can be used to support Suspend to DRAM state. OFF_PWR2 is used to control the Power plan except DRAM circuit. In Suspend to DRAM state, OFF_PWR2 will become active high to disable all the circuits except M1543C internal Suspend & DRAM circuit (controlled by OFF_PWR1). The pin is multi-functional and is selected by M7101 register Index-C6h bit2 setting. Value 0 is used to select OFF_PWR2, and value 1 is used to select GPO[23].
RI	I-Group C Schmitt	**Ring-in.** This input connects to Modem Ring-in input to support ACPI Ring-in function. The signal is active High by default, but can become active Low by setting M7101 register Index-90h bit2 = 1.
THRMJ	I-Group A Schmitt	**Thermal Event Input or General Purpose Input.** THRMJ is a triggered input to the M1543C showing that the external thermal detected circuits are requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input switch.
ACPWR	I-Group C Schmitt	Baby AT or ATX hardware configure input. This chip supports baby AT power supply when pull low, ATX power supply when pull high. In AT power mode, M1543C will enable the power on sequence when the power comes in. But in ATX power mode, M1543C will enter Soft-Off mode when the ATX Standby power comes in at the first time, and then enable the power on sequence after the Power Button is pushed. This pin has a 40K internal pull-low resistor.
DOCKJ/ SLPBTNJ	I-Group C	**Docking Insert Event Input or General Purpose Input or Sleep Button Input.** This triggered input is used as a docking event indicator, or as a general purpose input switch. It can also become as the Sleep Button input defined in ACPI specification when M7101 Register Index 90h bit3 = 1.
USB interface :		
USBP0+ USBP0-	I/O-Group B	**Universal Serial Bus Port 0.** These are the serial data pair for USB Port 0.
USBP1+ USBP1-	I/O-Group B	**Universal Serial Bus Port 1.** These are the serial data pair for USB Port 1.
OVCRJ/ GPI[0]	I Group B	**Over Current Detect Inputs or General Purpose Input.** This pin is used to monitor the USB Power Over Current, or as a general purpose input. The pin function is selected by M1543C register Index-59h bit0 setting. Value 0 is used to select OVCRJ, and value 1 is used to select GPI[0].
SM Bus signal :		
SMBCLK	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Clock.** SM Bus clock signal should be combined with SM Bus data to carry information between the devices connected to the SM Bus.
SMBDATA	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Data Line.** SM Bus data signal should be combined with SM Bus clock to carry information between the devices connected to the SM Bus.

Pin Description Table (continued) :

Pin Name	Type	Description
Floppy Disk Interface :		
RDATAJ (normal) (PPM mode)	I Group A Schmitt	**Read Data.** The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data. **Read Data.** An additional Read Data signal in PPM mode. RDATAJ is multiplexed with PD[3].
WGATEJ (normal) (PPM mode)	O Group A 4/36 mA	**Write Gate**. This active-low, high-drive output enables the write circuitry of the selected disk drive. **Write Gate**. An additional Write Gate signal in PPM mode. WGATEJ is multiplexed with SLCT.
0WDATAJ (normal) (PPM mode)	O Group A 4/36 mA	**Write Data**. This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media. **Write Data.** An additional Write DATA signal in PPM mode. Write Data is multiplexed with PE.
HDSELJ (normal) (PPM mode)	O Group A 4/36 mA	**Head Select**. This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1. **Head Select.** An additional Head Select signal in PPM mode. Head Select is multiplexed with ERRORJ.
DIRJ (normal) (PPM mode)	O Group A 4/36 mA	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). **Direction.** An additional Direction signal in PPM mode. Direction is multiplexed with INITJ.
STEPJ (normal) (PPM mode)	O Group A 4/36 mA	**Step.** This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation. **Step**. An additional Step signal in PPM mode. Step is multiplexed with SLCTINJ.
DSKCHGJ (normal) (PPM mode)	I Group A Schmitt	**Disk Change.** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of location base+7. **Disk Change.** An additional Disk Change signal in PPM mode. Disk Change is multiplexed with PD[4].
DRV0J, DRV1J (normal) (PPM mode)	O Group A 4/36 mA	**Drive Select 0, 1**. Active low, output select drives 0-1. **Drive Select 0,1.** An additional Drive Select signals in PPM mode. Drive Select signal 0 and 1 are multiplexed with STROBJ and ACKJ.
MOT0J, MOT1J (normal) (PPM mode)	O Group A 4/36 mA	**Motor On 0, 1**. These active-low outputs select motor drives 0-1. **Motor On 0,1.** Additional Motor On signals in PPM mode. Motor On 0 and 1 are multiplexed with PD[6] and BUSY.
WPROTJ (normal) (PPM mode)	I Group A Schmitt	**Write Protect**. This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected. **Write Protect.** An additional Write Protect signal in PPM. Write Protect is multiplexed with PD[2].
TRK0J (normal) (PPM mode)	I Group A Schmitt	**Track 0**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track. **Track 0.** An additional Track 0 signal in PPM mode. Track 0 is multiplexed with PD[1].
INDEXJ (normal) (PPM mode)	I Group A Schmitt	**Index**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole. **Index.** An additional Index signal in PPM mode. Index is multiplexed with PD[0]
DENSEL (normal) (PPM mode)	O Group A 4/36 mA	**Density Select**. Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected. **Density Select.** An additional Density Select signal in PPM mode. Density Select is multiplexed with AUTOFDJ.

Pin Description Table (continued) :

Pin Name	Type	Description
Serial Port Interface :		
SIN1, SIN2	I - Group A Schmitt	**Receive Data**. Receiver serial data input signal.
SOUT1, SOUT2	O-Group A 4/4 mA	**Transmit Data**. Transmitter serial data output from Serial Port.
RTS1J	O Group A 4/4 mA	**Request to Send**. Active low Request to Send output for UART port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
CFG_PORT	I Group A Schmitt	**Configuration Port Select.** During reset active, this input is read and latched to define the configuration register's base address. If CFG_PORT=1, 3F0 is selected. If CFG_PORT=0, 370 is selected. This pin has a 20K internal pull-up resistor.
RTS2J	O Group A 4/4 mA	**Request to Send**. Active low Request to Send output for UART port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
KBC_EN	I Group A Schmitt	**KBC Enable Control.** During reset active, this input is read and latched to enable KBC after reset. The enable could be overwritten by configuration register. This pin has a 20K internal pull-up resistor.
DTR1J	O Group A 4/4 mA	**Data Terminal Ready**. This is an active low output for UART port. Handshake output signal signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation.
DTR2J	O Group A 4/4 mA	**Data Terminal Ready**. This is an active low output for UART port. Handshake output signal signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation.
PS2_ATJ	I-Group A Schmitt	**KBC PS/2 or AT mode select.** During reset active, this input is read and latched to define the KBC is PS/2 or AT mode. This pin has a 20K internal pull-up resistor.
CTS1J CTS2J	I Group A Schmitt	**Clear to Send**. This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTSJ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	I Group A Schmitt	**Data Set Ready.** This active low input is for UART ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit5 of Modem Status Register (MSR). A DSRJ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. Note: Bit 5 of MSR is the complement of DSRJ.
DCD1J DCD2J	I Group A Schmitt	**Data Carrier Detect**. This active low input is for UART ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. Note : bit 7 of MSR is the complement of DCDJ.

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Pin Description Table (continued) :

Pin Name	Type	Description
RI1J, RI2J	I Group A Schmitt	**Ring Indicator**. This active low input is for UART ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). An RIJ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note : bit 6 of MSR is the complement of RIJ.
BOUT1, BOUT2	O-Group A 4/4 mA	**Baud Rate Output.** Multiplexed output signals to provide the associated serial channel Baud Rate generator output signal.
Printer Port Interface :		
AUTOFDJ	O Group A 16/16 mA	**Autofeed Output**. This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
INITJ	O-Group A 16/16 mA	**Initiate Output**. This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
SLCTINJ	O-Group A 16/16 mA	**Printer select input**. This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
STROBJ	O-Group A 8/16 mA	**Strobe Output**. This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	I -Group A Schmitt	**Busy**. This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	I Group A Schmitt	**Acknowledge**. This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	I - Group A Schmitt	**Paper End**. This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
SLCT	I - Group A Schmitt	**Printer Selected Status**. This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	I - Group A Schmitt	**Error**. This active low signal indicates an error condition at the printer.
PD[7:0]	I/O Group A 16/16 mA	**Port Data**. This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
Power Pins :		
VCC_A	P	**Vcc for Power Group A.** This power is 5V used for ISA interface & IDE interface.
VCC_3A	P	**Vcc for Power Group A.** This power is 3.3V used for ISA interface & IDE interface.
VCC_B	P	**Vcc for Power Group B.** This power is 3.3V used for PCI interface.
VCC_C	P	**Vcc for Power Group C.** The power is 3.3V/5V used for resume/suspend control interface output signals during normal operation and suspend periods.
VCC_3C	P	**Vcc for Power Group C.** This power is 3.3V used for Resume/Suspend Control interface input signals.
VCC_E	P	**Vcc 3.3V or 2.5V for Power Group E.** This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VDD_5	P	**Vcc 5.0V for core Power.** It supplies the core power for the internal circuit except the suspend circuit.
VDD_5S	P	**Vcc 5.0V for Suspend/Resume Core Power.** It supplies the core power for the internal suspend/resume circuit.
Vss or Gnd	P	**Ground.**

2.3 Numerical Pin List

Pin No.	Pin Name	Type
A1	AD21	I/O
A2	AD20	I/O
A3	AD19	I/O
A4	AD16	I/O
A5	IRDYJ	I/O
A6	SERRJ	I
A7	AD14	I/O
A8	AD10	I/O
A9	AD6	I/O
A10	AD1	I/O
A11	PHOLDJ	O
A12	PCIREQJ	I
A13	USBP1-	I/O
A14	RTCDS	O
A15	ROMKBCSJ	O
A16	XD2	I/O
A17	XD5	I/O
A18	SD15	I/O
A19	SD14	I/O
A20	SD13	I/O
B1	CBEJ3	I/O
B2	AD23	I/O
B3	AD22	I/O
B4	AD17	I/O
B5	FRAMEJ	I/O
B6	STOPJ	I/O
B7	AD15	I/O
B8	AD11	I/O
B9	AD7	I/O
B10	AD2	I/O
B11	PHLDAJ	I
B12	USBCLK	I
B13	USBP0+	I/O
B14	RTCRW	O
B15	XD0	I/O
B16	XD3	I/O
B17	XD6	I/O
B18	SD12	I/O
B19	DREQ7	I
B20	SD11	I/O
C1	AD26	I/O
C2	AD25	I/O
C3	AD24	I/O
C4	AD18	I/O
C5	CBEJ2	I/O

Pin No.	Pin Name	Type
C6	DEVSELJ	I/O
C7	CBEJ1	I/O
C8	AD12	I/O
C9	CBEJ0	I/O
C10	AD3	I/O
C11	PCI_STPJ	O
C12	OVCRJ	I
C13	USBP0-	I/O
C14	RTCAS	O
C15	XD1	I/O
C16	XD4	I/O
C17	XD7	I/O
C18	DACKJ7	O
C19	SD10	I/O
C20	DREQ6	I
D1	AD29	I/O
D2	AD28	I/O
D3	AD27	I/O
D4	AD30	I/O
D5	AD31	I/O
D6	TRDYJ	I/O
D7	PAR	I/O
D8	AD13	I/O
D9	AD8	I/O
D10	AD4	I/O
D11	CPU_STPJ	O
D12	SIRQI	I
D13	BIOSA17	O
D14	XDIR	I/O
D15	PCSJ	I/O
D16	SERIRQ	I/O
D17	SPKR	O
D18	SD9	I/O
D19	DACKJ6	O
D20	SD8	I/O
E1	PIDECS3J	O
E2	PIDECS1J	O
E3	PIDEA2	O
E4	INTAJ_MI	I
E5	INTBJS0	I/O
E6	INTCJS1	I/O
E7	PCIRSTJ	O
E8	PCICLK	I
E9	AD9	I/O
E10	AD5	I/O

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Numerical Pin List (continued)

Pin No.	Pin Name	Type
E11	AD0	I/O
E12	USBP1+	I/O
E13	SIRQII	I
E14	BIOSA16	O
E15	SQWO	O
E16	THRMJ	I
E17	SPLED	O
E18	DREQ5	I
E19	MEMWJ	I/O
E20	DACKJ5	O
F1	PIDEA0	O
F2	PIDEA1	O
F3	PIDEDAKJ	O
F4	INTDJS2	I/O
F5	PIDERDY	I
F6	VCC_B	P
F14	VCC_A	P
F15	VCC_E	P
F16	KBINH	I/O
F17	MEMRJ	I/O
F18	DREQ0	I
F19	LA17	I/O
F20	DACKJ0	O
G1	PIDEIORJ	O
G2	PIDEIOWJ	O
G3	PIDEDRQ	I
G4	PIDED15	I/O
G5	PIDED0	I/O
G6	VCC_A	P
G15	VCC_3C	P
G16	LA18	I/O
G17	IRQ14	I/O
G18	INIT	O
G19	A20MJ	O
G20	FERRJ	I
H1	PIDED14	I/O
H2	PIDED1	I/O
H3	PIDED13	I/O
H4	PIDED2	I/O
H5	PIDED12	I/O
H16	LA19	I/O
H17	IRQ15	I/O
H18	SMIJ	O
H19	NMI	O
H20	INTR	O

Pin No.	Pin Name	Type
J1	PIDED3	I/O
J2	PIDED11	I/O
J3	PIDED4	I/O
J4	PIDED10	I/O
J5	PIDED5	I/O
J9	GND	P
J10	GND	P
J11	GND	P
J12	GND	P
J16	LA20	I/O
J17	SLEEPJ	O
J18	STPCLKJ	O
J19	IGNNEJ	O
J20	CPURST	O
K1	PIDED9	I/O
K2	PIDED6	I/O
K3	PIDED8	I/O
K4	PIDED7	I/O
K5	SIDECS3J	O
K9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K16	ZZ	O
K17	OFF_PWR1	O
K18	RSMRSTJ	I
K19	SUSTAT1J	O
K20	ACPWR	I
L1	SIDECS1J	O
L2	SIDEA2	O
L3	SIDEA0	O
L4	SIDEA1	O
L5	SIDEDAKJ	O
L9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L16	SMBDATA	I/O
L17	OFF_PWR2	O
L18	DOCKJ	I
L19	IRQ8J	I
L20	PWRBTNJ	I
M1	SIDERDY	I
M2	SIDEIORJ	O
M3	SIDEIOWJ	O

Numerical Pin List (continued)

Pin No.	Pin Name	Type
M4	SIDEDRQ	I
M5	SIDED15	I/O
M9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M16	SMBCLK	I/O
M17	LA21	I/O
M18	RI	I
M19	CLK32KO	I/O
M20	PWG	I
N1	SIDED0	I/O
N2	SIDED14	I/O
N3	SIDED1	I/O
N4	SIDED13	I/O
N5	SIDED2	I/O
N15	VDD_5S	P
N16	IRQ11	I/O
N17	LA22	I/O
N18	IRQ10	I/O
N19	OSC32KII	I
N20	OSC32KI	I
P1	SIDED12	I/O
P2	SIDED3	I/O
P3	SIDED11	I/O
P4	SIDED4	I/O
P5	DIRJ	O
P6	VCC_A	P
P15	VCC_C	P
P16	LA23	I/O
P17	IO16J	I
P18	SBHEJ	I/O
P19	M16J	I/O
P20	OSC14M	I
R1	SIDED10	I/O
R2	SIDED5	I/O
R3	SIDED9	I/O
R4	MOT1J	O
R5	DRV0J	O
R6	VDD_5	P
R7	VCC_A	P
R14	VCC_3A	P
R15	VCC_A	P
R16	BALE	O
R17	TC	O

Pin No.	Pin Name	Type
R18	SA0	I/O
R19	SA1	I/O
R20	SA2	I/O
T1	SIDED6	I/O
T2	SIDED8	I/O
T3	DSKCHGJ	I/O
T4	DRV1J	O
T5	MOT0J	O
T6	DENSEL	O
T7	DCD1J	I
T8	PD3	I/O
T9	ACKJ	I
T10	RSTDRV	O
T11	MSCLK	O
T12	MSDATA	I/O
T13	SD0	I/O
T14	SA19	I/O
T15	DACKJ3	O
T16	DACKJ2	O
T17	SA6	I/O
T18	SA3	I/O
T19	SA4	I/O
T20	SA5	I/O
U1	SIDED7	I/O
U2	HDSELJ	O
U3	RDATAJ	I
U4	INDEXJ	I
U5	DCD2J	I
U6	DSR1J	I
U7	STROBJ	O
U8	PD4	I/O
U9	BUSY	I
U10	ERRORJ	I
U11	KBCLK	I/O
U12	KBDATA	I/O
U13	SD1	I/O
U14	SMEMRJ	O
U15	SA17	I/O
U16	IRQ3	I/O
U17	IRQ5	I/O
U18	SA8	I/O
U19	SA7	I/O
U20	IRQ4	I/O
V1	WPROTJ	I
V2	TRK0J	I

Numerical Pin List (continued)

Pin No.	Pin Name	Type
V3	WGATEJ	O
V4	DTR2J	O
V5	RI1J	I
V6	DTR1J	O
V7	PD0	I/O
V8	PD5	I/O
V9	PE	I
V10	INITJ	O
V11	IRQ9	I/O
V12	DREQ2	I
V13	NOWSJ	I
V14	AEN	O
V15	IORJ	I/O
V16	SA15	I/O
V17	DREQ1	I
V18	SA10	I/O
V19	IRQ6	I/O
V20	SA9	I/O
W1	WDATAJ	O
W2	STEPJ	O
W3	RTS2J	O
W4	SOUT2	O
W5	CTS1J	I
W6	SOUT1	I/O
W7	PD1	I/O
W8	PD6	I/O
W9	SLCT	I
W10	SLCTINJ	O
W11	SD6	I/O
W12	SD4	I/O
W13	SD2	I/O
W14	SMEMWJ	O
W15	SA18	I/O
W16	DREQ3	I
W17	SA14	I/O
W18	SYSCLK	O
W19	SA11	I/O
W20	IRQ7	I/O
Y1	RI2J	I
Y2	CTS2J	I
Y3	DSR2J	I
Y4	SIN2	I
Y5	RTS1J	O
Y6	SIN1	I
Y7	PD2	I/O
Y8	PD7	I/O
Y9	AUTOFDJ	O
Y10	IOCHKJ	I
Y11	SD7	I/O
Y12	SD5	I/O
Y13	SD3	I/O
Y14	IOCHRDY	I/O
Y15	IOWJ	I/O
Y16	SA16	I/O
Y17	DACKJ1	O
Y18	SA13	I/O
Y19	REFRSHJ	I
Y20	SA12	I/O

2.4 Alphabetical Pin List

Pin No.	Pin Name	Type
G19	A20MJ	O
T9	ACKJ	I
K20	ACPWR	I
E11	AD0	I/O
A10	AD1	I/O
A8	AD10	I/O
B8	AD11	I/O
C8	AD12	I/O
D8	AD13	I/O
A7	AD14	I/O
B7	AD15	I/O
A4	AD16	I/O
B4	AD17	I/O
C4	AD18	I/O
A3	AD19	I/O
B10	AD2	I/O
A2	AD20	I/O
A1	AD21	I/O
B3	AD22	I/O
B2	AD23	I/O
C3	AD24	I/O
C2	AD25	I/O
C1	AD26	I/O
D3	AD27	I/O
D2	AD28	I/O
D1	AD29	I/O
C10	AD3	I/O
D4	AD30	I/O
D5	AD31	I/O
D10	AD4	I/O
E10	AD5	I/O
A9	AD6	I/O
B9	AD7	I/O
D9	AD8	I/O
E9	AD9	I/O
V14	AEN	O
Y9	AUTOFDJ	O
R16	BALE	O
E14	BIOSA16	O
D13	BIOSA17	O
U9	BUSY	I
C9	CBEJ0	I/O
C7	CBEJ1	I/O
C5	CBEJ2	I/O
B1	CBEJ3	I/O

Pin No.	Pin Name	Type
M19	CLK32KO	I/O
D11	CPU_STPJ	O
J20	CPURST	O
W5	CTS1J	I
Y2	CTS2J	I
F20	DACKJ0	O
Y17	DACKJ1	O
T16	DACKJ2	O
T15	DACKJ3	O
E20	DACKJ5	O
D19	DACKJ6	O
C18	DACKJ7	O
T7	DCD1J	I
U5	DCD2J	I
T6	DENSEL	O
C6	DEVSELJ	I/O
P5	DIRJ	O
L18	DOCKJ	I
F18	DREQ0	I
V17	DREQ1	I
V12	DREQ2	I
W16	DREQ3	I
E18	DREQ5	I
C20	DREQ6	I
B19	DREQ7	I
R5	DRV0J	O
T4	DRV1J	O
T3	DSKCHGJ	I/O
U6	DSR1J	I
Y3	DSR2J	I
V6	DTR1J	O
V4	DTR2J	O
U10	ERRORJ	I
G20	FERRJ	I
B5	FRAMEJ	I/O
J10	GND	P
J11	GND	P
J12	GND	P
J9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K9	GND	P
L10	GND	P
L11	GND	P

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Pin No.	Pin Name	Type
L12	GND	P
L9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M9	GND	P
U2	HDSELJ	O
J19	IGNNEJ	O
U4	INDEXJ	I
G18	INIT	O
V10	INITJ	O
E4	INTAJ_MI	I
E5	INTBJS0	I/O
E6	INTCJS1	I/O
F4	INTDJS2	I/O
H20	INTR	O
P17	IO16J	I
Y10	IOCHKJ	I
Y14	IOCHRDY	I/O
V15	IORJ	I/O
Y15	IOWJ	I/O
A5	IRDYJ	I/O
N18	IRQ10	I/O
N16	IRQ11	I/O
G17	IRQ14	I/O
H17	IRQ15	I/O
U16	IRQ3	I/O
U20	IRQ4	I/O
U17	IRQ5	I/O
V19	IRQ6	I/O
W20	IRQ7	I/O
L19	IRQ8J	I
V11	IRQ9	I/O
U11	KBCLK	I/O
U12	KBDATA	I/O
F16	KBINH	I/O
F19	LA17	I/O
G16	LA18	I/O
H16	LA19	I/O
J16	LA20	I/O
M17	LA21	I/O
N17	LA22	I/O
P16	LA23	I/O
P19	M16J	I/O
F17	MEMRJ	I/O

Pin No.	Pin Name	Type
E19	MEMWJ	I/O
T5	MOT0J	O
R4	MOT1J	O
T11	MSCLK	O
T12	MSDATA	I/O
H19	NMI	O
V13	NOWSJ	I
K17	OFF_PWR1	O
L17	OFF_PWR2	O
P20	OSC14M	I
N20	OSC32KI	I
N19	OSC32KII	I
C12	OVCRJ	I
D7	PAR	I/O
C11	PCI_STPJ	O
E8	PCICLK	I
A12	PCIREQJ	I
E7	PCIRSTJ	O
D15	PCSJ	I/O
V7	PD0	I/O
W7	PD1	I/O
Y7	PD2	I/O
T8	PD3	I/O
U8	PD4	I/O
V8	PD5	I/O
W8	PD6	I/O
Y8	PD7	I/O
V9	PE	I
B11	PHLDAJ	I
A11	PHOLDJ	O
F1	PIDEA0	O
F2	PIDEA1	O
E3	PIDEA2	O
E2	PIDECS1J	O
E1	PIDECS3J	O
G5	PIDED0	I/O
H2	PIDED1	I/O
J4	PIDED10	I/O
J2	PIDED11	I/O
H5	PIDED12	I/O
H3	PIDED13	I/O
H1	PIDED14	I/O
G4	PIDED15	I/O
H4	PIDED2	I/O
J1	PIDED3	I/O

Pin No.	Pin Name	Type
J3	PIDED4	I/O
J5	PIDED5	I/O
K2	PIDED6	I/O
K4	PIDED7	I/O
K3	PIDED8	I/O
K1	PIDED9	I/O
F3	PIDEDAKJ	O
G3	PIDEDRQ	I
G1	PIDEIORJ	O
G2	PIDEIOWJ	O
F5	PIDERDY	I
M20	PWG	I
L20	PWRBTNJ	I
U3	RDATAJ	I
Y19	REFRSHJ	I
M18	RI	I
V5	RI1J	I
Y1	RI2J	I
A15	ROMKBCSJ	O
K18	RSMRSTJ	I
T10	RSTDRV	O
C14	RTCAS	O
A14	RTCDS	O
B14	RTCRW	O
Y5	RTS1J	O
W3	RTS2J	O
R18	SA0	I/O
R19	SA1	I/O
V18	SA10	I/O
W19	SA11	I/O
Y20	SA12	I/O
Y18	SA13	I/O
W17	SA14	I/O
V16	SA15	I/O
Y16	SA16	I/O
U15	SA17	I/O
W15	SA18	I/O
T14	SA19	I/O
R20	SA2	I/O
T18	SA3	I/O
T19	SA4	I/O
T20	SA5	I/O
T17	SA6	I/O
U19	SA7	I/O
U18	SA8	I/O

Pin No.	Pin Name	Type
V20	SA9	I/O
P18	SBHEJ	I/O
T13	SD0	I/O
U13	SD1	I/O
C19	SD10	I/O
B20	SD11	I/O
B18	SD12	I/O
A20	SD13	I/O
A19	SD14	I/O
A18	SD15	I/O
W13	SD2	I/O
Y13	SD3	I/O
W12	SD4	I/O
Y12	SD5	I/O
W11	SD6	I/O
Y11	SD7	I/O
D20	SD8	I/O
D18	SD9	I/O
D16	SERIRQ	I/O
A6	SERRJ	I
L3	SIDEA0	O
L4	SIDEA1	O
L2	SIDEA2	O
L1	SIDECS1J	O
K5	SIDECS3J	O
N1	SIDED0	I/O
N3	SIDED1	I/O
R1	SIDED10	I/O
P3	SIDED11	I/O
P1	SIDED12	I/O
N4	SIDED13	I/O
N2	SIDED14	I/O
M5	SIDED15	I/O
N5	SIDED2	I/O
P2	SIDED3	I/O
P4	SIDED4	I/O
R2	SIDED5	I/O
T1	SIDED6	I/O
U1	SIDED7	I/O
T2	SIDED8	I/O
R3	SIDED9	I/O
L5	SIDEDAKJ	O
M4	SIDEDRQ	I
M2	SIDEIORJ	O
M3	SIDEIOWJ	O

Pin No.	Pin Name	Type
M1	SIDERDY	I
Y6	SIN1	I
Y4	SIN2	I
D12	SIRQI	I
E13	SIRQII	I
W9	SLCT	I
W10	SLCTINJ	O
J17	SLEEPJ	O
M16	SMBCLK	I/O
L16	SMBDATA	I/O
U14	SMEMRJ	O
W14	SMEMWJ	O
H18	SMIJ	O
W6	SOUT1	I/O
W4	SOUT2	O
D17	SPKR	O
E17	SPLED	O
E15	SQWO	O
W2	STEPJ	O
B6	STOPJ	I/O
J18	STPCLKJ	O
U7	STROBJ	O
K19	SUSTAT1J	O
W18	SYSCLK	O
R17	TC	O
E16	THRMJ	I
D6	TRDYJ	I/O
V2	TRK0J	I
B12	USBCLK	I
B13	USBP0+	I/O
C13	USBP0-	I/O
E12	USBP1+	I/O
A13	USBP1-	I/O
R14	VCC_3A	P
G15	VCC_3C	P
F14	VCC_A	P
G6	VCC_A	P
P6	VCC_A	P
R15	VCC_A	P
R7	VCC_A	P
F6	VCC_B	P
P15	VCC_C	P
F15	VCC_E	P
R6	VDD_5	P
N15	VDD_5S	P

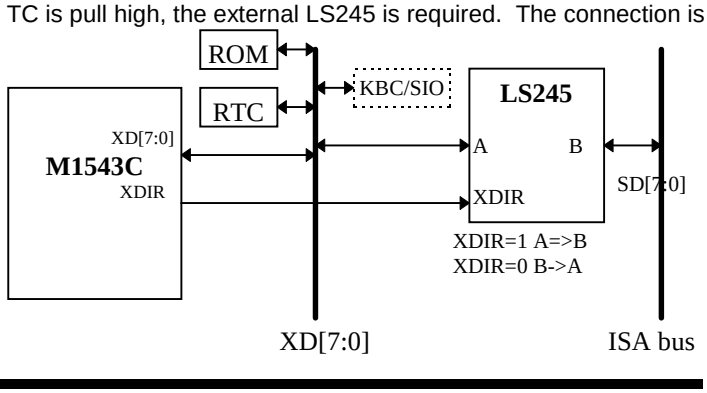
Pin No.	Pin Name	Type
W1	WDATAJ	O
V3	WGATEJ	O
V1	WPROTJ	I
B15	XD0	I/O
C15	XD1	I/O
A16	XD2	I/O
B16	XD3	I/O
C16	XD4	I/O
A17	XD5	I/O
B17	XD6	I/O
C17	XD7	I/O
D14	XDIR	I/O
K16	ZZ	O

2.5 Hardware Setting Description :

Pin No.	Pin Name	Setup, Configuration
D15	PCSJ	Pull-low, Hotkey function enable. Pull-high, Hotkey function disable. Please refer to section 1.4, 5.4 for more detailed information.
A11	XPHOLDJ	Pull-low, USB in test mode. (for test only) Pull-high, USB in normal mode. In normal operation, this pin must be pulled high.
E17	SPLED	Pull-low, supports 256KB ROM. Pull-high, supports 128KB ROM. This pin is pulled high to support 128KB ROM. There are two solutions for the 256KB(2Mbits) ROM connection : (a) When pin SPLED is pull-low, the 256KB(2Mbits) ROM option is supported. The BIOSA17 and BIOSA16 pins are used to control the 2Mbits ROM A17 and A16 pins respectively. BIOS will use one F region and three E regions to read/write the 2-Mbit ROM. (b) Second solution is pull-high pin SPLED (as 128Kbytes(1Mbits) option) and pin BIOSA17/GPO[19] is used as GPO[19] to control 2Mbits ROM A17 and ISA SA[16] is used to control 2Mbits ROM A16, i.e., BIOS will use two F regions and two E regions to program the 2-Mbit flash ROM.
D14	XDIR	Pull-low, Pentium II CPU is used. Pull-high, Pentium CPU is used. This pin setting will affect INIT active level (Pentium: Active High, Pentium II: Active Low), and the pin SLEEPJ/GPO[20] function selection (Pentium II: SLEEPJ, Pentium: GPO[20]).
R17	TC	Pull-low, pins SD[7:0]/GPIO[7:0] are SD[7:0], external LS245 is not required. Pull-high, pins SD[7:0]/GPIO[7:0] are GPIO[7:0], external LS245 is required. Please refer to section 1.4 for more detailed information.
D17	SPKR	Pull-low, internal Super I/O test mode enabled. (for test only) Pull-high, internal Super I/O test mode disabled. In normal operation, this pin must be pulled high.
A15	ROMKBCSJ	Pull-low, chip test mode is enabled. (for test only) Pull-high, chip test mode is disabled. In normal operation, this pin must be pulled high.
K20	ACPWR	Pull-low, AT power mode. Pull-high, ATX power mode. In AT power mode, M1543C will enable the power on sequence when the power comes in. But in ATX power mode, M1543C will enter Soft-Off mode when the ATX Standby power comes in for the first time, and then enable the power on sequence after the Power Button is pushed. This pin has a 40K internal pull-low resistor.
M19	CLK32KO	Pull-low, 32K Clock test mode is disabled. Pull-high, 32K Clock test mode. (for test only) This pin is used as 32K Clock test mode when it is pulled high. In normal operation, it must not be pulled high. This pin has a 40K internal pull-low resistor.
Y5	RTS1J	Pull-low, 0x370h. Pull-high, 0x3F0h. This pin is used to define the configuration register's base address. If it is pulled high, 3F0h is selected. If it is pulled low, 370h is selected. This pin has a 20K internal pull-up resistor.
W3	RTS2J	Pull-low, internal keyboard disable. Pull-high, internal keyboard enable. This input is used to enable KBC after reset. The enable can be overwritten by configuration register. This pin has a 20K internal pull-up resistor.
V4	DTR2J	Pull-low, internal keyboard is AT mode. Pull-high, internal keyboard is PS2 mode. This input is used to define the KBC is PS/2 or AT mode. This pin has a 20K internal pull-up resistor.

2.6 XDIR Control

When pin TC is pull high, the external LS245 is required. The connection is :



1) PCI I/O Read ISA : XDIR=0
2) PCI I/O Write ISA : XDIR=1
3) PCI Memory Read ISA : XDIR=0
4) PCI Memory Write ISA : XDIR=1
5) PCI access XD bus device (RTC,ROM,KBC) : XDIR =1
6) ISA Refresh : XDIR =1
7) ISA/DMA master MR/IOW : XDIR=1
8) ISA/DMA master MW/IOR : XDIR=0

2.7 GPIO Pins List Table

The following table shows the list of the GPIO pins :

NAME	MUX with Pin	How to enable	Suggestion/Comment
GPI0	OVCRJ	M1543C Register Index-59h, bit 0='1'	Drive high before enable.
GPI2	SERIRQ	M1543C Register Index-59h, bit 2='0'	
GPI3	PCIREQJ	M1543C Register Index-59h, bit 3='1'	Drive high before enable.
GPI9	KBCLK/LA[21]	RTS2J pull low	Disable internal keyboard. (No matter PCSJ pull low/high)
GPI10	KBDATA/IRQ[10]	RTS2J pull low	Disable internal keyboard. (No matter PCSJ pull low/high)
GPI11	MSCLK	RTS2J pull low	Disable internal keyboard.
GPO0	PCSJ	M1543C Register Index-5Ah, bit 0='1'	Output '1' before enable.
GPO1	ZZ	M1543C Register Index-5Ah, bit 1='1'	Output '0' before enable.
GPO2	CPU_STPJ	M1543C Register Index-5Ah, bit 2='1'	Output '1' before enable.
GPO3	PCI_STPJ	M1543C Register Index-5Ah, bit 3='1'	Output '1' before enable.
GPO9	SQWO/GPIOW	M1543C Register Index-5Ah, bit 9='1'	Output '0' before enable.
GPO12	XDIR	TC pull low	External LS245 is not required.
GPO18	BIOSA16	SPLED pull high	Not support 256KB ROM.
GPO19	BIOSA17	SPLED pull high	Not support 256KB ROM.
GPO20	SLEEPJ	XDIR pull high	Pentium is used. (not Pentium-II)
GPO22	OFF_PWR1	M7101 Register Index-C6h, bit 1='1'	Drive low before enable.
GPO23	OFF_PWR2	M7101 Register Index-C6h, bit 2='1'	Drive low before enable.
GPIO0/ IRTX	SD0	TC pull high and M1543C Register Index - 6Dh, bit4='0'/'1'	External LS245 should be used.
GPIO1/ IRRXH	SD1	TC pull high and M1543C Register Index - 6Dh, bit4='0'/'1'	External LS245 should be used.
GPIO2/ IRRX	SD2	TC pull high and M1543C Register Index - 6Dh, bit4='0'/'1'	External LS245 should be used.
GPIO3/ CVROFF	SD3	TC pull high and M1543C Register Index - 6Dh, bit4='0'/'1'	External LS245 should be used.
GPIO4/ USBP2+	SD4	TC pull high and M5237 Register Index - 40h, bit26='0'/'1'	External LS245 should be used.
GPIO5/ USBP2-	SD5	TC pull high and M5237 Register Index - 40h, bit26='0'/'1'	External LS245 should be used.
GPIO6/ Reserved	SD6	TC pull high and M1543C Register Index - 72h, bit6='0'/'1'	External LS245 should be used.
GPIO7/ PWR_EN	SD7	TC pull high and M1543C Register Index - 72h, bit6='0'/'1'	External LS245 should be used.
EGPI15-0		The input level can be read from M7101 Register Index-0BAh-0BBh.	Add two LS244s to drive SD[15:8] and XD[7:0] when XREFRESHJ is asserted.
EGPO15-0		M1543C Register Index-5Ah, bits [9:8]="01". The output level is controlled by M7101 Register Index-0B8h-0B9h.	Add two LS373s to latch the data of SD[15:8] and XD[7:0], and use GPIOW to be the latch signal.

Note :
1. All GPO defaults drive low after enable (except GPO19).
2. All GPIO defaults are inputs after enable.
3. All GPI must connect to fixed value if it is not used in motherboard implementation. System designer must avoid GPI pin in floating state.
4. The comment “drive high/low before enable” is caused by the default function. For example, GPI0/OVCRJ[0] is OVCRJ[0] after reset. But it is not necessary to do if you switch it to GPI0 at booting.
5. All default values can be found at registers of “how to enable” or at ’33 Cfg 54h for hardware setting pins.
6. All GPI/GPO/GPIO pins are 5V tolerance.

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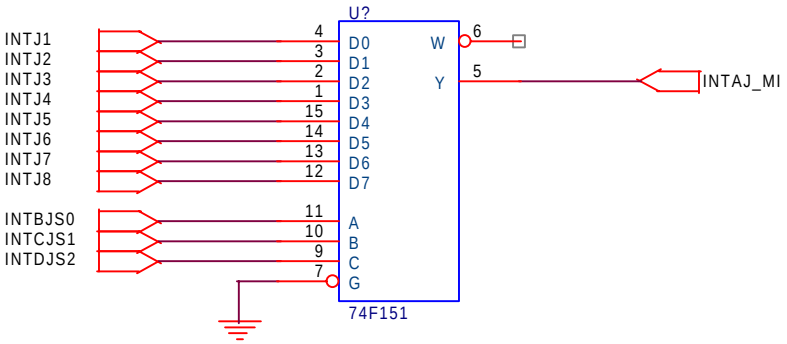
2.8 PCI Interrupt Polling Hardware Implementation



PCI Interrupt Polling mode is enabled by setting M1543C Register Index 45h bit7 to 1. The polling clock is selected by M1543C Register Index 57h-55h bit20. There are two options for the clock : PCICLK (bit20 = 0) or OSC14M (bit20 = 1). 74F151 is needed when PCICLK is selected. Otherwise, 74LS151 is enough. Also, M1543C Registers Index 4Bh-48h are used to decide the Routing table for INTJ8-INTAJ1.

Section 3 : Function Description

3.1 PCI Command Set

The command types M1543C supports in Slave mode are Interrupt Acknowledge, Special cycle, I/O read, I/O write, memory read, memory write, configuration read and configuration write and other multiple memory read/write cycles.

M1543C PCI Cycle Description

CBEJ	Command Type	as Target	as Initiator
0000	Interrupt	Yes	No
0001	Special Cycle	Yes - Note.1	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes - Note.2	No
1101	Reserved	No	No
1110	Memory Read line	Yes - Note.2	No
1111	Memory Write and Invalidate	Yes - Note.3	No

Note 1 : The M1543C only decodes Stop Grant special cycle, and Halt special cycle and Shutdown special cycle. All other special cycles are ignored.
Note 2 : Treated as Memory read
Note 3 : Treated as Memory write

3.2 PCI Slave Description

As a PCI slave, the M1543C will assert DEVSELJ signal to indicate it is the target of the PCI transaction. DEVSELJ is asserted when the M1543C positively or subtractively decodes the PCI transaction. The configuration cycle, USB programming cycle and IDE I/O cycle are positively decoded. The timer and interrupt controller programming cycles are positively or subtractively decoded via register setting. All others are subtractively decoded except for docking mode. All cycles will be positively decoded in docking mode. These cycles include PCI to ISA slave cycles. Under docking mode, M1543C only supports positive decode.

A 32-bit posted write buffer is embedded to support PCI-to-ISA memory write cycles and delay transaction cycle. Multiple read/write transactions are not supported. Hence, any burst cycles decoded by the M1543C will be terminated by disconnecting semantics after the first data transaction has been completed. The M1543C will retry any PCI initiated cycle when its internal buffer cycle is still active.

M1543C supports delay transaction and discard counter in compliance with PCI specification 2.1.

3.2.1 Posted Write Buffer

The PCI-to-ISA memory write cycles will be posted into the write buffer when it is enabled, and the buffer is scheduled to be written to the ISA bus. Any subsequent PCI cycles to the M1543C will be retried until the posted write buffer is empty. The buffer also optionally supports data I/O posted write cycle for sound cards.

The posted write buffer must be flushed and disabled before an ISA/DMA master owns the ISA and PCI bus. This rule eliminates the possibility of a deadlock caused by a committed ISA cycle.

3.3 PCI Master

3.3.1 M1543C as PCI Master

The M1543C will assert a master abort due to DEVSELJ timeout. The M1543C acts as a PCI Master when an ISA or DMA master accesses the PCI memory. The M1543C provides an 8-byte bi-directional line buffer for ISA/DMA Master memory read from or write to PCI bus. The line buffer is used to isolate the ISA bus' slower devices from the PCI. Only an ISA/DMA master memory write or read cycle to PCI bus can be assembled/disassembled into line buffer. When line buffer is enabled, the ISA/DMA master can prefetch 2 Doublewords to the line buffer for read cycle. However, only 4 bytes are used in the buffer for write cycle.

In some cases, a strong ordering must be kept due to coherency problems, the line buffer will be disabled. When the line buffer is disabled, the reorder problem caused by assembly/disassembly will be avoided and guarantees read/write ordering.

3.3.2 Posted - Write Buffer Flush

Once an ISA/ DMA master begins a cycle on the ISA bus, the cycle cannot be backed off. It can only be held in wait states via IOCHRDY. In order to avoid deadlock situations, the PCI to ISA post write buffer needs to be flushed before an ISA/ DMA master gets the ISA bus. When the ISA/DMA master owns the ISA bus, the PCI to ISA post write buffer will be disabled.

3.3.3 Line Buffer Management

When an ISA/DMA master reads from PCI memory, the M1543C prefetches 8 bytes of data into the line buffer. If there is a read "hit" from the line buffer, the "hit" bytes are marked as invalid. There are 3 conditions why the line buffer needs prefetching :

1. Line buffer is "Empty" when read.
2. Read "Miss" to the line buffer.
3. Read the invalid byte from the line buffer.

When ISA/DMA master writes to PCI memory, the M1543C writes data to the line buffer. When the 4-byte buffer is full, it flushes data to the PCI bus. There are five conditions which the line buffer must flush its data :

1. Line buffer is full. Flush the line buffer and mark empty.
2. Write "Miss" to the partially full 4-byte line. Flush the partially full line and mark as empty, then write to the empty line.
3. Write "Hit" to the valid bytes. Flush it and mark as empty, then write to the empty line.
4. Read after write transaction and the line buffer is partially full. Flush the line buffer then do read prefetch.
5. Master has changed on DACKJ going inactive and last transaction is write and line buffer is partially full. Flush the line buffer.

3.4 Parity Support

As a master, the M1543C will generate address parity for read/write cycles, and data parity for write cycles. Parity check will work at read cycle. As a target, the M1543C will generate data parity for read cycles. PAR is even parity across AD[31:0] and CBEJ[3:0]. Even parity means that the number of 1's within the 36 bits and PAR is even. PAR has the same timing as AD[31:0] but delayed by one clock.

3.5 Address decoding

M1543C address decoding includes the following :

a. Positively decodes configuration cycle.
b. Positively or subtractively decodes interrupt acknowledge cycle. It is controlled by M1543C register Index-44h bit[6]. Value 0 is for Positive decode, Value 1 is for Subtractive decode.
c. Positively decodes on-chip IDE access cycle.
d. Positively decodes on-chip USB access cycle.
e. Positively or subtractively decodes internal I/O cycle (interrupt controller 8259, timer counter 8254, ACPI I/O Port, SMB I/O Port, APM I/O Port). It is controlled by M1543C register Index-44h bit[6]. Value 0 is for Positively decode, Value 1 is for Subtractively decode.
f. Subtractively decodes DMA (8237) controller internal registers.
g. Others are subtractive decode.
h. When M1543C is programmed to be docking mode (M1543C register Index-5Ch bit0=1), all cycles are positively decoded including ISA-destinated cycles.

3.6 IDE Master Controller (M5229)

a. Supports PCI bus mastering, transfer rate up to 132 Mbytes/sec. This significantly lightens the load of CPU work burden.
b. Supports IDE PIO modes 0, 1, 2, 3, 4 ~~& 5~~ timing and multiword DMA modes 0,1,2 on enhanced IDE specifications. This chip is capable of accelerating PIO data transfers as well as acting as a PCI bus master ~~on behalf of an IDE DMA slave device~~. The M1543C provides an interface for two dedicated IDE connectors.
c. Supports compatible and native PCI mode. Compatible mode is the default mode, native PCI mode will only be chosen by the BIOS.
d. 16 Doubleword FIFOs for posted-write or read-ahead buffer for each channel (Total = 32 Doublewords). Each channel buffer is independent and concurrent.
e. Programmable command and data transfer timing per drive for maximum flexibility. Operation of two hard disks is possible even if they have different PIO modes.
f. Supports concurrent operation on two ATA channels. M1543C simultaneously operates two drives.
g. Supports ATAPI CD-ROM concurrent operation. Simultaneous use of hard disks and CD-ROM is possible.
h. Dedicated ATA bus pins and dedicated buffers for each channel, no extra TTLs are needed.
i. Supports Ultra 33 high performance ATA bus for 33 Mbytes transfer rate.

3.7 Distributed DMA

The Distributed DMA Host Controller supported by M1543C provides one way to allow the separation of the slave DMA controllers in the hardware architecture, and yet allows the OS and application base to still utilize two legacy DMA controllers.

3.8 Serialized IRQ

The serialized IRQ supported by M1543C provides one pin named SERIRQ to generate IRQs event to Interrupt Controller from serialized IRQ protocol. The frame number can be programmed from 17 to 32. The Operation mode (quiet or continuous) and Start Frame Pulse width (4 to 8 pciclks) are also programmable.

3.9 Advanced Power Management (M7101)

The M1543C Power Management Unit includes full ACPI compliance spec. and legacy power management including SMM, Stop clock control unit, APM, External SMI-switch control, Programmable counters for time-out event generation. M1543C can provide On (working)/ Sleeping (Power_on_suspend)/ Suspend_to_DRAM/ Suspend_to_Disk/ Soft_Off/ Mechanical_Off global system states to minimize the overall system power consumption. M1543C also provides an extra Standby state for monitoring over 16 peripheral devices activity. M1543C supports programmable Stop_Clock with throttle/ CLK_ON_STPCLK/CLK_OFF_STPCLK control for fitting the ACPI C0-C3 clock states. M1543C provides several hot plugging events detection and multiple external wake-up events for satisfying the notebook requirements. M1543C supports the battery, thermal detected logic and system/chip/devices power plane management logic. The M1543C provides full support for Advanced Configuration and Power Interface (ACPI), On-now technology and OS Directed Power Management (OSPM). M1543C also supports the legacy power management control, such as SMM and SMI features. For the most appealing modern motherboard design for hardware monitoring, M1543C can extend 16 GPI signals and 16 GPO signals. The goal of the M1543C power management not only targets to the current desktop/ notebook satisfaction but also to the future OS driven flexible requirements.

3.10 System Management Bus (SMBus)

The M1543C SMBus has been designed based on :
System Management Bus Specification Rev 1.0
Smart Battery Data Specification Rev 1.0
Smart Battery Charger Specification Rev 1.0
System Management Bus BIOS Specification Rev 1.0
Smart Battery Selector Specification Rev 0.9

The System Management Bus (SMBus) host controller in M1543C supports the ability to communicate with power-related devices by SMBus protocol. It can be a master or slave on the SMBus, providing quick send byte/receive byte/ write byte/write word/read word/block read/block write command with clock synchronization and arbitration functions.

3.11 Universal Serial Bus (USB) (M5237)

The M1543C USB is an implementation of the Universal Serial Bus (USB) 1.0 specification which contains PCI interface logic, Host Controller and an integrated Root Hub with three USB ports. For DOS compatibility, Keyboard and Mouse legacy are also supported. For the best AGP system implementation, M1543C supports 3 USB ports. One port can be used for AGP, and the other two ports can support the external connections. Unlike other chipset solutions, only two ports are supported. If one is used for AGP, there is only one left for external connection.

3.12 Super I/O

The M1543C Enhanced Super I/O Controller incorporates the following functions :

- Three full-function universal asynchronous receiver/ transmitters (UARTs)
- Keyboard interface with Hotkey function
- Floppy disk controller (FDC) with digital data separator
- Parallel port
- Standard XT/AT address decoding for on-chip functions
- One high speed Infrared wireless communication port
- Configuration register

With these functions the M1543C offers a single-chip solution to the most common IBM PC, XT, AT and Notebook peripherals.

M1543C supports the Hotkey function in the keyboard. Users can define the special function key to make the system entering or leaving different operation mode, for example, put the system into sleep or wake up the system, even force the system into Soft-Off mode.

The floppy disk controller is fully compatible with the industry-standard 765A and 82077SL architecture. It includes more advanced options such as a high performance data separator with send/receive 16 bytes FIFOs, implied seek command, scan command, and supports both IBM and ISO 360K/1.2M/720K/1.44M/2.88M FDD formats. The UARTs are compatible with the NS ~~16450 and~~ 16550 with send/receive 16 bytes FIFOs and a programmable baud rate generator. For the complete system architecture and specification, M1543C has the dedicated pins and COM port for the IR support, which means, the motherboard still can support two serial ports outside and have the IR support at the same time. The wireless communications supported by M1543C includes IrDA 1.0 (SIR), IrDA 1.1 (MIR and FIR), and Sharp-IR. The parallel port is fully compatible with the IBM AT as well as EPP and ECP. The configuration register is one-byte wide and can be programmed via hardware or software. By controlling this register, the user can assign standard AT addresses and disable any major on-chip function (e.g., the FDC, either UART, or the parallel port) independent of the others. This allows for flexibility in system configuration when adapter boards contain duplicate functions.

The M1543C is designed for PC98 to provide the functionality recommended to support Windows 95. Through internal configuration registers, each of the logic device I/O address, DMA channel and IRQ are programmable. There are 128 I/O address location options, 12 IRQ options, and three DMA channel options for each logical device except KBC. The KBC I/O address are not routable.