M1543: Desktop South Bridge

Section 1: Introduction

1.1 Features

- **Provides a bridge (with Super I/O) between the PCI bus and ISA bus for both Pentium and Pentium Pro systems**
- **PCI interface**
  - Supports PCI Master and Slave Interface
  - Supports PCI Master and Slave Initiated Termination
  - PCI spec. 2.1 Compliant (Delayed Transaction Support)
- **Buffers Control**
  - 8-byte Bi-directional Line Buffers for DMA/ISA Memory Read/Write Cycles to PCI Bus.
  - 32-bit Posted Write Buffer for PCI Memory Write and I/O Data Write (for Sound Card) to ISA bus.
- **Provides steerable PCI interrupts for PCI device Plug-and-Play**
  - Up to 8 PCI Interrupts Routing
  - Level to Edge Trigger Transfer
- **Enhanced DMA Controller**
  - Provides 7 Programmable Channels, 4 for 8-bit Data Size, 3 for 16-bit Data Size
  - 32-bit Addressability
  - Provides Compatible DMA Transfers
  - Provides Type F Transfers
- **Interrupt Controller**
  - Provides 14 Interrupt Channels
  - Independent Programmable Level/Edge Triggered Channels
- **Counter/Timers**
  - Provides 8254 Compatible Timers for System Timer, Refresh Request, Speaker Output Use
- **Distributed DMA Supported**
  - 7 DMA Channels can be Arbitrarily Programmed as Distributed Channel
- **Serialized IRQ Supported**
  - Quiet/Continuous Mode
  - Programmable (Default 21) IRQ/DATA Frames
  - Programmable START Frame Pulse Width
- **Plug-and-Play Supported**
  - 1 Programmable Chip Select
  - 2 Steerable Interrupt Request Lines
- **Built-in Keyboard Controller**
  - Built-in PS2/AT Keyboard and PS2 Mouse Controller
- **Supports up to 256 KB ROM Size Decoding**
- **Supports Positive/Subtractive Decode for ISA Device**
- **PMU Features**
  - Full Support for ACPI and OS Directed Power Management
  - CPU SMM Legacy Mode and SMI Feature Supported
  - Supports Programmable STPCLKJ : Throttle/CKONSTP/CKOFFSTP Control
  - Supports I/O Trap for I/O Restart Feature
  - PMU Operation States :
    - ON
    - Standby
    - Sleep (Power On Suspend)
    - Suspend (Suspend to DRAM)
    - Suspend to HDD
    - Soft-Off
    - Mechanical Off
  - APM State Detection and Control Logic Supported
  - Global and Local Device Power Control Logic
  - 8 Programmable Timers : Standby/ APMA/ Global_Display
  - Provides System Activity and Display Activity Monitorings, including
    - Video
    - Audio
    - Hard Disk
    - Floppy Disk
    - Serial Ports
    - Parallel Port
    - Keyboard
    - 1 Programmable I/O Group
    - 1 Programmable Memory Space

- Provides Hot Plugging Events Detection
  - AC Power
  - Docking Insert
- Multiple External Wakeup Events of Standby Mode
  - Power Button
  - Modem Ring
  - RTC alarm
  - DRQ2

- Suspend Wakeup Detected
  - Modem Ring
  - RTC alarm
  - Docking insert
  - Power Button
  - USB events
  - IRQ
  - ACPWR
- Thermal Alarm Supported
- Clock Generator Control Logic Supported
  - CPUCLK Stop Control
  - PCICLK Stop Control
- L2 Cache Power Down Control Logic Supported
- 6 General Purpose Input Signals, 10 General Purpose Output Signals.
- All Registers Readable/Restorable for Proper Resume from Suspend State

■ **Built-in PCI IDE Controller**
- Supports Ultra 33 Synchronous DMA Mode Transfers up to Mode 2 Timing (33 Mbytes/sec)
- Supports PIO Modes up to Mode 5 Timings, and Multiword DMA Mode 0,1,2 with Independent Timing of up to 4 Drives
- Integrated 10 x 32-bit Read Ahead & Posted Write Buffers for each channel (Total : 20 DWords)
- Dedicated Pins of ATA Interface for each channel
- Supports Tri-state IDE Signals for Swap Bay

■ **USB interface**
- One Root Hub with two USB ports based on OpenHCI 1.0a Specification
- Supports FS (12Mbits/sec) and LS (1.5Mbits/sec) Serial Transfer
- Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse

■ **Super I/O interface**
- Supports Windows 95 Plug-and-Play
- Supports 2 serial/ 1 parallel/ FDC functions
- 2.88 MB (formatted) Floppy Disk Controller
  - Software compatible with 82077 and supports 16-byte data FIFOs
  - High performance internal data separator
  - Supports standard 1 Mbps/ 500 Kbps/ 300 Kbps/ 250 Kbps data transfer rate
  - Supports 3 modes of 3.5“ FDD (720K/1.2M/ 1.44MB)
  - Swappable drives A and B
- Various mode Parallel Port
- Supports ECP/ EPP / PS/2 / SPP and 1284 Compliance
  - Standard mode
  - IBM PC/XT, PC/AT and PS/2 compatible Bi-directional parallel port
  - Enhanced mode
  - Enhanced Parallel Port (EPP) compatible
  - High speed mode
  - Microsoft and Hewlett Packard Extended Capabilities Port (ECP) compatible
  - includes protection circuit against damage caused when printer is powered up, or operated at higher voltages
- Serial ports
  - Two high performance 16550 compatible UARTs with send/receive 16-byte FIFOs
  - Programmable Baud Rate Generator
  - Serial Infra Red (SIR) from UART1, UART2 for wireless communications
  - MIDI (Musical Instrument Digital Interface) compatible
  - High performance Power Management for FDC, UART and Parallel Port
  - Option between 96 I/O addresses, 12 IRQs, and 3 DMA channels for each device

■ **SMBus Interface**
- System Management Bus Interface meets the V1.0 Specification

■ **328-pin (27mmx27mm) BGA Package**

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1.2 Functions

The M1543 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. The M1543 has Integrated Super I/O(Floppy Disk Controller, 2 serial ports/1 parallel port), System Peripherals (ISP) (2 x 82C59 and Serial interrupt, 1 x 82C54), advanced features (Type F and Distributed DMA) in the DMA controller (2 X 82C37), PS2 Keyboard/Mouse controller, 2-channel dedicated IDE Master Controller with Ultra-33 specification, System Management Bus (SMB), and 2 OpenHCI 1.0a USB ports. The ACPI (Advanced Configuration and Power Interface) and PCI 2.1 (Delayed Transaction) specification have also been implemented. M1543 also supports the deep flexible green function and provides the best solution for the best green system. It can connect to the ALi Pentium North Bridge (M1521/M1531/M1541) and also the ALi Pentium Pro North Bridge (M1615) to provide the best system solution.

One eight byte bi-directional line buffer is provided for ISA/DMA Master memory read/writes. One 32-bit wide posted write buffer is provided for PCI memory write & I/O write (for Audio) cycles to the ISA bus. M1543 also provides a PCI to ISA IRQ routing table, and level to edge trigger transfer.

The chip provides 2 extra IRQ lines and 1 programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts.

The on-chip IDE controller supports two separate IDE connectors for up to 4 IDE devices providing an interface for IDE hard disks and CD ROMs. The Ultra 33 specification (which supports the 33M bytes per second transfer rate) has been implemented in this IDE controller. The ATA bus pins & the Buffer (Read Ahead and Posted Write) are all dedicated for separate channel to improve the performance of IDE Master.

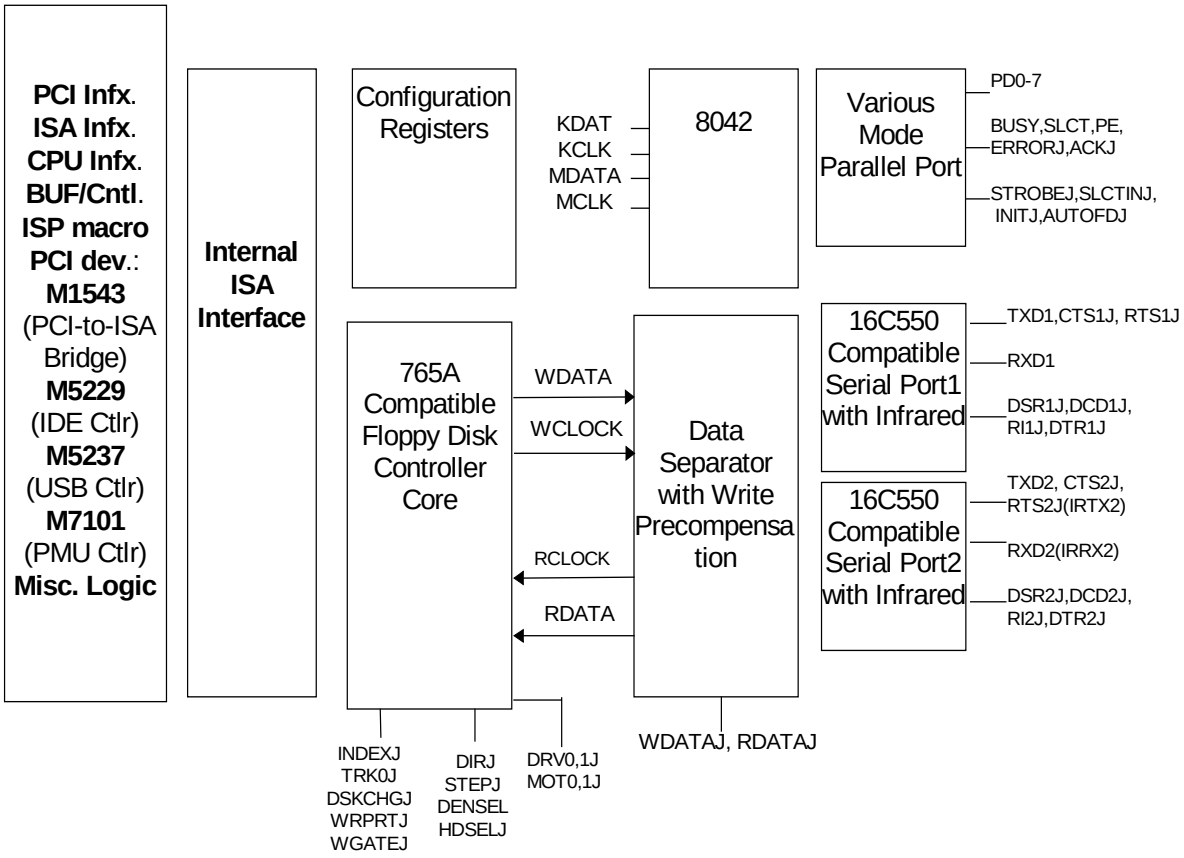
The M1543 supports Super Green for Intel and Intel compatible CPUs. It implements SMI or SCI (System Controller Interrupt) to meet the ACPI specification. It also meets the requirement for Microsoft's OnNow Design Initiative. The M1543 supports powerful power management for power saving including On, Standby, Sleeping, SoftOff, Mechanical Off state. To control the CPU power consumption, it provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control. Also, the M1543 can support the most flexible system clock design: it can be programmed to stop the CPU Clock, PCI Clock. The PBSRAM (Pipelined Burst SRAM) doze mode is also supported.

The built-in I/O in M1543 is an advanced Super I/O controller solution to basic IBM PC, XT, AT peripherals. It incorporates two full function universal asynchronous receiver/ transmitters (UARTs), a flexible high performance internal data separator with send/receive 16 byte FIFOs. It has Serial Infrared for wireless communications with other devices. It can swap your drives A & B. It features basic functions such as standard mode, enhanced mode, high speed mode. It supports SPP, PS/2, EPP and ECP parallel port. It also has a programmable baud rate generator. It has high performance power management for FDC, UART and parallel port.

The M1543 is a highly integrated chip including PS2 Keyboard/Mouse, SM Bus, 2 OpenHCI 1.0a USB ports, and the dedicated GPIO (General Purpose Input/Output) pins. The system designer can use this chip to implement the best green and cost/performance system.

1.3 M1543 Functional Block Diagram

M1543 Function Block Diagram



Section 2: Pin Description

2.1 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	AD21	AD20	AD19	AD16	IRDY J	SER RJ	AD14	AD10	AD6	AD1	PHLD J	GPI3	USB P1-	RTC DS	ROMK BCSJ	XD2	XD5	SD15	SD14	SD13
B	CBEJ 3	AD23	AD22	AD17	FRA MEJ	STO PJ	AD15	AD11	AD7	AD2	PHLD AJ	USB CLK	USB P0+	RTC RW	XD0	XD3	XD6	SD12	DRE Q7	SD11
C	AD26	AD25	AD24	AD18	CBEJ 2	**DEV SELJ**	CBEJ 1	AD12	CBEJ 0	AD3	GPO 3	GPI0	USB P0-	RTC AS	XD1	XD4	XD7	DAC KJ7	SD10	DRE Q6
D	AD29	AD28	AD27	AD30	AD31	TRDY J	PAR	AD13	AD8	AD4	GPO 2	SIRQ I	GPO 19	GPO 12	GPO 0	GPI2	SPK R	SD9	DAC KJ6	SD8
E	PIDE CS3	PIDE CS1	PIDE A2	INTA	INTB	INTC	PCI RSTJ	PCI CLK	AD9	AD5	AD0	USB P1+	SIRQ II	GPO 18	GPO 9	THR MJ	SPLE D	DRE Q5	MEM WJ	DAC KJ5
F	PIDE A0	PIDE A1	PIDE DAKJ	INTD	PIDE IRDY J	VCC _B				**M1543**				VCC _A	VCC _E	IRQ1I	MEM RJ	DRE Q0	LA17	DAC KJ0
G	PIDE RJ	PIDE WJ	PIDE DRQ	PIDE D15	PIDE D0	VCC _D									VCC 3C	LA18	IRQ 14	INIT	A20 MJ	IRQ 13
H	PIDE D14	PIDE D1	PIDE D13	PIDE D2	PIDE D12											LA19	IRQ 15	SMIJ	NMI	INTR
J	PIDE D3	PIDE D11	PIDE D4	PIDE D10	PIDE D5				GND	GND	GND	GND				LA20	GPO 20	STP CLK	IGN NEJ	CPU RST
K	**PIDE D9**	PIDE D6	PIDE D8	PIDE D7	SIDE CS3				GND	GND	GND	GND				GPO 1	GPO 22	RSM RSTJ	SUST AT1J	ACP WR
L	SIDE CS1	SIDE A2	SIDE A0	SIDE A1	SIDE DAKJ				GND	GND	GND	GND				SMB DATA	GPO 23	DOC KJ	IRQ8 J	PWR BTNJ
M	**SIDEI RDYJ**	SIDE RJ	SIDE WJ	SIDE DRQ	SIDE D15				GND	GND	GND	GND				SMB CLK	LA21	RI	OSC3 2KO	PWG
N	SIDE D0	SIDE D14	SIDE D1	SIDE D13	SIDE D2										VDD_ 5S	IRQ 11	LA22	IRQ 10	OSC 32II	OSC 32I
P	SIDE D12	SIDE D3	SIDE D11	SIDE D4	XDIR J	VCC _A_D									VCC _C	LA23	IO16	SBHE J	M16	OSC 14M
R	SIDE D10	SIDE D5	SIDE D9	XMO T1J	XDR V0J	VDD _5	VCC _A_D							VCC _3A	VCC _A	BALE	TC	SA0	SA1	SA2
T	SIDE D6	SIDE D8	XDSK CHGJ	XDR V1J	XMO T0J	XDE NSEL	XDC D1J	XPD3	XACK J	RST DRV	MS CLK	MS DATA	SD0	SA19	DAC KJ3	DAC KJ2	SA6	SA3	SA4	SA5
U	SIDE D7	XHD SELJ	XRDA TAJ	XIND EXJ	XDC D2J	XDS R1J	XSTR OBJ	XPD4	XBUS Y	XER RORJ	KB CLK	KB DATA	SD1	SME MRJ	SA17	IRQ3	IRQ5	SA8	SA7	IRQ4
V	XWP ROTJ	XTRK 0J	XWG ATEJ	XDTR 2J	XRI1J	XDTR 1J	XPD0	XPD5	XPE	XINIT J	IRQ9	DRE Q2	NOW SJ	AEN	IORJ	SA15	DRE Q1	SA10	IRQ6	SA9
W	XWD ATAJ	XSTE PJ	XRTS 2J	XSO UT2	XCTS 1J	XSO UT1	XPD1	XPD6	XSLC T	XSLC TINJ	SD6	SD4	SD2	SME MWJ	SA18	DRE Q3	SA14	SYS CLK	SA11	IRQ7
Y	XRI2J	XCTS 2J	XDSR 2J	XSIN 2	XRTS 1J	XSIN 1	XPD2	XPD7	XAUT OFDJ	IOCK	SD7	SD5	SD3	IOCH RDY	IOWJ	SA16	DAC KJ1	SA13	REFR SHJ	SA12

Figure 2-1. Pinout Diagram

Note: Please refer to p.199 for bottom view

2.2 Pin Description Table:

Pin Name	Type	Description
Clock & Reset Interface:		
PWG	I Group C Schmitt	**Power-Good Input.** This signal comes from the power supply to indicate that power is available and stable. The de-assertion of this input will enable the leakage control circuit between Soft-off (Suspend to Disk) resume circuit and no power circuit.
PCICLK	I Group B	**PCI Clock for Internal PCI Interface.** This is an input PCI clock, it should always be running at ON, STANDBY, SLEEP (Power-On Suspend) state. When CLKRUNJ is active, this clock should always be running. Internal PCI state machine and ISA state machine will use this clock.
OSC14M	I Group A	**14.318Mhz Clock Input.** This input clock will be used for Power Management timer, M8254 timer, SM Bus base frequency and ISA state machine.
OSC32KI	I Group C	**32 KHz Oscillator Input 1.** This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The M1543 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a Crystal is not used, an external 32 Khz clock input should be connected to this pin.
OSC32KII	I Group C	**32 KHz Oscillator Input2.** This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The M1543 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a Crystal is not used, this pin should be floated.
CLK32KO	O Group C 2.4/2.4 mA	**32 KHz Clock Output for DRAM Refresh.** At ON, STANDBY, SLEEP (Power On Suspend), SUSPEND (Suspend to DRAM) states, the output will send to Memory controller, to support DRAM refresh clock. At Soft off and Suspend to Disk states, the output will drive low to avoid leakage current.
USBCLK	I Group B	**48 MHz USB Clock Input.** This clock will send to USB state machine to generate USB signals.
PCI Bus Interface:		
PCIRSTJ	O-Group B 12/16 mA	**PCI Bus Reset.** This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.
AD[31:0]	I/O Group B 12/16 mA	**Address and Data Multiplexed Bus.** During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBEJ[3:0]	I/O-Group B 12/16 mA	**Bus Command and Byte Enable.** During address phase, CBEJ[3:0] define the Bus Command. During the data phase, CBEJ[3:0] define the Byte Enables.
FRAMEJ	I/O -Group B 12/16 mA	**Cycle Frame.** Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.
TRDYJ	I/O -Group B 12/16 mA	**Target Ready.** Target Ready indicates the target's ability to complete the current data phase of the transaction.
IRDYJ	I/O-Group B 12/16 mA	**Initiator Ready.** Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
STOPJ	I/O-Group B 12/16 mA	**Cycle Stop Request.** Cycle Stop indicates the target is requesting the master to stop the current transaction.
DEVSELJ	I/O Group B 12/16 mA	**Device Select.** This signal indicates that the target device has decoded the address as its own cycle. This pin is an output pin when M1543 acts as a PCI slave has decoded address as its own cycle including subtractive decoding.
SERRJ	I -Group B	**System Error.** This signal may be pulsed active by any agent that detects a system error condition. When SERRJ is sampling low, M1543 will assert NMI to generate non-maskable interrupt to CPU.
PAR	I/O Group B 12/16 mA	**Parity Signal.** PAR is an Even Parity and is calculated on AD[31:0] and CBEJ[3:0]. When M1543 acts as a PCI master, it drives PAR one PCI clock after address phase for read/write transaction and one PCI clock after data phase for write transaction. When the M1543 acts as a target, it drives PAR one PCI clock after data phase for PCI master read transaction.

Pin Description Table (continued):

Pin Name	Type	Description
PCI Bus Interface:		
PHLDAJ	I Group B	**PCI Bus Ownership Acknowledge.** When PCI bus arbiter asserts this pin, M1543 has owned the PCI bus.
PHOLDJ	O-Group B 4/4 mA	**PCI Bus Ownership Request.** M1543 requests the ownership of the PCI bus from the PCI bus arbiter on the North Bridge. M1543 will assert this signal on behalf of the ISA Master, DMA Device, IDE Master, and the USB Master.
INTAJ_MI	I Group B	**PCI INTA.** PCI interrupt input A or PCI interrupt polling input. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTAJ when 4 PCI Interrupts are supported, or connects to the 74F181 encoded output to support the 8 PCI Interrupts polling mode.
INTBJS0	I/O Group B Schmitt 4/4 mA	**PCI INTB.** PCI interrupt input B or polling select_0 output. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTBJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 0 to support the 8 PCI Interrupts polling mode.
INTCJS1	I/O Group B Schmitt 4/4 mA	**PCI INTC.** PCI interrupt input C or polling select_1 output. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTCJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 1 to support the 8 PCI Interrupts polling mode.
INTDJS2	I/O Group B Schmitt 4/4 mA	**PCI INTD.** PCI interrupt input D or polling select_2 output. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTDJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 2 to support the 8 PCI Interrupts polling mode.
CPU interface:		
INIT	O-Group E 2.4/2.4 mA	**CPU Initialize Interrupt.** CPU cold & warm reset. When CPU is Pentium Pro, this signal is low active. Otherwise, this signal is high active. When power on, KBC RC, port 92 RC, shutting down all will trigger INIT active.
CPURST	O-Group E 2.4/2.4 mA	**CPU Cold Reset.** When power turn on, this reset signal will be asserted, and then will become de-asserted until 4 ms after PWG becomes high.
IGNNEJ	O-Group E 2.4/2.4 mA	**Ignore Error.** This pin is used as the ignore numeric coprocessor error.
INTR	O-Group E 2.4/2.4 mA	**Interrupt Request to CPU.** This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt.
NMI	O Group E 2.4/2.4 mA	**Non-maskable Interrupt to CPU.** This is generated by the ISA Parity error (IOCHKJ assertion), PCI Parity error or DRAM Parity error (SERRJ assertion), and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt.
A20MJ	O-Group E 2.4/2.4 mA	**CPU A20 Mask.** This is the CPU Address line A20 mask signal.
FERRJ/ IRQ13	I Group E	**Floating Point Error.** FERRJ input to generate IRQ13. When coprocessor interface is disabled through configuration register Index-43h bit 6 setting, the function of this pin is IRQ13.
ISA Bus Interface:		
IRQ[15:14], IRQ[11:9], IRQ[7:3]	I/O Group A Schmitt 9.6/9.6 mA	**Interrupt Request.** The Interrupt Request lines are directly from the ISA Bus, from the PCI Interrupt Routing, or from the steerable Interrupt pins.
RSTDRV	O-Group A 12/16mA	**ISA Bus Reset.** This output is used to reset the ISA Bus and the system device. This pin will be active if the system reset is needed.
SD[15:8]	I/O-Group A 12/12 mA	**ISA High Byte Slot Data Bus.** These pins should connect to the ISA High Byte Slot Data Bus.

Pin Description Table (continued):

Pin Name	Type	Description
ISA Bus Interface:		
XD[7:0]	I/O Group A 12/12 mA	**XD Data Bus.** When the SD[7:0] pins are defined as GPIO[7:0] pins, these pins can be used to drive SD[7:0] if TTL LS245 is used as a buffer. The M1543 signal XDIR will control this buffer.
SD[7:0]/ GPIO[7:0]	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus or General Purpose I/O.** When external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL, these pins are used as the GPIO pins for green control. Otherwise, these pins are SD[7:0]. No external LS245 is required.
SA[19:17]	O-Group A 12/12 mA	**ISA Slot Address Bus A19-A17.** These pins should connect to the ISA System Address Bus.
SA[16:0]	I/O-Group A 12/12 mA	**ISA Slot Address Bus A16-A0.** These pins should connect to the ISA System Address Bus.
SBHEJ	I/O -Group A 12/12 mA	**ISA Byte High Enable.** This pin should connect to the ISA System Byte High Enable pin.
LA[23:17]	I/O-Group A 12/12 mA	**ISA Latched Address Bus.** They are inputs during ISA master cycle and should connect to ISA Slot Latch Address Bus.
IO16J	I -Group A	**ISA 16 Bit I/O Device Indicator.** This is an input and will be driven by the device if the ISA I/O cycle is a 16-bit access.
M16J	I/O-Group A 12/20 mA	**ISA 16 Bit Memory Device Indicator.** This pin will be driven by the device or by the M1543 if the ISA Memory cycle is a 16-bit access.
MEMRJ	I/O-Group A 12/12 mA	**ISA Memory Read.** This signal is an output when the M1543 is the ISA Bus master, or an input during ISA master cycle.
MEMWJ	I/O -Group A 12/12 mA	**ISA Memory Write.** This signal is an output when the M1543 is the ISA Bus master, or an input during ISA master cycle.
AEN	O-Group A 12/12 mA	**ISA I/O Address Enable.** This signal will become active high during DMA cycle to prevent I/O device to decode DMA cycles as valid I/O cycles.
IOCHRDY	I/O-Group A 12/20 mA	**ISA System Ready.** This signal is an output during ISA master cycle, or an input when the M1543 is the ISA Bus master .
NOWSJ	I-Group A	**ISA Zero Wait-State for Input.** This input signal will terminate the CPU to ISA command instantly.
IOCHKJ	I-Group A	**ISA Parity Error.** M1543 will generate NMI to CPU when this signal is asserted.
SYSCLK	O-Group A 12/12 mA	**ISA System Clock.** This output is generated by the PCI clock and is used as the ISA system clock.
BALE	O-Group A 12/12 mA	**Bus Address Latch Enable.** BALE will be asserted throughout DMA, ISA master, and the Refresh cycles. Otherwise, it will only assert half the SYSCLK before the ISA command is asserted.
IORJ	I/O-Group A 12/16 mA	**ISA I/O Read.** This signal is an input during ISA master cycle, and an output when the M1543 is the ISA Bus master.
IOWJ	I/O-Group A 12/12 mA	**ISA I/O write.** This signal is an input during ISA master cycle, and an output when the M1543 is the ISA Bus master.
SMEMRJ	O-Group A 12/12 mA	**ISA System Memory Read.** This signal indicates that the memory read command is below 1M Byte address.
SMEMWJ	O-Group A 12/12 mA	**ISA System Memory Write.** This signal indicates that the memory write command is below 1M Byte address.
DREQ[7:5], DREQ[3:0]	I-Group A Schmitt	**DMA Request Signals.** These are inputs from the DMA Device or ISA Master Request. The M1543 will combine the DMA request, ISA Master request, IDE Bus Master request, and USB Master request to generate the PHOLDJ to the PCI Arbiter.
DACKJ[7:5], DACKJ[3:0]	O-Group A 9.6/9.6 mA	**DMA Acknowledge Signals.** After the M1543 has acquired the PCI Bus grant (PHLDAJ), the internal arbiter will assert the DMA acknowledge signal to the DMA Device Request.

Pin Description Table (continued):

Pin Name	Type	Description
ISA Bus Interface:		
TC	O-Group A	**DMA End of Process.** This signal will be asserted after the DMA Device has ended the transaction.
REFRSHJ	I/O Group A	**ISA Refresh Cycle.** This signal is an input during ISA master cycle, and an output when the M1543 is the ISA Bus master.
Miscellaneous Logic:		
SPKR	O-Group A	**Speaker Output.** This pin is used to control the Speaker Output and should connect to the Speaker.
RTCAS	O-Group A	**RTC Address Strobe.** This pin is used as the RTC Address Strobe and should connect to the RTC.
RTCRW	O-Group A	**RTC Write Strobe.** This pin is used as the RTC Read/Write Command and should connect to the RTC. The M1543 will drive the RTC command through dedicated pin instead of the 74F32 decode to save the system cost.
RTCDS	O-Group A	**RTC Data Strobe.** This pin is used as the RTC Data Strobe and should connect to the RTC.
SPLED	O-Group A	**Speed LED Output.** This pin is used to control the Speed LED Output and should connect to LED.
ROMKBCSJ	O-Group A	**ROM/Keyboard Chip Select.** This pin is the ROM chip select and is the Keyboard chip select also when internal KBC is disabled.
SERIRQ/ GPI[2]	B/I Group A	**Serial Interrupt Request or General Purpose Input.** This pin is used to support the serial interrupt protocol or as a General Purpose Input.
SIRQI	I -Group A	**Steerable IRQ Input1.** This is a steerable Interrupt input, M1543 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
SIRQII	I -Group A	**Steerable IRQ Input2.** This is a steerable Interrupt input, M1543 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
IRQ8J	I -Group C	**RTC Interrupt Input.** This is the RTC Interrupt input. This pin belongs to the Power Group C, and it can support the RTC Alarm function during Soft-off or Suspend state.
XDIR/ GPO[12]	O-Group A	**XD Bus Direction Control or General Purpose Output.** When external XD bus is designed on motherboard, this pin is X-bus direction control. Otherwise, this pin is a general purpose output.
KBINH/ IRQ1I	I/O Group A	**Keyboard Inhibit or Interrupt One Input.** This pin will be the Keyboard Inhibit input when internal KBC is enabled. Otherwise, it will be the IRQ1 input.
KBCLK/ GPI[9]	I/O Group A	**Keyboard Clock or General Purpose Input.** This pin is the Keyboard interface Clock when internal KBC is enabled. Otherwise, it is a general purpose input.
KBDATA/ GPI[10]	I/O Group A	**Keyboard data or General Purpose Input.** This pin is a KB interface DATA when internal KBC is enabled. Otherwise, this pin is a general purpose input.
MSCLK/ GPI[11]	I/O Group A	**Mouse Clock or General Purpose Input.** This pin is a mouse clock when internal PS2 Keyboard is enabled. Otherwise, this pin is a general purpose input.
MSDATA/ IRQ12I	I/O Group A	**Mouse Data or Interrupt Line 12 Input.** This pin is mouse data when internal PS2 Keyboard is enabled. Otherwise, this pin is the IRQ12 input.
BIOSA17/ GPO[19]	O-Group A	**ROM Address 17 or General Purpose Output.** This pin is the ROM A17 control when 2M ROM is used, or it is a general purpose output.
BIOSA16/ GPO[18]	O-Group A	**ROM Address 16 or General Purpose Output.** This pin is the ROM A16 control when 2M ROM is used, or it is a general purpose output.
PCSJ/ GPO[0]	O-Group A	**Programmable Chip Select or General Purpose Output.** This pin can be selected as a programmable Chip Select, or as a general purpose output.
IDE interface:		
PIDE_DRQ	I-Group D	**Primary IDE DMA Request for IDE Master.** This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer.
SIDE_DRQ	I-Group D	**Secondary IDE DMA Request for IDE Master.** This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer.

Pin Description Table (continued):

Pin Name	Type	Description
IDE interface:		
PIDE_AKJ	O-Group D	**Primary IDE DACKJ for IDE Master.** This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer.
SIDE_AKJ	O-Group D	**Secondary IDE DACKJ for IDE Master.** This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer.
PIDE_RDY	I-Group D	**Primary IDE Ready.** This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
SIDE_RDY	I-Group D	**Secondary IDE Ready.** This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
PIDEIORJ	O-Group D	**Primary IDE IORJ Command.** This is the IORJ command output pin to notify the Primary IDE device to assert the Read Data.
SIDEIORJ	O-Group D	**Secondary IDE IORJ Command.** This is the IORJ command output pin to notify the Secondary IDE device to assert the Read Data.
PIDEIOWJ	O-Group D	**Primary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Primary IDE device that the available Write Data is already asserted by M1543.
SIDEIOWJ	O-Group D	**Secondary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Secondary IDE device that the available Write Data is already asserted by M1543.
PIDECS1J	O-Group D	**IDE Chip Select 1 for Primary Channel 0.** This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3J	O-Group D	**IDE Chip Select 3 for Primary Channel 1.** This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
SIDECS1J	O-Group D	**IDE Chip Select 1 for Secondary Channel 0.** This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3J	O-Group D	**IDE Chip Select 3 for Secondary Channel 1.** This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
PIDE_A[2:0]	O-Group D	**Primary IDE ATA Address Bus.** These are the Address pins connected to Primary Channel.
SIDE_A[2:0]	O-Group D	**Secondary IDE ATA Address Bus.** These are the Address pins connected to Secondary Channel.
PIDE_D[15:0]	I/O Group D	**Primary IDE ATA Data Bus.** These are the Data pins connected to Primary Channel.
SIDE_D[15:0]	I/O Group D	**Secondary IDE ATA Data Bus.** These are the Data pins connected to Secondary Channel.
Power Management Unit:		
RSM_RSTJ	I-Group C Schmitt	**Resume Circuit Initial Reset Input.** This input is used to initialize the resume circuit.
SMIJ	O-Group E 4/4 mA	**SMM Interrupt Output.** This output should be connected to CPU SMM Interrupt input.
STPCLKJ	O-Group E 4/4 mA	**Stop CPU Internal Clock Output.** This output is used to stop the CPU internal clock and should be connected to CPU STPCLKJ input.
SLEEPJ/ GPO[20]	O-Group E 4/4 mA	**Pentium PRO Sleep State or General Purpose Output.** This output will force Pentium PRO CPU to enter Sleep State, or as a general purpose output.

Pin Description Table (continued):

Pin Name	Type	Description
Power Management Unit:		
ZZ/ GPO[1]	O-Group E 4/4mA	**PBSRAM Power Saving Mode or General Purpose Output.** This output is used to control L2 cache entering power saving mode, or as a general purpose output.
CPU_STPJ/ GPO[2]	O-Group B 4/4mA	**Clock Cell CPU Clock Stop or General Purpose Output.** This output is used to stop the CPU Clock of the clock generator, or as a general purpose output.
PCI_STPJ/ GPO[3]	O-Group B 4/4mA	**Clock Cell PCI Clock Stop or General Purpose Output.** This output is used to stop the PCI Clock of the clock generator, or as a general purpose output.
SUSTAT1J	O-Group C 4/4 mA	**Suspend Status for North Bridge.** This output is used to notice the north bridge to control DRAM suspend refresh circuit.
PWRBTNJ	I-Group C Schmitt	**Power Button Input.** This input is used to support the ACPI Power Button function.
PCIREQJ/ GPI[3]	I-Group B	**PCI Bus Request Event Input or General Purpose Input.** This input comes from the North Bridge or external circuit to notice M1543 there is PCI request pending. This pin can also be programmed as a general purpose input.
SQWO/ GPO[9]	O-Group A 4/4mA	**Square Wave Output or General Purpose Output.** This output can be used to output Square Wave with 1Hz or 2Hz, or as a general purpose output.
OFF_PWR1/ GPO[22]	O-Group C 4/4mA	**Remove All Circuit Power Except Internal Suspend Circuit and External DRAM or General Purpose Output.**
OFF_PWR2/ GPO[23]	O-Group C 4/4mA	**Remove All Circuit Power Except Internal Suspend Circuit or General Purpose Output.**
RI	I-Group C Schmitt	**Ring-in.** This input connects to Modem Ring-in input to support ACPI Ring-in function.
THRMJ	I-Group A Schmitt	**Thermal Event Input or General Purpose Input.** THRMJ is a triggered input to the M1543 showing that the external thermal detected circuits are requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
ACPWR	I-Group C Schmitt	Baby AT or ATX hardware configure input. This chip supports baby AT power supply when pull low, ATX power supply when pull high.
DOCKJ	I-Group C	**Docking Insert Event Input or General Purpose Input.** This triggered input is used as a docking event indicator, or as a general purpose input signal.
USB interface:		
USBP0+ USBP0-	I/O Group B	**Universal Serial Bus Port 0.** These are the serial data pair for USB Port 0.
USBP1+ USBP1-	I/O Group B	**Universal Serial Bus Port 1.** These are the serial data pair for USB Port 1.
OVCRJ/ GPI[0]	I Group B	**Over Current Detect Inputs or General Purpose Input.** This pin is used to monitor the USB Power Over Current, or as a general purpose input.
SM Bus signal:		
SMBCLK	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Clock.** SM Bus clock signal should be combined with SM Bus data to carry information between the devices connected to the SM Bus.
SMBDATA	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Data Line.** SM Bus data signal should be combined with SM Bus clock to carry information between the devices connected to the SM Bus.

Pin Description Table (continued):

Pin Name	Type	Description
Floppy Disk Interface:		
RDATAJ	I (IS) Group A	**Read Disk Data.** The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
WGATEJ	O (O36) Group A	**Write Gate**. This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
WDATAJ	O (O36) Group A	**Write Data**. This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
HDSELJ	O (O36) Group A	**Head Select**. This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DIRJ	O (O36) Group A	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
STEPJ	O (O36) Group A	**Step.** This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
DSKCHGJ	I (IS) Group A	**Disk Change.** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
DRV0J, DRV1J	O (O36) Group A	**Drive Select 0, 1**. Active low, output select drives 0-1.
MOT0J, MOT1J	O (O36) Group A	**Motor on 0, 1**. These active-low outputs select motor drives 0-1.
WPROTJ	I (IS) Group A	**Write Protected**. This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.
TRK0J	I (IS) Group A	**Track 00**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.
INDEXJ	I (IS) Group A	**Index**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
DENSEL	O (O36) Group A	**Density Select**. Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected.
Serial Port Interface:		
SIN1, SIN2	I (IS) Group A	**Receive Data**. Receiver serial data input signal.
SOUT1, SOUT2	O (O4) Group A	**Transmit Data**. Transmitter serial data output from Serial Port.
RTS1J	O (O4) Group A	**Request to send**. Active low Request to send output for Primary Serial port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. RTS1J is a hardware setting pin for configuration port. When pull high-configuration port is 0x3F0h, when pull low-configuration port is 0x370h. This pin has a 20K(default) internal pull-up resistor.
RTS2J	O (O4) Group A	**Request to send**. This active low output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. RTS2J is a hardware setting pin for internal KBC. When pull high-KBC enable, when pull low-KBC disable. This pin has a 20K(default) internal pull-up resistor.

Pin Description Table (continued):

Pin Name	Type	Description
Serial Port Interface:		
DTR1J	O (O4) Group A	**Data Terminal Ready**. This is an active low output for primary serial port. Handshake output signal signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation.
DTR2J	O (O4) Group A	**Data Terminal Ready.** This active low output is for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive mode (high). Forced inactive during loop mode operation. DTR2J is a hardware setting pin for internal KB. When pull high- internal KB is PS2 mode, when pull low-internal KB is AT mode. This pin has a 20K(default) internal pull-up resistor.
CTS1J CTS2J	I (IS) Group A	**Clear to Send.** This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTSJ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	I (IS) Group A	**Data Set Ready.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit5 of Modem Status Register (MSR). A DSRJ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. Note: Bit 5 of MSR is the complement of DSRJ.
DCD1J, DCD2J	I (IS) Group A	**Data Carrier Detect**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. Note : bit 7 of MSR is the complement of DCDJ.
RI1J, RI2J	I (IS) Group A	**Ring Indicator**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). An RIJ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note : bit 6 of MSR is the complement of RIJ.
Printer Port Interface:		
AUTOFDJ	O (O20) Group A	**Autofeed Output**. This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
INITJ	O (O20) Group A	**Initiate Output**. This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
SLCTINJ	O (O20) Group A	**Printer select input**. This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.

Pin Description Table (continued):

Pin Name	Type	Description
Printer Port Interface:		
STROBJ	O (O20) Group A	**Strobe Output**. This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	I (IS) Group A	**Busy**. This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	I (IS) Group A	**Acknowledge**. This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	I (IS) Group A	**Paper End**. This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
SLCT	I (IS) Group A	**Printer Selected Status**. This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	I Group A	**Error**. This active low signal indicates an error condition at the printer.
PD0-PD7	I/O (I/O20) Group A	**Port Data**. This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
Power Pins:		
VCC_A	P	**Vcc for Power Group A.** This power is used for ISA interface.
VCC_3A	P	**Vcc for Power Group A.** This power is used for ISA interface.
VCC_B	P	**Vcc for Power Group B.** This power is used for PCI interface.
VCC_C	P	**Vcc for Power Group C.** This power is used for resume/suspend control interface signals during normal operation and suspend periods.
VCC_3C	P	**Vcc for Power Group C.** This power is used for Resume/Suspend Control interface.
VCC_D	P	**Vcc for Power Group D.** This power is used for IDE interface.
VCC_E	P	**Vcc 3.3V or 2.5V for Power Group E.** This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VDD_5	P	**Vcc 5.0V for core Power.** It supplies the core power for the internal circuit except the suspend circuit.
VDD_5S	P	**Vcc 5.0V for Suspend/Resume Core Power.** It supplies the core power for the internal suspend/resume circuit.
Vss or Gnd	P	**Ground.**

Type Description:

I	Input TTL compatible.
IS	Input with Schmitt Trigger.
I/O16	Input/Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V.
I/O20	Input/Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V.
ICLK	CLK input.
OCLK	CLK output.
O4	Output with 4 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
O8	Output with 8 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
O16	Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V.
O20	Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V.
O36	Output with 36 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
OD16	Open drain outputs, sinks 24 mA @ 0.4 V.

2.3 Numerical Pin List

Pin No.	Pin Name	Type
A1	AD21	I/O
A2	AD20	I/O
A3	AD19	I/O
A4	AD16	I/O
A5	IRDYJ	I/O
A6	SERRJ	I
A7	AD14	I/O
A8	AD10	I/O
A9	AD6	I/O
A10	AD1	I/O
A11	PHLDJ	O
A12	GPI3	I
A13	USBP1-	I/O
A14	RTCDS	O
A15	ROMCSJ	O
A16	XD2	I/O
A17	XD5	I/O
A18	SD15	I/O
A19	SD14	I/O
A20	SD13	I/O
B1	CBEJ3	I/O
B2	AD23	I/O
B3	AD22	I/O
B4	AD17	I/O
B5	FRAMEJ	I/O
B6	STOPJ	I/O
B7	AD15	I/O
B8	AD11	I/O
B9	AD7	I/O
B10	AD2	I/O
B11	PHLDAJ	I
B12	USBCLK	I
B13	USBP0+	I/O
B14	RTCRW	O
B15	XD0	I/O
B16	XD3	I/O
B17	XD6	I/O
B18	SD12	I/O
B19	DREQ7	I
B20	SD11	I/O
C1	AD26	I/O
C2	AD25	I/O
C3	AD24	I/O
C4	AD18	I/O
C5	CBEJ2	I/O

Pin No.	Pin Name	Type
C6	DEVSELJ	I/O
C7	CBEJ1	I/O
C8	AD12	I/O
C9	CBEJ0	I/O
C10	AD3	I/O
C11	GPO3	O
C12	GPI0	I
C13	USBP0-	I/O
C14	RTCAS	O
C15	XD1	I/O
C16	XD4	I/O
C17	XD7	I/O
C18	DACKJ7	O
C19	SD10	I/O
C20	DREQ6	I
D1	AD29	I/O
D2	AD28	I/O
D3	AD27	I/O
D4	AD30	I/O
D5	AD31	I/O
D6	TRDYJ	I/O
D7	PAR	I/O
D8	AD13	I/O
D9	AD8	I/O
D10	AD4	I/O
D11	GPO2	O
D12	SIRQI	I
D13	GPO19	O
D14	GPO12	O
D15	GPO0	O
D16	GPI2	I
D17	SPKR	O
D18	SD9	I/O
D19	DACKJ6	O
D20	SD8	I/O
E1	PIDECS3	O
E2	PIDECS1	O
E3	PIDEA2	O
E4	INTA	I
E5	INTB	I/O
E6	INTC	I/O
E7	PCIRSTJ	O
E8	PCICLK	I
E9	AD9	I/O
E10	AD5	I/O

Numerical Pin List (continued)

Pin No.	Pin Name	Type
E11	AD0	I/O
E12	USBP1+	I/O
E13	SIRQII	I
E14	GPO18	O
E15	GPO9	O
E16	THRMJ	I
E17	SPLED	O
E18	DREQ5	I
E19	MEMWJ	I/O
E20	DACKJ5	O
F1	PIDEA0	O
F2	PIDEA1	O
F3	PIDEDAKJ	O
F4	INTD	I/O
F5	PIDEIRDYJ	I
F6	VCC_B	P
F14	VCC_A	P
F15	VCC_E	P
F16	IRQ1I	I/O
F17	MEMRJ	I/O
F18	DREQ0	I
F19	LA17	I/O
F20	DACKJ0	O
G1	PIDERJ	O
G2	PIDEWJ	O
G3	PIDEDRQ	I
G4	PIDED15	I/O
G5	PIDED0	I/O
G6	VCC_D	P
G15	VCC_3C	P
G16	LA18	I/O
G17	IRQ14	I/O
G18	INIT	O
G19	A20MJ	O
G20	IRQ13	I/O
H1	PIDED14	I/O
H2	PIDED1	I/O
H3	PIDED13	I/O
H4	PIDED2	I/O
H5	PIDED12	I/O
H8		
H9		
H10		
H11		
H12		

Pin No.	Pin Name	Type
H13		
H16	LA19	I/O
H17	IRQ15	I/O
H18	SMIJ	O
H19	NMI	O
H20	INTR	O
J1	PIDED3	I/O
J2	PIDED11	I/O
J3	PIDED4	I/O
J4	PIDED10	I/O
J5	PIDED5	I/O
J8		
J9	GND	P
J10	GND	P
J11	GND	P
J12	GND	P
J13		
J16	LA20	I/O
J17	GPO20	O
J18	STPCLK	O
J19	IGNNEJ	O
J20	CPURST	O
K1	PIDED9	I/O
K2	PIDED6	I/O
K3	PIDED8	I/O
K4	PIDED7	I/O
K5	SIDECS3	O
K8		
K9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K13		
K16	GPO1	O
K17	GPO22	O
K18	RSMRSTJ	I
K19	SUSTAT1J	O
K20	ACPWR	I
L1	SIDECS1	O
L2	SIDEA2	O
L3	SIDEA0	O
L4	SIDEA1	O
L5	SIDEDAKJ	O
L8		
L9	GND	P

Numerical Pin List (continued)

Pin No.	Pin Name	Type
L10	GND	P
L11	GND	P
L12	GND	P
L13		
L16	SMBDATA	I/O
L17	GPO23	O
L18	DOCKJ	I
L19	IRQ8J	I
L20	PWRBTNJ	I
M1	SIDEIRDYJ	I
M2	SIDERJ	O
M3	SIDEWJ	O
M4	SIDEDRQ	I
M5	SIDED15	I/O
M8		
M9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13		
M16	SMBCLK	I/O
M17	LA21	I/O
M18	RI	I
M19	OSC32KO	O
M20	PWG	I
N1	SIDED0	I/O
N2	SIDED14	I/O
N3	SIDED1	I/O
N4	SIDED13	I/O
N5	SIDED2	I/O
N8		
N9		
N10		
N11		
N12		
N13		
N15	VDD_5S	P
N16	IRQ11	I/O
N17	LA22	I/O
N18	IRQ10	I/O
N19	OSC32II	I
N20	OSC32I	I
P1	SIDED12	I/O
P2	SIDED3	I/O
P3	SIDED11	I/O
P4	SIDED4	I/O
P5	XDIRJ	O
P6	VCC_A	P
P15	VCC_C	P
P16	LA23	I/O
P17	IO16	I
P18	SBHEJ	I/O
P19	M16	I/O
P20	OSC14M	I
R1	SIDED10	I/O
R2	SIDED5	I/O
R3	SIDED9	I/O
R4	MOT1J	O
R5	DRV0J	O
R6	VDD_5	P
R7	VCC_A,_D	P
R14	VCC_3A	P
R15	VCC_A	P
R16	BALE	O
R17	TC	O
R18	SA0	I/O
R19	SA1	I/O
R20	SA2	I/O
T1	SIDED6	I/O
T2	SIDED8	I/O
T3	DSKCHGJ	I
T4	DRV1J	O
T5	MOT0J	O
T6	DENSEL	O
T7	DCD1J	I
T8	PD3	I/O
T9	ACKJ	I
T10	RSTDRV	O
T11	MSCLK	O
T12	MSDATA	I/O
T13	SD0	I/O
T14	SA19	I/O
T15	DACKJ3	O
T16	DACKJ2	O
T17	SA6	I/O
T18	SA3	I/O
T19	SA4	I/O
T20	SA5	I/O
U1	SIDED7	I/O
U2	HDSELJ	O

Numerical Pin List (continued)

Pin No.	Pin Name	Type
U3	RDATAJ	I
U4	INDEXJ	I
U5	DCD2J	I
U6	DSR1J	I
U7	STROBJ	O
U8	PD4	I/O
U9	BUSY	I
U10	ERRORJ	I
U11	KBCLK	I/O
U12	KBDATA	I/O
U13	SD1	I/O
U14	SMEMRJ	O
U15	SA17	I/O
U16	IRQ3	I/O
U17	IRQ5	I/O
U18	SA8	I/O
U19	SA7	I/O
U20	IRQ4	I/O
V1	WPROTJ	I
V2	TRK0J	I
V3	WGATEJ	O
V4	DTR2J	O
V5	RI1J	I
V6	DTR1J	O
V7	PD0	I/O
V8	PD5	I/O
V9	PE	I
V10	XINITJ	O
V11	IRQ9	I/O
V12	DREQ2	I
V13	NOWSJ	I
V14	AEN	O
V15	IORJ	I/O
V16	SA15	I/O
V17	DREQ1	I
V18	SA10	I/O
V19	IRQ6	I/O
V20	SA9	I/O
W1	WDATAJ	O
W2	STEPJ	O
W3	RTS2J	O
W4	SOUT2	O
W5	CTS1J	I

Pin No.	Pin Name	Type
W6	SOUT1	O
W7	PD1	I/O
W8	PD6	I/O
W9	SLCT	I
W10	SLCTINJ	O
W11	SD6	I/O
W12	SD4	I/O
W13	SD2	I/O
W14	SMEMWJ	O
W15	SA18	I/O
W16	DREQ3	I
W17	SA14	I/O
W18	SYSCLK	O
W19	SA11	I/O
W20	IRQ7	I/O
Y1	RI2J	I
Y2	CTS2J	I
Y3	DSR2J	I
Y4	SIN2	I
Y5	RTS1J	O
Y6	SIN1	I
Y7	PD2	I/O
Y8	PD7	I/O
Y9	AUTOFDJ	O
Y10	IOCK	I/O
Y11	SD7	I/O
Y12	SD5	I/O
Y13	SD3	I/O
Y14	IOCHRDY	I/O
Y15	IOWJ	I/O
Y16	SA16	I/O
Y17	DACKJ1	O
Y18	SA13	I/O
Y19	REFRSHJ	I
Y20	SA12	I/O

2.4 Alphabetical Pin List

Pin No.	Pin Name	Type
G19	A20MJ	O
K20	ACPWR	I
T9	ACKJ	I
E11	AD0	I/O
A10	AD1	I/O
A8	AD10	I/O
B8	AD11	I/O
C8	AD12	I/O
D8	AD13	I/O
A7	AD14	I/O
B7	AD15	I/O
A4	AD16	I/O
B4	AD17	I/O
C4	AD18	I/O
A3	AD19	I/O
B10	AD2	I/O
A2	AD20	I/O
A1	AD21	I/O
B3	AD22	I/O
B2	AD23	I/O
C3	AD24	I/O
C2	AD25	I/O
C1	AD26	I/O
D3	AD27	I/O
D2	AD28	I/O
D1	AD29	I/O
C10	AD3	I/O
D4	AD30	I/O
D5	AD31	I/O
D10	AD4	I/O
E10	AD5	I/O
A9	AD6	I/O
B9	AD7	I/O
D9	AD8	I/O
E9	AD9	I/O
V14	AEN	O
Y9	AUTOFDJ	O
R16	BALE	O
U9	BUSY	I
C9	CBEJ0	I/O
C7	CBEJ1	I/O
C5	CBEJ2	I/O
B1	CBEJ3	I/O
J20	CPURST	O
W5	CTS1J	I

Pin No.	Pin Name	Type
Y2	CTS2J	I
F20	DACKJ0	O
Y17	DACKJ1	O
T16	DACKJ2	O
T15	DACKJ3	O
E20	DACKJ5	O
D19	DACKJ6	O
C18	DACKJ7	O
T7	DCD1J	I
U5	DCD2J	I
T6	DENSEL	O
C6	DEVSELJ	I/O
P5	DIRJ	O
L18	DOCKJ	I
F18	DREQ0	I
V17	DREQ1	I
V12	DREQ2	I
W16	DREQ3	I
E18	DREQ5	I
C20	DREQ6	I
B19	DREQ7	I
R5	DRV0J	O
T4	DRV1J	O
T3	DSKCHGJ	I
U6	DSR1J	I
Y3	DSR2J	I
V6	DTR1J	O
V4	DTR2J	O
U10	ERRORJ	I
B5	FRAMEJ	I/O
H10	-	
H11	-	
H12	-	
H13	-	
H8	-	
H9	-	
J10	GND	P
J11	GND	P
J12	GND	P
J13	-	
J8	-	
J9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P

Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
K13	-	
K8	-	
K9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L13	-	
L8	-	
L9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13	-	
M8	-	
M9	GND	P
N10	-	
N11	-	
N12	-	
N13	-	
N8	-	
N9	-	
C12	GPI0	I
D16	GPI2	I
A12	GPI3	I
D15	GPO0	O
K16	GPO1	O
D14	GPO12	O
E14	GPO18	O
D13	GPO19	O
D11	GPO2	O
J17	GPO20	O
K17	GPO22	O
L17	GPO23	O
C11	GPO3	O
E15	GPO9	O
U2	HDSELJ	O
J19	IGNNEJ	O
U4	INDEXJ	I
V10	INITJ	O
G18	INIT	O
E4	INTA	I
E5	INTB	I/O
E6	INTC	I/O
F4	INTD	I/O
H20	INTR	O

Pin No.	Pin Name	Type
P17	IO16	I
Y14	IOCHRDY	I/O
Y10	IOCK	I/O
V15	IORJ	I/O
Y15	IOWJ	I/O
A5	IRDYJ	I/O
N18	IRQ10	I/O
N16	IRQ11	I/O
G20	IRQ13	I/O
G17	IRQ14	I/O
H17	IRQ15	I/O
F16	IRQ1I	I/O
U16	IRQ3	I/O
U20	IRQ4	I/O
U17	IRQ5	I/O
V19	IRQ6	I/O
W20	IRQ7	I/O
L19	IRQ8J	I
V11	IRQ9	I/O
U11	KBCLK	I/O
U12	KBDATA	I/O
F19	LA17	I/O
G16	LA18	I/O
H16	LA19	I/O
J16	LA20	I/O
M17	LA21	I/O
N17	LA22	I/O
P16	LA23	I/O
P19	M16	I/O
F17	MEMRJ	I/O
E19	MEMWJ	I/O
T5	MOT0J	O
R4	MOT1J	O
T11	MSCLK	O
T12	MSDATA	I/O
H19	NMI	O
V13	NOWSJ	I
P20	OSC14M	I
N20	OSC32I	I
N19	OSC32II	I
M19	OSC32KO	O
D7	PAR	I/O
E8	PCICLK	I
E7	PCIRSTJ	O
V7	PD0	I/O

Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
W7	PD1	I/O
Y7	PD2	I/O
T8	PD3	I/O
U8	PD4	I/O
V8	PD5	I/O
W8	PD6	I/O
Y8	PD7	I/O
V9	PE	I
B11	PHLDAJ	I
A11	PHLDJ	O
F1	PIDEA0	O
F2	PIDEA1	O
E3	PIDEA2	O
E2	PIDECS1	O
E1	PIDECS3	O
G5	PIDED0	I/O
H2	PIDED1	I/O
H4	PIDED2	I/O
J1	PIDED3	I/O
J3	PIDED4	I/O
J5	PIDED5	I/O
K2	PIDED6	I/O
K4	PIDED7	I/O
K3	PIDED8	I/O
K1	PIDED9	I/O
J4	PIDED10	I/O
J2	PIDED11	I/O
H5	PIDED12	I/O
H3	PIDED13	I/O
H1	PIDED14	I/O
G4	PIDED15	I/O
F3	PIDEDAKJ	O
G3	PIDEDRQ	I
F5	PIDEIRDYJ	I
G1	PIDERJ	O
G2	PIDEWJ	O
M20	PWG	I
L20	PWRBTNJ	I
U3	RDATAJ	I
Y19	REFRSHJ	I
V5	RI1J	I
Y1	RI2J	I
M18	RI	I
A15	ROMCSJ	O
K18	RSMRSTJ	I

Pin No.	Pin Name	Type
T10	RSTDRV	O
C14	RTCAS	O
A14	RTCDS	O
B14	RTCRW	O
Y5	RTS1J	O
W3	RTS2J	O
R18	SA0	I/O
R19	SA1	I/O
V18	SA10	I/O
W19	SA11	I/O
Y20	SA12	I/O
Y18	SA13	I/O
W17	SA14	I/O
V16	SA15	I/O
Y16	SA16	I/O
U15	SA17	I/O
W15	SA18	I/O
T14	SA19	I/O
R20	SA2	I/O
T18	SA3	I/O
T19	SA4	I/O
T20	SA5	I/O
T17	SA6	I/O
U19	SA7	I/O
U18	SA8	I/O
V20	SA9	I/O
P18	SBHEJ	I/O
T13	SD0	I/O
U13	SD1	I/O
C19	SD10	I/O
B20	SD11	I/O
B18	SD12	I/O
A20	SD13	I/O
A19	SD14	I/O
A18	SD15	I/O
W13	SD2	I/O
Y13	SD3	I/O
W12	SD4	I/O
Y12	SD5	I/O
W11	SD6	I/O
Y11	SD7	I/O
D20	SD8	I/O
D18	SD9	I/O
A6	SERRJ	I
L3	SIDEA0	O

Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
L4	SIDEA1	O
L2	SIDEA2	O
L1	SIDECS1	O
K5	SIDECS3	O
N1	SIDED0	I/O
N3	SIDED1	I/O
R1	SIDED10	I/O
P3	SIDED11	I/O
P1	SIDED12	I/O
N4	SIDED13	I/O
N2	SIDED14	I/O
M5	SIDED15	I/O
N5	SIDED2	I/O
P2	SIDED3	I/O
P4	SIDED4	I/O
R2	SIDED5	I/O
T1	SIDED6	I/O
U1	SIDED7	I/O
T2	SIDED8	I/O
R3	SIDED9	I/O
L5	SIDEDAKJ	O
M4	SIDEDRQ	I
M1	SIDEIRDYJ	I
M2	SIDERJ	O
M3	SIDEWJ	O
Y6	SIN1	I
Y4	SIN2	I
D12	SIRQI	I
E13	SIRQII	I
W9	SLCT	I
W10	SLCTINJ	O
M16	SMBCLK	I/O
L16	SMBDATA	I/O
U14	SMEMRJ	O
W14	SMEMWJ	O
H18	SMIJ	O
W6	SOUT1	O
W4	SOUT2	O
D17	SPKR	O
E17	SPLED	O
W2	STEPJ	O
B6	STOPJ	I/O
U7	STROBJ	O
J18	STPCLK	O
K19	SUSTAT1J	O

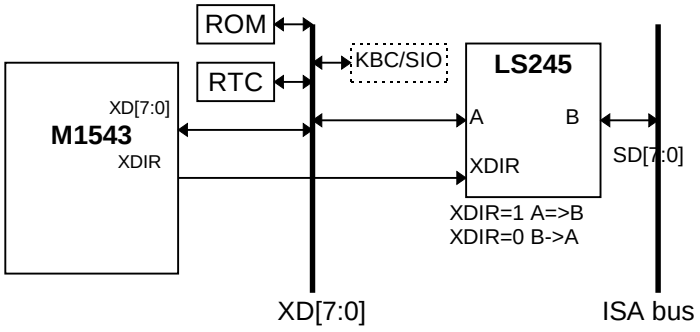
Pin No.	Pin Name	Type
W18	SYSCLK	O
V2	TRK0J	I
R17	TC	O
E16	THRMJ	I
D6	TRDYJ	I/O
B12	USBCLK	I
B13	USBP0+	I/O
C13	USBP0-	I/O
E12	USBP1+	I/O
A13	USBP1-	I/O
G6	VCC_D	P
R6	VDD_5	P
N15	VDD_5S	P
P6	VCC_A,_D	P
R7	VCC_A,_D	P
R14	VCC_3A	P
R15	VCC_A	P
P15	VCC_C	P
G15	VCC_3C	P
F15	VCC_E	P
F14	VCC_A	P
F6	VCC_B	P
W1	WDATAJ	O
V3	WGATEJ	O
V1	WPROTJ	I
B15	XD0	I/O
C15	XD1	I/O
A16	XD2	I/O
B16	XD3	I/O
C16	XD4	I/O
A17	XD5	I/O
B17	XD6	I/O
C17	XD7	I/O

2.5 Hardware Setting Description:

Pin No.	Pin Name	Setup, Configuration
D15	PCSJ	Pull-low, POWER PC mode Pull-high, INTEL PC mode
A11	XPHOLDJ	Pull-low, USB in test mode. (for test only) Pull-high, USB in normal mode.
E17	SPLED	Pull-low, support 256KB ROM Pull-high, not support 256KB ROM
P5	XDIR	Pull-low, Pentium Pro CPU is used. Pull-high, Pentium CPU is used.
R17	TC	Pull-low, pins SD/GPIO[7:0] are SD[7:0], external LS245 is not required. Pull-high, pins SD/GPIO[7:0] are GPIO[7:0], external LS245 is required.
D17	SPKR	Pull-low, internal Super I/O test mode enabled. (for test only) Pull-high, internal Super I/O test mode disabled.
A15	ROMKBCSJ	Pull-low, chip test mode is enabled. (for test only) Pull-high, chip test mode is disabled.
Y5	RTS1J	Pull-low, 0x370h. Pull-high, 0x3F0h.
W3	RTS2J	Pull-low, internal keyboard disable. Pull-high, internal keyboard enable.
V4	DTR2J	Pull-low, internal keyboard is AT mode. Pull-high, internal keyboard is PS2 mode.

2.6 XDIR Control

When pin TC is pull high, the external LS245 is required. The connection is:



1) PCI I/O Read ISA : XDIR=0
2) PCI I/O Write ISA : XDIR=1
3) PCI Memory Read ISA : XDIR=0
4) PCI Memory Write ISA : XDIR=1
5) PCI access XD bus device (RTC,ROM,KBC) : XDIR =1
6) ISA Refresh : XDIR =1
7) ISA/DMA master MR/IOW : XDIR=1
8) ISA/DMA master MW/IOR : XDIR=0

Section 3: Function Description

3.1 PCI Command Set

The command types M1543 supports in Slave mode are Interrupt Acknowledge, Special cycle, I/O read, I/O write, memory read, memory write, configuration read and configuration write and other multiple memory read/write cycles.

M1543 PCI Cycle Description

CBEJ	Command Type	as Target	as Initiator
0000	Interrupt	Yes	No
0001	Special Cycle	Yes - Note.1	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes - Note.2	No
1101	Reserved	No	No
1110	Memory Read line	Yes - Note.2	No
1111	Memory Write and Invalidate	Yes - Note.3	No

Note 1: The M1543 only decodes Stop Grant special cycle, and Halt special cycle and Shutdown special cycle. All other special cycles are ignored.
Note 2: Treated as Memory read
Note 3: Treated as Memory write

3.2 PCI Slave Description

As a PCI slave, the M1543 will assert DEVSELJ signal to indicate it is the target of the PCI transaction. DEVSELJ is asserted when the M1543 positively or subtractively decodes the PCI transaction. The configuration cycle, USB programming cycle and IDE I/O cycle are positively decoded. The timer and interrupt controller programming cycles are positively or subtractively decoded via register setting. All others are subtractively decoded except for docking mode. All cycles will be positively decoded in docking mode. These cycles include PCI to ISA slave cycles. Under docking mode, M1543 only supports positive decode.

A 32-bit posted write buffer is embedded to support PCI to ISA memory write cycles and delay transaction cycle. Multiple read/write transactions are not supported. Hence, any burst cycles decoded by the M1543 will be terminated by disconnecting semantics after the first data transaction has completed. The M1543 will retry any PCI initiated cycle when its internal buffer cycle is still active.

M1543 supports delay transaction and discard counter in compliance with PCI specification 2.1.

3.2.1 Posted Write Buffer

The PCI-to-ISA memory write cycles will be posted into the write buffer when it is enabled, and the buffer is scheduled to be written to the ISA bus. Any subsequent PCI cycles to the M1543 will be retried until the posted write buffer is empty. The buffer also optionally supports data I/O posted write cycle for sound cards.

The posted write buffer must be flushed and disabled before an ISA/DMA master owns the ISA and PCI bus. This rule eliminates the possibility of a deadlock caused by a committed ISA cycle.

3.3 PCI Master

3.3.1 M1543 as PCI Master

The M1543 will assert a master abort due to DEVSELJ timeout. The M1543 acts as a PCI Master when an ISA or DMA master accesses the PCI memory. The M1543 provides an 8-byte bi-directional line buffer for ISA/DMA Master memory read from or write to PCI bus. The line buffer is used to isolate the ISA bus' slower devices from the PCI. Only an ISA/DMA master memory write or read cycle to PCI bus can be assembled/disassembled into line buffer. When line buffer is enabled, the ISA/DMA master can prefetch 2 Doublewords to the line buffer for read cycle. However, only 4 bytes are used in the buffer for write cycle.

In some cases, a strong ordering must be kept due to coherency problems, the line buffer will be disabled. When the line buffer is disabled, the reorder problem caused by assembly/disassembly will be avoided and guarantees read/write ordering.

3.3.2 Posted - Write Buffer Flush

Once an ISA/ DMA master begins a cycle on the ISA bus, the cycle cannot be backed off. It can only be held in wait states via IOCHRDY. In order to avoid deadlock situations, the PCI master post write buffer needs to be flushed before an ISA/ DMA master gets the ISA bus. When the ISA/DMA master owns the ISA bus, the post write buffer will be disabled.

3.3.3 Line Buffer Management

When an ISA/DMA master reads from PCI memory, the M1543 prefetches 8 bytes of data into the line buffer. If there is a read "hit" from the line buffer, the "hit" bytes are marked as invalid. There are 3 conditions why the line buffer needs prefetching :

1. Line buffer is "Empty" when read.
2. Read "Miss" to the line buffer.
3. Read the invalid byte from the line buffer.

When ISA/DMA master writes to PCI memory, the M1543 writes data to the line buffer. When the 4-byte buffer is full, it flushes data to the PCI bus. There are five conditions why the line buffer must flush its data :

1. Line buffer is full. Flush the line buffer and mark empty.
2. Write "Miss" to the partially full 4-byte line. Flush the partially full line and mark as empty, then write to the empty line.
3. Write "Hit" to the valid bytes. Flush it and mark as empty, then write to the empty line.
4. Read after write transaction and the line buffer is partially full. Flush the line buffer then do read prefetch.
5. Master has changed on DACKJ going inactive and last transaction is write and line buffer is partially full. Flush the line buffer.

3.4 Parity Support

As a master, the M1543 will generate address parity for read/write cycles, and data parity for write cycles. Parity check will work at read cycle. As a target, the M1543 will generate data parity for read cycles. PAR is even parity across AD[31:0] and CBEJ[3:0]. Even parity means that the number of 1's within the 36 bits and PAR is even. PAR has the same timing as AD[31:0] but delayed by one clock.

3.5 Address decoding

a. Positively decodes configuration cycle.
b. Positively or subtractively decodes interrupt acknowledge cycle.
c. Positively decodes on-chip IDE access cycle.
d. Positively decodes on-chip USB access cycle.
e. Positively or subtractively decodes internal I/O cycle (interrupt controller and timer counter).
f. Subtractively decodes DMA controller internal registers.
g. Others are subtractive decode.
h. When M1543 is programmed to be docking mode, all cycles are positively decoded including ISA-destinated cycles.

3.6 IDE Master Controller

a. Supports PCI bus mastering, transfer rate up to 132 Mbytes/sec. This significantly lightens the load of CPU work burden.
b. Supports IDE PIO modes 0, 1, 2, 3, 4 & 5 timing and multiword DMA modes 0,1,2 on enhanced IDE specifications. This chip is capable of accelerated PIO data transfers as well as acting as a PCI bus master on behalf of an IDE DMA slave device. The M1543 provides an interface for two dedicated IDE connectors.
c. Supports compatible and native PCI mode. Compatible mode is the default mode, native PCI mode will only be chosen by the BIOS.
d. 10 Doubleword FIFO for posted-write or read-ahead buffer for each channel (Total = 20 Doublewords). Each channel buffer is independent.
e. Programmable command and data transfer timing per drive for maximum flexibility. Operation of two hard disks is possible even if they have different PIO modes.
f. Supports concurrent operation on two ATA channels. M1543 simultaneously operates two drives.
g. Supports ATAPI CD-ROM concurrent operation. Simultaneous use of hard disks and CD-ROM is possible.
h. Dedicated ATA bus pins and dedicated buffers for each channel, no extra TTLs are needed.
i. Supports Ultra 33 high performance ATA bus for 33 Mbytes transfer rate.

3.7 Distributed DMA

The Distributed DMA Host Controller supported by M1543 provides one way to allow the separation of the slave DMA controllers in the hardware architecture, and yet allows the OS and application base to still utilize two legacy DMA controllers.

3.8 Serialized IRQ

The serialized IRQ supported by M1543 provides one pin named SERIRQ to generate IRQs event to Interrupt Controller from serialized IRQ protocol. The frame number can be programmed from 17 to 32. The Operation mode (quiet or continuous) and Start Frame Pulse width (4 to 8 pciclks) are also programmable.

3.9 Advanced Power Management

The M1543 Power Management Unit includes full ACPI compliance spec. and legacy power management including SMM, Stop clock control unit, APM, External SMI-switch control, Programmable counters for time-out event generation. M1543 can provide On (working)/ Sleeping (Power_on_suspend)/ Suspend_to_DRAM/ Suspend_to_Disk/ Soft_Off/ Mechanical_Off global system states to minimize the overall system power consumption. M1543 also provides an extra Standby state for monitoring over 16 peripheral devices activity. M1543 supports programmable Stop_Clock with throttle/ CLK_ON_STPCLK/CLK_OFF_STPCLK control for fitting the ACPI C0-C3 clock states. M1543 provides several hot plugging events detection and multiple external wake-up events for satisfying the notebook requirements. M1543 supports the battery, thermal detected logic and system/chip/devices power plane management logic. The M1543 provides full support for Advanced Configuration and Power Interface (ACPI), On-now technology and OS Directed Power Management (OSPM). M1543 also supports the legacy power management control, such as SMM and SMI features. The goal of the M1543 power management not only targets to the current desktop/ notebook satisfaction but also to the future OS driven flexible requirements.

3.10 System Management Bus (SMBus)

The M1543 SMBus has been designed based on :
System Management Bus Specification Rev 1.0
Smart Battery Data Specification Rev 1.0
Smart Battery Charger Specification Rev 1.0
System Management Bus BIOS Specification Rev 1.0
Smart Battery Selector Specification Rev 0.9

The System Management Bus (SMBus) host controller in M1543 supports the ability to communicate with power-related devices by SMBus protocol. It can be a master or slave on the SMBus, providing quick send byte/receive byte/ write byte/write word/read word/block read/block write command with clock synchronization and arbitration functions.

3.11 Universal Serial Bus (USB)

The M1543 USB is an implementation of the Universal Serial Bus (USB) 1.0 specification which contains PCI interface logic, Host Controller and an integrated Root Hub with two USB ports. For DOS compatibility, Keyboard and Mouse legacy are also supported.

3.12 Super I/O

The M1543 Super I/O incorporates two full-function universal asynchronous receiver/ transmitters (UARTs), a keyboard interface, a floppy disk controller (FDC) with data separator, parallel port, full range (A0-A15) address decoding for on-chip functions, and a configuration register.

The floppy disk controller is fully compatible with the industry-standard 765A and 82077SL architecture. It includes more advanced options such as a high performance data separator, extended track range to 4096, high performance power management, implied seek command, scan command, and supports both IBM and ISO 360K/1.2M/720K/1.44M/2.88M FDD formats. The UARTs are compatible with the NS16550. The parallel port, completely compatible with the IBM AT. The configuration register is one-byte wide and can be programmed via hardware or software. By controlling this register, the user can assign standard AT addresses and disable any major on-chip function (e.g., the FDC, either UART, or the parallel port) independent of the others. This allows for flexibility in system configuration when adapter cards contain duplicate functions.

The M1543 Super I/O provides support for the ISA Plug-and-Play standard and recommended functionality to support Windows 95. Through internal configuration registers, each of the Super I/O logic devices I/O address, DMA channel and IRQ channel may be programmed. There are 96 I/O address location options, 12 IRQ options, and 4 DMA channel options for each logical device.

Section 4: Configuration Registers

4.1 Register Description

4.1.1 PCI to ISA Bridge Configuration Space (IDSEL= AD18)

The indices before 40h are read-only.
All reserved bits are read as 0's

Index-Offset **Description**

Register Index : **01h-00h**
Register Name : **Vendor ID**
Default Value : 10B9h
Attribute : RO

Register Index : **03h-02h**
Register Name : **Device ID**
Default Value : 1533h
Attribute : RO

Register Index : **05h-04h**
Register Name : **Command Byte**
Default Value : 000Fh
Attribute : RO

Bit No.	Bit Function
15-5	Reserved. Read as 0's ;
4	Cacheing Command Enable (always '0');
3	Special cycle Enable (always '1');
2	Bus Master Enable (always '1');
1	Memory Space Enable (always '1');
0	I/O Space Enable (always '1');

Register Index : **07h-06h**
Register Name : **Status Byte**

Bit No.	Bit Function
15	Detected Parity Error. Always '0';
14	Signal System error. Always '0' ;
13	Receive Master Abort When M1543 as a master. This bit is set to a '1' when M1543 generates a transaction (except for Special Cycle) is terminated with master-abort. This is a read only bit and is cleared by writing a '1' to it.
12	Receive Target Abort When M1543 as a master. This bit is set to a '1' when M1543 encounters a target abort condition. This is a read only bit and is cleared by writing a '1' to it.
11	Signal Target Abort When M1543 as a slave. M1543 as a slave never generates a Target abort this bit is always 0.
10-9	M1543 DEVSELJ Timing This status of DEVSELJ decode timing as PCI spec. M1543 always generates DEVSELJ with medium timing Bit9='1',Bit10='0'.
8-0	Reserved. Read as 0's.

Register Index : **08h**
Register Name : **Revision ID**.
Default Value : 00h
Attribute : Read Only

Register Index : **0B-09h**
Register Name : **Class code**.
Default Value : 0Bh=06h,0Ah=01h,09h=00h.
Attribute : Read Only

Register Index **0D-0Ch**
Register Name : **Reserved**
Attribute :

Register Index **0Eh** bit7=0 always single-function chip.
Register Name : **Device Type**
Default Value : 00h
Attribute : Read Only

Register Index : **2Bh-0Fh**
Register Name : **Reserved**
Attribute :

Register Index **2Dh-2Ch**
Register Name : **Subsystem Vendor ID**
Default Value : 00h
Attribute : Read/Write

Register Index **2Fh-2Eh**
Register Name : **Subsystem ID**
Default Value : 00h
Attribute : Read/Write

Register Index : **3Fh-30h**
Register Name : **Reserved**
Attribute :

M1543 PCI INTERFACE CONFIGURATIONS.
Register Index : **40h**
Register Name : **PCI Control**
Default Value : 00h

Bit No.	Bit Function
7	Reserved.
6	Sound card I/O posted-write enable/disable. 0 : disable 1 : enable Note: 1. When enabling this bit, D2 of cfg. 40h should be enabled simultaneously. 2. This bit is a switch of cfg. 50h-53h sound card I/O post write. 3. This bit has no effect on internal I/O port, eg. 8254, 8259, 8237 ports.
5	Select ISA master to PCI Bus request method 0 : Bus request at each time ISA MASTER requests the bus 1 : Bus request only MASTER assert command
4	PCI and ISA concurrent mode enable/disable. 0 : disable 1 : enable
3	Delay transaction for PCI spec. 2.1 enable/disable. 0 : disable 1 : enable
2	PCI-to-ISA Posted Write Buffer Enable/Disable 0 : disable 1 : enable Note: This bit includes PCI to ISA Memory Post Write and I/O Post Write.
1	ISA Master Line Buffer Enable/Disable 0 : disable 1 : enable
0	DMA Line Buffer Enable/Disable 0 : disable 1 : enable

Register Index : **41h**
Default Value : 00h

Bit No.	Bit Function
7	PS/2 Keyboard present feature 0 : Without PS/2 keyboard (AT IRQ1) 1 : With PS/2 Keyboard Bit 7 is used to enable IRQ1 latch, when IRQ1 goes high. And IRQ1 will be released when read Port 60H. If '0', IRQ1 will be compatible to AT definition. If '1', IRQ1 will be compatible to PS/2 definition. This bit is also used to select AT/PS/2 internal Keyboard Controller.
6	PS/2 Mouse/AT Mouse select 0 : AT mouse 1 : With PS/2 mouse Bit 6 is used to enable IRQ12 latch, when IRQ12 goes high. And IRQ12 will be released when read Port 60H. If '0', IRQ12 will be compatible to AT definition. If '1', IRQ12 will be compatible to PS/2 definition.
5-2	I/O recovery period 0,0,0,0 : 0 us 0,0,0,1 : 0.25 us (2/ATCLK) 0,0,1,0 : 0.5 us (4/ATCLK) 0,0,1,1 : 0.75 us (6/ATCLK) 0,1,0,0 : 1 us (8/ATCLK) 0,1,0,1 : 1.25 us (10/ATCLK) 0,1,1,0 : 1.5 us (12/ATCLK) 0,1,1,1 : 1.75 us (14/ATCLK) 1,0,0,0 : 2 us (16/ATCLK) 1,0,0,1 : 2.25 us (18/ATCLK) 1,0,1,0 : 2.5 us (20/ATCLK) 1,0,1,1 : 2.75 us (22/ATCLK) 1,1,0,0 : 3 us (24/ATCLK) 1,1,0,1 : 3.25 us (26/ATCLK) 1,1,1,0 : 3.5 us (28/ATCLK) 1,1,1,1 : 3.75 us (30/ATCLK)
1	On-Chip I/O recovery 0 : disable on-chip I/O recovery 1 : enable on-chip I/O recovery Bit0 is used to enable ISA I/O recovery timer, Bit1 is used for M1543 internal I/O Port I/O recovery, but Bit0 must be 1 first.
0	ISA I/O recovery feature 0 : disable ISA I/O recovery 1 : enable ISA I/O recovery

Register Index : **42h**
Default Value : 00h

Bit No.	Bit Function
7	Configuration Port read data mask function. 0 : Normal I/O read/write 1 : Read from 40-FFh are all 0's
6	DMA High Page register Enable/Disable. 0 : disable. (24 bits addressing) 1 : enable. (32 bits addressing)
5	Reserved (must be 0).
4	Reserved (must be 0).
3	Decoupled refresh control. 0 : Normal refresh 1 : Decoupled refresh This bit is 0, Refresh Master will own ISA and PCI bus. When this bit is set to 1, Refresh master will only own ISA Bus.
2-0	ISA clock select. 000 : 7.16 MHz 001 : PCICLK/2 010 : PCICLK/3 011 : PCICLK/4 100 : PCICLK/5 101 : PCICLK/6 110 : reserved 111 : reserved

Register Index : **43h**
Register Name : **ISA Bus cycle control**
Default Value : 00h

Bit No.	Bit Function
7	Port-92H RC/GATEA20 Selection 0 : Disable Port-92H 1 : Enable Port-92H PORT-92H is used to start FAST RC.
6	Coprocessor interface This bit is used to support the coprocessor error reporting or as an external IRQ13 for pin XFERRJ. 0 : disable (Pin XFERRJ as XIRQ13; XIGNNEJ always 1) 1 : enable (Pin XFERRJ as XFERRJ)
5-4	ISA Refresh period setting 0,0 : 15 us refresh period 0,1 : 30 us 1,0 : 60 us 1,1 : 120 us
3-2	16-bit ISA memory command insert wait count 0,0 : normal 16-bit access 0,1 : Insert 1 wait 1,0 : insert 2 wait 1,1 : insert 3 wait
1-0	16-bit ISA I/O command insert wait count 0,0 : normal 16-bit access 0,1 : insert 1 wait 1,0 : Insert 2 wait 1,1 : insert 3 wait

Register Index : **44h**
Default Value : 00h

Bit No.	Bit Function
7	PCI soft reset control 0 : When CPU soft reset init., PCIRSTJ will not be active 1 : When CPU soft reset init., PCIRSTJ will be active
6	On chip I/O decode (except DMA I/O port is always subtractive) 0 : positive decode 1 : subtractive decode
5	Reserved. (must be '0')
4	On-chip IDE master Primary INTAJ level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip IDE master Primary INTAJ routing when native mode is enable. D3-2-1-0 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **45h**
Default Value : 00h

Bit No.	Bit Function
7	PCI interrupt polling mode enable/disable. 0 : disable. 1 : enable.
6	ROM chip select activated when accessing 62h and 66h port. 0 : disable 1 : enable If this bit is enabled, ROM chip select will be active when accessing 60,64,62,66h ports.
5	Reserved.
4	Reserved.
3	Delay transaction timeout counter enable/disable. 0 : disable. 1 : enable.
2	Reserved.
1	Distributed DMA enable/disable 0 : disable. 1 : enable.
0	Parity check enable/disable. 0 : disable. 1 : enable.

Register Index : **46h**
Register Name : **Reserved**

Register Index : **47h**
Register Name : **BIOS chip select control**
Default Value : 00h

Bit No.	Bit Function
7	SA16 inverter control 0 : Normal SA16 1 : Invert SA16 when ROM chip select active
6	Flash ROM read/write control (write protest) 0 : disable; ROM chip select will be active only in memory read cycle. 1 : enable; ROM chip select will be active in memory read/write cycle.
5	0 : disable 1 : enable; ROMKBCSJ will be active when access memory 000D0000-000DFFFF.
4-3	Share memory VGA BIOS region decode
4	0 : disable 1 : enable; ROMKBCSJ will be active when access memory 000C8000-000CFFFF.
3	0 : disable 1 : enable; ROMKBCSJ will be active when access memory 000C0000-000C7FFF.
2-1	Extended ROM region enable/disable
2	0 : disable; 1 : enable; ROMKBCSJ will be active when access memory FFFC0000-FFFDFFFF. This bit will enlarge the ROM size to 256 KB.
1	0 : disable; 1 : enable; ROMKBCSJ will be active when access memory FFFE0000-FFFEFFFF.
0	ROM size define for ROM chip select decode 0 : 64 KB (000F0000-000FFFFF, FFFF0000-FFFFFFFF) 1 : 128KB (000E0000-000EFFFF, 000F0000-000FFFFF, FFFF0000-FFFFFFFF).

Register Index : **48h**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-2 to ISA IRQ routing table Above Routing Table : D3-D0 or D7-D4 D3 D2 D1 D0 or D7 D6 D5 D4 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15 The BIOS should inhabit to set the reserved value. The reserved setting will disable the IRQ at the present design.
3-0	INT-1 to ISA IRQ routing table

Register Index : **49h**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-4 to ISA IRQ routing table
3-0	INT-3 to ISA IRQ routing table

Register Index : **4Ah**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-6 to ISA IRQ routing table
3-0	INT-5 to ISA IRQ routing table

Register Index : **4Bh**
Register Name : **PCI Interrupt to ISA IRQ routing table**
Default Value : 00h

Bit No.	Bit Function
7-4	INT-8 to ISA IRQ routing table
3-0	INT-7 to ISA IRQ routing table

Register Index : **4Ch**
Register Name : **PCI INT to ISA Level to Edge transfer**
Default Value : 00h

Bit No.	Bit Function
7	INT-8 0 : disable, PCI Level trigger INT will be bypassed as level trigger to M8259. 1 : enable, PCI Level trigger INT will be transformed to be Edge trigger to M8259.
6	INT-7
5	INT-6
4	INT-5
3	INT-4
2	INT-3
1	INT-2
0	INT-1

Index 48h to 4Ch are used to define PCI INT 8 channel's routing tables for ISA system. For PCI, INT is level, not edge trigger. 4Ch index is used to enable each INT channel from level to edge transfer.

Register Index : **4Dh**
Register Name : **MBIRQ0(SIRQI), MBIRQ1(SIRQII) Interrupt to ISA IRQ routing table**
Default Value : 00h
Before using this register, Index 58h bit1-0 must be programmed to be SIRQI and SIRQII function.

Bit No.	Bit Function
7-4 3-0	SIRQI to ISA IRQ routing table SIRQII to ISA IRQ routing table Above Routing Table : D3-D0 or D7-D4 D3 D2 D1 D0 or D7 D6 D5 D4 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15
	The BIOS should inhabit to set the reserved value.
	The reserved setting will disable the IRQ at the present design.

Register Index : **4Eh**
Register Name : **Reserved**

Register Index : **4Fh**
Register Name : **Reserved**

Register Index : **51h-50h**
Register Name : **I/O cycle posted-write first port definition**.
Default Value : 0000h

Bit No.	Bit Function
15	0 : disable 1 : enable
14-12	Reserved.
11-0	Define the sound card's first I/O port for post-write.

Register Index : **53h-52h**
Register Name : **I/O cycle posted-write second port definition**
Default Value : 0000h

Bit No.	Bit Function
15	I/O cycle posted-write second port definition 1 : enable 0 : disable
14	On-chip USB device enable/disable. 0 : enable. 1 : disable.
13-12	Reserved
11-0	I/O cycle posted-write second port definition define the sound card first I/O port for post-write.

Register Index : **54h**
Register Name : **Hardware setting status bits**
Attribute : Read only

Bit No.	Bit Function
7	PCSJ hardware setting status. 0 : Pull-low, POWER PC mode 1 : Pull-high, INTEL PC mode
6	XPHOLDJ hardware setting status. 0 : Pull-low, USB in test mode. (for test only) 1 : Pull-high, USB in normal mode.
5	Reserved.
4	SPLED hardware setting status. 0 : Pull-low, support 256KB ROM 1 : Pull-high, not support 256kB ROM
3	XDIR hardware setting status. 0 : Pull-low, Pentium Pro CPU is used. 1 : Pull-high, Pentium CPU is used.
2	TC hardware setting status. 0 : Pull-low, pins SD/GPIO[7:0] are SD[7:0], external LS245 is not required. 1 : Pull-high, pins SD/GPIO[7:0] are GPIO[7:0], external LS245 is required.
1	SPKR hardware setting status. 0 : Pull-low, internal Super I/O test mode is enabled. (for test only) 1 : Pull-high, internal Super I/O test mode is disabled.
0	ROMKBCSJ hardware setting status. 0 : Pull-low, chip test mode is enabled. (for test only) 1 : Pull-high, chip test mode is disabled.

Register Index : **57h-55h**
Register Name : **Programmable chip select (pin PCSJ) address define**.
Default Value : 000002h

Bit No.	Bit Function
23	Included Port 62h, 66h in for decode PCSJ enable/disable. 0 : disable; 1 : enable.
22	The chip select qualified by ISA Bus IOWJ enable/disable. 0 : disable; 1 : enable.
21	The chip select qualified by ISA Bus IORJ enable/disable. 0 : disable; 1 : enable.
20-16	Reserved.
15-2	Defines the programmable I/O port address A15-A2.
1-0	00 : compare A15-A2 for chip select signal PCSJ. (4 bytes) 01 : compare A15-A3 for chip select signal PCSJ. (8 bytes) 10 : disable. Chip select signal PCSJ is always inactive ('1'). 11 : Compare A15-A4 for chip select signal PCSJ. (16 bytes)

Register Index : **58h**
Register Name : **IDE interface control**
Default Value : 00h

Bit No.	Bit Function
7	Reserved. (must be '0')
6	On-chip IDE controller enable/disable 0 : disable 1 : enable
5-4	IDE IDSEL address when internal IDE is enable 00 : A27 (default) 01 : A26 10 : A25 11 : A24
3	IDE ATA Secondary signal bus pad control 0 : disable, i.e. tri-state the secondary channel pins 1 : enable, i.e. internal IDE controls it.
2	IDE ATA Primary signal bus pad control 0 : disable, i.e.tri-state the primary channel pins. 1 : enable, i.e. internal IDE controls it.
1-0	ATA bus IDE IRQ connection define (H/W connected on motherboard). Primary IRQ Secondary IRQ 00 : SIRQI SIRQII 01 : IRQ14 IRQ15 10 : IRQ14 SIRQII 11 : IRQ14 SIRQI **Note** : IDE IRQ Hardware Connect : 1. When SIRQI is selected as IDE IRQ input, the SIRQI routing table in cfg_4dh_d[3:0] should be disabled. 2. When SIRQII is selected as IDE IRQ input, the SIRQII routing table in cfg_4dh_d[7:4] should be disabled. 3. When IDE is enabled, "Primary" channel routing table is in cfg_44h_d[3:0]. 4. When IDE is enabled, "Secondary" channel routing table is in cfg_75h_d[3:0].

Register Index : **59h**
Register Name : **General Purpose input multiplexed pin(GPI) select**
Default Value : 00h
These pins will be power off when entering Suspend to DRAM or Suspend to Disk.

Bit No.	Bit Function
7-4	Reserved.
3	PCIREQJ/GPI[3] select: 0=PCIREQJ;1=GPI[3].
2	SERIRQ/GPI[2] select: 0=GPI[2];1=SERIRQ.
1	Reserved.
0	OVCRJ[0]/GPI[0] select: 0=OVCRJ[0];1=GPI[0].

Register Index : **5B-5Ah**
Register Name : **General Purpose Output multiplexed pin (GPO) select**.
Default Value : 0000h
These pins will be power off when entering Suspend to DRAM or Suspend to Disk.

Bit No.	Bit Function
15-10	Reserved.
9	SQWO/GPO[9] select: 0=SQWO;1=GPO[9].
8-4	Reserved.
3	PCI_STPJ/GPO[3] select: 0=PCI_STPJ;1=GPO[3].
2	CPU_STPJ/GPO[2] select: 0=CPU_STPJ;1=GPO[2].
1	ZZ/GPO[1] select: 0=ZZ; 1=GPO[1].
0	PCSJ/GPO[0] select: 0=PCSJ; 1=GPO[0].

Register Index : **5D-5Ch**
Default Value : 0000h

Bit No.	Bit Function
15-10	Reserved.
9	I/O group C positive decode enable/disable when Docking mode is enable. 0 : subtractive decode. 1 : positive decode.
8-7	Reserved.
6	Parallel I/O ports positive decode enable/disable when Docking mode is enable. 0 : subtractive decode. 1 : positive decode.
5	Keyboard I/O ports positive decode enable/disable when Docking mode is enable. 0 : subtractive decode. 1 : positive decode.
4	Serial I/O ports positive decode enable/disable when Docking mode is enable. 0 : subtractive decode. 1 : positive decode.
3	Floppy I/O ports positive decode enable/disable when Docking mode is enable. 0 : subtractive decode. 1 : positive decode.
2	Video I/O ports positive decode enable/disable when Docking mode is enable. 0 : subtractive decode. 1 : positive decode.
1	Audio I/O ports positive decode enable/disable when Docking mode is enable. 0 : subtractive decode. 1 : positive decode.
0	Docking positive decode mode enable/disable. 0 : disable. 1 : enable. When docking positive decode mode is enabled, all ports are positive decode.

Register Index : **5Eh**
Default Value : 00h

Bit	Description
7	Stop USB PCICLK when entering suspend mode enable/disable. 0 : disable. USB PCICLK is still running during suspend mode. 1 : enable. USB PCICLK is stopped during suspend mode.
6	Stop ISP DMACLK when entering suspend mode enable/disable. 0 : disable. ISP DMACLK is still running during suspend mode. 1 : enable. ISP DMACLK is stopped during suspend mode.
5	Stop ISP PCICLK when entering suspend mode enable/disable. 0 : disable. ISP PCICLK is still running during suspend mode. 1 : enable. ISP PCICLK is stopped during suspend mode.
4-0	Reserved (must be "00000").

Register Index : **5Fh**
Default Value : 00h

Bit	Description
7	Output SYSCLK is stopped during suspend mode enable/disable. 0 : disable. SYSCLK is still running during suspend mode. 1 : enable. SYSCLK is stopped during suspend mode
6	Internal KB clock is stopped during suspend mode enable/disable. 0 : disable. Internal Keyboard clock is still running during suspend mode. 1 : enable. Internal Keyboard clock is stopped during suspend mode.
5	The clock of AT CLOCK DIVIDER is stopped during suspend mode enable/disable. 0 : disable. 1 : enable. All AT clocks (including SYSCLK and KBCLK) are stopped during suspend mode.
4	The 14.318 Mhz clock of CLKRST circuit is stopped during suspend mode enable/disable. 0 : disable 1 : enable. The 119 Khz of M8254 and cold reset counter are stopped during suspend mode.
3	Bit 9-0 of PCI-to-ISA Bridge configuration Command Register 04h lock/unlock control. 0 : Lock (cannot read/write) 1 : Unlock (can read/write)
2	On-chip PCI PMU device enable/disable 0 : enable 1 : disable
1	The ROM area 4G-1 to 4G-16M (FF000000h-FFFFFFFFh) decode enable/disable. The XPCSJ must be pull-low for POWER PC mode. 0 : enable. When accessing this area, pin ROMKBCSJ will be active. 1 : disable.
0	On-chip PCI device INT routing outside for POWER PC enable/disable. 0 : disable. 1 : enable. On-chip IDE INTAJ output via INTBJ/S0 pin; On-chip IDE INTBJ output via INTCJ/S1 pin; On-chip USB INTAJ output via INTDJ/S2 pin; When this bit is enabled, the cfg. 45h bit7 must be '0';

Register Index : **6Bh-60h**
Register Name : **Reserved.**

Register Index : **6Ch** (deleted)

Register Index : **6Dh**
Default Value : 00h

Bit No.	Bit Function
7	Float ISA Output Pads When Entering Suspend Mode. 0 : floating 1 : driving
6	Reserved
5 (0)	Release PCI Bus During ISA DMA Master Cycle Retried by North Bridge 0: Do not release 1: Release This bit is used to control the PHOLDJ assertion when ISA DMA Master cycle has been retried by North Bridge. '0' means PHOLDJ will keep assertion and North Bridge cannot grant the PCI bus to another PCI Master. '1' means M1543 will deassert PHOLDJ and North Bridge can grant the PCI bus to another PCI Master. '1' is recommended.

4	Super I/O IR Mode Enable/Disable.
	0 : disable.SD/GPIO[2:0] is GPIO[2:0] when TC is pull-high.
	1 : enable.SD/GPIO[2:0] is used as FIR pins when TC is pull-high.
	IRRX input from SD_GPIO(2);
	FIR input/output via SD_GPIO(1);// future version
	IRTX output to SD_GPIO(0);

3-2	On-Chip Arbiter Priority Assignment. 00 : Rotate mode. ISA->USB->IDE->D_DMA->ISA.... 01 : Fixed mode. ISA is highest priority. If ISA is servicing, USB is highest priority for next arbitration. 10 : Fixed mode. USB is highest priority. USB->ISA->IDE->D_DMA. If USB is servicing, ISA is highest priority for next arbitration. 11 : Common Architecture mode and Rotate mode. ISA->USB->IDE->D_DMA->ISA....
1-0	Output Pins BIOSA17, BIOSA16 Mapping When E0000-EFFFF Region is Accessed and ROM 256KB Mode is Enabled. 00 : BIOSA17=1; BIOSA16=0 (default) 01 : BIOSA17=0; BIOSA16=1 1x : BIOSA17=0; BIOSA16=0

Register Index : **6Eh**
Register Name : **ISP shadow I/O port select**
Default Value : 00h
The following is preliminary index for accessing shadow ISP ports:

Bit No.	Bit Function
7-5	Select device D7D6D5 : 000 : reserved 001 : 8254 programmable timer 010 : master 8259 011 : slave 8259 100 : master 8237 101 : slave 8237 110 : reserved 111 : reserved
4-0	Select device's ports
	D4D3D2D1D0: (as below) << 8237 >> D4D3D2D1D0: 0 0 0 0 0 master-37 channel[0] Mode register 0 0 0 0 1 master-37 channel[1] Mode register 0 0 0 1 0 master-37 channel[2] Mode register 0 0 0 1 1 master-37 channel[3] Mode register 0 0 1 0 0 master-37 Request register & Mask register combined 0 0 1 0 1 master-37 channel[0] Base Address register Low byte 0 0 1 1 0 master-37 channel[0] Base Address register High byte 0 0 1 1 1 master-37 channel[0] Base Word Count register Low byte 0 1 0 0 0 master-37 channel[0] Base Word Count register High byte 0 1 0 0 1 master-37 channel[1] Base Address register Low byte 0 1 0 1 0 master-37 channel[1] Base Address register High byte 0 1 0 1 1 master-37 channel[1] Base Word Count register Low byte 0 1 1 0 0 master-37 channel[1] Base Word Count register High byte 0 1 1 0 1 master-37 channel[2] Base Address register Low byte 0 1 1 1 0 master-37 channel[2] Base Address register High byte 0 1 1 1 1 master-37 channel[2] Base Word Count register Low byte 1 0 0 0 0 master-37 channel[2] Base Word Count register High byte 1 0 0 0 1 master-37 channel[3] Base Address register Low byte 1 0 0 1 0 master-37 channel[3] Base Address register High byte 1 0 0 1 1 master-37 channel[3] Base Word Count register Low byte 1 0 1 0 0 master-37 channel[3] Base Word Count register High byte Others : reserved

Bit No.	Bit Function
	D4D3D2D1D0 : 0 0 0 0 0 slave-37 channel[0] Mode register 0 0 0 0 1 slave-37 channel[1] Mode register 0 0 0 1 0 slave-37 channel[2] Mode register 0 0 0 1 1 slave-37 channel[3] Mode register 0 0 1 0 0 slave-37 Request register & Mask register combined 0 0 1 0 1 slave-37 channel[0] Base Address register Low byte 0 0 1 1 0 slave-37 channel[0] Base Address register High byte 0 0 1 1 1 slave-37 channel[0] Base Word Count register Low byte 0 1 0 0 0 slave-37 channel[0] Base Word Count register High byte 0 1 0 0 1 slave-37 channel[1] Base Address register Low byte 0 1 0 1 0 slave-37 channel[1] Base Address register High byte 0 1 0 1 1 slave-37 channel[1] Base Word Count register Low byte 0 1 1 0 0 slave-37 channel[1] Base Word Count register High byte 0 1 1 0 1 slave-37 channel[2] Base Address register Low byte 0 1 1 1 0 slave-37 channel[2] Base Address register High byte 0 1 1 1 1 slave-37 channel[2] Base Word Count register Low byte 1 0 0 0 0 slave-37 channel[2] Base Word Count register High byte 1 0 0 0 1 slave-37 channel[3] Base Address register Low byte 1 0 0 1 0 slave-37 channel[3] Base Address register High byte 1 0 0 1 1 slave-37 channel[3] Base Word Count register Low byte 1 0 1 0 0 slave-37 channel[3] Base Word Count register High byte Others : reserved
	<< 8259 >> D4D3D2D1D0: 0 0 0 0 0 master-59 ICW1 0 0 0 0 1 master-59 ICW2 0 0 0 1 0 master-59 ICW3 0 0 0 1 1 master-59 ICW4 0 0 1 0 0 master-59 OCW1 0 0 1 0 1 master-59 reserved (OCW2) 0 0 1 1 0 master-59 OCW3 Others: reserved
	D4D3D2D1D0: 0 0 0 0 0 slave-59 ICW1 0 0 0 0 1 slave-59 ICW2 0 0 0 1 0 slave-59 ICW3 0 0 0 1 1 slave-59 ICW4 0 0 1 0 0 slave-59 OCW1 0 0 1 0 1 slave-59 reserved (OCW2) 0 0 1 1 0 slave-59 OCW3 Others: reserved
	<< 8254 >> D4D3D2D1D0: 0 0 0 0 0 Counter[0] Low byte 0 0 0 0 1 Counter[0] High byte 0 0 0 1 0 Counter[1] Low byte 0 0 0 1 1 Counter[1] High byte 0 0 1 0 0 Counter[2] Low byte 0 0 1 0 1 Counter[2] High byte Others: reserved

Register Index : **6Fh.**
Register Name : **ISP shadow I/O select port data**
Attribute : Read only

Register Index : **70h**
Register Name : **Serial IRQ (IRQSER) Control Register**
Default Value : 12h
Attribute : Read/Write

Bit No.	Bit Function
7	Serial IRQ (IRQSER) Enable/Disable 0 : Disable 1 : Enable
6	Stop Frame Pulse Width 0 : 2 PCICLKs (Quiet mode) 1 : 3 PCICLKs (Continuous mode)
5-2(0000)	Number of IRQ/Data Frames 0000 : 17 Slots 0001 : 18 Slots 0010 : 19 Slots 0011 : 20 Slots 0100 : 21 Slots (default) 0101 : 22 Slots 0110 : 23 Slots 0111 : 24 Slots 1000 : 25 Slots 1001 : 26 Slots 1010 : 27 Slots 1011 : 28 Slots 1100 : 29 Slots 1101 : 30 Slots 1110 : 31 Slots 1111 : 32 Slots
1-0(10)	Start Frame Pulse Width 00 : 4 PCICLKs 01 : 6 PCICLKs 10 : 8 PCICLKs (default) 11 : reserved

Register Index : **71h**
Register Name : **Distributed DMA Channel on PCI or ISA side.**
Default Value : 00h

Bit No.	Bit Function
7	DMA Channel 7 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
6	DMA Channel 6 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
5	DMA Channel 5 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
4	Reserved.
3	DMA Channel 3 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
2	DMA Channel 2 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
1	DMA Channel 1 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot
0	DMA Channel 0 0 : DMA Device on ISA Slot(default) 1 : DMA Device on PCI Slot

Register Index : **72h**
Register Name : **USB IDSEL mux select**
Default Value : 00h

Bit No.	Bit Function
7	Routing table IRQ output synchronization enable/disable 0 : disable (bypass) 1 : enable (sync by PCICLK)
6	USB PWRENJ output via pins GPIO[7] enable/disable. 0 : disable 1 : enable
5	Repeat Serial IRQ continuous mode enable/disable. 0 : disable. 1 : enable.
4	Reserved.
3-2	PMU IDSEL Address select. 00 : A28 (default) 01 : A29 10 : A14 11 : A15
1-0	USB IDSEL Address when internal USB is enabled. 00 : A31 (default) 01 : A30 10 : A13 11 : A12

Register Index : **73h**
Register Name : **Distributed DMA Base Address**
Default Value : 00h

Bit No.	Bit Function
7-0	Distributed DMA BASE Address

Register Index : **74h**
Default Value : 00h

Bit No.	Bit Function
7	IOCHRDY driven case during DMA cycle. 0 : IOCHRDY will be driven during DMA cycle 1 : IOCHRDY will not be driven during DMA cycle
6	M1543 ISA bridge Subsystem vendor ID and Subsystem ID (Offset 2F-2Ch). Read only control. 0 : Read/Write 1 : Read only
5	Reserved.
4	On-chip USB master INTAJ level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip USB master INTAJ routing table D3-2-1-0 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **75h**
Default Value : 00h

Bit No.	Bit Function
7-5	Reserved.
4	On-chip IDE master Secondary INTBJ level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip IDE master Secondary INTBJ routing when native mode is enable. D3 -2 -1 -0 0 0 0 0 : Disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **76h**
Default Value : 00h

Bit No.	Bit Function
7-5	Reserved.
4	On-chip PMU system control interrupt(SCI) level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip PMU system control interrupt(SCI) routing table D3 -2 -1 -0 0 0 0 0 : IRQ13 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **77h**
Default Value : 00h

Bit No.	Bit Function
7-5	Reserved.
4	On-chip SMB controller event interrupt level to edge transform enable/disable. 0 : disable. (bypass) 1 : enable. (level -> edge)
3-0	On-chip Smart Battery Bus (SMB) controller event interrupt routing table. D3 -2 -1 -0 0 0 0 0 : disable 0 0 0 1 : IRQ9 0 0 1 0 : IRQ3 0 0 1 1 : IRQ10 0 1 0 0 : IRQ4 0 1 0 1 : IRQ5 0 1 1 0 : IRQ7 0 1 1 1 : IRQ6 1 0 0 0 : IRQ1 1 0 0 1 : IRQ11 1 0 1 0 : reserved 1 0 1 1 : IRQ12 1 1 0 0 : reserved 1 1 0 1 : IRQ14 1 1 1 0 : reserved 1 1 1 1 : IRQ15

Register Index : **FF-78h**
Register Name : **Reserved**

4.1.2 IDE master configuration registers (IDSEL = AD27 (default) , AD26, AD25, AD24)

Byte Index	Definition	R/W	Expected Value
1, 0	Vender ID	R	10B9H
3, 2	Device ID	R	5229H
5, 4	Command	R/W	0000H
7, 6	Status	R/W	0280H
8	Revision ID	R	20H
B, A, 9	Class Code	R	0101FAH
0EH	Header Type	R	00H
13H-10H	Base Address Regs	R/W	000001F1H
17H-14H	Base Address Regs	R/W	000003F5H
1BH-18H	Base Address Regs	R/W	00000171H
1FH-1CH	Base Address Regs	R/W	00000375H
23H-20H	Base Address Regs	R/W	0000F001H
2CH	Subsystem Vendor ID	R	00000000H
3CH	Interrupt Line	R/W	00000000H
3DH	Interrupt Pin	R/W	00000001H
3EH	Min_Gnt	R	00000002H
3FH	Max_Lat	R	00000004H

Register Index : **4Dh**
Register Name : **Configuration register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Read Programming Interface Index 09h Class code bit 4-6 R/W or Read only. 0 : Read/Write 1 : Read Only
6-0	Reserved.

Register Index : **4Fh**
Register Name : **Configuration register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
5	0 : Default 1 : Master state machine resets when ATA command recommences.
4	0 : Default. 1 : FIFO reset when ATA command recommences.
3,1	When set as (0,0) FIFO threshold 0~3 (0,1) FIFO threshold 4~7 (1,0) FIFO threshold 8~11 (1,1) FIFO threshold 12~15

Register Index : **50h**
Register Name : **Configuration register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-6	Reserved.
5	Only decodes the third byte of BASE2 and BASE4 during native mode. 0 : All 4 bytes are master IDE's cycle. (default) 1 : Only the 3rd byte is master IDE's cycle.
4	Reserved.
3	CFG_BEJDEC. 0 : Decode 3F6H and 376H that only uses address. 1 : Use byte enable decoding.
2	Reserved.
1	Read programming interface Index 09h Class code bits 6-4. 0 : Programming interface bits 6-4 are reserved (always 0) 1 : Normal read (default)
0	Enable internal IDE function. 0 : disable(default) 1 : enable

Register Index : **51h**
Register Name : **Reset and Testing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	CFG_CHIPRST, chip reset Writing a '1' to this bit will reset the whole chip as hardware reset. It generates a one cycle pulse only.
6	CFG_SOFTRST, soft reset Writing a '1' to this bit will reset all the blocks except the configuration space. It generates a one cycle pulse only.
5	CFG_RSTCH2, soft reset Writing a '1' to this bit will reset the ATASTATE and AUTOPOL2. It generates a one cycle pulse only.
4	CFG_RSTCH1, soft reset Writing a '1' to this bit will reset the ATASTATE and AUTOPOL1. It generates a one cycle pulse only.
3	Reserved.
2	CFG_ATA_TEST, auto polling test mode enable 0 : disable(default) 1 : enable
1	CFG_LATEST, latency timer test mode enable 0 : disable(default) 1 : enable
0	CFG_FIFO_TEST, FIFO test mode enable 0 : disable(default) 1 : enable

Register Index : **52h**
Register Name : **CFG_USE_CMDT and Flexible Channel Setting**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Exchange the two hard drives 0: Channel one is Master IDE and channel two is (Default) Slave IDE when configuring the two channels to the same channel. 1: Channel two is Master IDE and channel one is Slave IDE when configuring the two channels to the same channel.
6	Configure the two channels to secondary channel 0: Supports two channel IDE controller (Default). One is primary channel and another is secondary channel. 1: The two channels belong to primary and each channel only supports one hard drive. One channel support Master drive and another is Slave drive. The two channels can be exchanged by Bit 7.
5	Configure the two channels to primary channel 0: Support two channel IDE controller (Default). One is primary channel and another is secondary channel 1: The two channels belong to primary and each channel only supports one hard drive. One channel support Master drive and another is Slave drive. The two channels can be exchanged by Bit 7.
4	Exchange the two channels 0: Channel one is primary channel (Default) and channel two is secondary channel. 1: Channel two is primary channel and channel one is secondary channel.
3-0	CFG_USE_CMDT bit 0 forces the drive 0 of primary channel to use command block timing register for data transfer bit 1 forces the drive 1 of primary channel to use command block timing register for data transfer bit 2 forces the drive 0 of secondary channel to use command block timing register for data transfer bit 3 forces the drive 1 of secondary channel to use command block timing register for data transfer

Register Index: **53h**
Attribute : Read/Write

Bit	Description
7	Sub_System Vendor ID accessible or not 0: Read/Write 1: Read Only
6-4	Reserved
3	Mask Base address during compatibility mode 0 : unmask 1 : mask (return to '00000000')
2	Reserved
1	Supports CD_ROM FIFO (PIO mode) 0: Disable (default) 1: Enable
0	Supports CD_ROM DMA mode 0: Disable (default) 1: Enable

Register Index : **54h**
Register Name : **FIFO threshold of primary channel drive 0 and drive 1**
Default Value : 55h
Default Value : Read/Write

Bit No.	Bit Function
7-6	Operation level. Defines the slave operation level of primary drive 1.
5-4	FIFO threshold register. Defines when to start master transaction of primary drive 1. 00 : 12 WORDs 01 : 13 WORDs 10 : 14 WORDs 11 : 15 WORDs
3-2	Operation level. Defines the slave operation level of primary drive 0.
1-0	FIFO threshold register. Defines when to start master transaction of primary drive 0. 00 : 12 WORDs 01 : 13 WORDs 10 : 14 WORDs 11 : 15 WORDs

Register Index : **55h**
Register Name : **FIFO threshold of secondary channel drive 0 and drive 1**
Default Value : 55h
Attribute : Read/Write

Bit No.	Bit Function
7-6	Operation level. Defines the slave operation level of secondary drive 1.
5-4	FIFO threshold register. Defines when to start master transaction of secondary drive 1. 00 : 12 WORDs 01 : 13 WORDs 10 : 14 WORDs 11 : 15 WORDs
3-2	Operation level. Defines the slave operation level of secondary drive 0.
1-0	FIFO threshold register. Defines when to start master transaction of secondary drive 0. 00 : 12 WORDs 01 : 13 WORDs 10 : 14 WORDs 11 : 15 WORDs

Note: Operation level defines the access mode of each device :
00 : Slave FIFO off mode
01 : Slave FIFO on mode
10 : Master DMA mode
11 : Master PIO mode

Register Index : **56h**
Register Name : **Ultra DMA /33 setting for Primary drive 0 and drive 1**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Enable Primary Device 1 for Ultra DMA/33 1: Enable 0: Disable
6-4	Ultra DMA/33 cycle time for Primary Device 1 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T
3	Enable Primary Device 0 for Ultra DMA/33 1: Enable 0: Disable
2-0	Ultra DMA/33 cycle time for Primary Device 0 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T

Register Index : **57h**
Register Name : **Ultra DMA /33 setting for Secondary drive 0 and drive 1**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Enable Secondary Device 1 for Ultra DMA/33 1: Enable 0: Disable
6-4	Ultra DMA/33 cycle time for Secondary Device 1 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T
3	Enable Secondary Device 0 for Ultra DMA/33 1: Enable 0: Disable
2-0	Ultra DMA/33 cycle time for Secondary Device 0 000 : 8T 001 : 1.5T 010 : 2T 011 : 3T 100 : 4T 101 : 2.5T 110 : 6T 111 : 3.5T

Register Index : **58h**
Register Name : **Primary channel address setup timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-3	Reserved
2-0	Address setup count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks

Register Index : **59h**
Register Name : **Primary channel command block timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Command active count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Command recovery count 0000 : 16 clks (Default) 0001 : 1 clks 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Ah**
Register Name : **Primary channel Drive 0 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clks 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Bh**
Register Name : **Primary channel Drive 1 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clks 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Ch**
Register Name : **Secondary channel address setup timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-3	Reserved
2-0	Address setup count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks

Register Index : **5Dh**
Register Name : **Secondary channel command block timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Command active count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Command recovery count 0000 : 16 clks (Default) 0001 : 1 clks 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Eh**
Register Name : **Secondary channel Drive 0 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clks 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **5Fh**
Register Name : **Secondary channel Drive 1 data read/write timing register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved
6-4	Data read/write active count 000 : 8 clks (Default) 001 : 1 clks 010 : 2 clks 011 : 3 clks 100 : 4 clks 101 : 5 clks 110 : 6 clks 111 : 7 clks
3-0	Data read/write recovery count 0000 : 16 clks (Default) 0001 : 1 clks 0010 : 2 clks 0011 : 3 clks 0100 : 4 clks 0101 : 5 clks 0110 : 6 clks 0111 : 7 clks 1000 : 8 clks 1001 : 9 clks 1010 : 10 clks 1011 : 11 clks 1100 : 12 clks 1101 : 13 clks 1110 : 14 clks 1111 : 15 clks

Register Index : **60-61h**
Register Name: **Master byte counter for each PRD table entry**
Default Value : 00h
Attribute : Read only

Register Index : **62h**
Register Name : **Latency timer of PCI interface**
Default Value : 00h
Attribute : Read only

Register Index : **63h**
Register Name : **Latency timer expire indicator**
Default Value : 01h
Attribute : Read only

Register Index : **64-65h**
Register Name : **Byte counter for counting in ATA state machine**
Default Value : 0002h
Attribute : Read only

Register Index : **66h**
Register Name : **Sector count counter for counting in ATA state machine**
Default Value : 00h
Attribute : Read only

Register Index : **67h**
Register Name : **Block size counter for counting in ATA state machine**
Default Value : 01h
Attribute : Read only

Register Index : **68h**
Register Name : **Block size register of device 0 on primary channel**
Default Value : 00h
Attribute : read only

Register Index : **69h**
Register Name : **Block size register of device 1 on primary channel**
Default Value 00h
Attribute : read only

Register Index : **6Ah**
Register Name : **Block size register of device 0 on secondary channel**
Default Value 00h
Attribute : Read only

Register Index : **6Bh**
Register Name : **Block size register of device 1 on secondary channel**
Default Value 00h
Attribute : Read only

Register Index : **6Ch**
Register Name : **Primary channel sector count register**
This register is the duplicate of 1F2
Default Value : 00h
Attribute : Read only

Register Index : **6Dh**
Register Name : **Secondary channel sector count register**
This register is the duplicate of 172
Default Value : 00h
Attribute : Read only

Register Index : **6Eh**
Register Name : **Primary channel command register**
This register is the duplicate of 1F7
Default Value: 00h
Attribute : Read only

Register Index : **6Fh**
Register Name : **Secondary channel command register**
This register is the duplicate of 177
Default Value : 00h
Attribute : Read only

Register Index : **70h**
Register Name : **Primary channel byte count low register**.
This register is the duplicate of 1F4
Default Value : 00h
Attribute : Read only

Register Index : **71h**
Register Name : **Primary channel byte count high register**.
This register is the duplicate of 1F5
Default value : 00h
Attribute : Read only

Register Index : **72h**
Register Name : **Secondary channel byte count low register**
This register is the duplicate of 174
Default value : 00h
Attribute : Read only

Register Index : **73h**
Register Name : **Secondary channel byte count high register**
This register is the duplicate of 175
Default Value : 00h
Attribute : Read only

Register Index : **74h**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7	FIFO_OVERRD '1' means error condition occurred that FIFO is over read. This bit must be cleared by reset.
6	FIFO_OVERWR '1' means error condition occurred that FIFO is over written. This bit must be cleared by reset.
5-0	FIFO_FLAG Indicates how many words are in FIFO currently. It is binary coded.

Register Index : **75h**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
3	Secondary channel drive select (the duplicate of 176 bit 4) 0 : select drive 2 1 : select drive 3
2	Primary channel drive select (the duplicate of 1F6 bit 4) 0 : select drive 0 1 : select drive 1
1	Secondary channel interrupt status 0 : no interrupt pending 1 : interrupt pending
0	Primary channel interrupt status 0 : no interrupt pending 1 : interrupt pending

Register Index : **76h**
Register Name :
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
6-4	Secondary channel's status D4 - error D5 - DRQ D6 - busy
2-0	Primary channel's status D0 - error D1 - DRQ D2 - busy

Register Index : **78h**
Register Name :
Default Value : 21h
Attribute : Read/Write

Bit No.	Bit Function
7-0	IDE clock's frequency (default value is 33 = 21H)

4.1.3 USB PCI Configuration Register (IDSEL = AD31(default), AD30, AD13, AD12)

Register Index : **01h-00h**
Register Name : **Vendor ID Register**
Default Value : 10B9h
Attribute : Read only

Bit No.	Bit Function
15-0	This is a 16-bit value assigned to Acer Labs Inc. This register is combined with 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Index : **03h-02h**
Register Name : **Device ID Register**
Default Value : 5237h
Attribute : Read only

Bit No.	Bit Function
15-0	This register holds a unique 16-bit value assigned to a device, and combined with the vendor ID, it identifies any PCI device.

Register Index **05h-04h**
Register Name : **Command Register**
Default Value 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-10(0h)	Reserved. These bits are always 0.
9(0b)	Back to Back enable. M1543's USB only acts as a master to a single device, so this functionality is not needed. This bit is always 0.
8(0b)	Enable the SERRJ driver When this bit is set, M1543's USB will enable SERRJ output driver. This bit is reset to 0 and will set to 1 when it detects an address parity error. SERRJ is not asserted if this bit is 0.
7(0b)	Wait Cycle Control - M1543's USB does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.
6(0b)	Respond to Parity Errors If set to 1, M1543's USB will assert PERRJ when it is the agent receiving data AND it detects a data parity error. PERRJ is not asserted if this bit is 0.
5(0b)	Enable VGA Palette Snooping This bit is always 0.
4(0b)	Memory Write and Invalidate command If set to 1, M1543's USB is enabled to run Memory Write and Invalidate commands. The Memory Write and Invalidate Command will only occur if the cacheline size is set to 32 bytes and the memory write is exactly one cacheline.
3(0b)	Enable Special Cycle M1543's USB does not run special cycles on PCI. This bit is always 0.
2(0b)	Enable PCI Master If set to 1, M1543's USB is enabled to run PCI Master cycles.
1(0b)	Enable Response to Memory Access If set to 1, M1543's USB is enabled to respond as a target to memory cycles.
0(0b)	Enable Response to I/O Access If set to 1, M1543's USB is enabled to respond as a target to I/O cycles.

Register Index **07h-06h**
Register Name : **Status Register**
Default Value : 0280h
Attribute : Read only, Write clear

Bit No.	Bit Function
15(0b)	Detected Parity Error. This bit is set by M1543's USB to 1 whenever it detects a parity error, even if the Respond to Parity Errors bit (command register, bit 6) is disabled. This bit is cleared (reset to 0) by writing a 1 to it.
14(0b)	SERRJ Status. This bit is set by M1543's USB to 1 whenever it detects a PCI address parity error. This bit is cleared (reset to 0) by writing a 1 to it.
13(0b)	Received Master Abort Status. This bit is set to 1 when M1543's USB, acting as a PCI master, aborts a PCI bus memory cycle. This bit is cleared (reset to 0) by writing a 1 to it.
12(0b)	Received Target Abort Status. This bit is set to 1 when a M1543's USB generated PCI cycle (M1543's USB is the PCI master) is aborted by a PCI target. This bit is cleared (reset to 0) by writing a 1 to it.
11(0b)	Sent Target Abort Status. This bit is set to 1 when M1543's USB signals target abort. This bit is cleared (reset to 0) by writing a 1 to it.
10-9(01b)	DEVSELJ timing Read only bits indicating DEVSELJ timing when performing a positive decode. 00 : Fast 01 : Medium 10 : Slow Since DEVSELJ is asserted by M1543's USB to meet the medium timing, these bits are encoded as 01b.
8(0b)	Data Parity Reported. Set to 1 if the Respond to Parity Error bit (Command Register bit 6) is set, and M1543's USB detects PERRJ asserted while acting as PCI master (whether PERRJ was driven by M1543's USB or not).
7(1b)	Fast Back-to-Back Capable. M1543's USB does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6-0(0h)	Reserved. These bits are always 0.

Register Index : **08h**
Register Name : **Revision ID Register**
Default Value : 03h
Attribute : Read only

Bit No.	Bit Function
7-0(03h)	Functional Revision Level (00000011b)

Register Index **0B-09h**
Register Name : **Class Code Register**
Default Value 0C0310h
Attribute : Read only

Bit No.	Bit Function
23-0	This register identifies the generic function of M1543's USB the specific register level programming interface. The Base Class is 0Ch (Serial Bus Controller). The SubClass is 03h (Universal Serial Bus). The Programming Interface is 10h (OpenHCI).

Register Index : **0Ch**
Register Name : **Cache Line Size**
Default Value 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0(0h)	This register identifies the system cacheline size in units of 32-bit words. M1543's USB will only store the value of bit 3 in this register since the cacheline size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.

Register Index : **0Dh**
Register Name : **Latency Timer**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0(0h)	This register identifies the value of latency timer in PCI clocks for PCI bus master cycles.

Register Index : **0Eh**
Register Name : **Header Type Register**
Default Value 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register identifies the type of predefined header in the configuration space. Since M1543's USB is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.

Register Index : **0Fh**
Register Name : **BIST**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register identifies the control and status of Built In Self Test. M1543's USB does not implement BIST, so this register is read only.

Register Index : **13-10h**
Register Name : **Base Address Register**
Default Value : 00000000h
Attribute : Read/Write

Bit No.	Bit Function
31-12(0h)	Base Address. POST writes the value of the memory base address to this register.
11-4(0h)	Always 0. Indicates a 4K byte address range is requested
3(0b)	Always 0. Indicates there is no support for prefetchable memory.
2-1(0h)	Always 0. Indicates that the base register is 32-bit wide and can be placed anywhere in 32-bit memory space.
0(0b)	Always 0. Indicates that the operational registers are mapped into memory space.

Register Index: **2Dh-02Ch**
Register Name: **Subsystem Vendor ID**
Attribute: Read/Write
Default Value: 0000h

Bit	Bit Function
15-0	If the Test Mode Register (index 40h) D20=0, then this register can Read/Write. Else, this register is Read-Only.

Register Index : **2Fh-02Eh**
Register Name : **Subsystem ID**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-0	If the Test Mode Register (index 40h) D20=0, then this register can be Read/Write. Else, this register is Read-Only.

Register Index : **3Ch**
Register Name : **Interrupt Line Register**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0(0h)	This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to M1543's USB.

Register Index : **3Dh**
Register Name : **Interrupt Pin Register**
Default Value : 01h
Attribute : Read only

Bit No.	Bit Function
7-0(01h)	This register identifies which interrupt pin a device uses. Since M1543's USB uses INTAJ, this value is set to 01h.

Register Index **3Eh**
Register Name : **Min Gnt Register**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register specifies the desired settings for how long a burst M1543's USB needs assuming a clock rate of 33 Mhz. The value specifies a period of time in units of 1/4 microsecond.

Register Index **3Fh**
Register Name : **Max Lat Register**
Default Value : 00h
Attribute : Read only

Bit No.	Bit Function
7-0(0h)	This register specifies the desired settings for how often M1543's USB needs access to the PCI bus assuming a clock rate of 33 Mhz. The value specifies a period of time in units of 1/4 microsecond.

Register Index: **43h-040h**
Register Name: **Test Mode Register**
Attribute: Read/Write
Default Value: 00000000h

Bit	Bit Function
31-21	Reserved. Must always write 0's.
20	Subsystem/Vendor ID (index 2Fh-02Ch) lock bit. 0 : Index 2Fh-02Ch can Read/Write. 1 : Index 2Fh-02Ch is Read-Only.
19-0	Reserved. Must always write 0's.

4.1.4 PMU Configuration Registers Description (IDSEL=AD28(default), AD29, AD14, AD15)

All reserved bits are read as 0's

Index-Offset Description
Register Index : **01h-00h**
Register Name : **Vendor ID**
Attribute : Read Only
Default Value : 10B9h

Register Index : **03h-02h**
Register Name : **Device ID**
Attribute : Read Only
Default Value : 7101h

Register Index : **05h-004h**
Register Name : **Command Byte**
Attribute : Read Only
Default Value : 0000h

Bit	Description
15-5	Reserved. Read as 0's.
4	Cacheing Command Enable (always '0').
3	Special cycle Enable (always '0').
2	Bus Master Enable (always '0').
1	Memory Space Enable (always '0').
0	I/O Space Enable (R/W). This bit controls the PMU I/O and SMB I/O space registers. The Base address I/O (CFG_10-17) must be programmed before this bit is set.

Register Index : **07h-006h**
Register Name : **Status Byte**

Bit	Description
15	Detected Parity Error. Always '0'.
14	Signal System error. Always '0'.
13	Receive Master Abort When PMU as a master. (Not Implemented, always '0').
12	Receive Target Abort When PMU as a master. (Not Implemented, always '0').
11	Signal Target Abort When PMU as a slave. (Not Implemented, always '0').
10-9	PMU DEVSELJ Timing. This status of DEVSELJ decode timing as PCI spec. PMU always generates DEVSELJ with medium timing Bit9='1', Bit10='0'.
8-0	Reserved. Read as 0's.

Register Index : **08h**
Register Name : **Revision ID.**
Attribute : Read Only
Default Value : 00h

Register Index : **0B-009h**
Register Name : **Class code.** TBD
Attribute : Read Only

Register Index : **0D-00Ch**
Register Name : **Reserved**

Register Index : **0Eh**
Register Name : **Device Type**
Attribute : Read Only
Default Value : (00h) bit7=0 always single-function chip.

Register Index : **13h-010h**
Register Name : **Power Management I/O Base Address**
Default Value : 00000001h

Bit	Description
31-16	Reserved. Must be written as 0000h.
15-6	Corresponds to PMU I/O start address AD[15:6]. (64Bytes size).
5-1	Reserved. Read as 0's.
0	This bit is always '1', the PMU I/O base address in this register is indicated.

Register Index : **17h-014h**
Register Name : **SMB I/O Base Address**
Default Value : 00000001h

Bit	Description
31-16	Reserved. Must be written as 0000h.
15-5	Corresponds to SMB I/O start address AD[15:5]. (32Bytes size).
4-1	Reserved. Read as 0's.
0	This bit is always '1', the SMB I/O base address in this register is indicated.

Register Index : **2Bh-00Fh**
Register Name : **Reserved**

Register Index : **2Dh-02Ch**
Register Name : **Subsystem Vendor ID**
Attribute : Read/Write

Register Index : **2Fh-02Eh**
Register Name : **Subsystem ID**
Attribute : Read/Write

Register Index : **3Fh-030h**
Register Name : **Reserved**

Note: There are common status bits for ACPI and Legacy. Including ACPI released SMI.
Note: There are common enable/disable status bits for ACPI and Legacy. Including 4-resume GPSWs, HOTKEY, DOCK, COVSW, RTC, PWRBTN, RINGIN, USB, THERMJ, Thermal overide and BUS Master.

Register Index : **41h-40h**
Register Name : **SMI enable when ON to Green**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-13	Reserved.
12	Soft SMI, caused by writing IO port 0B1h.
11-5	Reserved.
4	APM timer A timeout SMI.
3	RTC SMI, caused by assertion of IRQ8I.
2	PWRBNJ (Power Button) SMI.
1	Display timer timeout SMI.
0	Standby timer timeout SMI.

Register Index : **43h-042h**
Register Name : **SMI status when ON to Green**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-13	Reserved.
12	Soft SMI, caused by writing IO port 0B1h.
11-5	Reserved.
4	APM timer A timeout SMI.
3	RTC SMI, caused by assertion of IRQ8I.
2	PWRBNJ (Power Button) SMI.
1	Display timer timeout SMI.
0	Standby timer timeout SMI.

Register Index : **46h-044h**
Register Name : **SMI enable when Wake Up.**
Attribute : Read/Write
Default Value : 200000h

Bit	Description
23-21	Reserved.
20	SIRQ access SMI.
19	SMB bus SMI.
18-16	Reserved.
15	I/O group C I/O access SMI.
14-13	Reserved.
12	Parallel Port I/O access SMI.
11	Keyboard I/O access SMI.
10	Serial I/O access SMI.
9	Flopy I/O access SMI.
8	Video I/O access SMI.
7	Audio I/O access SMI.
6	Secondary Driver I/O access SMI.
5	Primary Driver I/O access SMI.
4	Modem RING IN SMI.
3	BUS_Master active SMI.
2	USB access SMI.
1	Display timeout activity SMI.
0	Standby to ON SMI.

Register Index : **47h**
Register Name : **Reserved**.

Register Index : **4Ah-048h**
Register Name : **SMI status when Wake Up.**
Attribute : Read/Write
Default Value : 000000h

Bit	Description
23-22	Reserved.
21	USB bus SMI status. This bit is set when USB needs CPU service.
20	SIRQ access status.
19	SMB bus status.
18-16	Reserved.
15	IO group C I/O access status.
14-13	Reserved.
12	Parallel Port I/O access status.
11	Keyboard I/O access status.
10	Serial I/O access status.
9	Flopy I/O access status.
8	Video I/O access status.
7	Audio I/O access status.
6	Secondary Driver I/O access status.
5	Primary Driver I/O access status.
4	Modem RING IN status.
3	BUS_Master status.
2	USB access status. This bit is set when USB bus is busy.
1	Display timeout activity status.
0	Standby to ON status.

Register Index : **4Bh**
Register Name : **Reserved**.

Register Index : **4Dh-04Ch**
Register Name : **Enable of External Switch SMI.**
Attribute : Read/Write
Default Value : 0000h

Bit	Description
15-9	Reserved.
8	THERMALJ high/low toggle SMI.
7-3	Reserved.
2	DOCKJ in/out SMI.
1	Reserved.
0	AC Power in/out SMI.

Register Index : **4Fh-04Eh**
Attribute : Read/Write
Default Value : 0000h

Status of External Switches' SMI.

Bit	Description
15-9	Reserved.
8	THERMALJ high/low toggle status.
7-3	Reserved.
2	DOCKJ in/out status.
1	Reserved.
0	AC Power in/out status.

Register Index : **51h-050h**
Register Name : **Reserved**

Register Index : **53h-052h**
Register Name : **Reserved**

Register Index : **54h**
Register Name : **Standby timer**.
Default Value : 00h
Attribute : Read/Write
Generate Standby timer timeout SMI when it is timeout and be reset by the Standby monitor events.
Generate Standby to On SMI when the Standby monitor events occurs after timeout. The monitored events are selected at offset 060h-063h.

Bit	Description
7-0	Count. (=0, when disabled)(timebase = 1min)

Register Index : **55h**
Register Name : **APM timer A**
Default Value : 00h
Attribute : Read/Write
Generate APM timer A timeout SMI and stop when timeout. If in repeat mode, timer will be reset to count again after timeout.

Bit	Description
7	Reserved
6	Repeat mode
5-4	Timebase of APM timer A. 00 : 1ms. 01 : 1sec. 10 : 1min. 11 : reserved.
3-0	Count. (=0, when disabled)

Register Index : **56h**
Register Name : **Reserved.**

Register Index : **57h**
Register Name : **Reserved.**

Register Index : **58h**
Register Name : **Reserved**

Register Index : **59h**
Register Name : **Global Display timer**.
Default Value : 00h
Attribute : Read/Write
Generate Display timer timeout SMI when it is timeout and be reset by the Display monitor events.
Generate Display timeout activity SMI when the Display monitor events occurs after timeout. The monitored events are selected at offset 064h-065h.

Bit	Description
7-5	Reserved.
4	Timebase of Display timer. 0 : 5sec. 1 : 1min.
3-0	Count. (=0, when disabled)

Register Index : **5Ah**
Register Name : **Reserved**

Register Index : **5Bh**

Bit No.	Description
7	Reserved.
6	Enable/disable break event reset throttle when clock is high. 0 : enable 1 : disable
5	Select throttle period. 0 : Throttle period is 256 µs. 1 : Throttle period is 8 µs.
4	Bit 31-5 of ACPI P_CNTRL register lock/unlock control 0 : unlock (can read/write) 1 : lock (cannot read/write)
3	Enable/disable break event when throttle clock is low. 0 : enable 1 : disable.
2	SMB I/O base address register control. 0 : Read/Write 1 : Read Only and always '0'.
1	ACPI I/O base address register control. 0 : Read/Write 1 : Read Only and always '0'.
0	Self Refresh during STPCLK mode enable/disable. 0 : enable 1 : disable

Register Index : **5Fh-5Ch**
Register Name : **Reserved**

Register Index : **063h-060h**
Register Name : **Enable/disable systems events monitored by Standby timer**.
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-27	Reserved.
26	BUS_ACT detected.
25	PCI_REQJ or PHOLDJ asserted.
24	IRQ3-7, IRQ9-15, NMI, INIT or SMIJ asserted.
23	IRQ1 or IRQ12 asserted.
22	IRQ0.
21	PWRBTNJ (Power Button).
20	USB.
19-17	Reserved.
16	I/O group C.
15-13	Reserved.
12	Memory Group A.
11-10	Reserved.
9	Modem RING IN.
8	RTC.
7	Parallel Ports.
6	Keyboard.
5	Serial I/O.
4	Floppy.
3	Video.
2	Audio.
1	Secondary HDD.
0	Primary HDD.

Register Index : **65h-064h**
Register Name : **Enable/disable Display events monitored by Display timer**.
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-13	Reserved.
12	I/O group C.
11-9	Reserved.
8	Memory Group A.
7	Parallel Ports.
6	Keyboard.
5	Serial I/O.
4	Floppy.
3	Video.
2	Audio.
1	Secondary HDD.
0	Primary HDD.

Register Index : **67h-066h**
Default Value : **Reserved**

Register Index : **68h**
Register Name : **Activity Select.**
Default Value : 00h
Attribute : Read/Write
Select the IO ports of parallel port and FDD to be monitored.

Bit	Description
7-3	Reserved.
2-1	Select DRQ of Parallel Port event. 00 : DRQ0. 01 : DRQ1. 10 : DRQ3. 11 : reserved.
0	I/O port of FDD port 0 : 3F0h-3F7h. 1 : 370h-377h.

Register Index : **6Bh-069h**
Register Name : **Reserved**

Register Index : **6Fh-06Ch**
Register Name : **Enable/disable of event detected. (Part I)**
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-29	Reserved.
28	Keyboard event detect IRQ12.
27	Keyboard event detect IRQ1.
26	Floppy event detect DRQ2.
25	Video event detect Graphic IO.
24	Video event detect VCSJ pin.
23	Video event detect A-B pages.
22	Reserved.
21	Audio event detect DRQ7.
20	Audio event detect DRQ6.
19	Audio event detect DRQ5.
18	Audio event detect DRQ3.
17	Audio event detect DRQ1.
16	Audio event detect DRQ0.
15-12	I/O port of MS_Sound port.
15 14 13 12	Audio event detect F40h-F47h. Audio event detect E80h-E87h. Audio event detect 604h-60Bh. Audio event detect 530h-537h.
11-8	I/O port of SoundB-8/16 port.
11 10 9 8	Audio event detect 280h-293h. Audio event detect 260h-273h. Audio event detect 240h-253h. Audio event detect 220h-233h.
7-4	I/O port of MIDI port.
7 6 5 4	Audio event detect 330h-333h. Audio event detect 320h-323h. Audio event detect 310h-313h. Audio event detect 300h-303h.
3	Audio event detect ADLIB port, 338h-33Bh.
2	Audio event detect GAME port, 200h-207h.
1	Second drive event detect SDRQ.
0	Primary drive event detect PDRQ.

Register Index : **071h-070h**
Register Name : **Enable/disable of event detected. (Part II)**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-14	Reserved.
13-8	Select I/O port for Parallel Port event.
13	IOGPC detect I/O Group range C.
12	IOGPC detect 62h, 66h.
11	Parallel Port event detect DRQ0,1,3.
10	Parallel Port event detect 3BCh-3BEh.
9	Parallel Port event detect 278h-27Fh.
8	Parallel Port event detect 378h-37Fh.
7-0	Select I/O port for Serial port event.
7	Serial Port event detect 338h-33Fh.
6	Serial Port event detect 238h-23Fh.
5	Serial Port event detect 228h-22Fh.
4	Serial Port event detect 220h-227h.
3	Serial Port event detect 2E8h-2EFh.
2	Serial Port event detect 3E8h-3EFh.
1	Serial Port event detect 2F8h-2FFh.
0	Serial Port event detect 3F8h-3FFh.

Register Index : **073h-072h**
Register Name : **Enable/disable of event detected. (Part III)**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-4	Reserved.
3	Video detect GPI(3).
2	Audio detect GPI(2).
1	Reserved.
0	Primary HDD detect GPI(0).

Register Index : **074h**
Register Name : **System wake up status.**
Default Value : 00h
Attribute : Read/Write

The status is set when the occurrence of the corresponding event causes a StandBy to On SMI.

Bit	Description
7-6	Reserved.
5	System wake up by RTC(IRQ8J).
4	System wake up by PWRBNJ(Power Button).
3-2	Reserved.
1	System wake up by RING IN.
0	System wake up by DRQ2.

Register Index : **075h**
Register Name : **Time interval to measure Bus activity.**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-0	Count. (timebase = PCICLK).

Register Index : **076h**
Register Name : **Threshold number of TRDYJ detected in the time interval**
Default Value : 00h
Attribute : Read/Write
If the detected number is larger than the threshold number in the time interval as set at offset 75h. Then, an BUS_ACT activity event will be generated.

Bit	Description
7	Reserved.
6	Enable/disable BUS_ACT
5-0	Threshold

Register Index : **077h**
Register Name : **SMI control register (SMI_CNTL)**
Default Value : 00h
Attribute : Read/Write
Note: Only level SMI is generated.

Bit	Description
7	Select ACPI mode or M7101 mode. 0 : ACPI mode, status bit is set as soon as event occurs no matter whether the SMI is enabled or not. 1 : M7101 mode, status bit is set if and only if both events occur and the SMI is enabled.
6	SMI acknowledge control 0 : SMIACK deasserted. 1 : SMIACK asserted.
5	Clear both ACPI and Legacy status. 0 : Clear status bits will reset both ACPI and Legacy status. 1 : Clear status bits only one side.
4	Read/write clear SMI. 0 : The status bit of all status registers can only be cleared by writing '1' to it. 1 : Reading the status registers will clear the registers also.
3	Enable/disable SMI. Decides whether to generate SMI or not.
2	Enable/disable delayed Soft SMI.
1-0	SMI delay time. For AC Power, EXTSW, Cover Switch, CRT, SETUP, HOTKEY, DOCK, EJECT and Soft SMI (option). When the above SMI events occurs, SMI will be generated after the delay timer's timeout. Any monitored events set in standby monitor event en/disable register will reset this timer and delay the SMI again. Refer to Index 0D8h. 00 : no delay. 01 : 125ms. 10 : 250ms. 11 : 500ms.

*Clock management
Register Index : **079h-078h**
Register Name : **PLL timer setting**.
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-12	Reserved.
11-9	Selection of switching time of SUSPEND to NORMAL. When system switches from SUSPEND to NORMAL, the XSTPCLKJ control signal can not deassert until the refresh circuit is switched to normal refresh. 000 : 0 ms. 001 : 128 µs. 010 : 256 µs. 011 : 512 µs. 100 : 1 ms. 101 : 2 ms. 110 : 4 ms. 111 : 8 ms.
8-6	Selection of switching time of NORMAL to SUSPEND. When system switches from NORMAL to SUSPEND, the XOFF_PWR1 signal cannot assert until the refresh circuit is switched to suspend refresh. 000 : 0 ms. 001 : 128 µs. 010 : 256 µs. 011 : 512 µs. 100 : 1 ms. 101 : 2 ms. 110 : 4 ms. 111 : 8 ms.
5-3	Selection of CPU PLL time. When CPU is from STPCLK to STPGNT, XSTPCLKJ signal should delay for a period of time to deassert for the stability of internal clock of CPU. 000 : 0 ms. 001 : 0.25 ms. 010 : 0.50 ms. 011 : 1 ms. 100 : 2 ms. 101 : 4 ms. 110 : 8 ms. 111 : 16 ms.
2-0	Selection of clock generator PLL time. When clock generator changes from off to on, XCPU_STPJ and XPCI_STPJ signals should delay for a period of time to deassert for the stability of clock when resumed from SLEEP. 000 : 0 ms. 001 : 1 ms. 010 : 2 ms. 011 : 4 ms. 100 : 8 ms. 101 : 16 ms. 110 : 32 ms. 111 : 64 ms.

Register Index : **07Ah**
Register Name : **Slowdown and AMSTATE control**
Default Value : 00h
Attribute : Read/Write
Transition of D0 will assert STPCLKJ first and then change SLOWDOWN after the STPGNT cycle is detected. STPCLKJ will deassert after the CPU PLL time. If D1 is set, AMSTATJ will assert after the HALT cycle detected.

Note : SLOWDOWN and AMSTATJ always synchronize by rising edge of PCICLK.

Bit	Description
7-2	Reserved.
1	Enable/disable AMSTATE.
0	Reserved.

Register Index : **07Bh**
Register Name : **STPCLKJ control**
Default Value : 00h
Attribute : Read/Write.

Bit	Description
7-6	Reserved.
5	Select High/Low active of Auto Thermal Throttle. 0 : high active. 1 : low active
4	Auto Thermal Throttle enabled.
3	En/disable STPCLK function. Select function when Soft STPCLK enabled(Read IO port 0B2h). 0 : STPGNT. 1 : STPCLK.
2	Software STPCLK enable/disable. 0 : disable 1 : enable
1	Enable/disable SLPJ output.
0	Enable/disable ZZ output.

Note : When D4='1' THRMJ='0' for 2 seconds, THROTTLE function will be enabled automatically. Besides, if I/O port 10h D4 (THT_EN='1'), then THROTTLE function will be enabled, too.

	R_LVL2	R_LVL3	STPCLK_EN	Soft_STPCLK
STPGNT	1	0	X	0
	0	0	0	1
STPCLK	0	1	X	0
	0	0	1	1

Note: All the functions listed above runs only when I/O offset 13h-10h, D9 has enabled.

Register Index : **07Ch**
Register Name : **Break event for STPCLKJ**.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Enable/disable break event of PCI_Master.
6	Enable/disable break event of all devices.
5	Enable/disable break event of PWRBTNJ.
4	Enable/disable break event of INTR.
3	Enable/disable break event of IRQ1-7, IRQ9-15, NMI, INIT and SMI.
2	Enable/disable break event of IRQ8.
1	Enable/disable break event of IRQ0.
0	Enable/disable break event of PCI Access.

Register Index : **07Dh**
Register Name : **Direction control of GPIO[7:0].**
Default Value : 00h
Attribute : Read/Write
0 : GPIO[n] is a General purpose input pin.
1 : GPIO[n] is a General purpose output pin.

Bit	Description
7	Direction of GPIO[7].
6	Direction of GPIO[6].
5	Direction of GPIO[5].
4	Direction of GPIO[4].
3	Direction of GPIO[3].
2	Direction of GPIO[2].
1	Direction of GPIO[1].
0	Direction of GPIO[0].

Register Index : **07Eh**
Register Name : **Data output to GPIO[7:0] when pin GPIO[n] is set as general purpose output pin**.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Data of GPIO[7].
6	Data of GPIO[6].
5	Data of GPIO[5].
4	Data of GPIO[4].
3	Data of GPIO[3].
2	Data of GPIO[2].
1	Data of GPIO[1].
0	Data of GPIO[0].

Register Index : **07Fh**
Register Name: **Data input from GPIO[7:0] when pin GPIO[n] is set as general purpose input pin.**
Default Value : xxh
Attribute : Read

Bit	Description
7	Data input of GPIO[7].
6	Data input of GPIO[6].
5	Data input of GPIO[5].
4	Data input of GPIO[4].
3	Data input of GPIO[3].
2	Data input of GPIO[2].
1	Data input of GPIO[1].
0	Data input of GPIO[0].

*SWITCH control
Register Index : **082h-080h**
Register Name : **Control of external SWITCH.**
Default Value : 0000_x000_x000_x000_x000_x000b
Attribute : Read/Write

Bit	Description
23-16	Reserved.
15	Status of pin THERMALJ.
14	Detects rising edge of THERMALJ.
13	Detects falling edge of THERMALJ.
12	Enable/disable debounce circuit of THERMALJ.
11-0	Reserved.

Register Index : **083h**
Register Name : **Reserved**.

Register Index : **084h**
Register Name : **Reserved**

Register Index : **085h**
Register Name : **Reserved**

Register Index : **086h**
Register Name : **Reserved**

Register Index : **087h**
Register Name : **Reserved**

Register Index : **088h**
Register Name : **Reserved**

Register Index : **089h**
Register Name : **Reserved**

Register Index : **08Ah**
Register Name : **Reserved**

Register Index : **08Bh**
Register Name : **Reserved**

Register Index : **08Eh-08Ch**
Register Name : **Control of External Switch. (resume**)
Default Value : x000_x000_x000_x000_x000_x000b
Attribute : Read/Write

Bit	Description
23-12	Reserved.
11	Status of pin AC Power.
10	Detect rising edge of AC Power.
9	Detect falling edge of AC Power.
8	Enable/disable debounce circuit of AC Power.
7-4	Reserved.
3	Status of pin DOCKJ.
2	Detect rising edge of DOCKJ.
1	Detect falling edge of DOCKJ.
0	Enable/disable debounce circuit of DOCKJ.

Register Index : **08Fh**
Register Name : **Reserved**

Register Index : **090h**
Register Name : **Control of General Purpose external SWITCH A. (resume)**
Default Value : 00x0_0000b
Attribute : Read/Write

Bit	Description
7-1	Reserved.
0	Select PWRBTNJ mode. 0 : The falling edge of PWRBTNJ will generate XSMIJ first. If it is asserted over four seconds, a hardware Soft-Off proceeds automatically. 1 : Generating XSMIJ or proceeding Soft-Off are decided at the rising edge of PWRBTNJ.

Register Index : **091h**
Register Name : **Reserved**

Register Index : **092h**
Register Name : **Reserved**

Register Index : **093h**
Register Name : **Reserved**

Register Index : **097h-094h**
Register Name : **Memory Group A**
Default Value : 00000000h
Attribute : Read/Write

Bit	Description
31-14	Address of A[31:14].
13-4	Mask of address A[23:14].
3-0	Reserved.

Register Index : **09Bh-098h**
Register Name : **Reserved**

Register Index : **09Fh-09Ch**
Register Name : **Reserved**

Register Index : **0A1h-0A0h**
Register Name : **Reserved**

Register Index : **0A3h-0A2h**
Register Name : **Reserved**

Register Index : **0A5h-0A4h**
Register Name : **IO Group C**
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-2	Address of A[15:2].
1-0	Mask of address A[3:2].

Register Index : **0A7h-0A6h**
Register Name : **Reserved**

Register Index : **0A9h-0A8h**
Register Name : **Reserved**

Register Index : **0ABh-0AAh**
Register Name : **Reserved**

Register Index : **0AFh-0ACh**
Register Name : **Reserved**

Register Index : **0B1h-0B0h**
Register Name : **Reserved**

Register Index : **0B2h**
Register Name : **The current state**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-1	Reserved.
0	0 : ON 1 : Standby

Register Index : **0B3h**
Register Name : **Speaker Control**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Reserved.
6	Enable/disable speak function. 0 : Disable speak function. 1 : Enable speak function.
5-4	Latency time of write beep function when writing 0CAh. 00 : 125 ms. 01 : 62.5 ms. 10 : 31.25 ms. 11 : 15.625 ms.
3-2	4-beep function control. 00 : disable 4-beep function. 01 : 4 beeps in 1 sec. 10 : 4 beeps in 2 sec. 11 : 4 beeps in 4 sec.
1-0	Interval time of periodic 4-beep function. 00 : 60 sec. 01 : 30 sec. 10 : 15 sec. 11 : reserved.

Register Index : **0B4h**
Register Name: **Suspend LED. (resume)**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7	Reserved.
6-4	Debounce clock of debounce circuits of all external pins. 000 : 128 Hz 001 : 64 Hz 010 : 32 Hz 011 : 16 Hz 100 : 8 Hz 101 : 4 Hz 110 : 2 Hz 111 : 1 Hz
3	Enable power saving of All resume switches. 0 : disable 1 : enable
2	Power Botton Override Enable/Disable. 0 : enable 1 : disable
1-0	Reserved.

Register Index : **0B5h**
Register Name : **LED control**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-4	Reserved.
3-2	SQWO control. 00 : low. 01 : high. 10 : 1Hz. 11 : 2Hz.
1-0	SLED control. 00 : low. 01 : high. 10 : 1Hz. 11 : 2Hz.

Register Index : **0B6h**
Register Name : **Reserved**

Register Index : **0B7h**
Register Name : **Ring counter**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-4	Reserved.
3-0:	Count.

Register Index : **0B9h**-**0B8h**
Register Name: **Reserved**

Register Index : **0BBh-0BAh**
Register Name : **Reserved**

Register Index : **0BCh**
Register Name : **Shadow register of IO port 70h.**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-0	This register has the same value as IO port 70h. But, when in SMM, writing to port 70h does not change its value. And the value of port 70h will be updated as its value when exiting SMM.

Register Index : **0BDh**
Default Value : 00h
Attribute : Read/Write

Bit	Description
3	PMU Class Code Writable Enable /Disable. 0 : Enable. 1 : Disable.
2	Select 24/32 Bits PM Timer 0 : 24 Bits. 1 : 32 Bits.
1-0	ACPI 24/32 bits timer test mode select (for testing).

Register Index : **0BEh**
Register Name : **Other Configuration**.
Default Value : 00h

Bit	Description
1	Enable power saving of all normal switches. 0 : disable. 1 : enable.
0	Disable internal USB SMIACKJ 0 : Enable. 1 : Disable.

Register Index : **0BFh**
Register Name : **Reserved**.

* GPO and GPI functions
Register Index : **0C2h**-**0C0h**
Register Name : **Data output to GPO pins.**
Default Value : 000000h
Attribute : Read/Write

Bit	Description
23-21	Reserved.
20	GPO[20].
19	GPO[19].
18	GPO[18].
17	Reserved.
16	Reserved.
15	Reserved.
14	Reserved.
13	Reserved.
12	GPO[12].
11-10	Reserved.
9	GPO[9].
8-4	Reserved.
3	GPO[3].
2	GPO[2].
1	GPO[1].
0	GPO[0].

Register Index : **0C3h**
Register Name : **Output data for GPO[23:21]. (resume**)
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-3	Reserved.
2	GPO[23].
1	GPO[22].
0	Reserved.

Register Index : **0C5h-0C4h**
Register Name : **Input data of GPI[11:0].**
Default Value : 0xxxh
Attribute : Read

Bit	Description
15-12	Reserved.
11	GPI[11].
10	GPI[10].
9	GPI[9].
8-4	Reserved.
3	GPI[3].
2	GPI[2].
1	Reserved.
0	GPI[0].

Register Index : **0C6h**
Register Name : **Select Multifunctions in Resume block**. **(resume)**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-3	Reserved.
2	OFF_PWR2/GPO[23] select. 0 : OFF_PWR2. 1 : GPO[23].
1	OFF_PWR1/GPO[22] select. 0 : OFF_PWR1. 1 : GPO[22].
0	Reserved.

Register Index : **0C8h**
Register Name : **Mask monitored events of all timers**.
Default Value : 00h
Attribute : Read/Write
0 : Idle timers can be reset by its monitored event.
1 : Idle timers cannot be reset by its monitored event.

Register Index : **0C9h**
Register Name : **Lock read/write of all configure registers**.
Default Value : 00h
Attribute : Read/Write
0 : All configuration register from offset 040h can be read/write
1 : All configuration registers from offset 040h cannot be read/write except offset 0C9h.

Register Index : **0CAh**
Register Name : **Write Beep Port**. **Write to this port will cause beep**.
Attribute : Write Only

Register Index : **0CBh**
Register Name : **Reserved**

Register Index : **0CCh**
Register Name : **Reserved**.

Register Index : **0CDh**
Register Name : **Reserved**.

Register Index : **0CFh**-**0CEh**
Register Name : **Reserved**.

Register Index : **0D1h**-**0D0h**
Register Name : **Reserved**.

Register Index : **0D4h**
Register Name : **Suspend TEST Mode disable/enable**.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-1	Reserved
0	0 : Disable. 1 : Enable.

Register Index : **0D7h-0D5h**
Register Name : **Reserved**.

Register Index : **0D9h-0D8h**
Register Name : **Dummy register**.
Default Value : 0000h
Attribute : Read/Write

Bit	Description
15-8	Reserved.
7	Enable/Disable HDD monitored access of 1F0-1F7, 3F6, 170-177 and 376. 0 : Disable 1 : Enable
6	Enable/Disable of sleeping state stop external PCICLK. 0 : Disable 1 : Enable
5	Subsystem Vendor ID Writable Enable/Disable. 0 : Enable. 1 : Disable.
4	IRQ1/IRQ12 source select. 0 : IRQ1 & IRQ12. 1 : KBCLK & MSCLK.
3	Enable CPU_STPJ monitor PHOLDJ. 0 : Disable. 1 : Enable. CPU_STPJ will be inactive when PHOLDJ is asserted.
2	Enable delayed SMI of ACPWR and CRT. 0 : Disable. 1 : Enable.
1	Reserved.
0	Enable delayed SMI of all external switches. Except for the following four pins. 0 : Disable. 1 : Enable.

Register Index : **E0h**
Register Name : **SMBus Host & Slave Interface Configuration**
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-2	Reserved.
1	Host Slave Interface Enable.
0	SMB Host Controller Interface Enable.

Register Index : **E1h**
Register Name : **SMBus Host Slave Command Register** : while host being a slave device on the SMBus and the register matches the receiving command data, host generates SMI or Interrupt event.
Default Value : 00h
Attribute : Read/Write

Bit	Description
7-0	SMB Host Slave Command port.

Register Index : **E2h**
Register Name : **SMBus Host Controller Base Clock Setting**
Default Value : 20h

Bit	Description
7-5	Base Clock Select [7:5] "clock" 000 OSC14M/6 : 2.39M 001 OSC14M/12 : 1.19M (default) 010 OSC14M/24 : 0.60M 100 OSC14M/4 : 3.58M 101 OSC14M/8 : 1.79M 110 OSC14M/16 : 0.89M
4-3	Idle delay setting [4:3] "idle time" 00 BaseClk*64 53.76 us ref. 1.19M base clock. (default) 01 BaseClk*32 10 BaseClk*128
2-0	Reserved.

Register Index : **E3h**
Register Name : **Reserved**

4.2 Other I/O and Memory Spaces

4.2.1 DMA Register Description.

a. Command Register, the same as 82C37
b. DMA Channel Mode Register, the same as 82C37
c. DMA Channel Extended Mode Register,
Channels 0-3 port address - 040Bh
Channels 4-7 port address - 04D6h

Bit No.	Bit Name	Bit function	Def.
[1-0]	DMA Channel Select	00 Channel 0(4) select 01 Channel 1(5) select 10 Channel 2(6) select 11 Channel 3(7) select	XX
[3-2]	Reserved		00
[5-4]	DMA Cycle Timing Mode	00 Compatible Timing 01 Compatible Timing 10 Compatible Timing 11 Type F	00
[7-6]	Reserved		00

Compatible Timing : runs at 9 SYSCLKs (1080 nsec/ single cycle) and 8 SYSCLKs (960 nsec/cycle) during the repeated portion of a BLOCK or DEMAND mode.

Type F Timing: runs at 3 SYSCLKs (360 nsec/single cycle) and 2 SYSCLKs (240 nsec/ cycle) during the repeated portion of a BLOCK or DEMAND mode.

d. DMA Request Register, the same as 82C37
e. Mask Resistor-Write Single Mask Bit, the same as 82C37
f. Mask Registor-Write All Mask Register Bits, the same as 82C37
g. Status Register, the same as 82C37
h. DMA Base and Current Address Register 8237 Compatible Segment
i. DMA Base and Current Byte/Word Count Register 8237 Compatible Segment
j. DMA Memory Low/High Page Register
DMA Memory Base Low Page Register
DMA Channel 0 port address - 087h
DMA Channel 1 port address - 083h
DMA Channel 2 port address - 081h
DMA Channel 3 port address - 082h
DMA Channel 5 port address - 08Bh
DMA Channel 6 port address - 089h
DMA Channel 7 port address - 08Ah
DMA Memory Base High Page Register
(Before using 32-bit addressing, index 42h bit6 must be set to '1')
DMA Channel 0 port address - 487h
DMA Channel 1 port address - 483h
DMA Channel 2 port address - 481h
DMA Channel 3 port address - 482h
DMA Channel 5 port address - 48Bh
DMA Channel 6 port address - 489h
DMA Channel 7 port address - 48Ah
These bits form the full 32-bit address for a DMA transfer.
k. Clear Byte Pointer Flip-Flop, the same as 82C37
l. Master Clear, the same as 82C37
m. Clear Mask Register, the same as 82C37

4.2.1.2 TIMER UNIT Register Description

a. Timer Control Word Register, the same as 82C54
b. Interval Timer Read Back Command, the same as 82C54
c. Interval Timer Status Byte Format, the same as 82C54
d. Counter Latch Command Register, the same as 82C54
e. Counter Access Ports, the same as 82C54

4.2.1.3 INTERRUPT UNIT Register Description

Initialization Command Word 1 (ICW1):

Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-5	Reserved
4	Must be 1
3	0 : Edge triggered interrupts for all channels 1 : Level triggered interrupts for all channels
2	Reserved
1	0 : Cascade Controller(M1543 must write 0) 1 : Single Controller
0	0 : No ICW4 needed 1 : ICW4 is needed (M1543 must write 1)

Initialization Command Word 2 (ICW2):

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-3	Interrupt Vector Address
2-0	Reserved

Initialization Command Word 3 (ICW3):

Port 021h (W/O) -- INT Controller 1

M1543 must be programmed to 04h, indicating INT of CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit No.	Bit Function
7-0	0 : IR Input does not have a slave 1 : IR Input has a slave

Port 0A1h (W/O) -- INT Controller 2

M1543 must be programmed to 02h, indicating CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit No.	Bit Function
7-3	must be 0h
2-0	Slave identification code

Initialization Command Word 4 (ICW4):

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-5	must be 0h.
4	0 : Not Specially Fully Nested Mode 1 : Specially Fully Nested Mode
3-2	0x : Non Buffered Mode 10 : Buffer Mode/Slave 11 : Buffer Mode/Master
1	0 : Normal EOI 1 : Auto EOI
0	0 : MCS-80/85 Mode 1 : 80x86 Mode (M1543 must write 1)

Operation Command Word 1 (OCW1):

Port 021h (R/W) -- INT Controller 1
Port 0A1h (R/W) -- INT Controller 2

Bit No.	Bit Function
7-0	0 : Reset IRQ<x> mask 1 : Set IRQ<x> mask

Operation Command Word 2 (OCW2):
Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit No.	Bit Function
7-5	EOI, SL, R 000 : Rotate in Auto EOI Command(Clear) 001 : Non Specific EOI Command 010 : Set Priority Command * L2-L0 are used 011 : * Specific EOI Command 100 : Rotate in Auto EOI Command(Set) 101 : Rotate Non Specific EOI Command 110 : * Set Priority Command 111 : * Rotate on Specific EOI Command
4-3	Must be 00b to select OCW2
2-0	L2,L1,L0 - Interrupt Level Select 000 : IRQ<0(8)> select 001 : IRQ<1(9)> select 010 : IRQ<2(10)> select 011 : IRQ<3(11)> select 100 : IRQ<4(12)> select 101 : IRQ<5(13)> select 110 : IRQ<6(14)> select 111 : IRQ<7(15)> select

Operation Command Word 3 (OCW3):

Port 020h (R/W) -- INT Controller 1
Port 0A0h (R/W) -- INT Controller 2

Bit No.	Bit Function
7	Reserved, must be 0b
6-5	0x : No Action 10 : Reset Special Mask Mode 11 : Set Special Mask Mode
4-3	Must be 01b to select OCW3.
2	0 : No Poll Command 1 : Poll Command
1-0	0x : No Action 10 : Read IRQ Register 11 : Read IS Register

Interrupt Unit Edge/Level Control Register (ELCR):

Port 04D0h (R/W) -- INT Controller 1
Port 04D1h (R/W) -- INT Controller 2

Bit No.	Bit Function
7	0 : IRQ<7(15)> Edge trigger 1 : IRQ<7(15)> Level trigger
6	0 : IRQ<6(14)> Edge trigger 1 : IRQ<6(14)> Level trigger
5	0 : IRQ<5(13)> Edge trigger 1 : IRQ<5(13)> Level trigger
4	0 : IRQ<4(12)> Edge trigger 1 : IRQ<4(12)> Level trigger
3	0 : IRQ<3(11)> Edge trigger 1 : IRQ<3(11)> Level trigger
2	0 : IRQ<2(10)> Edge trigger 1 : IRQ<2(10)> Level trigger
1	0 : IRQ<1(9)> Edge trigger 1 : IRQ<1(9)> Level trigger
0	0 : IRQ<0(8)> Edge trigger 1 : IRQ<0(8)> Level trigger

4.2.1.4 NMI Registers

NMI Enable/Disable and RTC Address register:

Port 70h, 72h
Attribute : Write Only
Default value : 0xxxxxxxb

Bit No.	Bit Function
7	0 : enable NMI interrupt 1 : disable all NMI sources
6-0	RTC Memory addressing

Note : When I/O write port 70h or 72h, pin RTCAS will be active. Port 72h is used to support 256byte RTC.

Port 71h, 73h
Note : When I/O write port 71h or 73h, pin RTCRW will be active (low). When I/O read port 71h or 73h, pin RTCDS will be active (low).

NMI Status and Control register(Port B):

Port 61h
Attribute : Read/Write
Default value : 00h

Bit No.	Bit Function
7 (R only)	0 : No SERRJ from System Board 1 : SERRJ active, NMI requested. To reset this interrupt, set bit 2 to 1.
6 (R only)	0 : No NMI Interrupt from IOCHKJ 1 : IOCHKJ is active and NMI requested. To reset this interrupt, set bit 3 to 1.
5 (R only)	Timer Counter 2 OUT status.
4 (R only)	Toggled from 0 to 1 or 1 to 0 following every refresh cycle.
3 (R/W)	0 : IOCHKJ NMI enable 1 : IOCHKJ NMI disable and clear
2 (R/W)	0 : System board error enable 1 : System board error disable and clear
1 (R/W)	0 : Pin SPKR output is always '0'. 1 : Pin SPKR output is the Timer Counter 2 OUT signal value.
0 (R/W)	0 : Timer Counter 2 disable 1 : Timer Counter 2 enable

4.2.1.5 FAST RC/GATE-A20 Registers.

Port 92h
Default value : 24h
Attribute : Read/Write

Bit No.	Bit Function
7	Reserved (must be read as a 0).
6	Reserved (must be read as a 0).
5	Reserved (must be read as a 1).
4	Reserved (must be read as a 0).
3	Reserved (must be read as a 0).
2	Reserved (must be read as a 1).
1	Directly reflects the A20MJ signal 0 : A20MJ is driven inactive (low) 1 : A20MJ is driven active (high)
0	0 : Allow FAST RC to be pulsed 1 : FAST RC is pulsed active

4.2.2 USB OpenHCI Registers

Register Index **103h-100h**
Register Name : **HceControl Register**
Default Value : 00000000h
Attribute : Read/Write

Bit No.	Bit Function
31-9(0h)	Reserved. Read as 0. I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.
8(0)	A20State. This bit indicates current state of Gate A20 on keyboard controller. This bit is used to compare against value written to 60h when GateA20Sequence is active.
7(0)	IRQ12Active. This bit indicates that a positive transition on IRQ12 from keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
6(0)	IRQ1Active. Indicates that a positive transition on IRQ1 from keyboard controller has occurred. Software may write a 1 to this bit to clear it (set it to 0). Software write of a 0 to this bit has no effect.
5(0)	GateA20Sequence. Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC when a data value of FFh is written to I/O port 64h.
4(0)	ExternalIRQEn. When set to 1, IRQ1 and IRQ12 from the keyboard controller will cause an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
3(0)	IRQEn. When set the Host Controller will generate IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, then IRQ1 is generated and if it is 1, then an IRQ12 is generated.
2(0)	CharacterPending. When set, an emulation interrupt will be generated when the OutputFull bit of the HceStatus register is set to 0.
1(0)	EmulationInterrupt (Read) This bit is a static decode of the emulation interrupt condition.
0(0)	EmulationEnable. When set to 1, the Host Controller will be enabled for legacy emulation. The Host Controller will decode accesses to I/O registers 60H and 64H and generate IRQ1 and/or IRQ12 when appropriate. Additionally, the host controller will generate an emulation interrupt at appropriate times to invoke the emulation software.

Register Index : **107h-104h**
Register Name : **HceInput Register**
Default Value : 000000xxh
Attribute : Read/Write

Bit No.	Bit Function
31-8(000000h)	Reserved. Read as 0.
7-0(xxh)	InputData. This register holds data that is written to I/O ports 60h and 64h. The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

Register Index : **10Bh-108h**
Register Name : **HceOutput Register**
Default Value : 000000xxh
Attribute : Read/Write

Bit No.	Bit Function
31-8(000000h)	Reserved. Read as 0. The contents of the HceStatus Register is returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Access of this register through its memory address produces no side effects.
7-0(xxh)	OutputData. This register hosts data that is returned when an I/O read of port 60h is performed by application software.

Register Index : **10Fh-10Ch**
Register Name : **HceStatus Register**
Default Value : 00000000h
Attribute : Read/Write

Bit No.	Bit Function
31-8(000000h)	Reserved. Read as 0.
7(0)	Parity. Indicates parity error on keyboard/mouse data.
6(0)	Timeout. This is used to indicate a time-out.
5(0)	AuxOutputFull. IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
4(0)	Inhibit Switch. This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
3(0)	CmdData. The HC will set this bit to 0 on an I/O write to port 60h and on an I/O write to port 64h, the HC will set this bit to 1.
2(0)	Flag. Nominally used as a system flag by software to indicate a warm or cold boot.
1(0)	InputFull. Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0(0)	OutputFull. The HC will set this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0 then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1 then and IRQ12 will be generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.

4.2.3 Power Management I/O Space Registers

4.2.3.1 ACPI I/O Registers

The "Base" address is programmed in the PMU PCI DEVICE Configuration Space Offset 10-13h

Register Index : **01h-00h**
Register Name : **Power Management 1 Status Register(PM1_STS)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15	Wakeup Status (WAK_STS) 0 : Cleared by write '1' to this position. 1 : An enabled resume event occurs when system is in the suspend state.
14-11	Reserved. Read as 0's
10	RTC Status (RTC_STS) 0 : Cleared by write '1' to this position. 1 : RTC generate an alarm.(IRQ8J Assert)
9	Reserved. Read as 0's
8	Power Button Status (PWRBTN_STS) 0 : Cleared by write '1' to this position or by Power Button Override condition. 1 : PWRBTNJ is asserted LOW.
7-6	Reserved. Read as 0's
5	Global Status (GBL_STS) 0 : Cleared by write '1' to this position. 1 : The BIOS wanting the attention of the SCI handler (by writing a '1' to the BIOS_RLS bit).
4	Bus Master Status (BM_STS) 0 : Cleared by write '1' to this position. 1 : Anytime a system bus master requests the system bus.
3-1	Reserved. Read as 0's
0	Power Management Timer Carry Status(PMTC_STS) 0 : Cleared by write '1' to this position. 1 : The 22nd (30th) bit of the 24-bit (32-bit) PM timer goes high to low.

Register Index : **03h-02h**
Register Name : **Power Management 1 Enable Register(PM1_EN)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-11	Reserved. Read as 0's.
10	RTC Enable (RTC_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI, SMI or RSM event is generated anytime the RTC_STS bit is set.
9	Reserved. Read as 0's.
8	Power Button Enable (PWRBTN_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI, SMI or RSM event is generated anytime the PWRBTN_STS bit is set.
7-6	Reserved. Read as 0's.
5	Global Enable (GBL_EN) 0 : When reset, then no SCI event is generated. 1 : When set, then an SCI event is generated anytime the GBL_STS bit is set.
4-1	Reserved. Read as 0's.
0	Power Management Timer Carry Enable (PMTC_EN) 0 : When reset, then no SCI event is generated. 1 : When set, then an SCI event is generated anytime the PMTC_STS bit is set.

Register Index : **05h-04h**
Register Name : **Power Management 1 Control Register (PM1_CNTRL)**
Default Value : 1000h
Attribute : Read/Write

Bit No.	Bit Function
15-14	Reserved. Read as 0's.
13	Suspend Enable(SLP_EN) -- Writable and Read as 0's 0 : When reset, then no suspend mode is entering. 1 : When set, then causes the system to sequence into the suspend mode defined by the SLP_TYP field.
12-10	Suspend Type(SLP_TYP) This 3-bit field defines the type of hardware suspend mode. The system should enter when SLP_EN bit is set. 100 : Working 011 : Sleeping 010 : Suspend To DRAM 001 : Suspend To DISK 000 : Soft Off other : reserved The SUS_TYP field is used by the BIOS and OS code to determine the suspend mode that system is resuming from. Before entering any low state(LVL2 or LVL3) this field should be programmed to the Working mode.
9-3	Reserved. Read as 0's
2	Global Release(GBL_RLS) 0 : The resource ownership for ACPI software is not released. 1 : Set by ACPI software to raise SMI event to inform BIOS software, the resource ownership is released.
1	Bus Master Break Event Enable(BM_RLD) 0 : When reset, then bus master request does not affect the processor state. 1 : When set, then bus master request will transition processor from clock control state(C3) to normal state(C0).
0	SCI Enable(SCI_EN) 0 : When reset, then these events will generate SMI interrupt. 1 : When set, then these events will generate SCI interrupt.

Register Index : **07h-06h**
Register Name : **Reserved**

Register Index : **0Bh-08h**
Register Name : **Power Management 1 Timer Register(PM1_TMR)**
Attribute : Read Only

Bit No.	Bit Function
31-24	Extend Power Management Timer Value(E_PMT_VAL) Return the upper eight bits of a 32bits power management timer
23-0	Power Management Timer Value(PMT_VAL) Return the running count of the power management timer currently.

Register Index : **0Fh-0Ch**
Register Name : **Reserved**

Register Index : **13h-10h**
Register Name : **Processor Control Register(P_CNTRL)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
31-18	Reserved. Read as 0's
17	Throttle Status(THRO_STS) -- R0 0 : The clock control state is exit throttling mode. 1 : The clock control state is in the throttling mode.
16-14	Reserved. Read as 0's
13	Clock Run Enable (CR_EN) 0 : Disable 1 : Enable the M1543 becomes a PCI CLKRUN host Programmable (IDLE CYCLE to stop PCI clock).
12-10	Reserved. Read as 0's
9	Clock Control Enable(CLK_EN) 0 : Disable the clock control function. 1 : Enable the clock control function, read to the LVL2 and LVL3 register will cause M1543 enter the enabled clock control mode.
8-5	Reserved. Read as 0's
4	Throttle Enable(THRO_EN) 0 : Disable the CPU clock throttling function. 1 : Enable the CPU clock throttling function.
3-1	Throttle Dutysetting Values (THRO_DTY) This 3-bit duty width field (Dutyset) determines the performance of the processor by the following equation. %Performance = Dutyset/ $2^{dutywidth}$ x 100 % Dutyset : %Performance 000 : reserved 001 : 0-12.5% (about 1/8 high and 7/8 low per throttle period) 010 : 12.5-25%(about 2/8 high and 6/8 low per throttle period) 011 : 25-37.5%(about 3/8 high and 5/8 low per throttle period) 100 : 37.5-50%(about 4/8 high and 4/8 low per throttle period) 101 : 50-62.5%(about 5/8 high and 3/8 low per throttle period) 110 : 62.5-75%(about 6/8 high and 2/8 low per throttle period) 111 : 75-87.5%(about 7/8 high and 1/8 low per throttle period)
0	Reserved. Read as 0's

Register Index : **14h**
Register Name : **Processor Level 2 Register (LVL2)**
Default Value : 00h
Attribute : Read Only

Bit No.	Bit Function
7-0	Reads to this register generate a “enter a level 2 power state” to the clock control logic.

Register Index : **15h**
Register Name : **Processor Level 3 Register (LVL3)**
Default Value : 00h
Attribute : Read Only

Bit No.	Bit Function
7-0	Reads to this register generate a “enter a level 3 power state” to the clock control logic.

Register Index : **17h-16h**
Register Name : **Reserved**

Register Index : **19h-18h**
Register Name : **General Purpose Event0 Status Register (GPE0_STS)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-12	Reserved. Read as 0's
11	RI Status(RING_STS) 0 : Cleared by write '1' to this position. 1 : Anytime the RIJ signal is asserted .
10	ACPWR Status(ACPWR_STS) 0 : Cleared by write '1' to this position. 1 : The ACPWR signal is asserted.
9	Reserved. Read as 0's.
8	DOCKJ Status(DOCK_STS) 0 : Cleared by write '1' to this position. 1 : The DOCKJ signal is asserted .
7-3	Reserved. Read as 0's.
2	USB Event Status(USBE_STS) 0 : Cleared by write '1' to this position. 1 : Anytime the USB Event is actived.
1	Thermal Override Status(THEROR_STS) 0 : Cleared by write '1' to this position. 1 : Anytime the THRMJ signal is driven active for greater than 2 seconds,and starts throttling the CPU's clock at the THTL_DTY ratio(when Auto Thermal Throttle Enabled)
0	Thermal Status(THER_STS) 0 : Cleared by write '1' to this position. 1 : Anytime the THRMJ signal is driven active as defined by the THRM_POL bit.

Register Index : **1Bh-1Ah**
Register Name : **General Purpose Event0 Enable Register (GPE0_EN)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-12	Reserved. Read as 0's.
11	RI Enable (RING_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI,SMI or RSM event is generated anytime the RING_STS bit is set.
10	ACPWR Enable (ACPWR_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI,SMI or RSM event is generated anytime the ACPWR_STS bit is set.
9	Reserved. Read as 0's.
8	DOCKJ Enable (DOCK_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI,SMI or RSM event is generated anytime the DOCK_STS bit is set.
7-3	Reserved. Read as 0's.
2	USB Event Enable (USBE_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI,SMI or RSM event is generated anytime the USBE_STS bit is set.
1	Thermal Override Enable (THEROR_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI or SMI event is generated anytime the THEROR_STS bit is set.
0	Thermal Enable (THER_EN) 0 : When reset, then no event is generated. 1 : When set, then an SCI or SMI event is generated anytime the THER_STS bit is set.

Register Index : **1Dh-1Ch**
Register Name : **General Purpose Event1 Status Register (GPE1_STS)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-12	Reserved. Read as 0's.
11	IRQ Resume Status (IRQ_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : The IRQ(15-9,7-3,1) signal assert.
10	IRQ0 Resume Status (IRQ0_RSM_STS) 0 : Cleared by writing '1' to this position. 1 : The IRQ0 signal assert.
9-1	Reserved. Read as 0's
0	BIOS Status(BIOS_STS) 0 : Cleared by writing '1' to this position. 1 : ACPI software requesting attention (by writing a '1' to the GBL_RLS bit).

Register Index : **1Fh-1Eh**
Register Name : **General Purpose Event1 Enable Register (GPE1_EN)**
Default Value : 0000h
Attribute : Read/Write

Bit No.	Bit Function
15-12	Reserved. Read as 0's
11	IRQ Resume Enable(IRQ_RSM_EN) 0 : When reset, then no event is generated. 1 : When set, then an RSM event is generated anytime the IRQ_RSM_STS is set. (Only in the Sleeping state)
10	IRQ0 Resume Enable(IRQ0_RSM_EN) 0 : When reset, then no event is generated. 1 : When set, then an RSM event is generated anytime the IRQ0_RSM_STS is set.(Only in the Sleeping state)
9-1	Reserved. Read as 0's.
0	BIOS Enable(BIOS_EN) 0 : When reset, then no SMI is generated. 1 : When set, the SMI is generated anytime the BIOS_STS is set.

Register Index : **27h-20h**
Register Name : **General Purpose Event1 Control Register (GPE1_CTL)**
Default Value : 0000_0000h
Attribute : Read/Write

Bit No.	Bit Function
31-2	Reserved. Read as 0's
1	BIOS Release(BIOS_RLS) -- R:0 0 : The resource ownership for BIOS software is not released. 1 : Set by BIOS software to raise SCI event to inform ACPI software, the resource ownership is released.
0	Reserved. Read as 0's

Register Index : **2Fh-28h**
Register Name : **Reserved.**

Register Index : **30h**
Register Name : **Power Management 2 Control Register(PM2_CNTRL)**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-1	Reserved. Read as 0's
0	Arbiter Disable(ARB_DIS) 0 : The arbiter is enabled. 1 : The arbiter is disabled and default CPU has ownership of the system.

Register Index : **3Fh-31h**
Register Name : **Reserved**

4.2.3.2 Advanced Power Management Registers

Register Index : **B1h**
Register Name : **Advances Power Management Access Port (I/O)**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0	Write generates an SMI

Register Index : **B2h**
Register Name : **Advances Power Management Access Port (I/O)**
Default Value : 00h
Attribute : Read Only

Bit No.	Bit Function
7-0	Read causes the STPCLKJ signal to be asserted

Register Index : **B3h**
Register Name : **Advances Power Management Status Port (I/O)**
Default Value : 00h
Attribute : Read/Write

Bit No.	Bit Function
7-0	Pass status information between the OS and SMI handler

4.2.3.3 SMB I/O Space Registers

The "Base" address is programmed in the PMU PCI DEVICE Configuration Space Offset 14-17h

Register Index : **00h**
Register Name : **SMBSTS : SMBus Host/Slave Status Register**
Default Value : 00h
Attribute : (Read/Write, & write '1' clear)

Bit	Description
7	TERMINATE, "1" means the interrupt (or SMI) was caused by a terminated bus transaction in response to "ABORT".
6	BUS_COLLI, Bus Collision, "1" means the interrupt (or SMI) was caused by the collision of bus transaction.
5	DEVICE_ERR, Device Error, "1" means the interrupt (or SMI) was caused by the SMB controller or device due to the generation of an error.
4	SMI_I_STS, "1" means that the Interrupt (or SMI) was caused by the SMB controller after completing a command. (RO)
3	HST_BSY, Host Controller Busy, "1" means that the SMB host controller is going to complete a command.(RO)
2	IDL_STS, "1" means SMBus at Idle Status. (RO)
1	HSTSLV_STS, Host Slave Status, "1" means the interrupt (or SMI) was caused by the host SMB slave interface.
0	HSTSLV_BSY, Host Slave Busy, "1" means that SMB slave interface is going to receive a command. (RO)

Register Index : **01h**
Register Name : **SMBCMD : SMBus Host/Slave Command**
Default Value : 00h
Attribute : Write Only

Bit	Description
7	SMB_BLK_CLR, SMB Block Register Pointer Reset, to reset block register's pointer.(WO)
6-4	SMB_COMMAND, SMB Command, indicates that which kind of command to be asked to perform. (R/W) [6:4] Command 000 Quick command 001 Send/Receive Byte 010 Write/Read Byte 011 Write/Read Word 100 Write/Read Block
3	T_OUT_CMD, like "Abort" command, it (WO) performs the Time Out condition on the SMBus to reset not only Host controller but also other devices on the SMBus. -->DEVICE_ERR
2	Abort, reset Host controller. --> TERMINATE (WO)
1-0	Reserved.

Register Index : **02h**
Register Name : **STRT_PRT : I/O Port to Start to generate the programmed cycle on the SMBus**
Default Value : 00h
Attribute : Write

Register Index : **03h**
Register Name : **SMBus Address Register for Host Controller**
Default Value : 00h
Attribute : Read/Write

Register Index : **04h**
Register Name : **SMBus DataA Register for Host Controller**
Default Value : 00h
Attribute : Read/Write

Register Index : **05h**
Register Name : **SMBus DataB Register for Host Controller**
Default Value : 00h
Attribute : Read/Write

Register Index : **06h**
Register Name : **SMBus Block Register for Host Controller**
Default Value : 00h
Attribute : Read/Write

Register Index : **07h**
Register Name : **SMBus Command Register for Host Controller**
Default Value : 00h
Attribute : Read/Write

Register Index : **08h ~ 1Eh**
Register Name : **Reserved**

4.2.3.4 PCI IDE Controller I/O Space Registers Definition.
The Primary and Secondary Channel can be disabled by setting Byte 09h.

Byte 09h - D7 - Bus master IDE
0 : No, it is not a bus master IDE.
1 : Yes, it is a Bus master IDE.

Byte 09h - D6 - Report IDE channel status
0 : No, this is the default zero value of PCI 2.1 specification.
1 : Yes, D4-5 can be queried to determine status of the IDE controller.

Byte 09h - D5 - Primary Channel
0 : No, the Primary channel is disabled.
1 : Yes, the Primary channel is enabled.

Byte 09h - D4 - Secondary Channel
0 : No, the Secondary channel is disabled.
1 : Yes, the Secondary channel is enabled.

Byte 09h - D3 - Secondary channel support
0 : compatibility only
1 : both compatibility and native mode.
Byte 09h - D2 - Operation of Secondary channel
0 : compatibility mode
1 : Native mode
Byte 09h - D1 - Primary channel support
0 : compatibility only.
1 : both compatibility and native mode.
Byte 09h - D0 - Operation of Primary channel
0 : compatibility mode
1 : Native mode

2. The PIO Mode IDE I/O Space Define.

a. Compatibility Mode.
Primary channel I/O space is from 1F0H to 1F7H and 3F6H. Secondary channel I/O space is from 170H to 177H and 376H.
b. Native Mode.
Primary Channel I/O space can be programmed at 10H and 14H. The I/O range is 8bytes that is descripted at 10H and1 byte is descripted at 14H. Secondary Channel I/O space can be programmed at 18H and 1CH. The I/O range is 8 bytes that is descripted at 18H and 1 byte is descripted at 1Ch.

3. Bus Master IDE Register Description.

The Bus master IDE function uses 16 bytes of I/O space. All bus master IDE I/O space can be accessed as byte, word, or Dword quantities. The description of the 16 bytes of I/O registers are as follows :

Offset from Base Address	Register	Register Access
00h	Bus Master IDE Command Register Primary	R/W
01h	Device Specific	
02h	Bus Master IDE Status Register Primary	RWC
03h	Device Specific	
04h-07h	Bus Master IDE PRD Table Address Primary	R/W
08h	Bus Master IDE Command Register Secondary	R/W
09h	Device Specific	
0Ah	Bus Master IDE Status Register Secondary	RWC
0Bh	Device Specific	
0Ch-0Fh	Bus Master IDE PRD Table Address Secondary	R/W

a. Register Name: Bus Master IDE Command register
Address Offset:
Primary Channel - Base address defined in 20H + 00H
Secondary Channel - Base address defined in 20H + 08H
Base address : F001H
Default Value : 00H
Attribute : Read/Write
Size : 8 bits

Bit	Description
7-4	Reserved. must be 0.
3	Read or Write Control. This bit sets the direction of the bus master transfer. 0 : PCI bus master read 1 : PCI bus master write. This bit must not be changed when the bus master function is active.
2-1	Reserved. must be 0.
0	Start/Stop Bus Master. Writing a '1' to this bit enables bus master operation of the controller. Bus Master operation begins when this bit is detected changing from a zero to a one. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a '0' to this bit. All state information is lost when a '0' is written; Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active and the drive has not yet finished its data transfer, the bus master command is said to be aborted and data transfered from the drive maybe discarded before being written to system memory. This bit is intended to be reset after the data transfer is completed, as indicated by either the Bus Master IDE active bit or the interrupt bit of the Bus master IDE status register for that IDE channel being set, or both.

b. Register Name: Bus Master IDE Status Register Address Offset :
Primary Channel - Base address defined in 20H + 02H
Secondary Channel - Base address defined in 20H + 0AH
Base Address : F001H
Default Value: 00H
Attribute: Read/Write
Size: 8 bits

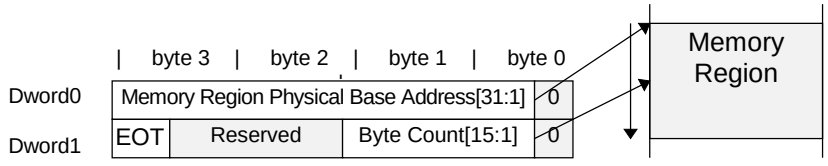
Bit	Description
D7	**Simplex Only**. (RO) This bit indicates whether or not both bus master channels (primary and secondary) can be operated at the same time. 0 : channels operate independently and can be used at a time. 1 : only one channel can be used at a time.
D6	**Drive 1 DMA capable**. (R/W) This bit is set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
D5	**Drive 0 DMA capable**. (R/W) This bit is set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance.
D4-D3	Reserved. must be 0.
D2	**Interrupt**. This bit is set by the rising edge of the IDE interrupt line. This bit is cleared when a '1' is written to it by software. Software can use this bit to determine if an IDE device has asserted its interrupt line. When this bit is one, all data transferred from the drive is visible in system memory.
D1	**Error**. This bit is set when the controller encounters an error in transferring data to/from memory. The exact error condition is bus specific and can be determined in a bus specific manner. This bit is cleared when a '1' is written to it by software.
D0	**Bus Master IDE active**. This bit is set when the Start bit is written to the Command Register. This bit is cleared when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared when the Start bit is cleared in the Command register. When this bit is read as a zero, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted.

c. Register Name : Descriptor Table Pointer Register
Primary Channel - Base address defined in 20H + 04H
Secondary Channel - Base address defined in 20H + 0CH
Base address : F001H
Default Value : 00000000H
Attribute : Read/Write
Size : 32 bits

Bit	Description
D31-2	Base address of Descriptor table. Corresponds to A[31:2]
D1-0	Reserved.

4. The Physical Region Descriptor Table

Before the controller starts a master transfer it is given a pointer to a Physical Region Descriptor Table. This table contains some number of Physical Region Descriptor (PRD) which describe areas of memory that are involved in the data transfer. The PRD table must be aligned on a 4 bytes boundary and the table cannot cross a 64K boundary in memory. The EOT is "END of TABLE". It means that this transaction is ending.



4.3 ISA Compatible Registers Summary:

The ISA compatible registers of the M1543 are summarized as below:

I/O Address	Attribute	Register Name
0000h	Read/Write	DMA1 (slave) CH0 Base and Current Address
0001h	Read/Write	DMA1 (slave) CH0 Base and Current Count
0002h	Read/Write	DMA1 (slave) CH1 Base and Current Address
0003h	Read/Write	DMA1 (slave) CH1 Base and Current Count
0004h	Read/Write	DMA1 (slave) CH2 Base and Current Address
0005h	Read/Write	DMA1 (slave) CH2 Base and Current Count
0006h	Read/Write	DMA1 (slave) CH3 Base and Current Address
0007h	Read/Write	DMA1 (slave) CH3 Base and Current Count
0008h	Read/Write	DMA1 (slave) Status(R)/Command(W)
0009h	Write-only	DMA1 (slave) Write Request
000Ah	Write-only	DMA1 (slave) Write Single Mask Bit
000Bh	Write-only	DMA1 (slave) Write Mode
000Ch	Write-only	DMA1 (slave) Clear Byte Pointer
000Dh	Write-only	DMA1 (slave) Master Clear
000Eh	Write-only	DMA1 (slave) Clear Mask
000Fh	Read/Write	DMA1 (slave) Read/Write All Mask Register Bits
0020h	Read/Write	INT_1 (master) Control Register
0021h	Read/Write	INT_1 (master) Mask Register
0040h	Read/Write	Timer Counter - Channel 0 Count
0041h	Read/Write	Timer Counter - Channel 1 Count
0042h	Read/Write	Timer Counter - Channel 2 Count
0043h	Read/Write	Timer Counter Command Mode Register
0060h	Read_access	Clear IRQ12 (for PS2), IRQ1 Latched Status
0060h	Read/Write	Keyboard Data Buffer
0061h	Read/Write	NMI and Speaker Status and Control
0064h	Read/Write	Keyboard Status(R)/Command(W)
0070h	Write-only	CMOS RAM Address Port and NMI Mask Register
0071h	Read/Write	CMOS Data Register Port
0081h	Read/Write	DMA Channel 2 Page Register
0082h	Read/Write	DMA Channel 3 Page Register
0083h	Read/Write	DMA Channel 1 Page Register
0087h	Read/Write	DMA Channel 0 Page Register
0089h	Read/Write	DMA Channel 6 Page Register
008Ah	Read/Write	DMA Channel 7 Page Register
008Bh	Read/Write	DMA Channel 5 Page Register
008Fh	Read/Write	Refresh Address Register for Address 23 to 17

The ISA compatible registers of M1543 (continued)

I/O Address	Attribute	Register Name
00A0h	Read/Write	INT_2 (slave) Control Register
00A1h	Read/Write	INT_2 (slave) Mask Register
00C0h	Read/Write	DMA2 (master) CH0 Base and Current Address
00C2h	Read/Write	DMA2 (master) CH0 Base and Current Count
00C4h	Read/Write	DMA2 (master) CH1 Base and Current Address
00C6h	Read/Write	DMA2 (master) CH1 Base and Current Count
00C8h	Read/Write	DMA2 (master) CH2 Base and Current Address
00CAh	Read/Write	DMA2 (master) CH2 Base and Current Count
00CCh	Read/Write	DMA2 (master) CH3 Base and Current Address
00CEh	Read/Write	DMA2 (master) CH3 Base and Current Count
00D0h	Read/Write	DMA2 (master) Status(R)/Command(W)
00D2h	Write-only	DMA2 (master) Write Request
00D4h	Write-only	DMA2 (master) Write Single Mask Bit
00D6h	Write-only	DMA2 (master) Write Mode
00D8h	Write-only	DMA2 (master) Clear Byte Pointer
00DAh	Write-only	DMA2 (master) Master Clear
00DCh	Write-only	DMA2 (master) Clear Mask
00DEh	Read/Write	DMA2 (master) Read/Write All Mask Register Bits
00F0h	Write-only	Coprocessor Error Ignored Register
040Bh	Write only	DMA1 Extended Mode Register
0481h	Read/Write	DMA CH2 High Page Register
0482h	Read/Write	DMA CH3 High Page Register
0483h	Read/Write	DMA CH1 High Page Register
0487h	Read/Write	DMA CH0 High Page Register
0489h	Read/Write	DMA CH6 High Page Register
048Ah	Read/Write	DMA CH7 High Page Register
048Bh	Read/Write	DMA CH5 High Page Register
04D0h	Read/Write	INT_1 (master) Edge/Level Control
04D1h	Read/Write	INT_2 (slave) Edge/Level Control
04D6h	Write only	DMA2 Extended Mode Register

4.4 Super I/O Register Overview

Table 4-4-1 I/O Address Decode

Address Range	Block Name	Logical Device	Function
Base + (0-5) and + (7)	Floppy Disk	0	
Base + (0-3) Base + (0-7) Base + (0-3), + (400-402) Base + (0-7), + (400-402)	Parallel port SPP EPP ECP ECP+EPP+SPP	3	
Base + (0-7)	Serial Port COM1	4	IR support
Base + (0-7)	Serial Port COM2	5	IR support
0x60, 0x64	KBC	7	

4.4.1 Configuration Description and Power Management Features

4.4.1.1 Configuration Port

This configuration is based on the typical Plug-and-Play architecture and allows the BIOS to assign resources at POST.

To assign M1543 with Built-in Super I/O a configuration key, <0x51, 0x23> must be written to CONFIG PORT to enter the CONFIGURE mode. Then follow the Plug-and-Play procedure to configure each device.

A configuration key = < 0xBB > must be written to CONFIG PORT to exit the CONFIGURE mode and enter the RUN mode.

After a hard reset or Power on reset, the M1543 with Built-in Super I/O is in the RUN mode with all logical devices disable except KBC. The hardware setting pins control the enable of the KBC after the hard reset. Then the normal configure procedure is also suitable for KBC.

All logical devices may be configured through 2 standard Configuration I/O Ports (INDEX and DATA) by placing the M1543 with Built-in Super I/O into Configuration Mode. The BIOS uses these configuration ports to initialize the logical devices at POST. The INDEX and DATA ports are only valid when the M1543 with Built-in Super I/O is in Configuration Mode.

A hardware setting pin CFG_PORT is latched to select the CFG_PORT as 3F0 or 370.

Port Name	CFG_PORT=1	CFG_PORT=0	Type
CONFIG PORT	0x3F0	0x370	W
INDEX PORT	0x3F0	0x370	W
DATA PORT	0x3F1	0x371	R/W

Programming Example

```
;--------------------------------------
; Enter Configuration mode,
;--------------------------------------
MOV   DX,3F0H
MOV   AX,051H
CLI
OUT   DX,AL
MOV  AX,023H
OUT  DX,AL
;------------------------------------------------------
; Program register 0x60 of Logic Device 4
;------------------------------------------------------
MOV  DX,3F0H
MOV  AL,07H
OUT  DX,AL       ; Point to Device select register
MOV  DX,3F1H
MOV  AL,04H
OUT  DX,AL       ; Point to Device 4
MOV  DX,3F0H
MOV  AL,060H
OUT  DX,AL       ; Point to register 60H
MOV  DX,3F1H
MOV  AL,02H
OUT  DX,AL       ; Update content of register 60H

;-------------------------------
;Exit Configuration Mode
;-------------------------------
MOV  DX,3F0H
MOV  AL,0BBH
OUT  DX,AL
```

Note: The selected logic device number will keep its old value until the next new one is written.

CHIP LEVEL REGISTERS

Index name	**Hard reset, Soft reset default values**
Index 0x02h	0x00, 0x00
Bit 7-1	Reserved
Bit 0	1 : Soft reset the configuration registers. This bit is automatically cleared after write. This register is write only.
Index 0x07h	0x00, 0x00
Bit 7-4	Read as 0.
Bit 3-0	Select the current logic device. This allows the access to each logical device's registers.
Index 0x20h	0x43, 0x43 ALi defined device identification. Read only.
Index 0x21h	0x15, 0x15 ALi defined device identification. Read only.
Index 0x22h	0x00, 0x00
Bit 7-6	Read as 0.
Bit 5	Direct powerdown UART2 (Note 3) 0 : disable 1 : enable
Bit 4	Direct powerdown UART1 (Note 3) 0 : disable 1 : enable
Bit 3	Direct powerdown Parallel Port (Note 3) 0 : disable 1 : enable
Bit 2-1	read as 0.
Bit 0	Direct powerdown FDC (Note 3) 0 : disable 1 : enable

Index 0x23h	0x00, N/A
Bit 7-6	read as 0
Bit 5	Auto powerdown UART2. 0 : disable 1 : enable
Bit 4	Auto powerdown UART1. 0 : disable 1 : enable
Bit 3	Auto powerdown Parallel Port. 0 : disable 1 : enable
Bit 2-0	read as 0.
Index 0x2Dh	0x20, N/A
Bit 7-0	Reserved.
Index 0x2Eh	0x20, N/A
Bit 7-0	Reserved.

LOGICAL DEVICE 0 REGISTERS (FDC)

Index 0x30h	0x00, 0x00
Bit 7-1	read as 0.
Bit 0	FDC (Note 4) 0 : disable 1 : enable
Index 0x60h	0x03, 0x03
Bit 7-2	read as 0.
Bit 1-0	The higher address of the FDC I/O base address.
Index 0x61h	0xF0, 0xF0
Bit 7-3	The lower address of the FDC's I/O base address.
Bit 2-0	set to 0.
Index 0x70h	0x06, 0x06
Bit 7-4	read as 0.
Bit 3-0	Select IRQ channel used by FDC. 0000 : None 0001 : IRQ1 0010 : N/A 0011 : IRQ3 0100 : IRQ4 0101 : IRQ5 0110 : IRQ6 0111 : IRQ7 1000 : N/A 1001 : IRQ9 1010 : IRQ10 1011 : IRQ11 1100 : IRQ12 1101 : N/A 1110 : IRQ14 1111 : IRQ15
Index 0x74h	0x02, 0x02
Bit 7-3	read as 0.
Bit 2-0	Select DMA channel used by FDC 000 : DMA0 001 : DMA1 010 : DMA2 011 : DMA3 100 : None

Index 0xF0h 0x08, N/A

Bit 7-5 read as 0.

Bit 4 0 : No swap.
1 : Swap Drive 0 and Drive 1

Bit 3 0 : PS2 mode
1 : AT mode

Bit 2 read as 0.

Bit 1 0 : Burst DMA mode.
1 : Non-burst DMA mode

Bit 0 0 : Normal mode
1 : Enhanced OS2 mode

Index 0xF1h 0x00, N/A

Bit 7-6 Boot Floppy.
00 : FDD 0
01 : FDD 1
10 : FDD 2
11 : FDD 3

Bit 5-4 Media ID[1-0] polarity.
0 : normal
1 : inverted

Bit 3-2 Density Select.
0x : Normal
10 : force to 1
11 : force to 0

Bit 1-0 External Floppy Select.
0x : internal FDC
10 : external FDC
11 : Drive A internal, Drive B external

Index 0xF2h 0xFF, N/A

Bit 7-6 Floppy Drive D type

Bit 5-4 Floppy Drive C type

Bit 3-2 Floppy Drive B type.

Bit 1-0 Floppy Drive A type.

Index 0xF4h 0x00, N/A

Bit 2, 7-5 read as 0.

Bit 4-3 Data Rate Table Select (refer to Table 3-3).

Bit 1-0 DRVDEN[1-0] signal definition (refer to Table 3-4).

LOGICAL DEVICE 3 REGISTERS (Parallel Port)

Index 0x30h 0x00, 0x00

Bit 7-1 read as 0.

Bit 0 Activate Parallel Port. (Note 4)
0 : disable
1 : enable

Index 0x60h 0x03, 0x03

Bit 7-2 read as 0.

Bit 1-0 The higher address of the Parallel Port's I/O base address.

Index 0x61h 0x78, 0x78

Bit 7-2 The lower address of the Parallel Port's I/O base address.

Bit 1-0 set to 0.

Note : An 8-byte boundary is required if EPP is available

Index 0x70h 0x05, 0x05

Bit 7-4 read as 0.

Bit 3-0 Select IRQ channel used by Parallel Port.

0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Index 0x74h	0x04, 0x04
Bit 7-3	read as 0.
Bit 2-0	Select DMA channel used by Parallel Port. 000 : DMA0 001 : DMA1 010 : DMA2 011 : DMA3 100 : None
Index 0xF0h	0x0C, N/A
Bit 7	read as 0.
Bit 6-3	ECP FIFO threshold value. Default is 0001.
Bit 2-0	EPP Compatible mode. 000 : PS2 001 : EPP 1.9 010 : ECP 011 : ECP+EPP1.9 100 : SPP (default) 101 : EPP 1.7 111 : ECP+EPP 1.7
Index 0xF1h	0x05, N/A
Bit 7	Output Type 0 : Open Drain 1 : Force Driving
Bit 6-3	read as 0.
Bit 2	PP operation clock. 0 : 24Mhz. 1 : 12Mhz
Bit 1	EPP time-out interrupt. 0 : disable 1 : enable
Bit 0	0 : Non-burst DMA mode. 1 : Burst DMA transfer mode in ECP

LOGICAL DEVICE 4 REGISTERS (UART1)

Index 0x30h	0x00, 0x00
Bit 7-1	read as 0.
Bit 0	UART1 (Note 4) 0 : disable 1 : enable
Index 0x60h	0x03, 0x03
Bit 7-2	read as 0.
Bit 1-0	The higher address of the UART1's I/O base address.
Index 0x61h	0xF8, 0xF8
Bit 7-3	The lower address of the UART1's I/O base address.
Bit 2-0	set to 0.
Index 0x70h	0x04, 0x04
Bit 7-4	read as 0.
Bit 3-0	Select IRQ used by UART1. 0000 : None 0001 : IRQ1 0010 : N/A 0011 : IRQ3 0100 : IRQ4 0101 : IRQ5 0110 : IRQ6 0111 : IRQ7 1000 : N/A 1001 : IRQ9 1010 : IRQ10 1011 : IRQ11 1100 : IRQ12 1101 : N/A 1110 : IRQ14 1111 : IRQ15
Index 0xF0h	0x00, N/A
Bit 7-3	read as 0.
Bit 2	0 : Normal 1 : 8Mhz clock source for UART1
Bit 1	High speed mode 0 : disable 1 : enable
Bit 0	MIDI support 0 : disable 1 : enable

Index 0xF1h 0x02, N/A

Bit 7-5 read as 0.

Bit 4-3 IR mode.
00 : Normal
01 : IrDA
10 : ASK IR
11 : Normal

Bit 2 0 : Full duplex in IR
1 : Half duplex in IR

Bit 1 IR transmit polarity.
0 : active high
1 : active low

Bit 0 IR receive polarity.
0 : active high
1 : active low

Index 0xF2h 0x0C, N/A

Bit 7-5 read as 0.

Bit 4-3 IR half-duplex time-out time control
00: 41-bit time for TR, 39-bit time for RX
01: 42-bit time for TR, 39-bit time for RX
1x: 40-bit time for TR and RX

Bit 2 IR half-duplex Rx-to-Tx time-out timer.
0 : disable
1 : enable

Bit 1 IR half-duplex Tx-to-Rx time-out timer.
0 : disable
1 : enable

Bit 0 Baud Rate output on RI1.
0 : disable
1 : enable

LOGICAL DEVICE 5 REGISTERS (UART2)

Index 0x30h 0x00, 0x00

Bit 7-1 read as 0.

Bit 0 UART2 (Note 4)
0 : disable
1 : enable

Index 0x60h 0x02, 0x02

Bit 7-2 read as 0.

Bit 1-0 The higher address of the UART2's I/O base address.

Index 0x61h 0xF8, 0xF8

Bit 7-3 The lower address of the UART2's I/O base address.

Bit 2-0 set to 0.

Index 0x70h 0x03, 0x03

Bit 7-4 read as 0.

Bit 3-0 Select IRQ channel used by UART2.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Index 0xF0h 0x00, N/A

Bit 7-3 read as 0.
Bit 2 1 : 8Mhz clock source for UART2
0 : Normal

Bit 1 High speed mode
0 : disable
1 : enable

Bit 0 MIDI support
0 : disable
1 : enable

Index 0xF1h 0x02, N/A

Bit 7, 5 read as 0.

Bit 6 IR input source.
0 : use SIN2 and SOUT2
1 : use IRRX2 and IRTX2

Bit 4-3 IR mode.
00 : Normal
01 : IrDA
10 : ASK IR
11 : Normal

Bit 2 1 : Half duplex in IR
0 : Full duplex in IR.
Bit 1 IR transmit polarity.
0: active high
1: active low
Bit 0 IR receive polarity.
0 : active high
1 : active low

Index 0xF2h 0x0C, N/A

Bit 7-5 read as 0.

Bit 4-3 IR half-duplex time-out time control.
1x : 40-bit time for TR and RX
01 : 42-bit time for TR, 39-bit time for RX
00 : 41-bit time for TR, 39-bit time for RX.
Bit 2 IR half-duplex Rx-to-Tx time-out timer
0 : disable
1 : enable
Bit 1 IR half-duplex Tx-to-Rx time-out timer.
0 : disable
1 : enable
Bit 0 Baud Rate output on RI2
0 : disable
1 : enable

LOGICAL DEVICE 7 REGISTERS (KEYBOARD)

Index 0x30h 0x00, 0x00

Bit 7-1 read as 0.

Bit 0 Keyboard controller. This is a hardware setting bit by RTS2J. (Note 4)
0 : disable
1 : enable

Index 0x70h 0x01, 0x01

Bit 7-4 read as 0.

Bit 3-0 Select IRQ channel used by Keyboard.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Index 0x72h 0x00, 0x00

Bit 7-4 read as 0.

Bit 3-0 Select IRQ channel used by PS/2 Mouse.
0000 : None
0001 : IRQ1
0010 : N/A
0011 : IRQ3
0100 : IRQ4
0101 : IRQ5
0110 : IRQ6
0111 : IRQ7
1000 : N/A
1001 : IRQ9
1010 : IRQ10
1011 : IRQ11
1100 : IRQ12
1101 : N/A
1110 : IRQ14
1111 : IRQ15

Index 0xF0h N/A, N/A

Bit 7,5-4 read as 0.

Bit 6 Read only. Indicates the type of keyboard

0 : PS2.
1 : AT

Bit 2-0 read as 0.

Table 4-4-2 M1543 with Super I/O Hardware Setting Configuration

Pin Name	Function
RTS1J	CFG_PORT
0	0x370
1	0x3F0
RTS2J	KBC_EN
0	disable
1	enable
DTR2J	PS2_ATJ (KBC)
0	AT mode
1	PS2 mode

Table 4-4-3 Drive Option 1 and 2

Data Rate	Register Settings (3F7)		FDC 0xF4[4:3]*		Densel
KB/sec	Drate Sel 1	Drate Sel 0	Drate Opt1	Drate Opt0	(1)
1000	1	1	0	0	1
500	0	0	0	0	1
300	0	1	0	0	0
250	1	0	0	0	0
1000	1	1	0	1	1
500	0	0	0	1	1
500	0	1	0	1	0
250	1	0	0	1	0

Note: *Drive Table 00 = Regular drives and 2.88MB
01 = 3-mode drive

Table 4-4-4 Drvden Output Mapping for Drive Type Table

0xF4 [1:0]		Drvden Signal Definition	
DT1	**DT0**	**DRVDEN1**	**DENSEL**
0	0	DRATE0	Densel
1	0	DRATE0	DRATE1
0	1	DRATE0	nDensel
1	1	DRATE1	DRATE0

4.4.1.2 Power Management Features

The M1543 with Built-In Super I/O contains power management features that makes it ideal for design of green personal computers.

4.4.1.3 Part Power Management

This section deals with the power management of the chip. This part shows how powerdown modes and wake up modes are activated.

4.4.1.3.1 Powerdown Modes of FDC

The FDC is powered down in two ways: direct powerdown and automatic powerdown. Direct powerdown results in immediate powerdown of the part without regard to the current state of the part. Automatic powerdown results when certain conditions become true within the part.

A. Direct Powerdown

Direct powerdown is conducted via the powerdown bit in the DSR register (bit 6) or FDC_PWD bit in 0X22. Programming this bit high will powerdown M1543 with Built-in Super I/O after the part is internally reset. All current status is lost if this type of powerdown mode is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown will override the automatic powerdown. If the part is in automatic powerdown when the DSR powerdown is issued, then all the previous status of the part will be lost, and the M1543 with Built-in Super I/O will be reset to its default values.

B. Auto Powerdown

Automatic powerdown is conducted via a "Set Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions are listed as follows :

1. The motor enable pins ME[0:3] must be inactive,
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt),
3. The head unload timer must have expired, and
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the AUTOPD bit in the command to high. The command also provides a capability of programming a minimum power-up time via the MIN DLY bit in the command. The minimum power-up time refers to a minimum amount of time the part will remain powered-up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down provided all the remaining conditions are met. Any software reset will reinitialize the timer. Changing of data rate extends the auto powerdown timer by up to 10 ms, but only if the data rate is changed during the countdown.
Disabling the auto powerdown mode cancels the timers and holds the M1543 with Built-in Super I/O out of auto powerdown.

4.4.1.3.2 Powerdown Mode of UART and Printer

UART1, UART2 and printer can enter direct powerdown or auto powerdown respectively by setting their relative powerdown bit in the 0X22 and 0x23.

4.4.1.3.3 WAKE UP MODES of FDC

This section describes the conditions for awakening the FDC from both direct and automatic powerdown. Power conservation of battery life is the main reason power management is required. This means that the M1543 with Built-in Super I/O must be kept in powerdown state as long as possible and should be powered up as late as possible without compromising software transparency.
To keep the part in powerdown mode as late as possible implies that the part should wake-up as fast as possible. However, some amount of time is required for the part to exit powerdown state and prepare the internal microcontroller to accept commands. Application software is very sensitive to such a delay and in order to maintain software transparency, the recovery time of the wake-up process must be carefully controlled by the system software.

A. Wake Up from DSR Powerdown

If the M1543 with Built-In Super I/O enters powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will serve, although DSR is recommended. No other register access will awaken the part, including writing to the DOR's motor enable (ME[0:3]) bits.

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command is not blocking it. Finally, after a delay, the polling interrupt will be issued.

B. Wake Up from Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.
If a hardware or software reset is used, then the part goes through the normal reset sequence. If the access is through the selected registers, then the M1543 with Built-in Super I/O resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake-up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not wake-up the part)
2. A read from the MSR register
3. A read or write to the FIFO register

Any of these actions will wake-up the part. Once awake, M1543 with Built-in Super I/O will initiate the auto powerdown time for 10 ms or 0.5 sec. (Depending on the MIN DLY bit the auto powerdown command). The part will powerdown again when all the powerdown conditions stated in the *Auto Powerdown* section are satisfied.

4.4.2 Floppy Disk Controller

4.4.2.1 Register Overview

The integrated FDC of the M1543 with Built-in Super I/O part is register- and hardware-level compatible with the industry standard 765A and 82077SL standards. Table 4-1 lists the I/O address map of the FDC controller. Table 4-2 is the summary of FDC register hardware reset.

Table 4-4-5 FDC Controller I/O Address Map

A2	A1	A0	R/W	Register
0	0	0	R	SRA (PS/2 mode only)
0	0	1	R	SRB (PS/2 mode only)
0	1	0	R/W	Digital Output Register DOR
0	1	1	R/W	Tape Drive Register TDR
1	0	0	R	Main Status Register MSR
1	0	0	W	Data Rate Select Register DSR
1	0	1	R/W	Data (First In First Out) FIFO
1	1	0	-	Reserved
1	1	1	R	Digital Inout Register DIR
1	1	1	W	Configuration Control Register CCR

* When this location is accessed, only bit 7 is driving, all other bits are held tristate.

Table 4-4-6 Summary of FDC Register Hardware Reset and Powerdown State

Register Map	Bits State	7	6	5	4	3	2	1	0	I/O Address
DOR(R/W)	H/W Reset State	0	0	0	0	0	0	0	0	3F2
TDR(R/W)	H/W Reset State	_	_	_	_	_	_	0	0	3F3
MSR(R)	H/W Reset State	0	X	X	X	X	X	X	X	3F4
DSR(W)	H/W Reset State	0	0	0	0	0	0	1	0	3F4
DIR(R)	H/W Reset State	na	_	_	_	_	_	_	_	3F7
CCR(W)	H/W Reset State	_	_	_	_	_	_	1	0	3F7
SRA(R)	H/W Reset State	0	na	0	na	0	na	na	0	3F0
SRB(R)	H/W Reset State	1	1	0	0	0	0	0	0	3F1

4.4.2.2 Register Description

This section describes the register bits for all the registers that are directly accessible to the CPU.

4.4.2.2.1 Status Register A (SRA)

Address 3F0 Read only

This register is read-only and monitors the state of the IRQ6 pin and several disk interface pins in PS/2 modes. The SRA can be accessed at any time when it is in PS/2 mode. In the PC/AT mode, the data bus pins D0-D7 are held in a high impedance state for a read of address 3F0.

PS/2 mode

Bit	Name
7	Int Pending
6	DRV2J
5	STEP
4	TRK0J
3	HDSEL
2	INDXJ
1	WPJ
0	DIR

Bit 7 **Interrupt Pending** : The state of the Floppy Disk Interrupt output (active high).

Bit 6 **DRV2J** : DRV2 disk interface input pin, indicates that a second drive has been installed.

Bit 5 **Step** : Step output disk interface output pin (active high)

Bit 4 **Track 0** : TRK0 disk interface input (active low)

Bit 3 **Head Select** : HDSEL disk interface input.

A logic "1" selects side 1 and a logic "0" selects side 0.

Bit 2 **Index** : Index disk interface input (active low)

Bit 1 **Write Protect** : Write protect disk interface input. A logic "0" indicates that the disk is write protected.

Bit 0 **Direction** : The direction of head movement (active high). A logic "1" indicates inward direction a logic "0" outward.

4.4.2.2.2 Status Register B (SRB)

Address 3F1 Read only

This register is read-only and monitors the state of several disk interface pins, in PS/2 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode, the data bus pins D0-D7 are held in a high impedance state for a read of address 3F1.

PS/2 mode

Bit	Name
7	1
6	1
5	Drive Sel0
4	Wdata Toggle
3	Rdata Toggle
2	Wgate
1	MOTEN1
0	MOTEN0

Bit 7 **Reserved** : Always read as a logic "1"

Bit 6 **Reserved** : Always read as a logic "1"

Bit 5 **Drive Select 0** : Reflects the status of the Drive Select bit 0 of DOR (address 3F2 bit 0). This bit is cleared after a hardware reset, it is unaffected by a software reset.

Bit 4 **Write Data Toggle** : This bit changes state at every inactive edge of the WDATA

Bit 3 **Read Data Toggle** : Every inactive edge of the RDATA input causes this bit to change state.

Bit 2 **Write Gate** : The WGATE disk interface output (active high)

Bit 1 **Motor Enable 1** : The MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

Bit 0 **Motor Enable 0** : The MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

4.4.2.2.3 Digital Output Register (R/W)

Address 3F2 R/W

Table 4-4-7 Digital Output Register Description

Bit	Description
7	**Motor Enable 3:** This controls the Motor for drive 3, MTR3. The output is high when it is inactive, and low when it is active. This bit and DOR bit 6 provide information that control the MTR1 and 0 pins, respectively when bit 7 of the configuration register is set.
6	**Motor Enable 2:** Same function as D7 except for drive 2's motor. Note that this signal is not brought out to a pin.
5	**Motor Enable 1:** This bit controls the Motor for drive 1's motor. When this bit is 0, the MTR1 output is high.
4	**Motor Enable 0:** Same as D5 except for drive 0's motor.
3	**DMA Enable:** When set to a 1, this enables the DRQ, DAK, and INT pins. A zero disables these signals.
2	**Reset Controller:** This bit resets the controller when 0 and enables normal operation when it is a 1. It does not affect the drive control or data rate registers which are reset only by a hardware reset.
1-0	**Drive Select:** These two pins are encoded for the four drive select, and are gated with the motor enable lines, so that only one drive is selected when its motor enable is active.

Table 4-4-8 Internal 4 Drive Decode - Normal

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DS1J	DS0J	MTR1J	MTR0J
x	x	x	1	0	0	1	0	/D5	/D4
x	x	1	x	0	1	0	1	/D5	/D4
x	1	x	x	1	0	1	1	/D5	/D4
1	x	x	x	1	1	1	1	/D5	/D4
0	0	0	0	x	x	1	1	/D5	/D4

Table 4-4-9 Internal 4 Drive Decode - Drives 0 and 1 Swapped

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DS1J	DS0J	MTR1J	MTR0J
x	x	x	1	0	0	0	1	/D4	/D5
x	x	1	x	0	1	1	0	/D4	/D5
x	1	x	x	1	0	1	1	/D4	/D5
1	x	x	x	1	1	1	1	/D4	/D5
0	0	0	0	x	x	1	1	/D4	/D5

4.4.2.2.4 Tape Drive Register (TDR)

Address 3F3 R/W

This register is included for 82077 software compatibility. The robust data separator used in the M1543 with Built-in Super I/O does not require its characteristics modified for tape support. The contents of this register are not used internally to the device. The TDR is unaffected by a software reset. Bits 2-7 are tri-stated when read in this mode.

Normal Floppy mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2- 7 are at high impedance.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tapesel 1	tapesel 0

Enhanced Floppy mode 2 (OS2)

Register 3F3 for Enhanced Floppy mode 2 operation

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Media ID1	Media ID0	Drive type ID		Floppy boot drive		tapesel1	tapesel0

Bit 7 **Media ID 1** Read only (pin 1) see table next page

Bit 6 **Media ID 0** Read only (pin 100) see table next page

Bits 5 and 4 **Drive Type ID** - These bits reflect two of the bits of FDC 0XF2 configuration register (see next page for more detail).

Bits 3 and 2 **Floppy Boot Drive**. These bits show the value of FDC 0xF1 configuration register bits.

Bits 1 and 0 - **Tape Drive Select** (R/W). Same as in Normal and Enhanced Floppy mode 1.

Media ID1

Drate1	Media ID1	
pin 1	FDC 0xF1-db5=0	FDC 0xF1-db5=1
0	0	1
1	1	0

Media ID0

Drate0	Media ID0	
pin 100	FDC 0xF1-db4=0	FDC 0xF1-db4=1
0	0	1
1	1	0

Drive type ID

Digital Output Register		Register 3F3 - drive type ID	
bit 1	bit 0	bit 5	bit 4
0	0	FDC 0xF2 - bit 1	FDC 0xF2 - bit 0
0	1	FDC 0xF2 - bit 3	FDC 0xF2 - bit 2
1	0	FDC 0xF2 - bit 5	FDC 0xF2 - bit 4
1	1	FDC 0xF2 - bit 7	FDC 0xF2 - bit 6

4.4.2.2.5 Main Status Register

Address 3F4h Read only

The read-only main status register indicates the current status of the disk controller. It is always available to be read. One of its functions is to control the flow of data to and from the data register. It also indicates when the disk controller is ready to send or receive data. It should be read before each byte is transferred to or from the data register except during a DMA transfer. No delay is required when reading this register after a data transfer.

Main Status Register Description

Bit	Description
7	**Request for Master:** Indicates that the data register is ready to send or receive data from the CPU. This bit is cleared immediately after a byte transfer, and is set again as soon as the disk controller is ready for the next byte.
6	**Data Direction:** Indicates whether the controller is expecting a byte to be written to or read from the data register.
5	**Non-DMA Execution:** If this bit is set, the multiple byte data transfer (in the execution phase) must be monitored by the CPU either through interrupts, or software polling as described in the processor software interface section.
4	**Command in Progress:** Bit is set after the first byte of the command phase is written. Bit is cleared after the last byte of the result phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the command phase is written.
3~0	**Drives 3~0 Seeking:** Set after the last byte of the command phase of a seek or recalibrate command is issued for drives 3~0, respectively. Cleared after reading the first byte in the result phase of the sense interrupt command for this drive.

4.4.2.2.6 Data Rate Select Register (DSR)

Address 3F4 Write only

Table 4-4-11 Datarate Select Register Description

Bit	Description
7	**S/W RESET** behaves the same as DOR RESET except that this reset is self clearing.
6	**POWERDOWN** bit implements direct powerdown. Setting this bit high puts the FDC into the powerdown state regardless of the state of the part. The part is reset internally and then put into powerdown. No status is saved and any operation in progress is aborted. This powerdown mode does not turn off the internal oscillator. Any hardware or software reset will exit the M1543 with Built-in Super I/O from this powerdown state.
5	**Reserved.**
4~2	**PRECOMP 0-2** adjusts the WRDATA output to the and disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the M1543 with Built-in Super I/O compensates the data pattern as it is written to the disk. The amount of precompensation depends upon the drive and media but in most cases the default value is acceptable. The M1543 with Built-in Super I/O starts precompensating the data pattern starting on Track 0. The CONFIGURE command can change the starting track for precompensation. Table below lists the precompensation values that can be selected and a table lists the default precompensation values. The default value is selected if the three bits are zeros.
1~0	**DRATE 0-1** select one of the four data rates as listed in table next page. The default value is 250 Kbps upon a chip ("Hardware") reset. Other ("Software") Resets do not affect the DRATE or PRECOMP bits.

Precompensation Delay Values

PRECOMP 432 bits	Precompensation Delay--DISABLED
111	0.00ns
001	41.67ns
010	83.34ns
011	125.00ns
100	166.67ns
101	208.33ns
110	250.00ns
000	DEFAULT

Default Precompensation Delay Values

Data Rate	Precompensation Delay
1 Mbps	41.67ns
500 Kbps	125ns
300 Kbps	125ns
250 Kbps	125ns

Data Rates

DRATESEL		Data Rate	
		MFM	FM
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

4.4.2.2.7 Data Register (R/W)

Address 3F5 R/W

This is the location through which all commands, data, and status flow between the CPU and the FDC. During the command phase, the CPU loads the controller's commands into this register based on the status register request for master and data direction bits. The result phase transfers the status registers and header information to the CPU in the same fashion.

All command parameter information and disk data transfers go through the FIFO. The 16-byte FIFO has programmable threshold values. Data transfers are generated by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to an M5105 compatible mode after a "Hardware" reset (Reset via pin 1). "Software" Resets (Reset via DOR or DSR register) can also place the M1543 with Built-in Super I/O into M5105-compatible mode if the LOCK bit is set to "0". This maintains PC-AT hardware compatibility.

The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk error. Table 4-13 gives several examples of the delays with a FIFO. The data is based upon the following formula:

Threshold# * 1/DATA RATE * 8 - 1.5$_{us}$ = DELAY

Table 4-4-15 FIFO Service Delay

FIFO Threshold Examples	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	1 * 8$_{us}$ - 1.5$_{us}$ = 6.5$_{us}$
2 bytes	2 * 8$_{us}$ - 1.5$_{us}$ = 14.5$_{us}$
8 bytes	8 * 8$_{us}$ - 1.5$_{us}$ = 62.5$_{us}$
15 bytes	15 * 8$_{us}$ - 1.5$_{us}$ = 118.5$_{us}$
FIFO Threshold Examples	**Maximum Delay to Servicing at 500 Mbps Data Rate**
1 byte	1 * 16$_{us}$ - 1.5$_{us}$ = 14.5$_{us}$
2 bytes	2 * 16$_{us}$ - 1.5$_{us}$ = 30.5$_{us}$
8 bytes	8 * 16$_{us}$ - 1.5$_{us}$ = 126.5$_{us}$
15 bytes	15 * 16$_{us}$ - 1.5$_{us}$ = 238.5$_{us}$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the M1543 with Built-in Super I/O enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred.
An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

4.4.2.2.8 Configuration Control Register (CCR, PC-AT Modes)

Address 3F7 Write only

Table 4-4-16 Configuration Control Register Description

Bit	Description
7~2	Not used.
1, 0	**Data Rate Select:** These bits set the data-rate and write-precompensation values for the disk controller. After a hardware reset, these bits are set to 1, 0 (250 Kbps). (please refer to table 4-12)

4.4.2.2.9 Digital Input Register (DIR, Read)

Address 3F7 Read only

Table 4-4-17a Digital Input Register Description (PC/AT mode)

Bit	Description
7	DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable, regardless of the value of /INVERT/. The DSKCHG bit is forced inactive along with all the inputs from the FDD. All the other bits remain tri-stated.
6~0	These bits are reserved for use by the hard disk controller, thus during a read of this register, these bits are in high impedance state.

Table 4-4-17b Digital Input Register (PS/2 mode)

Bit	Description
7	DSKCHG monitors the pin of the same name and reflects the opposite value seen on the disk cable.
6~3	undefined, always read as logic "1".
2~1	Data rate select. These bits control the data rate of the floppy controller. These bits are unaffected by a software reset, and are set to 250 kbps after a hardware reset.
0	High density. This bit is low whenever the 500 kbps or 1 Mbps data rates are selected, and high when 250 kbps and 300 kbps are selected.

4.4.2.3 Result Phase Status Registers

The result phase of a command contains bytes that hold status information. The format of these bytes are described in the following sections. Do not confuse these register bytes with the main status register which is a read-only register that is always available. The result phase status registers are read from the data register only during the result phase.

4.4.2.3.1 Status Register 0 (ST0)

Table 4-4-18 Status Register 0 Description

Bit	Description
7~6	**Interrupt Code :** 00 = Normal termination of command. 01 = Abnormal termination of command. Command was executed, but not successfully completed. 10 = Invalid command issue. Command issued was not recognized as a valid command. 11 = Ready changed state during the polling mode.
5	**Seek End :** This bit is set after a seek or recalibrate command is completed by the controller. Used during sense interrupt command.
4	**Equipment Check :** This bit is set after a recalibrate command track 0 signal failed to occur. Used during sense interrupt command.
3	**Not Used :** 0
2	**Head Number :** At end of execution phase.
1, 0	**Drive Select :** At end of execution phase. 00 = Drive 0 selected 01 = Drive 1 selected 10 = Drive 2 selected 11 = Drive 3 selected

4.4.2.3.2 Status Register 1 (ST1)

Table 4-4-19 Status Register 1 Description

Bit	Description
7	**End of Track :** This bit is set when the controller has transferred the last byte of the last sector without the TC pin becoming active. The last sector is the end-of-track sector number programmed in the command phase.
6, 3	**Not Used :** 0
5	**CRC Error :** If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the address field of the correct sector. If bit 5 of ST2 is set, then there was a CRC error in the data field.
4	**Over Run :** This bit is set when the controller was not serviced by the CPU soon enough during a data transfer in the execution phase. Table 4-18 shows the time values.
2	**No Data :** This bit is set for any three possible problems : 1. Controller cannot find the sector specified in the command phase during the execution of a read, write, or scan command. An address mark was found even if it is not a blank disk. 2. Controller cannot read any address fields without a CRC error during read ID command. 3. Controller cannot find the starting sector during execution of read a track command.
1	**Not Writable :** Set if the write protect pin is active when a write or format command is issued.
0	**Missing Address Mark :** If this bit is set and bit 0 of ST2 is clear then the disk controller cannot detect any address field address mark after two disk revolutions. If bit 0 of ST2 is set, then the disk controller cannot detect the data field address mark.

Table 4-4-20 Maximum Time Allowed to Service an Interrupt or Acknowledge a DMA Request in Execution Phase

Data Rate	Time to Service
125	62.0 us
250	30.0 us
500	14.0 us
125	6.0 us

4.4.2.3.3 Status Register 2 (ST2)

Table 4-4-21 Status Register 2 Description

Bit	Description
7	**Not Used :** 0
6	**Control Mark :** This bit is set if the controller tried to read a sector which contained a deleted data address mark during execution of read-data or scan commands. Or, if a read-deleted-data command was executed, a regular address mark was detected.
5	**CRC Error in Data Field :** This bit is set if the controller detected a CRC error in the data field. Bit 5 of ST1 is also set.
4	**Wrong Track :** This bit is only set if the desired sector is not found, and the track number recorded on any sector of the current track is different from that stored in the track register.
3	**Scan Equal Hit :** This bit is only set if the equal condition is satisfied during any scan command.
2	**Scan Not Satisfied :** This bit is set if the controller cannot find a sector on the track number recorded on any sector on the track which meets the desired condition during scan command.
1	**Bad Track :** This bit is only set if the desired sector is not found, and the track number recorded on any sector on the track is different from that stored in the track register and the recorded track number is FF.
0	**Missing Address Mark in Data Field :** This bit is set if the controller cannot find the data field address mark during read/scan command. Bit 0 of ST1 is also set.

4.4.2.3.4 Status Register 3 (ST3)

Table 4-4-22 Status Register 3 Description

Bit	Description
7	**Not Used :** 0
6	**Write Protect Status :** This bit is the complement of the associated FDC interface pin for the drive selected in DCR.
5	**Not Used :** 1
4	**Track 0 Status :** This bit is the complement of the associated FDC interface pin for the drive selected in the DCR.
3	**Not Used :** 0
2	**Head Select Status :** This bit shows the status of the associated bit in the sense-drive-status command phase.
1, 0	**Drive Selected :** These bits show the status of the associated bits in the sense-drive-status command phase. These bits show the same status as ST0 bits 1, 0. 00 = Drive 0 selected 01 = Drive 1 selected 10 = Drive 2 selected 11 = Drive 3 selected

4.4.2.4 Processor Software Interface

Bytes are transferred to and from the disk controller in different ways for the different phases in a command.

4.4.2.4.1 Command Sequence

The disk controller can perform various disk transfers and head movement commands. Most commands involve three separate phases.

Command Phase: The CPU writes a series of bytes to the data register. These bytes indicate the command desired and the particular parameters required for the command. All the bytes must be written in the order specified in the command description table. The execution phase starts immediately after the last byte in the command phase is written. Set the drive-control and data-rate registers before performing the command phase.

Execution Phase: The disk controller performs the desired command. Some commands require the CPU to read or write data to or from the data register during this phase. Reading data from a disk is an example of this.

Result Phase: The CPU reads a series of bytes from the data register. These bytes indicate whether the command executed properly, and other pertinent information. The bytes are read in the order specified in the command description table.

Initiate a new command by writing the command phase bytes after the last byte required from the result phase have been read. Update the drive control and data rate registers if the next command requires selecting a different drive or changing the data rate. If the command is the last command, then the software should deselect the drive.

As a general rule, the operation of the controller core is independent of how the CPU updates the drive control and data rate registers. The software must ensure that manipulation of these registers is coordinated with the controller operation.

During the command phase and the result phase, bytes are transferred to and from the data register. The main status register is monitored by the software to determine when a data transfer can take place. Bit 6 of the main status register must be clear and bit 7 must be set before a byte can be written to the data register during the command phase. Bits 6 and 7 of the main status register must both be set before a byte can be read from the data register during the result phase.

There are three methods for transferring information during the execution phase. The DMA mode is used if the system has a DMA controller. This allows the CPU to do other things during the execution phase data transfer. If DMA is not used, an interrupt can be issued for each byte transferred during the execution phase. If interrupts are not used, the Main status register can be polled to indicate when a byte transfer is required.

4.4.2.4.2 DMA Mode

If the DMA mode is selected, a DMA request is generated in the execution phase when each byte is ready to be transferred. To enable DMA operations during the execution phase, the DMA mode bit in the specify command must be enabled, and the DMA signals must be enabled in the drive control register. The DMA controller responds to the DMA request with a DMA-acknowledge and a read- or write-strobe. The DMA request is cleared by the active edge of the DMA-acknowledge and a read-or write-strobe. The DMA request is cleared by the active edge of the DMA-acknowledge. After the last byte is transferred, an interrupt is generated, indicating the beginning of the result phase. During DMA operations, the chip select input must be held high. TC is asserted to terminate an operation. Due to internal gating, TC is only recognized when the -DAK input is low.

4.4.2.4.3 Interrupt Mode

If the non-DMA mode is selected, an interrupt is generated in the execution phase when each byte is ready to be transferred. The main status register should be read to verify that the interrupt is for a data transfer. Bits 5 and 7 of the main status register is set. The interrupt is cleared when the byte is transferred to or from the data register. The CPU should transfer the byte within the time allotted by Table 4-18. If the byte is not transferred within the time allotted, an overrun error is indicated in the result phase when the command terminates at the end of the current sector.

An interrupt is also generated after the last byte is transferred. This indicates the beginning of the result phase. Bits 7 and 6 of the main status register are set, and bit 5 is cleared. This interrupt is cleared by reading the first byte in the result phase.

4.4.2.4.4 Software Polling

If the non-DMA mode is selected and interrupts are not suitable, the CPU can poll the main status register during the execution phase to determine when a byte is ready to be transferred.
In the non-DMA mode, bit 7 of the main status register reflects the state of the interrupt pin. Otherwise, the data transfer is similar to the interrupt mode described above.

4.4.2.5 Command Set Descriptions

Commands can be written whenever the M1543 with Built-in Super I/O is in the command phase. Each command has a unique set of needed parameters and status results. The M1543 with Built-in Super I/O checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is valid, the next time the RQM bit in the MSR register is a "1", the DIO and CB bits will also be "1" indicating the FIFO must be read. A result byte of 80H will be read out of the FIFO, indicating an invalid command was issued. After reading the result byte from the FIFO, the M1543 with Built-in Super I/O returns to the command phase. Table 4-23 lists the summary of the command set.

Table 4-4-23 M1543 with Built-in Super I/O FDC Command Set

READ DATA

Command Phase

MT	MFM	SK	0	0	1	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ DELETED DATA

Command Phase

MT	MFM	SK	0	1	1	0	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ A TRACK

Command Phase

0	MFM	0	0	0	0	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data read from disk drive is transferred to system via DMA or Non-DMA modes.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

READ ID

Command Phase

0	MFM	0	0	1	0	1	0
0	0	0	0	0	HD	DR1	DR0

Execution Phase: Controller reads first ID Field header bytes it can find and reports these bytes to the system in the result bytes

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

M1543 FDC Command Set (continued)

WRITE DATA

Command Phase

MT	MFM	0	0	0	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is transferred form the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

WRITE DELETED DATA

Command Phase

MT	MFM	0	0	1	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is transferred form the system to the controller via DMA or Non-DMA modes and written to the disk.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

FORMAT A TRACK

Command Phase

0	MFM	0	0	1	1	0	1
0	0	0	0	0	HD	DR1	DR0
Bytes per Sector							
Sector per Track							
Format Gap							
Data Pattern							

Execution Phase: System transfers four ID bytes per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the Data Field of each sector is filled with the data pattern byte

Result Phase

Status Register 0
Status Register 1
Status Register 2
Undefined
Undefined
Undefined
Undefined

SCAN EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

M1543 FDC Command Set (continued)

SCAN HIGH OR EQUAL

Command Phase

MT	MFM	SK	1	1	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

SCAN LOW OR EQUAL

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data transfer from system to controller is compared to data read from disk

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

VERIFY

Command Phase

MT	MFM	SK	1	0	1	1	0
0	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

Execution Phase: Data is read from disk but not transferred to the system.

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

DUMPREG

Command Phase

0	0	0	0	1	1	1	0

Execution Phase: Internal registers read

Result Phase

Present Track Number on Drive 0							
Present Track Number on Drive 1							
Present Track Number on Drive 2							
Present Track Number on Drive 3							
Step Rate Time				Motor Off Time			
Motor On Time							DMA
Sector per Track/End of Track							
LOCK	0	D3	D2	D1	D0	GAP	WG
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

PERPENDICULAR MODE

Command Phase

0	0	0	1	0	0	1	0
OW	0	D3	D2	D1	D0	GAP	WG

Execution Phase: Internal registers are written.

No Result Phase.

M1543 FDC Command Set (continued)

CONFIGURE

Command Phase

0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

Execution Phase: Internal registers are written.

No Result Phase

RECALIBRATE

Command Phase

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

Execution Phase: Disk drive head is stepped out to Track 0.

No Result Phase

RELATIVE SEEK

Command Phase

1	DIR	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
Relative Track Number							

Execution Phase: Disk drive head stepped in or out a programmable number of tracks.

No Result Phase

SEEK

Command Phase

0	0	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
New Track Number							

Execution Phase: Disk drive head is stepped in or out to a desired track.

No Result Phase

SENSE DRIVE STATUS

Command Phase

0	0	0	0	0	1	0	0
0	0	0	0	0	HD	DR1	DR0

Execution Phase: Disk drive status information is detected and reported.

Result Phase

Status Register 3

SENSE INTERRUPT

Command Phase

0	0	0	0	1	0	0	0

Execution Phase: Status of interrupt is reported

Result Phase

Status Register 0
Present Track Number

SPECIFY

Command Phase

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

Execution Phase: Internal registers are written.

No Result Phase

POWERDOWN MODE

Command Phase

0	0	0	1	0	1	1	1
0	0	0	0	0	0	DLY	APD

Execution Phase: Internal registers are written

Result Phase

0	0	0	0	0	0	DLY	APD

VERSION

Command Phase

0	0	0	1	0	0	0	0

Result Phase

1	0	0	1	0	0	0	0

LOCK

Command Phase

LOCK	0	0	1	0	1	0	0

Execution Phase: Internal registers are written.

Result Phase

0	0	0	LOCK	0	0	0	0

INVALID

Command Phase

Invalid Codes

Result Phase

Status Register 0 (80H)

Table 4-4-24 Parameter Abbreviations

Symbol	Description
AUTOPD	**Auto Powerdown Control**. If this bit is 0, the automatic powerdown is disabled. If it is set to 1, the automatic powerdown is enabled.
C	**Cylinder Address**. This is the currently selected cylinder address. Valid values are from 0 ~ 255.
D_0, D_1 D_2,D_3	**Drive Select 0 ~ 3**. This bit designates which drives are perpendicular. A '1' indicates perpendicular drive.
D	**Data Pattern**. This bit sets the pattern to be written in each sector data field during formatting.
DIR	**Direction Control**. If this bit is 0, the head steps out from the spindle during a relative seek. If set to a 1, the head steps in toward the spindle.
DS0, DS1	**Disk Drive Select**. DS1 DS0 0 0 drive 0 0 1 drive 1 1 0 drive 2 1 1 drive 3
DTL	**Special Sector Size**. When N is zero (00), DTL controls the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but not passed to the host during read commands. During write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	**Enable Count**. When this bit is 1, the DTL parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	**Enable FIFO**. When this bit is 0, FIFO is enabled. A 1 puts the M1543 with Built-in Super I/O in the 8272A-compatible mode where the FIFO is disabled.
EIS	**Enable Implied Seek**. When set, M1543 with Built-in Super I/O performs a seek operation before executing any read or write command that requires the C parameter in the command phase. A 0 disables the implied seek.
EOT	**End of Track**. The final sector number of the current track.
GAP	This bit alters Gap 2 length when using perpendicular mode.

Table 4-4-24 Parameter Abbreviations (continued)

Symbol	Description
GPL	**Gap Length**. The gap 3 size. Gap 3 is the space between sectors excluding the VCO synchronization field.
H/HDS	**Head Address**. Selected address: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	**Head Load Time**. The time interval that M1543 with Built-in Super I/O waits after loading the head and before initiating a read or write operation. Refer to the Specify command for actual delays.
Lock	Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the Configure command can be reset to their default values by a software reset.
MFM	**MFM/FM mode selector**. 1 selects the double density (MFM) mode. 0 selects single-density (FM) mode.
MIN DLY	**Minimum Power-Up time Control**. This bit is active only if AUTO PD bit is enabled. Set this bit to 0 to assign a 10-ms minimum power-up time. Set this bit to 1 to assign a 0.5-second minimum power-up time.
MT	**Multitrack selector**. When set, this flag selects the multitrack operating mode. In this mode, the M1543 with Built-in Super I/O treats a complete cylinder, under head 0 and 1, as a single track. The M1543 with Built-in Super I/O operates as if this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation automatically continues to the first sector under head 1 when the M1543 with Built-in Super I/O finishes operating on the last sector under head 0.
N	**Sector Size Decode**. This specifies the number of bytes in a sector. If this parameter is 00, the sector size is 128-bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise, the sector size is (2 raised to the Nth power) times 128. All values up to 07 hex are allowable. 07h equals a sector size of 16K. N — Sector Size 00 — 128 bytes 01 — 256 bytes 02 — 512 bytes 03 — 1024 bytes 04 — 2048 bytes 05 — 4096 bytes 06 — 8192 bytes 07 — 16 Kbytes
NCN	**New Cylinder Number**. The desired cylinder number.
ND	**Non-DMA Mode Flag**. When set to 1, indicates that the M1543 with Built-in Super I/O is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the M1543 with Built-in Super I/O operates in DMA mode, interfacing to a DMA controller by means of the DRQ and DACKJ signals.
OW	These bits, denoted by D_0, D_1, D_2 and D_3 of the Perpendicular Mode command can only be overwritten when the OW bit is set to 1.
PCN	**Present Cylinder Number**. The current position of the head at the completion of the Sense Interrupt Status command.
POLL	**Polling Disabled**. When set, the internal polling routine is disabled, when clear, polling is enabled.
PRETRK	**Precompensation Start Track Number**. Programmable from track 00 to FFH.
R	**Sector Address**. The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	**Relative Cylinder Number**. Relative cylinder offset from present cylinder as used by the relative seek command.
SC	**Number of Sectors**. The number of sectors to be initialized by the Format command. The number of sectors to be verified during a Verify command when EC is set.

Table 4-4-24 Parameter Abbreviations (continued)

Symbol	Description
SK	**Skip flag**. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to 0, the sector is read or written the same as the read and write commands.
SRT	**Step Rate Interval**. The time interval between step pulses issued by the M1543 with Built-in Super I/O. It is programmable from 0.5 ~ 8 milliseconds, in increments of 0.5 ms at the 1-Mbit data rate.
ST0, ST1	**Status register 0 ~ 3**. Registers within the M1543 with Built-in Super I/O that store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	**Write Gate**. This bit alters the WE timing to allow for pre-erase loads in perpendicular drives.

4.4.2.5.1 Floppy Disk Controller (FDC)

The FDC is a microcontroller PD765A software-compatible with additional hardware and software enhancements. It has logic circuitry required for an IBM PC, XT, AT, and 386/486 design.

This controller has write-precompensation circuitry. Its shift register allows a fixed 125 ns early-late precompensation for all tracks at 500/300/250 Kb/s (83 ns for 1 mb/s), or a precompensation value that scales with the data rate, 250/208/125/83 ns for data rates of 250/300/500 Kb/s and 1.0 Mb/s, respectively.

It includes address decode for the A0 ~ A2 address lines, the motor/drive-select register, data-rate register for selecting 250/300/500 kb/s and 1Mb/s, disk-change status, dual-speed spindle motor control, and DMA interrupt logic. It can be connected directly to the disk drive via internal high-drive outputs, and Schmitt inputs. It has 1.0 Mb/s data rate, extended track range to 4096, implied seek, working scan commands, motor control timing, both IBM formats as well as Sony 3.5-inch (ISO) formats, and other enhancements.

4.4.2.5.1.1 765A Compatible Micro-Engine

This section describes the basic architectural features of the FDC. The core of the FDC is a PD765A-compatible microcoded engine. This engine consists of a sequencer, program ROM, and disk/misc registers. This core is clocked by either a 4-MHz, 4.8-MHz or 8-MHz clock selected in the data-rate register. All of these core including the data separator and write -precompensation logic comprise the glue logic used to implement a PC-XT, AT, or PS/2 floppy controller.

The FDC takes commands and returns data and status through the data register in a byte serial fashion. Handshake for command/status I/O is provided via the main status register. All of the PD765A commands are supported, as are many other enhanced commands.

The FDC controls the entire operation of the chip including:

- coordination of data transfer with the CPU
- control of the drive controls
- performance of the algorithm associated with reading (for the data separator) and writing data to/from the disk.

4.4.2.5.1.2 PC/XT and PC/AT Logic Blocks

This section describes the major functional blocks of the PC logic that have been integrated on the controller.

DMA Enable Logic: This is a gating logic that disables the DMA lines and the Interrupt output, under the control of the DMA enable bit in the drive control register. When the DMA enable bit is 0 then the INT, and DRQ are held tristate, and -DAK is disabled.

Drive Output Buffers/Input Receivers: The drive interface output pins can drive 150 ± 10% terminate resistors. This enables connection to a standard floppy drive. All drive interface inputs are TTL-compatible, Schmitt-trigger inputs with typically 250 mV of hysteresis.

4.4.2.6 Command Description Table

4.4.2.6.1 Read Data

The read data op-code is written to the data register followed by 8 bytes as specified in the command description table. After the last byte is written, the controller starts looking for the correct sector header. Once the controller is found, the controller sends data to the CPU. After one sector is finished, the sector number is incremented by one and this new sector is searched for. If MT (multi-track) is set, both sides of one track can be read. Starting on side zero, the sectors are read until the sector number specified by end of track sector number is reached. Then, side one is read by starting with sector number one.

In DMA mode, the read-data command continues to read until the TC pin is set. This means that the DMA controller should be programmed to transfer the correct number of bytes. TC should be controlled by the CPU and be asserted when enough bytes are received. An alternative to these methods of stopping the read-data command is to program the end of track sector number as the last sector number that to be read. The controller stops reading the disk with an error message indicating that it tried to access a sector number beyond the end of the track.

The number of data bytes per sector parameter is defined in Table 4-27. If this is set to zero, the data length parameter defines the number of bytes that the controller transfers to the CPU. If the data length specified is smaller than 128, the controller still reads the entire 128 byte sector and checks the CRC, though only the number of bytes specified by the data length parameter are transferred to the CPU. Data length parameter should not be set to zero. If the number of bytes per sector parameter is not zero, the data length parameter has no meaning and should be set to FFh.

Table 4-4-25 Sector Size Selection

Bytes/Sector Code	Number of Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192

If the implied seek mode is enabled by both the mode command and the IPS bit in this command, a seek is performed to the track number specified in the command phase. The controller also waits for the head-settle-time if the implied seek is enabled. After all these conditions are met, the controller searches for the specified sector by comparing the track number, head number, sector number, and number of bytes/sector given in the command phase with the appropriate bytes read off the disk in the address fields.

If the correct sector is found, but there is a CRC error in the address field, bit 5 of ST1 (CRC error) is set and an abnormal termination is indicated. If the correct sector is not found, bit 2 of ST1 (no data) is set and an abnormal termination is indicated. In addition to this, if any address field track number is FF, bit 1 of ST2 (bad track) is set or, if any address field track number is different from that specified in the command phase, bit 4 of ST2 (wrong track) is set.

After finding the correct sector, the controller reads that data field. If a deleted data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a deleted data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination. If a CRC error is detected in the data field, bit 5 is set to both ST1 and ST2 (CRC error) and an abnormal termination is indicated.

If no problems occur in the read command, the read continues from one sector to the next in logical order (not physical order) until either TC is set or an error occurs. If a disk has not been inserted into the disk drive, there are many opportunities for the controller to hang. It does this if it is waiting for a certain number of disk revolutions. If this occurs, the controller can be forced to abort the command by writing a byte to the data register.

An interrupt is generated when an execution phase of the read data command terminates. Table 4-28 shows the values that are read back in the result phase. If an error occurs, the result bytes indicate the sector being read when the error occurred.

Table 4-4-26 Result Phase Termination Values with No Error

Last	ID Information at Result Phase					
MT	**HD**	**Sector**	**Track**	**Head**	**Sector**	**B/S**
0	0	< EOT	NC	NC	S + 1	NC
0	0	= EOT	T + 1	NC	1	NC
0	1	< EOT	NC	NC	S + 1	NC
0	1	= EOT	T + 1	NC	1	NC
1	0	< EOT	NC	NC	S + 1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S + 1	NC
1	1	= EOT	T + 1	0	1	NC

EOT = End of track sector number from command phase
NC = No change in value
S = Sector number last operated on by controller
T = Track number programmed in command phase

4.4.2.6.2 Read-Deleted-Data

This command is the same as the read-data command except for how it handles a deleted data mark. If a deleted data mark is read, the sector is read normally. If a regular data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a regular data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination.

4.4.2.6.3 Write-Data

The write-data command is very similar to the read-data command except that data is transferred from the CPU to the disk rather than the other way around. If the controller detects the write-protect signal, bit 1 of ST1 (not writable) is set and an abnormal termination is indicated.

4.4.2.6.4 Write-Deleted-Data

This command is the same as the write-data command except that a deleted-data mark is written at the beginning of the data field instead of the normal data mark.

4.4.2.6.5 Read a Track

This command is similar to the read-data command except for the following: the controller starts at the index hole and reads the sectors in their physical order, not their logical order.
Even though the controller reads sectors in their physical order, it still compares the header ID bytes with the data programmed in the command phase. The exception to this is the sector number. Internally, this is set to one, then incremented for each successive sector read. Whether or not the programmed address field matches that read from the disk, the sectors are still read in their physical order. If a header ID comparison fails, bit 2 of ST1 (No data) is set, but the operation continues. If there is a CRC error in the address or data field, the read also continues. The command terminates when it has read the number of sectors programmed in the EOT parameter.

4.4.2.6.6 Read ID

This command causes the controller to read the first address field it finds. The result phase contains the header bytes that are read. There is no data transfer during the execution phase of this command. An interrupt is generated when the execution phase is completed.

4.4.2.6.7 Format-a-Track

This command formats one track on the disk. After the index hole is detected, data patterns are written on the disk including all gaps, address marks, address fields, and data fields. The exact details of the number of bytes for each field is controlled by the parameters given in the format-a-track command, and the IAF (Index Address Field) bit in the mode command. The data field consists of the fill-byte specified in the command, repeated to fill the entire sector. To allow for floppy formatting, the CPU must supply the four address field bytes (track, head, sector, number of bytes) for each sector formatted during the execution phase. In other words, as the controller formats each sector, it requests four bytes through either DMA requests or interrupts. This allows for non-sequential sector interleaving. Table 4-29 shows some typical values for the programmable gap size.

The format command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the result phase are significant.

Table 4-4-27A Gap Length for Various Sector Sizes and Disk Types

Mode	Sector Size (Dec)	Sector Code (Dec)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
8-inch Drives (360 RPM, 500 kb/s)					
FM	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	0F	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5.25-inch Drives (300 RPM, 250 kb/s)					
FM	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3.5-inch Drives (300 RPM, 250 kb/s)					
FM	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM	256	01	0F	0E	36
	512	02	09	1B	54
	1024	03	05	35	74

Table 4-4-27B Format Table for PC-Compatible Diskette Media

Media Type	Sector Size (Dec)	Sector Code (Hex)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
360 K	512	02	09	2A	50
1.2 M	512	02	0F	1B	54
720 M	512	02	09	1B	50
1.44 M	512	02	12	1B	6C
2.88 M	512	02	24	1b	54

* Format gap is the gap length used only for the format command.

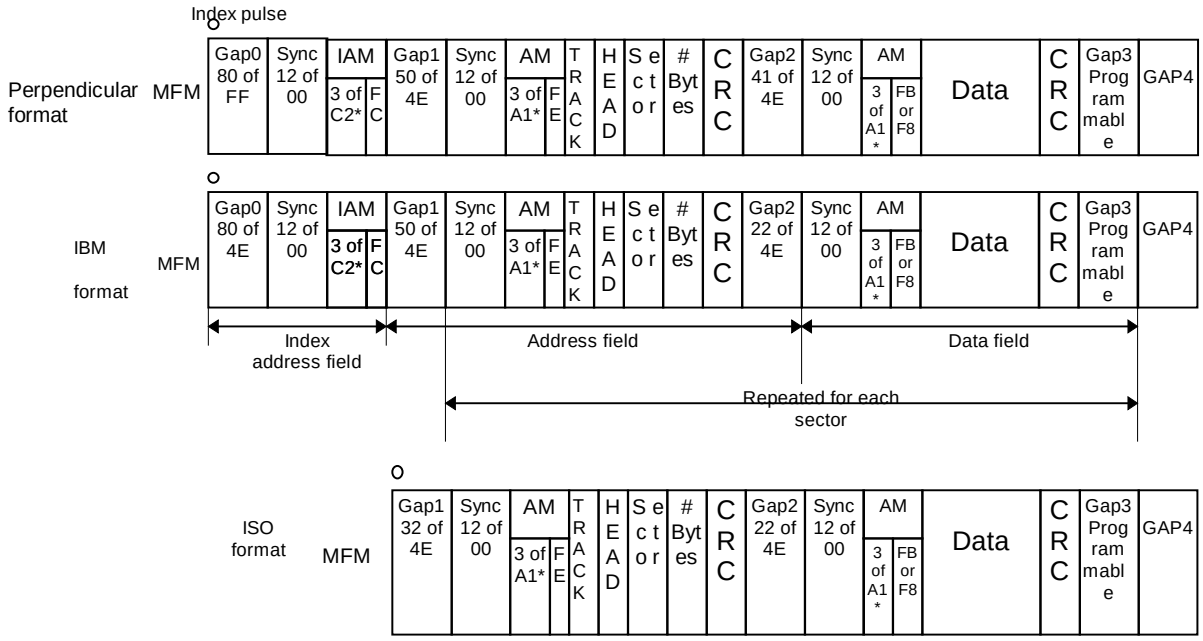


Figure 4-4-1 IBM and ISO Formats Supported by the Format Command

4.4.2.6.8 Scan Commands

The scan commands allow data read from the disk to be compared against data sent from the CPU. There are three scan commands to choose from:

Scan equal	Disk data = CPU data
Scan less than or equal	Disk data ≤ CPU data
Scan greater than or equal	Disk data ≥ CPU data

Each sector is interpreted with the most significant byte first. If the wildcard mode is enabled from the mode command, an FFh from either the disk or CPU is used as a "don't care" byte that always matches equal. If each sector is read, the desired condition has not been met, and the next sector is read. The next sector is defined as the current sector number plus the sector step-size specified.

The scan command continues until the scan condition has been met, or the end of track sector number has been reached, or if TC is asserted. If the SK bit is set, sectors with deleted data marks are ignored. If all sectors read are skipped, the command terminates with D3 of ST2 set (scan equal hit). Table 4-30 shows the result phase of the command.

Table 4-4-28 Scan Command Termination Values

Status Register Command	D2	D3	Conditions
Scan equal	0	1	Disk = CPU
	1	0	Disk <> CPU
Scan low	0	1	Disk = CPU
or equal	0	0	Disk < CPU
	1	0	Disk > CPU
Scan high	0	1	Disk = CPU
or equal	0	0	Disk < CPU
	1	0	Disk > CPU

4.4.2.6.9 Seek

There are two ways to move the disk drive head to the desired track number. The first method is to enable the implied seek mode. This way, each individual read or write command automatically moves the head to the track specified in the command.

The second method is by using the seek command. During the execution phase of the seek command, the track number to seek for is compared with the present track number, and a step pulse is produced to move the head one track closer to the desired track number. This is repeated at the rate specified by the specify command until the head reaches the correct track. At this point, an interrupt is generated and a sense-interrupt command is required to clear the interrupt.

During the execution phase of the seek command, the only indication via software that a seek command is in progress is bits 0~3 (drive busy) of the main status register. Bit 4 of the main status register (command in progress) is not set. While the internal micro-engine is capable of multiple seeks on two or more drives at the same time since the drives are selected via the drive-control register in software, software should ensure that only one drive performs the seek command at one time. No other command except the sense-interrupt command is issued while a seek command is in progress.

If the extended track range mode is enabled, write a fourth byte in the command phase to indicate the four most significant bits of the desired track number. Otherwise, write only three bytes.

4.4.2.6.10 Relative Seek

The Relative Seek command steps the selected drive in or out a given number of steps. This command will step the read/write head an incremental number of tracks from the current track number, contrasting to step it to the desired track number as Seek command. The Relative Seek parameters are defined as follows:

DIR: Read/Write Head Step Direction Control
0=Step Head Out, 1=Step Head In

RTN: Relative Track Number. This value will determine how many incremental tracks to step the head in or out from the current track number.

4.4.2.6.11 Recalibrate

The recalibrate command is very similar to the seek command. It is used to step a drive head out to track zero. Step pulses are produced until the track zero signal from the drive becomes true. If the track zero signal does not go true before 77 step pulses are issued, an error is generated. If the extended track range mode is enabled, an error is not generated until 3,917 pulses are issued.

Recalibrations on more than one drive at a time should not be issued for the same reason as explained in the seek command. No other command except the sense-interrupt command should be issued while a recalibrate command is in progress.

4.4.2.6.11 Sense-Interrupt Status

An interrupt is generated by the controller when any of the following conditions occur:

1. Upon entering the result phase of:
   a. Read-data command
   b. Read-deleted-data command
   c. Write-data command
   d. Write-deleted-data command
   e. Read-a-track command
   f. Read-ID command
   g. Format command
   h. Scan commands

2. During data transfers in the execution phase while in the non-DMA mode

3. Internal ready signal changes state (only occurs immediately after a hardware or software reset).

4. Seek or recalibrate command termination

An interrupt generated for reasons 1 and 2 above occurs during normal command operations and are easily recognized by the CPU. During an execution phase in non-DMA mode, bit 5 (execution mode) in the MSR is set to 1. Upon entering result phase, this bit is set to 0.

Reasons 1 and 2 do not require the sense interrupt status command. The interrupt is cleared by reading or writing information to the data register. Interrupts caused by reasons 3 and 4 are identified with the aid of the sense interrupt status command. This command resets the interrupt when the command byte is written.

Table 4-31 shows how to identify the cause of the interrupt by using bits 5, 6 and 7 of ST0.

Issuing a sense-interrupt status command without an interrupt pending is treated as an invalid command. If the extended track range mode is enabled, a third byte should be read in the result phase which indicates the four most significant bits of the present track number. Otherwise, only two bytes should be read.

4.4.2.6.12 Specify

The specify command sets the initial values for each of the three internal timers. Table 4-32 shows the timer programming values.

The head-load and head-unload timers are artifacts of the UPD765A. These timers determine the delay from loading the head until a read or write command is started, and unloading the head sometime after the command was completed. Since the M1543 with Built-in Super I/O head-load signal is now the software-controlled motor lines in the drive-control register, these timers only provide some delay from the initialization of a command until it is actually started. Similar to the DP8474, extend these timers setting the TMR bit in the mode command.

The step-rate time defines the time interval between adjacent step pulses during a seek, implied-seek, or recalibrate command. The times stated in Table 4-32 are affected by the data rate. These values are for 500 kb/s MFM (250 Kb/s FM) and 1 Mb/s MFM (500 Kb/s FM). For 300 kb/s MFM data rate (150 Kb/s FM), these values, multiply by 1.6667, and for 250 Kb/s MFM (125 Kb/s FM) double these values.

The choice of DMA or non-DMA operation is made by the non-DMA bit. When this bit is 1, the non-DMA mode is selected, and when this bit is 0, DMA mode is selected. This command does not generate an interrupt.

Table 4-4-29 Status Register 0 Termination Codes

Interrupt Code D7	D6	D5	Seek End Cause
1	1	0	Internal ready went true
0	0	1	Normal seek termination
0	1	1	Abnormal seek termination

Table 4-4-30 Step, Head, Load and Unload Timer Definitions (500 kb/s MFM)

Timer	Mode 1 Value	Range	Mode 2 Value	Range	Unit
Step Rate	(16 - N)	1~16	(16 - N)	1~16	ms
Head Unload	N x 16	0~240	N x 512	0~7680	ms
Head Load	N x 2	0~254	N x 32	0~4064	ms

4.4.2.6.13 Sense Drive Status

This two-byte command obtains the status of a disk drive. Status register 3 is returned in the result phase and contains the drive status. This command does not generate an interrupt.

4.4.2.6.14 Verify

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously stored value.

4.4.2.6.15 Version

The Version command can be used to determine the floppy controller being used. The result phase uniquely identifies the floppy controller version. The FDC returns a value of 90h in order to be compatible with the 82077. For older version compatible with NEC765 controller a value of 80h (invalid command) will return.

4.4.2.6.16 Dumpreg

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. The command returns important information regarding the status of many of the programmed field in the FDC. This can be used to verify the values initialized in the FDC.

4.4.2.6.17 Configure

The Configure command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power up. These bits are set to their default values after a hardware reset.
EIS: Enable implied seek. When EIS=1, the FDC will perform a SEEK operation before executing a read/write command. The default value is 0 (no implied seek).
EFIFO: Enable FIFO. When EFIFO=1, the FIFO is disabled (NEC765A compatible mode). This means data is transferred on a byte by byte basis. The default value is 1 (FIFO disable).
POLL: Disable Polling. When POLL=1, polling of the drives is disabled. POLL defaults to 0 (polling enable). When enabled, a single interrupt is generated after reset.
FIFOTHR: The FIFO threshold in the execution phase of a read/write command. This is programmable from 1 to 16 bytes. FIFOTHR defaults to 00. A 00h selects one byte and 0Fh selects 16 bytes.
PRETRK: Precompensation start track number. Programmable from track 0 to 255. PRETRK defaults to track 0. A 00h selects track 0 and a FFh selects track 255.

4.4.2.6.18 Powerdown Mode

The Powerdown mode command allows the automatic power management. The use of the command can extend the battery life in portable PC applications. To enable auto powerdown the command may be issued during the BIOS power on self test (POST).
DLY: Minimum powerup timer. This bit is active only if APD bit is enabled. Set this bit to 0 assigns a 10msec timer, and to 1 assigns a 0.5sec timer. The timer will be re-initialized after a command execution is finished (idle state) and start to countdown. When the timer is expired, the FDC will enter the powerdown state automatically.
APD: Enable auto powerdown. When set to 1, the auto powerdown is enabled.

4.4.2.6.19 Lock

The Lock command allows the user full control of the FIFO parameters after a software reset. If the LOCK bit is set to 1, then the EFIFO, FIFOTHR and PRETRK bits in the Configure command are not affected by a software reset.
After the command byte is written, the result byte must be read before continuing to the next command.

4.4.2.6.20 Invalid

If an invalid command (illegal Opcode byte in the command phase) is received by the controller, the controller responds with ST0 in the Result Phase. The controller does not generate an interrupt during this condition. The system reads an 80h from ST0 indicating an invalid command was received.

4.4.2.6.21 Perpendicular Mode

The Perpendicular Mode command is designed to support the Perpendicular Recording disk drives (4Mbytes unformatted capacity). The Perpendicular Mode command configures each of the four logical drives as a perpendicular or conventional disk drive. Configuration of the four logical disk drives is done via the D3-D0 bits, or with the GAP and WG control bits. This command should be issued during the initialization of the floppy controller.
A 0 written to Dn sets drive n to conventional mode, and a 1 sets drive n to perpendicular mode. Also, the OW bit offers additional control. When OW=1, changing the values of D3-D0 is enabled. When OW=0, the internal values of D3-D0 are unaffected, regardless of what is written to D3-D0.
The function of the Dn bits must also be qualified by setting both WG and GAP to 0. If WG and GAP are not set to 00, they override whatever is programmed in the Dn bits. Table 4-4 below indicates the operation of the FDC based on the values of GAP and WG. D3-D0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset. A hardware reset resets all the bits to zero.

Table 4-4 Effects of WG and GAP bits

GAP	WG	Mode	GAP2 Length during Format	Portion of GAP2 re-written by Write Data Command
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1Mbps)	41 Bytes	38 Bytes

4.4.2.6.22 Parallel Port FDC

In this mode, the floppy disk control signals are available on the parallel port pins. When this mode is selected, the parallel port is not available. There are four modes of operation. These modes can be selected in configuration register 0xF1.

0xF1[1:0]		Parallel port function
0	0	printer
0	1	printer
1	0	FDC(drive 0 or 1)
1	1	FDC(drive 1)

The FDC signals are multiplexed onto the Parallel port pins as shown in table below.

Conn Pin no.	Chip pin no.	SPP mode	Type	FDC mode	Pin direction
1	65	STBJ	I/O	DS0J	O
2	59	PD0	I/O	INDEXJ	I
3	58	PD1	I/O	TRK0J	I
4	57	PD2	I/O	WPJ	I
5	56	PD3	I/O	RDATAJ	I
6	50	PD4	I/O	DSKCHGJ	I
7	49	PD5	I/O		
8	48	PD6	I/O	MTR0J	O
9	47	PD7	I/O		
10	54	ACKJ	I	DS1J	O
11	53	BUSY	I	MTR1J	O
12	52	PE	I	WDATAJ	O
13	51	SLCT	I	WGATEJ	O
14	64	AFDJ	I/O	DENSEL	O
15	63	ERRJ	I	HDSELJ	O
16	62	INITJ	I/O	DIRJ	O
17	61	SLINJ	I/O	STEPJ	O

4.4.3 Serial Port Registers

Each of the serial ports function as data input/output interface in a microcomputer system. The system software determines the functional configuration of the UARTs via a tri-state 8-bit bi-directional data bus.

The UARTs are completely independent and perform serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of any of the UARTs at any time during the functional operation. Status information reported includes the type and condition of the transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UARTs have programmable baud rate generator capable of dividing the timing reference clock input by divisors of 1 to (2^{16} - 1), and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16 X clock to drive the receiver logic. The UARTs have complete modem-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle communications link.

Table 4-4-31 lists the register addresses A2 ~ A0 (AEN is equal to zero). DLAB is the divisor latch access bit.

Table 4-4-31 Serial Port Registers

Register Address	Access (AEN=0)	Abbreviation	Register Name	Access
Base +	DLAB			
0h	0	THR	Transmit Holding Register	W
0h	0	RBR	Receiver Buffer Register	R
0h	1	DLL	Divisor Latch LSB	R/W
1h	1	DLM	Divisor Latch MSB	R/W
1h	0	IER	Interrupt Enable Register	R/W
2h	-	IIR	Interrupt Identification Register	R
2h	-	FCR	FIFO Control Register	W
3h	-	LCR	Line Control Register	R/W
4h	-	MCR	Modem Control Register	R/W
5h	-	LSR	Line Status Register	R
6h	-	MSR	Modem Status Register	R
7h	-	SCR	Scratch Pad Register	R/W

Table 4-4-32 Register Summary for Each UART Channel

Bit no.			0	1	2	3	4	5	6	7
0 DLAB=0	Receiver Buffer Register (Read only)	RBR	Data bit 0 (note 1)	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
0 DLAB=0	Transmitter Holding Register (Write only)	THR	Data bit 0	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
1 DLAB=0	Interrupt Enable Register	IER	Enable received data available interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Modem Status Interrupt (EMSI)	0	0	0	0
2	Interrupt Ident. Register (Read only)	IIR	'0' if interrupt pending	Interrupt ID bit	Interrupt ID bit	0	0	0	FIFO enable	FIFO enable
2	FIFO control register (write only)	FCR	FIFO enable	RCVR FIFO Reset	Xmit FIFO reset	reserved	reserved	reserved	RCVR Trigger (LSB)	RCVR Trigger (MSB)
3	Line control register	LCR	Word length select bit 0 (WLS0)	Word Length Select bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
4	Modem control register	MCR	Data Terminal Ready (DTR)	Request to send (RTS)	Out 1 (Note 2)	IRQ Enable (Note 2)	Loop	0	0	0
5	Line status register	LSR	Data ready (DR)	Overrun error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT)	Error in RCVR FIFO
6	Modem status register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)	Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
7	Scratch register	SCR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0 DLAB=1	Divisor latch (LS)	DLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 DLAB=1	Divisor latch (MS)	DLM	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 1. Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
2. This bit no longer has a pin associated with it.

4.4.3.1 Line Control Register (LCR)

The system programmer uses this read/write register to specify the format of the asynchronous data communications exchange and set the divisor latch access bit.

Table 4-4-33 LCR Registers

Bit	Function
7	Divisor latch access bit (DLAB). 1 = To access divisor latches of the baud generator or the alternate function register during a read or write operation. 0 = To access any other register.
6	Break control bit. This bit causes a break condition to be transmitted to the receiving UART. 1 = Serial output (SOUT) is forced to the spacing logic 0 = Break is disabled This bit acts only on SOUT and has no effect on transmitter logic. This enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters are transmitted because of the break: 1. Load all 0s, pad character in response to THRE. 2. Set break after the next THRE. 3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration.
5	Stick parity bit. When parity is enabled, it is used in conjunction with bit 4 to select, mark or space parity. 1 = Enable stick parity 0 = Disable stick parity
4	Parity select bit. Selects either an odd or even number of 1's to be transmitted/checked in the data word bit and parity bit. 0 = Odd number of 1's (parity bit is a logic 1, mark parity) 1 = Even number of 1's (parity bit is a logic 0, space parity)
3	Parity enable bit. The parity bit is used to produce an even or odd number of 1's when the data bits and the parity bit are summed. A parity bit is generated (transmit data) or checked (received data) between the last data bit and the stop bit of the serial data. 0 = Parity bit is not generated/checked 1 = Parity bit is generated/checked
2	Specifies the number of stop bits transmitted with each serial character. The receiver checks the first stop bit only, regardless of the number of stop bits selected. 0 = 1 stop bit 1 = 1.5 stop bits, when a 5-bit data length is selected 1 = 2 stop bits, when 6-, 7-, or 8-bit data length is selected
0-1	Specify the number of data bits (data length) in each transmitted or received serial character. The following are the bit values: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

4.4.3.2 Programmable Baud Generator

The UART contains two independently programmable baud generators. The 24-MHz crystal oscillator frequency input is divided by 13, resulting in a frequency of 1.8462-MHz. This is sent to each baud generator and divided by the divisor for the associated UART. The output frequency of the baud generator is 16 X the baud rate, [divisor # = (frequency input) / (baud rate x 16)]. The output of each baud generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization to ensure proper operation of the baud generator. Upon loading either of the divisor latches, a 16-bit baud counter is loaded.

Table 5-5 provides decimal divisors to use with crystal frequencies of 24-MHz. The oscillator input to the chip should always be 24-MHz to ensure that the FDC timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

4.4.3.3 Line Status Register (LSR)

This register provides status information to the CPU concerning the data transfer. LSR is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

Table 4-4-34 Line Status Register Function Definition

Bit	Function
7	In FIFO off mode, this bit is set to 0. In FIFO, LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU read the LSR, if there are no subsequent errors in the FIFO.
6	**Transmitter empty (TEMT) indicator**. It is set to 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to 0 whenever either the THR or TSR contains a data character.
5	**Transmitter holding register empty (THRE) indicator**. It indicates that the UART is ready to accept a new character for transmission. It also causes the UART to issue an interrupt to the CPU when the THRE interrupt enable is set high. It is set to 1 when a character is transferred from the THRE into TSR. It is reset to 0 whenever the CPU loads the THRE.
4	**Break interrupt (BI) indicator**. It is set to 1 when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit data bits parity stop bits). It is reset whenever the CPU reads the contents of the LSR. Restarting after a break is received requires the SIN pin to be logical 1 for at least 1/2-bit time.
3	**Framing error (FE) indicator**. This bit indicates that the received character did not have a valid stop bit. It is set to 1 whenever the stop bit following the last data bit or parity bit is a logic 0 (spacing level). The FE indicator is reset whenever the CPU reads the contents of LSR. The UART tries to resynchronize after a framing error. To do this, it assumes that the FE was due at the next start bit, so it samples this start bit twice and then takes in the data.
2	**Parity error (PE) indicator**. This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. It is set to 1 upon detection of a parity error and reset to 0 whenever the CPU reads the contents of the LSR.
1	**Overrun error (OE) indicator**. It indicates that data in the RBR was not read by the CPU before the next data was transferred into the RBR, thereby destroying the previous data. It is set to 1 upon detection of an overrun condition and reset to 0 whenever the CPU reads the contents of the LSR.
0	**Receive data ready (DR) indicator**. It is set to 1 whenever a complete incoming character has been received and transferred into the RBR. It is reset to 0 by reading the data in the RBR.

Table 4-4-35 Baud rates using 1.8462 MHz Clock (24 MHz/13)

Desired baud rate	Divisor used to generate 16x clock	C	Bit 1 in 0xF0 of LDN4 or 5
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note: C refers to % Error Difference between desired and actual, except where shown otherwise, is 0.2 %.

4.4.3.4 Interrupt Identification Register (IIR)

This register keeps a record of the four interrupts prioritized by the UART to reduce software overhead during data transfers. The four levels of interrupt conditions in order of priority are: receiver-line-status, received-data-ready, transmitter-holding-register-empty, and modem-status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete.

Table 4-4-36 Interrupt Identification Register

Bit	Function
7~6	These two bits are set when the FIFO control register bit 0 equals 1.
5~4	Always '0'.
3	In non-FIFO mode, this bit is a logic 0. In FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
2~1	Identifies the highest interrupt pending.
0	Used in an interrupt environment to indicate whether an interrupt condition is pending. If yes, the IIR contents may be used as a pointer to the appropriate interrupt service routine. 0 = Interrupt pending 1 = No interrupt pending

Table 4-4-37 Interrupt Control Table

FIFO mode only	Interrupt ID. register	Interrupt Set and Reset Functions			
D3	D2-D1-D0	**Priority level**	**Interrupt type**	**Interrupt source**	**Interrupt Reset control**
0	0- 0- 1	-	None	None	-
0	1- 1- 0	highest	Receiver line status	Overrun error, Parity error, Framing error Break interrupt	Reading the line status register
0	1- 0- 0	second	Received data available	Received data available	Read receiver buffer or the FIFO drops below the trigger level
1	1- 0- 0	second	Character timeout Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time.	Reading the Receiver Buffer Register
0	0- 1- 0	third	Transmitter holding register empty	Transmitter Holding Register Empty	Reading the IIR Register or writing the transmitter holding register
0	0- 0- 0	fourth	MODEM status	Delta	Reading the Modem status register

4.4.3.5 Interrupt Enable Register (IER)

This register enables the four types of UART interrupts. Each interrupt can individually activate the UR2IRQ or UR1IRQ output signal. Resetting bits 0 ~ 3 of the IER disables the interrupt system. Similarly, setting bits of this register to 1 enables the selected interrupts. Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the interrupt output signal. All other system functions operate in their normal manner, including the setting of the line status and modem status registers.

Table 4-4-38 Interrupt Enable Register

Bit	Function
0	Enables the received-data-available interrupt
1	Enables the THRE interrupt
2	Enables the receiver-line-status interrupt
3	Enables the modem-status interrupt
4-7	Always 0

4.4.3.6 FIFO Control Register

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs. When changing from FIFO mode to non-FIFO mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.
Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.
Bit 3: Reserved.

Bit 4, 5: FCR4 to FCR5 are reserved for future use.
Bit 6, 7: FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

4.4.3.7 Modem Control Register (MCR)

This register controls the interface with the modem or data set (or a peripheral emulating a modem).

Table 4-4-39 Modem Control Register

Bit	Function
7~5	Set to logic 0.
4	This bit provides a local loopback feature for the UART diagnostic testing. When set to 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is looped back into the receiver shift register input; the four modem control inputs (DSRJ, CTSJ, RIJ, and DCDJ) are disconnected; and the DTR, RTS, OUT1, IRQ enable bits in MCR respectively. The modem control output pins are forced to their high (inactive) states. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-receive data paths of the serial port. In the diagnostic mode, UARTIRQs are not operational. The modem status interrupts are operational, but the interrupt's sources are the lower four bits of MCR instead of the four modem control inputs. Writing a 1 to any of them causes an interrupt. The interrupts are still controlled by the IER.
3	This bit enables the interrupt when set. In local loopback mode, this bit controls bit 7 of the MSR.
2	This is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In local loopback mode, this bit controls bit 6 of the MSR.
1	Controls the RTSJ output. In local loopback mode, this bit controls bit 4 of the MSR. 1 = DTRJ output is forced to 0 0 = DTRJ output is forced to 1
0	Controls the DTRJ output. In local loopback mode, this bit controls bit 5 of the MSR. 1 = DTRJ output is forced to 0 0 = DTRJ output is forced to 1

4.4.3.8 Modem Status Register (MSR)

This register gives the current state of the control lines from the modem to the CPU. The bits 3-0 are set to 1 whenever a control input from the modem changes state, and set to 0 when CPU reads the MSR.

Table 4-4-40 Modem Status Register

Bit	Function
7	Complement of the DCDJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to IRQ enable in the MCR.
6	Complement of the RIJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	Complement of the DSRJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	Complement of the CTSJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	Delta data carrier detect (DDCD) indicator indicates that the DCDJ input to the chip has changed state. Whenever bit 0, 1, 2 or 3 is set to 1, a modem status interrupt is generated.
2	Trailing edge of ring indicator (TERI) detector indicates that the RIJ input of the chip has changed from a low to high state.
1	Delta data set ready (DDSR) indicator indicates that the DSRJ input to the chip has changed its state since the last time it was read by the CPU.
0	Delta clear to send (DCTS) indicator indicates that CTSJ input to the chip has changed its state since the last time it was read by CPU.

4.4.3.9 Scratchpad Register (SCR)

The 8-bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

4.4.3.10 Infrared Interface

The M1543 with Built-in Super I/O's infrared interface provides a two-way wireless communications port using infrared as a transmission medium. Two infrared implementations have been provided in the IrDA and Amplitude Shift Keyed IR.

IrDA allows serial communication at baud rates up to 115K baud. Each word is sent serially beginning with a zero value start bit. A zero is signalled by sending a single infrared pulse at the beginning of the serial bit time. A one is signalled by sending no infrared pulse during the bit time.

The Amplitude Shift Keyed infrared allows serial communication at baud rates up to 19.2K baud. Each word is sent serially beginning with a zero value start bit. A zero is signalled by sending a 500 KHz waveform for the duration of the serial bit time. A one is signalled by sending no transmission at bit time.

4.4.5 Parallel Port

4.4.5.1 Parallel Port Interface

The M1543 with Built-in Super I/O incorporates one IBM XT/AT compatible parallel port. The M1543 with Built-in Super I/O supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Please refer to the Configuration Description (Section 4) for information on disabling, powerdown, changing the base address of the parallel port, and selecting the mode of operation.

The M1543 with Built-in Super I/O also incorporates a pad protective circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports with their associated registers and control gating. The control and data ports are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below :

DATA PORT BASE ADDRESS + 00H
STATUS PORT BASE ADDRESS + 01H
CONTROL PORT BASE ADDRESS + 02H
EPP ADDR PORT BASE ADDRESS + 03H
EPP DATA PORT 0 BASE ADDRESS + 04H
EPP DATA PORT 1 BASE ADDRESS + 05H
EPP DATA PORT 2 BASE ADDRESS + 06H
EPP DATA PORT 3 BASE ADDRESS + 07H

The bit map of these registers :

Table 4-4-41 Bit Mapped Registers

Data Port	D0	D1	D2	D3	D4	D5	D6	D7	Note
	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
Status Port	TMOUT	0	OSLC	ERRJ	SLCT	PE	ACKJ	BUSYJ	1
Control Port	STROBE	AUTOFD	INITJ	SLC	IRQE	PCD	0	0	1
EPP ADDR Port	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 0	PD0	PD1	PD2	DP3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3
EPP DATA Port 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2, 3

Note 1: These registers are available in all modes.
2: These registers are only available in EPP mode.
3: For EPP mode, IOCHRDY must be connected to the ISA bus.

Table 4-4-42 Parallel Port Connector

HOST Connector	STANDARD	EPP	ECP
1	StrobeJ	WriteJ	StrobeJ
2-9	PData <0:7>	PData <0:7>	PData<0:7>
10	AckJ	Intr	Ack
11	Busy	WaitJ	Busy,PeriphAck(3)
12	PE	(NU)	PError, nAckReverse(3)
13	Select	(NU)	Select
14	AutofdJ	DSTRBJ	AutoFd, HostAck(3)
15	ErrorJ	(NU)	Fault(1) PeriphRequest(3)
16	InitJ	(NU)	Init(1) ReverseRqst(3)
17	SelectinJ	AstrbJ	Selectin(1,3)

(1) = compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.09, Jan. 7, 1993. This document is available from Microsoft.

4.4.5.2 IBM XT/AT Compatible, Bi-Directional and EPP Modes

DATA PORT Address Offset = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus with the rising edge of the IOWJ input. The contents of this register are buffered (non inverting) and output onto the PD0 -PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

STATUS PORT Address Offset = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an IORJ read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT
This bit is valid in EPP mode only and indicates that a 10 µsec time out has occurred on the EPP bus. A logic 0 means that no time out error has occurred; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

BITS 1, 2 - are not implemented as register bits. During a read of the Printer Status Register, these bits are at low level.

BIT 3 ERRJ - ERRORJ
The level on the ERRORJ input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 ACKJ - ACKNOWLEDGEJ
The level on the ACKJ input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the Printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 BUSYJ - BUSYJ
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

CONTROL PORT Address Offset = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the STROBEJ output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the AUTOFDJ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 INITJ - INITIATE OUTPUTJ
This bit is output onto the INITJ output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the SLCTINJ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going ACKJ input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is valid in extended mode only (PS2, EPP and ECP). In printer mode, the direction is always out regardless of the state of this bit. In bi-directional mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

EPP ADDRESS PORT Address Offset = 03H
The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PDO - PD7 ports, the leading edge of IOWJ causes an EPP Address WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP Write cycle. During a READ operation, PDO -PD7 ports are read, the leading edge of IOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the Pdata for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 0 Address Offset = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non-inverting) and output onto the PD0 - PD7 ports, the leading edge of IOWJ causes an EPP DATA WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0- PD7 ports are read, the leading edge of IOR causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the Pdata for the duration of the IOR cycle. This register is only available in EPP mode. To maintain compatibility with Intel's 82360SL device that has 32-bit Host bus interface, four consecutive byte address locations (data port 0~4) are provided for transferring data.

EPP DATA PORT 1 Address Offset = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Please refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 2 Address Offset = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Please refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 3 Address Offset = 07H

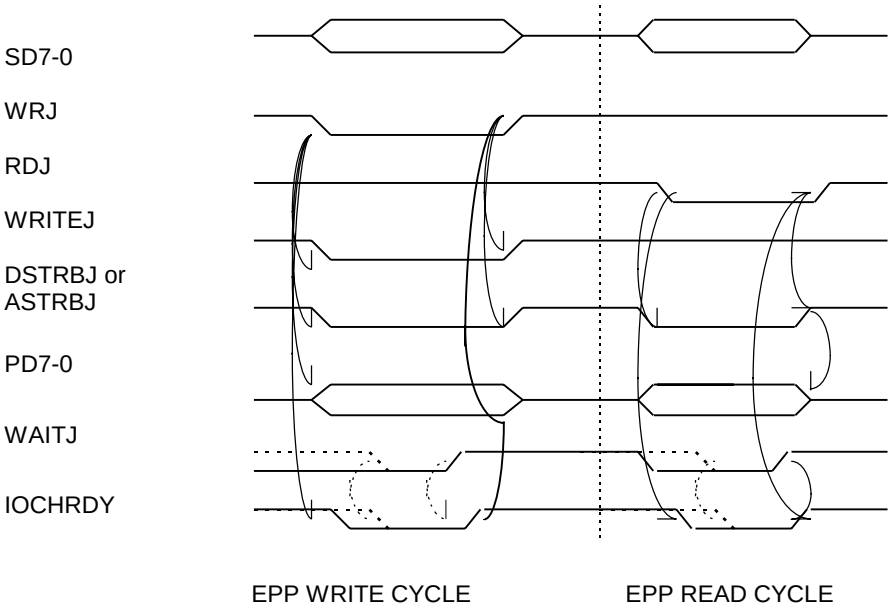
The EPP Data Port 3 is located at an offset of '07H' from the base address. Please refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10 usec have elapsed from the start of the EPP cycle (IORJ or IOWJ asserted) WAITJ will be deasserted. If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

EPP mode version 1.7 Timing



The timing for a Write/Read EPP 1.7 operation is shown in timing diagram above
The sequence of operation is:

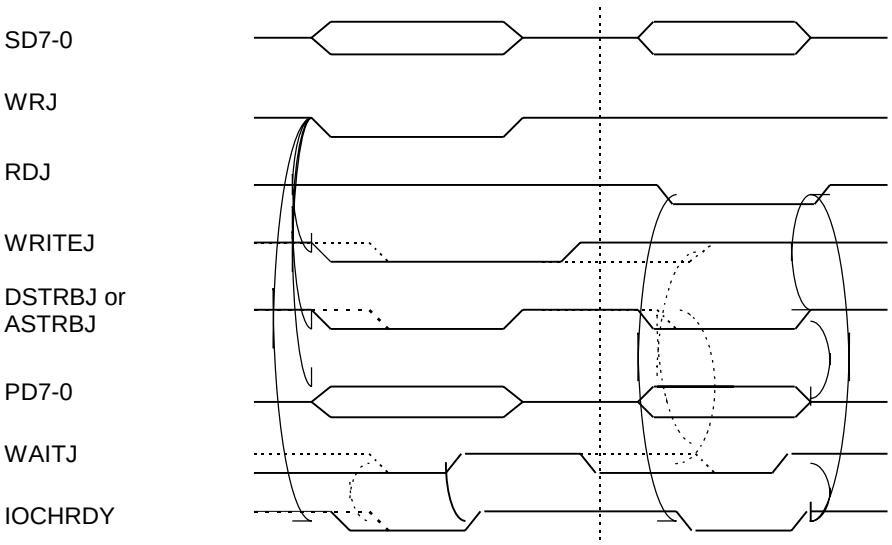
EPP 1.7 Data/Address Write

1. The host writes a byte to Data (Address) port. WRJ goes low to drive data to PD7-0.
2. The EPP pulls WRITEJ low to indicate it's a write cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to signal that data is valid.
4. If WAITJ goes low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then WRJ will go high
6. When WRJ goes high, it pulls WRITEJ & DSTRBJ(ASTRBJ) high, and then the EPP can change PD7-0

EPP 1.7 Data/Address Read

1. The host reads a byte from Data (Address) port. RDJ goes low to input data from PD7-0.
2. The EPP keeps WRITEJ high to indicate it's a read cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that peripheral have to start sending data.
4. If WAITJ is low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then RDJ will go high
6. When RDJ goes high, it pulls DSTRBJ(ASTRBJ) high, and then the peripheral can tri-state PD7-0

EPP mode version 1.9 Timing



EPP WRITE CYCLE EPP READ CYCLE

The timing for a Write/Read EPP 1.9 operation is shown in timing diagram above
The sequence of Write/Read operation is:

EPP 1.9 Data/Address Write

1. The host writes a byte to Data (Address) port. WRJ goes low to drive data to PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low or already low, the EPP pulls or keeps WRITEJ low to show being a write cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that data is ready and waits for WAITJ to go high.
5. When WAITJ goes high, the EPP pulls IOCHRDY high, and then WRJ will go high to turn off this cycle.
6. When WRJ goes high, it pulls DSTRBJ (ASTRBJ) high, and then the EPP can change PD7-0

EPP 1.9 Data/Address Read

1. The host reads a byte from Data (Address) port. RDJ goes low to input data from PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low or was already low, the EPP pulls or keeps WRITEJ high to indicate being a read cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to signal the peripheral to start sending data and waits for WAITJ to go high.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then RDJ will go high
6. When RDJ goes high, it pulls DSTRBJ (ASTRBJ) high, and then the peripheral can tri-state PD7-0

Table 4-4-43- EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
WRITEJ	WriteJ	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/ Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP.)
WAIT	WaitJ	I	This signal is active low. It is driven inactive as a positive acknowledgment from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	DATA StrobeJ	O	This signal is active low. It is used to denote data read or write operation.
RESET	ResetJ	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	Address StrobeJ	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Select Status	I	Same as SPP mode.
ERRJ	Error	I	Same as SPP mode.
PDIR	Parallel Port Direction	O	This output shows the direction of the data transfer on the parallel port bus. A low means an output /write condition and a high means an input/read condition. This signal is normally a low (output/write) uniess PCD of the control register is set or if an EPP read cycle is in progress.

Note 1: SPP and EPP can use 1 common register.
Note 2: WriteJ is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

4.4.5.3 Extended Capabilities Parallel Port

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

- High performance half-duplex forward and reverse channel
- Interlocked handshake, for fast reliable transfer
- Optional single byte RLE compression for improved throughput (64:1)
- Channel addressing for low-cost peripherals
- Maintains link and data layer separation
- Permits the use of active output drivers
- Permits the use of adaptive signal timing
- Peer-to-peer capability

PWord A port word; equal in size to the width of the ISA interface. For this implementation, PWord is always 8 bits.
1 A high level.
0 A low level.

These terms may be considered synonymous:

- PeriphClk, AckJ
- HostAck, AutoFdJ
- PeriphAck, Busy
- PeriphRequestJ, FaultJ
- ReverseRequestJ, InitJ
- AckReverseJ, PError
- Xflag, Select
- ECPMode, SelectinJ
- HostClk, StrobeJ

Vocabulary
The following terms are used in this document:
assert When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward Host to Peripheral communication.
reverse Peripheral to Hose communication.

Reference Document

IEEE 1284 Extended Capabilities Port Protocol
and ISA Interface Standard, Rev 1.09, Jan 7, 1993. This document is available from Microsoft.
The bit map of the Extended Parallel Port registers is :

	D7	D6	D5	D4	D3	D2	D1	D0	Note
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/ RLE	Address or RLE field							2
dsr	BusyJ	AckJ	PError	Select	FaultJ	0	0	0	1
dcr	0	0	Direction	ackIntEn	Selectin	InitJ	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	IRQ Channel			DMA Channel			
ecr	MODE			ErrintrEnJ	DmaEn	Service Intr	full	empty	

Note 1: These registers are available in all modes.
Note 2: All FIFOs use one common 16 byte FIFO.

ISA IMPLEMENTATION STANDARD

This specification describes the standard ISA interface to the Extended Capabilities Port (ECP). All ISA devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.09, Jan. 7, 1993. This document is available from Microsoft.

Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to be implemented. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Decompression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 4-4-44 ECP Pin Descriptions

Name	Type	Description
StrobeJ	O	During write operations, StrobeJ registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
AckJ	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with AutoFdJ in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with StrobeJ in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with StrobeJ. PeriphAck also provides command information in the reverse direction.
PError (Ack ReverseJ)	I	Used to acknowledge a change in the direction the transfer (asserted= forward). The peripheral drives this signal low to acknowledge ReverseRequestJ. It is an "interlocked" handshake with ReverseRequestJ. The host relies upon AckReverseJ to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
AutoFdJ (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with AckJ in the reverse direction. This signal indicates whether the data lines contain ECP address or data, the host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with AckJ. HostAck also provides command information in the forward phase.
FaultJ (Periph RequestJ)	I	Generates an error interrupt when asserted. This signal provides a mechanism or peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
InitJ	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and SelectlnJ is high.
SelectlnJ	O	Always deasserted in ECP mode.

Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ECR. The table below lists these dependencies. Operation of the devices in modes other than those specified is undefined.

Table 4-4-45 ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 4-4-46 Mode Descriptions

Mode	Description*
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	(Reserved)
110	Test mode
111	Configuration mode

* Refer to ECR Register Description

DATA and ECPAFIFO PORT Address Offset = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the IOWJ input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO- Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet.

Device Status Register (DSR) Address Offset = 01H

The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status port are defined as follows:

BIT 3 FaultJ
The level on the Fault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 AckJ
The level on the AckJ input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 BusyJ
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

Device Control Register (DCR) Address Offset = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the STROBEJ output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the AUTOFDJ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 INITJ - INITIATE OUTPUT
This bit is output onto the INITJ output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the SLCTINJ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 acklntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the ACKJ input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION
If mode = 000 or mode = 010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

CFIFO (Parallel Port Data FIFO) Address Offset = 400h

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ECPDFIFO (ECP Data FIFO) Address Offset = 400h

Mode = 011
Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

TFIFO (Test FIFO Mode) Address Offset =400H

Mode = 110
Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the tFIFO will not be transmitted to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntr Threshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntr Threshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

CNFGA (Configuration Register A) Address Offset = 400H

Mode = 111
This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (Pword = 1 byte)

CNFGB (Configuration Register B) Address Offset = 401H

Mode = 111
BIT 7 compress
This bit is read only. During a read, it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression.

BIT 6 IntrValue
Returns the value on the ISA IRQ line to determine possible conflicts.

BITS 5~0 : The ECP Parallel port Configuration register B must reflect the IRQ and DRQ selected by the Configuration registers

IRQ selected	Config.Reg. B Bits 5: 3
14	110
13	101
11	100
10	011
9	010
7	001
5	111
Others	000

DMA selected	Config.Reg. B Bits 2: 0
3	011
2	010
1	001
Others	000

ECR (Extended Control Register) Address Offset = 402H

Mode = all
This register controls the extended ECP parallel port functions.

BITS 7, 6, 5
These bits are Read/Write and select the Mode.

BIT 4 ErrIntrEnJ
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of FaultJ.
0: Enables an interrupt pulse on the high to low edge of FaultJ. Note that an interrupt will be generated if Fault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disable DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disable DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred, serviceIntr bit shall be set to a 1 by hardware, it must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.
case dmaEn = 1:
During DMA (this bit is set to a 1 when terminal count is reached).
case dmaEn = 0 direction = 0:
This bit shall be set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.
case dmaEn = 0 direction = 1:
This bit shall be set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

BIT 1 full
Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty
Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

Table 4-4-47 - Extended Control Register

R/W	Mode
000	Standard Parallel Port mode. In this mode the FIFO is reset and common collector drivers are used on the control lines (StrobeJ, AutoFdJ, InitJ and SelectlnJ). Setting the direction bit will not tri-state the output drivers in this mode.
001	PS/2 Parallel Port mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010	Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register CR4. All drivers have active pull-ups (push-pull)
101	Reserved
110	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

OPERATION
Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001) hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert AutoFdJ independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:
. Set Direction = 0, enabling the drivers.
. Set strobe = 0, causing the StrobeJ signal to default to the deasserted state.
. Set autoFd = 0, causing the AutoFdJ signal to default to the deasserted state.
. Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ECPAFIFO or ECPDFIFO respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel., setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be changed into the forward direction.

Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8-bit data or 8-bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8-bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address. When in the reverse direction, normal data is transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low.
The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 4-4-48

Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	**D[6:0]**
0	Run-Length Count (0-127) (mode 0011 0x00 only)
1	Channel Address (0-127)

Data Compression

The M1543 with Built-in Super I/O supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. a run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition
The drivers for StrobeJ, AutoFdJ, InitJ and SelectlnJ are open-collector in mode 000 and are push-pull in all other modes.

ISA Connections

The interface can never stall causing the host to hang. The width of data transfers if strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section.) Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

Interrupts

The interrupts are enabled by servicelntr in the ecr register.

servicelntr = 1 Disables the DMA and all of the service interrupts.

servicelntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.

An interrupt is generated when:

1. For DMA transfers: When servicelntr is 0, dmaEn is 1 and the DMA TC is received.

2. For Programmed I/O:
   a. When servicelntr is 0, dmaEn is 0, direction is 0 and there are writelntr Threshold or more free bytes in the FIFO. Also, an interrupt is generated when servicelntr is cleared to 0 whenever there are writelntr Threshold or more free bytes in the FIFO.

   b. (1) When servicelntr is 0, dmaEn is 0, direction is 1 and there are readlntr Threshold or more bytes in the FIFO. Also, an interrupt is generated when servicelntr is cleared to 0 whenever there are readlntr Threshold or more bytes in the FIFO.

3. When nErrlntrEn is 0 and nFault transitions from high to low or when nErrlntrEn is set from 1 to 0 and nFault is asserted.

4. When acklntEn is 1 and the nAck signal transitions from a low to a high.

FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Model. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or PDRQ depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e.2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.
A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting PDACKJ and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until PDACKJ is deasserted for a minimum of 350 nsec. (**Note** : The only way to properly terminate DMA transfers is with a TC.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode - Transfers from the FIFO to the Host

(**Note**: In the reverse mode, the peripheral may not continue to fill the FIFO if it turns out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by PDACKJ), indicating that no more data is required. PDRQ goes inactive after PDACKJ goes active for the last byte of a data transfer (or on the active edge of IORJ, on the last byte, if no edge is present on PDACKJ). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and serviceIntr has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle.)

Programmed I/O Mode or Non-DMA Mode

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000h or from the ecpDFifo located at 400H, or to/ from the tFifo at 400H to use the programmed I/O transfers, the host first sets up the direction and state, then sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the PINTR point. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note : A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

Programmed I/O - Transfers from the FIFO to the Host

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntr Threshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntr Threshold bytes may be read from the FIFO in a single burst.

Programmed I/O - Transfers from the Host to the FIFO

In the forward direction, an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit need to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

The FIFO threshold value is selected via <THR> = Logic Device No. 3 <0xF0h bit6-3>

The readIntr Threshold = {
- 16 data bytes FIFO, if <THR>=0
- <THR> data bytes FIFO, if <THR> =1 to 15

For example, if the <THR>=4, then the serviceIntr is set whenever there are 4-16 bytes in the FIFO.

The writeIntr Threshold = {
- 16 free bytes FIFO, if <THR>=0
- <THR> free bytes FIFO, if <THR>=1 to 15

For example, if the <THR>=4, then the serviceIntr is set whenever there are 4-16 bytes free in the FIFO.

Section 5: Power Management Unit Programming Guide

There are two important parts in Power Management Unit of M1543. They are Legacy Power Management Unit and Advanced Configuration and Power Interface Specification (abbreviated as ACPI). The details of both are listed below.

5.1 Legacy Power Management Unit

A. Top View.
B. Timers.
C. Event Configuration.
D. External Switches.
E. Clock Control.
F. General Purpose Input/Output.
G. SMI control.
H. Others.

A. Top View.
The Legacy Power Management Unit based on the default functions of M1533, gives minimum requirements for the desktop. It can be divided into several parts.
When talking about the traditional power management, as it is familiar to every one, the SMI or SMM. It is the major method of how the BIOS communicates with the hardware. The SMI sources are all included in Configuration Space of offset 0x40h-0x53h. ("offset 0xxxh" means the registers of Configuration Space in Section 5.1 of this document.) There are two idle timer timeout SMIs, one APM timer timeout SMIs, IO traps, external switches SMIs and general purpose switch SMIs. The configuration of all timers are at offset 0x54h-0x5Dh. The monitored events of the timers and the IO traps are set at offset 0x60h-0x73h. Offset 0x74h is the status bit that indicates which event resets the Standby timer when system is in Standby State. Offset 0x75h-0x76h configures the busy condition of the PCI bus. The External Switches' event is configured at offset 0x80h-0x82h and 0x8Ch-0x8Eh. Furthermore, the programmable monitored IO/Memory range can be set at offset 0x94h-0x97h and 0xA4h-0xA5h.
Besides the SMI sources and the monitored events, CPU clock control is also an important method for power saving. M1543 supports Pentium and Pentium Pro clock control. It can transfer the CPU into STPGNT or STPCLK states. Besides, system clock controls such as clock throttling function are also supported. Most of all, the Auto Thermal throttling can be enabled to prevent system overheat. All of the configuration registers are at 0x78h-0x7Ch. Note that some configuration registers of throttling are set at offset 0x10h-0x13h of ACPI IO space.
Some other functions, such as Speaker control, etc., are set at offset 0B2h-0BEh.
Most important of all is the Suspend states supported. There are three states supported by M1543, namely the Power On Suspend, Suspend to DRAM and Suspend to Disk. An overview of design for suspend is introduced at ACPI.
The details of how to design the hardware or program the registers are described below.

B. Timers.

a. Standby timer and System state.
There are two states, ON & STANDBY, in this chip. The transition between both is determined by Standby timer and what events it monitors. The monitored events can be selected at offset 0x60h-0x64h and the Standby timer can be programmed at offset 0x54h. Assume Standby timer is programmed as 27 minutes and the monitored events as 01h. Then the timer begins to count immediately after being programmed. If there is any Primary HDD access (the enabled monitored event) detected before timeout, the timer will be reset. Otherwise, if it is timeout because no event occurs, it will stop and the system will transfer to STANDBY state. At the same time, the Standby timeout SMI is generated. If there is an event detected in STANDBY state, the timer will be reset to count again and a STANDBY to ON SMI will be generated. As soon as the SMI is generated, system will transfer to ON state. By the way, system states can be changed by reading or writing at offset 0xB2h, D0.
b. Display timer.
This timer is similar to the Standby timer except that it has no relation with the System state. If there is an enabled Display access event detected, the timer will be reset immediately no matter what state it is in. The only difference is that the Display timeout SMI is generated when no events are detected and the timer timeout, and Display Activity SMI is generated when there is an event detected after timeout. The timer can be configured at offset 0x59h and the monitored events at offset 0x64h-0x65h.

c. APM timers.
There is an APM timer that can be used for Advanced Power Management. It has two modes. When offset 0x55h, D6='0', the timer will generate an SMI when timeout and then stop until it is written again. When D6='1', the timer would reset to count again when timeout and generate SMI. The timer can be programmed at offset 0x55h.

Note : All of the monitored events monitored by the idle timers are masked when offset 0xC8h is set.

C. Event Configuration.
There are more than twenty events that should be configured before use. Listed below are those devices. Besides, some devices can monitor another GPI pin as an input event. Refer to offset 0x72h-0x73h.

a. Primary HDD.
This event monitors 01F0h-01F7h and 3F6h, optionally. When internal IDE is enabled, any IO cycle accessing it would be monitored, too. Besides, Primary DRQ can be enabled/disabled to be monitored at D0 of offset 0x6Ch.

b. Second HDD.
This event monitors 0170h-0177h and 376h, optionally. When internal IDE is enabled, any IO cycle accessing it would be monitored, too. Besides, secondary-DRQ can be enabled/disabled to be monitored at D1 of offset 0x6Ch.

c. Audio.
The audio access is decided by monitoring accesses to MIDI, SoundB, MS_Sound, ADLIB and GAME ports which are selected at D2-D15 of offset 0x6Ch-0x6Fh. Besides, whether DRQ is monitored or not is decided at D16-D21 of offset 0x6Ch-0x6Fh.

d. Video.
There are four sources of Video Events, including Memory access A0000-BFFFF, VCSJ and Graphic IO(3B0h-3DFh). VCSJ is an low active pin.

e. FDD.
The default monitor range of FDD Event is 3F0h-3F7h. It can be changed to 370h-377h by writing '1' to D0 of offset 0x68h. Besides, whether DRQ2 would be monitored is decided at D26 of offset 0x6Ch-0x6Fh.

f. Serial IO.
There are eight COM ports to be monitored at most. They can be enabled/disabled individually at D0-D7 of offset 0x70h.

g. Keyboard.
IO access ports 060h and 064h will generate Keyboard Event. Moreover, IRQ1 or IRQ12 can be monitored by enabling D27-D28 of offset 0x6Ch-0x6Fh.

h. Parallel IO.
Parallel IO Event monitors D8-D11 of offset 070h-071h. Note that only one of DRQ0, DRQ1 and DRQ3 can be monitored at once. It is selected at D1-D2 of offset 0x68h.

i. Memory Group Range.
There is one Programmable Monitored Memory ranges, MEMGPA. The first two are used as two single devices. MEMGPC is used as one of the Video Events. All three are programmable at offset 094h-09Fh. An example of how to program MEMGPA is shown below. The other two can be programmed similarly. Now, suppose there is a device that occupies memory range from 012340000h to 01235FFFFh. If D31-D14 of offset 0x94h-0x97h are the address bits of A[31:14], then it must be programmed as 0001_0010_0011_010X_XXb where 'X' means "don't care". Because D13-D4 are the masks of address bits A[23:14], it must be programmed as 00_0000_0111b. As a result, the written value is 012340070h.

j. IO Group Range.
There is one Programmable Monitored IO Range, IOGPC, that can be configured to monitor the programmed range or/and the IO ports 062h and 066h at D12-D13 of offset 070h-071h. An example of how to program IOGPC is shown below. The others can follow the steps. Suppose IO range 01230h-01237h is to be monitored. If D15-D2 of offset 0xA4h-0xA5h are the address bits of A[15:2], then it must be programmed as 0001_0010_ 0011_0Xb. Because D1-D0 are the masks of address bits A[3:2], it must be programmed as 01b. As a result, the written value is 01231h.

k. USB.
USB Event is generated when there is a device plugged in/out or the USB bus is busy.

Event	Corresponding Register
Primary Driver IO access	D7 of D8h-D9h Enable/Disable of internal IDE
Primary HDD event	Primary Driver IO access D0 of 6Fh-6Ch D0 of 73h-72h.
Secondary Driver IO access	D7 of D8h-D9h Enable/Disable of internal IDE
Secondary HDD event	Secondary Driver IO access D1 of 6Fh-6Ch D0 of 73h-72h
Audio IO access	D4-D15 of 6Fh-6Ch
Audio event	Audio IO access D16-D21 of 6Fh-6Ch
Video IO access	D25 of 6Fh-6Ch
Video Event	D22-D24 of 6Fh-6Ch Video I/O access D3 of 73h-72h
Floppy IO access	D0 of 68h
Floppy Event	D26 of 6Fh-6Ch D4 of 73h-72h
Serial IO access	D0-D7 of 71h-70h
Serial Event	D5 of 73h-72h Serial IO access
Keyboard IO access	Any access to IO port 60h, 64h
Keyboard Event	Keyboard IO access. D27-D28 of 6Fh-6Ch D6 of 73h-72h
Parallel IO access	D8-D10 of 071h-070h
Parallel IO event	D11 of 71h-70h D7 of 73h-72h Parallel IO access
IO group C IO access/ IOGP C event	Offset 0A5h-0A4h D12-D3 of 71h-70h
Memory group A event	Offset 097h -094h
RTC event	IRQ8J asserted
Ring IN event	Count number of Ring IN until matching offset B7h
BUS_ACT event	Offset 076h-075h

l. BUS_ACT.
BUS_ACT event is active when the PCI bus is busy. How frequent the PCI access can be defined is indicated in offset 0x75h-0x76h. Suppose D7-D0 is written as 80h and D13-D8 as 10h. Most of all, D14 should be set to '1' in advance. Then M1543 starts to count number of XTRDYJs in every period of 128 PCICLKs. If it is more than 16 XTRDYJs in the period, a BUS_ACT Event will be generated.

D. External Switches.
There are 2 specified External Switches because ACPWR is used as a hardware setting pin to select AT/ATX mode. For the specified External Switches, they can be programmed to be sensed by rising/falling/debounce at offset 0x80h-0x82h and 0x8Ch-0x8Eh. Moreover, some specified switches are used not only to generate SMI here, but also some other functions. For example, THERMALJ pin can be used as auto thermal throttle as described in the following section. In general, when rising (falling) is enabled and is sensed, then an SMI will be generated to inform CPU. When debounce circuit is enabled, the debounce clock of all switches can be selected at offset 0B4h, D6-D4.

E. Clock Control.
Before using any function of Clock Control, the Clock Control should be enabled first at D9 of offset 0x10h-0x13h of IO space. Every function is influenced by the Break Events selected at offset 0x7Ch of configuration space. Following are the Clock Control Functions supported by M1543.

a. Normal Throttle.
In addition to the Clock Control Enable described above, the Duty cycle should be configured in advance and then set Throttle Enable bit to start Normal Throttle. When it is enabled, the STPCLKJ deasserted and asserted periodically with 256µs/8µs period. The Break Events can deassert STPCLKJ immediately and reset the high/low timer. That is, STPCLKJ would start throttling again if there is no Break Event for a period of time. Only disabling the Throttle Enable bit can stop this function. By the way, all of the configured registers are at offset 0x10h-0x13h of IO space.

b. Auto Thermal Throttle.
It must be done first to program the Duty Cycle of offset 0x10h-0x13h of IO space and set D4 of offset 0x7Bh of configure space to Enable the Auto Thermal Throttle. When it is enabled and THERMALJ has asserted for 2 seconds, throttling is started. The Break Events can deassert STPCLKJ immediately and reset the high/low timer, too. Throttling is disabled immediately when THERMALJ has deasserted.

c. STPGNT
Before using STPGNT function, the D1-D0 of offset 0x7Bh of Configuration Space should be selected first. If Soft STPCLK is demanded, then D3 should be set to '0' to select STPGNT. Finally, READ offset 0xB2h of IO Space for Soft STPCLK or READ 0x14h for Processor Level 2 forces CPU input to the STPGNT state by asserting STPCLKJ. When SLEEPJ is enabled (D1 of offset 0x7Bh), timing of Pentium Pro is matched; otherwise, Pentium. Besides, ZZ is used to force L2 cache into Powerdown mode. STPCLKJ will be deasserted when any Break Event occurs. By the way, Soft STPCLK or READ LVL2 causes the same result.

d. STPCLK
Before using STPCLK function, the D1-D0 of offset 0x7Bh of Configure Space should be selected first. If Soft STPCLK is demanded, then D3 should be set to '1' to select STPCLK. Finally, READ offset 0xB2h of IO Space for Soft STPCLK or READ 0x15h for Processor Level 3 both forces CPU input the STPCLK state by asserting STPCLKJ, CPUSTPJ. They will be deasserted when any Break Event occurs. By the way, Soft STPCLK or READ LVL3 causes the same result.

Note: D5-D3 of offset 0x78h-0x79h are the CPU PLL time when CPU transfers from STPCLK state to STPGNT state.

F. General Purpose Input/Output.
There are 10 General Purpose Output pins, 6 General Purpose Input pins and 8 General Purpose IO pins. As most of these pins are multi-function pins, they must be enabled by programming offset 0x59h-0x5Bh of configuration space of device M1543 (not PMU) and offset 0xC6h of configuration space of device PMU.

a. GPI.
The input status of GPI pins can be read from offset 0xC4h-0xC5h.

b. GPO.
The output level of GPO pins can be programmed at offset 0xC0h-0xC3h.

c. GPIO[7:0].
1. Programming the directions of GPIO[7:0] at offset 0x7Dh.
2. Programming the output level of GPIOx at offset 0x7Eh, if it is configured as output.
3. Read the status of GPIOx at offset 0x7Fh, if it is configured as input.

G. SMI control.
a. ACPI mode/M7101 mode.
When set as ACPI mode, the status bit of any event is set as soon as the event occurs, no matter whether its corresponding enable/disable bit is set or not. As M7101 mode, the status bit is set if and only if both event occurs and the enable/disable bit is set. Set at D7 of offset 0x77h.
b. Soft SMI.
Write offset 0xB1h of IO space will generate Soft SMI. It can be delayed to generate Soft SMI if D2 of offset 0x77h is set.
c. Read/Write clear SMI.
When set as Read Clear SMI, all status port in configure space are cleared when read. As Write Clear SMI, writing '1' to the corresponding status bit can clear it. Set at D4 of offset 0x77h.
d. Delayed SMI.
SMI generated after a period of time when an SMI source is generated. Moreover, the SMI will be delayed again if there is any event monitored by Standby timer occurs. Only when no event occurs during that period of time, then SMI is generated.
1. Select Delayed time at D1-D0 of offset 0x77h.
2. Enable/Disable delayed SMI at D2 of offset 0x77h and D2&D0 of offset 0xD8h.

H. Others.
a. Write Beep function.
1. Enable D6 of offset 0xB3h.
2. Select Beep latency time at D5-D4 of offset 0xB3h.
3. Write 0xCAh to generate Beeps. A maximum of 3 writings are allowed in a time.
b. Periodical Beep function.
1. Enable D6 of offset 0xB3h.
2. Select Beep period at D1-D0 of offset 0xB3h.
3. Select Beep latency time at D3-D2 of offset 0xB3h.

Note : As soon as D3-D2 of offset 0xB3h are not "00", the Periodical Beep function is enabled and the first beep beeps.
c. LED control.
Two LED output controls are supported.
1. XSLED and XSQWO. Programmed at offset 0xB5h.

5.2 Advanced Configuration and Power Interface Specification.

A. Top View.
B. Power Management Timer.
C. SCI(SMI) Sources.
D. Suspend Modes.
E. Clock Control.
F. Resume Events.
G. Global Lock.
H. Point for Attention.

A. Top View.
The M1543 supports the ACPI (ver. 1.0) specification, includes the SCI interrupt, 24/32bit Power Management Timer, System Suspend modes, CPU Power saving modes and ACPI I/O Registers.

B. Power Management Timer.
M1543 supports a 24-bit or 32-bit (PG_BD_D2) fixed rate free running count-up Power Management Timer. The ACPI uses the read-only port (IO_08_D, 32bit) to read the current value of the timer. To allow software to extend the number of bits in the timer, the Status bit (IO_00_D0) is set any time the bit-22 or bit-30 of the timer goes from HIGH to LOW. If the Enable bit (IO_02_D0) is set, then the timer generates a system control interrupt (SCI).

C. SCI(SMI) Sources.

Source	Status Reg	Enable Reg	Interrupt
Power Management Timer	IO_00_D0	IO_02_D0	SCI
BIOS Release	IO_00_D5	IO_02_D5	SCI
Power Button	IO_01_D0	IO_03_D0	SCI/SMI
RTC alarm	IO_01_D2	IO_03_D2	SCI/SMI
Thermal Control	IO_18_D0	IO_1A_D0	SCI/SMI
Thermal Override	IO_18_D1	IO_1A_D1	SCI/SMI (THRMJ assert > 2sec)
USB Event	IO_18_D2	IO_1A_D2	SCI/SMI
Docking	IO_19_D0	IO_1B_D0	SCI/SMI
AC Adapter	IO_19_D2	IO_1B_D2	SCI/SMI
Ring	IO_19_D3	IO_1B_D3	SCI/SMI
ACPI Release	IO_1C_D0	IO_1E_D0	SMI

Some sources can be enabled to generate the ACPI interrupt, SCI or an SMI. (SCI_EN, IO_04_D0)

D. Suspend Modes.

The M1543 supports five types of system suspend modes.

1)S0: Working

2)S1: Sleeping(Sleeping with Processor Context Maintained)

- .CPU enters the STOP CLOCK state (using STPCLKJ, CPU_STPJ)
- .SRAM Power Saving Mode (using ZZ, PG_7B_D0)
- .Pentium Pro Sleep Mode (using SLEEPJ, PG_7B_D1, Hardware Setting)
- .Inform M1531 to switch to Suspend Refresh mode (using SUSTAT1J)
- .PAD enters Power Saving Mode
- .Stop Internal PCICLK (PG_CB_D2) Option:
  - .Stop ISP PCICLK (CFG_5E_D5)
  - .Stop ISP DMACLK (CFG_5E_D6)
  - .Stop USB PCICLK (CFG_5E_D7)
  - .Stop 119 KHz clock of M8254 and cold reset counter clock (CFG_5F_D4)
  - .Stop All AT clocks, including SYSCLK and KB CLK (CFG_5F_D5)
  - .Stop Internal Keyboard clock (CFG_5F_D6)
  - .Stop SYSCLK (CFG_5F_D7)

3)S2: Suspend To DRAM (Sleeping with Processor Context Lost)

- .Inform M1531 to switch to Suspend Refresh mode (using SUSTAT1J)
- .All Power Off except Resume Block
- .Stop M1543 XPCICLK (using OFF_PWR1)
- .Stop M1543 XOSC14M (using OFF_PWR1)
- .Run M1543 XCLK32O
- .Run M1543 XCLK32I

4)S3: Suspend To DISK(Non_volatile storage)

- .All Power Off except Resume Block
- .Stop M1543 XPCICLK (using OFF_PWR1)
- .Stop M1543 XOSC14M (using OFF_PWR1)
- .Stop M1543 XCLK32O
- .Run M1543 XCLK32I

5)S4: Soft Off

- .The same as S3

How to enter S1 state:
.Set CLK_EN='1' (IO_11_D1)
.Program the time of Switch Normal to Suspend Refresh
(PG_78_D6-8,0,1,2,4,8,16,32,64 ms)
.Program the stable time of Clock Generator PLL, when system is from S1 to s0
(PG_78_D0-2,0,1,2,4,8,16,32,64 ms)
.Program the stable time of CPU PLL, when system is from S1 to s0
(PG_78_D3-5,0,1,2,4,8,16,32,64 ms)
.Program the time of Switch Suspend to Normal Refresh
(PG_78_D9-11,0,1,2,4,8,16,32,64 ms)
.Set SLP_EN='1', SLP_TYP="011" (IO_05_D5, IO_05_D2-4)
How to enter S2 state:
.Set SLP_EN='1', SLP_TYP="010" (IO_05_D5, IO_05_D2-4)
How to enter S3 state:
.Set SLP_EN='1', SLP_TYP="001" (IO_05_D5, IO_05_D2-4)
How to enter S4 state:
.Set SLP_EN='1', SLP_TYP="000" (IO_05_D5, IO_05_D2-4) or
.Power Button Override Event (PWRBTNJ Assert > 4 sec, PG_B4_D2)

E. Clock Control.
.CPU Clock Control(CLK_EN)
.THROTTLE (THRO_EN=>IO_10_D4, THRO_DTY=>IO_10_D1-3)
.STOP GRANT STATE (Read LVL2,IO_14_D7-0)
.STOP CLOCK STATE (Read LVL3,IO_15_D7-0)

F. Resume Events.

Event	Status Reg	Enable Reg	Resume from
Power Button	IO_01_D0	IO_03_D0	S1/S2/S3/S4
RTC alarm	IO_01_D2	IO_03_D2	S1/S2/S3/S4
USB Event	IO_18_D2	IO_1A_D2	S1
Docking	IO_19_D0	IO_1B_D0	S1/S2/S3/S4
AC Adapter	IO_19_D2	IO_1B_D2	S1/S2/S3/S4
Ring	IO_19_D3	IO_1B_D3	S1/S2/S3/S4
IRQ0 assert	IO_1D_D2	IO_1F_D2	S1
IRQ assert	IO_1D_D3	IO_1F_D3	S1

G. Global Lock.
M1543 supports two sets of Registers :
a. BIOS_RLS(IO_20_D1), GLB_STS(IO_00_D5), GLB_EN(IO_02_D5)
b. GLB_RLS(IO_04_D2), BIOS_STS(IO_1C_D0), BIOS_EN(IO_1E_D0)

In the event of a resource conflict, the Global Lock is used by the ACPI driver to inform the BIOS driver that it is finished u sing a shared resource, or by the BIOS driver to inform the ACPI driver.

H. Point of Attention.
.The ACPI Status Registers only support "write '1'" clear method
.The Legacy Status Registers support "write '1'" clear or "Read Clear" method. (PG_77_D4)
.The ACPI and Legacy Common Status Registers can clear both or one side. (PG_77_D5)
.The ACPI and Legacy SMI method can select ACPI or 7101 mode. (PG_77_D7)
.CFG represents the M1543 Configuration Space Register
.PG represents the PMU Configuration Space Register
.IO represents the ACPI I/O Space Register

5.3 System Management Bus Host Controller Programming Example

Programming Guide for SMBus
* if PMU(M7101) register index 14h-17h set to be 00003A81h
* For SMB Host Controller to be a master only, just set M7101's reg E0h = "01h" & E2h = "20h".
* then below Example's index "03h" will be "00003A80h+03h" that is 'I/O address of SMB Host Controller' = "00003A83h".

Example:
1. A "Write Byte" cycle for Smart Battery Selector (address="14h"), and the write data is 3Ah (DataA="3Ah") with "Command Reg" being "22h".
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "14h"(address="14h" and write cycle).
=> write index 01h "20h"(Write/Read Byte command).
=> write index 04h "3Ah"(DataA is for Byte data use).
=> write index 07h "22h"(Command Reg = "22h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully.
=> else then write '1' clear and restart the protocol.

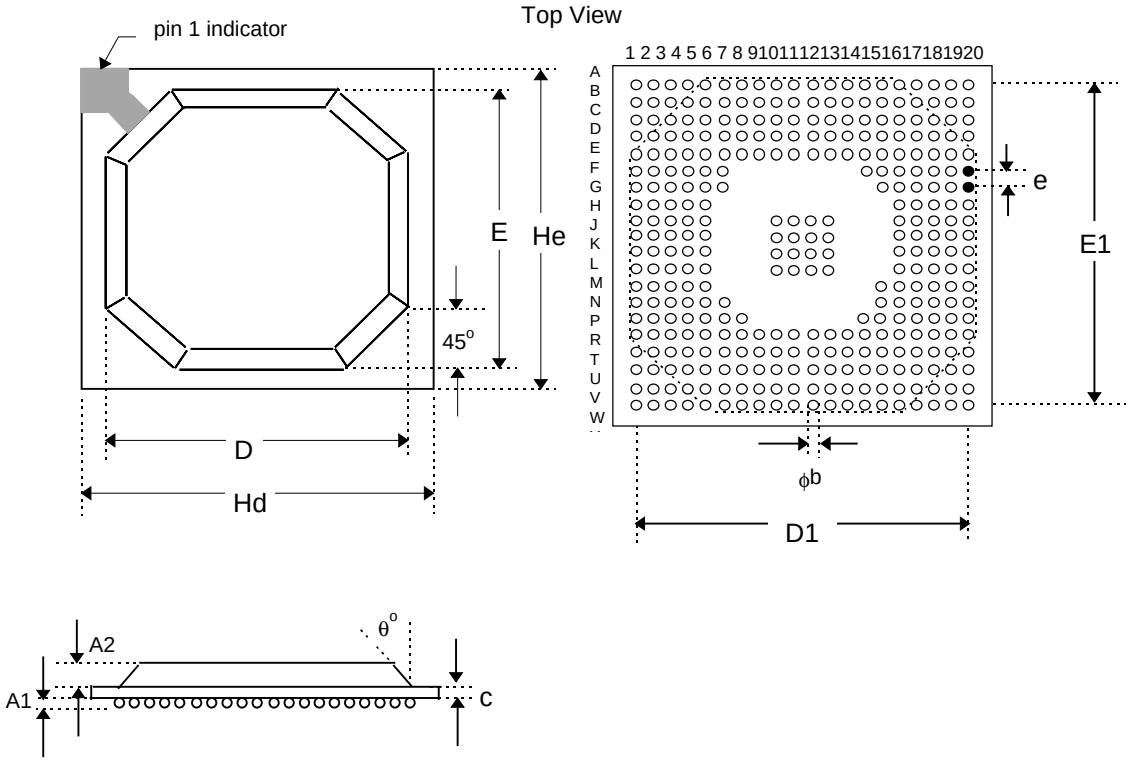
2. A "Write Word" cycle for Smart Battery (address="16h"), and the write data is Low Byte=27h (DataA="27h"), and High Byte=D1h (DataB="D1h") with "Command Reg" being "33h".
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "16h"(address="16h" and write cycle).
=> write index 01h "30h"(Write/Read Word command).
=> write index 04h "27h"(DataA is for Low Byte data use).
=> write index 05h "D1h"(DataB is for High Byte data use).
=> write index 07h "33h"(Command Reg = "33h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully .
=> else then write '1' clear and restart the protocol.

3. A "Read Word" cycle for Thermal (address="90h"-"9Eh"), this procedure is based on the address="92h" with "Command Reg" being "45h".
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "93h"(address="92h" and read cycle).
=> write index 01h "30h"(Write/Read Word command).
=> write index 07h "45h"(Command Reg = "45h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully .
=> else then write '1' clear and reinitial the procedure.
=> if succeed, read index 04h for Low Byte (DataA) , and index 05h for High Byte (DataB).

4. A "Write Block" cycle for Clock Synthesizer (address="D2h"). It has a total of 6 bytes data, for example, to send and the write data is "07h", "2A", "51h", "D0h", "46h" and "38h" with "Command Reg" being "77h" .
=> write '1' clear to let read index 00h to be "04h" (Idle).
=> write index 03h "D2h"(address="D2h" and write cycle).
=> write index 01h "C0h"(Write/Read Block command and reset Block Register Pointer).
=> write index 04h "06h"(DataA is for Block Byte number).
=> write index 06h "07h"(Block Data).
=> write index 06h "2Ah"(Block Data).
=> write index 06h "51h"(Block Data).
=> write index 06h "D0h"(Block Data).
=> write index 06h "46h"(Block Data).
=> write index 06h "38h"(Block Data).
=> write index 07h "77h"(Command Reg = "77h").
=> write index 02h "XXh"(write any data for index 02h to start).
=> wait SMI (or Interrupt).
=> read index 00h, if bit4='1' it means complete successfully .
=> else then write '1' clear and restart the protocol.

Section 6: Packaging Information

328L BGA Dimension Spec (27 x 27 mm)



Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕb	0.60	0.75	0.90
c	0.51	0.56	0.61
D	23.80	24.00	24.20
D1	23.93	24.13	24.33
E	23.80	24.00	24.20
E1	23.93	24.13	24.33
e		1.27	
Hd	26.80	27.00	27.20
He	26.80	27.00	27.20
θ°	23°	30°	37°
Y (radius of ball)			0.25

Section 7: Revision History

p.24	RTS1J
p.40,45,51,75,76,78,84,90,91	04-10-97
p.56,58	04-25-97
p.12,50	05-19-97
p.110	05-27-97
p.46	06-02-97
p.55,56,59	06-06-97
p.71,77,108,117	07-22-97
p.10-12,25,27,28,39,42,45,49,79,84,91,92,98-101,117,119-121,123,192-194,196	08-19-97
p.13-15, 24	08-25-97
p.46	09-11-97

Pinout Diagram (Bottom view)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	SD13	SD14	SD15	XD5	XD2	ROMKBCSJ	RTCDS	USBP1-	GPI3	PHLDJ	AD1	AD6	AD10	AD14	SERRJ	IRDYJ	AD16	AD19	AD20	AD21
B	SD11	DREQ7	SD12	XD6	XD3	XD0	RTCRW	USBP0+	USBCLK	PHLDAJ	AD2	AD7	AD11	AD15	STOPJ	FRAMEJ	AD17	AD22	AD23	CBEJ3
C	DREQ6	SD10	DACKJ7	XD7	XD4	XD1	RTCAS	USBP0-	GPI0	GPO3	AD3	CBEJ0	AD12	CBEJ1	**DEVSELJ**	CBEJ2	AD18	AD24	AD25	AD26
D	SD8	DACKJ6	SD9	SPKR	GPI2	GPO0	GPO12	GPO19	SIRQI	GPO2	AD4	AD8	AD13	PAR	TRDYJ	AD31	AD30	AD27	AD28	AD29
E	DACKJ5	MEMWJ	DREQ5	SPLED	THRMJ	GPO9	GPO18	SIRQII	USBP1+	AD0	AD5	AD9	PCICLK	PCIRSTJ	INTC	INTB	INTA	PIDEA2	PIDECS1	PIDECS3
F	DACKJ0	LA17	DREQ0	MEMRJ	IRQ1I	VCC_E	VCC_A								VCC_B	PIDEIRDYJ	INTD	PIDEDAKJ	PIDEA1	PIDEA0
G	IRQ13	A20MJ	INIT	IRQ14	LA18	VCC3C				**M1543**					VCC_D	PIDED0	PIDED15	PIDEDRQ	PIDEWJ	PIDERJ
H	INTR	NMI	SMIJ	IRQ15	LA19											PIDED12	PIDED2	PIDED13	PIDED1	PIDED14
J	CPURST	IGNNEJ	STPCLK	GPO20	LA20				GND	GND	GND	GND				PIDED5	PIDED10	PIDED4	PIDED11	PIDED3
K	ACPWR	SUSTAT1J	RSMRSTJ	GPO22	GPO1				GND	GND	GND	GND				SIDECS3	PIDED7	PIDED8	PIDED6	**PIDED9**
L	PWRBTNJ	IRQ8J	DOCKJ	GPO23	SMBDATA				GND	GND	GND	GND				SIDEDAKJ	SIDEA1	SIDEA0	SIDEA2	SIDECS1
M	PWG	OSC32KO	RI	LA21	SMBCLK				GND	GND	GND	GND				SIDED15	SIDEDRQ	SIDEWJ	SIDERJ	**SIDEIRDYJ**
N	OSC32I	OSC32II	IRQ10	LA22	IRQ11	VDD_5S										SIDED2	SIDED13	SIDED1	SIDED14	SIDED0
P	OSC14M	M16	SBHEJ	IO16	LA23	VCC_C									VCC_A_D	XDIRJ	SIDED4	SIDED11	SIDED3	SIDED12
R	SA2	SA1	SA0	TC	BALE	VCC_A	VCC_3A							VCC_A_D	VDD_5	XDRV0J	XMOT1J	SIDED9	SIDED5	SIDED10
T	SA5	SA4	SA3	SA6	DACKJ2	DACKJ3	SA19	SD0	MSDATA	MSCLK	RSTDRV	XACKJ	XPD3	XDCD1J	XDENSEL	XMOT0J	XDRV1J	XDSKCHGJ	SIDED8	SIDED6
U	IRQ4	SA7	SA8	IRQ5	IRQ3	SA17	SMEMRJ	SD1	KBDATA	KBCLK	XERRORJ	XBUSY	XPD4	XSTROBJ	XDSR1J	XDCD2J	XINDEXJ	XRDATAJ	XHDSELJ	SIDED7
V	SA9	IRQ6	SA10	DREQ1	SA15	IORJ	AEN	NOWSJ	DREQ2	IRQ9	XINITJ	XPE	XPD5	XPD0	XDTR1J	XRI1J	XDTR2J	XWGATEJ	XTRK0J	XWPROTJ
W	IRQ7	SA11	SYSCLK	SA14	DREQ3	SA18	SMEMWJ	SD2	SD4	SD6	XSLCTINJ	XSLCT	XPD6	XPD1	XSOUT1	XCTS1J	XSOUT2	XRTS2J	XSTEPJ	XWDATAJ
Y	SA12	REFRSHJ	SA13	DACKJ1	SA16	IOWJ	IOCHRDY	SD3	SD5	SD7	IOCK	XAUTOFDJ	XPD7	XPD2	XSIN1	XRTS1J	XSIN2	XDSR2J	XCTS2J	XRI2J

Pinout Diagram (Bottom View) (Chip rotated left - right)

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