M1521: CPU-to-PCI bridge, Memory, Cache and Buffer Controller

Section 1: Introduction

1.1 Features

- Supports all Intel/Cyrix/AMD/TI 586-class processors. Host bus at 66 MHz, 60 MHz and 50MHz at 3.3V.
  - Supports linear wrap mode for M1
- Supports Async/Pipelined-Burst SRAM
  - Direct mapped, 256KB/512KB/1MB
  - Write-Back/Dynamic-Write-Back cache policy
  - Built-in 8K*2 bit SRAM for MESI protocol to reduce cost and enhance performance
  - Cacheable memory up to 64MB with 8-bit Tag SRAM
  - Cacheable memory up to 512MB with 11-bit Tag SRAM
  - 3-1-1-1-1-1-1-1 for Pipelined Burst SRAM at back-to-back burst read and write cycles.
  - Supports 3V/5V SRAMs for Tag Address
- Supports FPM/EDO/BEDO/SDRAM DRAMs
  - 8 RAS Lines
  - 64-bit data path to Memory
  - Symmetrical/Asymmetrical DRAMs
  - 3.3V or 5V DRAMs
  - Duplicated MA[1:0] driving pins for burst access
  - No buffer needed for RASJ and CASJ and MA[1:0]
  - CBR and RAS-only refresh
  - 8 QWORD deep merging buffer for 3-1-1-1-1-1-1-1 posted write cycle
  - 6-3-3-3-3-3-3-3 for back-to-back FPM read-page-hit (@ 66mhz)
    5-2-2-2-2-2-2-2 for back-to-back EDO read-page-hit (@ 66mhz)
    6-1-1-1-1-1-1-1 for back-to-back BEDO read-page-hit (@ 66mhz)
    7-1-1-1-2-1-1-1 for back-to-back SDRAM read-page-hit (@ 66mhz)
    4-2-2-2-2-2-2-2 for back-to-back EDO read-page-hit (@ 60mhz)
    5-1-1-1-1-1-1-1 for back-to-back BEDO read-page-hit (@ 60mhz)
    2-2-2-2 for retired data for posted write on FPM and EDO page-hit
    x-1-1-1 for retired data for posted write on BEDO and SDRAM page-hit
  - Supports 64M-bit (16M*4, 8M*8, 4M*16) technology DRAMs
  - Supports Programmable-strength RAS/CAS/MWE/MA buffers.
  - Supports Error Checking & Correction (ECC) and Parity for DRAM
  - Supports the most flexible six 32-bit populated banks of DRAM (to spare 12MB for Windows 95)
  - Supports SIMM and DIMM
- UMA (Unified Memory Architecture)
  - Dedicated UMA Arbiter Pins
  - Supports several protocols from major graphics vendors.
  - SFB size : 512KB/1MB/2MB/3MB/4MB
  - CPU could access frame buffer memory through system memory controller
  - Alias address for frame buffer memory
- Fully synchronous 25/30/33Mhz 5V PCI interface
  - PCI bus arbiter: five PCI masters and M1523 (ISA Bridge) supported
  - 5 DWORDs for CPU-to-PCI Memory write posted buffers
  - Convert back-to-back CPU to PCI memory write to PCI burst cycle
  - 22 DWORDS for PCI-to-DRAM Write-posted/ Read-prefetching buffers
  - PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write-back)
  - L1/L2 pipelined snoop ahead for PCI-to-DRAM cycle
  - Supports PCI mechanism #1 only
  - PCI spec. 2.1 support. (N(16/8)+8 rule, passive release, fair arbitration)
  - Enhanced performance for Memory-Read-Line and Memory-Read-Multiple and Memory-write-Invalidate PCI commands.
- DRAM refresh during 5V system Suspend
- I/O leakage stopper for power saving during system suspend.
- 328-pin or 388-pin BGA process

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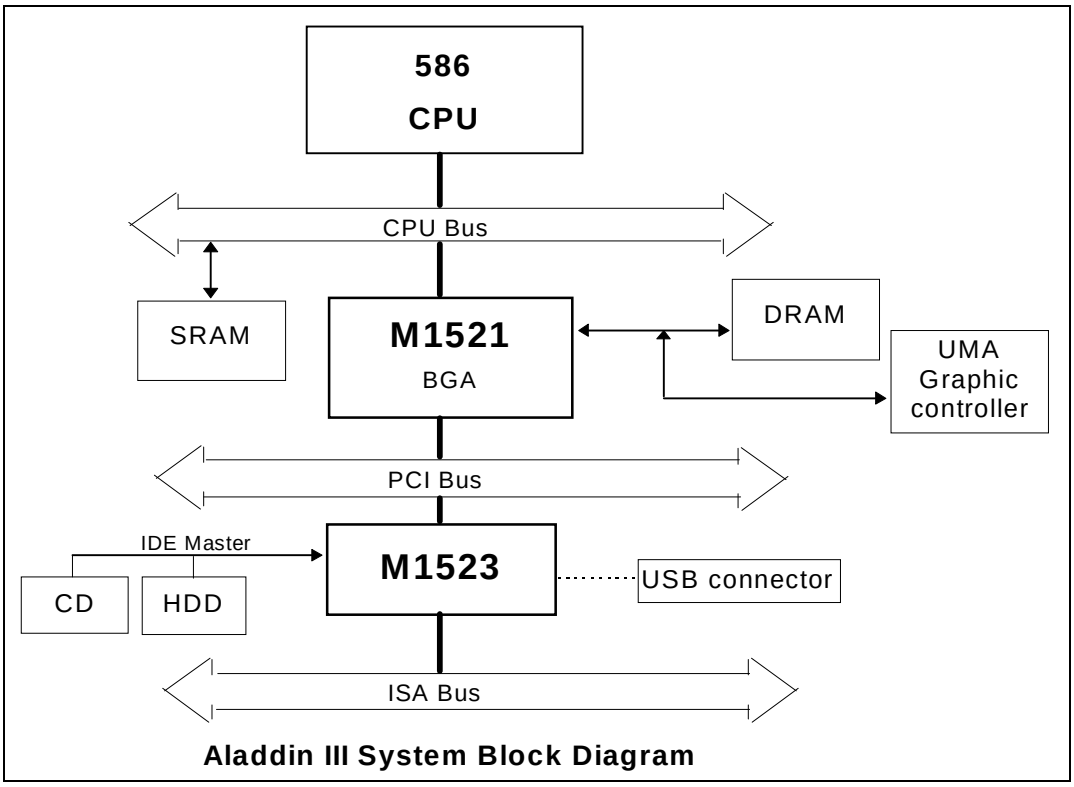
1.2 Introduction

With availability of new PC packaging technology, ALADDIN-III is launched by providing highly efficient bus transaction, highly concurrent architecture and highly integrated design with MESI Tag Memory built-in, USB, UMA, KBC, RTC, and high performance IDE Master with the minimum TTLs needed.

The ALADDIN-III consists of two chips to give the 586 class system a complete solution with most up-to-date feature and architecture for the new multimedia/ multithreading OS.

It utilizes the BGA package to improve the AC characterization, resolves system bottleneck and make the system manufacturing easier.

In the following diagram, ALADDIN-III gives a highly integrated system solution and a most up-to-date architecture, which includes the UMA, ECC, PBSRAM, SDRAM/BEDO, flexible 32/64-bit memory bus and very concurrent multi-bus with highly efficient/ deep FIFO between the buses, such as the HOST/ PCI/ ISA/ dedicated IDE bus.



Aladdin III System Block Diagram

Section 2: Pin Description

2.1 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	HD63	AD31	AD29	AD27	CBE3J	AD21	AD18	CBE2J	AD14	AD11	AD8	AD6	AD3	AD1	AD0	MD62	MD29	MD60	MD27	MD43
B	HD62	AD30	AD28	AD26	AD23	AD20	AD17	CBE1J	AD13	AD10	CBE0J	AD5	AD2	MD31	MD14	MD13	MD61	MD12	MD59	MD58
C	HD59	HD60	HD61	AD25	AD22	AD19	AD16	AD15	AD12	AD9	AD7	AD4	MD15	MD47	MD63	MD45	MD28	MD11	MD10	MD42
D	HD55	HD58	HD57	PHLDJ	PHLDAJ	AD24	REQ0J	GNT0J	REQ1J	GNT1J	REQ2J	GNT2J	REQ3J	GNT3J	MD46	MD30	MD44	MD26	MD57	MD9
E	HD52	HD54	HD56	HD53	LOCKJ	FRAMEJ	IRDYJ	TRDYJ	DEVSELJ	**PCLKIN**	STOPJ	PAR	SERRJ	VDD5V	GND	RAS3J	MD25	MD41	MD24	MD56
F	HD48	HD47	HD51	HD50	VCC	VCC	MGNTJ							VCC	VCC	RAS2J	RAS1J	MD8	MD40	MPD3
G	HD45	HD41	HD49	HD43	HLOCKJ	VCC				**M1521**					PRIO	CAS6J	RAS0J	MPD7	MPD1	MPD5
H	HD39	HD40	HD46	HD44	MIOJ	MREQJ				328-PIN						CAS4J	CAS2J	MPD4	MPD0	MPD6
J	HD37	HD36	HD42	HD38	CACHEJ					GND	GND	GND	GND			CAS5J	CAS0J	MPD2	MD55	MD23
K	HD34	BE0J	BE1J	BE2J	KENJ					GND	GND	GND	GND			HCLKIN	CAS1J	MD39	MD7	MD54
L	BE3J	BE4J	BE5J	BE6J	AHOLD					GND	GND	GND	GND			CAS7J	CAS3J	MD22	MD38	MD6
M	BE7J	HD33	HD32	HD35	BRDYJ					GND	GND	GND	GND			RAS6J	RAS4J	MD53	MD21	MD37
N	HD27	HD30	HD29	HD31	NAJ											RAS7J	RAS5J	MD5	MD52	MD20
P	HD23	HD26	HD25	HD28	BOFFJ	SUSPENDJ									VCC	TIO0	MD19	MD36	MD4	MD51
R	HD7	HD21	HD19	HD24	EADSJ	VCC	VCC								VCC	VCC	MD35	MD18	MD50	MD3
T	HD12	HD22	HD17	HD20	ADSJ	GND	DCJ	HITMJ	WRJ	SMIACTJ	MWEJ	MAA1	MA6	TIO4	RSTJ	GND	MD1	MD49	MD2	MD34
U	HD8	HD18	HD14	HD16	A20	A16	A12	A5	A23	A22	A29	MAB1	MA5	MA8	COEJ	TIO1	TIO2	MD16	MD33	MD17
V	HD6	HD15	HD10	HD13	A19	A14	A9	A8	A21	A26	A3	MAA0	MA4	MA11	CADVJ	TWEJ	TIO3	TIO5	MD32	MD48
W	HD4	HD5	HD9	HD11	A18	A15	A11	A31	A25	A24	A30	MAB0	MA3	MA7	CADSJ	CCSJ	32K	TIO6	TIO8	MD0
Y	HD0	HD2	HD1	HD3	A17	A13	A10	A7	A27	A28	A4	A6	MA2	MA10	MA9	GWEJ	BWEJ	TIO7	TIO9	TIO10

TOP VIEW

2.2 Pin Description Table

Pin Name	Type	Description
Host Interface		
A[31:3]	I/O	**Host Address Bus Lines**. A[31:3] have two functions. As inputs, along with the byte enable signals, these serve as the address lines of the host address bus, which define the physical area of memory or I/O being accessed. As outputs, the M1521 drives them during inquiry cycles on behalf of PCI masters.
BEJ[7:0]	I	**Byte Enables**. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte and BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these are ignored by the M1521.
ADSJ	I	**Address Strobe**. The CPU or M1521 will start a new cycle by asserting ADSJ first. The M1521 will not precede to execute a cycle until it detects ADSJ active.
BRDYJ	O	**Burst Ready**. The assertion of BRDYJ means the current transaction is complete. The CPU will terminate the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.
NAJ	O	**Next Address**. It is asserted by the M1521 to inform the CPU that pipelined cycles are ready for execution.
AHOLD	O	**CPU AHold Request Output**. It serves as the input of CPU's AHOLD pin and actively driven for inquiry cycles.
EADSJ	O	**External Address Strobe**. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1521 will assert this signal to proceed snooping.
BOFFJ	O	**CPU Back-Off**. If BOFFJ is sampled active, CPU will float all its buses in the next clock.
HITMJ	I	**Host Cache Hit after Modified**. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written-back.
MIOJ	I	**Host Memory or I/O**. This bus definition pin indicates the current bus cycle is either memory or input/ output.
DCJ	I	**Host Data or Code**. This bus definition pin is used to distinguish data access cycles from code access cycles.
WRJ	I	**Host Write or Read**. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.
HLOCKJ	I	**Host Lock**. When HLOCKJ is asserted by the CPU, the M1521 will recognize the CPU is locking the current cycles.
CACHEJ	I	**Host Cacheable**. This pin is used to indicate the host's internal cacheability of the read cycles. If it is driven inactive, the CPU will not cache the returned data, regardless of the state of KENJ.
KENJ/INV	O	**Cache Enable Output**. This signal is connected to the CPU's KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1521 drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.
SMIACTJ	I	**SMM Interrupt Active**. It is asserted by the CPU to inform the M1521 that SMM mode is being entered.
HD[63:0]	I/O	**Host Data Bus Lines**. These signals are connected to the CPU's data bus.

Pin Description Table (continued)

Pin Name	Type	Description
DRAM Interface		
MPD[7:0]	I/O	**DRAM Parity /ECC check bits**. These are the 8-bit parities/ECC check bits over DRAM bus.
RASJ[7] / SRASJ[0]	O	**Row Address Strobe 7**, (FPM/EDO/BEDO) of DRAM bank 7. **SDRAM Row address strobe (SDRAM) copy 0**.
RASJ[6] / SCASJ[0]	O	**Row Address Strobe 6**, (FPM/EDO/BEDO) of DRAM bank 6. **SDRAM Column address strobe (SDRAM) copy 0**.
RASJ[5:0] / SCSJ[5:0]	I/O	**Row Address Strobes or synchronous DRAM chip select**. These signals are used to drive the corresponding RASJs of DRAMs or synchronous DRAM chip select[5:0].
CASJ[7:0] / DQM[7:0]	O	**Column Address Strobes or synchronous DRAM Input/Output Data Mask**. These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and a byte mask during a write cycle.
MA[11:2]	O	**DRAM Address lines**. These signals are the address lines of all DRAMs. The M1521 supports DRAM types ranging from 256K to 64Mbits.
MAA[1:0]	O	**Memory Address copy A** for [1:0]
MAB[1:0]	O	**Memory Address copy B** for [1:0]
MWEJ[0]	O	**DRAM Write Enable**. This is the DRAM write enable pin and behaves according to the early-write mechanism; i.e. it activates before the CASJs do. For refresh cycles, it will remain deasserted.
MD[63:0]	I/O	**Memory Data**. These pins are connected to DRAMs.
Secondary Cache Interface		
CADVJ/CA4	O	**Synchronous SRAM advance** or **Asynchronous SRAM address line 4**.
CADSJ/CA3	O	**Synchronous SRAM address strobe cache** or **Asynchronous SRAM address line 3**.
CCSJ/CB4	O	**Synchronous SRAM chip select or Cache Address line 4 copy**. This pin has two modes of operation depending on the type of SRAM selected via hardware strapping options or programming the CC register.
GWEJ	O	**Synchronous SRAM Global Write Enable** or **Asynchronous SRAM write enable**.
COEJ	O	**Synchronous/ Asynchronous SRAM output enable**.
BWEJ/CGCSJ	O	**Synchronous SRAM Byte-Write Enable**/ **Asynchronous SRAM global chip select**.
TIO[10]/ MWEJ[1]	I/O	**SRAM Tag[10]** or **another copy of MWEJ**. Please refer to Register Index-41h bit3 and bit0 description.
TIO[9]/ SRASJ[1]	I/O	**SRAM Tag[9]** or **Synchronous DRAM (SDRAM) RAS copy 1**. Please refer to Register Index-41h bit3 and bit0 description.
TIO[8]/ SCASJ[1]	I/O	**SRAM Tag[8]** or **Synchronous DRAM (SDRAM) CAS copy 1**. Please refer to Register Index-41h bit3 and bit0 description.
TIO[7:0]	I/O	**SRAM Tag[7:0]**. This pin contains the L2 tag address for 256 KB L2 caches. TIO[5:0] contain the L2 tag address and TIO7 contains the L2 cache dirty bit for 512 KB caches and TIO6 contains the L2 cache valid bit for 1MB cache. Please refer to index-41h cache configuration table.
TWEJ	O	**Tag Write Enable**. This signal, when asserted, will write into the external tag new state and tag addresses.

Pin Description Table (continued)

Pin Name	Type	Description
PCI Interface		
AD[31:0]	I/O	**PCI Address-and-Data Bus Lines**. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
CBEJ[3:0]	I/O	**PCI Bus Command and Byte Enables**. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.
FRAMEJ	I/O	**Cycle Frame of PCI Buses**. This indicates the beginning and duration of a PCI access.
DEVSELJ	I/O	**Device Select**. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.
IRDYJ	I/O	**Initiator Ready**. This indicates the initiator is ready to complete the current data phase of transaction.
TRDYJ	I/O	**Target Ready**. This indicates the target is ready to complete the current data phase of transaction.
STOPJ	I/O	**Stop**. This indicates the target is requesting the master to stop the current transaction.
LOCKJ	I/O	**Lock Resource Signal**. This indicates the PCI master or the bridge intends to do exclusive transfers.
REQJ[3:0]	I	**Bus request signals of PCI Masters**. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.
GNTJ[3:0]	O	**Grant signals to PCI Masters**. When asserted by the arbiter, it means the PCI master has been legally granted to own the bus.
PHLDJ	I	**PCI bus hold request**. This active low signal is a request from M1523 for the PCI bus.
PHLDAJ	O	**PCI bus hold acknowledge**. This active low signal grants PCI bus to M1523.
PAR	I/O	**Parity bit of PCI bus**. It is the even parity bit across PAD[31:0] and CBEJ[3:0].
SERRJ	O	**System Error**. If the M1521 detects parity errors in DRAMs, it will assert SERRJ to notify the system.
Clock, Reset, and Suspend		
RSTJ	I	**System Reset**. This pin, when asserted, resets the M1521 and sets the register bits to their default values.
SUSPENDJ	I	**Suspend**. When actively sampled, the M1521 will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.
HCLKIN	I	**CPU bus clock input**. This signal is used by all of the M1521 logic that is in the Host clock domain.
PCLKIN	I	**PCI bus clock input**. This signal is used by all of the M1521 logic that is in the PCI clock domain.
32K	I	The refresh reference clock of frequency 32KHz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.
UMA Interface		
MREQJ/ REQJ[4]	I	**Memory Request**. This input signal is from the GUI device's MREQJ output. This pin can also be used as bus request signal of the fifth PCI master. This function is controlled by Index -72h bit 0.
MGNTJ/ GNTJ[4]	O	**Memory Grant**. This output is connected to the MGNTJ of the GUI device. This pin can also be used as grant signal of the fifth PCI master. This function is controlled by Index -72h bit 0.
PRIO	I	**Priority**. The high priority is requested from the GUI device to do high priority memory access.
Power Pins		
VCC	P	**Vcc 3.3V**
VDD_5	P	**Vcc 5.0V**
Vss or Gnd	P	**Ground**

2.3 Numerical Pin List : (388-pin)

Pin no.	Pin name	Type
A1	Gnd	P
A2	Gnd	P
A3	NC	-
A4	AD29	I/O
A5	AD25	I/O
A6	AD23	I/O
A7	AD21	I/O
A8	FRAMEJ	I/O
A9	AD17	I/O
A10	CBE2J	I/O
A11	TRDYJ	I/O
A12	AD12	I/O
A13	AD10	I/O
A14	STOPJ	I/O
A15	AD8	I/O
A16	GNT2J	O
A17	SERRJ	O
A18	AD3	I/O
A19	AD0	I/O
A20	MD46	I/O
A21	MD14	I/O
A22	MD62	I/O
A23	MD11	I/O
A24	MD27	I/O
A25	NC	-
A26	Gnd	P
B1	MREQJ	I
B2	Gnd	P
B3	AD31	I/O
B4	AD27	I/O
B5	PHLDJ	I
B6	PHLDAJ	O
B7	AD19	I/O
B8	AD18	I/O
B9	REQ0J	I
B10	AD15	I/O
B11	AD13	I/O
B12	DEVSELJ	I/O
B13	GNT1J	O
B14	AD7	I/O
B15	PAR	I/O
B16	AD5	I/O
B17	AD2	I/O
B18	GNT3J	O
B19	MD47	I/O
B20	MD63	I/O
B21	MD13	I/O
B22	MD29	I/O
B23	MD60	I/O
B24	MD43	I/O

Pin no.	Pin name	Type
B25	Gnd	P
B26	Gnd	P
C1	HD62	I/O
C2	HD63	I/O
C3	Gnd	P
C4	MGNTJ	O
C5	AD30	I/O
C6	AD26	I/O
C7	CBE3J	I/O
C8	LOCKJ	I/O
C9	AD24	I/O
C10	AD16	I/O
C11	CBE1J	I/O
C12	AD14	I/O
C13	REQ1J	I
C14	AD11	I/O
C15	PCLKIN	I
C16	CBE0J	I/O
C17	AD4	I/O
C18	REQ3J	I
C19	AD1	I/O
C20	MD31	I/O
C21	MD30	I/O
C22	MD28	I/O
C23	MD12	I/O
C24	Gnd	P
C25	MD59	I/O
C26	PRIO	I
D1	HD61	I/O
D2	HD59	I/O
D3	HD60	I/O
D4	Gnd	P
D5	AD28	I/O
D6	Vcc	P
D7	AD22	I/O
D8	AD20	I/O
D9	Gnd	P
D10	IRDYJ	I/O
D11	Vcc	P
D12	GNT0J	O
D13	AD9	I/O
D14	Gnd	P
D15	REQ2J	I
D16	Vcc	P
D17	AD6	I/O
D18	MD15	I/O
D19	Gnd	P
D20	MD45	I/O
D21	Vcc	P
D22	MD61	I/O

Numerical Pin List (continued)

Pin no.	Pin name	Type
D23	Gnd	P
D24	MD58	I/O
D25	MD57	I/O
D26	MD10	I/O
E1	HD52	I/O
E2	HD55	I/O
E3	HD57	I/O
E4	HD58	I/O
E23	MD9	I/O
E24	MD42	I/O
E25	MD56	I/O
E26	MD44	I/O
F1	HD48	I/O
F2	HD54	I/O
F3	HD53	I/O
F4	Vcc	P
F23	Vcc	P
F24	MD26	I/O
F25	RAS3J	I/O
F26	MD41	I/O
G1	HD51	I/O
G2	HD47	I/O
G3	HD50	I/O
G4	HD56	I/O
G23	MD25	I/O
G24	MD24	I/O
G25	RAS1J	I/O
G26	MD40	I/O
H1	HD49	I/O
H2	HD45	I/O
H3	HD43	I/O
H4	Gnd	P
H23	MD8	I/O
H24	MPD3	I/O
H25	MPD1	I/O
H26	MPD5	I/O
J1	HD39	I/O
J2	HLOCKJ	I
J3	HD46	I/O
J4	HD41	I/O
J23	Gnd	P
J24	RAS2J	I/O
J25	CAS6J	O
J26	MPD7	I/O
K1	HD44	I/O
K2	HD40	I/O
K3	HD36	I/O
K4	MIOJ	I
K23	MPD6	I/O
K24	RAS0J	I/O

Pin no.	Pin name	Type
K25	CAS2J	O
K26	MPD0	I/O
L1	HD42	I/O
L2	HD37	I/O
L3	HD34	I/O
L4	Vcc	P
L11	Gnd	P
L12	Gnd	P
L13	Gnd	P
L14	Gnd	P
L15	Gnd	P
L16	Gnd	P
L23	Vcc	P
L24	MPD4	I/O
L25	MPD2	I/O
L26	MD23	I/O
M1	CACHEJ	I
M2	HD38	I/O
M3	KENJ	O
M4	BE1J	I
M11	Gnd	P
M12	Gnd	P
M13	Gnd	P
M14	Gnd	P
M15	Gnd	P
M16	Gnd	P
M23	CAS4J	O
M24	MD55	I/O
M25	MD54	I/O
M26	CAS0J	O
N1	BE2J	I
N2	BE0J	I
N3	BE4J	I
N4	Gnd	P
N11	Gnd	P
N12	Gnd	P
N13	Gnd	P
N14	Gnd	P
N15	Gnd	P
N16	Gnd	P
N23	CAS1J	O
N24	CAS5J	O
N25	HCLKIN	I
N26	MD39	I/O
P1	BE5J	I
P2	AHOLD	O
P3	BRDYJ	O
P4	BE6J	I
P11	Gnd	P
P12	Gnd	P

Numerical Pin List (continued)

Pin no.	Pin name	Type
P13	Gnd	P
P14	Gnd	P
P15	Gnd	P
P16	Gnd	P
P23	Gnd	P
P24	MD7	I/O
P25	MD38	I/O
P26	CAS3J	O
R1	HD35	I/O
R2	BE3J	I
R3	HD33	I/O
R4	NAJ	O
R11	Gnd	P
R12	Gnd	P
R13	Gnd	P
R14	Gnd	P
R15	Gnd	P
R16	Gnd	P
R23	MD22	I/O
R24	CAS7J	O
R25	RAS4J	I/O
R26	RAS6J	O
T1	BE7J	I
T2	HD32	I/O
T3	HD29	I/O
T4	VDD-5V	P
T11	Gnd	P
T12	Gnd	P
T13	Gnd	P
T14	Gnd	P
T15	Gnd	P
T16	Gnd	P
T23	VDD-5V	P
T24	MD6	I/O
T25	MD37	I/O
T26	MD53	I/O
U1	HD30	I/O
U2	HD31	I/O
U3	HD28	I/O
U4	HD27	I/O
U23	RAS7J	O
U24	MD21	I/O
U25	MD52	I/O
U26	RAS5J	I/O
V1	HD25	I/O
V2	BOFFJ	O
V3	EADSJ	O
V4	Gnd	P
V23	MD4	I/O
V24	MD5	I/O

Pin no.	Pin name	Type
V25	MD48	I/O
V26	MD20	I/O
W1	HD23	I/O
W2	HD26	I/O
W3	HD7	I/O
W4	HD19	I/O
W23	Gnd	P
W24	MD19	I/O
W25	MD51	I/O
W26	MD36	I/O
Y1	HD21	I/O
Y2	HD24	I/O
Y3	HD22	I/O
Y4	HD20	I/O
Y23	MD49	I/O
Y24	MD35	I/O
Y25	MD50	I/O
Y26	MD18	I/O
AA1	HD17	I/O
AA2	ADSJ	I
AA3	HD14	I/O
AA4	Vcc	P
AA23	Vcc	P
AA24	MD1	I/O
AA25	MD2	I/O
AA26	MD3	I/O
AB1	HD16	I/O
AB2	HD12	I/O
AB3	HD6	I/O
AB4	HD8	I/O
AB23	MD33	I/O
AB24	MD16	I/O
AB25	MD17	I/O
AB26	MD34	I/O
AC1	HD15	I/O
AC2	HD18	I/O
AC3	HD4	I/O
AC4	Gnd	P
AC5	HD3	I/O
AC6	Vcc	P
AC7	A18	I/O
AC8	Gnd	P
AC9	A10	I/O
AC10	A5	I/O
AC11	Vcc	P
AC12	A24	I/O
AC13	Gnd	P
AC14	A6	I/O
AC15	MWEJ	O
AC16	Vcc	P

Numerical Pin List (continued)

Pin no.	Pin name	Type
AC17	MA3	O
AC18	Gnd	P
AC19	COEJ	O
AC20	TI01	I/O
AC21	Vcc	P
AC22	BWEJ	O
AC23	Gnd	P
AC24	MD32	I/O
AC25	TIO0	I/O
AC26	MD0	I/O
AD1	NC	-
AD2	HD5	I/O
AD3	Gnd	P
AD4	HD1	I/O
AD5	HD11	I/O
AD6	A19	I/O
AD7	A14	I/O
AD8	A9	I/O
AD9	A31	I/O
AD10	A27	I/O
AD11	WRJ	I
AD12	A22	I/O
AD13	A3	I/O
AD14	A4	I/O
AD15	MAA0	O
AD16	MA5	O
AD17	MA9	O
AD18	MA10	O
AD19	CADSJ	O
AD20	CCSJ	O
AD21	TIO3	I/O
AD22	TIO7	I/O
AD23	TIO9	I/O
AD24	Gnd	P
AD25	TIO10	I/O
AD26	TIO5	I/O
AE1	Gnd	P
AE2	Gnd	P
AE3	SUSPENDJ	I
AE4	HD2	I/O
AE5	HD10	I/O
AE6	A17	I/O
AE7	A13	I/O
AE8	A16	I/O
AE9	A12	I/O
AE10	A7	I/O
AE11	HITMJ	I
AE12	A21	I/O

Pin no.	Pin name	Type
AE13	A28	I/O
AE14	SMIACTJ	I
AE15	A30	I/O
AE16	MAB1	O
AE17	MA6	O
AE18	MA2	O
AE19	MA11	O
AE20	RSTJ	I
AE21	TIO4	I/O
AE22	GWEJ	O
AE23	32K	I
AE24	TIO8	I/O
AE25	Gnd	P
AE26	NC	-
AF1	Gnd	P
AF2	NC	-
AF3	HD0	I/O
AF4	HD9	I/O
AF5	HD13	I/O
AF6	A20	I/O
AF7	A15	I/O
AF8	A11	I/O
AF9	DCJ	I
AF10	A8	I/O
AF11	A25	I/O
AF12	A23	I/O
AF13	A26	I/O
AF14	A29	I/O
AF15	MAA1	O
AF16	MAB0	O
AF17	MA4	O
AF18	MA8	O
AF19	MA7	O
AF20	CADVJ	O
AF21	TWEJ	O
AF22	TIO2	I/O
AF23	TIO6	I/O
AF24	NC	-
AF25	Gnd	P
AF26	Gnd	P

Numerical Pin List (328-pin)

Pin no.	Pin name	Type
A1	HD63	I/O
A2	AD31	I/O
A3	AD29	I/O
A4	AD27	I/O
A5	CBE3J	I/O
A6	AD21	I/O
A7	AD18	I/O
A8	CBE2J	I/O
A9	AD14	I/O
A10	AD11	I/O
A11	AD8	I/O
A12	AD6	I/O
A13	AD3	I/O
A14	AD1	I/O
A15	AD0	I/O
A16	MD62	I/O
A17	MD29	I/O
A18	MD60	I/O
A19	MD27	I/O
A20	MD43	I/O
B1	HD62	I/O
B2	AD30	I/O
B3	AD28	I/O
B4	AD26	I/O
B5	AD23	I/O
B6	AD20	I/O
B7	AD17	I/O
B8	CBE1J	I/O
B9	AD13	I/O
B10	AD10	I/O
B11	CBE0J	I/O
B12	AD5	I/O
B13	AD2	I/O
B14	MD31	I/O
B15	MD14	I/O
B16	MD13	I/O
B17	MD61	I/O
B18	MD12	I/O
B19	MD59	I/O
B20	MD58	I/O
C1	HD59	I/O
C2	HD60	I/O
C3	HD61	I/O
C4	AD25	I/O
C5	AD22	I/O

Pin no.	Pin name	Type
C6	AD19	I/O
C7	AD16	I/O
C8	AD15	I/O
C9	AD12	I/O
C10	AD9	I/O
C11	AD7	I/O
C12	AD4	I/O
C13	MD15	I/O
C14	MD47	I/O
C15	MD63	I/O
C16	MD45	I/O
C17	MD28	I/O
C18	MD11	I/O
C19	MD10	I/O
C20	MD42	I/O
D1	HD55	I/O
D2	HD58	I/O
D3	HD57	I/O
D4	PHLDJ	I
D5	PHLDAJ	O
D6	AD24	I/O
D7	REQ0J	I
D8	GNT0J	O
D9	REQ1J	I
D10	GNT1J	O
D11	REQ2J	I
D12	GNT2J	O
D13	REQ3J	I
D14	GNT3J	O
D15	MD46	I/O
D16	MD30	I/O
D17	MD44	I/O
D18	MD26	I/O
D19	MD57	I/O
D20	MD9	I/O
E1	HD52	I/O
E2	HD54	I/O
E3	HD56	I/O
E4	HD53	I/O
E5	LOCKJ	I/O
E6	FRAMEJ	I/O
E7	IRDYJ	I/O
E8	TRDYJ	I/O
E9	DEVSELJ	I/O
E10	PCLKIN	I

Numerical Pin List (continued)

Pin no.	Pin name	Type
E11	STOPJ	I/O
E12	PAR	I/O
E13	SERRJ	O
E14	VDD-5V	P
E15	Gnd	P
E16	RAS3J	I/O
E17	MD25	I/O
E18	MD41	I/O
E19	MD24	I/O
E20	MD56	I/O
F1	HD48	I/O
F2	HD47	I/O
F3	HD51	I/O
F4	HD50	I/O
F5	VCC	P
F6	VCC	P
F7	MGNTJ	O
F14	VCC	P
F15	VCC	P
F16	RAS2J	I/O
F17	RAS1J	I/O
F18	MD8	I/O
F19	MD40	I/O
F20	MPD3	I/O
G1	HD45	I/O
G2	HD41	I/O
G3	HD49	I/O
G4	HD43	I/O
G5	HLOCKJ	I
G6	VCC	P
G15	PRIO	I
G16	CAS6J	O
G17	RAS0J	I/O
G18	MPD7	I/O
G19	MPD1	I/O
G20	MPD5	I/O
H1	HD39	I/O
H2	HD40	I/O
H3	HD46	I/O
H4	HD44	I/O
H5	M/IOJ	I
H6	MREQJ	I
H16	CAS4J	O
H17	CAS2J	O
H18	MPD4	I/O

Pin no.	Pin name	Type
H19	MPD0	I/O
H20	MPD6	I/O
J1	HD37	I/O
J2	HD36	I/O
J3	HD42	I/O
J4	HD38	I/O
J5	CACHEJ	I
J9	Gnd	P
J10	Gnd	P
J11	Gnd	P
J12	Gnd	P
J16	CAS5J	O
J17	CAS0J	O
J18	MPD2	I/O
J19	MD55	I/O
J20	MD23	I/O
K1	HD34	I/O
K2	BE0J	I/O
K3	BE1J	I/O
K4	BE2J	I/O
K5	KENJ	O
K9	Gnd	P
K10	Gnd	P
K11	Gnd	P
K12	Gnd	P
K16	HCLKIN	I
K17	CAS1J	O
K18	MD39	I/O
K19	MD7	I/O
K20	MD54	I/O
L1	BE3J	I
L2	BE4J	I
L3	BE5J	I
L4	BE6J	I
L5	AHOLD	O
L9	Gnd	P
L10	Gnd	P
L11	Gnd	P
L12	Gnd	P
L16	CAS7J	O
L17	CAS3J	O
L18	MD22	I/O
L19	MD38	I/O
L20	MD6	I/O
M1	BE7J	I

Numerical Pin List (continued)

Pin no.	Pin name	Type
M2	HD33	I/O
M3	HD32	I/O
M4	HD35	I/O
M5	BRDYJ	O
M9	Gnd	P
M10	Gnd	P
M11	Gnd	P
M12	Gnd	P
M16	RAS6J	O
M17	RAS4J	I/O
M18	MD53	I/O
M19	MD21	I/O
M20	MD37	I/O
N1	HD27	I/O
N2	HD30	I/O
N3	HD29	I/O
N4	HD31	I/O
N5	NAJ	O
N16	RAS7J	O
N17	RAS5J	I/O
N18	MD5	I/O
N19	MD52	I/O
N20	MD20	I/O
P1	HD23	I/O
P2	HD26	I/O
P3	HD25	I/O
P4	HD28	I/O
P5	BOFFJ	O
P6	SUSPENDJ	I
P15	VCC	P
P16	TIO0	I/O
P17	MD19	I/O
P18	MD36	I/O
P19	MD4	I/O
P20	MD51	I/O
R1	HD7	I/O
R2	HD21	I/O
R3	HD19	I/O
R4	HD24	I/O
R5	EADSJ	O
R6	VCC	P
R7	VCC	P
R15	VCC	P
R16	VCC	P

Pin no.	Pin name	Type
R17	MD35	I/O
R18	MD18	I/O
R19	MD50	I/O
R20	MD3	I/O
T1	HD12	I/O
T2	HD22	I/O
T3	HD17	I/O
T4	HD20	I/O
T5	ADSJ	I
T6	Gnd	P
T7	D/CJ	I
T8	HITMJ	I
T9	W/RJ	I
T10	SMIACTJ	I
T11	MWEJ	O
T12	MAA1	O
T13	MA6	O
T14	TIO4	I/O
T15	RSTJ	I
T16	Gnd	P
T17	MD1	I/O
T18	MD49	I/O
T19	MD2	I/O
T20	MD34	I/O
U1	HD8	I/O
U2	HD18	I/O
U3	HD14	I/O
U4	HD16	I/O
U5	A20	I/O
U6	A16	I/O
U7	A12	I/O
U8	A5	I/O
U9	A23	I/O
U10	A22	I/O
U11	A29	I/O
U12	MAB1	O
U13	MA5	O
U14	MA8	O
U15	COEJ	O
U16	TIO1	I/O
U17	TIO2	I/O
U18	MD16	I/O
U19	MD33	I/O
U20	MD17	I/O

Numerical Pin List (continued)

Pin no.	Pin name	Type
V1	HD6	I/O
V2	HD15	I/O
V3	HD10	I/O
V4	HD13	I/O
V5	A19	I/O
V6	A14	I/O
V7	A9	I/O
V8	A8	I/O
V9	A21	I/O
V10	A26	I/O
V11	A3	I/O
V12	MAA0	O
V13	MA4	O
V14	MA11	O
V15	CADVJ	O
V16	TWEJ	O
V17	TIO3	I/O
V18	TIO5	I/O
V19	MD32	I/O
V20	MD48	I/O
W1	HD4	I/O
W2	HD5	I/O
W3	HD9	I/O
W4	HD11	I/O
W5	A18	I/O
W6	A15	I/O
W7	A11	I/O
W8	A31	I/O
W9	A25	I/O
W10	A24	I/O
W11	A30	I/O
W12	MAB0	O
W13	MA3	O
W14	MA7	O
W15	CADSJ	O
W16	CCSJ	O
W17	32K	I
W18	TIO6	I/O
W19	TIO8	I/O
W20	MD0	I/O
Y1	HD0	I/O
Y2	HD2	I/O
Y3	HD1	I/O
Y4	HD3	I/O
Y5	A17	I/O
Y6	A13	I/O
Y7	A10	I/O
Y8	A7	I/O
Y9	A27	I/O
Y10	A28	I/O
Y11	A4	I/O
Y12	A6	I/O
Y13	MA2	O
Y14	MA10	O
Y15	MA9	O
Y16	GWEJ	O
Y17	BWEJ	O
Y18	TIO7	I/O
Y19	TIO9	I/O
Y20	TIO10	I/O

2.4 Alphabetical Pin List : (388-pin)

Pin no.	Pin name	Type
AE23	32K	I
AD13	A3	I/O
AD14	A4	I/O
AC10	A5	I/O
AC14	A6	I/O
AE10	A7	I/O
AF10	A8	I/O
AD8	A9	I/O
AC9	A10	I/O
AF8	A11	I/O
AE9	A12	I/O
AE7	A13	I/O
AD7	A14	I/O
AF7	A15	I/O
AE8	A16	I/O
AE6	A17	I/O
AC7	A18	I/O
AD6	A19	I/O
AF6	A20	I/O
AE12	A21	I/O
AD12	A22	I/O
AF12	A23	I/O
AC12	A24	I/O
AF11	A25	I/O
AF13	A26	I/O
AD10	A27	I/O
AE13	A28	I/O
AF14	A29	I/O
AE15	A30	I/O
AD9	A31	I/O
A19	AD0	I/O
C19	AD1	I/O
B17	AD2	I/O
A18	AD3	I/O
C17	AD4	I/O
B16	AD5	I/O
D17	AD6	I/O
B14	AD7	I/O
A15	AD8	I/O
D13	AD9	I/O
A13	AD10	I/O
C14	AD11	I/O
A12	AD12	I/O
B11	AD13	I/O
C12	AD14	I/O
B10	AD15	I/O
C10	AD16	I/O
A9	AD17	I/O
B8	AD18	I/O
B7	AD19	I/O

Pin no.	Pin name	Type
D8	AD20	I/O
A7	AD21	I/O
D7	AD22	I/O
A6	AD23	I/O
C9	AD24	I/O
A5	AD25	I/O
C6	AD26	I/O
B4	AD27	I/O
D5	AD28	I/O
A4	AD29	I/O
C5	AD30	I/O
B3	AD31	I/O
AA2	ADSJ	I
P2	AHOLD	O
N2	BE0J	I
M4	BE1J	I
N1	BE2J	I
R2	BE3J	I
N3	BE4J	I
P1	BE5J	I
P4	BE6J	I
T1	BE7J	I
V2	BOFFJ	O
P3	BRDYJ	O
AC22	BWEJ	O
M1	CACHEJ	I
AD19	CADSJ	O
AF20	CADVJ	O
M26	CAS0J	O
N23	CAS1J	O
K25	CAS2J	O
P26	CAS3J	O
M23	CAS4J	O
N24	CAS5J	O
J25	CAS6J	O
R24	CAS7J	O
C16	CBE0J	I/O
C11	CBE1J	I/O
A10	CBE2J	I/O
C7	CBE3J	I/O
AD20	CCSJ	O
AC19	COEJ	O
AF9	DCJ	I
B12	DEVSELJ	I/O
V3	EADSJ	O
A8	FRAMEJ	I/O
B13	GNT1J	O
A16	GNT2J	O
B18	GNT3J	O
A1	Gnd	P

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
A2	Gnd	P
A26	Gnd	P
B2	Gnd	P
B25	Gnd	P
B26	Gnd	P
C3	Gnd	P
C24	Gnd	P
D4	Gnd	P
J23	Gnd	P
D9	Gnd	P
D14	Gnd	P
D19	Gnd	P
D23	Gnd	P
H4	Gnd	P
L11	Gnd	P
L12	Gnd	P
L13	Gnd	P
L14	Gnd	P
L15	Gnd	P
L16	Gnd	P
M11	Gnd	P
M12	Gnd	P
M13	Gnd	P
M14	Gnd	P
M15	Gnd	P
M16	Gnd	P
N4	Gnd	P
N11	Gnd	P
N12	Gnd	P
N13	Gnd	P
N14	Gnd	P
N15	Gnd	P
N16	Gnd	P
P11	Gnd	P
P12	Gnd	P
P13	Gnd	P
P14	Gnd	P
P15	Gnd	P
P16	Gnd	P
P23	Gnd	P
R11	Gnd	P
R12	Gnd	P
R13	Gnd	P
R14	Gnd	P
R15	Gnd	P
R16	Gnd	P
T11	Gnd	P
T12	Gnd	P
T13	Gnd	P
T14	Gnd	P

Pin no.	Pin name	Type
T15	Gnd	P
T16	Gnd	P
V4	Gnd	P
W23	Gnd	P
AC4	Gnd	P
AC8	Gnd	P
AC13	Gnd	P
AC18	Gnd	P
AC23	Gnd	P
AD3	Gnd	P
AD24	Gnd	P
AE1	Gnd	P
AE2	Gnd	P
AE25	Gnd	P
AF1	Gnd	P
AF25	Gnd	P
AF26	Gnd	P
D12	GNT0J	O
AE22	GWEJ	O
N25	HCLKIN	I
AF3	HD0	I/O
AD4	HD1	I/O
AE4	HD2	I/O
AC5	HD3	I/O
AC3	HD4	I/O
AD2	HD5	I/O
AB3	HD6	I/O
W3	HD7	I/O
AB4	HD8	I/O
AF4	HD9	I/O
AE5	HD10	I/O
AD5	HD11	I/O
AB2	HD12	I/O
AF5	HD13	I/O
AA3	HD14	I/O
AC1	HD15	I/O
AB1	HD16	I/O
AA1	HD17	I/O
AC2	HD18	I/O
W4	HD19	I/O
Y4	HD20	I/O
Y1	HD21	I/O
Y3	HD22	I/O
W1	HD23	I/O
Y2	HD24	I/O
V1	HD25	I/O
W2	HD26	I/O
U4	HD27	I/O
U3	HD28	I/O
T3	HD29	I/O

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
U1	HD30	I/O
U2	HD31	I/O
T2	HD32	I/O
R3	HD33	I/O
L3	HD34	I/O
R1	HD35	I/O
K3	HD36	I/O
L2	HD37	I/O
M2	HD38	I/O
J1	HD39	I/O
K2	HD40	I/O
J4	HD41	I/O
L1	HD42	I/O
H3	HD43	I/O
K1	HD44	I/O
H2	HD45	I/O
J3	HD46	I/O
G2	HD47	I/O
F1	HD48	I/O
H1	HD49	I/O
G3	HD50	I/O
G1	HD51	I/O
E1	HD52	I/O
F3	HD53	I/O
F2	HD54	I/O
E2	HD55	I/O
G4	HD56	I/O
E3	HD57	I/O
E4	HD58	I/O
D2	HD59	I/O
D3	HD60	I/O
D1	HD61	I/O
C1	HD62	I/O
C2	HD63	I/O
B6	HLDAJ	O
J2	HLOCKJ	I
AE11	HITMJ	I
D10	IRDYJ	I/O
M3	KENJ	O
C8	LOCKJ	I/O
AE18	MA2	O
AC17	MA3	O
AF17	MA4	O
AD16	MA5	O
AE17	MA6	O
AF19	MA7	O
AF18	MA8	O
AD17	MA9	O
AD18	MA10	O
AE19	MA11	O

Pin no.	Pin name	Type
AD15	MAA0	O
AF15	MAA1	O
AF16	MAB0	O
AE16	MAB1	O
AC26	MD0	I/O
AA24	MD1	I/O
AA25	MD2	I/O
AA26	MD3	I/O
V23	MD4	I/O
V24	MD5	I/O
T24	MD6	I/O
P24	MD7	I/O
H23	MD8	I/O
E23	MD9	I/O
D26	MD10	I/O
A23	MD11	I/O
C23	MD12	I/O
B21	MD13	I/O
A21	MD14	I/O
D18	MD15	I/O
AB24	MD16	I/O
AB25	MD17	I/O
Y26	MD18	I/O
W24	MD19	I/O
V26	MD20	I/O
U24	MD21	I/O
R23	MD22	I/O
L26	MD23	I/O
G24	MD24	I/O
G23	MD25	I/O
F24	MD26	I/O
A24	MD27	I/O
C22	MD28	I/O
B22	MD29	I/O
C21	MD30	I/O
C20	MD31	I/O
AC24	MD32	I/O
AB23	MD33	I/O
AB26	MD34	I/O
Y24	MD35	I/O
W26	MD36	I/O
T25	MD37	I/O
P25	MD38	I/O
N26	MD39	I/O
G26	MD40	I/O
F26	MD41	I/O
E24	MD42	I/O
B24	MD43	I/O
E26	MD44	I/O
D20	MD45	I/O

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
A20	MD46	I/O
B19	MD47	I/O
V25	MD48	I/O
Y23	MD49	I/O
Y25	MD50	I/O
W25	MD51	I/O
U25	MD52	I/O
T26	MD53	I/O
M25	MD54	I/O
M24	MD55	I/O
E25	MD56	I/O
D25	MD57	I/O
D24	MD58	I/O
C25	MD59	I/O
B23	MD60	I/O
D22	MD61	I/O
A22	MD62	I/O
B20	MD63	I/O
C4	MGNTJ	O
K4	MIOJ	I
K26	MPD0	I/O
H25	MPD1	I/O
L25	MPD2	I/O
H24	MPD3	I/O
L24	MPD4	I/O
H26	MPD5	I/O
K23	MPD6	I/O
J26	MPD7	I/O
B1	MREQJ	I
AC15	MWEJ	O
R4	NAJ	O
AD1	NC	-
A25	NC	-
A3	NC	-
AE26	NC	-
AF2	NC	-
AF24	NC	-
B15	PAR	I/O
C15	PCLKIN	I
B5	PHLDJ	O
C26	PRIO	I
K24	RAS0J	I/O
G25	RAS1J	I/O
J24	RAS2J	I/O
F25	RAS3J	I/O
R25	RAS4J	I/O
U26	RAS5J	I/O
R26	RAS6J	O
U23	RAS7J	O
B9	REQ0J	I

Pin no.	Pin name	Type
C13	REQ1J	I
D15	REQ2J	I
C18	REQ3J	I
AE20	RSTJ	I
A17	SERRJ	O
AE14	SMIACTJ	I
A14	STOPJ	I/O
AE3	SUSPENDJ	I
AC25	TIO0	I/O
AC20	TIO1	I/O
AF22	TIO2	I/O
AD21	TIO3	I/O
AE21	TIO4	I/O
AD26	TIO5	I/O
AF23	TIO6	I/O
AD22	TIO7	I/O
AE24	TIO8	I/O
AD23	TIO9	I/O
AD25	TIO10	I/O
A11	TRDYJ	I/O
AF21	TWEJ	O
D6	Vcc	P
D11	Vcc	P
D16	Vcc	P
D21	Vcc	P
F4	Vcc	P
F23	Vcc	P
L4	Vcc	P
L23	Vcc	P
AA23	Vcc	P
AA4	Vcc	P
AC11	Vcc	P
AC6	Vcc	P
AC16	Vcc	P
AC21	Vcc	P
T4	V_{DD}-5	P
T23	V_{DD}-5	P
AD11	WRJ	I

Alphabetical Pin List (328-pin)

Pin no.	Pin name	Type
W17	32K	I
V11	A3	I/O
Y11	A4	I/O
U8	A5	I/O
Y12	A6	I/O
Y8	A7	I/O
V8	A8	I/O
V7	A9	I/O
Y7	A10	I/O
W7	A11	I/O
U7	A12	I/O
Y6	A13	I/O
V6	A14	I/O
W6	A15	I/O
U6	A16	I/O
Y5	A17	I/O
W5	A18	I/O
V5	A19	I/O
U5	A20	I/O
V9	A21	I/O
U10	A22	I/O
U9	A23	I/O
W10	A24	I/O
W9	A25	I/O
V10	A26	I/O
Y9	A27	I/O
Y10	A28	I/O
U11	A29	I/O
W11	A30	I/O
W8	A31	I/O
A15	AD0	I/O
A14	AD1	I/O
B13	AD2	I/O
A13	AD3	I/O
C12	AD4	I/O
B12	AD5	I/O
A12	AD6	I/O
C11	AD7	I/O
A11	AD8	I/O
C10	AD9	I/O
B10	AD10	I/O
A10	AD11	I/O
C9	AD12	I/O
B9	AD13	I/O
A9	AD14	I/O
C8	AD15	I/O
C7	AD16	I/O
B7	AD17	I/O
A7	AD18	I/O
C6	AD19	I/O

Pin no.	Pin name	Type
B6	AD20	I/O
A6	AD21	I/O
C5	AD22	I/O
B5	AD23	I/O
D6	AD24	I/O
C4	AD25	I/O
B4	AD26	I/O
A4	AD27	I/O
B3	AD28	I/O
A3	AD29	I/O
B2	AD30	I/O
A2	AD31	I/O
T5	ADSJ	I
L5	AHOLD	O
K2	BE0J	I
K3	BE1J	I
K4	BE2J	I
L1	BE3J	I
L2	BE4J	I
L3	BE5J	I
L4	BE6J	I
M1	BE7J	I
P5	BOFFJ	O
M5	BRDYJ	O
Y17	BWEJ	O
J5	CACHEJ	I
W15	CADSJ	O
V15	CADVJ	O
J17	CAS0J	O
K17	CAS1J	O
H17	CAS2J	O
L17	CAS3J	O
H16	CAS4J	O
J16	CAS5J	O
G16	CAS6J	O
L16	CAS7J	O
B11	CBE0J	I/O
B8	CBE1J	I/O
A8	CBE2J	I/O
A5	CBE3J	I/O
W16	CCSJ	O
U15	COEJ	O
T7	D/CJ	I
E9	DEVSELJ	I/O
R5	EADSJ	O
E6	FRAMEJ	I/O
D8	GNT0J	O
D10	GNT1J	O
D12	GNT2J	O
D14	GNT3J	O

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
E15	Gnd	P
J9	Gnd	P
J10	Gnd	P
J11	Gnd	P
J12	Gnd	P
K9	Gnd	P
K10	Gnd	P
K11	Gnd	P
K12	Gnd	P
L9	Gnd	P
L10	Gnd	P
L11	Gnd	P
L12	Gnd	P
M9	Gnd	P
M10	Gnd	P
M11	Gnd	P
M12	Gnd	P
T6	Gnd	P
T16	Gnd	P
Y16	GWEJ	O
K16	HCLKIN	I
Y1	HD0	I/O
Y3	HD1	I/O
Y2	HD2	I/O
Y4	HD3	I/O
W1	HD4	I/O
W2	HD5	I/O
V1	HD6	I/O
R1	HD7	I/O
U1	HD8	I/O
W3	HD9	I/O
V3	HD10	I/O
W4	HD11	I/O
T1	HD12	I/O
V4	HD13	I/O
U3	HD14	I/O
V2	HD15	I/O
U4	HD16	I/O
T3	HD17	I/O
U2	HD18	I/O
R3	HD19	I/O
T4	HD20	I/O
R2	HD21	I/O
T2	HD22	I/O
P1	HD23	I/O
R4	HD24	I/O
P3	HD25	I/O
P2	HD26	I/O
N1	HD27	I/O
P4	HD28	I/O

Pin no.	Pin name	Type
N3	HD29	I/O
N2	HD30	I/O
N4	HD31	I/O
M3	HD32	I/O
M2	HD33	I/O
K1	HD34	I/O
M4	HD35	I/O
J2	HD36	I/O
J1	HD37	I/O
J4	HD38	I/O
H1	HD39	I/O
H2	HD40	I/O
G2	HD41	I/O
J3	HD42	I/O
G4	HD43	I/O
H4	HD44	I/O
G1	HD45	I/O
H3	HD46	I/O
F2	HD47	I/O
F1	HD48	I/O
G3	HD49	I/O
F4	HD50	I/O
F3	HD51	I/O
E1	HD52	I/O
E4	HD53	I/O
E2	HD54	I/O
D1	HD55	I/O
E3	HD56	I/O
D3	HD57	I/O
D2	HD58	I/O
C1	HD59	I/O
C2	HD60	I/O
C3	HD61	I/O
B1	HD62	I/O
A1	HD63	I/O
T8	HITMJ	I
G5	HLOCKJ	I
E7	IRDYJ	I/O
K5	KENJ	O
E5	LOCKJ	I/O
Y13	MA2	O
W13	MA3	O
V13	MA4	O
U13	MA5	O
T13	MA6	O
W14	MA7	O
U14	MA8	O
Y15	MA9	O
Y14	MA10	O
V14	MA11	O

Alphabetical Pin List (continued)

Pin no.	Pin name	Type
V12	MAA0	O
T12	MAA1	O
W12	MAB0	O
U12	MAB1	O
W20	MD0	I/O
T17	MD1	I/O
T19	MD2	I/O
R20	MD3	I/O
P19	MD4	I/O
N18	MD5	I/O
L20	MD6	I/O
K19	MD7	I/O
F18	MD8	I/O
D20	MD9	I/O
C19	MD10	I/O
C18	MD11	I/O
B18	MD12	I/O
B16	MD13	I/O
B15	MD14	I/O
C13	MD15	I/O
U18	MD16	I/O
U20	MD17	I/O
R18	MD18	I/O
P17	MD19	I/O
N20	MD20	I/O
M19	MD21	I/O
L18	MD22	I/O
J20	MD23	I/O
E19	MD24	I/O
E17	MD25	I/O
D18	MD26	I/O
A19	MD27	I/O
C17	MD28	I/O
A17	MD29	I/O
D16	MD30	I/O
B14	MD31	I/O
V19	MD32	I/O
U19	MD33	I/O
T20	MD34	I/O
R17	MD35	I/O
P18	MD36	I/O
M20	MD37	I/O
L19	MD38	I/O
K18	MD39	I/O
F19	MD40	I/O
E18	MD41	I/O
C20	MD42	I/O
A20	MD43	I/O
D17	MD44	I/O
C16	MD45	I/O

Pin no.	Pin name	Type
D15	MD46	I/O
C14	MD47	I/O
V20	MD48	I/O
T18	MD49	I/O
R19	MD50	I/O
P20	MD51	I/O
N19	MD52	I/O
M18	MD53	I/O
K20	MD54	I/O
J19	MD55	I/O
E20	MD56	I/O
D19	MD57	I/O
B20	MD58	I/O
B19	MD59	I/O
A18	MD60	I/O
B17	MD61	I/O
A16	MD62	I/O
C15	MD63	I/O
F7	MGNTJ	O
H19	MPD0	I/O
G19	MPD1	I/O
J18	MPD2	I/O
F20	MPD3	I/O
H18	MPD4	I/O
G20	MPD5	I/O
H20	MPD6	I/O
G18	MPD7	I/O
H5	M/IOJ	I
H6	MREQJ	I
T11	MWEJ	O
N5	NAJ	O
E12	PAR	I/O
E10	PCLKIN	I
D4	PHLDJ	I
D5	PHLDAJ	O
G15	PRIO	I
G17	RAS0J	I/O
F17	RAS1J	I/O
F16	RAS2J	I/O
E16	RAS3J	I/O
M17	RAS4J	I/O
N17	RAS5J	I/O
M16	RAS6J	O
N16	RAS7J	O
D7	REQ0J	I
D9	REQ1J	I
D11	REQ2J	I
D13	REQ3J	I
T15	RSTJ	I
E13	SERRJ	O

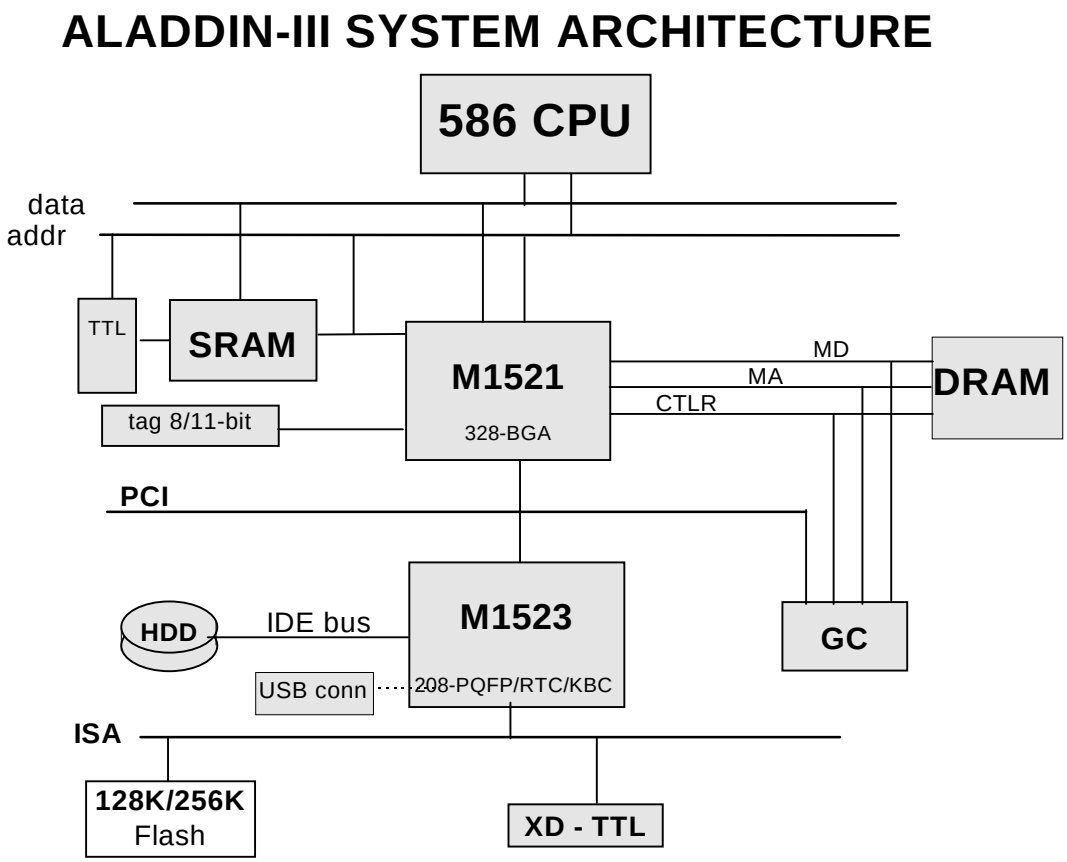
Alphabetical Pin List (continued)

Pin no.	Pin name	Type
T10	SMIACTJ	I
E11	STOPJ	I/O
P6	SUSPENDJ	I
P16	TIO0	I/O
U16	TIO1	I/O
U17	TIO2	I/O
V17	TIO3	I/O
T14	TIO4	I/O
V18	TIO5	I/O
W18	TIO6	I/O
Y18	TIO7	I/O
W19	TIO8	I/O
Y19	TIO9	I/O
Y20	TIO10	I/O
E8	TRDYJ	I/O
V16	TWEJ	O
F5	VCC	P
F6	VCC	P
F14	VCC	P
F15	VCC	P
G6	VCC	P
P15	VCC	P
R6	VCC	P
R7	VCC	P
R15	VCC	P
R16	VCC	P
E14	VDD5V	P
T9	W/RJ	I

Section 3: Function Description

3.1 System Architecture

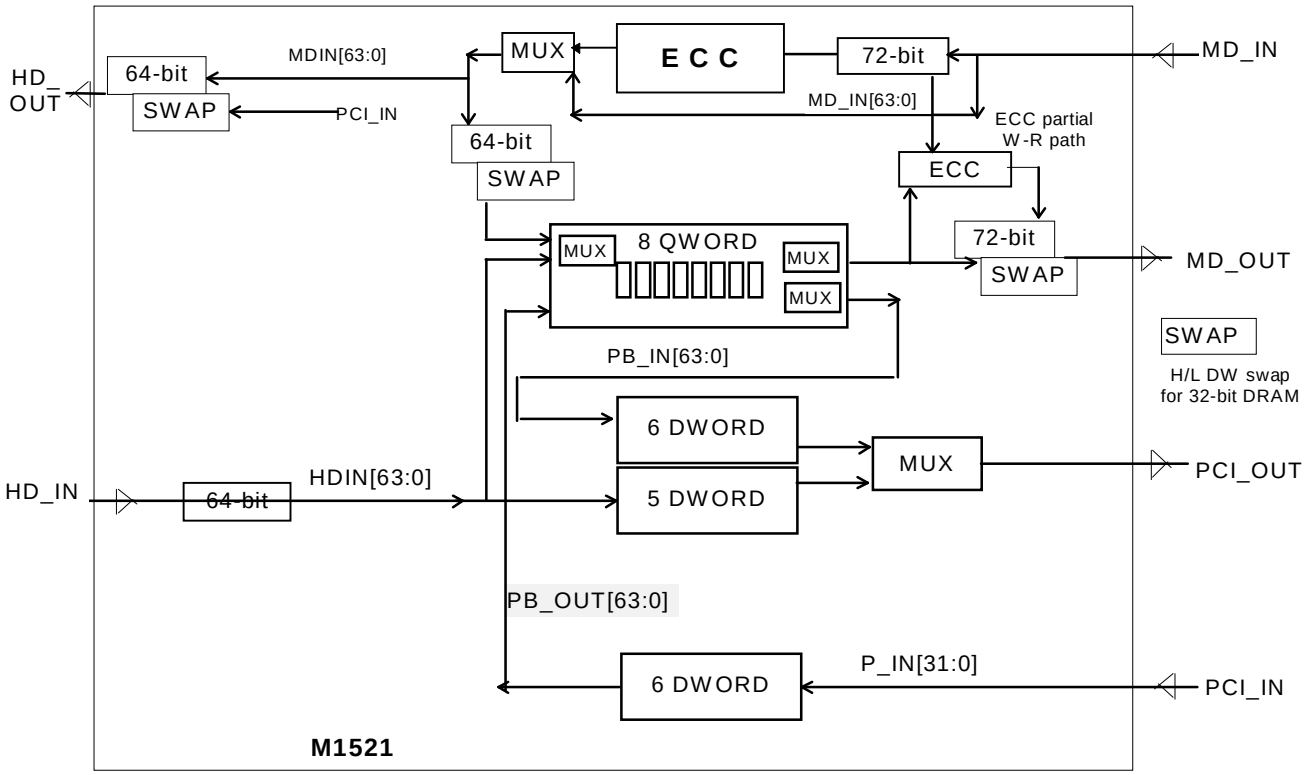
In the following diagram, ALADDIN-III gives a highly integrated system solution and a most up-to-date system architecture, which includes the UMA, ECC, PBSRAM, SDRAM/BEDO and very concurrent multi-bus with highly efficient/ deep FIFO between the buses, such as the HOST/ PCI/ ISA/ DEDICATED IDE bus.



The M1521 provides a complete integrated solution for the system controller and data path components in a Pentium processor system. It provides 64-bit CPU bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including Pipelined Burst SRAM or Asynchronous SRAM, PCI master to DRAM interface, 4 PCI master arbiters, and a UMA arbiter. The following figure shows the highly efficient data path in the M1521. The M1521 bus interfaces are designed to interface with 3V and 5V buses. It directly connects to 3V CPU bus, 3V or 5V Tag, 3V or 5V DRAM bus, and 5V PCI bus.

The M1523 provides a highly integrated PCI to ISA bridge solution. It comprises a fast dedicated IDE master interface, Plug-and-Play port, APIC interface, PS/2 keyboard and mouse, RTC, reserved Universal Serial Bus feature, and PCI 2.1 Compliance operation.

Data Path of M1521



3.2 Cache Memory Timing/Configuration

The M1521 integrates a high performance L2 writeback/direct mapping cache controller using MESI protocol of L1 and L2, and has an L2 MESI tag built-in to maintain the data coherence for optimizing CPU bus utilization. The L2 cache can be configured for asynchronous SRAM or Pipelined Burst SRAM with cache size from 256KB, 512KB to 1MB. The cacheable region can be up to 512MB under 256KB cache memory configuration, by using 11-bit tag option. Or, by using an 8Kx8 tag RAM, the cacheable region of the system is 64MB. The controller can perform a dynamic-write-back cycle to DRAM, which the L1 write cycle will be directed to DRAM intelligently with 3-1-1-1 timing without stalling the CPU execution.

The timing of cache memory system is shown in following table:

	READ	WRITE	B2B READ	B2B WRITE
PBSRAM	3-1-1-1	3-1-1-1	3-1-1-1-1-1-1-1	3-1-1-1-1-1-1-1
ASRAM	3-2-2-2	4-2-2-2	-----	-----
		4-3-3-3		

The following L2 CACHE Table shows the different configurations supported by M1521.

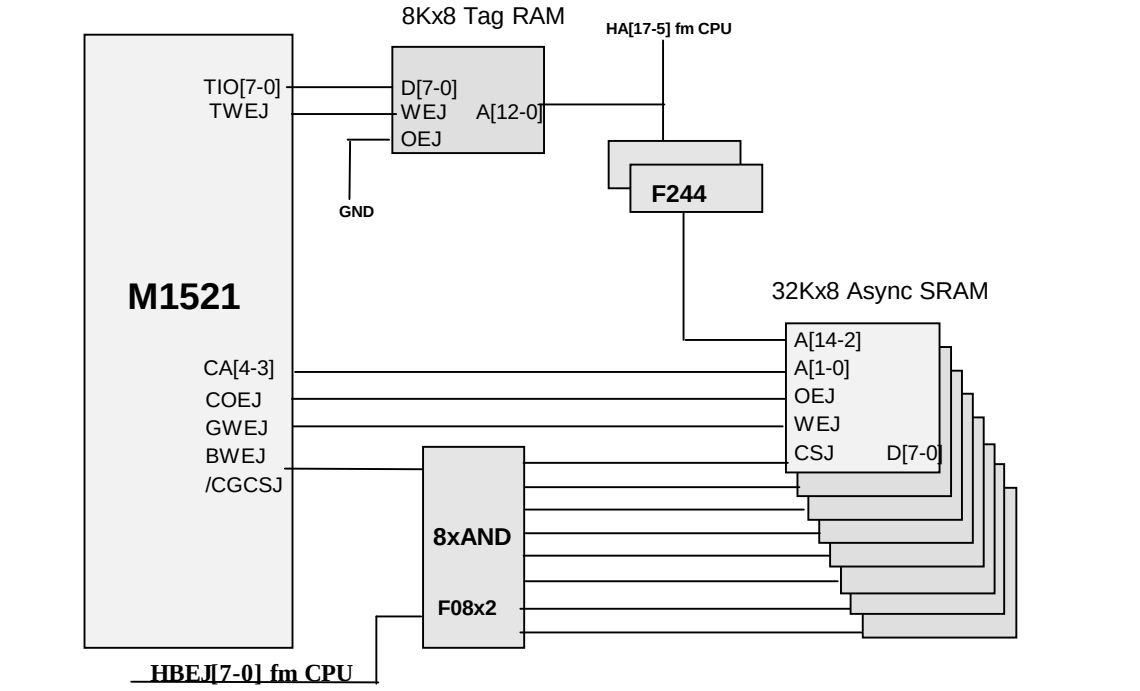
Configuration		**DATA SRAM**			**TAG SRAM**				**Internal**
Cache Type	Cache Size	Size	Bank	Address lines	Address lines	Data Lines	Tag Size	Cacheable DRAM Size	**MESI**
ASRAM	256K	(32K8)*8	1	A3-A17	A5-A17	A18-A25	8K8	64M	8K2
ASRAM	512K	(64K8)*8	1	A3-A18	A5-A18	A19-A25	16K8	64M TAG[7] as dirty bit	16K1 valid bit
ASRAM	1M	(128K8)*8	1	A3-A19	A5-A19	A20-A25	32K8	64M TAG[7] as dirty bit TAG[6] as valid bit	Disable
PBSRAM	256K	(32K32)*2	1	A3-A17	A5-A17	A18-A25	8K8	64M	8K2
PBSRAM	512K	(64K16)*4	1	A3-A18	A5-A18	A19-A25	16K8	64M TAG[7] as dirty bit	16K1 valid bit
2 Bank PBSRAM	512K	(32K32)*4	2	A3-A18	A5-A18	A19-A25	16K8	64M TAG[7] as dirty bit	16K1 valid bit
ASRAM	256K	(32K8)*8	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2
ASRAM	512K	(64K8)*8	1	A3-A18	A5-A18	A19-A27	16K10	256M TAG[7] as dirty bit	16K1 valid bit
ASRAM	1M	(128K8)*8	1	A3-A19	A5-A19	A20-A27	32K10	256M TAG[7] as dirty bit TAG[6] as valid bit	Disable
PBSRAM	256K	(32K32)*2	1	A3-A17	A5-A17	A18-A25	8K10	256M	8K2
PBSRAM	512K	(64K16)*4	1	A3-A18	A5-A18	A19-A25	16K10	256M TAG[7] as dirty bit	16K1 valid bit
2 Bank PBSRAM	512K	(32K32)*4	2	A3-A18	A5-A18	A19-A25	16K10	256M TAG[7] as dirty bit	16K1 valid bit
ASRAM	256K	(32K8)*8	1	A3-A17	A5-A17	A18-A28	8K11	512M	8K2
ASRAM	512K	(64K8)*8	1	A3-A18	A5-A18	A19-A28	16K11	512M TAG[7] as dirty bit	16K1 valid bit
ASRAM	1M	(128K8)*8	1	A3- A19	A5-A19	A20-A28	32K11	512M TAG[7] as dirty bit TAG[6] as valid bit	Disable
PBSRAM	256K	(32K32)*2	1	A3-A17	A5-A17	A18-A25	8K11	512M	8K2
PBSRAM	512K	(64K16)*4	1	A3-A18	A5-A18	A19-A25	16K11	512M TAG[7] as dirty bit	16K1 valid bit
2 Bank PBSRAM	512K	(32K32)*4	2	A3-A18	A5-A18	A19-A25	16K11	512M TAG[7] as dirty bit	16K1 valid bit

The following table shows the different standard SRAM access time requirements for different CPU clock frequencies.

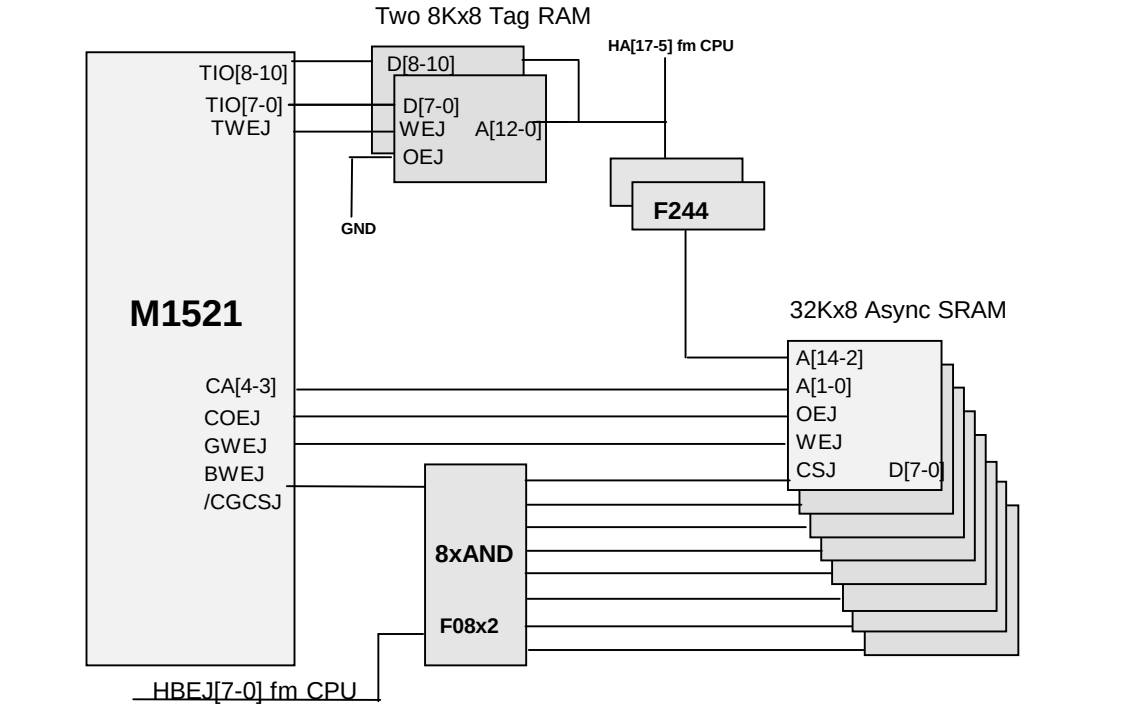
CPU Bus Frequency (MHz)	PBSRAM Clock-to-Output Access Time (ns)	Async. SRAM Access Time (ns)	Tag RAM Access Time (ns)
50	13.5	20	20
60	10	15	15
66	8.5	15	15

In the following figures, four recommended cache subsystems are shown as follows :

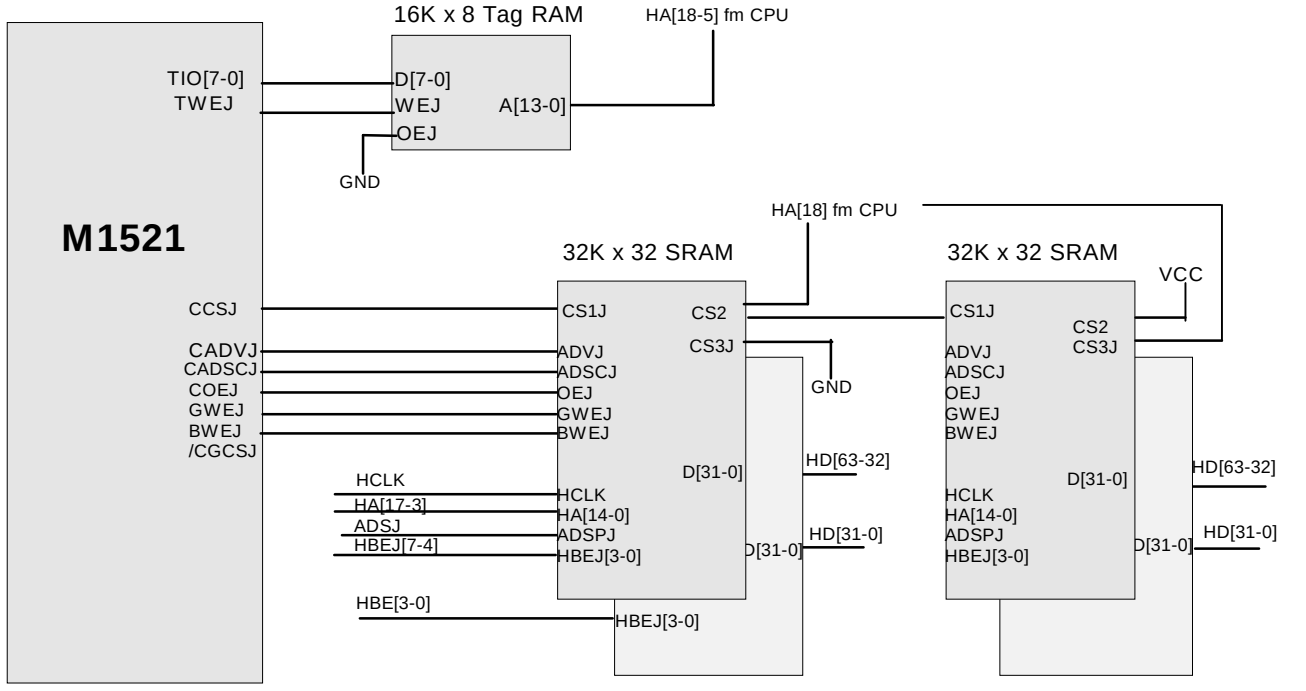
Asynchronous L2 with 256K & 8-bit Tag RAM (64M cacheable region)



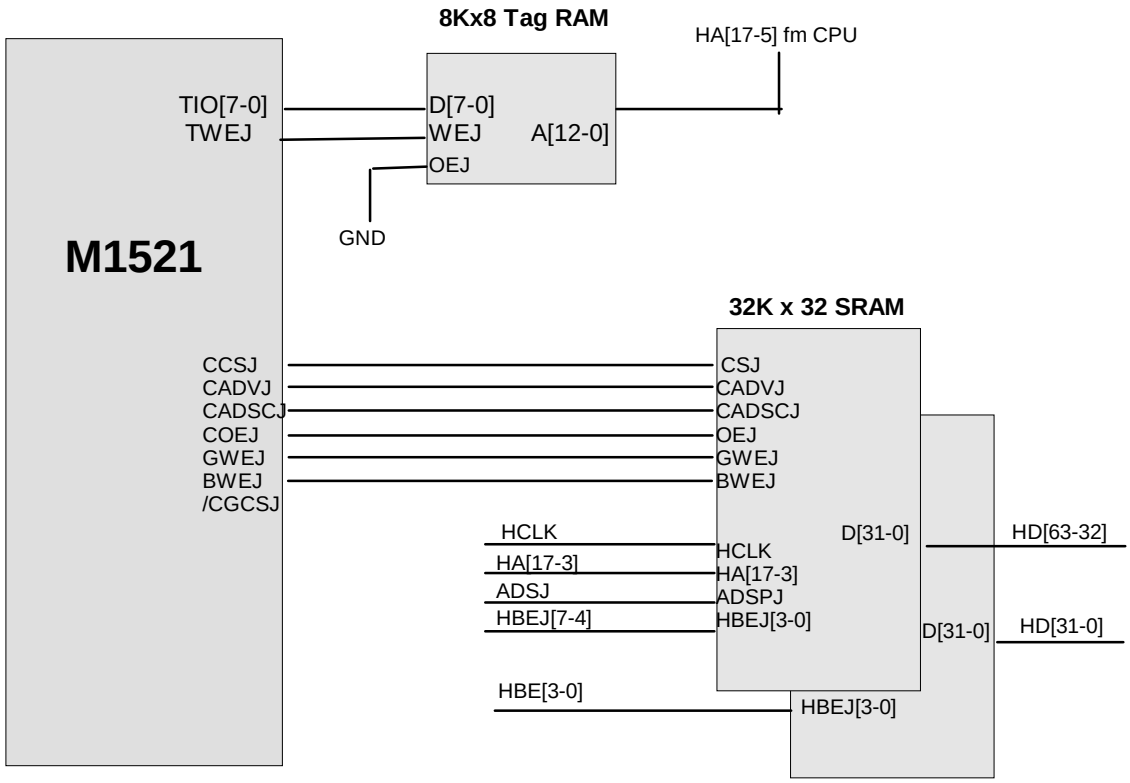
Asynchronous L2 with 256K & 11-bit Tag RAM (512M cacheable region)



Pipelined Burst SRAM L2 with 512K & 8-bit Tag RAM (64M cacheable region)



Pipelined Burst SRAM L2 with 256K & 8-bit Tag RAM (64M cacheable region)



3.3 SYSTEM MEMORY TIMING/CONFIGURATION

The DRAM controller of the M1521 supports a variety of DRAM types and improves the 1st data transaction performance by using a speculative cycle to shorten the latency. Basically, it supports a 64-bit memory bus for 8 banks of single-sided SIMMs or 4 banks of double sided SIMMs. For best system memory configuration in Windows 95 & UMA architecture, ALADDIN III supports six single-sided 32-bit populated DRAM banks or three double-sided 32-bit populated DRAM banks. The system memory can be easily configured to 12MB by using the most popular 16-Mbit memory types. In this configuration, one bank is 64-bit 8MB shared with UMA, and the other bank is 32-bit 4MB. In the upgrade path, all banks can be extended to 64-bit memory. M1521 also supports the most flexible 32-bit memory population, it supports low DWord and High DWord population.

The controller can handle 8 banks of single-sided or 4 banks of double-sided 64-bit memory, with the memory size from 4MB to 1GB. It also supports a programmable driving capability of MA/RAS/CAS/WE to optimize the access timing and the system cost in certain system memory configurations. MA[0-1] are duplicated to gain the timing design of the system. Both the EDO and FPM are supported with an optimized timing to support the possible cacheless systems in low end market segments. The SDRAM features are also configured in this chip.

In terms of UMA, a programmable memory size, 0.5/1/2/3/4MB, can be mapped to an arbitrary location as a frame buffer, accessed by the GC (Graphics Controller). For the DCI/DirectDraw architecture, the system supports an ALIAS REGION, which allows the M1521 to directly access the Frame Buffer, not through the PCI and GC.

As to the System Management RAM (SMRAM), the chip allows several optional noncacheable space to map the SMRAM which includes regions such as 38000h-3FFFFh to B page, A/B region to A/B page and D page to B region.

3.3.1 Memory Type supported

Table 1 - Memory Structure Supported

Memory Structure	Address mode	Address size
4Mbits		
512Kx8	Asymmetric	10x9
1Mx4	Symmetric	10x10
16Mbits		
1Mx16	Asymmetric	12x8
1Mx16	Symmetric	10x10
2Mx8	Asymmetric	11x10
4Mx4	Symmetric	11x11
4Mx4	Asymmetric	12x10
64Mbits		
4Mx16	Symmetric	11x11
8Mx8	Asymmetric	12x11
16Mx4	Symmetric	12x12

3.3.2 MA Mapping Table supported

In the following table, ALADDIN-III supports a versatile memory MA mapping table to accommodate many different approaches of graphics controller (GC) in UMA which includes the current draft of VESA standards. Furthermore, it supports the 32-bit memory bus on each possible available bank.

Table 2 - Several DRAM Address translation supported for some specific purpose

Normal DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A24/25	A23	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A26	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

Row MA[11] : If 64Mbits DRAM is not populated, then A24 is driven; if 64Mbits DRAM is populated, then A25 is driven

1M x 16 DRAM Address Translation Table

Specific DRAM Address Translation Table for Asymmetric 1M x 16

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A22	A21	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column					A10	A9	A8	A7	A6	A5	A4	A3

Address Size = 12 x 8

32-bit bank DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A23/A24	A22	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A25	A23	A21	A4	A10	A9	A8	A7	A6	A5	(A2)	A3

Row MA[11] : if 64Mbits DRAM is not populated, then A23 is driven; if 64Mbits DRAM is populated, then A24 is driven

32-bit Bank 1M x 16 DRAM Address Translation Table

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A10	A21	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column					A4	A9	A8	A7	A6	A5	(A2)	A3

Address Size = 12 x 8

16MB Synchronous DRAM Address Translation Table:

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A11	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A11	0	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

3.3.3 Outstanding DRAM timing

The following table shows the timing of BEDO/EDO/FPM DRAMs:

Table 1. Lead time of first data transaction, check time at T2

r.lead	**w.lead**	**ras.prch**	**t.lead(t2)**	**sle.lead**	**ras-cas**	**read..hit**	**wr..hit**	**r.row.mis**	**r.pg.mis**	**w.rtr.row.m**	**w.rtr.pg.ms**
6	5	3	-1	-1	3	4	5	7	10	8	11
6	5	3	-1	-1	2	4	5	6	9	7	10
6	5	4	-1	-1	3	4	5	7	11	8	12
6	5	4	-1	-1	2	4	5	6	10	7	11
6	5	3	-1	0	3	5	5	8	11	8	11
6	5	3	-1	0	2	5	5	7	10	7	10
6	5	4	-1	0	3	5	5	8	12	8	12
6	5	4	-1	0	2	5	5	7	11	7	11

Note: r.lead means “read lead off cycle” w.lead means “write lead off cycle”
ras.prch means “RAS precharge time”, and is controlled by Index -44h bit2.
t.lead (t2) means “Hit/Miss check point”, and is controlled by Index-40h bit0.
sle.lead means “Read Speculative Leadoff”, and is controlled by Index-45h bit5.
ras-cas means “RAS to CAS delay”, and is controlled by Index-44h bit3.
read hit means “read hit lead off cycle”
write hit means “write hit lead off cycle”
r.row.mis means “read row miss lead off cycle”
r.pg.mis means “read page miss lead off cycle”
w.rtr.rw.m means “write buffer retired write row miss cycle”
w.rtr.pg.ms means “write buffer retired write page miss cycle”

Table 2. CPU to DRAM read performance Summary for BEDO/EDO/FPM DRAMs

DRAM speed	**DRAM type**	**Performance (in Host CLK)**		
Read (Burst rate)		50 Mhz	60 MHz	66 Mhz
50 ns	BEDO	x-111	x-111	x-111
	EDO	x-222	x-222	x-222
	FPM	x-333	x-333	x-333
60 ns	BEDO	x-111	x-111	x-222
	EDO	x-222	x-222	x-222
	FPM	x-333	x-333	x-333
70 ns	BEDO	x-111	x-222	x-222
	EDO	x-333	x-333	x-333
	FPM	x-333	x-444	x-444

Rd.Phit/Pmiss/Rdmiss lead Page hit		50/60 Mhz	66 Mhz
60 ns	BEDO	5	6
60 ns	EDO/FPM	4	5
Row Miss			
60 ns	BEDO	7	8
60 ns	EDO/FPM	6	7
Page Miss			
60 ns	BEDO	10	11
60 ns	EDO/FPM	9	10

Back-to-back Burst Reads with Page hit		50/60 Mhz	66 Mhz
60 ns	BEDO	5-111-1111	6-111-1111
60 ns	EDO	4-222-2222	5-222-2222
60 ns	FPM	4-333-3333	5-333-3333

Table 3. CPU to DRAM Write Performance Summary

DRAM speed	DRAM type	Performance (in Host CLK)	
Posted Single Write with Write buffer Empty		50 Mhz	60/66 Mhz
60 ns	BEDO/EDO/FPM	3.3.3	3.3.3

Posted Single Write with Write buffer Empty		50 Mhz	60/66 Mhz
60 ns	BEDO/EDO/FPM	3-111	3-111

Single Retire Hit		50/60 MHz	66 Mhz
50 ns	BEDO	1	1
60 ns	EDO	2	2
60 ns	FPM	2	3

Single Retire row Miss with RAS-CAS = 2T		50/60 Mhz	66 Mhz
50 ns	BEDO	5	6
60 ns	EDO	4	4
60 ns	FPM	4	5

Single Retire Page Miss with RAS-CAS = 2T		50/60 Mhz	60/66 Mhz
50 ns	BEDO	7	8
60 ns	EDO	7	7
60 ns	FPM	7	8

Retire Burst		50/60 Mhz	66 Mhz
50 ns	BEDO	x-111	x-111
60 ns	EDO	x-222	x-222
60 ns	FPM	x-222	x-333

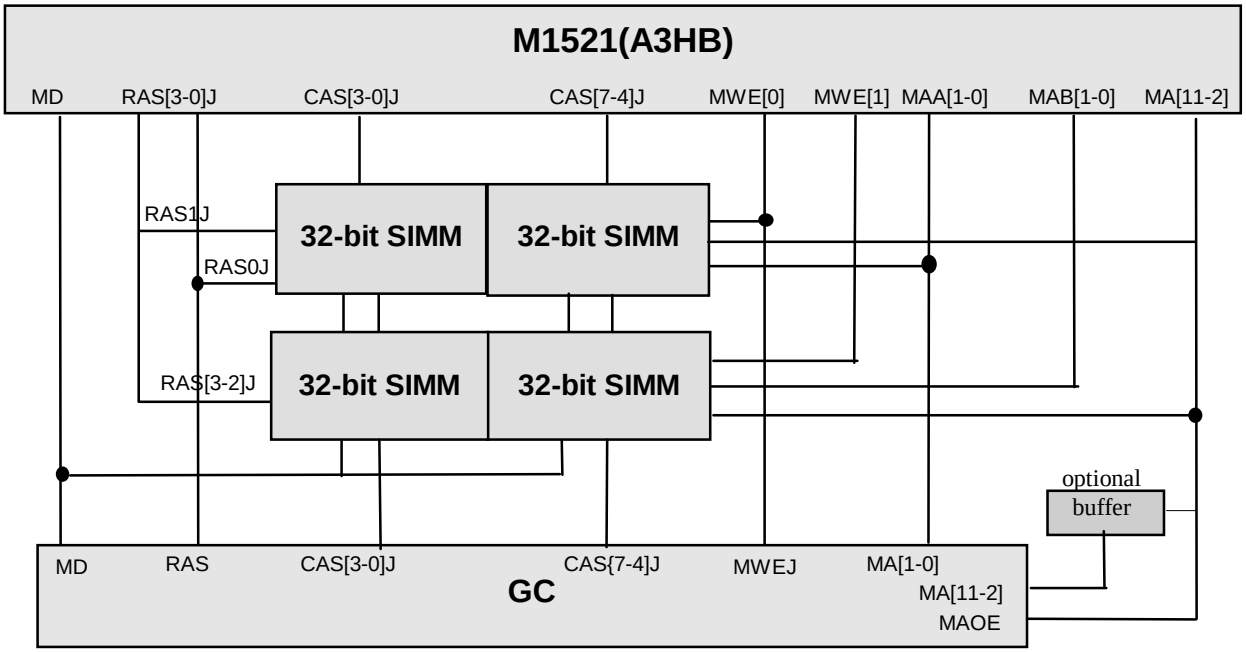
Table 4. SDRAM Performance Summary

Cycle Type	66 MHz		60 MHz		50 MHz	
CAS Latency	CL=3	CL=2	CL=3	CL=2	CL=3	CL=2
Burst Read Page Hit	7-1-1-1	6-1-1-1	7-1-1-1	6-1-1-1	7-1-1-1	6-1-1-1
Read Row Miss	10-1-1-1	8-1-1-1	10-1-1-1	8-1-1-1	10-1-1-1	8-1-1-1
Read Page Miss	14-1-1-1	11-1-1-1	14-1-1-1	11-1-1-1	14-1-1-1	11-1-1-1
Back-to-back Burst Read Page Hit	7-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1	7-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1	7-1-1-1-2-1-1-1	6-1-1-1-2-1-1-1
Write Page Hit	3	3	3	3	3	3
Write Row Miss	6	5	6	5	6	5
Write Page Miss	10	8	10	8	10	8
Posted Write	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1	3-1-1-1
Write Retire rate from Posted Write Buffer	-1-1-1	-1-1-1	-1-1-1	-1-1-1	-1-1-1	-1-1-1

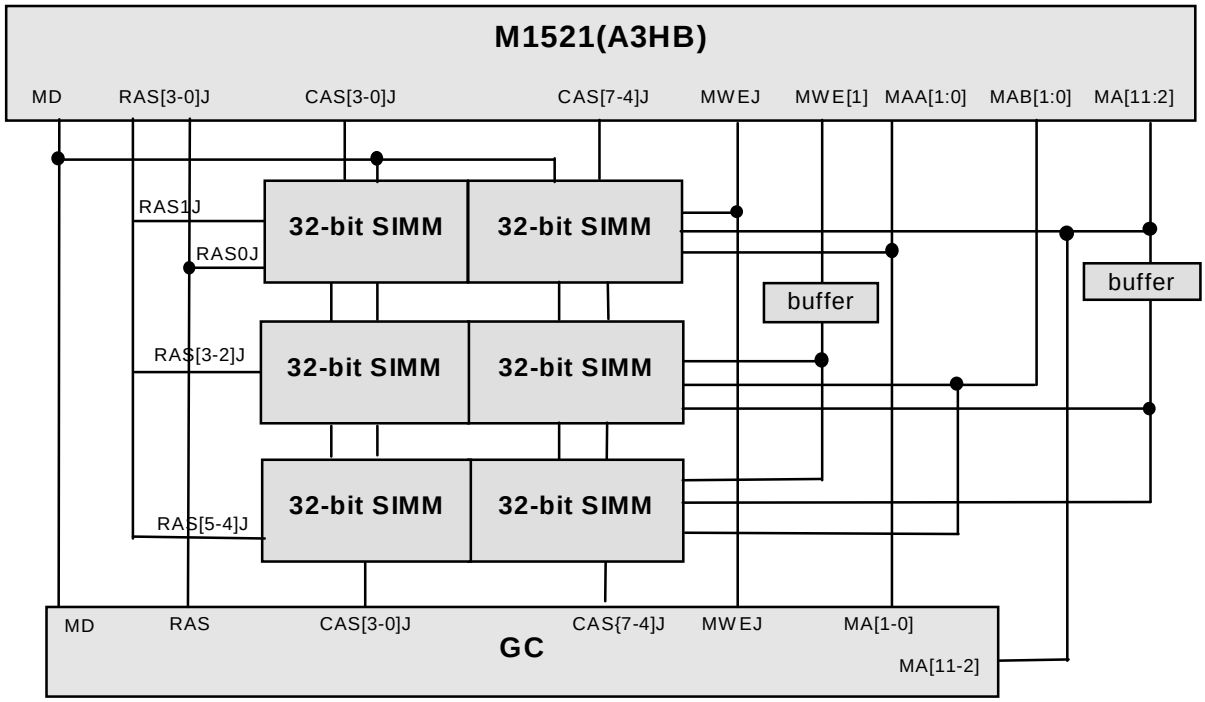
3.3.4 EDO/FPM/(BEDO) DRAM Configuration

ALADDIN-III supports 8 banks of single sided SIMMs or 4 banks of double sided SIMMs maximum so that any mentioned combination can be fully supported. But in UMA, ALADDIN-III would prefer to recommend the limited number of banks be implemented, 3 double-sided banks or 6 single-sided banks maximum. Certainly, the driver of the GC must be put into consideration to decide the number of banks.

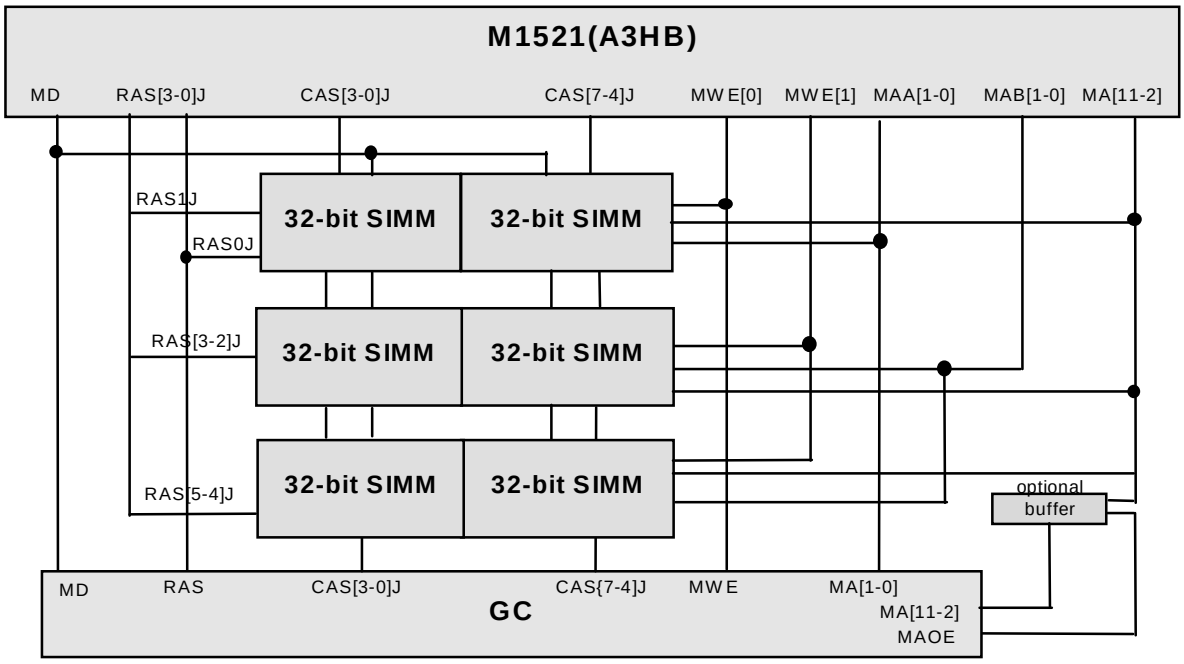
2 Double-Sided DRAM Bank + UMA Driving Organization (EDO/FPM)



3 Double-Sided DRAM Bank + UMA Driving Organization (EDO/FPM) - with buffer

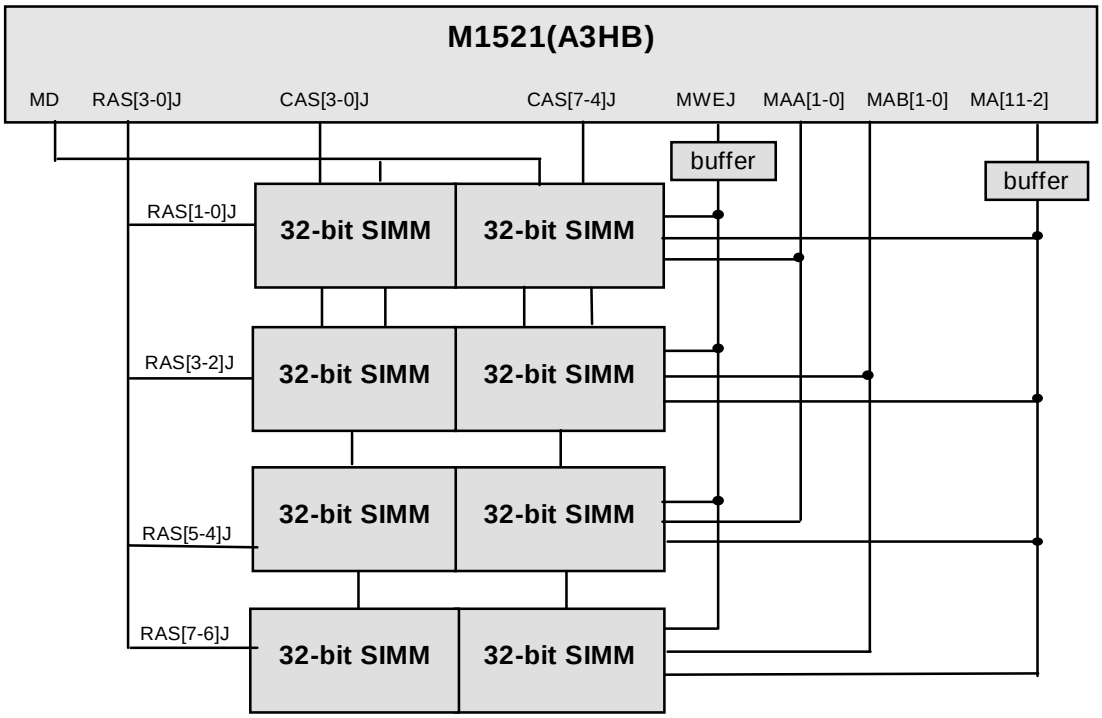


3 Double-Sided DRAM Bank + UMA Driving Organization (EDO/FPM) - without buffer



In this configuration, only x16 DRAMs are recommended since the driving capability of GC should be taken into consideration.

4 Double-Sided DRAM Bank Driving Organization (EDO/FPM)



3.3.5 SDRAM support

ALADDIN-III supports flexible population for up to 6 banks of single-sided or 3 banks of double-sided SDRAM. It can be mixed with FPM/EDO/BEDO on a row by row basis in any order. With graphic controller supporting SDRAM, ALADDIN-III also supports UMA with SDRAM. But, unlike FPM/EDO/BEDO, ALADDIN-III does not support 32-bit population of SDRAM banks.

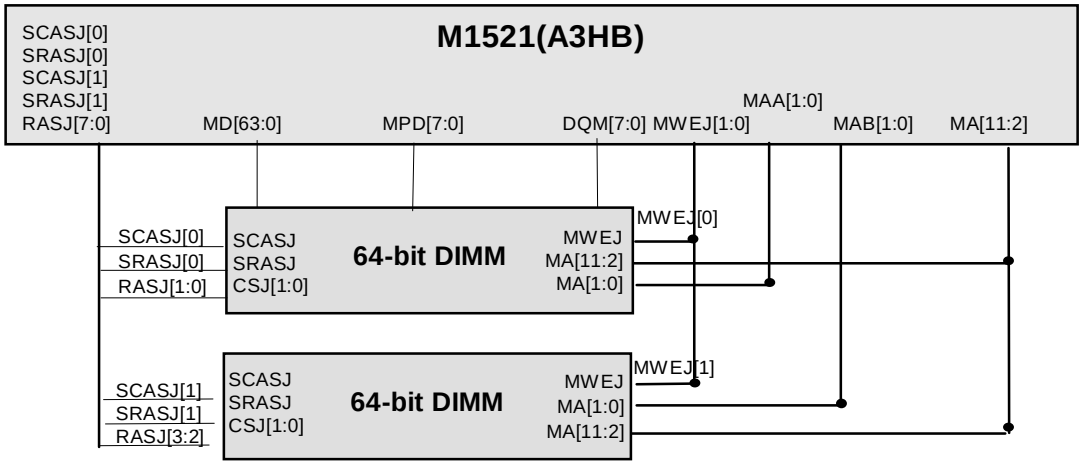
ALADDIN-III utilizes SDRAM commands that support both SDRAM and PC SDRAM. The commands are :

- Mode Register Set (MRS)
- CAS-Before-RAS Refresh (CBR)
- Self-Refresh (SEFR)
- Precharge All Banks (PALL)
- Precharge Selected Bank (PRCH)
- Row Active (RACT)
- Write (WRITE)
- Read (READ)
- No Operation (NOP)

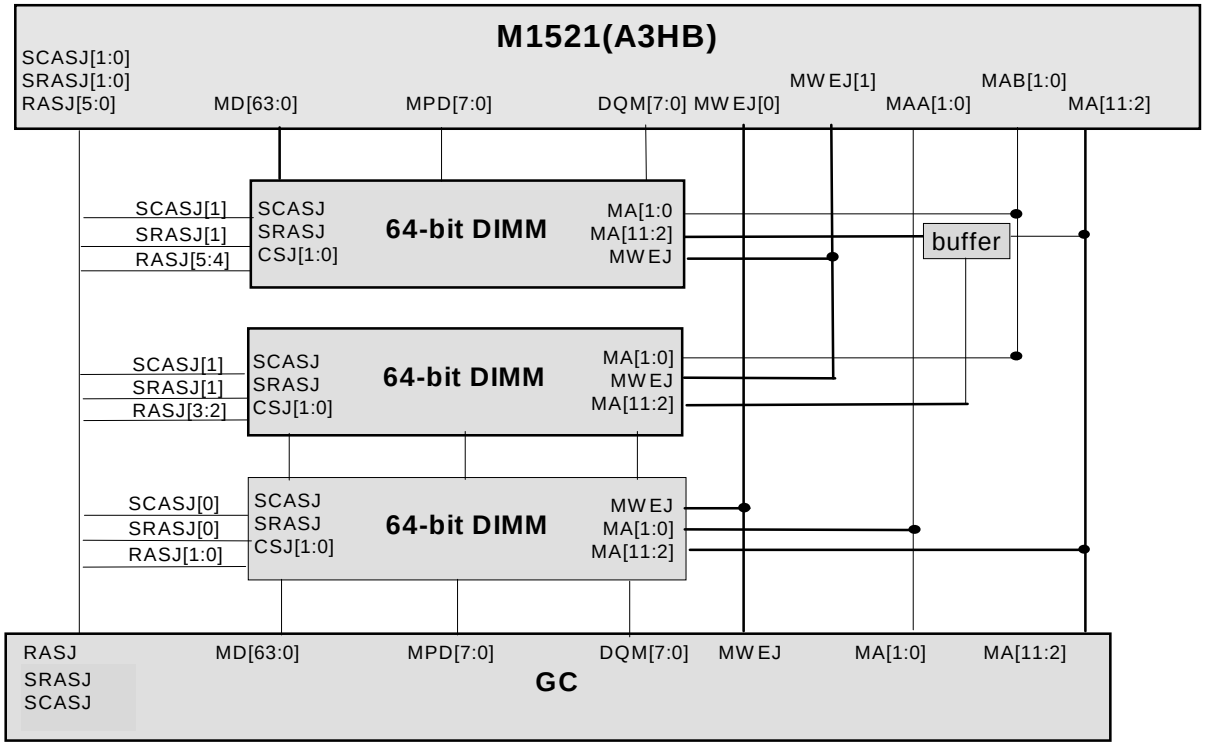
In terms of Wrap Type of SDRAM, ALADDIN-III supports both Interleave mode and Linear (Sequential) mode.

ALADDIN-III supports two sets of SDRAM control signals. Following figures show the topological configuration when supporting SDRAM. The first figure below illustrates 4-bank single-sided or 2-bank double sided support of SDRAM. The following figure shows 6 banks support of SDRAM with UMA. Please refer to Table 5 for the source of SRASJ[1:0], SCASJ[1:0] and MWEJ[1:0].

2 Double-sided DIMM socket with SDRAM & 8-bit Tag



3 Double-Sided SDRAM DIMM socket with UMA & 8-bit Tag



3.3.6 Signal Assignment of DRAM interface

As several DRAM architectures are supported, the signal of each configuration have to be multiplexed to optimize the pinout. Shown here is the signal assignment for each configuration.

Table 5. Signal Assignment of Versatile DRAM Architecture

		without buffer	with buffer		w/o buffer
EDO/Cache/8BK	**4-bank+UMA**	**6-bank+UMA**	**6-bank+UMA**	**4SD.BK+UMA**	**6SD.BK+UMA**
TAG[7:0]	TAG[7:0]	TAG[7:0]	TAG[7:0]	TAG[7:0]	TAG[7:0]
TAG[8]	TAG[8]	TAG[8]	TAG[8]	SCAS1	SCAS1
TAG[9]	TAG[9]	TAG[9]	TAG[9]	SRAS1	SRAS1
TAG[10]	MWE[1]	MWE[1]	TAG[10]	MWE[1]	MWE[1]
RAS0	RAS0	RAS0	RAS0	SCS0	SCS0
RAS1	RAS1	RAS1	RAS1	SCS1	SCS1
RAS2	RAS2	RAS2	RAS2	SCS2	SCS2
RAS3	RAS3	RAS3	RAS3	SCS3	SCS3
RAS4	RAS4	RAS4	RAS4	SCS4	SCS4
RAS5	RAS5	RAS5	RAS5	SCS5	SCS5
RAS6	RAS6	RAS6	RAS6	SCAS0	SCAS0
RAS7	RAS7	RAS7	RAS7	SRAS0	SRAS0
CAS[7-0]	CAS[7-0]	CAS[7-0]	CAS[7-0]	DQM[7-0]	DQM[7-0]
MAA[1-0]	MAA[1-0]	MAA[1-0]	MAA[1-0]	MAA[1-0]	MAA[1-0]
MAB[1-0]	MAB[1-0]	MAB[1-0]	MAB[1-0]	MAB[1-0]	MAB[1-0]
MWE[0]	MWE[0]	MWE[0]	MWE[0]	MWE[0]	MWE[0]

3.3.7 DRAM Load Analysis for each memory configuration and memory type.

The existing versatile/ complicated memory configuration, which might result in a big variation of DRAM loading and the control signal timing. ALADDIN-III is designed to target some large reasonable memory types and number of banks to optimize COST and TIMING.

3.4 PCI MASTER Latency and Throughput Analysis

3.4.1 Smart Deep Post Write & Prefetch Buffer

The M1521 includes 22 DWORD PCI-to-DRAM posted write buffers to enhance the PCI master bandwidth of accessing DRAM. With the implementation of L1/L2 writeback merge and smart buffer management, the M1521 can sustain the ultimate 133 Mbps bandwidth for PCI master writing to local memory. More significantly, the maximum bandwidth is independent of results from the L1/L2 snooping and writeback cycle, the DRAM types and L2 types.

The M1521 includes 22 DWORD PCI-to-DRAM read prefetch buffers to enhance the PCI Master bandwidth of accessing DRAM. With the implementation of L1/L2 writeback and smart buffer management, the M1521 can sustain the ultimate 133 Mbps bandwidth for PCI Master reading from Local memory. And the maximum bandwidth is independent of results of the L1/L2 snooping, writeback cycle and L2 types.

3.4.2 PCI 2.1 Compliant

The M1521 is fully compliant to the PCI 2.1 Specification. With the flexible PCI latency control, it can achieve the best system performance.

3.4.3 Pipelined Snoop Ahead

The M1521 uses an enhanced pipelined snoop protocol to minimize the L1 & L2 snoop overhead. It combines with the deep smart read/write buffer to optimize PCI master performance.

3.4.4 PCI Arbiter

The M1521 integrates an enhanced PCI arbiter. It provides a fair arbitration by using a PCI and CPU Time Slice mechanism and supports up to 4 PCI masters. It can also support a 5th PCI master by programming MREQJ and MGNTJ as another PCI master arbitration signal. It also supports passive release of PCI 2.1 latency requirements.

3.5 UNIFIED MEMORY Architecture Requirement/ Analysis

The M1521 supports a unified memory architecture (UMA) interface which allows the frame buffer of on-board graphics controller (GC) to be implemented using the system main memory, rather than dedicated graphics memory. In the ALADDIN-III, it supports 2-signal and 3-signal protocol to arbitrate memory bus ownership between the system and GC. To optimize the memory bus utilization and shorten the host request latency, the protocol supports Hi/Lo priority request from the GC. The reason to support two kinds of protocols is to meet several proposals from several GC/System controller vendors before the VESA standard. Currently, the protocol will include the current VESA draft both the BIOS and the handshake signal definitions. The signal names of these two pin protocols are MREQJ and MGNTJ. Depending on the MREQ's waveform, the M1521 will distinguish between High or Low priority. Furthermore, there is a third signal named HPRIO, which is used to tell the priority.

3.5.1 UMA MEMORY MAPPING

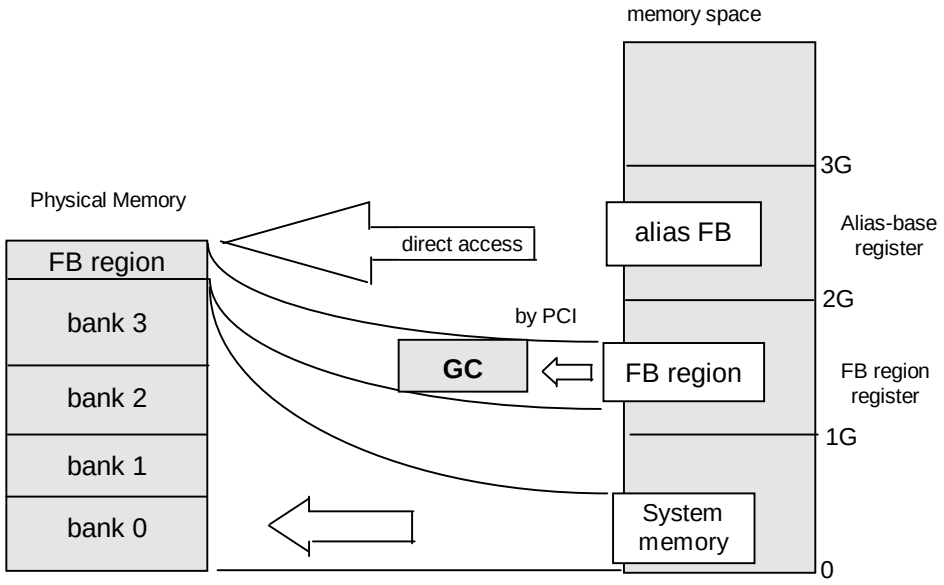
The ALADDIN-III is designed for 4-bank DRAM under the UMA architecture to relieve GC of driving concern. Otherwise, it might support 8-banks. So in the following contents, 4-banks are used as an example to describe the memory mapping.

There is only one bank that can be used as a SHARED BANK due to the pin limitations (RAS) of the GC. This bank can be any bank programmed by BIOS depending on the hardware implementation. In the diagram, we see that the system memory always start from address 0 to the top of the system memory which is decided by substracting frame buffer size from DRAM size. Physically, the frame buffer region will be next to the system memory cell. In Address Space of host, one might reallocate the frame buffer to arbitrary location by using a BASE REGISTER, defined in the M1521. The following figure is a possible application example.

In ALADDIN-III's UMA, it allows the host to access the frame buffer memory through two paths, one is latency device goes through PCI. The other is to directly access by system controller with an ALIAS MAPPING mechanism which will allow the host to access the 1G + BASE region which will be mapped to the same frame buffer region as the latency device did. The alias mapping can be disabled.

In ALADDIN-III, all the PCI memory and the frame buffer region is noncacheable. The PCI memory is defined by non-local memory or non ALIAS region.

Frame Buffer Region Allocation and Access



3.5.2 The UMA arbitration

To optimize the transition overhead of the memory bus, the protocol is synchronized to the HOST clock. It is also very important to shorten the latency of host request and satisfy the GC's real time requirement in screen refresh, by accepting the Hi-priority request from GC, so that the system can minimize the performance degradation. There are some special mechanisms to achieve this goal.

* The low priority request allows the system performance impact to be minimized, preventing unnecessary system resource stalls during these non-critical GC accesses, such as the line drawing or when GC's FIFO has enough data to be fetched by the display.
* The ALADDIN-III's memory bus is default System Parking.

* The maximum latency seen by the GC when asserting a high priority request is approximately 400ns which is programmable through the M1521 register. And the value will be required to be fine tuned, based on the GC's behavior. The maximum latency of low priority will be dependent on the system activity. For example, if there is no bus activity on PCI bus and CPU bus, the latency will be the smallest.

* In ALADDIN-III, there is a programmable register to record the maximum latency of GC request under high priority which will allow the buffered data in M1521 to be flushed as much as possible and will allow the M1521 to prefetch the data from the DRAM as much as possible before the time out occurs. The maximum value is 28 CPU CLOCKs.

3.6 Low Power Feature

The ALADDIN-III supports a sophisticated power saving feature, called 5V suspend, under which the system will turn off the signal event of host and keep the DRAM refresh active through the M1521's DRAM interface that is triggered by a 32K clock source. After the 5V suspend event is triggered, by programming a bit of M1523's internal register, the M1523 will initiate a handshake with the M1521. During the handshake, the M1523 will issue STPCLK to the host, stop the system clock generator, pull the I/O output level to leakageless polarity and turn on the SUSPEND REFRESH to sustain the DRAM data.

The M1521 and the M1523 are designed with a very sophisticated I/O circuit to perform the leakage control under the power saving mode, which is very popular in notebook designs.

For desktop designs, the 5V suspend can provide the system a very efficient **STAND-ON** feature that is more demanding in future home PC systems.

In the M1523 of ALADDIN-III, the solution gives a deep green function. Regarding deep PMU for Peripheral device, one might design a dedicated PMU device to accompany the 5V suspend feature to form a very deep power saving system, such as a notebook system.

To leave the power saving mode, ALADDIN-III provides several internal event detectors or external event detectors. The system will resume in a very careful/dedicated process and protocol to recover the system to original status, same as the status before entering.

Theoretically, the only power request under the 5V suspend is the circuit of DRAM refresh.

3.7 ECC/Parity algorithm

The M1521 provides an ECC DRAM data integrity feature when Index 49h D0 is set to '1'. The ECC feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DEC-S4ED) for DRAM data integrity. But, the ECC algorithm will not be implemented for the 32-bit only DRAM populated banks. The M1521 will generate 8-bit ECC check bits for 64-bit data to DRAM when the ECC feature is enabled and the current DRAM cycle is a write access operation.

If a partial write (less than 64-bit write) event occurs, a read-modified-write operation will be performed by the M1521. The M1521 will detect all single bit, double-bit errors, and all errors confined to a single nibble when ECC is enabled and a DRAM read is performed. The M1521 also corrects all single-bit errors and the corrected data is then transferred to the requestor (CPU or PCI). This corrected data will not be written back to DRAM in the current M1521 version. The ECC error reporting condition and status are defined in Index 49h-4Ah. The ECC errors are latched until cleared by software. The software programmer also can detect 64 from 72-bit wide SIMMs or check ECC circuit operations via the ECC (parity) test mode (Index 49h D1 set to '1'). The ECC check bits (or parities) can be forced to any value (defined in Index 4Bh) during all DRAM write access cycles in the ECC/Parity test mode. All the DRAM read leadoff latency timings should add 1 HCLK when the ECC feature is enabled.

The M1521 also provides another DRAM data integrity feature -- conventional DRAM even parity generation and checking when Index 49h D0 is set to '0'. The DRAM parity checking error reporting condition and status also are defined in Index 49h-4Ah. The DRAM parity generation and checking feature will also be supported to the 32-bit only DRAM populated banks. The software can differentiate the 64 from 72-bit wide SIMMs or check parity circuit operation via the ECC/Parity test mode.

3.8 DRAM Refresh

The M1521 provides CAS-before-RAS (CBR) refresh and RAS-only refresh. Both refresh methods use "staggered" and "smart refresh" (i.e. refresh is only performed on banks that are populated) algorithm. The DRAM refresh rate can be controlled via the Index 45h D1-D0. For shortening the GC request latency (UMA requirements), the DRAM banks can be distributed to 2 groups for performing DRAM refresh operations when Index 45h D7 is set to '1' and the total banks of populated DRAM exceeds 4. On the other hand, when "distributed DRAM refresh" is enabled, the refresh rate will become half of the original rate for the same DRAM bank.

Section 4 : Configuration Registers

I. M1521 PCI Mechanism #1 Configuration Cycle Ports

Register Name : **CFGADR** - Configuration Address Register
I/O Address 0CF8h
Default Value 00000000h
Attribute Read/Write
Size This register must be 32-bit I/O access in PCI configuration access mechanism #1. An 8-bit or 16-bit access will pass through the Configuration Address Register onto the PCI bus.

Bit Number	Bit Function
31(0)	0 : Configuration Disable 1 : Configuration Enable. When this bit is set to 1 accesses to PCI configuration space are enabled, otherwise, accesses to PCI configuration space are disabled.
30-24 (00h)	reserved.
23-16 (00h)	Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to the M1521 and a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on the PCI bus.
15-11 (00h)	Device Number. It is used by M1521 to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when BUS Number is 0h. As for the others, the M1521 will send the configuration to a PCI or PCI bridge device.
10-8(0h)	Function Number. It is used to select a specific device function during initialization.
7-2 (00h)	Register Number. It is used to select a specific register during initialization.
1-0 (0h)	Reserved. Fixed at '00'.

Register Name : **CFGDAT** - Configuration Data Register
I/O Address 0CFCh
Default Value 00000000h
Attribute Read/Write
Size This register may be 8-bit or 16-bit or 32-bit I/O access in configuration access mechanism #1.
Description This register contains the information which is sent or received during the PCI bus data phase of configuration write or read cycles. CPU access of 8, 16 or 32 bits wide to this register are supported.

Note : M1521 only supports PCI mechanism #1 access.

II. M1521 PCI Configuration Space Mapped Registers

The M1521 will respond to CPU/PCI configuration access for which AD16 is high during the address phase.

Register Name : VID - Vendor Identification Register
Register Index **01h-00h**
Default Value 10B9h
Attribute Read Only
Size 16 bits
Description This is a 16-bit value assigned to Acer Labs Inc. This register is combined with index 03h-02h uniquely to identify any PCI device. Write to this register has no effect.

Register Name: DID - Device Identification Register
Register Index **03h-02h**
Default Value 1521h
Attribute Read Only
Size 16 bits
Description This is a 16-bit value assigned to the M1521.

Register Name : COM - Command Register
Register Index **05h-04h**
Default Value 0006h
Attribute Read/Write
Size 16 bits

Bit Number	Bit Function
15-9(000h)	reserved
8 (0)	Enable the SERRJ driver. 0 : Disable. 1 : Enable. When this bit is set, the M1521 will enable SERRJ output driver. This bit is reset to 0 and should be set to 1 once memory has been scrubbed by BIOS in systems that wish to report memory errors.
7 (0)	Enable Address/Data Stepping M1521 does not support this. Write to this bit has no effect.
6(0)	Respond to Parity Errors 0 : Disable. 1 : Enabled. The M1521 will do a PCI parity check in CPU to PCI read and PCI to local memory write. This bit is used to enable the parity check. When a parity error is detected, the M1521 will assert SERRJ and set the Parity Error Bit in the DS register.
5(0)	Enable VGA Palette Snooping. M1521 does not support this. Write to this bit has no effect.
4(0)	Enable Postable Memory Write Command. M1521 does not support this. Write to this bit has no effect.
3 (0)	Enable Special Cycle. M1521 does not support this. Write to this bit has no effect.
2 (1)	Control to Act As a PCI Bus Master. M1521 does not support to disable bus master operations. This bit is set to 1 during Power-On to enable PCI master operations. Write to this bit has no effect.
1 (1)	Enable Response to Memory Access. M1521 always accepts PCI master accesses to local memory. Write to this bit has no effect.
0(0)	Enable Response to I/O Access. M1521 does not respond to any PCI master I/O accesses. Write to this bit has no effect.

Register Name: DS - Device Status Register
Register Index **07h-06h**
Default Value 0400h
Attribute Read Only, Read/Write Clear
Size 16 bits

Bit Number	Bit Function
15 (0)	Detected Parity Error. This bit is set by the M1521 whenever it detects a parity error in a PCI transaction even if parity error handling is disabled (As controlled by bit6 in the command register). Software can reset this bit to 0 by writing a 1 to it.
14(0)	Signaled System Error. The M1521 will set this bit whenever it asserts SERRJ. Software can reset this bit to 0 by writing a 1 to it.
13 (0)	Received Master Abort. This bit is set by M1521 whenever it terminates a transaction with master abort. This bit is cleared by writing a 1 to it.
12 (0)	Received Target Abort. This bit is set by the M1521 whenever its initiated transaction is terminated with a target abort. This bit is cleared by writing a 1 to it.
11(0)	Sent Target Abort. This bit is set by devices that act as a target to terminate a transaction by target abort. The M1521 never terminates a transaction with target abort therefore this bit is never set. A write to this bit has no effect.
10-9(10)	DEVSELJ Timing. 00 : Fast 01 : Medium 10 : Slow The M1521 timing for DEVSELJ assertion. Slow timing is selected.
8-0(000h)	Reserved.

Register Name : RI - Revision ID Register
Register Index **08h**
Default Value 01h(A0 Stepping)
Attribute Read Only
Size 8 bits
Description This register contains the version no. of M1521. The value 01 means A0 stepping.

Register Name : CC - Class Code Register
Register Index **0Bh-09h**
Default Value 060000h
Attribute : Read Only
Size : 24 bits
Description : These registers contain the Class Codes of the M1521.

Register Name : LT - PCI Latency Timer value
Register Index : **0Dh**
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

Bit Number	**Bit Function**
7-3(4h)	Master Latency Timer Count Value. LT is used to control the amount of time the M1521, as a bus master, can burst data to the PCI Bus. It can be used to guarantee a minimum amount of the system resources
2-0(0h)	Reserved. They are assumed to be 0 when determining the Count Value.

Register Name : Reserved Registers
Register Index : **3Fh-0Eh**
Default Value : 00h
Attribute : Read Only

Register Name : L2CP - L2 Cache Performance
Register Index: **40h**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	**Bit Function**
7-5 (0h)	reserved.
4 (0)	L1 Snoop HITMJ Check Point. 0 : 3rd CPU Clock after asserting EADSJ. 1 : 2nd CPU Clock after asserting EADSJ. This bit controls the HITMJ strobe point during L1 snoop cycle. Value 1 is recommended during normal operation.
3 (0)	L2 Asynchronous SRAM Write Cycle Wait State. 0 : X-3-3-3. 1 : X-2-2-2. X is defined by Offset 40 Bit 0, Bit 0=0, X=5, Bit 0=1, X=4. This bit controls L2 Asynchronous SRAM write access wait state.
2(0)	L2 Async. SRAM Read Cycle Wait State. 0 : X-3-3-3. 1 : X-2-2-2. X is defined by Offset 40 Bit 0, Bit 0=0, X=4, Bit 0=1, X=3. This bit controls L2 Asynchronous SRAM read access wait state.
1(0)	Early CA4/CA3 toggle feature. 0 : Disable. 1 : Enable When this bit is enabled, CA4/CA3 will toggle in CPU Clock falling edge. This feature should be disabled when system isoperating in low-speed situation (60 and 50 MHz CPU bus frequency). This feature is used to increase Asynchronous SRAM cache address access time.
0(0)	Hit/Miss Check Point (L2 Hit/Miss & DRAM Page Hit/Miss). 0 : T3end (3rd CPU Clock after Sampling ADSJ). 1 : T2end (2nd CPU Clock after Sampling ADSJ). This bit is for test purpose only. In normal operation, this should be programmed as 1.

Register Name : L2CCI - L2 Cache Configuration-1
Register Index: **41h**
Default Value: 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	**Bit Function**
7-6(00)	L2 Cache Type. 0X : Standard Async. SRAM. 10 : 2-bank Pipelined Burst SRAM. 11 : Pipelined Burst SRAM. BIOS should program the correct L2 configuration for normal operation after sorting L2 cache.
5 (0)	reserved.
4 (0)	Internal MESI Software Test Mode 0 : Disable. 1 : Enable. This bit can be used to test internal MESI tag bits by software. It must be kept '0' in normal operation. Please refer to the MESI Software Test Mode Section.
2-1(00)	L2 Cache Size. 00 : None. 01 : 256K. 10 : 512K. 11 : 1M. Bios should program the correct L2 configuration for normal operation after sorting L2 cache.
3,0(00)	TAG[10-8] Configuration. 00 : TAG[10-8] are disabled. 01 : TAG[10-8] are enabled. 10 : TAG[9-8] are disabled and TAG[10] used as MWEJ[1]. 11 : TAG[9-8] are enabled and TAG[10] used as MWEJ[1]. TAG[10-8] are multifunctional pins and these two bits are used to determine which function is used. 00 means TAG[10-8] as TAG[10-8], but not used to check cache hit/miss. 01 means TAG[10-8] as TAG[10-8] to extend cacheable region up to 512M. 10 means TAG[10-8] as MWEJ[1], SRASJ[1], and SCASJ[1] to support SDRAM config and another MWEJ driver. 11 means TAG[10-8] as MWEJ[1] and TAG[9-8] to support another MWEJ driver and extend cacheable region up to 256M. Please refer to the following table.

The following L2 Cache Table shows the different configurations supported by M1521.

Configuration		**DATA SRAM**			**TAG SRAM**				**Internal**	**x41-**
x41 bit2-1	Cache size	SIZE	Bank	Addr Lines	Addr Lines	Data Lines	Tag Size	Cacheable DRAM Size	**MESI**	**Bit 3,0**
01	256K	(32K8)*8	1	A3-A17	A5-A17	A18-A25	8K8	64M	8K2	00 or 10
10	512K	(64K8)*8	1	A3-A18	A5-A18	A19-A25	16K8	64M TAG[7] as dirty bit	16K1	00 or 10 valid bit
11	1M	(128K8)*8	1	A3-A19	A5-A19	A20-A25	32K8	64M TAG[7] as dirty bit TAG[6] as valid bit	Disable	00 or 10
01	256K	(32K8)*8	1	A3-A17	A5-A17	A18-A27	8K10	256M	8K2	11
10	512K	(64K8)*8	1	A3-A18	A5-A18	A19-A27	16K10	256M TAG[7] as dirty bit	16K1	11 valid bit
11	1M	(128K8)*8	1	A3-A19	A5-A19	A20-A27	32K10	256M TAG[7] as dirty bit TAG[6] as valid bit	Disable	11
01	256K	(32K8)*8	1	A3-A17	A5-A17	A18-A28	8K11	512M	8K2	01
10	512K	(64K8)*8	1	A3-A18	A5-A18	A19-A28	16K11	512M TAG[7] as dirty bit	16K1	01 valid bit
11	1M	(128K8)*8	1	A3-A19	A5-A19	A20-A28	32K11	512M TAG[7] as dirty bit TAG[6] as valid bit	Disable	01

Register Name : L2CCII - L2 Cache Configuration-2
Register Index: 42h
Default Value: 00h
Attribute : Read/Write
Size : 8 bits

Bit Number **Bit Function**

7(0) L2 TAG Output-enable Delay.
0 : Disable.
1 : Enable.
This bit is used to increase L2 Tag data hold time. A '1' is recommended in normal operation.

6-5(00) reserved.

4(0) L2 Dirty Bit Setting.
0 : Normal.
1 : Force Non_dirty (Dirty Bit =0).
When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force non_dirty. This bit is used to initialize L2 cache. Please refer to the hardware and software setup section.

3 (0) Force L2 hit
0 : disable
1 : enable

2 (0) L2 Cache Miss or Invalidate.
0 : Normal.
1 : Force L2 Cache Miss or Invalidate.
When this bit is set to 1, all tag lookups result in a miss. This bit is used to initialize L2 cache. Please refer to the hardware and software setup section.

1 (0) L2 Dirty Bit Setting.
0 : Normal.
1 : Force Dirty (Dirty Bit =1).
When this bit is set to 1, all tag lookups will ignore the tag dirty bit and force dirty. This bit can be used to flush L2 cache in green application. Software can set this bit and then read all l2 cache tag address to flush the cache.

0(0) L2 Cache ON/OFF.
0 : Disable External Cache.
1 : Enable External Cache.
This bit is used to disable or enable L2 cache.

Register Name : L1CDBC - L1 Cache/DRAM Buffer Control
Register Index : 43h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	Row 5 (RAS5J) populated with 32-bit DRAMs 0 : Disable. 1 : Enable.

The M1521 supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.

6(0)	Row 4 (RAS4J) populated with 32 bit DRAM. 0 : Disable. 1 : Enable.

The M1521 supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.

5(0)	Row 3 (RAS3J) populated with 32 bit DRAM. 0 : Disable. 1 : Enable.

The M1521 supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.

4 (0)	Row 2 (RAS2J) populated with 32 bit DRAM. 0 : Disable. 1 : Enable.

The M1521 supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.

3 (0)	Row 1 (RAS1J) populated with 32 bit DRAM 0 : Disable. 1 : Enable.

The M1521 supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.

2(0)	Row 0 (RAS0J) populated with 32 bit DRAM. 0 : Disable. 1 : Enable.

The M1521 supports 32-bit DRAM access. BIOS should program this bit to the correct configuration after DRAM sizing for normal operation.

1(0)	Support DRAM POSTED WRITE BUFFER Read around Write cycle. 0 : Disable. 1 : Enable.

This bit is used to control buffer for back-to-back CPU write and read cycles. Since the M1521 implements the DRAM write buffer to post CPU write cycles, the M1521 will do the read first and then flush the DRAM write buffer if this feature is enabled and the required data of the read cycle do not reside in the buffer. A '1' is recommended for normal operation.

0(0)	L1 Cache ON/OFF. 0 : Disable Internal Cache. 1 : Enable Internal Cache

This bit is used to disable or enable L1 cache. When this bit is reset to 0, the M1521 will negate KENJ to prevent either L1 or L2 line fill. When this bit is set to '1', the M1521 will assert KENJ for cacheable memory cycles.

Register Name : DTCI - DRAM Timing Configuration - 1
Register Index : 44h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6(00)	EDO Detection TIMER. 00 : 128 CPU Clock. 01 : 256 CPU Clock. 10 : 512 CPU Clock. 11 : 1024 CPU Clock. These two bits combined with bit 5 are used to do the EDO detection.
5(0)	EDO Detection Mode 0 : Disable. 1 : Enable The following procedures must be done before activating EDO DRAM detection mode. (1) The banks to be detected should be set as "standard DRAM", i.e. the corresponding bits in offset 60h-6Fh should be set correctly. (2) L1 and L2 should be disabled. (3) Index-45h bit 5 set to '0'.
4(0)	EDO Page mode DRAM Read Timing. 0 : X-3-3-3. 1 : X-2-2-2. This bit is used to control EDO DRAM read timing. Please refer to lead off table to check X value.
3(0)	RAS-to-CAS Delay Time. 0 : 3T. 1 : 2T. This bit controls the RASJ to CASJ delay. T is the CPU clock cycle.
2(0)	RAS Precharge Period. 0 : 4T, and Refresh RAS Assertion 5T. 1 : 3T, and Refresh RAS Assertion 4T. This bit controls the RASJ precharge high time in row miss and refresh cycle. T is the CPU clock cycle.
1(0)	Page Mode DRAM Read Timing. 0 : X-4-4-4 (1H+3L). 1 : X-3-3-3 (1H+2L). This bit is used to control the Page Mode DRAM read timing. Please refer to lead off table for the X value.
0 (0)	EDO or Page Mode DRAM Write Timing. 0 : X-3-3-3. 1 : X-2-2-2. This bit is used to control the EDO or Page Mode DRAM write timing. Please refer to lead off table to check X value.

Register Name : DTCII - DRAM Timing Configuration -2
Register Index : 45h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	Distributed DRAM Refresh Cycle 0 : Disable. 1 : Enable. When UMA is used, all DRAM access cycles should be optimized including DRAM refresh cycle. This feature is used to optimize DRAM refresh cycle.
6(0)	reserved.
5(0)	Read Speculative Leadoff Enable. 0 : Disable. 1 : Enable (CASJ Pre-asserted in T2 when Memory Read). This bit is valid only if index-40h bit 0 ='1'. When set to '1', the DRAM controller read request is presented 1 CPU clock earlier than it normally is, before the final memory target has been decoded. If the memory cycle does not actually target DRAM, the DRAM state machine will terminate and return back its previous state.
4(0)	Refresh Mode. 0 : CAS-before-RAS Mode. 1 : RAS-only Mode. This bit is used to control DRAM refresh mode. In suspend mode, only the CAS-before-RAS mode is supported to save power consumption.
3(0)	CPU to DRAM Page Mode. 0 : DRAM use Page Mode. 1 : DRAM use Non-page Mode. When this bit is set to '1', the M1521 will close the DRAM page after DRAM access. Otherwise, it will keep DRAM page open until next access.
2(0)	Enhanced DRAM Paging Enable 0 : Disable. 1 : Enable. When this bit is enabled, the M1521 will use additional information to close the DRAM page in advance. That is, during DRAM irrelevant cycles, an intelligent guess is done to deassert the RASJ lines and precharge them for later use. This bit is recommended to be set '1' in normal operation to enhance DRAM performance.
1-0(00)	Refresh period. 00 : 1024 CPU Clocks(15 us in 66Mhz) 01 : 2048 CPU Clocks(30 us in 66Mhz) 10 : 4096 CPU Clocks(60 us in 66Mhz) 11 : 8192 CPU Clocks(120 us in 66Mhz) These two bits are used to control the period to refresh DRAMs.

Register Name : PIPEF - Pipe Function
Register Index : 46h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	Burst EDO WCBR program cycle address toggle mode. 0 : Interleave 1 : Linear

This bit is used to control the address toggle mode. Linear mode is used to support M1 Linear Burst order. Otherwise interleave mode is selected.

6(0)	Burst EDO WCBR program cycle 0 : disable 1 : enable

This bit is used to program and test Burst EDO. Please refer to Section 5 for details.

5(0)	Support Dynamic Write-Back for Burst Writes. 0 : Disable. 1 : Enable.

This feature is used to optimize DRAM buffer usage. When CPU issues a burst write cycle and L2 cache is not only enabled but also hit, whether this cycle will direct to L2 cache or DRAM write buffer depends on the availability of the DRAM write buffer. If this feature is enabled and there is still a space in the buffer for the incoming cycle, the data will be pushed into the buffer, instead of the L2 cache. It can keep L2 cache clean to speed up later L2 cache accesses.

4(0)	Supports Dynamic Write-Back for Single Write. 0 : Disable. 1 : Enable.

This feature is used to optimize DRAM buffer usage. When CPU issues a single write cycle and L2 cache is not only enable but also hit, whether this cycle will direct to L2 cache or DRAM write buffer depends on the availability of the DRAM write buffer. If this feature is enabled and there is still a space in the buffer for the incoming cycle, the data will be pushed into the buffer, instead of the L2 cache. It can keep L2 cache clean to speed up later L2 cache access.

3(0)	Burst EDO wait state 0 : 0 wait 1 : 1 wait

This bit is used to add wait states when slow Burst EDO is populated. The Bit setting table below is recommended for different types and Host clock freqs.

Type /freq.	50 Mhz	60 Mhz	70 Mhz
-5	0	0	0
-6	0	0	1
-7	0	1	1

2-0(00)	Pipelined Function Option. 0XX : Disabled. 100 : Enabled and L2 is async. SRAMs 111 : Enabled and L2 is pipelined SRAMs or not installed. other combinations are reserved.

Register Name : MISI - Miscellaneous-1
Register Index : 47h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	Support M1 "1+4" Burst Mode. 0 : Disable. 1 : Enable. This bit is used to support the Cyrix M1 "1+4" mode to toggle cache address, MA issues the correct KENJ.
6(0)	Support M1 Linear Burst Order 0 : Disable. 1 : Enable. This bit is used to support the Cyrix M1 linear burst mode to toggle cache address and MA. When it is disabled, Intel toggle mode (interleaved burst) is selected.
5(0)	14-15M Memory's Location. 0 : Local Memory Area. 1 : Non_Local Memory Area. When this bit is set to '1', all memory access address 14M- 15M will decode as local memory cycle and access local DRAM if total memory size is beyond 15M. Otherwise, it will decode as non local memory and pass through PCI bus.
4(0)	15-16M Memory's Location. 0 : Local Memory Area. 1 : Non_Local Memory Area. When this bit is set to '1', all memory access address 15M-16M will decode as local memory cycle and access local DRAM if total memory size is beyond 16M. Otherwise, it will decode as non local memory and pass through PCI bus.
3(0)	Page A-B as Local Memory Area. 0 : Non_local Memory Area. 1 : Local Memory Area. When this bit is set to '1', all memory access address A0000h- BFFFFh will decode as local memory cycle and access local DRAM. Otherwise, it will decode as non local memory and pass through PCI bus.
2(0)	Force 80000h-9FFFFh as Non_local Memory Area. 0 : Disable. 1 : Enable. When this bit is set to '1', all memory access address 80000h-9FFFFh will decode as non local cycle and pass through PCI bus. Otherwise, it will decode as local memory and access to DRAM.
1-0(00)	Reserved.

Register Name : SMRM - SMRAM Mapping
Register Index : 48h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-5(0h)	Reserved.
4 (0)	SMM Page -A or -B Region Code/Data Split. 0 : Disable. 1 : Enable **NOTE**: This bit is valid only if bit 3-2="01". When this bit is enabled, only DCJ='0' can access SMRAM. CPU data access will pass through PCI bus
3-2(00)	SMRAM Region. 00: SMM Region at D000 Segment will be remapped to B000 Segment 01: SMM Region at A000 or B000 Segment. 10: SMM Region at 3000 Segment will be remapped to B000 Segment 11 : reserved Please refer to the following table.
1 (0)	SMRAM Access Control. 0 : Disable. 1 : Enable. When this bit is disabled, SMRAM can only be accessed during SMI handler. Otherwise, SMRAM area can be accessed any time. This bit is used in SMRAM initialization and must be set to '0' when the initialization process is finished
0 (0)	Suppost SMRAM Mapping. 0 : Disable. 1 : Enable. This bit is used to disable or enable SMRAM Mapping.

The following is M1521 address remapping table for SMRAM mapping enable.

Bit 3-2-1	SMI ACTJ	CPU Logical Address	Remapped Physical Address	Access DRAM Y/N
000	0	D0000	B0000	Y
000	1	D0000	non-local	N
001	X	D0000	B0000	Y
010	0	A0000/ B0000	A0000/ B0000	Y
010	1	A0000/ B0000	non-local	N
011	X	A0000/ B0000	A0000/ B0000	Y
100	0	30000	B0000	Y
100	1	30000	30000	Y
101	X	30000	B0000	Y

Register Name : ECCP - ECC/Parity Feature
Register Index : 49h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number **Bit Function**

7(0) Reserved.

6(0) SERRJ Duration.
0 : SERRJ will be asserted for 1 PCICLK.
1 : SERRJ will be asserted until All The ECC(parity) Error Flags Cleared.
When the M1521 detects a ECC or parity error, the M1521 will assert a SERRJ for 1 PCICLK(pulse mode) if this bit is set to '0'. Otherwise, the M1521 will assert the SERRJ to report the memory error until all the ECC/parity error flags are cleared (level mode).

5 (0) SERRJ on Parity or Multiple-bit ECC Error.
0 : Disable
1 : Enable.
When this bit is set to '0', the memory parity or multiple-bit error occurred will not assert the SERRJ signal. Otherwise, the memory data error will be reported to the system via SERRJ active signal.

4(0) SERRJ on Single-bit ECC Error.
0 : Disable.
1 : Enable.
When this bit is set to '0', the M1521 will not assert SERRJ on single-bit errors. Otherwise, the M1521 asserts SERRJ when it detects a single-bit ECC error.

3-2(0h) reserved.

1(0) ECC/Parity Test Mode Enable.
0 : Disable.
1 : Enable.

When this bit is set to '1', the ECC check bits or parity bits will be forced to the value defined in register index 4Bh during all the DRAM write cycles. Otherwise, the ECC check bits or parity bits normal function will be performed. This bit must be set to '0' for normal operation.

0(0) DRAM Data Integrity Mode.
0 : Parity.
1 : ECC.
When this bit is set to '0', the DRAM data integrity will be implemented by the parity algorithm. Otherwise, the ECC data integrity will be implemented.

Register Name : ECCE - ECC or Parity Error Status
Register Index : 4Ah
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-5(0h)	Multiple-bit or Parity First Row error. These 3 bits record the first row associated with the multiple-bit or parity error. When an error is detected, these bits are updated and ECCE[4] is set.
4(0)	Multiple-bit ECC Error or Parity Error Flag. The M1521 sets this bit to 1 when either a multiple-bit error or parity error has occurred, depending on whether ECC or parity is enabled, respectively. A write of 1 by software to ECCE[4] will clear it and write of 0 has no effect on it.
3-1 (0h)	Single-bit First Row Error. These 3 bits record the first row associated with the single-bit error. When an error is detected, these bits are updated and ECCE[0] is set.
0 (0)	Single-bit ECC Error Flag. The M1521 sets this bit to 1 when a single-bit ECC error has occurred and if ECC function is enabled. A write of 1 by software to ECCE[0] will clear it and write of 0 has no effect on it.

Register Name ECCT - ECC/Parity CHK/PDbits Setting in test Mode
Register Index : **4Bh**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Check-bit/Parity bit forced value in test mode. When ECCP[1] is set to 1, the parity (or ECC check) bits drive on MPD[7:0] during DRAM write cycles will be forced to ECCT[7:0].

Register Name : SHADRI - SHADOW Regions Read Enable - 1
Register Index : 4Ch
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	DC000h-DFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, DC000h-DFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
6 (0)	D8000h-DBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, D8000h-DBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
5(0)	D4000h-D7FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, D4000h-D7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
4 (0)	D0000h-D3FFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, D0000h-D3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
3(0)	CC000h-CFFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, CC000h-CFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.
2(0)	C8000h-CBFFFh Shadow Region Read Enable. 0 : Disable. 1 : Enable. When this bit is enabled, C8000h-CBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

1(0) C4000h-C7FFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable.
When this bit is enabled, C4000h-C7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

0(0) C0000h-C3FFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable.
When this bit is enabled, C0000h-C3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Name: SHADRII - SHADOW Regions Read Enable - 2
Register Index : 4Dh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number **Bit Function**

7(0) FC000h-FFFFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable
When this bit is enabled, FC000h-FFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

6(0) F8000h-FBFFFh Shadow Region Read Enable.
0 : Disable
1 : Enable.
When this bit is enabled, F8000h-FBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

5(0) F4000h-F7FFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable.
When this bit is enabled, F4000h-F7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

4(0) F0000h-F3FFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable.
When this bit is enabled, F0000h-F3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

3(0) EC000h-EFFFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable.
When this bit is enabled, EC000h-EFFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

2(0) E8000h-EBFFFh Shadow Region Read Enable
0 : Disable.
1 : Enable.
When this bit is enabled, E8000h-EBFFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

1(0) E4000h-E7FFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, E4000h-E7FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

0 (0) E0000h-E3FFFh Shadow Region Read Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, E0000h-E3FFFh memory read cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Name : SHADWI - SHADOW Regions Write Enable - 1
Register Index : 4Eh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number **Bit Function**

7(0) DC000h-DFFFFh Shadow Region Write Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, DC000h-DFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

6 (0) D8000h-DBFFFh Shadow Region Write Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, D8000h-DBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

5 (0) D4000h-D7FFFh Shadow Region Write Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, D4000h-D7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

4 (0) D0000h-D3FFFh Shadow Region Write Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, D0000h-D3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

3(0) CC000h-CFFFFh Shadow Region Write Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, CC000h-CFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

2(0) C8000h-CBFFFh Shadow Region Write Enable
0 : Disable.
1 : Enable.

When this bit is enabled, C8000h-CBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

1(0) C4000h-C7FFFh Shadow Region Write Enable.
0 : Disable.
1 : Enable.

When this bit is enabled, C4000h-C7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

0(0) C0000h-C3FFFh Shadow Region Write Enable.
0 : Disable.
1 : Enable.

When the above bits are enabled, the corresponding memory write cycle region will access local DRAM. Otherwise, it will pass through PCI bus.

Register Name : SHADWII - SHADOW Regions Write Enable - 2
Register Index : 4Fh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	FC000h-FFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, FC000h-FFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

6(0)	F8000h-FBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, F8000h-FBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

5 (0)	F4000h-F7FFFh Shadow Region Write Enable 0 : Disable. 1 : Enable.

When this bit is enabled, F4000h-F7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

4 (0)	F0000h-F3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, F0000h-F3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

3(0)	EC000h-EFFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, EC000h-EFFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

2(0)	E8000h-EBFFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, E8000h-EBFFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

1(0)	E4000h-E7FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, E4000h-E7FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

0(0)	E0000h-E3FFFh Shadow Region Write Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, E0000h-E3FFFh memory write cycle will access local DRAM. Otherwise, it will pass through PCI bus.

Register Name : SHADCI - SHADOW Regions Cacheable Enable - 1
Register Index : 50h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	DC000h-DFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, DC000h-DFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.

6(0)	D8000h-DBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, D8000h-DBFFFh memory access will become cacheable. Otherwise, it will be non cacheable.

5(0)	D4000h-D7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, D4000h-D7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

4(0)	D0000h-D3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, D0000h-D3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

3(0)	CC000h-CFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, CC000h-CFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.

2 (0)	C8000h-CBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, C8000h-CBFFFh memory access will become cacheable. Otherwise, it will be non cacheable.

1(0)	C4000h-C7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable

When this bit is enabled, C4000h-C7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

0 (0)	C0000h-C3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, C0000h-C3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

Register Name : SHADCII - SHADOW Regions Cacheable Enable - 2
Register Index : 51h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	FC000h-FFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, FC000h-FFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.

6(0)	F8000h-FBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable

When this bit is enabled, F8000h-FBFFFh memory access will become cacheable. Otherwise, it will be non cacheable

5 (0)	F4000h-F7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, F4000h-F7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

4 (0)	F0000h-F3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, F0000h-F3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

3(0)	EC000h-EFFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, EC000h-EFFFFh memory access will become cacheable. Otherwise, it will be non cacheable.

2 (0)	E8000h-EBFFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, E8000h-EBFFFh memory access will become cacheable. Otherwise, it will be non cacheable.

1(0)	E4000h-E7FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, E4000h-E7FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

0(0)	E0000h-E3FFFh Shadow Region Cacheable Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, E0000h-E3FFFh memory access will become cacheable. Otherwise, it will be non cacheable.

Register Name : MISII - Miscellaneous - 2
Register Index : 52h
Default Value : F0h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-3(00)	SRAM Module Presence Detect Bits HA[31:27] (Read Only). The M1521 will strobe HA[31:27] values and write them into the four-bit register during reset. BIOS can use these five bits to determine the SRAM module configuration and program the L2 size and type.
2-1(0)	reserved.
0(0)	PCI/CPU Concurrency Enable. 0 : Disable. 1 : Enable.

When this bit is enabled, CPU to L2 access will be concurrent with PCI-to-DRAM access. Otherwise, PCI to DRAM access will always prevent the CPU from issuing cycles by asserting AHOLD.

Register Name : reserved
Register Index : 53h
Default Value : 00h
Attribute : Read Only
Size : 8 bits

Register Name : FBMR - PCI Programmable Frame Buffer Memory Region
Register Index : 55h-54h
Default Value : FFFFh
Attribute : Read/Write
Size : 16 bits

Bit Number	Bit Function
15-4(000)	Starting address of Programmable Frame Buffer. The 12 Bits correspond to A[31:20] of the starting address. The remaining bits A[19:0] are assumed to be zero. These bits can combine with bits 3-0 to determine the Frame Buffer starting address and stopping address. When Index-56h bit 0 is set to '1', the M1521 will decode the boundary and enable CPU to PCI write buffer.
3-0(0)	Size of Programmable Frame Buffer. X000 : 1 MBytes. X001 : 2 Mbytes X010 : 4 Mbytes. X011 : 8 Mbytes. X100 : 16 Mbytes. Others : Reserved. These bits are used to program the Frame Buffer Size.

Note : The Frame Buffer Region should not overlap with local memory.

Register Name : H2PW - CPU to PCI Write Buffer Option
Register Index : 56h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7 (0)	H2PW Buffered Cycle Selection. 0 : Only CPU Memory Write to PCI Frame Buffer. 1 : All CPU to PCI Memory Write Cycle. If this bit is enabled, all non-local memory cycle will enable the CPU to PCI write buffer. Otherwise, only programmable Frame Buffer or fixed A/B segment Frame Buffer will use CPU to PCI write buffer.
6(0)	Linear-merge for Frame Buffer Cycle. 0 : Disable. 1 : Enable. When this bit is enabled, only the consecutive linear addresses can be merged.
5 (0)	Word-merge for Frame Buffer Cycle. 0 : Disable. 1 : Enable. This bit is used to enable the word-merge feature for Frame Buffer cycle. The M1521 will check the CPU HBEJ[7:0] and determine if they can be merged or not.
4(0)	Byte-merge for Frame Buffer Cycle. 0 : Disable. 1 : Enable. This bit is used to enable the byte-merge feature for Frame Buffer cycle. The M1521 will check the CPU HBEJ[7:0] and determine if they can be merged or not.
3(0)	Use PCI Fast Back-to-Back. 0 : Disable. 1 : Enable This bit is used to enable PCI Fast Back-to-Back capability. If this bit is enabled, consecutive PCI write cycles targeted to the same slave will become fast back-to-back on the PCI bus.
2 (0)	Use PCI Write-Burst. 0 : Disable. 1 : Enable. This bit is used to enable PCI write burst capability. If this bit is enabled, consecutive PCI write cycles will become burst cycle on the PCI bus.

1(0) VGA 0A0000-0BFFFF Fixed Frame Buffer.
0 : Disable.
1 : Enable.
This bit is used to enable 0A0000h-0BFFFFh Frame Buffer and CPU to PCI write buffer.

0 (0) Programmable Frame Buffer.
0 : Disable.
1 : Enable.
This bit is used to combine with index 55h-54h to enable the PCI Frame Buffer and CPU to PCI write buffer.

Register Name : H2PO - CPU to PCI Option
Register Index : **57h**
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number **Bit Function**

7(0) PCI Signals Float Delay Control.
0 : Disable.
1 : Enable, + 1/2 CPU Clock.
When this bit is enabled, the M1521 will delay the PCI bus signal transition for 1/2 CPU clock to increase PCI bus hold time.

6(0) APIC support, invalidate P2HR buffer when PHLDAJ goes low.
0 : enable
1 : disable
When APIC is supported in Dual processor system, this bit must be reset to '0' to invalidate P2HR buffer since the M1521 cannot realize Interrupt Synchronous event. But in single processor systems, the M1521 can detect Interrupt Synchronous event to invalidate P2HR Buffer automa-tically. This bit is recommended to be set to '1' in single processor systems.

5 (0) Translate CPU Shutdown cycle to Port 92 cycle.
0 : Enable.
1 : Disable.
When this bit is reset to '0', the M1521 will forward a Shut-down special cycle from CPU bus to PCI bus. When this bit is set to '1', the M1521 will write 01h to I/O address port 92 on PCI bus.

4(0) Short data output period for CPU read PCI.
0 : Disable, Drive Output Data for 2 CPU Clocks.
1 : Enable, Drive Output Data for 1 CPU Clock.
When this bit is enabled, the M1521 will assert BRDYJ immediately after it strobes the PCI read TRDYJ. Otherwise, it will delay a CPU Clock to add data propagation time to the CPU.

3-0 (0h) Reserved.

Register Name : P2HO - PCI to Main Memory / PCI Arbiter Option
Register Index : 58h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-3 (00h)	Reserved.
2(0)	CPU Access PCI During Passive Release 0 : Disable. 1 : Enable. This bit controls CPU to PCI access during passive release. When it is enabled, CPU to PCI access is allowed during passive release. Otherwise, arbiter only accepts another PCI master access to local DRAM.
1(0)	Passive Release of PHOLD. 0 : Disable. 1 : Enable. When this bit is enabled, the M1521 will recognize passive release signaled by M1523. The M1521 will rearbitrate PCI and possibly allow the CPU to access PCI depending on Bit 2 value. When this bit is disabled, the M1521 does not recognize passive release, i.e. PHLDAJ continues to be asserted. PHOLDJ must be deasserted for two consecutive PCI clocks signaling an active release before PHLDAJ will be deasserted. A value '1' is recommended for normal operation.
0(0)	reserved.

Register Name : PCIA - PCI Arbiter Time Slice
Register Index : 59h
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Number of PCI clocks for PCI Bus time slice. The Time-Slice will guarantee the minimum clocks that the PCI master is granted the ownership of PCI bus. The time-slice counter is started when PCI grant is asserted and bus is idle. The Bits 1-0 are assumed to be "00" and are ignored.

Register Name : CPUA - CPU Arbiter Time Slice
Register Index : 5Ah
Default Value : 20h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	No. of PCI clocks for CPU Bus time slice. The Time-Slice will guarantee the minimum clocks that the CPU master is granted the ownership of PCI bus. The time-slice counter is started when CPU grant is asserted and bus is idle. The Bits 1-0 are assumed to be "00" and are ignored.

Register Name : PCIRC - PCI Retry control for P2H cycle
Register Index : 5Bh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-4(0h)	Reserved.
3-2(00)	Retry Latency for Second Data Phase Control. 00 : Retry on Second Data phase if wait state > 8 PCI clocks. 01 : Retry on Second Data phase if wait state > 4 PCI clocks. 10 : Retry on Second Data phase if wait state > 2 PCI clocks. 11 : Never Retry on Second Data phase. These bits are used to retry a PCI master cycle when the latency to the second data is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1521 will complete the second data transfer regardless of latency.
1-0(00)	Retry Latency for First Data Phase Control. 00 : Retry on first Data phase if wait state > 32 PCI clocks. 01 : Retry on first Data phase if wait state > 16 PCI clocks. 10 : Retry on first Data phase if wait state > 8 PCI clocks. 11 : Never Retry on first Data phase. These bits are used to retry a PCI master cycle when the latency to the first data is about to exceed the programmed number of PCI clocks. When these bits are set to '11', the M1521 will complete the first data transfer regardless of latency.

Register Name : SDRAMCI - Synchronous DRAM Control Register I
Register Index : 5Ch
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-5(0h)	SDRAM Operation Mode Selection. 000 : Normal Operation(Default). 001 : NOP(No Operation) Command Enable. 010 : PALL(Precharge All Banks) Command Enable. 011 : MRS(Mode Register Set) Command Enable. 100 : CBR(CAS Before RAS Refresh) Enable. Others : reserved.

Note: (1) Before switching from one mode of SDRAM to another, the BIOS should ensure the DRAM buffer is empty. For example, by issuing a DRAM read cycle to flush the DRAM buffer. (2) In the MRS mode, the MA is translated as the column address and the BIOS should issue the appropriate CPU addresses to program the SDRAMs. NOP mode is used to force all CPU cycles to DRAM to generate an SDRAM NOP command on the memory interface. PALL mode is used to force all CPU cycles to DRAM to generate an SDRAM precharge all banks command on the memory interface. MRS command is used to convert all CPU cycles to commands on the memory interface. MA[11:0] lines are used to drive command: MA[2:0]=010 for burst of 4 mode, MA[3]=1/0 for interleave/linear wrap mode, MA[4]=the value of CAS Latency(bit4), MA[6:5]=01 and MA[11:7]=00000. All these modes are used to initialize SDRAM. Please refer to the hardware and software setup section.

4(0) CAS Latency.
0 : 3 HCLKIN's.
1 : 2 HCLKIN's.
This bit is used to control read data valid wait states after read command has been issued. '0' means the CAS Latency is 3 HCLKINs, and 1 means the CAS Latency is 2 HCLKINs.

3(0) RAS Active to Read/Write Command Delay Time(tRCD).
0 : 3 HCLKIN's.
1 : 2 HCLKIN's.
This bit is used to control RASJ to CASJ delay. The same programmed value as bit 4 is highly recommended for normal operation.

2-1(0h) RAS Precharge Timing (in HCLKIN's). RAS Precharge Time(tRP) / RAS Active to Refresh/RAS-Active to Precharge Time(tRAS) / Refresh/RAS-Active Time(tRC)

00 : 4	6	10
01 : 4	5	9
10 : 3	4	7

11 : Reserved.
These two bits are used to control RAS precharge time, RAS active to precharge time, refresh to RAS active, refresh to refresh, RASJ active to refresh, and RASJ active to RASJ active time.

0(0) Selection of RASJ[7]/SRASJ[0] and RASJ[6]/SCASJ[0].
0 : RASJ[7] and RASJ[6].
1 : SRASJ[0] and SCASJ[0]. When SDRAM is populated, a '1' is selected. When 8 banks of DRAMs are selected, a '0' is selected.

Register Name : SDRAMCII - Synchronous DRAM Control Register II
Register Index : 5Dh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-2(00h)	Reserved.
1(0)	Power-down Mode(Self Refresh) Enable. 0 : Disable 1 : Enable

When this is set to '1', RASJ[5:4] will become as CLKEN[1:0] to support SDRAM self refresh mode for Notebook applications. In desktop applications, 0 is recommended for normal operation, and RASJ[5:4] are RASJ[5:4].

0(0) JEDEC "2n rule" Restricted.
0 : Yes.
1 : No. (The Interval Between Two Commands Not Limited to Be Even-numbered.) This bit is used to support TI 2n rule SDRAM, the interval between two commands has to be limited to even-numbers.

Register Name : Reserved
Register Index : 5Eh
Default Value : 00h
Attribute : Read Only
Size : 8 bits

Register Name : DRAMHP - DRAM Configuration of Half-Populated Banks
Register Index : 5Fh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	Reserved.
5(0)	Which Half of Row5 (RAS5J) Is Populated 0 : Lower Dword. 1 : Higher Dword.
4 (0)	Which Half of Row4 (RAS4J) Is Populated. 0 : Lower Dword. 1 : Higher Dword.
3 (0)	Which Half of Row3 (RAS3J) Is Populated. 0 : Lower DWord. 1 : Higher Dword.
2(0)	Which Half of Row2 (RAS2J) Is Populated. 0 : Lower Dword. 1 : Higher Dword.
1(0)	Which Half of Row1 (RAS1J) Is Populated. 0 : Lower Dword. 1 : Higher Dword.
0(0)	Which Half of Row0 (RAS0J) Is Populated. 0 : Lower DWord. 1 : Higher Dword.

Note: This bit is valid only if offset x43 bit7 = 1. This bit is used to control Row5 High/Low Dword data swap.

Note: This bit is valid only if offset x43 bit6 = 1. This bit is used to control Row4 High/Low Dword data swap.

Note : This bit is valid only if offset x43 bit5 = 1. This bit is used to control Row3 High/Low Dword data swap.

Note: This bit is valid only if offset x43 bit4 = 1. This bit is used to control Row2 High/Low Dword data swap.

Note: This bit is valid only if offset x43 bit3 = 1. This bit is used to control Row1 High/Low Dword data swap.

Note: This bit is valid only if offset x43 bit2 = 1. M1521 supports flexible 32 Bits access. This bit is used to control Row0 High/Low Dword data swap.

Register Name : DB0CI - DRAM Row0 Configuration -1
Register Index : 60h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row0 DRAM Top Address Boundary-1. A27-A20 Address Boundary.

Register Name : DB0CII - DRAM Row0 Configuration-2
Register Index : 61h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row0 DRAM Disable. 01 : Row0 DRAM Use standard MA Mapping. 10 : Row0 DRAM Use 64M technology MA Mapping. 11 : Row0 DRAM Use 1Mx16 MA Mapping.

These two bits are used to program the DRAM MA used on DRAM Row 0. Please refer to the DRAM MA translation table.

5-4(0h)	Row0 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Sync. DRAM.

These two bits are used to program the DRAM type used on DRAM Row 0.

3-0(0h)	Row0 DRAM Top Address Boundary-2. A31-A28 Address Boundary.

These four bits are used to combine index-60h to decide the top memory size for DRAM Row 0.

The following types of DRAMs are supported when Bits [7-6] = '01'.

Memory Org	Memory Size	Row Address	Column Address
512Kx8	4Mb	10	9
1Mx4	4Mb	10	10
1Mx16	16Mb	10	10
2Mx8	16Mb	11	10
4Mx4	16Mb	11	11
4Mx4	16Mb	12	10

The following types of DRAMs are supported when Bits [7-6] = '10'.

Memory Org	Memory Size	Row Address	Column Address
4Mx16	64Mb	11	11
8Mx8	64Mb	12	11
16Mx4	64Mb	12	12

The following types of DRAMs are supported when Bits [7-6] = '11'.

Memory Org	Memory Size	Row Address	Column Address
1Mx16	16Mb	12	8

The M1521 supports 8 rows of DRAM, and each of them can be 32-bit or 64-bit wide. DRAM Rowx Configuration register defines populated DRAM type and Top Address Boundary for each row. DB0CI and DB0CII define for Row 0, DB1CI and DB1CII define for Row 1, DB2CI and DB2CII define for Row 2, DB3CI and DB3CII define for Row 3, DB4CI and DB4CII define for Row 4, DB5CI and DB5CII define for Row 5, B6CI and DB6CII define for Row 6, and DB7CI and DB7CII define for Row 7. Contents of these 8-bit registers represent the boundary address in 1MB granularity and DRAM type populated.

DB0CII[3:0]&DB0CI[7:0] = Total amount of memory in row 0 (in 1MB)

DB0CII[5:4] define different DRAM Type for row 0.
DB0CII[7:6] define different MA Type or unpopulated for row 0.
DB1CII[3:0]&DB1CI[7:0] = Total amount of memory in row 0 + row 1 (in 1MB)

DB1CII[5:4] define different DRAM Type for row 1.

DB1CII[7:6] define different MA Type or unpopulated for row 1.

DB2CII[3:0]&DB2CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 (in 1MB)

DB2CII[5:4] define different DRAM Type for row 2.

DB2CII[7:6] define different MA Type or unpopulated for row 2.

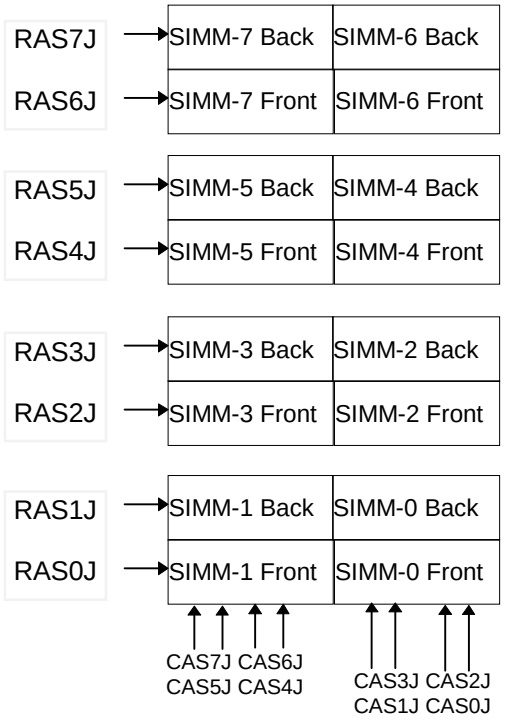
DB3CII[3:0]&DB3CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 (in 1MB)

DB3CII[5:4] define different DRAM Type for row 3.
DB3CII[7:6] define different MA Type or unpopulated for row 3.

DB4CII[3:0]&DB4CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 (in 1MB)

DB4CII[5:4] define different DRAM Type for row 4.
DB4CII[7:6] define different MA Type or unpopulated for row 4.
DB5CII[3:0]&DB5CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 (in 1MB)
DB5CII[5:4] define different DRAM Type for row 5.
DB5CII[7:6] define different MA Type or unpopulated for row 5.
DB6CII[3:0]&DB6CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 (in 1MB)
DB6CII[5:4] define different DRAM Type for row 6.
DB6CII[7:6] define different MA Type or unpopulated for row 6.
DB7CII[3:0]&DB7CI[7:0] = Total amount of memory in row 0 + row 1 + row 2 + row 3 + row 4 + row 5 + row 6 + row 7 (in 1MB)
DB7CII[5:4] define different DRAM Type for row 7.
DB7CII[7:6] define different MA Type or unpopulated for row 7.

As an example of a system configuration where 8 physical rows are configured for either single-sided or double-sided SIMMs, the DRAM will be configured like the following Figure.



In this configuration, the M1521 will drive two RASJ lines to the SIMM row. If the single-sided SIMMs are populated, the even RASJ is used and the odd RASJ is not used. If the double-sided SIMMs are populated, both RASJ lines are used.

Example A
Two single-sided 1MB X 32 FPM DRAMs (standard MA mapping) are populated at row 0, a total of 8 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 08h DB0CII = 40h
DB1CI = 08h DB1CII = 00h
DB2CI = 08h DB2CII = 00h
DB3CI = 08h DB3CII = 00h
DB4CI = 08h DB4CII = 00h
DB5CI = 08h DB5CII = 00h
DB6CI = 08h DB6CII = 00h
DB7CI = 08h DB7CII = 00h

Example B
Four single-sided 1MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 0 and row 2, a total of 16 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 08h DB0CII = D0h
DB1CI = 08h DB1CII = 00h
DB2CI = 10h DB2CII = D0h
DB3CI = 10h DB3CII = 00h
DB4CI = 10h DB4CII = 00h
DB5CI = 10h DB5CII = 00h
DB6CI = 10h DB6CII = 00h
DB7CI = 10h DB7CII = 00h

Example C
Two double-sided 2MB X 32 FPM DRAMs (standard MA mapping) are populated on row 4 , row 5, row 6, and row 7, a total of 32 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 00h DB0CII = 00h
DB1CI = 00h DB1CII = 00h
DB2CI = 00h DB2CII = 00h
DB3CI = 00h DB3CII = 00h
DB4CI = 08h DB4CII = 40h
DB5CI = 10h DB5CII = 40h
DB6CI = 18h DB6CII = 40h
DB7CI = 20h DB7CII = 40h

Example D
One double-sided 2MB X 32 EDO DRAMs (1Mx16 MA mapping) are populated on row 2 and row 3, and one double-sided 8MB X 32 FPM DRAMs (64Mb MA mapping) are populated on row 6 and row 7, a total of 80 MB of DRAM. The DBxCI and DBxCII registers should be programmed as follows:

DB0CI = 00h DB0CII = 00h
DB1CI = 00h DB1CII = 00h
DB2CI = 08h DB2CII = D0h
DB3CI = 10h DB3CII = D0h
DB4CI = 10h DB4CII = 00h
DB5CI = 10h DB5CII = 00h
DB6CI = 30h DB6CII = 80h
DB7CI = 50h DB7CII = 80h

Register Name : DB1CI - DRAM Row1 Configuration -1
Register Index : 62h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	**Bit Function**
7-0(00h)	Row1 DRAM Top Address Boundary-1. A27-A20 Address Boundary.

Register Name : DB1CII - DRAM Row1 Configuration-2
Register Index : 63h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6(0h)	DRAM MA Definition. 00 : Row1 DRAM Disable. 01 : Row1 DRAM uses standard MA Mapping. 10 : Row1 DRAM Use 64M technology MA Mapping. 11 : Row1 DRAM Use 1Mx16 MA Mapping. These two bits are used to program the DRAM MA used on DRAM Row 1. Please refer to the DRAM MA translation table.
5-4(0h)	Row1 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 1.
3-0(0h)	Row1 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide top memory size for DRAM Row1.

Register Name : DB2CI - DRAM Row2 Configuration-1
Register Index : 64h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row2 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Name : DB2CII - DRAM Row2 Configuration-2
Register Index : 65h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row2 DRAM Disable. 01 : Row2 DRAM Use standard MA Mapping. 10 : Row2 DRAM Use 64M technology MA Mapping. 11 : Row2 DRAM Use 1Mx16 MA Mapping. These two bits are used to program the DRAM MA used on DRAM Row 2. Please refer to the DRAM MA translation table
5-4(0h)	Row2 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 2.
3-0 (0h)	Row2 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide top memory size for DRAM Row2.

Register Name : DB3CI - DRAM Row3 Configuration-1
Register Index : 66h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row3 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Name : DB3CII - DRAM Row3 Configuration-2
Register Index : 67h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6(0h)	DRAM MA Definition. 00 : Row3 DRAM Disable. 01 : Row3 DRAM Use standard MA Mapping. 10 : Row3 DRAM Use 64M technology MA Mapping. 11 : Row3 DRAM Use 1Mx16 MA Mapping. These two bits are used to program the DRAM MA used on DRAM Row 3. Please refer to the DRAM MA translation table.
5-4(0h)	Row3 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 3.
3-0(0h)	Row3 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combined index-60h to decide top memory size for DRAM Row3.

Register Name : DB4CI - DRAM Row4 Configuration-1
Register Index : 68h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row4 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Name : DB4CII - DRAM Row4 Configuration-2
Register Index : 69h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row4 DRAM Disable. 01 : Row4 DRAM Use standard MA Mapping. 10 : Row4 DRAM Use 64M technology MA Mapping. 11 : Row4 DRAM Use 1Mx16 MA Mapping. These two bits are used to program the DRAM MA used on DRAM Row 4. Please refer to the DRAM MA translation table.
5-4(0h)	Row4 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 4.
3-0(0h)	Row4 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combined index-60h to decide top memory size for DRAM Row4.

Register Name : DB5CI - DRAM Row5 Configuration-1
Register Index : 6Ah
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row5 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Name : DB5CII - DRAM Row0 Configuration-2
Register Index : 6Bh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row5 DRAM Disable. 01 : Row5 DRAM Use standard MA Mapping. 10 : Row5 DRAM Use 64M technology MA Mapping. 11 : Row5 DRAM Use 1Mx16 MA Mapping. These two bits are used to program the DRAM MA used on DRAM Row 5. Please refer to the DRAM MA translation table.
5-4(0h)	Row5 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 5.
3-0(0h)	Row5 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combined index-60h to decide top memory size for DRAM Row5.

Register Name : DB6CI - DRAM Row6 Configuration-1
Register Index : 6Ch
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	Row6 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Name : DB6CII - DRAM Row6 Configuration-2
Register Index : 6Dh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6(0h)	DRAM MA Definition. 00 : Row6 DRAM Disable. 01 : Row6 DRAM Use standard MA Mapping. 10 : Row6 DRAM Use 64M technology MA Mapping. 11 : Row6 DRAM Use 1Mx16 MA Mapping. These two bits are used to program the DRAM MA used on DRAM Row 6. Please refer to the DRAM MA translation table.
5-4(0h)	Row6 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 6.
3-0 (0h)	Row6 DRAM Top Address Boundary-2. A31-A28 Address Boundary. These four bits are used to combined index-60h to decide top memory size for DRAM Row6.

Register Name : DB7CI - DRAM Row7 Configuration-1
Register Index : 6Eh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0 (00h)	Row7 DRAM Top Address Boundary - 1. A27-A20 Address Boundary.

Register Name : DB7CII - DRAM Row7 Configuration-2
Register Index : 6Fh
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	DRAM MA Definition. 00 : Row7 DRAM Disable. 01 : Row7 DRAM Use standard MA Mapping. 10 : Row7 DRAM Use 64M technology MA Mapping. 11 : Row7 DRAM Use 1Mx16 MA Mapping. These two bits are used to program the DRAM MA used on DRAM Row 7. Please refer to the DRAM MA translation table.
5-4(0h)	Row7 DRAM Type. 00 : Standard Fast-page Mode DRAM. 01 : EDO DRAM. 10 : Burst EDO DRAM. 11 : Synchronous DRAM. These two bits are used to program the DRAM type used on DRAM Row 7.
3-0(0h)	Row7 DRAM Top Address Boundary - 2. A31-A28 Address Boundary. These four bits are used to combine index-60h to decide top memory size for DRAM Row7.

Register Name : UMAI - UMA Function - 1
Register Index : 70h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-0(00h)	SFB Aliasing Starting Address - 1. A27-A20 Address Boundary. These 8 bits define the Shared Frame Buffer (SFB) region start address boundary A27-A20 which can be directly accessed by the host memory controller. This defined address region is meaningful only when the Index-71h bit 4 is set to '1'.

Register Name : UMAII - UMA Function - 2
Register Index : 71h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	System Preempt in Refresh Timeout Pending over 2 us. 0 : Disable. 1 : Enable. When this bit is set to '1', a refresh timeout pending over 2 us event will preempt the graphics controller from the DRAM bus. Otherwise, the refresh timeout event will not perform the preemption. The minimal MGNTJ (grantj) active time is 3 HCLK before preemption.
6(0)	System Preempt in PCI Bus Pending for DRAM Access. 0 : Disable. 1 : Enable. When this bit is set to '1', a PCI bus pending for DRAM access event will preempt the graphics controller from the DRAM bus. Otherwise, the PCI bus pending event will not perform the preemption. The minimal MGNTJ(grantj) active time is 3 HCLK before preempt ion.
5(0)	System Preempt in CPU Bus Pending for DRAM Access. 0 : Disable. 1 : Enable. When this bit is set to '1', a CPU bus pending for DRAM access event will preempt the graphics controller from the DRAM bus. Otherwise, the CPU bus pending event will not perform the preemption. The minimal MGNTJ (grantj) active time is 3 HCLK before preemption.
4(0)	SFB Aliasing Feature. 0 : Disable. 1 : Enable. When this bit is set to '1', the CPU can access the SFB via the host memory controller. These access cycles will not pass through a slower PCI bus. This SFB region address can be different from the graphics controller PCI region. The M1521 host memory controller only recognizes the SFB aliasing defined region to directly access the SFB memory. This region cannot be defined to overlap with the system memory region (but, it can be adjacent to the top of system memory address). The SFB aliasing address region is not cacheable for the L1 and L2. For the SFB data consistency in the host controller and PCI bus view, a dummy SFB aliasing Read cycle needs to be added for flushing the host memory write buffers. And, this dummy read cycle address location should be the same as the latest SFB write access cycle. The SFB aliasing feature will be disabled when this bit is set to '0'.

3-0 (0h)	SFB Aliasing starting address - 2. A31-A28 Address Boundary. These 4 bits define the Shared Frame Buffer (SFB) region start address boundary A31-A28 which can be directly accessed by the host memory controller. This defined address region is meaningful only when the Index-71h bit 4 is set to '1'.

Register Name : UMAIII - UMA Function - 3
Register Index : 72h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	**Bit Function**
7(0)	Reserved.
6-4 (0h)	SFB size. 000 : 512K. 001 : 1M. 010 : 2M. 011 : 3M. 100 : 4M. Others : reserved.

These 3 bits define the SFB memory size.

Note : Because of the occupation of the SFB memory, the DRAM bank (row) boundary should be recalculated and reprogrammed by the BIOS programmer. The programming procedure is described as below :

1. Start : UMA feature disable
2. DRAM sizing for each bank (without UMA) and pro gramming DRAM size to Index 60h-6Fh.
3. System(Board) makers decide the UMA populated bank. And, BIOS programmers set proper value to Index 75h.
4. System makers or users decide the SFB memory size. And, BIOS programmers set proper value to Index 72h Bit6-4.
5. BIOS programmers re-calculate the DRAM boundary value for each bank by substracting the SFB DRAM size (the SFB size subtrahend value) and re-program the corrected system memory boundary value to Index 60h-6Fh. (i.e. the DRAM boundary value of all the banks after the UMA bank should substract the SFB size- subtrahend value.)

SFB size	Subtrahend
512K	1M(The boundary should substract 1M when the SFB size is 512K. The M1521 will automatically compensate 512K size to the system memory)
1M	1M
2M	2M
3M	3M
4M	4M

6. Sub-program exit.

Example A	For a SFB size of 1M (populated in Row0) in an 8M/ Row0 and 8M/Row1 system, the new corrected DRAM boundary value is 7M in Row0, 15M in Row1, and 15M in all other rows.
Example B	For a SFB size of 512K (populated in Row0) in an 8M/bank0 and 8M/bank1 system, the new corrected DRAM boundary value is 7M in Row0, 15M in Row1 and 15M in all other banks.
Example C	For a SFB size of 2M (populated in Row0) in a 16M/bank0 and 8M/bank1 system, the new corrected DRAM boundary value is 14M in Row0, 22M in bank1, and 22M in all other banks.
Example D	For a SFB size of 1M (populated in Row0) in a 32M/bank0 system, the new corrected DRAM boundary value is 31M in Row0, and 31M in all other banks.
Example E	For an SFB size of 1M (populated in Row1) in a 8M/bank0, 8M/bank1 system, the new corrected DRAM boundary value is 8M in Row0, and 15M in Row1, and 15M in all other banks.
Example F	For an SFB size of 1M (populated in Row2) in a 8M/bank0, 8M/bank1, 8M/bank2, and 8M/bank3 system , the new corrected DRAM boundary value is 8M in Row0, 16M in Row1, 23M in Row2, 31M in Row3, and 31M in all other banks.
Example G	For an SFB size of 1M (populated in Row2) in a 0M/bank0, 8M/bank1, 8M/bank2, and 8M/bank3 system, the new corrected DRAM boundary value is 0M in Row0, 8M in Row1, 15M in Row2, 23M in Row3, and 23M in all other banks.

3(0) UMA Protocol Synchronous Mode.
0 : Synchronous Mode.
1 : Asynchronous Mode.

When the Host memory controller (HMC) achieves arbitration with the graphics controller (GC) via a synchronous signal interfacing scheme, this bit should be set to '0'. Otherwise, this bit should be set to '1' in an asynchronous signal interfacing protocol system. When the system is running the HMC and GC interfacing asynchronous mode, an additional 2 host clock re-synchronization time is required to acquire and release the system memory bus to the GC.

2-1(00) UMA Protocol Definition
00 : 3 pin-1(requestj/grantj/priority, PRIORITY active high)
01 : 2 pin-1(REQUESTJ/GRANTJ, PRIORITY fixed at high)
10 : 2 pin-2(requestj/grantj, PRIORITY indicated by requestj)
11 : 3 pin-2(requestj/grantj/priority, PRIORITY active low)

These 2 bits define the UMA interfacing protocol.
00 : 3-pin protocol is supported. A third signal indicating the high priority is a high active one.
01 : 2-pin protocol is supported. The interfacing protocol (requestj/ grantj) timing spec. is same as 3 pins'. But, the eliminated signal priority logic is fixed to high priority recognition.
10 : 2 pins with high/ low priority protocol is supported. When the GC asserts MREQJ (requestj) to make a low priority request, it can raise MREQJ high for one clock cycle and re-assert MREQJ to make a high priority request.
11 : 3-pin protocol is supported. A third signal indicating the high priority is a low active one.

0(0) UMA Protocol and Feature.
0 : Disable.
1 : Enable.
When this bit is set to '0', all the UMA protocol handshaking signals, functions, and features will be disabled.

Register Name : UMAIV - UMA Function - 4
Register Index : 73h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-4(0h)	Reserved.

3-2(0) UMA DRAM Address Translation Mode Status (Read-only)
00 : Reserved.
01 : Standard Mapping.
10 : 64M Technology Mapping.
11 : 1Mx16 Mapping.
These 2 bits are described the translation of CPU address to SFB DRAM row and column address.

1-0 (00) UMA DRAM Type Status (Read-only).
00 : Fast Page mode.
01 : EDO DRAM.
10 : BEDO DRAM.
11 : Sync. DRAM.
These 2 bits are described the SFB DRAM type.

Register Name : UMALT - UMA Controller Latency Timer
Register Index : 74h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	The latency time after graphics request asserted when the current cycle is CPU DRAM read access cycle. 0 : 0 HCLK Latency. 1 : Same as Bit [5-3] Defined.

NOTE: If the time required to complete the current cycle is less than the latency timer, the current cycle will finish without being interrupted.

6 (0) Latency timer counter is disabled when DRAM current cycle is a 32-bit bank access cycle.
0 : Enable counter in 32-bit access cycle, but the latency time will be doubled.
1 : Disable the latency timer, i.e. the host DRAM arbiter will release the DRAM bus to the VGA as soon as possible when the VGA requests the DRAM bus.

5-3 (0h) DRAM bus release latency time after graphics request asserted in PCI read from DRAM. During the PCI read from DRAM period, the host DRAM controller will relinquish to DRAM bus when the DRAM buffer is full or this timer timeouts.

NOTE 1: If the time required to complete the current cycle is less than the latency timer, the current cycle will finish without being interrupted.

Bit [5-3]/ Latency(HCLK)		Bit [5-3]/ Latency(HCLK)	
000	0	100	16
001	4	101	20
010	8	110	24
011	12	111	28

NOTE 2: An on-going DRAM access (or refresh) cycle will not be broken when an active MREQJ is sampled. In this situation, the DRAM bus release latency time from the host controller is within 18 HCLKs.

2-0 (0h) DRAM bus release latency time after graphics request asserted in CPU/PCI Write to DRAM. During the CPU/PCI buffer write to DRAM period, the host DRAM controller will relinquish the DRAM bus when the DRAM buffer is empty or this timer timeout.

NOTE 1 : If the time required to complete the current cycle is less than the latency timer, the current cycle will finish without being interrupted.

Bit [2-0] /Latency(HCLK)		Bit [2-0]/ Latency(HCLK)	
000	0	100	16
001	4	101	20
010	8	110	24
011	12	111	28

NOTE 2 : An on-going DRAM access (or refresh) cycle will not be broken when an active MREQJ is sampled. In this situation , the DRAM bus release latency time from the host controller is within 18 HCLKs.

Register Name : UMAD - UMA DRAM Populated Row
Register Index : 75h
Default Value : 00h
Attribute : Read/Write
Size : 8 bits

Bit Number **Bit Function**

7-5 (0h) Reserved.

4(0) UMA REQJ and PRIO synchronized by 1 HCLK.
0 : Disable
1 : Enable.

This is a backup option for guaranteeing the MREQJ and PRIOrity adequate setup time to the M1521. When this feature is enabled (this bit is set to '1'), an additional 1 host clock re synchronization time is required to acquire and release the system memory bus to the GC.

3 (0h) Reserved

2-0 (0h) UMA DRAM Populated Row.
000 : Row 0 DRAM for UMA.
001 : Row 1 DRAM for UMA.
010 : Row 2 DRAM for UMA.
011 : Row 3 DRAM for UMA.
100 : Row 4 DRAM for UMA.
101 : Row 5 DRAM for UMA.
Others : Reserved.
These 3 bits define the UMA populated bank.

Register Name : POD - Programmable Output Driving Strength
Register Index: 76h
Default Value: 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7(0)	MWEJ Driving Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the MWEJ pins.
6 (0)	MAA[1:0]/MAB[1:0] Driving Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the MAA[1:0] and MAB[1:0] pins.
5 (0)	MA[11:2] Driving Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the MA[11:2] pins.
4(0)	CASJ[7:0] Driving Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the CASJ[7:0] pins.
3(0)	RASJ[5:0] Driving Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the RASJ[5:0] pins.
2(0)	RASJ[7:6]/SRASJ[1:0], SCASJ[1:0] Driving Select. 0 : 12 mA. 1 : 24 mA. This bit controls the strength of the output buffers driving the RASJ[7:6]/SRASJ[1:0], SCASJ[1:0] pins.
1(0)	MD[63:0] and MPD[7:0] Driving Select. 0 : 8 mA. 1 : 6 mA. This bit controls the strength of the output buffers driving the MD[63:0] and MPD[7:0] pins.
0(0)	HD[63:0] Driving Select. 0 : 8 mA. 1 : 6 mA. This bit controls the strength of the output buffers driving the HD[63:0] pins.

Register Name : SUSC - 5-V Suspend Control Register
Register Index: 77h
Default Value: 00h
Attribute : Read/Write
Size : 8 bits

Bit Number	Bit Function
7-6 (0h)	Reserved.
5(0h)	Host Local Memory Access Resume 5-V Suspend (Wakeup). 0 : Disable. 1 : Enable. When this bit is set to '1', the CPU local memory access event will wakeup the 5-V suspend refresh mode and keep on the normal DRAM access mode until the Index 77h D0 reset to '0'. When this bit is set to '0', only the Index 77h D0 reset to '0' can resume (or wakeup) the 5-V suspend refresh mode.
4 (0h)	DRAM Controller Status (Read-only). 0 : Normal DRAM. 1 : 5-V Suspend Refresh. This bit is the DRAM controller status bit for indicating the memory system is in normal DRAM access or 5-V suspend mode.
3(0h)	5-V Suspend Period MA Logic Value. 0 : Logic 0. 1 : Logic 1. When this bit is set to '0', all the MA logic value will stuck at 0 during the 5-V suspend period. When this bit is set to '1', all the MA logic value will be stuck to 1 during the 5-V suspend period.
2-1 (00)	5-V Suspend Refresh Period. 00 : 15 us. 01 : 30 us. 10 : 60 us. 11 : 120 us. These 2 bits define the 5-V suspend refresh period.
0(0)	5-V Suspend Refresh Enable. 0 : Normal DRAM Controller Operation. 1 : Suspend Refresh Owns DRAM Bus Enable. When this bit is set to '1', the M1521 will wait for a CPU clock stop grant cycle and then enter the 5-V DRAM suspend refresh mode. This bit should be reset to '0' before re-entering the next 5-V suspend refresh sequence. The M1521 pin - SUSPENDJ is meaningful only when this bit is 0 (or in 5-V suspend mode).

Register Name : reserved
Register Index: FFh-78h
Default Value : 00h
Attribute : Read/Write

Section 5 : Hardware and Software Programming Guide

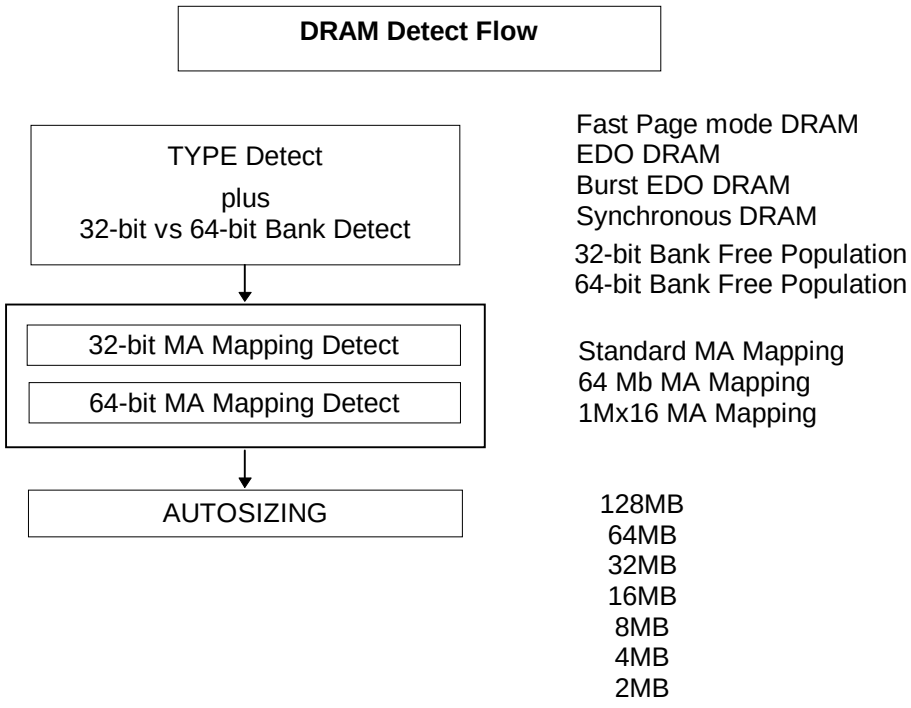


Figure 1. DRAM Detect Flow

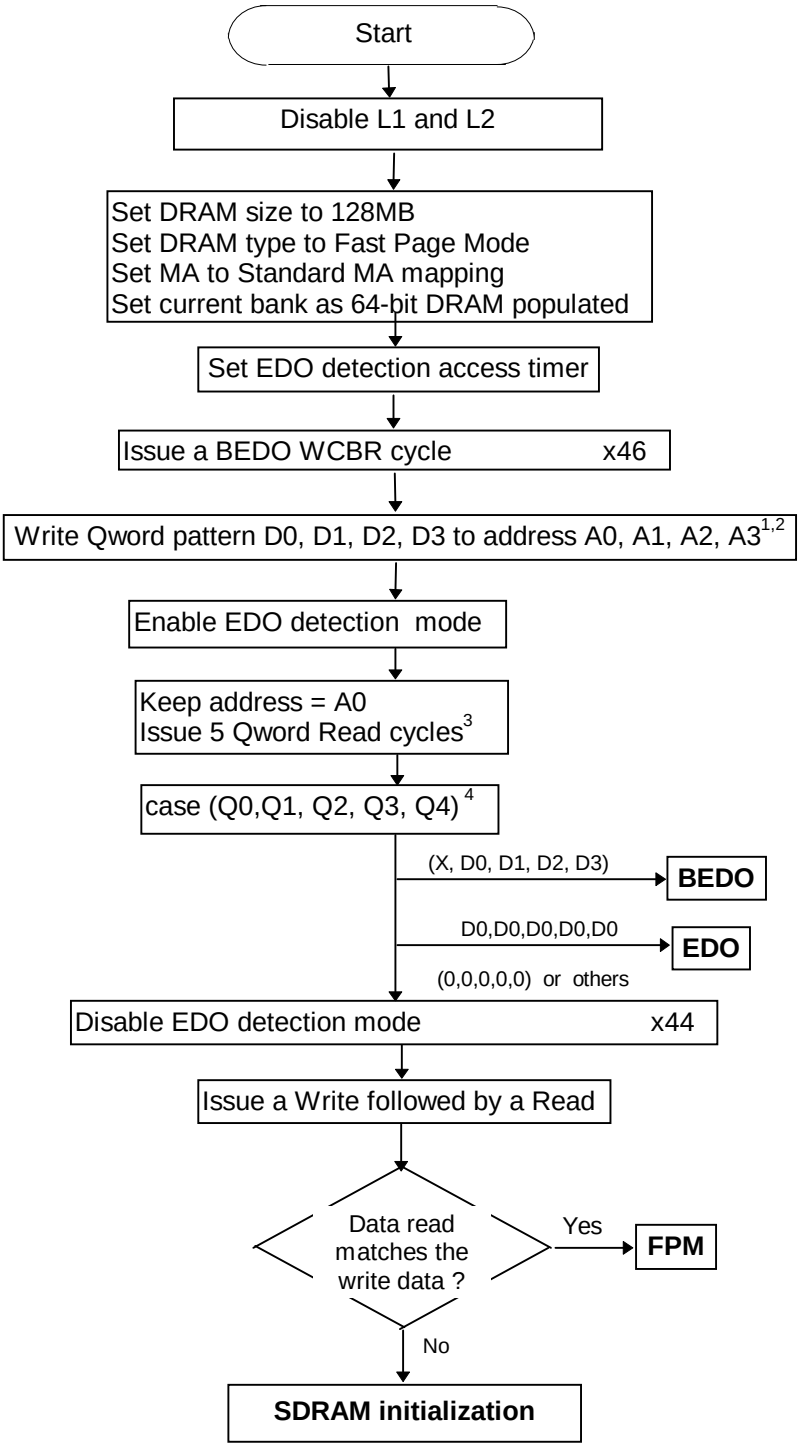


Figure 2. Type Detect plus 32-bit vs. 64-bit Bank Detect

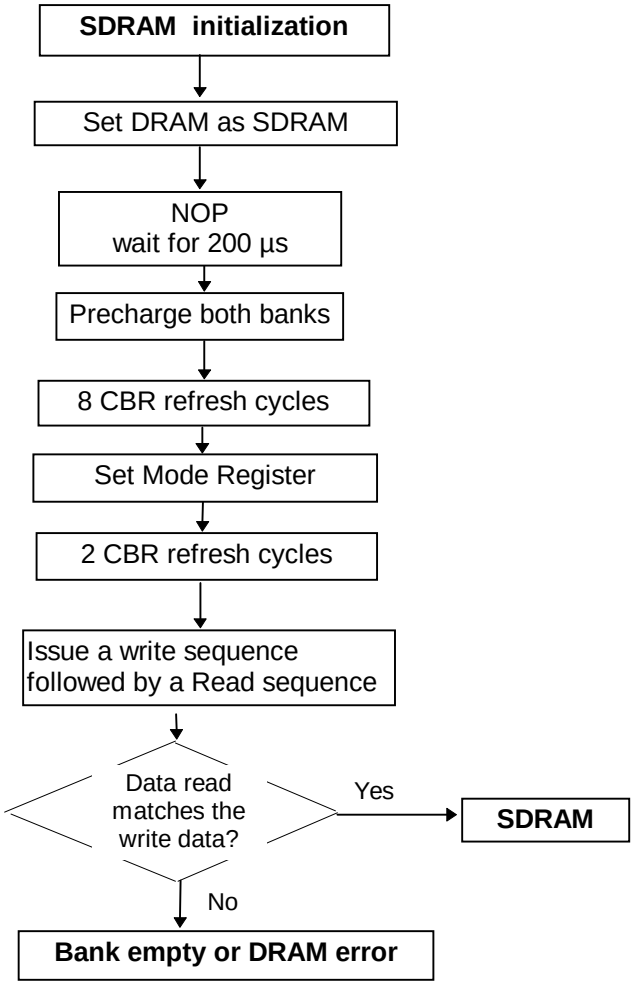
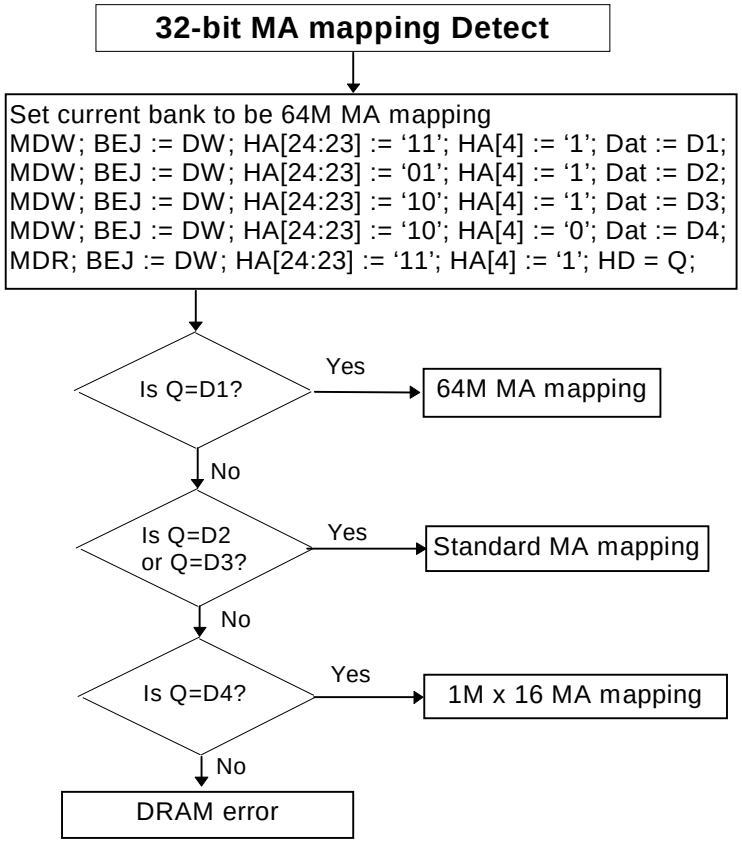


Figure 2-1. 32-bit vs. 64-bit Bank Detect

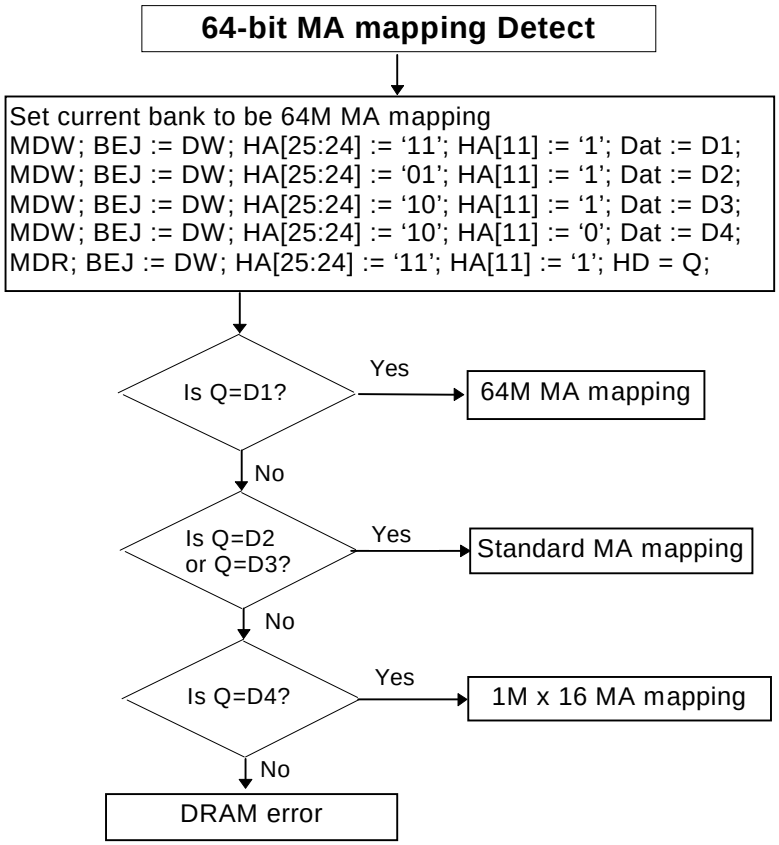
Note 1: Addresses A0-A3 must be lower than 1K and the Qword pattern D1-D3 must be Dword distinguishable.
Note 2: 4 Qword write must be broken into 4 lower Dword write followed by 4 higher Dword Write.
Note 3: 5 Qword Read must be broken into 5 lower Dword read followed by 5 higher Dword Read.
Note 4: Lower Dword, higher Dword, and Qword must be compared separately to detect lower 32-bits, higher 32-bits and 64-bit population.



	Din	D1	D2	D3	D4		
	Command	MDW	MDW	MDW	MDW	MDR	Dout
	MA	800 500	000 500	800 100	800 000	800 500	Q
64Mb	12x12	800 500	000 500	800 100	800 000	800 500	D1
	12x11	800 500	000 500	800 100	800 000	800 500	D1
	11x11	000 500	000 500	000 100	000 000	000 500	D2
STD	12x10	800 100	000 100	800 100	800 000	800 100	D3
	11x11	000 500	000 500	000 100	000 000	000 500	D2
	11x10	000 100	000 100	000 100	000 000	000 100	D3
	10x10	000 100	000 100	000 100	000 000	000 100	D3
	10x9	000 100	000 100	000 100	000 000	000 100	D3
1Mx16	12x8	800 000	000 000	800 000	800 000	800 000	D4

64M MA Mapping Table 32-bits

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A24	A22	A11	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A25	A23	A21	A4	A10	A9	A8	A7	A6	A5	(A2)	A3

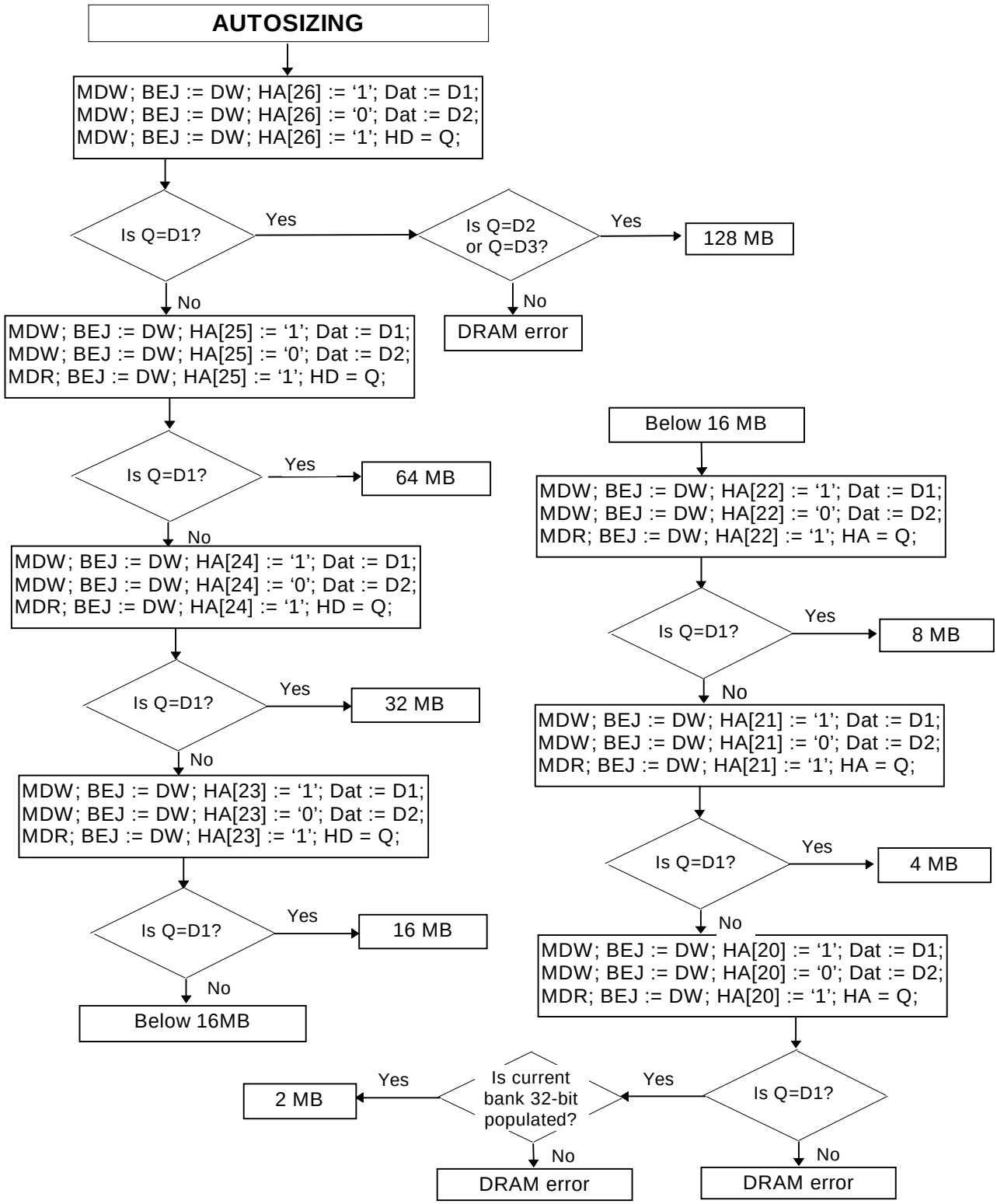


	Din	D1	D2	D3	D4		
	Command	MDW	MDW	MDW	MDW	MDR	Dout
	MA	800	000	800	800	800	Q
		500	500	100	000	500	
64Mb	12x12	800	000	800	800	800	D1
		500	500	100	000	500	
	12x11	800	000	800	800	800	D1
		500	500	100	000	500	
	11x11	000	000	000	000	000	D2
		500	500	100	000	500	
STD	12x10	800	000	800	800	800	D3
		100	100	100	000	100	
	11x11	000	000	000	000	000	D2
		500	500	100	000	500	
	11x10	000	000	000	000	000	D3
		100	100	100	000	100	
	10x10	000	000	000	000	000	D3
		100	100	100	000	100	
	10x9	000	000	000	000	000	D3
		100	100	100	000	100	
1Mx16	12x8	800	000	800	800	800	D4
		000	000	000	000	000	

64M MA Mapping Table 64-bits

MA[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
Row	A25	A23	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Column	A26	A24	A22	A11	A10	A9	A8	A7	A6	A5	A4	A3

QW


AUTOSIZING
MDW; BEJ := DW; HA[26] := '1'; Dat := D1;
MDW; BEJ := DW; HA[26] := '0'; Dat := D2;
MDW; BEJ := DW; HA[26] := '1'; HD = Q;
Is Q=D1?
Yes
Is Q=D2 or Q=D3?
Yes
128 MB
No
No
DRAM error
MDW; BEJ := DW; HA[25] := '1'; Dat := D1;
MDW; BEJ := DW; HA[25] := '0'; Dat := D2;
MDR; BEJ := DW; HA[25] := '1'; HD = Q;
Is Q=D1?
Yes
64 MB
No
MDW; BEJ := DW; HA[24] := '1'; Dat := D1;
MDW; BEJ := DW; HA[24] := '0'; Dat := D2;
MDR; BEJ := DW; HA[24] := '1'; HD = Q;
Is Q=D1?
Yes
32 MB
No
MDW; BEJ := DW; HA[23] := '1'; Dat := D1;
MDW; BEJ := DW; HA[23] := '0'; Dat := D2;
MDR; BEJ := DW; HA[23] := '1'; HD = Q;
Is Q=D1?
Yes
16 MB
No
Below 16MB
Below 16 MB
MDW; BEJ := DW; HA[22] := '1'; Dat := D1;
MDW; BEJ := DW; HA[22] := '0'; Dat := D2;
MDR; BEJ := DW; HA[22] := '1'; HA = Q;
Is Q=D1?
Yes
8 MB
No
MDW; BEJ := DW; HA[21] := '1'; Dat := D1;
MDW; BEJ := DW; HA[21] := '0'; Dat := D2;
MDR; BEJ := DW; HA[21] := '1'; HA = Q;
Is Q=D1?
Yes
4 MB
No
MDW; BEJ := DW; HA[20] := '1'; Dat := D1;
MDW; BEJ := DW; HA[20] := '0'; Dat := D2;
MDR; BEJ := DW; HA[20] := '1'; HA = Q;
Is Q=D1?
Yes
Is current bank 32-bit populated?
Yes
2 MB
No
DRAM error
No
DRAM error

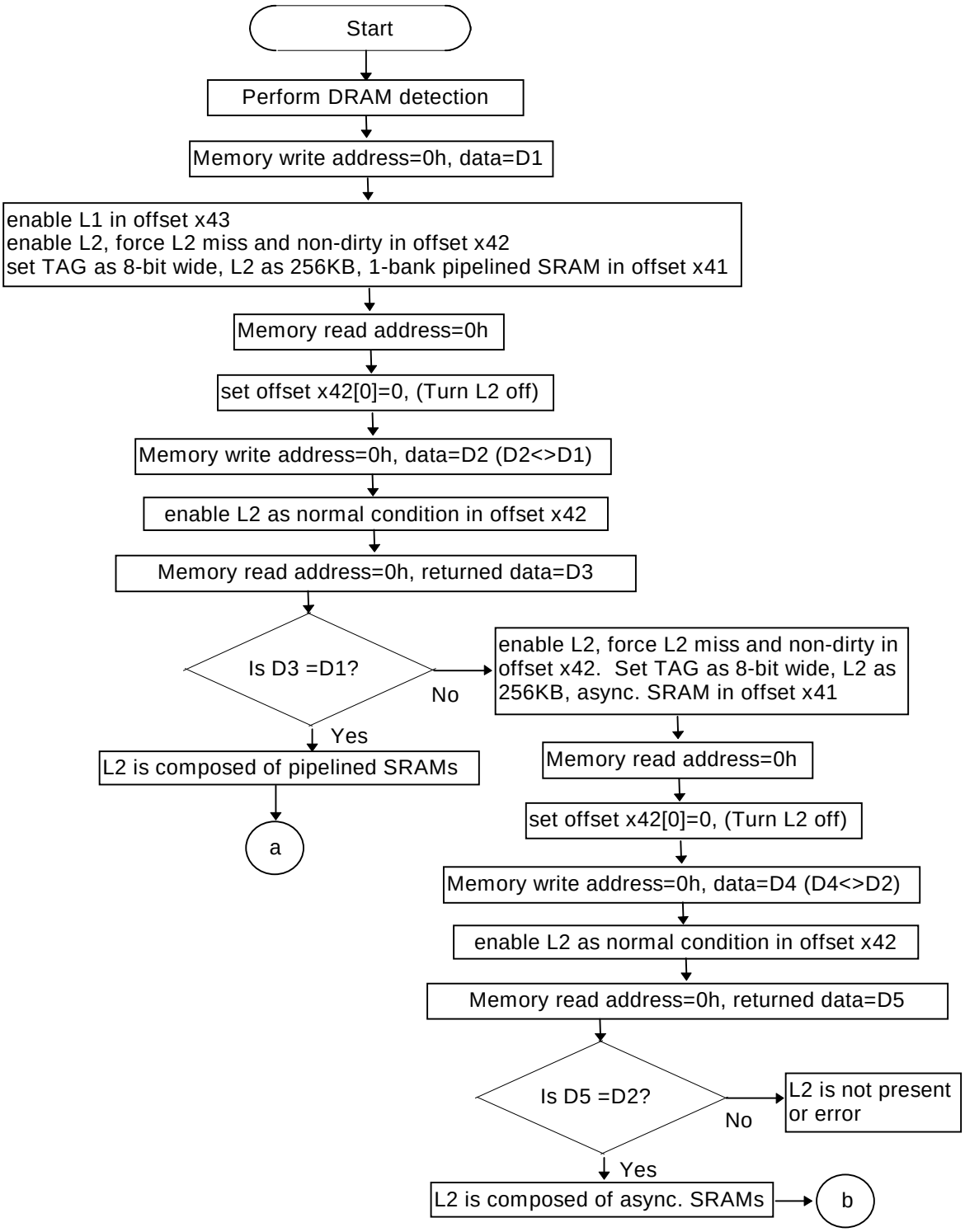
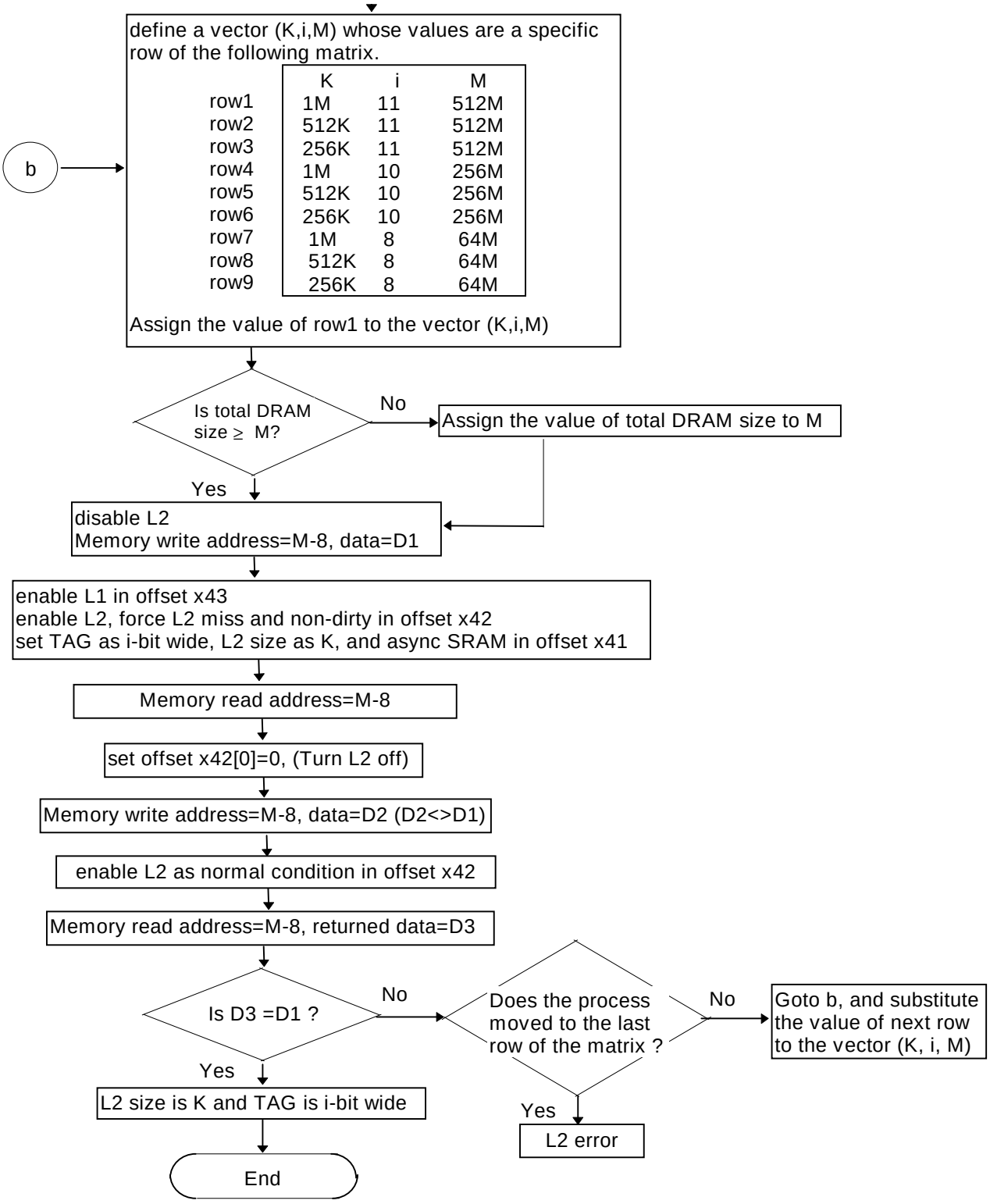
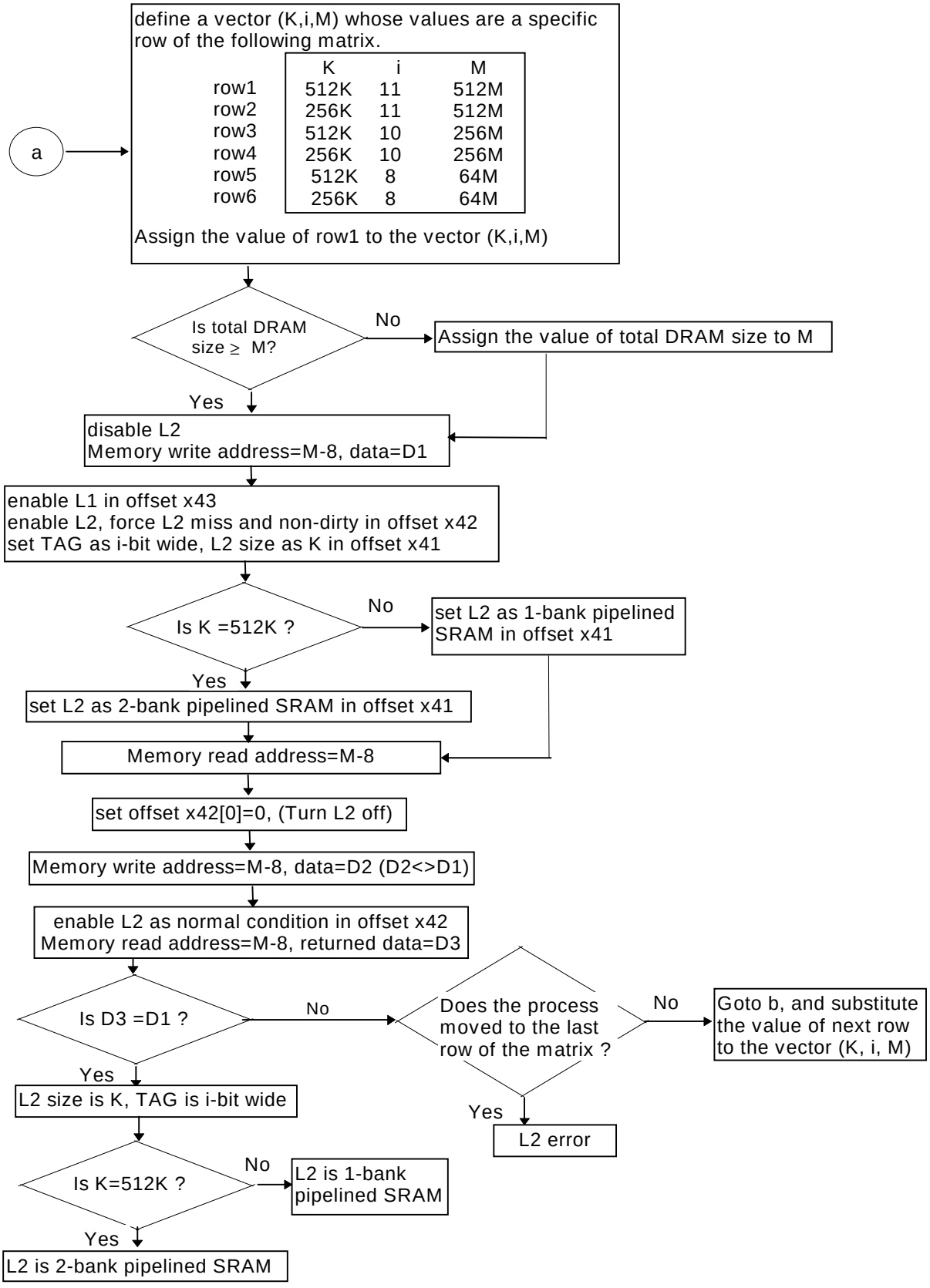


Figure 7. L2 Cache Autosizing Flowchart


b
define a vector (K,i,M) whose values are a specific row of the following matrix.
K i M
row1 1M 11 512M
row2 512K 11 512M
row3 256K 11 512M
row4 1M 10 256M
row5 512K 10 256M
row6 256K 10 256M
row7 1M 8 64M
row8 512K 8 64M
row9 256K 8 64M
Assign the value of row1 to the vector (K,i,M)
Is total DRAM size ≥ M?
No
Assign the value of total DRAM size to M
Yes
disable L2
Memory write address=M-8, data=D1
enable L1 in offset x43
enable L2, force L2 miss and non-dirty in offset x42
set TAG as i-bit wide, L2 size as K, and async SRAM in offset x41
Memory read address=M-8
set offset x42[0]=0, (Turn L2 off)
Memory write address=M-8, data=D2 (D2<>D1)
enable L2 as normal condition in offset x42
Memory read address=M-8, returned data=D3
Is D3 =D1 ?
No
Does the process moved to the last row of the matrix ?
No
Goto b, and substitute the value of next row to the vector (K, i, M)
Yes
L2 size is K and TAG is i-bit wide
Yes
L2 error
End


a
define a vector (K,i,M) whose values are a specific row of the following matrix.
K i M
row1 512K 11 512M
row2 256K 11 512M
row3 512K 10 256M
row4 256K 10 256M
row5 512K 8 64M
row6 256K 8 64M
Assign the value of row1 to the vector (K,i,M)
Is total DRAM size ≥ M?
No
Assign the value of total DRAM size to M
Yes
disable L2
Memory write address=M-8, data=D1
enable L1 in offset x43
enable L2, force L2 miss and non-dirty in offset x42
set TAG as i-bit wide, L2 size as K in offset x41
Is K =512K ?
No
set L2 as 1-bank pipelined SRAM in offset x41
Yes
set L2 as 2-bank pipelined SRAM in offset x41
Memory read address=M-8
set offset x42[0]=0, (Turn L2 off)
Memory write address=M-8, data=D2 (D2<>D1)
enable L2 as normal condition in offset x42
Memory read address=M-8, returned data=D3
Is D3 =D1 ?
No
Does the process moved to the last row of the matrix ?
No
Goto b, and substitute the value of next row to the vector (K, i, M)
Yes
L2 size is K, TAG is i-bit wide
Yes
L2 error
Is K=512K ?
No
L2 is 1-bank pipelined SRAM
Yes
L2 is 2-bank pipelined SRAM

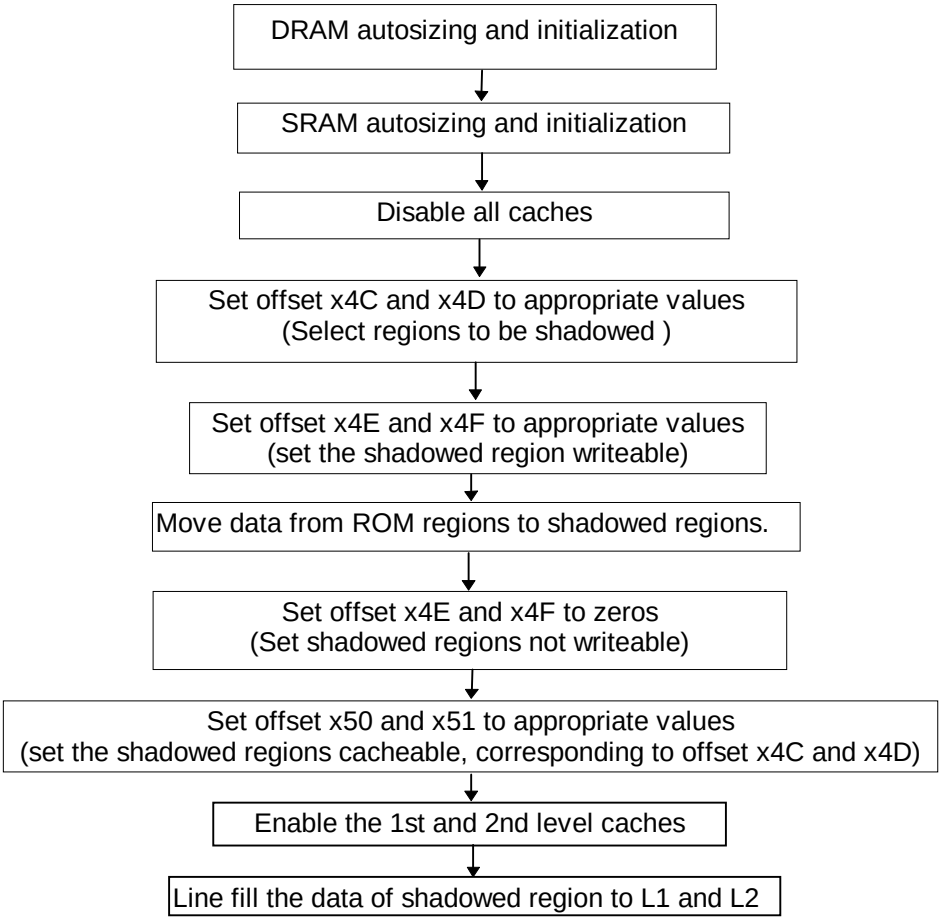


Figure 8. Flowchart of Enabling the Shadowed Regions

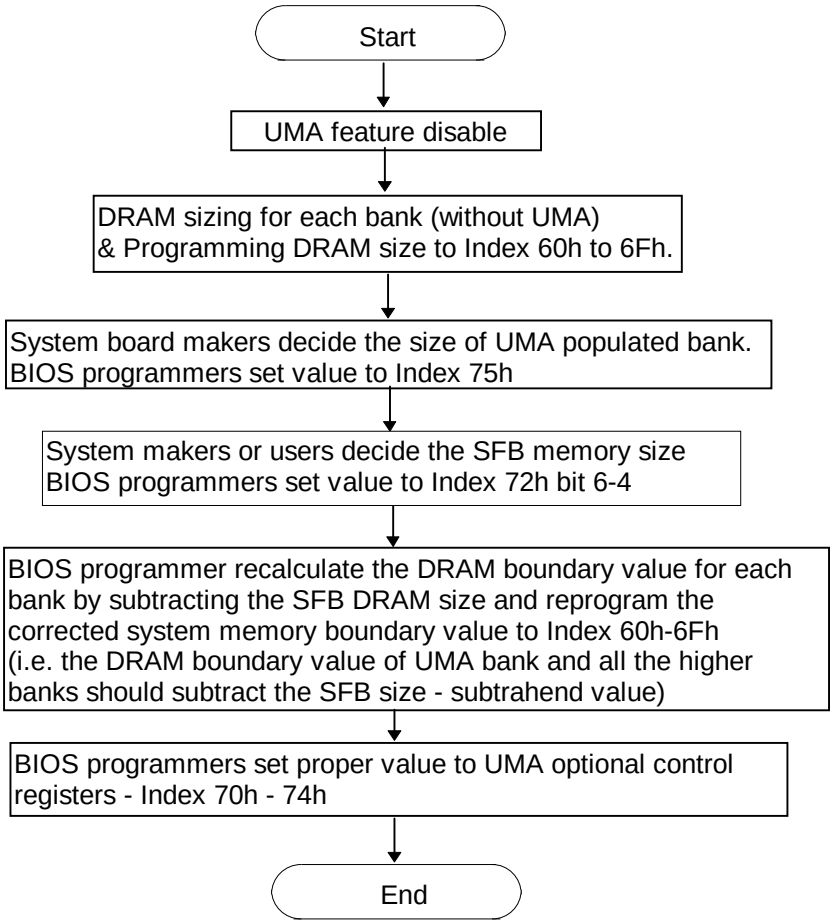
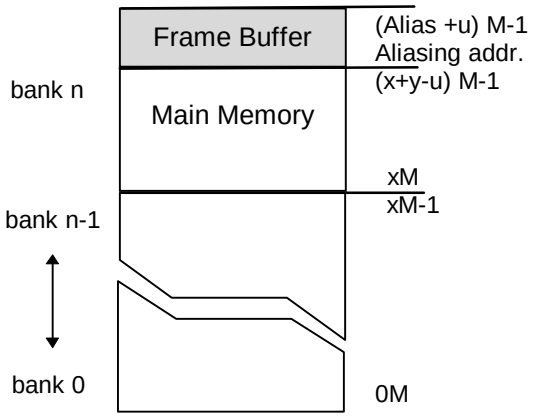


Figure 9. DRAM bank Boundary Programming Flowchart in UMA System

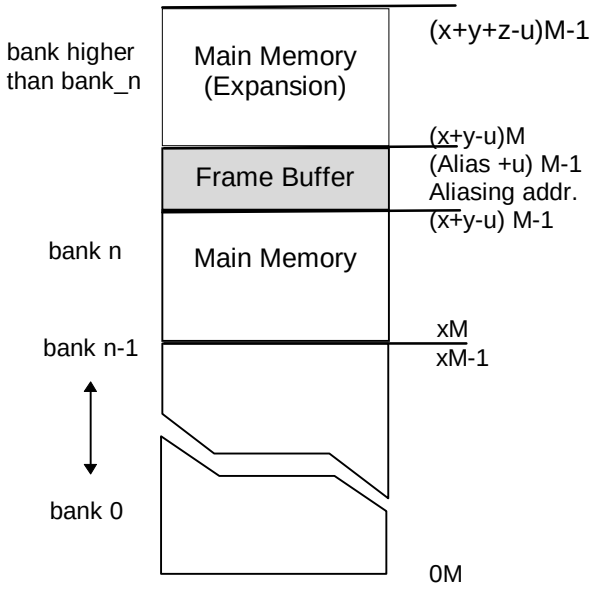
Note : SFB size	Subtrahend
512K	1M
1M	1M
2M	2M
3M	3M
4M	4M

The boundary should subtract 1M when the SFB size is 512K. And, the M1521 will automatically compensate 512K to the size of system memory.

Frame Buffer Memory logical remapped algorithm after system memory has expanded.
Formulas : UMA memory is populated in bank_n
Bank_n populated DRAM size = y MB
UMA memory size = u MB
bank_0~ bank_n-1 total DRAM size : x MB
Expanded DRAM size = z MB populated after bank_n



Main Memory before Expansion



Main Memory after Expansion

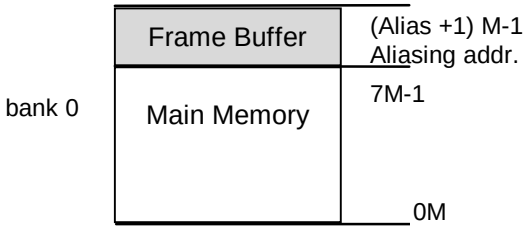
Note : Aliasing start address should not be less than (x+y-u)M

Note : Aliasing start address should not be less than (x+y+z-u)M

Figure 10. Frame Buffer Memory Logical Remapped Algorithm

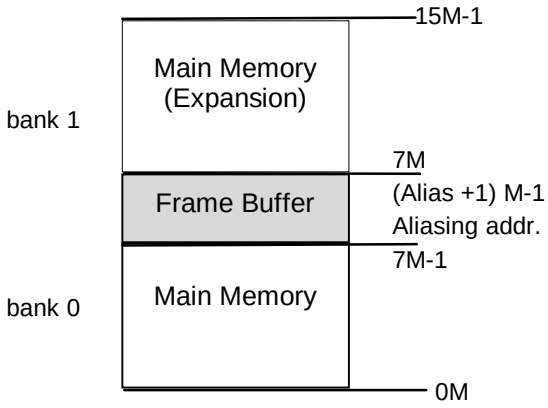
Frame Buffer Memory logical remapped algorithm after system memory has expanded.

Example : UMA memory is populated in bank 0
Bank 0 populated DRAM size = 8 MB
UMA memory size = 1 MB
Expanded DRAM size = 8 MB populated in bank 1



Main Memory before Expansion

Note : Aliasing start address should not be less than 7M

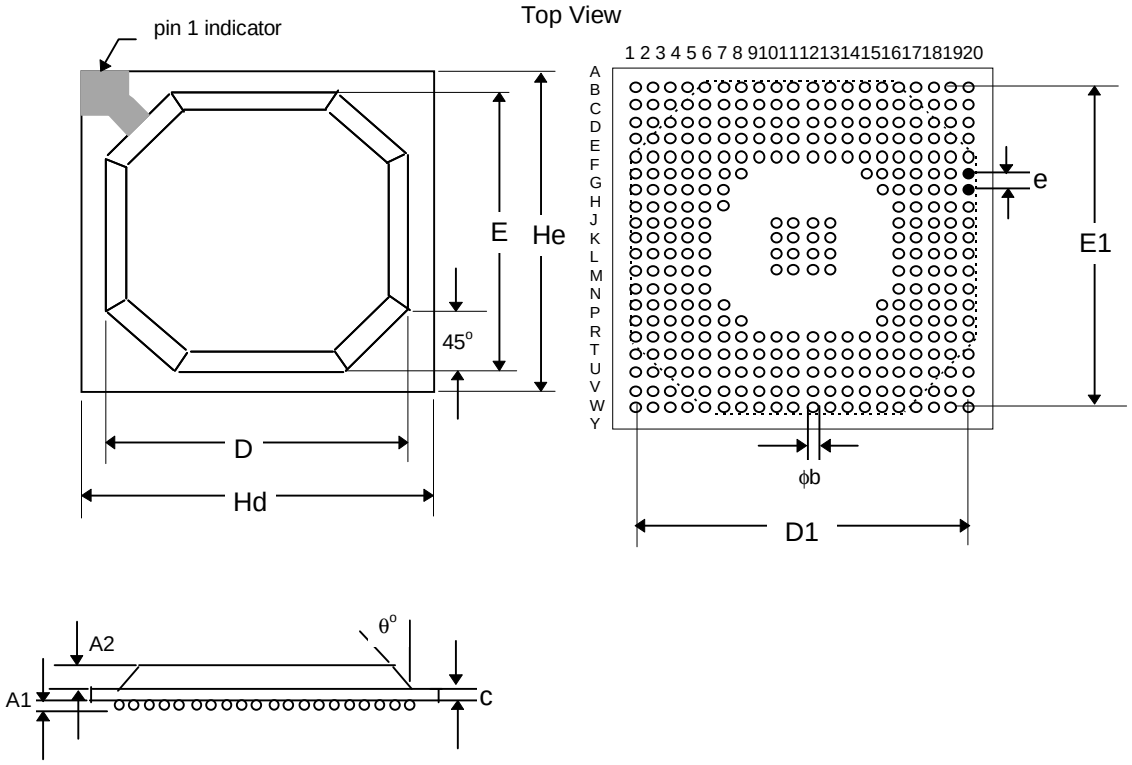


Main Memory after Expansion

Note : Aliasing start address should not be less than 15M

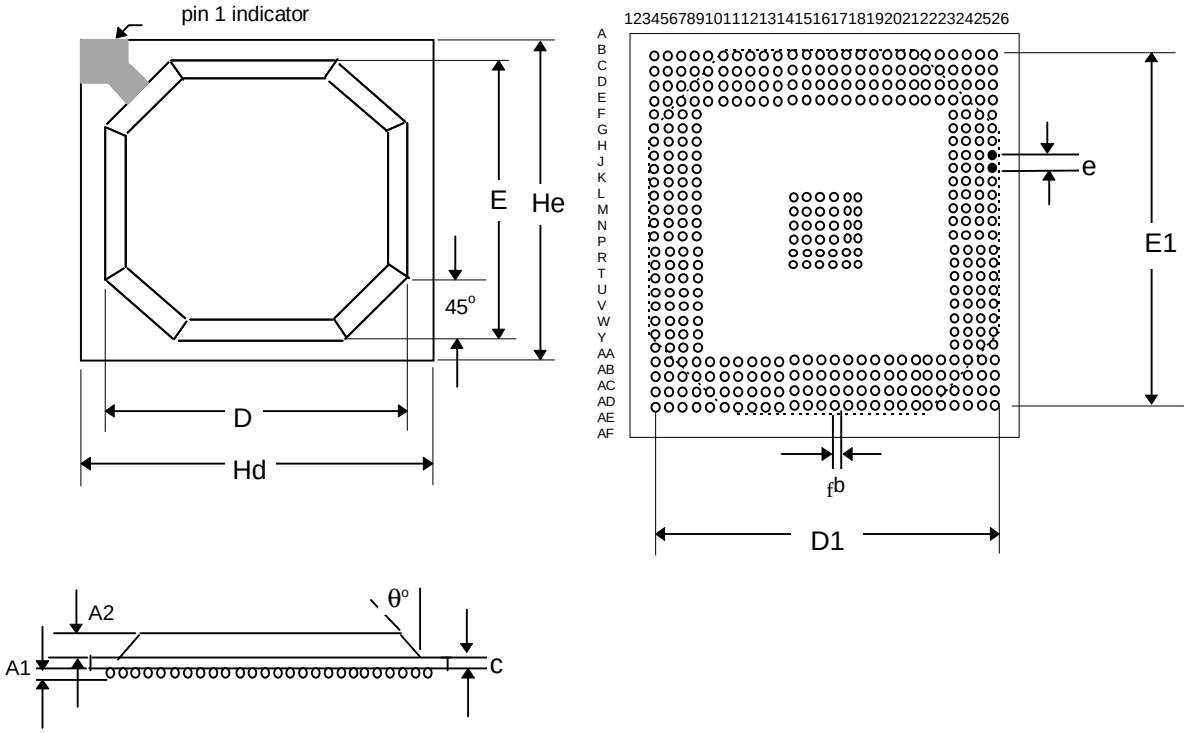
Section 6 : Packaging Information

BGA -5 Dimension Spec (27 x 27 mm)



Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕb	0.60	0.75	0.90
c	0.51	0.56	0.61
D	23.80	24.00	24.20
D1	23.93	24.13	24.33
E	23.80	24.00	24.20
E1	23.93	24.13	24.33
e		1.27	
Hd	26.80	27.00	27.20
He	26.80	27.00	27.20
θ°	23°	30°	37°
Y (radius of ball)			0.25

BGA -4 Dimension Specification (35 x 35 mm)



Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕb	0.60	0.75	0.90
c	0.51	0.56	0.61
D	29.80	30.00	30.20
D1	31.55	31.75	31.95
E	29.80	30.00	30.20
E1	31.55	31.75	31.95
e		1.27	
Hd	34.80	35.00	35.20
He	34.80	35.00	35.20
θ°	23°	30°	37°
Y(radius of ball)			0.25