93C488
5x86/486 Single Chip

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Rev. 09/21/96-12:00PM

Revision changes:

Rev. 08/02/96-6:57 PM
Correct the meanings of configuration register 23H Bit 7 and Bit 6.

Rev. 08/05/96-11:12 AM
Index C6H bit 4 definition change from I/O address decode to ROMCS decode in memory write cycle.

Rev. 08/28/09-4:21 PM
Add DC characteristics table.

Rev. 09/04/96-10:42 AM
Add introduction page.

Rev. 09/21/96-12:00 PM
Add control bit to support Cyrix burst write back cycle. (Index 12H bit 0)
Correct the default setting of 80H bit 2.

Notice

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1. Introduction

ALD93C488 is the world first single chip 486/5x86 core logic that supports Pipeline Burst/Burst (PB) Synchronous SRAM for L2 cache implementation. This innovative feature results in much superior performance than the previous generation core logic design that uses Asynchronous SRAM for L2 cache. ALD93C488 also features one of the highest integration in the market and requires only DRAM, BIOS and 9 pieces TTL to complete a cost-effective PCI/ISA system that supports all available 486 pinout CPUs up to bus speed of 50 MHz.

Employing state-of-the-art 0.6 Micron CMOS technology, ALD93C488 integrates the PB Cache Controller, DRAM Controller, ISA Peripheral Controllers (Interrupt Controller, DMA Controller, Timer/Counter, Real-time Clock and Keyboard Controller), PCI and ISA Interface and an Enhanced Local Bus IDE Interface into a single 208 QFP (Quad Flat Pack) IC.

Applying the same technique as the latest Pentium systems, the PB Cache Controller achieves 3,1,1,1 burst cycle with Pipeline Burst Synchronous SRAM. Write Back Cache Policy is employed for better CPU bandwidth utilization. Cache size can range from 128 KB to 1 MB. The DRAM Controller supports Page, Fast Page and EDO DRAM for maximum compatibility and ultimate performance. Four banks of DRAM, from 1 MB to 256 MB, can be accessed, with Auto-detection of memory type and size.

The PCI Interface meets the requirements of PCI Specifications 2.1 (5 V). To support PCI cards that have on-board intelligence, two PCI Bus Masters can be used. In addition to Host- to- PCI Byte Merging, a 4-level Host- to- PCI Write Buffer is designed to ensure maximum system throughput..

The built-in Enhanced Local Bus IDE Interface supports up to 4 IDE devices (PIO Mode 4 timing). Advanced features like Address Swapping between Primary and Secondary IDE Ports and separate Master/Slave modes are implemented. To make computers environmentally friendly , ALD93C488 is equipped with integrated power management technique to stop or slow down the CPU.

2. Features

ÿ Support processor bus up to 50MHz.
- AMD 5x86-133, 486DX4-120/100, 486DX2-80/66, 486DX-50/40/33/25
- Cyrix/IBM/ST 5x86-120/100, 486DX4-120/100, 486DX2-80/66/50, 486DX-40/33/25
- TI 486DX4-100, 486DX2-80/66
- Intel 486DX4-100/75, 486DX2-66, 486DX-40/33/25, 486SX

ÿ Integrated DRAM controller
- 1Mbyte to 256Mbyte main memory
- Non-page mode, Fast page mode, Nibble mode, Write per bit mode, EDO mode DRAM providing flexible timing control
- Supports for auto detection of memory type including size, refresh cycle.
- 4 RAS lines for 4 DRAM banks
- Supports for symmetrical and asymmetrical DRAM addressing
- Supports RAS only, CBR hidden refresh
- Supports shadow memory and 384K relocated memory

ÿ Integrated synchronous cache controller
- 128Kbyte to 1Mbyte cache
- Support pipeline/non-pipeline burst SSRAM
- Support X,1,1,1/X,2,2,2 burst cycle

ÿ Fast IDE interface
- Supports up to PIO mode 4 Timings
- Separate master/slave IDE mode support
- Supports primary/secondary port address swapping

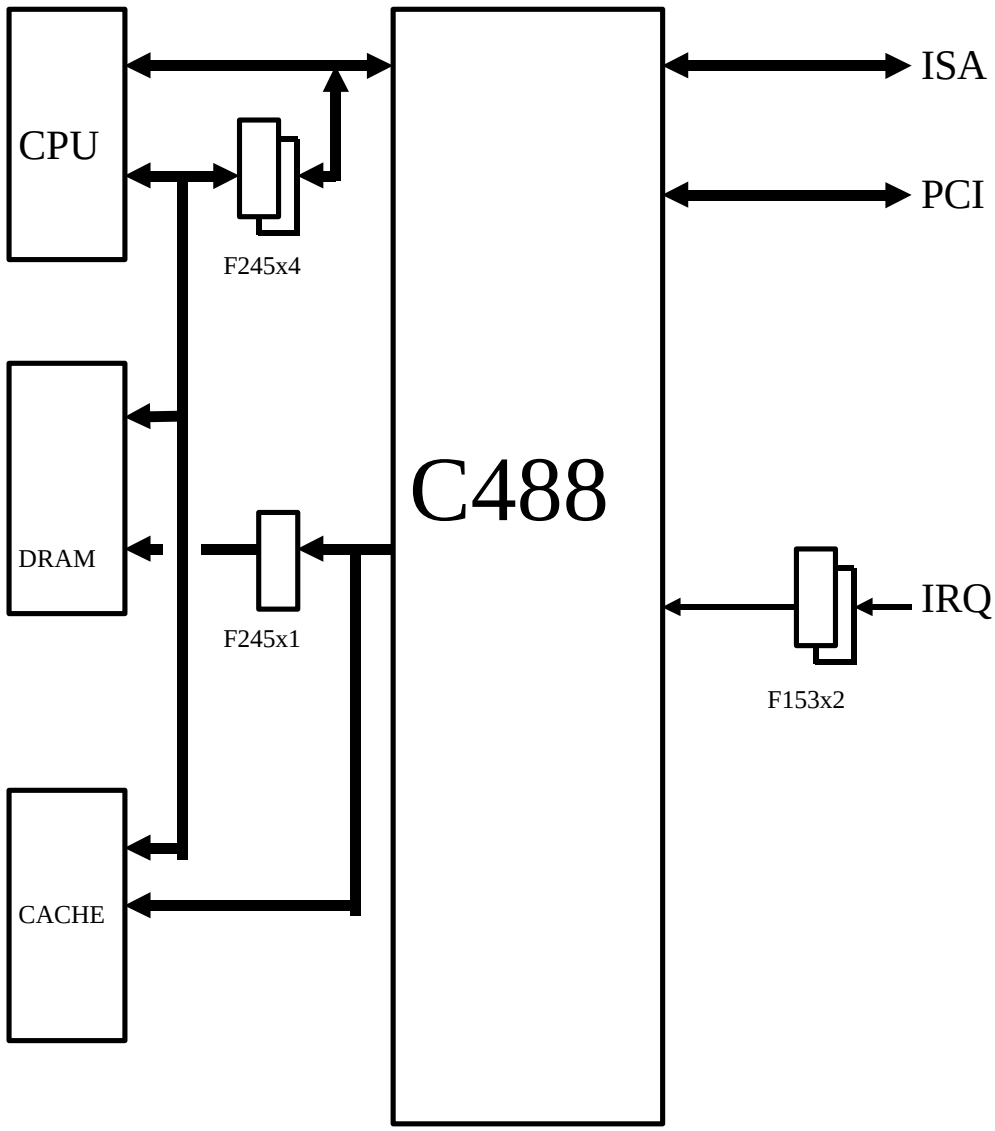
ÿ PCI bus controller
- 4 level host to PCI write buffer
- Supports host to PCI byte merging
- Supports two PCI bus master

ÿ Integrated IPC includes
- Two 8259 interrupt controllers
- Two 8237 DMA controllers
- One 8254 timer/counter
- RTC
- Keyboard controller

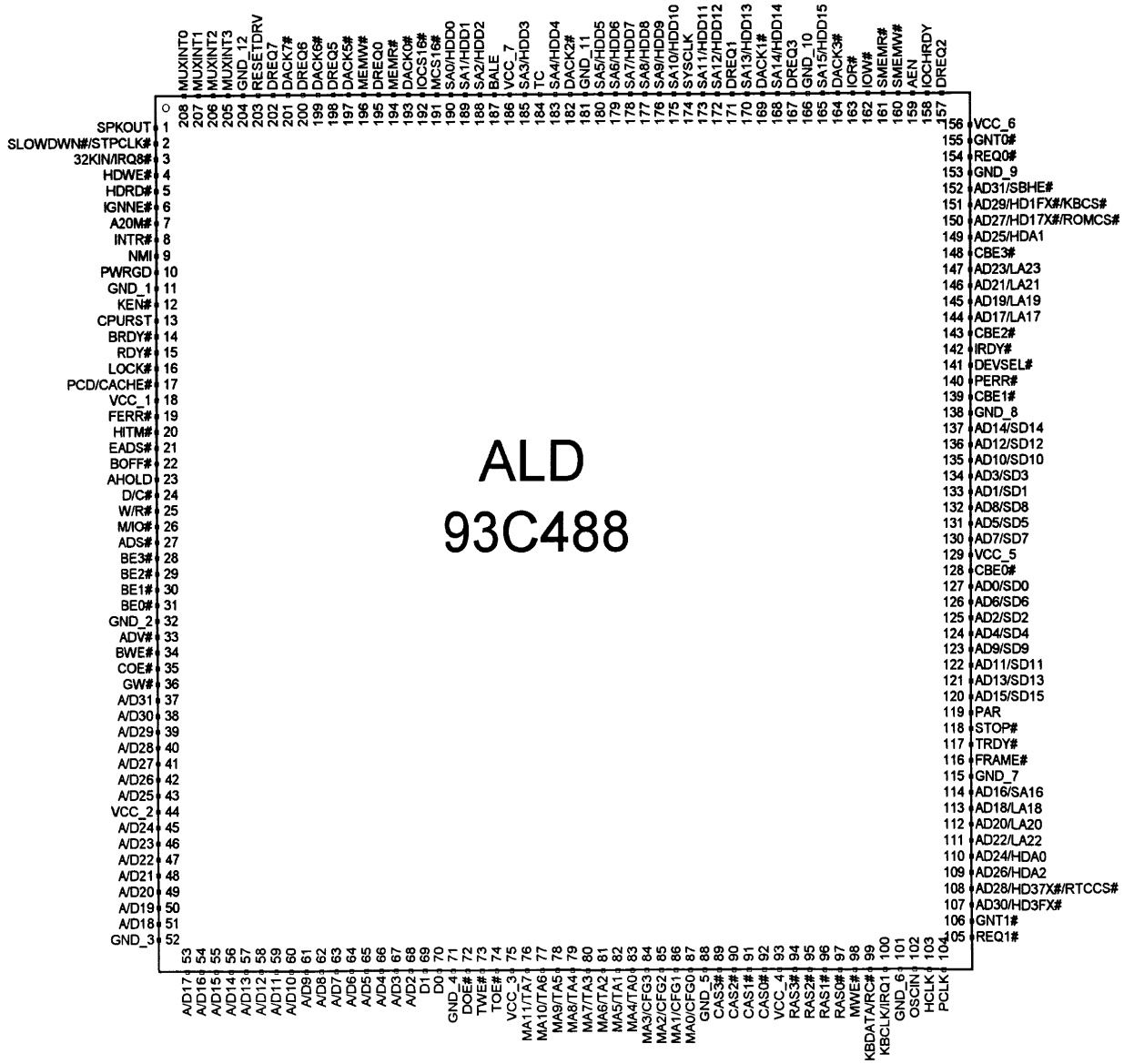
ÿ Power management
- Programmable hardware events
- Programmable CPU clock control (STPCLK#)
- Slow down system clock speed (SLOWDWN#)

ÿ Single chip 208 pin QFP

3. System block diagram



4. Pin diagram



5. Pin description

Signal Name	Pin Number	I/O	Description	Driving Capability
Host interface signals:-				
D[1:0]	69,70	I/O	Host data lines D0 and D1.	8mA
A/D[31:2]	37 - 43, 45 - 51, 53 - 68	I/O	Multiplexed Host address and data bus.	8mA
ADS#	27	I/O	Host address strobe. External 10Kohm pull-up is required.	8mA
M/IO# D/C# W/R#	26 24 25	I/O	The memory/input-output, data/control and write/read lines are the primary bus definition signals. These signal is sampled when ADS# is asserted. M/IO# D/C# W/R# Bus Cycle type 0 0 0 Interrupt acknowledge 0 0 1 Halt/Special cycle 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write	8mA
AHOLD	23	O	Address hold request. Host should float its address bus in the clock following this signal going active.	8mA
BOFF#	22	O	Bus off request. Host should float the control/address/data bus in the clock following this signal going active.	8mA
EADS#	21	O	This signal indicates that a valid external address has been driven onto the host address pins to perform a cache invalidation cycle.	8mA
HITM#	20	I	In write-back mode, HITM# indicate that an external snoop cache tag comparison hit a modified line. CPU will then drive this pin to low two clock after EADS# is asserted to initiate a write-back cycle. External 10Kohm pull-up is required.	---
PCD/CACHE#	17	I	PCD of write-through CPU or CACHE# of a write-back CPU. When this pin acts as PCD pin, it is used with LOCK#, M/IO#, and W/R# pins to determine whether the bus cycle is cacheable or not. When this pin acts as CACHE# pin, a low on this pin indicates that the current read cycle is cacheable, or that the current cycle is a burst write or copy-back cycle.	---
LOCK#	16	I	Bus lock. This signal is used with PCD, M/IO# and W/R# to determine whether the current cycle is cacheable or not. For write-through CPU, a cacheable cycle is defined as a Unlocked memory read cycle with PCD de-asserted. For write-back CPU and PCD/CACHE# pin is selected as	---

			CACHE# signal, this pin is not used.	
RDY#	15	O	Non-burst Ready. A low on this pin indicates that the current bus cycle is completed, and valid data has been presented in response to a read, or data has been accepted in response to a write in a non-burst cycle.	12mA
BRDY#	14	O	Burst Ready. A Low on this pin indicates that valid data has been presented in response to a read, or data has been accepted in response to a write in a burst cycle.	12mA
CPURST/SRESET	13	O	CPU Reset for a write-through CPU or Soft Reset for a write-back CPU. It will assert when PWRGD is low, or a shutdown cycle is detected, or a reset processor signal(RC#) is activated. This signal will assert at least 16 HCLK after both PWRGD and RC# return to logic ONE. For proper operation, an external 10K pull-up resister is required.	4mA
KEN#	12	O	Cache Enable. It is asserted when the current bus cycle is determined as a cacheable DRAM cycle. It is always asserted when the bus is idle or at the first clock of a bus cycle.	8mA
BE[3:0]#	28 - 31	I/O	Byte Enable. They indicate which bytes are enabled and active during read or write cycles. They are ignored and assume all byte are active during the cache fill cycle.	8mA
FERR#	19	I	Floating-Point Error. A low on this pin indicates an error occurs in the floating-point unit. Upon the reception of this signal, hardware interrupt IRQ13 is generated internally and, if not masked, will cause processor to enter the error-handling routine.	---
IGNNE#	6	O	Ignore Numeric Error. This pin is normally high, after a write to I/O location 03F0H or 03F1H when FERR# is asserted, it will set to low. It will go high after FERR# returns to a high state.	4mA
NMI	9	O	Non-maskable Interrupt. It is asserted when a parity error occurs during PCI transfer cycle, or a power management interrupt occur when the power management interrupt is routed to this output.	4mA
INTR	8	O	Interrupt Request. It is asserted by the internal interrupt controller when it receives a interrupt request from the peripherals.	4mA

Signal Name	Pin Number	I/O	Description	Driving Capability
PCI Interface signals:-				
AD[31]/SBHE#	152	I/O	During PCI cycle, it is the address/data line 31. During ISA cycle, it is the byte high enable signal.	12mA
AD[30]/HD3FX#/ P70CS#	107	I/O	During PCI cycle, it is the address/data line 30. During on-chip IDE access, it is the primary IDE chip select signal. During ISA cycle, it is the I/O port 70 chip select signal.	12mA
AD[29]/HD1FX#/ KBCS#	151	I/O	During PCI cycle, it is the address/data line 29. During on-chip IDE access, it is the primary IDE chip select signal. During ISA cycle, it is the chip select signal for the external keyboard controller.	12mA
AD[28]/HD37X#/ RTCCS#	108	I/O	During PCI cycle, it is the address/data line 28. During on-chip IDE access, it is the secondary IDE chip select signal. During ISA cycle, it is the chip select signal for the external real time clock.	12mA
AD[27]/HD17X#/ ROMCS#	150	I/O	During PCI cycle, it is the address/data line 27. During on-chip IDE access, it is the secondary IDE chip select signal. During ISA cycle, it is the chip select signal for the BIOS ROM.	12mA
AD[26:24]/HDA[2:0]	109, 149, 110	I/O	During PCI cycle, it is the address/data line 26:24. During on-chip IDE access, it is the IDE address line 2:0.	12mA
AD[23:17]/LA[23:17]	147, 111, 146, 112, 145, 113, 144	I/O	During PCI cycle, it is the address/data line 23:17. During ISA cycle, it is the address line LA[23:17].	12mA
AD[16]/SA[16]	114	I/O	During PCI cycle, it is the address/data line 16. During ISA cycle, it is the address line SA[16].	12mA
AD[15:0]/SD[15:0]	120, 137, 121, 136, 122, 135, 123, 132, 130, 126, 131, 124, 134, 125, 133, 127	I/O	During PCI cycle, it is the address/data line 15:0. During ISA cycle, it is the data line SD[15:0].	12mA
CBE[3:0]#	148, 143, 139, 128	I/O	PCI Command/Byte Enable signals. During address phase of a transaction, they define the bus command (Refer to following table for bus command definitions.) During data phase they are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. CBE# Description 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read	PCI spec.

			0011 I/O Write 0100 Reserved 0101 Reserved 0110 Memory Read 0111 Memory Write 1000 Reserved 1001 Reserved 1010 Configuration Read 1011 Configuration Write 1100 Memory Read Multiple 1101 Dual Address Cycle 1110 Memory Read line 1111 Memory Write and Invalidate	
FRAME#	116	I/O	Frame is driven by the current master to indicate the beginning and duration of an access. External 10Kohm pull-up is required.	PCI spec.
IRDY#	142	I/O	Initiator Ready. This signal indicates the PCI bus master ability to complete the current data phase of the transaction. This pin is output when C488 acts as a PCI master. External 10Kohm pull-up is required.	PCI spec.
TRDY#	117	I/O	Target Ready. This indicates the target ability to complete the current data phase of transaction. This pin is output when C488 acts as a slave. External 10Kohm pull-up is required.	PCI spec.
STOP#	118	I/O	This indicates the current target is requesting the master to stop the current transaction. This pin is output in PCI master cycle when multiple data transfer is disable. External 10Kohm pull-up is required.	PCI spec.
DEVSEL#	141	I/O	Device Select. This indicates the target device has decoded the address as its own cycle. This is output when C488 acts as a PCI slave. External 10Kohm pull-up is required.	PCI spec.
GNT[1:0]#	106, 155	O	PCI Grant. These indicate to the requesting device that access to the bus has been granted.	12mA
REQ[1:0]#	105, 154	I	PCI Master Request. These indicate that the corresponding PCI device desires to use the bus. External 10Kohm pull-up is required.	---
PAR	119	I/O	PCI Parity. It is even parity across AD[31:0] and CB[3:0]#. C488 generates parity bit when :- 1. It acts as a PCI slave in read cycle data phase. 2. It acts as a PCI master in write cycle. 3. It acts as a PCI master in read cycle address phase.	PCI spec.
PERR#	140	I/O	Parity Error. This pin may be pulsed by target device which detects a data parity error. C488 will generate NMI when PERR# is sampled low. External 10Kohm pull-up is required.	PCI spec.
MUXINT[3:0]#	205 - 208	I	Multiplexed Interrupt input. C488 will use OSC and SYSCLK to de-multiplex these signals and forms the IRQ and INT# signals as:- SYS-CLK / OSC / MUX-INT[3] / MUX-INT[2] / MUX-INT[1] / MUX-INT[0] 0 / 0 / IRQ12 / IRQ7 / IRQ3 / INTA#	---

			0	1	IRQ14	IRQ9	IRQ4	INTB#	
			1	0	IRQ15	IRQ10	IRQ5	INTC#	
			1	1	KBINH#	IRQ11	IRQ6	INTD#	

Signal Name	Pin Number	I/O	Description	Driving Capability
ISA Interface signals:-				
AD[23:17]/LA[23:17]	147, 111, 146, 112, 145, 113, 144	I/O	During PCI cycle, it is the address/data line 23:17. During ISA cycle, it is the address line LA[23:17].	12mA
AD[16]/SA[16]	114	I/O	During PCI cycle, it is the address/data line 16. During ISA cycle, it is the address line SA[16].	12mA
AD[15:0]/SD[15:0]	120, 137, 121, 136, 122, 135, 123, 132, 130, 126, 131, 124, 134, 125, 133, 127	I/O	During PCI cycle, it is the address/data line 15:0. During ISA cycle, it is the data line SD[15:0].	12mA
DREQ[7:5,3:0]	202, 200, 198, 167, 157, 171, 195	I	DMA Request. DREQ[3:0] is 8-bit DMA channel and DREQ[7:5] is 16-bit DMA channel. External 10Kohm pull-down is required.	---
DACK[7:5, 3:0]#	201, 199, 197, 164, 182, 169, 193	O	DMA Acknowledge.	8mA
SMEMR#	161	O	System Memory Read. This is a output signal which is driven low only when the system read ISA memory resided below 1Mbyte address range.	12mA
SMEMW#	160	O	System Memory Write. This is a output signal which is driven low only when the system write ISA memory resided below 1Mbyte address range.	12mA
IOR#	163	I/O	I/O read. This is driven by C488 in Processor or DMA cycle. During ISA bus master cycle, it becomes a input. External 10Kohm pull-up is required.	12mA
IOW#	162	I/O	I/O write. This is driven by C488 in Processor or DMA cycle. During ISA bus master cycle, it becomes a input. External 10Kohm pull-up is required.	12mA
MEMR#	194	I/O	Memory Read. This is driven by C488 in Processor or DMA cycle. During ISA bus master cycle, it becomes a input. External 10Kohm pull-up is required.	12mA
MEMW#	196	I/O	Memory Write. This is driven by C488 in Processor or DMA cycle. During ISA bus master cycle, it becomes a input. External 10Kohm pull-up is required.	12mA
SYSCLK	174	O	System Clock. This is a 7.159MHz clock signal.	12mA
BALE	187	O	Bus Address Latch enable. A high pulse with halt SYSCLK is generated at the beginning of Processor ISA cycle. During ISA DMA or bus master cycle. It is kept at high level.	8mA

AEN	159	O	DMA address enable. During DMA cycle, it is driven high to inhibit I/O device to decode the address.	8mA
TC	184	O	DMA Terminal Count. It is driven high to indicate the last transfer in multiple DMA transfer cycle.	8mA
IOCS16#	192	I	I/O chip select 16. It is driven low by a 16 bit I/O device. External 330ohm pull-up is required.	---
RESETDRV	203	O	System Reset output. It is driven high only when PWRGD input is low. This is used to initialize the Peripheral to a known state. It will go to CPU reset pin for Supporting CPU L1 write-back function. For proper operation, an external 10K pull-up resister is required.	16mA
SA[15:0]/HDD[15:0]	165, 168, 170, 172, 173, 175 - 180, 183, 185, 188 - 190	I/O	For ISA cycle, these are the address line 15 to 0. For On-chip IDE cycle, these are data line 15 to 0 for the IDE port. External 10Kohm pull-up is required.	12mA
IOCHRDY	158	I/O	This pin is driven low by ISA device to extend the ISA command cycle. External 4.7Kohm pull-up is required.	16mA

Signal Name	Pin Number	I/O	Description	Driving Capability
Memory Interface signals:-				
MA[11:4]/TA[7:0]	76 - 83	I/O	Memory Address line 11:4 or L2 cache Tag 7:0. When L2 cache is not enable, they are the memory address lines for DRAM interface. When L2 cache is enable, they are the multiplex bus for both cache tag data and DRAM address. Signal pin TOE# high represents they are carrying memory address information; TOE# low represents they are carrying tag data information.	24mA
MA[3:0]/CFG[3:0]	84 - 87	I/O	Memory Address line 3:0 and Configuration line 3:0. During PWRGD is low, they are the hardware configuration input, it is recommend to connect to the hardwire jumper through 10Kohm resisters. After RESETDRV returns to low, They become memory address line 3:0. CFG[0] Set high to enable internal keyboard controller. CFG[1] Set high to enable internal real time clock. CFG[2] Reserved, must be high. CFG[3] Test mode, must be high for normal operation.	24mA Note *
MWE#	73	O	DRAM Write. It is driven low to enable write data to memory, for EDO memory, it is pulse low to terminate the read cycle. During memory refresh, it will be driven high.	24mA
RAS[3:0]#	94 - 97	O	DRAM Row Address Strobe. The negate going edge of these signals are used to latch the row address on the MA lines to the DRAM banks. RAS[3] applies to bank 3, RAS[2] applies to bank2 and so on.	16mA
CAS[3:0]#	89 - 92	O	DRAM Column Address Strobe. The negate going edge of these signals are used to latch the column address on the MA lines to the DRAM banks and enable the DRAM banks' output buffer if it is a read cycle or store the data into DRAM banks if is a write cycle. CAS[3] applies to byte 3, CAS[2] applies to byte 2 and so on.	16mA

Note * Correction made after Rev. 07/05/96-2:01 PM

Signal Name	Pin Number	I/O	Description	Driving Capability
Hard Disk Interface signals:-				
AD[30]/HD3FX#/ P70CS#	107	I/O	During PCI cycle, it is the address/data line 30. During on-chip IDE access, it is the primary IDE chip select signal. During ISA cycle, it is the I/O port 70 chip select signal.	12mA
AD[29]/HD1FX#/ KBCS#	151	I/O	During PCI cycle, it is the address/data line 29. During on-chip IDE access, it is the primary IDE chip select signal. During ISA cycle, it is the chip select signal for the external keyboard controller.	12mA
AD[28]/HD37X#/ RTCCS#	108	I/O	During PCI cycle, it is the address/data line 28. During on-chip IDE access, it is the secondary IDE chip select signal. During ISA cycle, it is the chip select signal for the external real time clock.	12mA
AD[27]/HD17X#/ ROMCS#	150	I/O	During PCI cycle, it is the address/data line 27. During on-chip IDE access, it is the secondary IDE chip select signal. During ISA cycle, it is the chip select signal for the BIOS ROM.	12mA
AD[26:24]/HDA[2:0]	109, 149, 110	I/O	During PCI cycle, it is the address/data line 26:24. During on-chip IDE access, it is the IDE address line 2:0.	12mA
SA[15:0]/HDD[15:0]	165, 168, 170, 172, 173, 175 - 180, 183, 185, 188 - 190	I/O	For ISA cycle, these are the address line 15 to 0. For On-chip IDE cycle, these are data line 15 to 0 for the IDE port. External 10Kohm pull-up is required.	12mA
HDRD#	5	O	On-chip IDE Read. This is an active low output which enables data to be read from the IDE drive.	12mA
HDWE#	4	O	On-chip IDE write. This is an active low output which enables data to be written to the IDE drive.	12mA

Signal Name	Pin Number	I/O	Description	Driving Capability
L2 Cache Interface signals:-				
MA[11:4]/TA[7:0]	76 - 83	I/O	Memory Address line 11:4 or L2 cache Tag 7:0. When L2 cache is not enable, they are the memory address lines for DRAM interface. When L2 cache is enable, they are the multiplex bus for both cache tag data and DRAM address. Signal pin TOE# high represents they are carrying memory address information; TOE# low represents they are carrying tag data information.	24mA
TWE#	73	I/O	Cache Tag RAM Write enable. This is an active low signal which enables TAG data to be written to the external TAG RAM. It is asserted during L2 cache burst fill, or write hit clean cycle in 7+1 TAG mode.	12mA
COE#	35	O	Cache data Output Enable. It is always asserted in memory read cycle if L2 cache is enabled. If the cycle is not a cache hit cycle, it will be driven in-active at the following clock.	8mA
TOE#	74	O	Tag RAM Output Enable. This signal is use to enable the external TAG RAM output the TAG information on TA[7:0]. During DRAM access, it is driven high to prevent the bus conflict between TA and MA lines.	8mA
BWE#	34	O	Cache byte Write Enable. This is an active low signal which enables data to be written to the external cache.	8mA
GW#	36	O	Cache global Write. This is an active low signal which enables a 32-bit date to be written to the external cache.	8mA
ADV#	33	O	Cache Advance. This is an active low signal which instructs the burst cache to advance to next address.	8mA

Signal Name	Pin Number	I/O	Description	Driving Capability
MISC signals:-				
AD[30]/HD3FX#/ P70CS#	107	I/O	During PCI cycle, it is the address/data line 30. During on-chip IDE access, it is the primary IDE chip select signal. During ISA cycle, it is the I/O port 70 chip select signal.	12mA
AD[29]/HD1FX#/ KBCS#	151	I/O	During PCI cycle, it is the address/data line 29. During on-chip IDE access, it is the primary IDE chip select signal. During ISA cycle, it is the chip select signal for the external keyboard controller.	12mA
AD[28]/HD37X#/ RTCCS#	108	I/O	During PCI cycle, it is the address/data line 28. During on-chip IDE access, it is the secondary IDE chip select signal. During ISA cycle, it is the chip select signal for the external real time clock.	12mA
AD[27]/HD17X#/ ROMCS#	150	I/O	During PCI cycle, it is the address/data line 27. During on-chip IDE access, it is the secondary IDE chip select signal. During ISA cycle, it is the chip select signal for the BIOS ROM.	12mA
KBDATA/RC#	99	I/O	For internal keyboard controller, it is the keyboard data pin., an external 10Kohm pull-up resister is required. For external keyboard controller, it is the reset CPU" signal coming from external keyboard controller.	12mA
KBCLK/IRQ1	100	I/O	For internal keyboard controller, it is the keyboard clock pin, an external 10Kohm pull-up resister is required. For external keyboard controller, it is the output buffer fill" signal coming from external keyboard controller.	12mA
PWRGD	10	I	Power Good. This is an active a high signal which tells the system that the power supply is stable. C488 use this signal to reset the internal logic to a known state.	---
OSCIN	102	I	14.31818MHz input. This signal is used to drive the 8254 timer counter inside C488 to generate the speaker tone, refresh request signal, and DOS timer interrupt. It is also used to drive the timer counter of the power management unit.	---
HCLK	103	I	Host Clock. Same as CPU clock.	---
PCLK	104	I	PCI Clock. PCI controller clock, it should be the same as or one half of the HCLK. This clock must synchronize with the HCLK.	---
SLOWDWN#/ STPCLK#	2	O	This signal is used to control either the clock chip slow down or CPU stop clock.	4mA
SPKOUT	1	O	Speaker output. it drive the speaker through an external NPN transistor.	4mA

RTCLK/IRQ8#	3	I	Clock input for internal RTC, or alarm interrupt input for external RTC.	---
DOE#	72	O	Data Output Enable. This is an active low signal which enables data flow from host data bus to address bus. C488 uses this signal with AHOLD to multiplex the address and data bus onto A/D[31:2].	8mA
GND	11, 32, 52, 71, 88, 101, 115, 138, 153, 166, 181, 204			
VCC	18, 44, 75, 93, 129, 156, 186			

6. Configuration register
   Index port : 8-bit I/O port at 24H
   Data port: 8-bit I/O port at 28H

Index	Description
Memory control unit	
00H - 03H	Bank 0 - 3 configuration
	Bit 7-6 Access mode [ExD] 00 Non page mode/Nibble mode DRAM (default) 01 Fast page mode DRAM 10 EDO DRAM 11 Burst EDO RAM(not supported in this revision) Bit 5 Not used Bit 4-3 Page mode type [BxM]. (See Appendix 1 for details) 00 Page I (default) 01 Page II 10 Page III 11 Reserved Bit 2-0 Memory size 000 None (default for bank 1-3) 001 256Kbyte 010 512Kbyte 011 1Mbyte (default for bank 0) 100 2Mbyte 101 4Mbyte 110 8Mbyte 111 16Mbyte
04H	Shadow control 1, access control
	Bit 7 Segment 0A000H, 128Kbyte [S7] Bit 6 Segment 0C000H, 32Kbyte [S6] Bit 5 Segment 0C800H, 32Kbyte [S5] Bit 4 Segment 0D000H, 32Kbyte [S4] Bit 3 Segment 0D800H, 32Kbyte [S3] Bit 4 Segment 0E000H, 32Kbyte [S2] Bit 1 Segment 0E800H, 32Kbyte [S1] Bit 0 Segment 0F000H, 64Kbyte [S0] 0 Disable shadow RAM, all access will forward to PCI bus. (default) 1 Enable shadow RAM, access cycle will process by DRAM controller.
05H	Shadow control 2, write protected control
	Bit 7 Segment 0A000H, Read/write control [R7] Bit 6 Segment 0C000H, Read/write control [R6] Bit 5 Segment 0C800H, Read/write control [R5] Bit 4 Segment 0D000H, Read/write control [R4] Bit 3 Segment 0D800H, Read/write control [R3] Bit 2 Segment 0E000H, Read/write control [R2] Bit 1 Segment 0E800H, Read/write control [R1] Bit 0 Segment 0F000H, Read/write control [R0] 0 Disable write protect, host can read or write to this area. (default) 1 Enable write protect, host can only read from this area.
06H	384K relocation control
	Bit 7 Global control [RC7] 0 Disable relocation (default) 1 Enable relocation Bit 6 Segment 0A000H [RC6]

	Bit 5 Segment 0B000H [RC5] Bit 4 Segment 0C000H [RC4] Bit 3 Segment 0D000H [RC3] Bit 2 Segment 0E000H [RC2] Bit 1 Segment 0F000H [RC1] 0 Don t relocate this segment (default) 1 Relocate this segment Bit 0 Refresh address test [TESTRMA]. For proper operation, do not write "1" to this bit. 0 normal operation (default) 1 enable the address test
07H	Reserved

Index	Description
DRAM timing unit (See Appendix 2 for details)	
08H	Refresh timing
	Bit 7-6 Refresh period [REP] 00 15.6uS (default) 01 31.2uS 10 46.8uS 11 62.4uS Bit 5 Refresh mode [REFM]. Select CBR refresh mode will consume less power during refresh. 0 CBR refresh mode 1 RAS only refresh mode (default) Bit 4 Staggered refresh mode [STAGREF]. Enable this mode can low RAS switch noise, but 4 more clocks are needed in one refresh cycle. 0 Disable 1 Enable (default) Bit 3-2 CAS to RAS delay for CBR refresh, or MA setup timer for RAS only refresh. [CRD1]. 00 1 CLK for CBR refresh 2 CLKs for RAS only refresh 01 2 CLKs 3 CLKs 10 3 CLKs 4 CLKs 11 4 CLKs 5 CLKs (default) Bit 1 Refresh option [REFHOLD]. When external cache is used with DRAM refresh mode set to RAS only, This bit MUST be "0" in order to preserve the memory address line for refresh cycle. 0 Hold CPU during refresh 1 Select hidden refresh (default) Bit 0 Not used
09H	DRAM timing 1
	Bit 7-5 RAS pre-charge time [RP] 000 1 CLK 001 2 CLKs 010 3 CLKs 011 4 CLKs 100 5 CLKs 101 6 CLKs 110 7 CLKs 111 8 CLKs (default) Bit 4-3 Row address setup time [RS] 00 1 CLK 01 2 CLKs 10 3 CLKs 11 4 CLKs (default) Bit 2-0 RAS active to CAS active delay [RCD] 000 1 CLK 001 2 CLKs 010 3 CLKs 011 4 CLKs 100 5 CLKs 101 6 CLKs 110 7 CLKs 111 8 CLKs (default)
0AH	DRAM timing 2
	Bit 7-5 ROW address hold time [RAH]

	000 0.5 CLK 001 1 CLK 010 1.5 CLKs 011 2 CLKs 100 2.5 CLKs 101 3 CLKs 110 3.5 CLKs 111 4 CLKs (default) Bit 4-2 RAS active time [RW] 000 1 CLK 001 2 CLKs 010 3 CLKs 011 4 CLKs 100 5 CLKs 101 6 CLKs 110 7 CLKs 111 8 CLKs (default) Bit 1-0 Column address setup in page hit cycle [CS] 00 1 CLK 01 2 CLKs 10 3 CLKs 11 4 CLKs (default)
0BH	DRAM timing 3
	Bit 7-5 RAS hold time for non-page mode cycle [RH] 000 1 CLK 001 2 CLKs 010 3 CLKs 011 4 CLKs 100 5 CLKs 101 6 CLKs 110 7 CLKs 111 CAS width (default) Bit 4-3 CAS pre-charge time [CP] 00 1 CLK 01 2 CLKs 10 3 CLKs 11 4 CLKs Bit 2-0 Column address hold time [CAH] 000 1 CLK 001 2 CLKs 010 3 CLKs 011 4 CLKs 100 5 CLKs 101 6 CLKs 110 7 CLKs 111 8 CLKs (default)
0CH	DRAM timing 4
	Bit 7-5 Read cycle CAS active time for fast page mode [CA] 000 1 CLK 001 2 CLKs 010 3 CLKs 011 4 CLKs 100 5 CLKs 101 6 CLKs 110 7 CLKs

	111 8 CLKs (default) Bit 4-2 Read cycle CAS active time for EDO mode [EA] 000 1 CLK 001 2 CLKs 010 3 CLKs 011 4 CLKs 100 5 CLKs 101 6 CLKs 110 7 CLKs 111 8 CLKs (default) Bit 1 DRAM refresh test [TSTREF]. For Normal operation, this bit MUST be "0" 0 Normal operation (default) 1 Enable refresh request input from "CK#" pin Bit 0 EDO DRAM test [EDOTEST]. This bit is used to detect the present of EDO RAM, for normal operation, this bit MUST be "0". 0 Normal operation (default) 1 Enable test mode.
0DH	Write cycle control
	Bit 7 PCI/ISA master extra wait-state [WSM] 0 No wait-state added 1 Add one wait-state for read cycle (default) Bit 6 Write delay for PCI/ISA master access [WDM] 0 Normal 1 Delay by 1 CLK (default) Bit 5 Write delay for host access [WD] 0 Normal 1 Delay by 1 CLK (default) Bit 4-3 Write mode [EWM] 00 Same as read cycle (default) 01 Assert READY when CAS falls. 10 Assert READY when column address hold time reaches 11 Zero wait-state write cycle (Not supported yet) Bit 2 EDO output disable pulse width [WPW] 0 1 CLK (default) 1 0.5 CLK Bit 1-0 Write cycle CAS active time [WA] 00 1 CLK 01 2 CLKs 10 3 CLKs 11 4 CLKs (default)
0EH-0FH	Reserved

Index	Description
Level 2 cache control unit (See appendix 3)	
10H	Level 2 cache control 1
	Bit 7-6 Cache size [CS] 00 128Kbyte (default) 01 256Kbyte 10 512Kbyte 11 1Mbyte Bit 5-4 Cache mode [CC] 00 No cache (default) 01 Test cache RAM 10 Initialize cache RAM 11 Enable cache Bit 3-2 Cache hit/miss check point [CCKP] 00 End of T1 (default) 01 Middle of First T2 10 End of first T2 11 Reserved Bit 1 Cache hit wait state [CHW] 0 0 wait-state if possible (default) 1 1 wait-state Bit 0 Copy-back cycle data setup time [DSU] 0 1 CLK (default) 1 2 CLK
11H	Level 2 cache control 2
	Bit 7 Burst read cycle [BRC] 0 X,1,1,1 (default) 1 X,2,2,2 Bit 6 Burst write cycle [BWC] 0 X,1,1,1 (default) 1 X,2,2,2 Bit 5 Tag RAM option [TO] 0 7 bit + 1 dirty (default) 1 8 bit Bit 4 Burst type [LINEAR] 0 Interleave burst (default) 1 Linear burst Bit 3 PCD/CACHE# pin definition [P_C] 0 PCD pin (default) 1 CACHE# pin, support burst write Bit 2 Shadow RAM cacheability for level 2 cache [CASHW] 0 Not cacheable (default) 1 Cacheable Bit 1 Initialize cache option [ICO] 0 Fill cache data on any DRAM read cycle (default) 1 Fill cache data on burst read cycle Bit 0 Burst fill option [BFO] 0 Burst fill cache data on burst cycle only (default) 1 Burst fill cache data on any read cycle
12H	Level 2 cache control 3
	Bit 7 Cache type [PIPEBURST] 0 Flow-through burst cache. (default) 1 Pipeline burst cache.

	Bit 6 PCI/ISA master read wait-state control [RCWSM] 0 Add one wait-state .(default) 1 Same as CPU access. Bit 5 Delay DRAM cycle after Tag RAM write 0 No delay (default) 1 1 CLK delay (always select this option) Bit 4-1 Not used. Bit 0 Support Cyrix burst write back [CYRIXBW] 0 Not support or not Cyrix CPU (default) 1 Supported
13H-1Fh	Reserved

Index	Description
PCI bus control	
20H	Control 1
	Bit 7 Host to PCI fast back to back write [R_HP_FBB] 0 Enable. 1 Disable. (default) Bit 6 Host to PCI byte merged write cycle [R_HP_BM] 0 Enable. 1 Disable. (default) Bit 5 Host to PCI burst write cycle [R_HP_BUR] 0 Enable. 1 Disable. (default) Bit 4 Host to PCI buffer write cycle [R_HP_BUF] 0 Enable. 1 Disable. (default) Bit 3 PCI to host burst write/read cycle [R_PH_BUR] 0 Enable. 1 Disable. (default) Bit 2 CPU level 1 cache type. [R_CBCPU] 0 Write-through CPU 1 Write-back CPU (default) Bit 1-0 Not used.
21H	PCI Master time slot
	Bit 7-0 Time in 16 x PCI clock 0 Disable X (X+1) times 16 CLKs, where x is 1 to 255. Maximum is 4096 CLKs. When the time slot reaches the end, the corresponding GNT# line will be de-asserted to prompt the master to complete the transaction as far as possible. This timer will be reloaded when the REQ# is inactive.
22H	Top of memory low word
	Bit 7-0 Low word of memory size in 64Kbyte increment. 0 No RAM X Number of 64Kbye.
23H	Control 2 and Top of memory high word
	Bit 7 PCI parity control 0 Disable 1 Enable (default) Bit 6 ADS# output timing for PCI master cycle [R_SLOWOADS] 0 Fast timing decode 1 Medium timing decode (default) Bit 5 PCI master time slot counter pre-scalar. (R_SCALAR) 0 By pass the divided by 16 pre-scalar 1 Normal(default) Bit 4-0 High word of memory size
24H-5FH	Reserved

Index	Description
IDE control unit	
60H	Hardware configuration
	Bit 7 Global Pre-fetch control 0 Disable (default) 1 Enable Bit 6 Command de-assertion after IOCHRDY active. 0 2 CLKs (default) 1 3 CLKs Bit 5 Swapping port address. Normally port 1 responds to primary address and port 2 responds to secondary address. Setting this bit to "1" will swap these two address. 0 Normal (default) 1 Swapped Bit 4 Secondary address decode 0 Enable. (default) 1 Disable. Bit 3 Primary address decode 0 Enable (default) 1 Disable Bit 2 32-bit access mode 0 Disable (default) 1 Enable Bit 1 Posted-write cycle 0 Disable (default) 1 Enable Bit 0 Reserved
61H 66H 6BH 70H	Address setup for primary port master IDE. Address setup for primary port slave IDE. Address setup for secondary port master IDE. Address setup for secondary port slave IDE.
	Bit 7 Pre-fetch control for command 20H (for 61H only) 0 Enable (default) 1 Disable Bit 6 Pre-fetch control for command E4H (for 61H only) 0 Enable (default) 1 Disable Bit 5 Pre-fetch control for command C4H (for 61H only) 0 Enable (default) 1 Disable Bit 4 Reserved Bit 3-0 Setup time 0 16 CLKs (default) X X CLKs, where X = 1 to 15
62H 67H 6CH 71H	Recovery time for primary port master IDE. Recovery time for primary port slave IDE. Recovery time for secondary port master IDE. Recovery time for secondary port slave IDE.
	Bit 7-4 Write recovery time 0 16 CLKs (default) X X CLKs, where X = 1 to 15 Bit 3-0 Read recovery time 0 16 CLKs (default)

	X X CLKs, where X = 1 to 15
63H 68H 6DH 72H	16-bit access cycle active time for primary port master IDE. 16-bit access cycle active time for primary port slave IDE. 16-bit access cycle active time for secondary port master IDE. 16-bit access cycle active time for secondary port slave IDE.
	Bit 7-4 Write active time 0 16 CLKs (default) X X CLKs, where X = 1 to 15 Bit 3-0 Read active time 0 16 CLKs (default) X X CLKs, where X = 1 to 15
64H 69H 6EH 73H	8-bit read access active time for primary port master IDE. 8-bit read access active time for primary port slave IDE. 8-bit read access active time for secondary port master IDE. 8-bit read access active time for secondary port slave IDE.
	Bit 7 Reserved Bit 6 IOCHRDY control 0 Disable (default) 1 Enable. Bit 5-0 Read cycle active time 0 64 CLKs (default) X X CLKs, where X = 1 to 63
65H 6AH 6FH 74H	8-bit write access active time for primary port master IDE. 8-bit write access active time for primary port slave IDE. 8-bit write access active time for secondary port master IDE. 8-bit write access active time for secondary port slave IDE.
	Bit 7-6 Reserved Bit 5:0 Write cycle active time 0 64 CLKs (default) X X CLKs, where X = 1 to 63
75H-7FH	Reserved

Index	Description
Bus interface unit	
80H	Host address/data bus timing control
	Bit 7 System reset option [PULSE_RESETDRV] RESETDRV will driven active during CPU shutdown cycle. 0 CPURST and RESETDRV 1 CPURST only (default) Bit 6-4 Reserved. Bit 3 Enable delay RDY# signal [R_SLOWRDY] 0 No delay. 1 RDY# will be delayed by 1 clock during host read cycle. (default) Bit 2 Enable delay AHOLD signal [R_EN_AHOLDTIMING] 0 No delay 1 AHOLD will be delayed by 1 clock when level 2 cache is enabled. This bit has to be set when host clock speed greater than 40MHz. (default) Bit 1-0 Host address/data bus transfer speed [R_AHOLD_S] MSB control the begin of DOE# timing, LSB control the ending of AHOLD timing. 00 Fastest, suitable for clock speed ≤ 33MHz 01 Fast, suitable for clock speed 10 Slow, suitable for clock speed 11 Slowest, suitable for clock speed ≥ 50MHz (default)
81H-9FH	Reserved

Index	Description
Power Management unit	
0A0H	Doze timer. [DT] Doze timer is an 8-bit re-loadable down counter, it is reloaded when a activity happens. Activities are defined in an activity register. When the timer reaches zero, it can generate a interrupt or directly drive the SLOWDWN#/STPCLK# low.
	Bit 7-0 8-bit register, one second per unit. (default = 00H).
0A1H	Sleep timer. [ST] Sleep timer is an 8-bit re-loadable down counter, it is reloaded when a activity happens. It counts only when doze timer is ZERO.
	Bit 7-0 8-bit register, one minute per unit. (default = 00H)
0A2H	Activity register
	Bit 7 Hard disk port [HDD] I/O address 1F0H-1F7H, 170H-177H. Bit 6 Serial port [COM] I/O address 3F8H-3FFH, 2F8H-2FFH, 3E8H-3EFH, 2E8H-2EFH. Bit 5 Parallel port [LPT] I/O address 378H-37FH, 278H-27FH, 3BCH-3BFH. Bit 4 Floppy [FDD] I/O address 3F0H-3F7H. Bit 3 Keyboard controller [KBC] I/O address 60H. Bit 2 Display [VGA] I/O address 3B0H-3BBH, 3D0H-3DBH, 3C0H-3CFH. Write memory segment A000H-B000H. 0 Disable (default) 1 Enable Bit 1-0 Not used
0A3H	Control register 1
	Bit 7 Generates interrupt when doze timer reaches zero. Bit 6 Generates interrupt when sleep timer reaches zero. Bit 5 Generates interrupt when activity happens. Bit 4 Asserts SLOWDWN#/STPCLK# pin when doze timer reaches zero. Bit 3 Asserts SLOWDWN#/STPCLK# pin when sleep timer reaches zero. Bit 2 De-asserts SLOWDWN#/STPCLK# pin during interrupt service. Bit 1 De-asserts SLOWDWN#/STPCLK# pin during PCI/ISA master cycle. Bit 0 De-asserts SLOWDWN#/STPCLK# pin during DRAM refresh cycle. 0 Disable (default) 1 Enable
0A4H	Control register 2
	Bit 7 Set when doze timer generates a interrupt. Write a “1” to clear this flag. Bit 6 Set when sleep timer generates a interrupt. Write a “1” to clear this flag. Bit 5 Set when activity generates a interrupt. Write a “1” to clear this flag. Bit 4 Doze mode indicator. Set by power management handler, clear automatically when a activity happens. Bit 3 Set “1” to assert SLOWDWN#/STPCLK# pin. Reset automatically when a activity happens, or INTR activates. Bit 2 Not used. Bit 1 Activity control. Control the functioning of activity register. 0 Disable (default) 1 Enable Bit 0 Reload timer.

	0 No function 1 Reload all timers.
0A5H	Test register
	Bit 7 Enable test activity register output. 0 Normal operation. 1 Route the activity register output to SLOWDWN#/STPCLK# output. Bit 6-2 Not used. Bit 1-0 Select second divider pre-load register. [R] 00 Select low second divider. 01 Select middle second divider. 10 Select high second divider. 11 Select minute divider.
0A6H	Second divider pre-load register. 1. Low second divider. 8-bit register (default = 063H). 2. Middle second divider. 8-bit register (default = 07AH). 3. High second divider. 8-bit register (default = 0DAH). 4. Minute divider and test control.
	Bit 7-6 Bypass the carry chain of the four 8-bit divider. 00 Normal operation. 01 Bypass low second divider. 10 Bypass middle second divider 11 Reserved. Bit 5-0 6-bit minute divider (default = 3BH).
0A7H- 0BFH	Reserved

Index	Description
ISA control unit	
0C0H	Interrupt request signal mode 0
	Bit 7 IRQ15 Bit 6 IRQ14 Bit 5 IRQ13 Bit 4 IRQ12 Bit 3 IRQ11 Bit 2 IRQ10 Bit 1 IRQ9 Bit 0 IRQ8 0 Edge sensing (default) 1 Level sensing
0C1H	Interrupt request signal mode 1
	Bit 7 IRQ7 Bit 6 IRQ6 Bit 5 IRQ5 Bit 4 IRQ4 Bit 3 IRQ3 Bit 2 IRQ2 Bit 1 IRQ1 Bit 0 IRQ0 0 Edge sensing (default) 1 Level sensing
0C2H	PCI interrupt signal router 0
	Bit 7-4 INTA# is routed to X IRQ[X], where X = 0 to 15. Bit 3-0 INTB# is routed to X IRQ[X], where X = 0 to 15.
0C3H	PCI interrupt signal router 1
	Bit 7-4 INTC# is routed to X IRQ[X], where X = 0 to 15. Bit 3-0 INTD# is routed to X IRQ[X], where X = 0 to 15.
0C4H	ROMCS# decode control 0
	Bit 7-4 Reserved Bit 3 Segment D800H Bit 2 Segment D000H Bit 1 Segment C800H Bit 0 Segment C000H 0 Disable (default) 1 Enable.
0C5H	ROMCS# decode control 1
	Bit 7 Segment FFF E800H Bit 6 Segment FFF E000H Bit 5 Segment FFF D800H Bit 4 Segment FFF D000H Bit 3 Segment FFF C800H Bit 2 Segment FFF C000H Bit 1 Segment E800H Bit 0 Segment E000H 0 Disable (default)

	1 Enable.
0C6H	ISA timing control
	Bit 7 Bus cycle recovery 0 Disable (default) 1 Enable Bit 6 Fast DMA cycle 0 Disable (default) 1 Enable Bit 5 Extend DMA read command 0 Disable (default) 1 Enable. Bit 4 ROMCS decode in CPU memory write cycle 0 Disable (default) 1 Enable. Bit 3 Display type 0 CGA display (default) 1 MDA display Bit 2 PERR# function control 0 No function (default) 1 Assertion of PERR# will generate NMI Bit 1-0 Power manage interrupt routing 00 None (default) 01 NMI 10 IRQ10 11 IRQ12
0C7H	Switch status (Read only)
	Bit 7-4 Reserved Bit 3-0 Hardware configuration input from CFG[3:0]. CFG[1] : “1” means using internal RTC. CFG[0] : “1” means using internal KBC.
0CEH	Test register of KBC (Write only, for testing purpose only)
	Bit 7-3 Reserved Bit 2-0 KBC test pins.
0CFH	Test register of IPC (Write only, for testing purpose only)
	Bit 7 IPC command width 0 Normal (default) 1 One OSC. Bit 6-5 Reserved Bit 4 DMAC test pin Bit 3-0 RTC test pins.

7. DC electrical characteristics

(V_{CC} = 5V ±5%, T_A = 0 to 70°C)

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	TTL interface		2.0		V
	TTL schmitt trigger		2.4		
	CMOS interface		0.7V_{CC}		
	CMOS schmitt trigger		4.0		
V_{IL}	TTL interface			0.8	
	TTL schmitt trigger			0.6	
	CMOS interface			0.3V_{DD}	
	CMOS schmitt trigger			1.0	
I_{IH}	Input high current	V_{IN} = V_{DD}	-10	10	µA
	Input with pull-down		10	200	
I_{IL}	Input low current	V_{IN} = G_{ND}	-10	10	µA
	Input with pull-up		-200	-10	
V_{OH}	Type B1, B2, B4, B8, B12, B16, B20, B24[NOTE1]	I_{OH} = -1µA	V_{DD} - 0.05		V
	Type B1	I_{OH} = -1mA	2.4		
	Type B2	I_{OH} = -2mA	2.4		
	Type B4	I_{OH} = -4mA	2.4		
	Type B8	I_{OH} = -8mA	2.4		
	Type B12	I_{OH} = -12mA	2.4		
	Type B16	I_{OH} = -16mA	2.4		
	Type B20	I_{OH} = -20mA	2.4		
	Type B24	I_{OH} = -24mA	2.4		
V_{OL}	Type B1, B2, B4, B8, B12, B16, B20, B24[NOTE1]	I_{OL} = -1µA		0.05	V
	Type B1	I_{OL} = -1mA		0.4	
	Type B2	I_{OL} = -2mA		0.4	
	Type B4	I_{OL} = -4mA		0.4	
	Type B8	I_{OL} = -8mA		0.4	
	Type B12	I_{OL} = -12mA		0.4	
	Type B16	I_{OL} = -16mA		0.4	
	Type B20	I_{OL} = -20mA		0.4	
	Type B24	I_{OL} = -24mA		0.4	
I_{OZ}	Tri-state output leakage current	V_{OUT} = G_{ND} or V_{CC}	-10	10	µA
I_{DD}	Quiescent supply current	V_{IN} = G_{ND} or V_{CC}		100	µA

Notes:
1. Type B1 means 1mA output driver cells and type B24 means 24mA output driver cells.

Maximum ratings

Absolute maximum ratings

Symbol	Parameter	Range	Unit
V_{CC}	DC supply voltage	-0.3 to 7	V
V_{IN}	DC input voltage	-0.3 to V_{CC}+0.3	V

I_{IN}	DC input current	±10	mA
T_{STG}	Storage temperature	-40 to 125	°C

Recommended operating conditions

Symbol	Parameter	Range	Unit
V_{CC}	DC supply voltage	4.5 to 5.5	V
T_A	Commercial temperature	0 to 70	°C
	Industrial temperature	-40 to 85	°C

Appendix 1. MA address mapping

Type	Page/ (Refresh)	MA	0	1	2	3	4	5	6	7	8	9	10	11
256K	Page I (512b)	Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10			
		Row	A11	A12	A13	A14	A15	A16	A17	A18	A19			
	Page II (1K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9				
		Row	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19		
512K (1K)		Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10			
		Row	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20		
1M	Page I (1K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11		
		Row	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21		
	Page II (2K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10			
		Row	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	
	Page III (4K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9				
		Row	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21
2M	Page I (2K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11		
		Row	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	
	Page II (4K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10			
		Row	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A22	A22
4M	Page I (2K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	
		Row	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	
	Page II (4K)	Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11		
		Row	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23
8M (4K)		Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	
		Row	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24
16M (4K)		Col.	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13
		Row	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25

Appendix 2. DRAM timing parameter

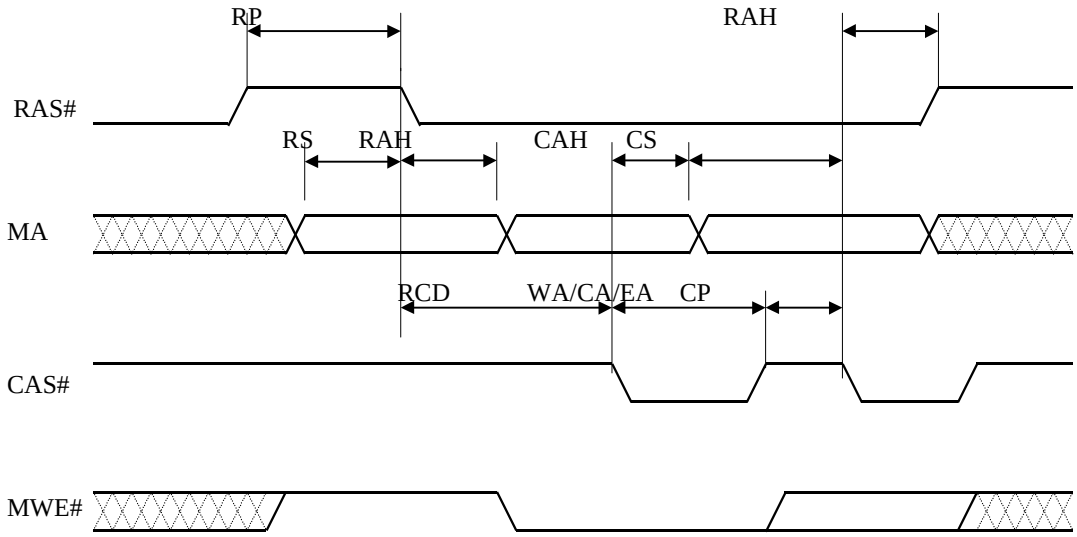


Figure 1. Page mode DRAM timing.

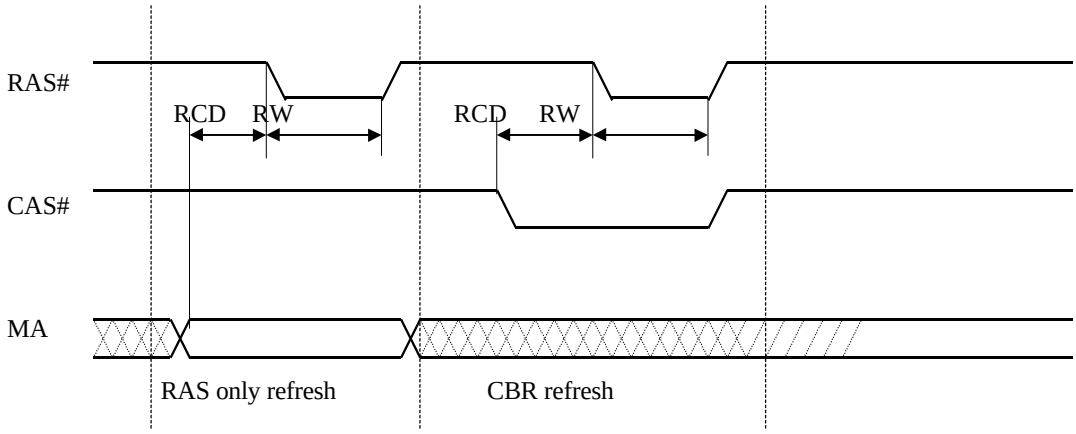


Figure 2. Refresh timing

Appendix 3. Tag address mapping

Cache size	TA0	TA1	TA2	TA3	TA4	TA5	TA6	TA7 (8 bit tag)	Cacheable Area
128K	A17	A18	A19	A20	A21	A22	A23	Dirty(A24)	16M(32M)
256K	A24	A18	A19	A20	A21	A22	A23	Dirty(A25)	32M(64M)
512K	A24	A25	A19	A20	A21	A22	A23	Dirty(A26)	64M(128M)
1M	A24	A25	A26	A20	A21	A22	A23	Dirty(A27)	128M(256M)

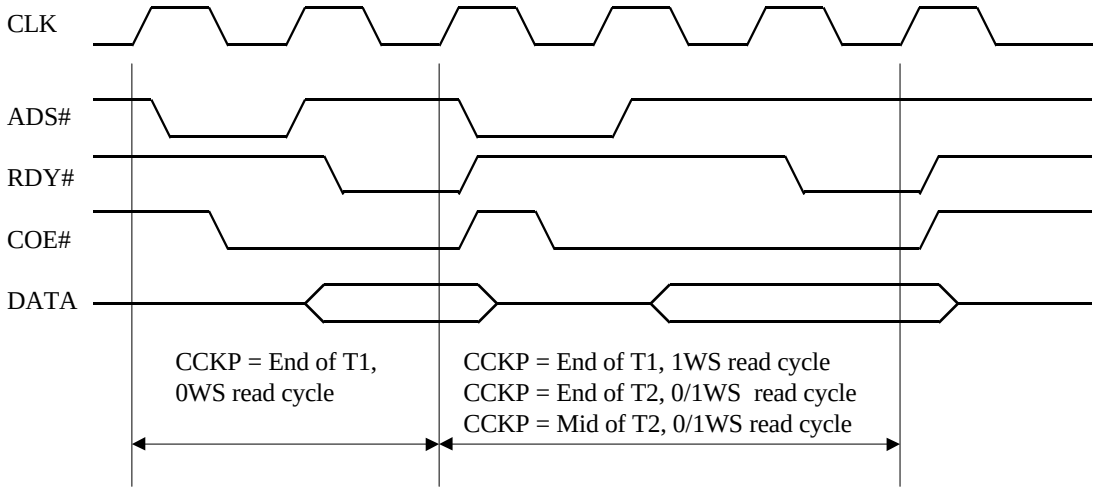


Figure 3. Flow through burst Cache read timing.

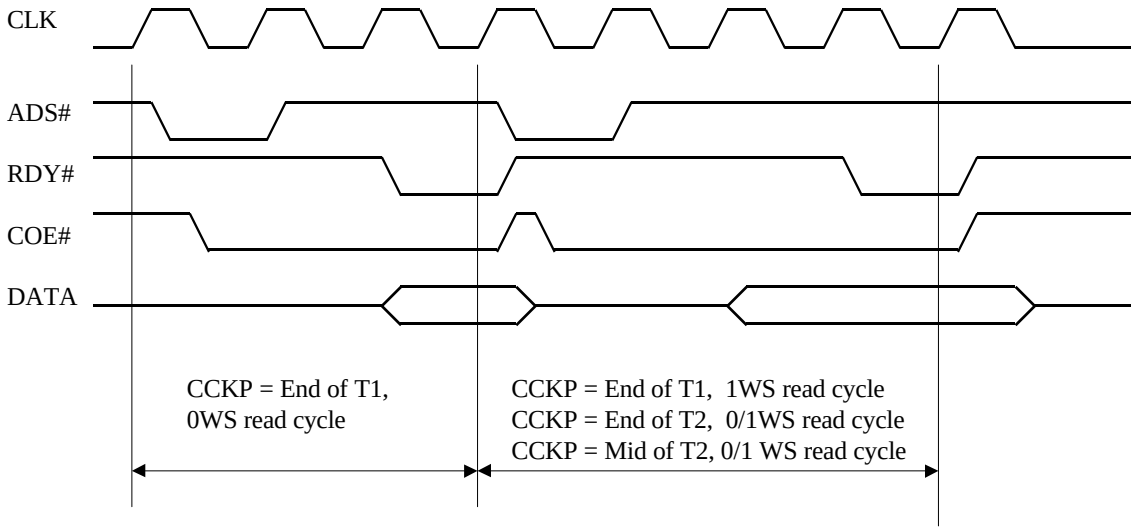
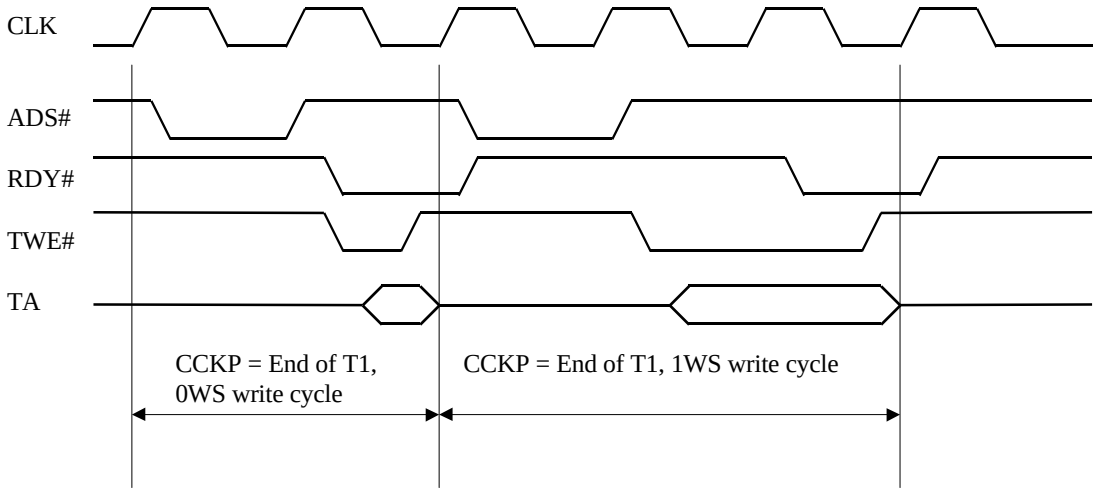
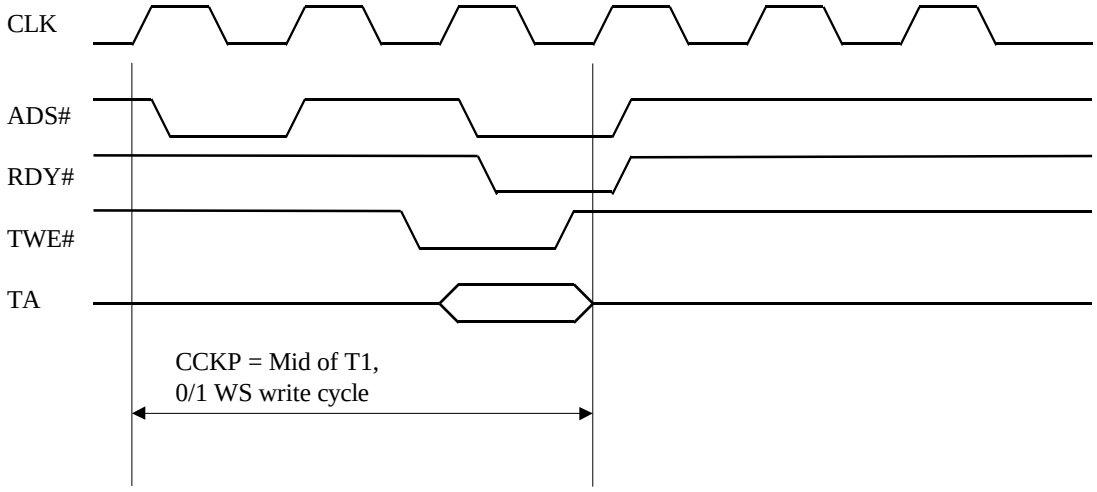


Figure 4. Pipeline burst cache read timing.


CLK
ADS#
RDY#
TWE#
TA
CCKP = End of T1,
0WS write cycle
CCKP = End of T1, 1WS write cycle


CLK
ADS#
RDY#
TWE#
TA
CCKP = Mid of T1,
0/1 WS write cycle

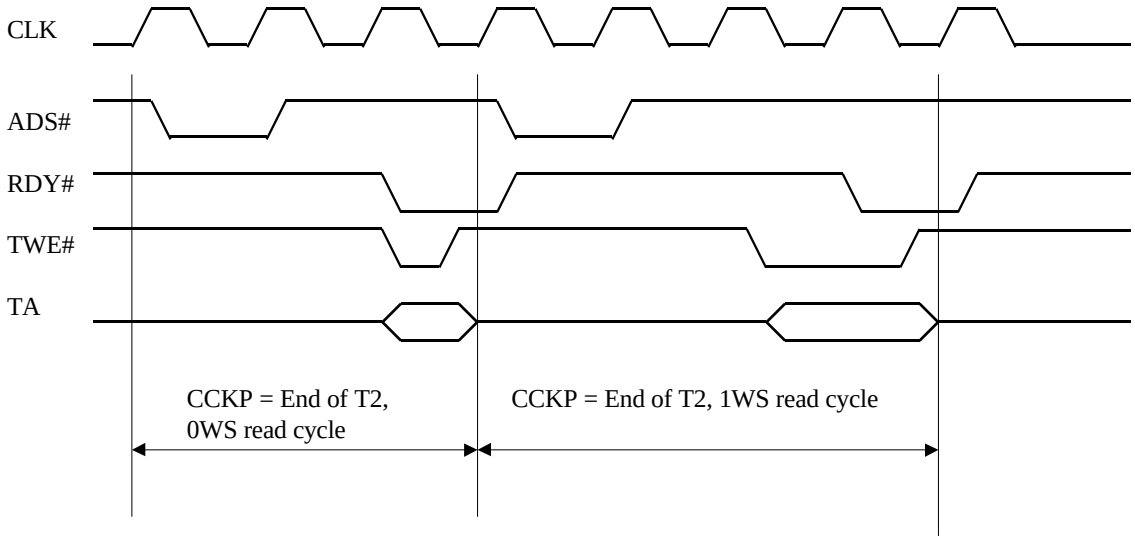

CLK
ADS#
RDY#
TWE#
TA
CCKP = End of T2,
0WS read cycle
CCKP = End of T2, 1WS read cycle

Figure 5. Cache tag write timing.

Appendix 4. Power management interrupt programming guide

Example 1: When doze timer expires, stop the CPU clock. When sleep timer expires, blank the display.

```
Initialization begin
    Program both timers.
    Select activity.
    Enable de-assertion of STPCLK# pin during interrupt service.
    Clear interrupt flag.
    Enable timer generate interrupt.
    Reload timer.
end


begin (SMI)
   If (DOZE = 0, bit 4 of index 0A4H) begin
      if doze generate interrupt begin
         set DOZE = 1
         send EOI to interrupt controller
         while (DOZE = 1) begin
            set STPCLK# pin to low
            halt
         end
         enable display if required
         return
      end
   end
   else begin
      if sleep generate interrupt begin
         set STPCLK# pin to high
         disable activity
         blank display
         enable activity
         send EOI
         return
      end
   else
      send EOI
      return
   end
end
```