ACC 5810
Micro Channel Interface Chip

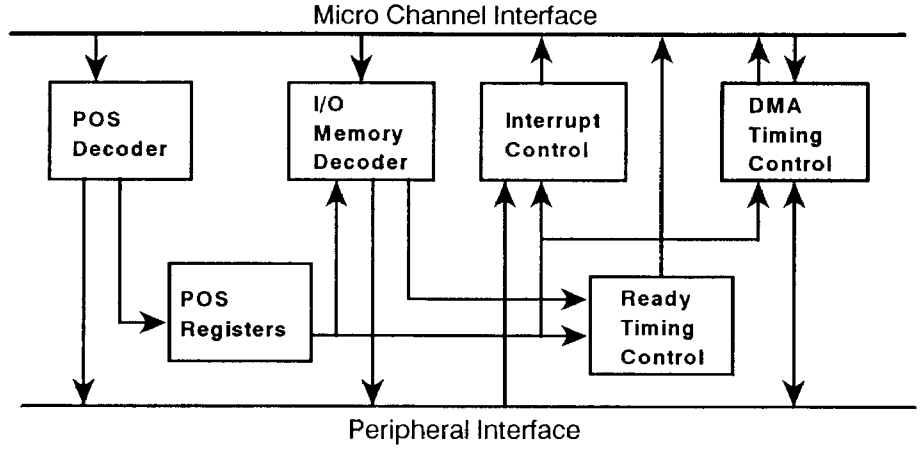
The ACC 5810 is a high performance CMOS Micro Channel* interface chip that allows designers to build a Micro Channel compatible add-in adapter in a short time. The ACC 5810 replaces 15 SSI/MSI in a typical Micro Channel adapter. The ACC 5810 supports I/O slave, memory slave and DMA slave adapters with interrupt sharing. The flexible predefined POS configuration simplifies and reduces the amount of logic required to design a Micro Channel compatible application circuit.

Features

- 100% compliance with the implementation of IBM PS/2* Micro Channel Interface
- Optional predefined POS registers reduce the required Micro Channel interfacing logic
- Supports up to 256 memory starting addresses
- Supports up to 256 I/O locations
- Supports up to 16 arbitration requests from a peripheral
- Supports burst DMA transfer
- Implements level-sensitive interrupt sharing
- Supports two sets of interrupt sharing logic, each set supports four interrupt sources
- Flexible I/O and memory mapping support
- Supports POS port decode logic and handshaking
- Supports channel check
- Supports 4 programmable wait states
- 60-pin PFP package

* Trademarks of International Business Machines

Block Diagram



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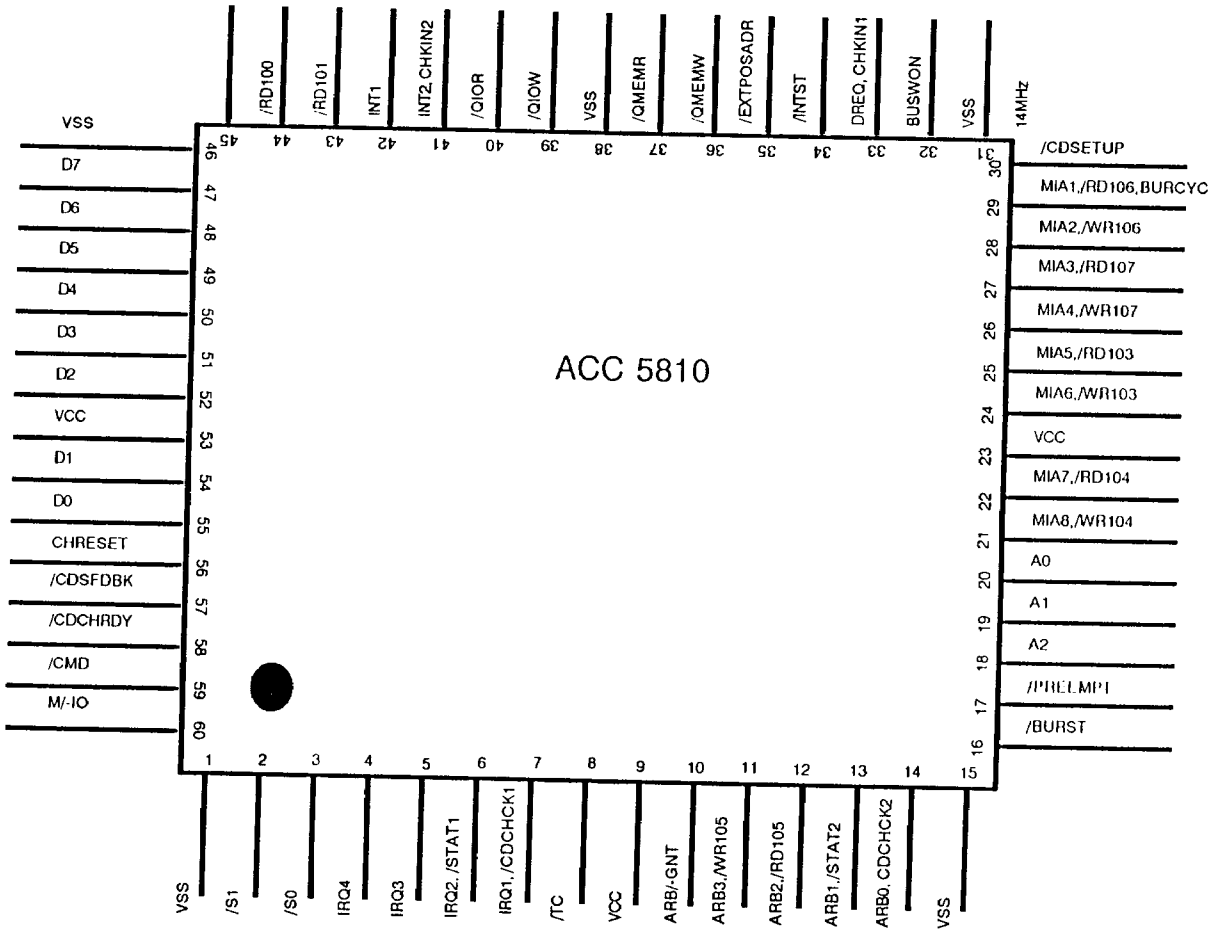
Pin Diagram


ACC 5810
VSS
D7
D6
D5
D4
D3
D2
VCC
D1
D0
CHRESET
/CDSFDBK
/CDCHRDY
/CMD
M/-IO
/RD100
/RD101
INT1
INT2,CHKIN2
/QIOR
/QIOW
VSS
/QMEMR
/QMEMW
/EXTPOSADR
/INTST
DREQ,CHKIN1
BUSWON
VSS
14MHz
/CDSETUP
MIA1,/RD106,BURCYC
MIA2,/WR106
MIA3,/RD107
MIA4,/WR107
MIA5,/RD103
MIA6,/WR103
VCC
MIA7,/RD104
MIA8,/WR104
A0
A1
A2
/PREEMPT
/BURST
VSS
/S1
/S0
IRQ4
IRQ3
IRQ2,/STAT1
IRQ1,/CDCHCK1
/TC
VCC
ARB/-GNT
ARB3,/WR105
ARB2,/RD105
ARB1,/STAT2
ARB0, CDCHCK2
VSS

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/S1	2	I	Status bit 1 from the Micro Channel bus interface. With M/-IO and /S0, this signal identifies the cycle type in progress, high for write cycle, low for read cycle.
/S0	3	I	Status bit 0 from the Micro Channel bus interface. With M/-IO and /S1, this signal identifies the cycle type in progress, high for read cycle, low for write cycle.
IRQ4 IRQ3 IRQ2 IRQ1	4 5 6* 7*	O	Generates interrupt request to the Micro Channel bus. It can be mapped through the Apapter Description File to drive one of the level sensitive interrupt signals low (/IRQ 3-7, 9-12,14,15). This output is an open collector.
/STAT1	6*	I	Channel Check status indicator. When set to 0, this pin indicates that the adapter has additional status information available at POS 106 and 107. This pin is valid only when channel check is active and DMA is deselected.
/CDCHCK1	7*	O	Channel Check. This signal flags a serious error and requests a nonmaskable interrupt. Output is an open collector. This pin is valid only when DMA is deselected.
/TC	8	I	Terminal count. This signal indicates that the DMA has completed data transfer.
ARB/-GNT	10	I	Arbitrate/-Grant. This signal identifies a DMA arbitration cycle or DMA grant cycle; High means an arbitration cycle is in process, low means the channel has been granted.
ARB3 ARB2 ARB1 ARB0	11* 12* 13* 14*	I/O	In DMA mode, this signals goes directly to Micro Channel pin ARB3. With ARB2, ARB1, and ARB0, these four outputs represent an encoded arbitration bus priority level from 0 to Hex F. When ARB/-GNT is high, a DMA request is pending. The ACC 5810 drives and monitors the bidirectional arbitration lines. If the value on the bus matches the arbitration level of the ACC 5810 (determined by POS 105 bits 0-3), the adapter has won the bus. This signal is an open collector.
/WR105	11*	O	Write POS 105. This signal is valid only when external POS 105 is selected and DMA is deselected.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/RD105	13*	O	Read POS 105. This signal is valid only when external POS 105 is selected and DMA is deselected.
/STAT2	13*	I	Channel Check status indicator. When set to 0, this pin indicates that the adapter has additional status information available at POS 106 and 107. This pin is valid only when channel check is active and DMA is deselected.
/CDCHCK2	14*	O	Channel Check. This signal indicates a serious error and requests a nonmaskable interrupt. Open Collector. This pin is valid only when DMA is deselected.
/BURST	16	O	Active low burst DMA cycle output. Open Collector.
/PREEMPT	17	I/O	This pin connects directly to the Micro Channel / Preempt pin. When the adapter requests the bus, this line is driven low. It raises the preempt after it detects that it has won the bus. Open collector for output.
A2 A1 A0	18 19 20	I	Address bit. Input signal from the Micro Channel bus to select the POS registers in the ACC 5810.
MIA8 MIA7 MIA6 MIA5 MIA4 MIA3 MIA2 MIA1	21* 22* 24* 25* 26* 27* 28* 29*	I	Input signal for the I/O or memory address relocation inside the ACC 5810. The signal is compared to POS 103 or POS 104. The address is qualified and output is QIOR, QIOW, QMEMW, or QMEMR.
/WR104	21*	O	Active low write strobe to write data to external register 104 on the adapter. This pin is valid only when external POS 104 is activated.
/RD104	22*	O	Active low read strobe to read data from external register 104 on the adapter. This pin is valid only when external POS 104 is activated.
/WR103	24*	O	Active low write strobe to write data to external register 103 on the adapter. This pin is valid only when external POS 103 is activated.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/RD103	25*	O	Active low read strobe to read data from external register 103 on the adapter. This pin is valid only when external POS 103 is activated.
/WR107	26*	O	Active low write strobe to write data to external register 107 on the adapter. This pin is valid only when external POS 107 is activated
/RD107	27*	O	Active low read strobe to read data from external register 107 on the adapter. This pin is valid only when external POS 107 is activated
/WR106	28*	O	Active low write strobe to write data to external register 106 on the adapter. This pin is valid only when external POS 106 is activated
/RD106	29*	O	Active low read strobe to read data from external register 106 on the adapter. This pin is valid only when external POS 106 is activated
BUSCYC	29*	O	Burst Cycle. This ouput signal notifies the adapter if a burst cycle is finished. During the burst transfer DMA cycle, this signal is high. When the POS 104 fairness bit is 0, this signal matches the BUSWON signal.
/CDSETUP	30	I	This line connects directly to the Micro Channel /CDSETUP pin. During the setup cycle, this line is driven low by the system board logic and POS registers 100-107 are accessed. The system reads the PS/2 adapter card's ID and writes initialization bytes.
14MHz	31	I	14 MHz clock. This signal generates asynchronous /CDCHRDY signals for the ACC 5810.
BUSWON	33	O	This signal indicates that the adapter has won the Micro Channel bus (ARB0-3 match POS 105 bits 0-3 and ARB/-GNT is low). In single transfer mode, this signal can be used as the DACK signal for the AT bus.
CHKIN1	34*	I	Channel check request input. This pin has a low to high edge trigger and is valid only when DMA is deselected.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
DREQ	34*	I	DMA Request. This signal originates from the adapter to trigger the ACC 5810 to send a preempt signal requesting the Micro Channel bus and compete in the arbitration cycle for DMA transfer. This signal has a low to high edge trigger.
/INTST	35	I	Interrupt Status. This signal is decoded from the adapter. It determines which I/O port address resets the interrupt pending latch inside the ACC 5810 during a write cycle, or reads the interrupt status latch during a read cycle.
/EXTPOSADR	36	I	External POS Address. This signal from the adapter qualifies the I/O or memory address, or informs the ACC 5810 to send 103-107 R/W signals to the adapter.
/QMEMW	37	O	Qualified memory write signal to the adapter. This signal is active when /S1 is high, /S0 is low, M/-IO is high, /EXPOSADR is low, POS 102 bit 0 is 1, and MIA1-8 match POS 104 bits 0-7.
/QMEMR	38	O	Qualified memory read signal to the adapter. This signal is active when /S1 is low, /S0 is high, M/-IO is high, /EXPOSADR is low, POS 102 bit 0 is 1, and MIA1-8 match POS 104 bits 0-7.
/QIOW	40	O	Qualified I/O write signal to the adapter. This signal is active when /S1 is high, /S0 is low, M/-IO is low, /EXPOSADR is low, POS 102 bit 0 is 1, and MIA1-8 match POS 104 bits 0-7.
/QIOR	41	O	Qualified I/O read signal to the adapter. This signal is active when /S1 is low, /S0 is high, M/-IO is low, /EXPOSADR is low, POS 102 bit 0 is 1, and MIA1-8 match POS 104 bits 0-7.
INT2 INT1	42* 43	I	Edge triggered interrupt request lines from the adapter to inform the ACC 5810 to send signals IRQ1-4 to the Micro Channel Bus. This signal has a low to high edge trigger.
CHKIN2	42*	I	Channel check request 2. This pin is valid only when INT2 is deselected. This signal has a low to high edge trigger.

Pin Descriptions

Symbol	Pin	I/O	Pin Description
/RD101	44	O	Active low read strobe to read register 101 from the adapter to the data bus. Register 101 corresponds to the high byte of the 16 bit CARD ID.
/RD100	45	O	Active low read strobe to read register 100 from the adapter to the data bus. Register 100 corresponds to the low byte of the 16 bit CARD ID.
D7 D6 D5 D4 D3 D2 D1 D0	47 48 49 50 51 52 54 55	I/O	Data bus bit. Bidirectional data bus which transfers data between the Micro Channel bus and the POS registers. This signal must be isolated from the Micro Channel with a transceiver.
CHRESET	56	I	Channel Reset. This signal from the Micro Channel bus resets the POS registers.
/CDSFDBK	57	O	Sends the Card Selected Feedback signal to the Micro Channel requesting acknowlegment of the presence of the adapter at a specified address qualified by the ACC 5810.
/CDCHRDY	58	O	Channel Ready. This line is used by a memory or an I/O slave to provide a extended cycle time to complete a channel operation. The extended cycle time can be programmed by POS 103 bit 0-3. This output is a standard totem-pole output which connects directly to the Micro Channel CDCHRDY pin. When CDCHRDY is used, S0 and S1 must be qualified in the I/O or memory decoder.
/CMD	59	I	Command. This signal is from the Micro Channel bus. It determines when data is valid on the data bus and uses its negative edge to latch the address line on the bus.
M/-IO	60	I	Memory/-Input Output. This signal from the Micro Channel bus determines if a memory cycle or an I/O cycle is in progress. High for memory cycles, low for I/O cycles.
VCC	9, 23, 53		+5 volt supply
VSS	1, 15, 32, 39, 46		Ground

Functional Description

ACC 5810 provides the following major functions:

- POS Decoder
- POS Registers
- I/O Memory Relocator
- Interrupt Control
- Ready Timing Control
- DMA Timing Control

POS Decoder

The ACC 5810 POS decoder decodes /CDSETUP, A0, A1, A2, /CMD, /S0, and /S1. It sends out /RD100, /RD101, /RD103 through /RD107 and /WR103 through /WR107. /RD100 and /RD101 are read strobes to gate ID bytes to the data bus. Figure 1 is an example of ID support implementation with a 74LS244.

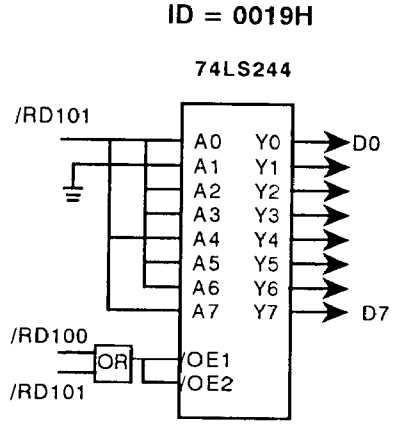
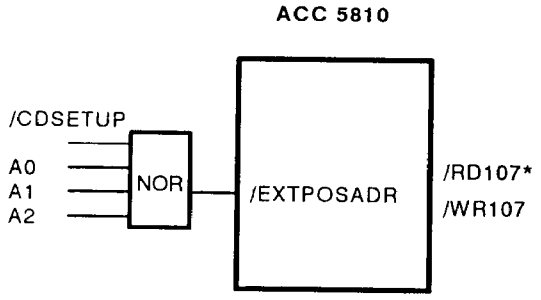


Figure 1 ID Support with a 74LS244

/RD103 through /RD107 and /WR103 through /WR107 are control signals for POS registers 103-107 inside ACC 5810. /RD103 through /RD107 and /WR103 through /WR107 can be accessed from the ACC 5810 when /EXTPOSADR is low. Figure 2 is an example of an external POS register R/W strobe.



* If external POS 107 is deselected, the pins for /RD107, /WR107 are MIA3 and MIA4.

Figure 2 R/W102-107 as Control Signals

POS Registers

The POS (programmable option select) registers are predefined in the ACC 5810. The POS registers can be disabled when /EXTPOSADR is low.

The POS registers inside the ACC 5810. accept system configuration data. Functions such as I/O or memory relocation, interrupt, memory range, extended cycle, DMA level, burst can all be selected through the POS registers.

The POS Register Definition Table lists predefined registers. Some of the POS register bits were originally defined by IBM namely POS102 Bit 0, POS105 Bit 7 and Bit 6. Other POS registers bits are defined by the ACC 5810.

POS Register Definitions

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POS 102	INT12	INT11	BURST	INT2DSL	DMADSL	INTSEL	RDYSEL	CDEN
POS 103	IO8	IO7	IO6	IO5	IO4	IO3 (When RDYSEL = 0)	IO2	IO1
					MY2	MY1 (When RDYSEL = 1)	IY2	IY1
POS 104	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1
	(When BURST = 0)							
	MS4 (When DMADSL = 1 & BURST = 1)	MS3	MS2	MS1				
	FAIR (When DMADSL = 0 & BURST = 1)	B3	B2	B1				
POS 105	CHCK	STAT	INT22 (When INT2DSL =0)	INT21	ARB3 (When DMADSL=0)	ARB2	ARB1	ARB0
			MCAS (When INT2DSL =1)	ICAS	MS8 (When DMADSL = 1 & BURST = 0)	MS7	MS6	MS5

POS102 (Status Registers)

POS102 is predefined as a status register by the ACC 5810.

Bit 0: CDEN (Card Enable)

The CDEN bit controls the /QIOR, /QIOW, /QMEMR, and /QMEMW.
If CDEN = 1, these signals are active.
If CDEN = 0, these signals are inactive.

Bit 1: RDYSEL (RDY Signal Select)

RDYSEL is a control bit. When RDYSEL is high, /CDCHRDY is an external extended cycle depending on programmable wait state number register 103 Bit 0-3. When RDYSEL is low, /CDCHRDY is always inactive.

Bit 2: INTSEL (Interrupt Select)

When INTSEL is high, IRQ1-4 are in mode 1. In mode 1, the interrupt request line terminates its request by 14 MHz OSC. When INTSEL is low, the interrupt is in mode 0. In mode 0, the interrupt request line terminates by write 03 to interrupt status port.

Bit 3: DMADSL (DMA Deselect)

When DMADSL is low, DMA circuits inside the ACC 5810 are enabled. When DMADSL is high, the DMA circuits inside the ACC 5810 are disabled.

Bit 4: INT2DSL (INT2 Deselect)

When INT2DSL is high, the second interrupt set is disabled and used as a non-maskable interrupt. When INT2DSL is low, the second interrupt set is enabled.

Bit 5: BURST

When BURST is high, the DMA circuit operates in burst mode if DMADSL is low. When BURST is low, the DMA circuit operates in single transfer mode if DMADSL is low.

If DMADSL is high, BURST serves as a control bit for the POS registers. Refer to the table on Page 12.

Bit 6-7: INT11, INT12 (INT Mapping)

These bits map INT1 to one of the IRQ1-4 signals.

POS103 (I/O Relocator Register)

Bit 3-0: IO4-IO1 (when RDYSEL =0)
MY2, MY1, IY2, IY1 (when RDYSEL= 1)

IO4-1 are inputs for the I/O relocator. They correspond to MIA4-MIA1.

Bits MY2 and MY1 control the extended memory cycle.

MY2,MY1	00	01	10	11
/CDCHRDY TIME	12 T_{OSC}	8 T_{OSC}	4 T_{OSC}	synchonous extended cycle

T_{OSC}: period for 14MHz OSC

Bits IY2 and IY1 control the I/O extended cycle. (Refer to the POS register table.) Only the qualified memory or I/O sends out the extended cycle signal, /CDCHRDY.

IY2,IY1	00	01	10	11
/CDCHRDY TIME	12 T_{OSC}	8 T_{OSC}	4 T_{OSC}	synchonous extended cycle

T_{OSC}: period for 14MHz OSC

Bit 7-4: IO8-IO5

Signals IO8-5 are inputs for the I/O relocator, corresponding to MIA8-MIA5. They generate qualified I/O addresses.

POS104 (Memory Relocator Register)

Bit 3-0: MA4-MA1

MA4 through MA1 are inputs for the memory relocator corresponding with MIA4-MIA1. They generate qualified memory addresses for the ACC 5810.

Bit 7-4: MA8-MA5 (when Burst =0)
MS4-MS1 (when Burst =1, DMADSL =1)
FAIR, B3, B2, B1 (when Burst =1, DMADSL =0)

MA8-MA5 are inputs to the memory relocator corresponding to MIA8-MIA5 to qualify the memory address.

MS4-MS1 bits control the comparator by controlling MA4-MA1 and MIA4-MIA1 inside the memory relocator. For example, if MS1 is high, the first bit of the 4-bit comparator is disabled, then the comparator functions as a 3-bit comparator. MIA1 and MA1 have no further meaning to the memory relocator. MS2-4 have the same function as MS1 but use different bits in the comparator.

When the fairness bit is high, burst DMA is in fairness mode. When the fairness bit is low, burst DMA is in regular mode. Bits B3-B1 select the DMA transfer number in each DMA burst request.

B3B2B1	000	001	010	011	100	101	110	111
DMA Burst Transfer Number	1	8	16	24	32	40	48	56

POS105

Bit 3-0: ARB3-ARB0 (When DMADSL =0)
MS8-MS5 (When DMADSL =1, BURST = 0)

Bits ARB3-ARB0 map DREQ to one of sixteen arbitration levels.

Bits MS8-MS5 control the comparator with MA8-MA5 and MIA8-MIA5 inside the memory relocator. The function of these bits is identical to bits MS4-MS1.

Bits 5-4:
INT22, INT21 (When INT2DSL =0)
MCAS, ICAS (When INT2DSL =1)

Bits INT22 and INT21 map INT2 to one of the IRQ1-4 signals.

When MCAS is 0, the memory relocator serves as two sets of 4-bit relocators (MA1-MA4, nd MA5-MA8). When the MCAS bit is 1, the memory relocator serves as one 8-bit relocator (MA1-MA8).

When ICAS is 0, the I/O relocator serves as two sets of 4-bit relocators (IO1-IO4, and IO5-IO8). When ICAS is 1, the I/O relocator serves as one 8-bit relocator (IO1-IO8).

Bit 6: STAT (Channel Check Status)

When STAT is set to 0, channel status is available using POS bytes 106 and 107 hex. When STAT is set to 1, status is not available.

Bit 7: CHCK (Channel Check Active)

This check bit reports the adapter CHCK as active.

I/O Memory Relocator

The I/O memory relocator relocates I/O and memory addresses to avoid system configuration conflict. See Figures 3 and 4.

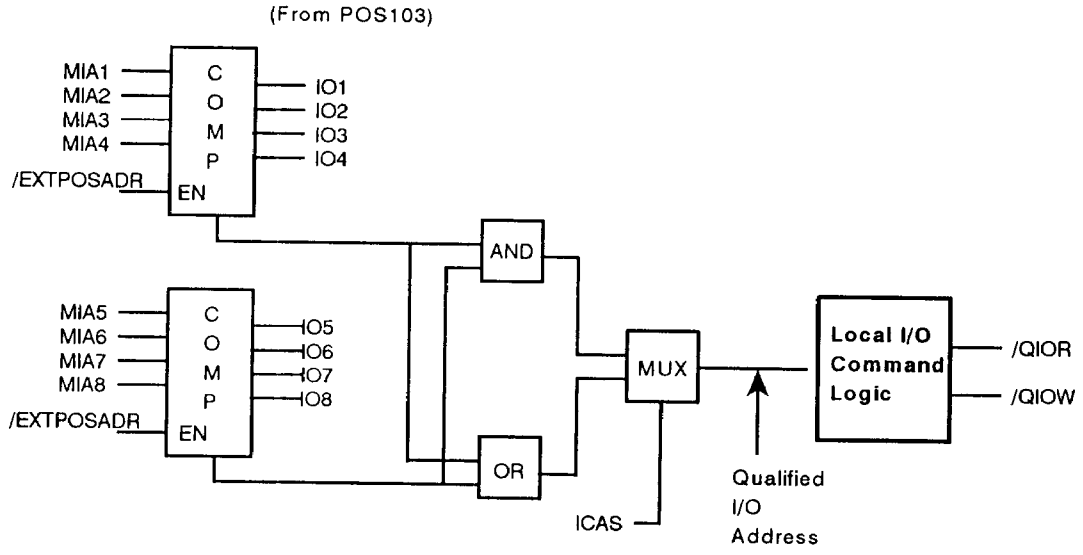


Figure 3 I/O Relocation Map

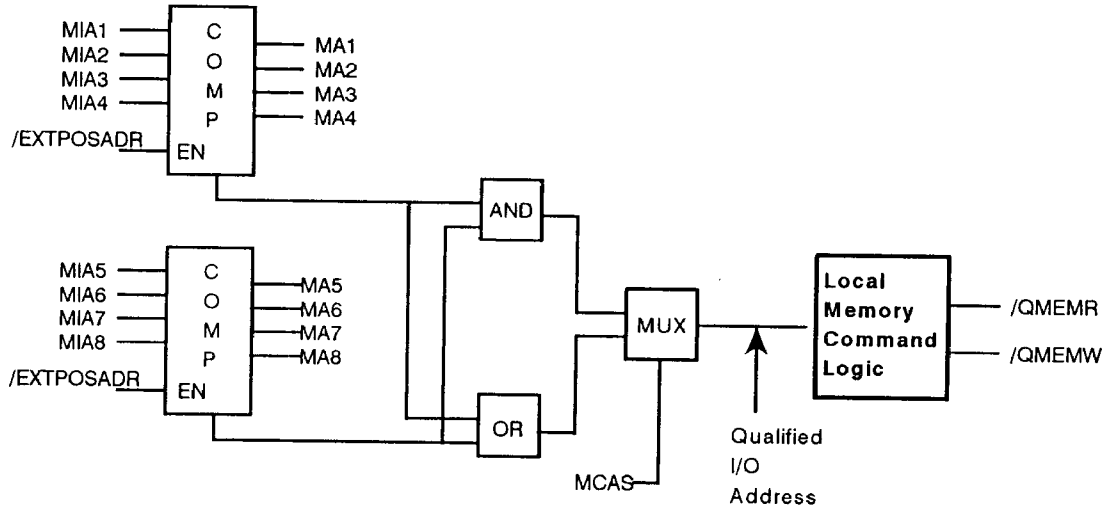


Figure 4 Memory Relocation Map

There are two 4-bit comparators in the I/O memory relocator. They are enabled by /EXTPOSADR. Comparator results go to an AND gate and an OR gate. ICAS or MECAS selects either the OR gate output or the AND gate output as the qualified address. If the OR gate output is selected, the relocator is two 4-bit relocators. If the AND gate output is selected, the relocator is an 8-bit relocator. The address must be prequalified and to enable the comparators.

Interrupt Control

Interrupt control maps two edge-trigger input request lines to two of four level trigger output request lines through POS102 and POS105. The interrupt has two modes.

In mode 0, the pending latch is built inside the ACC 5810. The pending latch is accessed by an I/O port. The I/O port is implemented by decoding an I/O address to the INST signal. This port is a read/write port. To read the pending latch, read the INST port: Bit 1 is the INT2 pending latch, Bit 0 is the INT1 pending latch.

To clear pending latch INT1, write 0 to INST port bit 0, then write 1 to INST port bit 0. To clear pending latch INT2, write 0 to INST port bit 1, then write 1 to INST port bit 1.

In mode 1, the output request line for the interrupt is not controlled by the pending latch. The output request line is terminated by 14M OSC.

To use the pending latch outside the ACC 5810, the interrupt control circuit must operate in mode 2. Figure 5 diagrams the application circuit in effect.

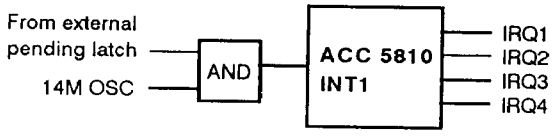


Figure 5 Mode 2 Application Circuit

Ready Control Timing

/CDCHRDY becomes active when RDYSEL is 1 and the address is qualified. The cycle time of /CDCHRDY depends on POS103 Bits 0-3.

DMA Timing Control

DMA timing control is inside the ACC 5810. It supports single cycle mode, burst mode and a fairness feature.

In single cycle mode, DREQ initiates the DMA control circuit to access /PREEMPT. Once PREEMPT is accessed, the arbitration bus signal is activated by the local arbitrator when ARB/-GNT is high. When ARB/-GNT goes low, the local arbitrator compares the arbitration bus with POS105 bits 0-3. If the bits match, BUSWON goes high, and /QIOR or /QIOW is accessed and /PREEMPT goes high. /PREEMPT stays low if the bits do not match.

In burst mode, the operation sequence is similar to single cycle mode, however /BURST goes low when BUSWON is active. /BURST is activated until the the expected number of words is transferred by DMA. POS104 bits 7-5 control the transfer number.

The /BURST signal becomes inactive when /TC occurs.

DMA burst mode operates differently depending on the fairness bit. When the fairness bit is 1 and the ACC 5810 occupies the bus, the ACC 5810 will relinquish the bus at any other adapter request. Once the bus is occupied by the other adapter request, ACC 5810 internal logic issues another request. This cycle continues until the DMA transfer is complete. The fairness algorithm avoids high priority device lockout for all other devices.

If fairness is 0 and the ACC 5810 occupies the bus, other requests do NOT affect ACC 5810 DMA operations. All other devices are locked out.

ACC 5810 has three DMA adapter logic signals: DREQ, BUSWON, BUSCYC. DREQ initiates the DMA cycle for the ACC 5810. BUSWON indicates that the ACC 5810 occupies the bus. BUSCYC indicates that the burst cycle is complete. BUSCYC has the same timing as BUSWON when fairness is 0.

Absolute Maximum Ratings

T_a = 25° C, VSS = 0 V

Parameter	Symbol	Min	Max	Unit
Power supply voltage	VCC	-0.5	-7	V
Input voltage	VI	-0.5	VCC+0.5	V
Output voltage	VO	-0.5	VCC+0.5	V
Input current	I_I	-10	10	mA
Output current	I_O	-30	30	mA
Storage temp	Tstg	-65	150	C

Operating Conditions

Parameter	Symbol	Min	Max	Typ	Unit
Power supply voltage	VCC	4.5	5.5	5	V
Operation temperature	Top	-40	85	25	C
High level input voltage	V1H	2.2	VCC+0.3		V
Low level input voltage	V1L	VSS-0.3	0.8		V
Output sink control	I_{OL}		24	12	mA
Output Load capacity	CL			20	PF

DC Specifications

GROUP 1 INPUT

/S0, /S1, ARB/-GNT, A0, A1, A2, /INST, /EXTPOSADR, CHRESET, M/-IO, /CMD, /CDSETUP

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS-0.3	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.2	VCC+0.3	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-1.0	n/a	uA	VIN = VSS
Input high current	IIH	n/a	1.0	uA	VIN = VCC

GROUP 2 INPUT WITH SCHMITT TRIGGER

/TC, INT1, INT2, DREQ, 14MHZ

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS-0.3	0.6	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.4	VCC+0.3	V	VCC = 5 V +/- 0.25 V
Input low current	IIL	-1.0	n/a	uA	VIN = VSS
Input high current	IIH	n/a	1.0	uA	VIN = VCC

GROUP 3 TOTEM POLE OUTPUT

/CDCHRDY, /QIOR, /QIOW, /MEMR, /MEMW, /RD100, /RD101, BUSWON, /CDSFDBK

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL	VSS	0.5	V	IOL = 8.0 mA
Output high voltage	VOH	2.4	VCC	V	IOH = -8.0 mA

GROUP 4 OPEN COLLECTOR OUTPUT

IRQ1, IRQ2, IRQ3, IRQ4, /BURST

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 24 mA
Output high Impedance current	IOZH	n/a	10.0	uA	VSS < VOUT < VCC

GROUP 5 INPOUT/OUTPUT WITH PULLUP (24 mA)

/PREEMPT, ARB0, ARB1, ARB2, ARB3

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS-0.3	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC+0.3	V	VCC = 5 V +/- 0.25 V
Output low voltage	VOL		0.4	V	IOL = 24.0 mA
Output high voltage	VOH	2.4		V	IOH = -24.0 mA
Output high Impedance current	IOZH	-10.0	-120	uA	VSS < VOUT < VCC

GROUP 6 INPOUT/OUTPUT WITH PULLUP (8 mA)

MIA1-8, D0-7

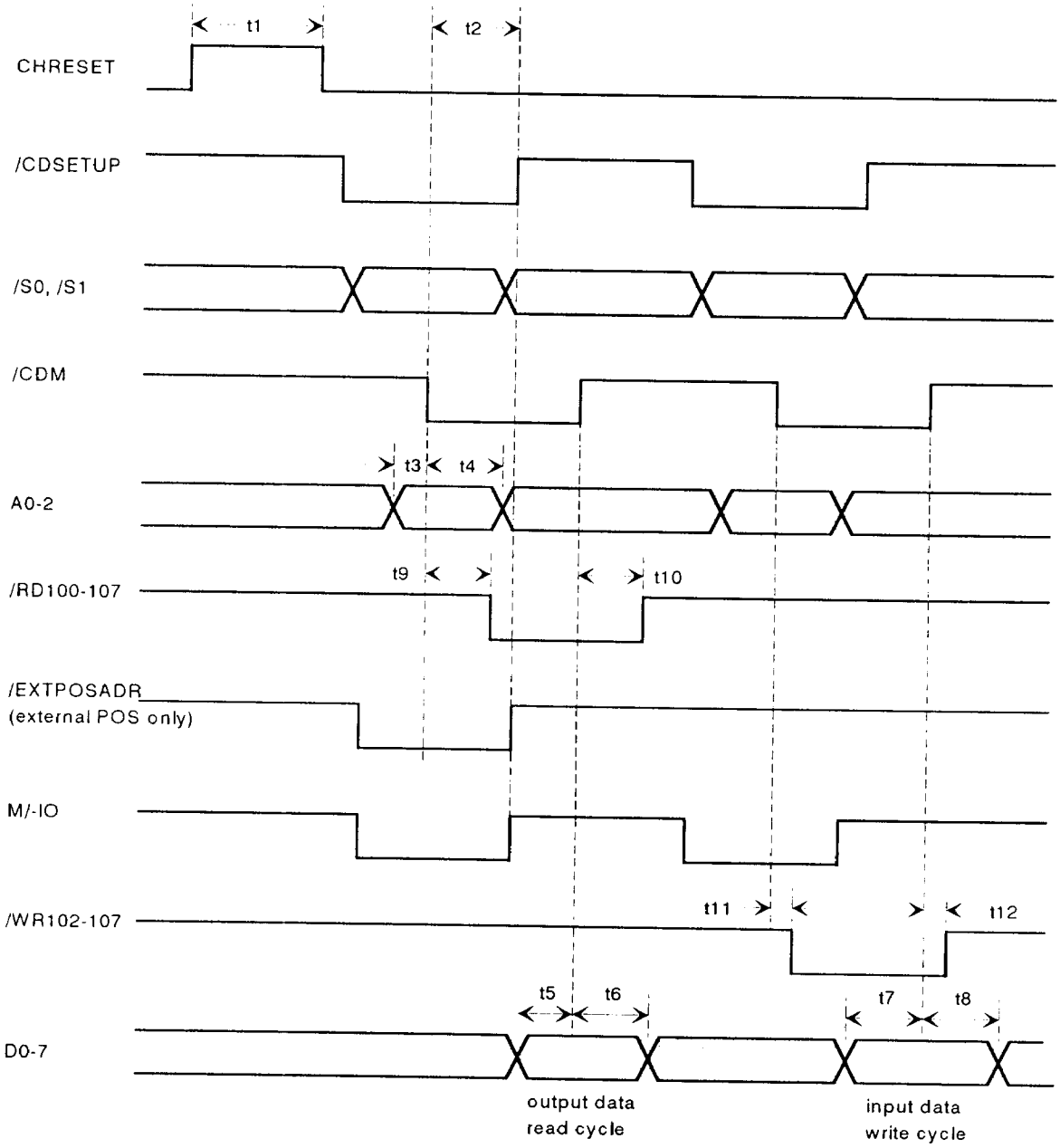
Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL	VSS-0.3	0.8	V	VCC = 5 V +/- 0.25 V
Input high voltage	VIH	2.0	VCC+0.3	V	VCC = 5 V +/- 0.25 V
Output low voltage	VOL		0.4	V	IOL = 8.0 mA
Output high voltage	VOH	2.4		V	IOH = -8.0 mA
Output high Impedance current	IOZH	-10.0	-120	uA	

AC Specifications

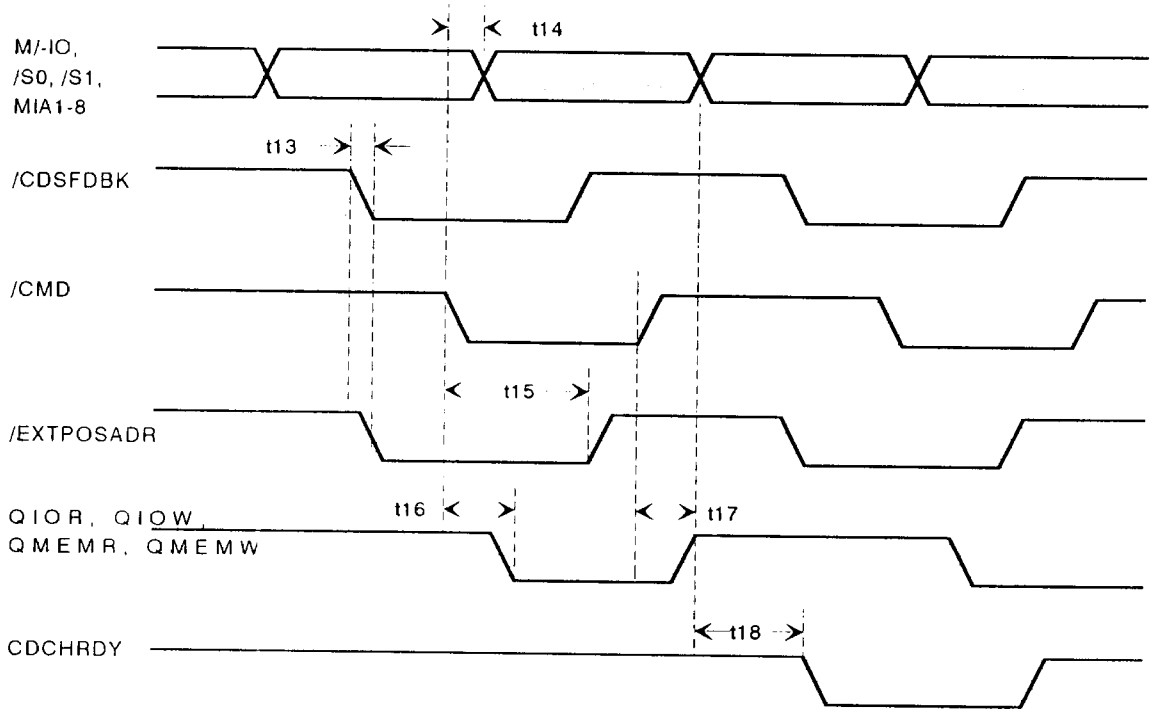
Setup Cycle

Symbol	Description	Min	Max	Units
t1	CHRESET pulse width	100		ns
t2	/CDSETUP, /S0, /S1, M/-IO, /EXTPOSADR Hold time from /CMD negative edge	20		ns
t3	Address setup time to /CMD negative edge	30		ns
t4	Address hold time from /CMD negative edge	10		ns
t5	Read data setup time to /CMD positive edge	50		ns
t6	Read data hold time from /CMD positive edge	40	80	ns
t7	Write data setup time to /CMD positive edge	30		ns
t8	Write data hold time from /CMD positive edge	10		ns
t9	/RD100 - /RD107 low output delay		20	ns
t10	/RD100 - /RD107 high output delay		20	ns
t11	/WR102 - /WR107 low output delay		20	ns
t12	/WR102 - /WR107 high output delay		20	ns

Setup Cycle

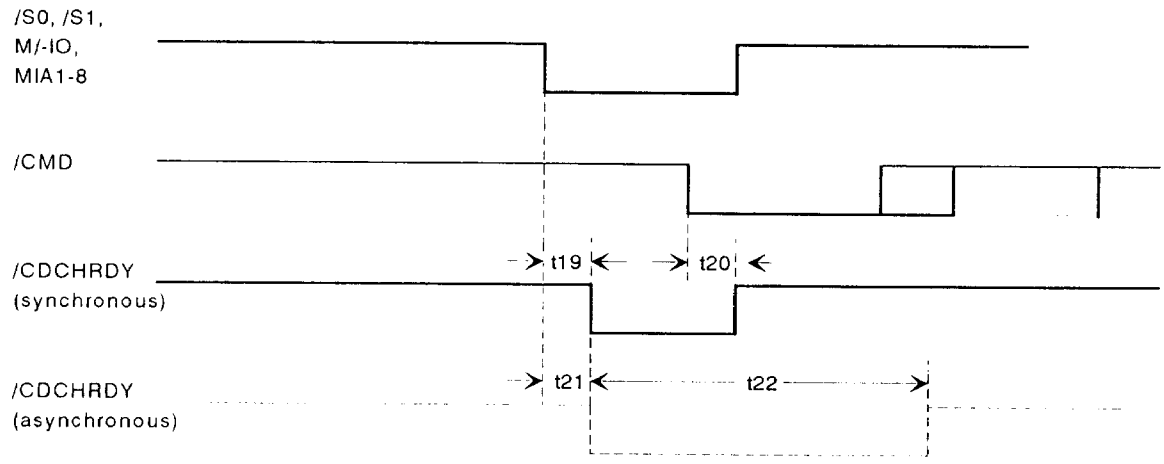

t1
t2
CHRESET
/CDSETUP
/S0, /S1
/CDM
t3
t4
A0-2
t9
t10
/RD100-107
/EXTPOSADR
(external POS only)
M/-IO
t11
t12
/WR102-107
t5
t6
t7
t8
D0-7
output data
read cycle
input data
write cycle

I/O and Memory Cycle



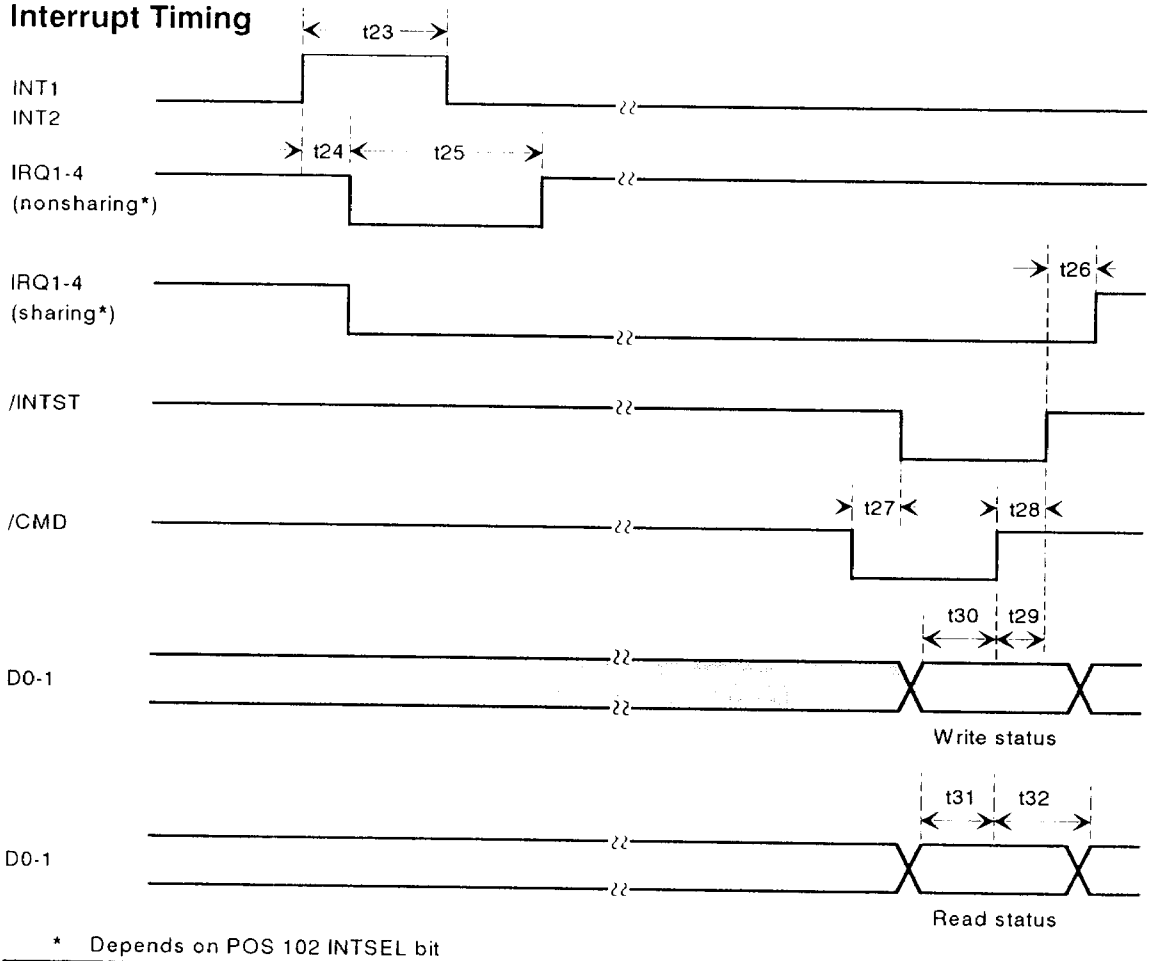
Symbol	Description	Min	Max	Units
t13	/CDSFDBK to /EXTPOSADR		20	ns
t14	M/-IO, /S0, /S1, MIA1-8 hold time	20		ns
t15	/EXTPOSADR hold time from /CMD negative edge	20		ns
t16	QIOR, QIOW, QMEMR, QMEMW (low) from CMD (low) output delay		15	ns
t17	QIOR, QIOW, QMEMR, QMEMW (high) from CMD (high) output delay		15	ns
t18	/S0, /S1 valid to CDCHRDY output delay		25	ns

RDY Timing



Symbol	Description	Min	Max	Units
t19	/S0, /S1, MIA1-8 to /CDCHRDY low		35	ns
t20	/CMD low to /CDCHRDY high (synchronous)		30	ns
t21	/S0, /S1, MIA1-8 to /CDCHRDY low (asynchronous)		35	ns
t22	Asynchronous pulse width at 14MHz OSC	300	1.2	us

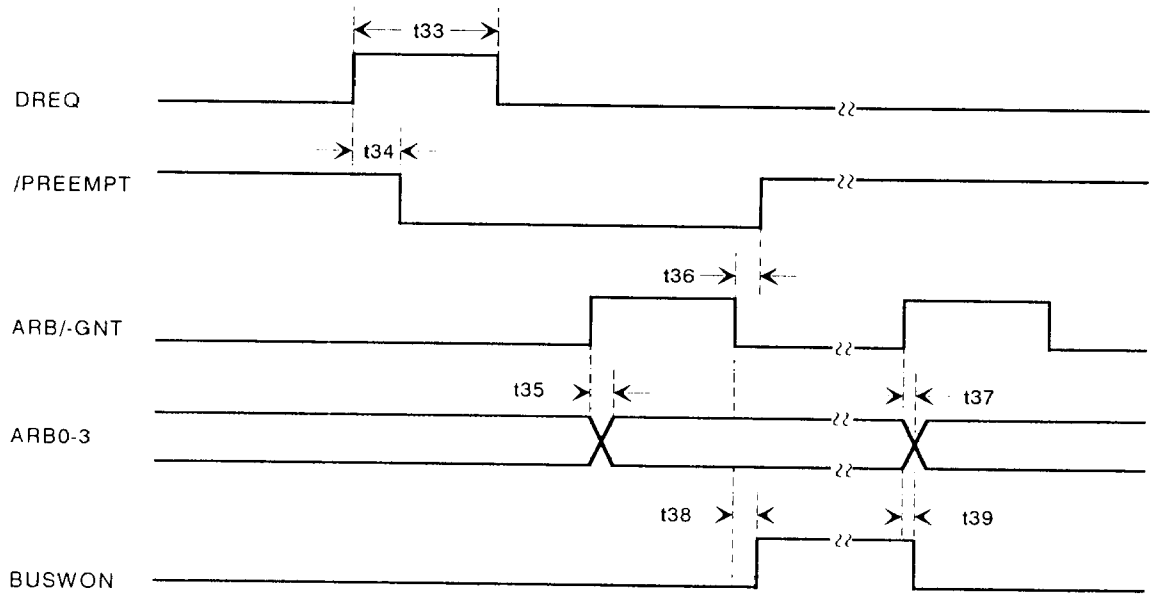
Interrupt Timing



* Depends on POS 102 INTSEL bit

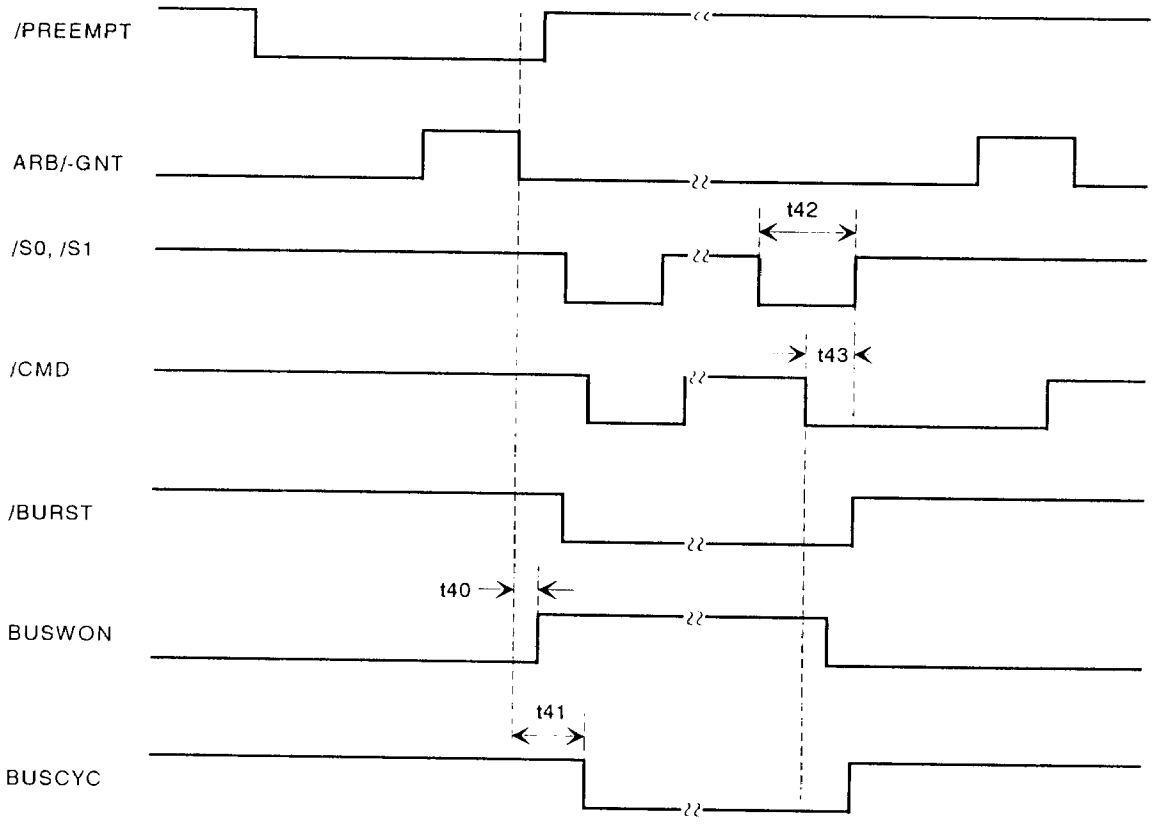
Symbol	Description	Min	Max	Units
t23	INT pulse width	30		ns
t24	IRQ dly from INT		20	ns
t25	Nonsharing IRQ pulse width	3CLK	4CLK	ns
t26	Sharing IRQ high to /INTST high		30	ns
t27	/INST low to /CMD low		30	ns
t28	/INST high to /CMD high		30	ns
t29	D0-D1 to /CMD hold time (write status)	10		ns
t30	D0-D1 to /CMD setup time	30		ns
t31	D0-D1 to /CMD hold time (read status)	40		ns
t32	D0-D1 to /CMD setup time	30	70	ns

DMA Timing



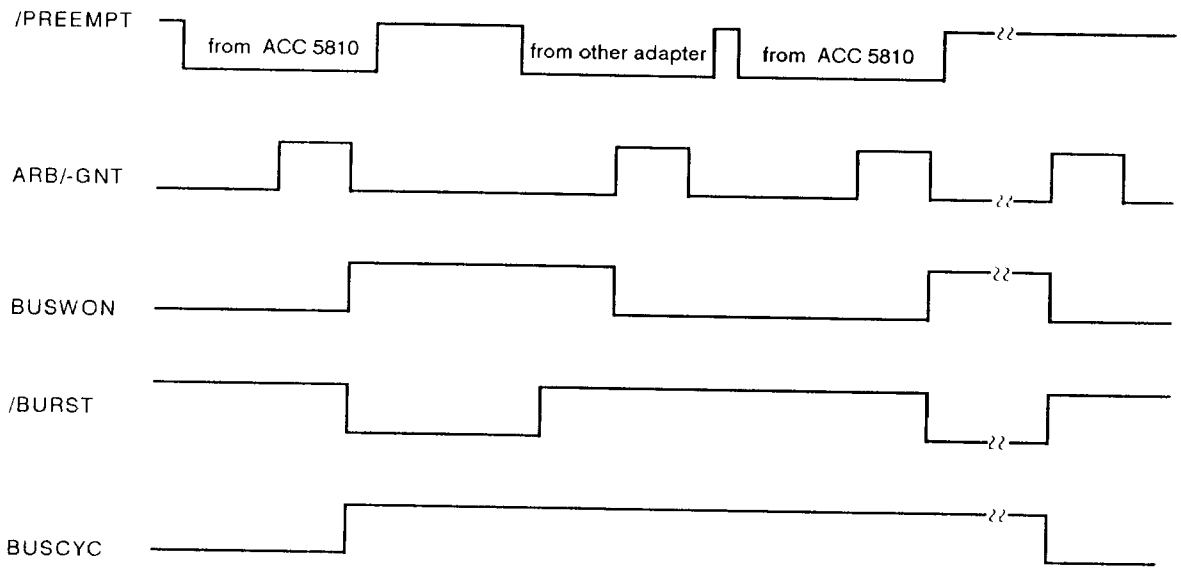
Symbol	Description	Min	Max	Units
t33	DREQ pulse width	30		ns
t34	DREQ to PREEMPT output delay		20	ns
t35	ARB/GNT to ARB0-3 valid		30	ns
t36	/PREEMPT high from ARB/-GNT		50	ns
t37	ARB0-3 nonvalid from ARB/-GNT		30	ns
t38	BUSWON high from ARB/-GNT		40	ns
t39	BUSWON low from ARB/-GNT		30	ns

Burst Timing (Fairness = 0)

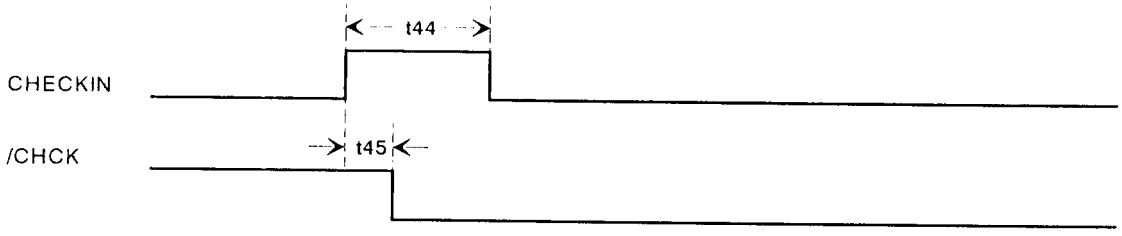


Symbol	Description	Min	Max	Units
t40	BUSWON from ARB/-GNT		40	ns
t41	BUSCYC from ARB/-GNT		40	ns
t42	Status to BURST inactive (default cycle)		20	ns
t43	/CMD (low) to BURST inactive (default cycle)		30	ns

Burst Timing (Fairness = 1)



Channel Check Timing



Symbol	Description	Min	Max	Units
t44	CHCHIN pulse width	30		ns
t45	CHCKIN to CDCK dly		20	ns

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