3221
Data Processor

ACC Micro's 3221 Data Processor is a single chip controller providing a total I/O solution for the PC/XT and PC/AT systems. This data processor supports a floppy disk controller, two serial ports, bidirectional parallel ports, and an IDE interface in either a 144-, 128- or 100-pin PQFP package. The 3221 has a unique power conservation feature that allows the whole chip and each individual data I/O device to be powered down. That is, all the inputs are disabled, and all the outputs are tri-stated.

Floppy Disk Controller

* Compatible with IBM PC/AT and PC/XT disk drive systems
* Supports 360K/720K/1.2M/1.44M formats
* Supports up to three 3.5" or 5.25" floppy disk drives
* Emulates the NEC765A in an IBM PC environment
* Supports variable write precompensation
* On-chip digital data separator eliminates critical analog adjustments
* Data rates of 250, 300 and 500 Kbits
* Programmable data record length 128, 256, 512, or 1024 bytes/sector
* 16-bit half cell divide algorithm reduces soft error rates
* Direct high current drive output for floppy drives
* Supports external bootable floppy drives[2]

IDE (Integrated Drive Electronics) Interface

* Supports one IDE bus interface hard disk drive for AT/XT systems

Serial and Parallel Ports

* Supports two serial ports and bi-directional parallel ports
* Direct drive for parallel ports
* Controller signals for parallel port B[1]
* Parallel port extended mode supports bidirectional input and output
* Serial ports fully 16C450 compatible

General

* EISA support mode[2]
* RTC interface[2]
* General purpose chip selects[2]
* Power down individual port in the chip
* Programmable configuration registers to eliminate hardware jumpers
* Hardware or software disable of ports[3]
* Supports board level in-circuit testing[3]
* All configuration registers are readable
* 1.2 micron high performance CMOS
* 144-L/128-L/100-L PQFP package

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General Description

ACC Micro's 3221 is a high performance CMOS single-chip data processor. This chip integrates Floppy disk controller, AT hard disk interface, two serial ports, and bi-directional parallel ports into a single chip with advanced features. The 3221-EP and 3221-DP chips integrate two bi-directional parallel ports. The 3221-SP integrates one bi-directional port.

Floppy Disk Controller

With the 3221, designers can build an IBM PC/XT or AT compatible Floppy Disk Drive with fast access time, high reliability and low cost per bit capability. The 3221 integrates the functions of a standard floppy disk drive controller.

- Data separator
- Write precompensation circuit
- Decode logic
- Data rate selection
- Clock generation
- Drive interface drivers and receivers.

This integration greatly reduces the number of components required to interface floppy disk drives to a microprocessor system.

The 3221 supports up to three floppy disk drives. It is compatible with IBM System 34 double density format (MFM), and Sony EMCA format.

The 3221 contains the decode logic for the internal registers, the write logic and the read logic. The system address decoder is compatible with the IBM PC drive system. Handshaking signals are provided to make DMA operation easy to incorporate with the aid of an external DMA control chip. The 3221 operates in either DMA or Non-DMA modes. In the Non-DMA mode, the 3221 generates interrupts to the processor each time a data byte is available. In DMA mode, the processor only needs to load the command into the 3221 which will control all data transfers.

The Data Separator in the 3221 minimizes read error rates for high performance floppy disk drives. The on-chip phase locked loop digital circuit adjusts the clock used during data read to keep it in phase with the data signal. Write precompensation is included in addition to the formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible, and outputs are high current, open drain with direct drive interface.

Using a single 24 MHz crystal input, the 3221's internal Clock Generation circuit provides all timing signals for the sampling clock, write clock, and master clock. It generates 8 and 4 MHz to handle standard data rates of 500 and 250 Kb/s and 4.8 MHz to support a 300 Kb/s data rate. This chip can support 1Mb/s data transfer rate by using 48MHz oscillator.

The 3221 executes the following fifteen commands from the microprocessor.

- Read Data
- Read Deleted Data
- Read a Track
- Read ID
- Write Data
- Write Deleted Data
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek

AT Hard Disk Interface

The 3221 supports one AT hard disk drive interface through a 40-pin AT interface connector, and includes the address decoding and buffering of signals for this interface.

Bi-directional Parallel Port

The 3221-EP and 3221-DP provide two bi-directional parallel ports. The 3221-SP provides one bi-directional parallel port. Each parallel port supports PS/2 compatible extended mode for the parallel port to receive data from external devices.

In 3221-DP and 3221-SP, parallel ports have direct drives to interface to the line printer port.

The 3221-EP parallel port A has direct drives to interface to the line printer. Parallel port B needs to add data buffers to interface to the line printer port.

Serial Ports

The 3221 supports two serial ports. Each serial port interface converts data from peripheral devices or modems from serial-in-data to parallel-out-data. Data transmitted from the CPU is converted from parallel-in-data to serial-out-data. The status of the UART can be read during any CPU operation. Status includes type and condition of the transfer operations in progress, and error conditions.

Individual Port Hardware Disable

For add-in board applications, the 3221-DP and 3221-SP allow power-on status of each individual port to be set by adding a pull-up resistor, or a pull-down resistor, on the pins shown below. A pull-up resistor on the pin disables the associated port. A pull-down resistor enables the associated port. For instance, if 3221 senses there is a pull-up resistor on pin 116 (/HCS0), then the primary serial port will be disabled at power-on. Applies only to 3221-DP and 3221-SP.

Pin DP	Pin SP	Symbol	Port
116	93	/HCS0	Primary Serial Port
121	97	/IENL	Secondary Serial Port
117	94	/HCSI	Floppy Disk Controller
120	96	/IENH	Primary Parallel Port
13	13	DBIR	IDE
77	n/a	DISPAR2	Secondary Parallel Port

After power-on, each individual port can then be programmed by the associated control registers to enable or disable individually as needed (refer to programmable confirmation registers).

Multifunction Modes

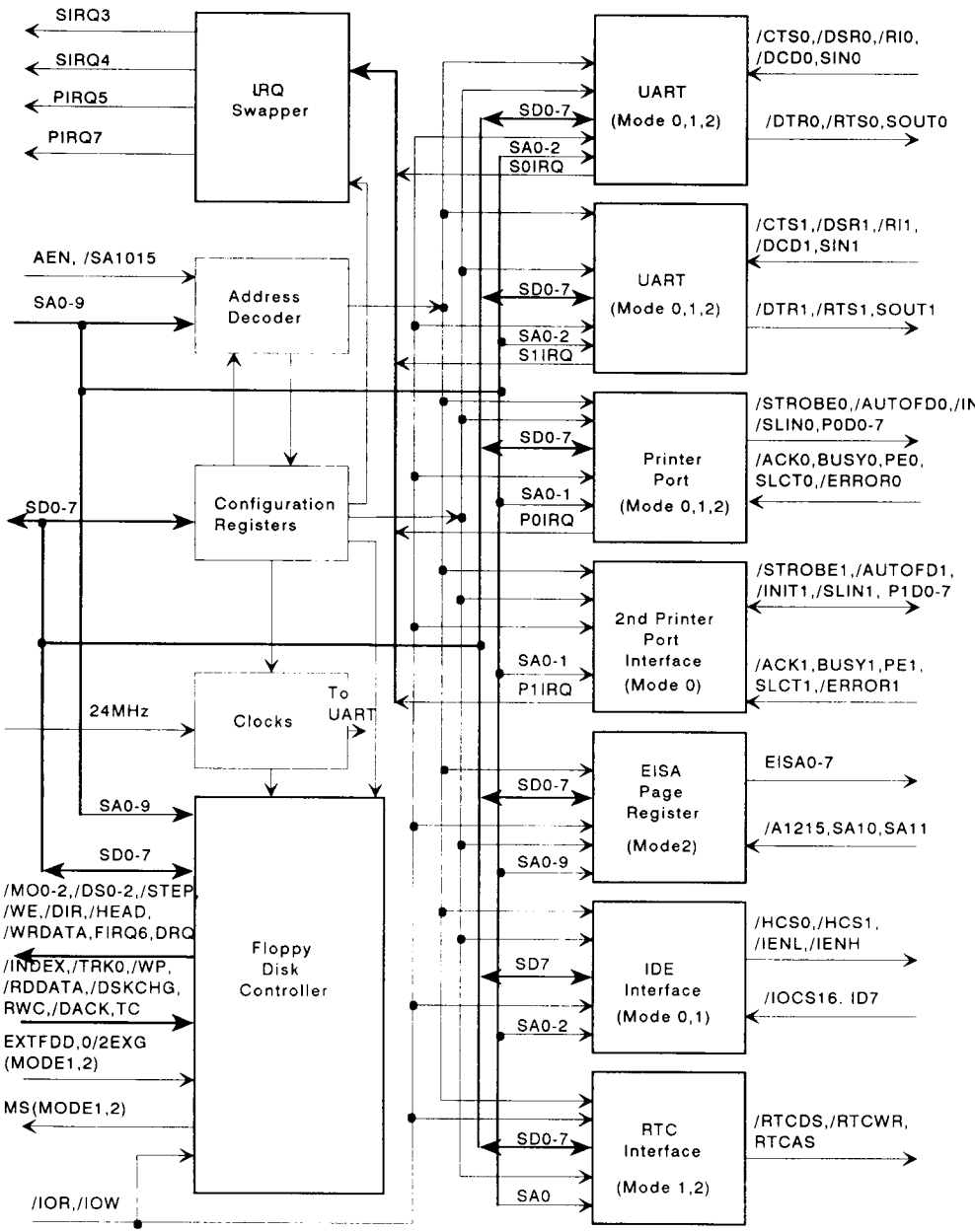
The 3221-EP and 3221-DP support three modes of operation. Configuration register DF, bits 0 and 1 select the operation modes.

In Mode 0, multifunction pins are used for second parallel port control and IDE interface. In Mode 1, multifunction pins are used for IDE, RTC interface*, and general chip selects. In Mode 2, multifunction pins are used for supporting EISA registers and RTC interface. The default in 3221-EP is Mode 1. The default in 3221-DP is Mode 0. The 3221-SP has only one operation mode to keep the pin count to a minimum.

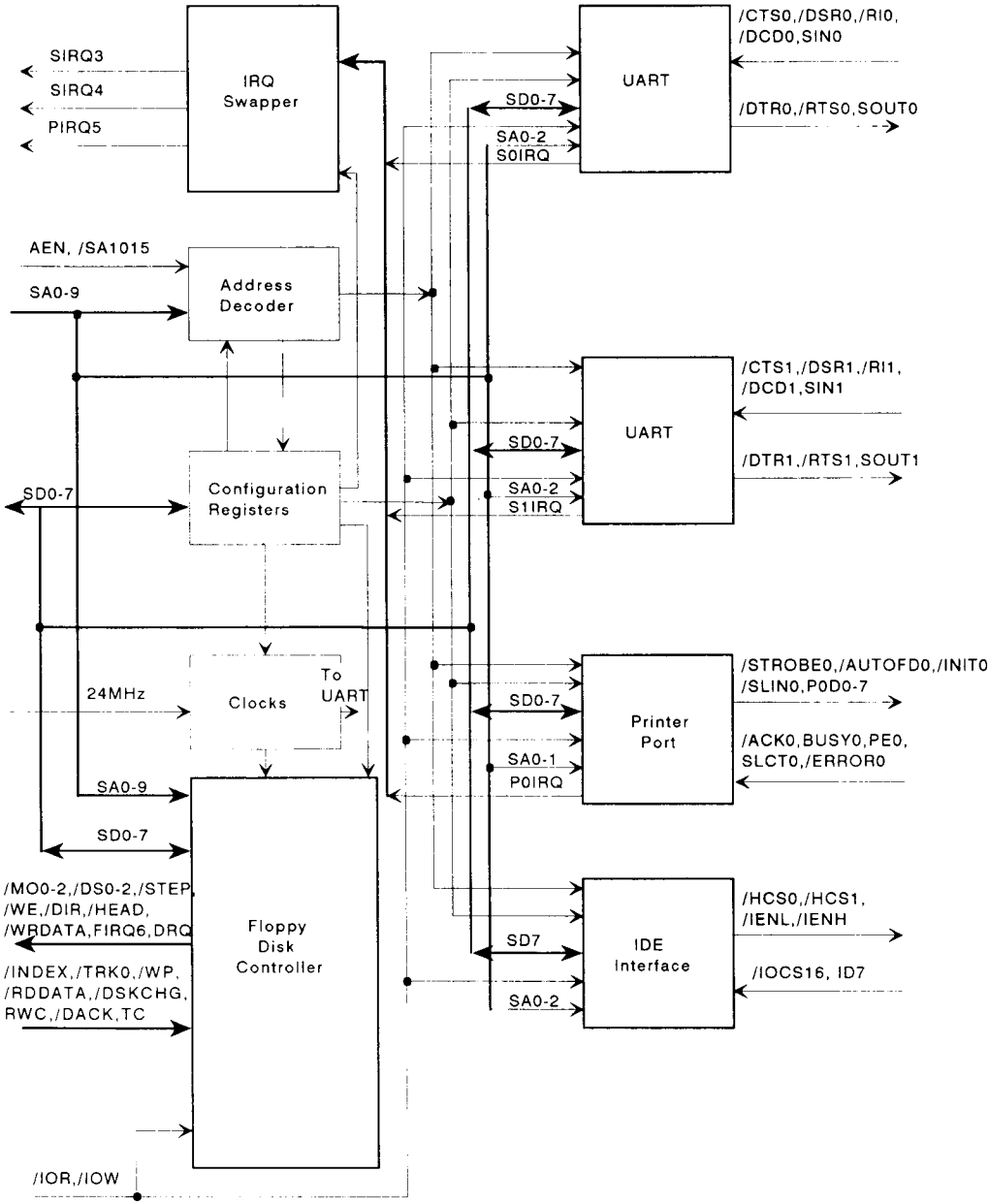
Notes:

1 Feature supported in 3221-EP only.
2 Feature supported in 3221-EP and 3221-DP.
3 Feature supported in 3221-EP and 3221-SP.

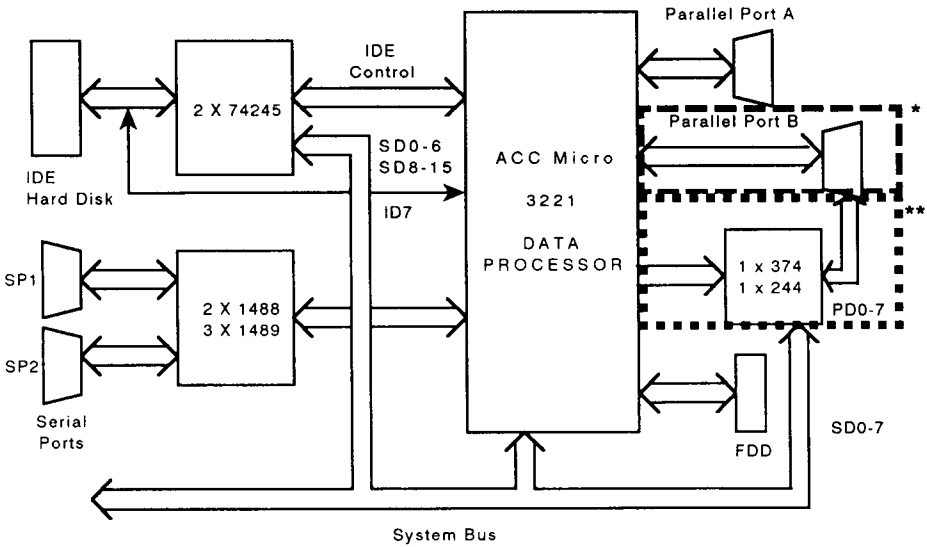
Block Diagram (3221-EP/DP)



Block Diagram (3221-SP)



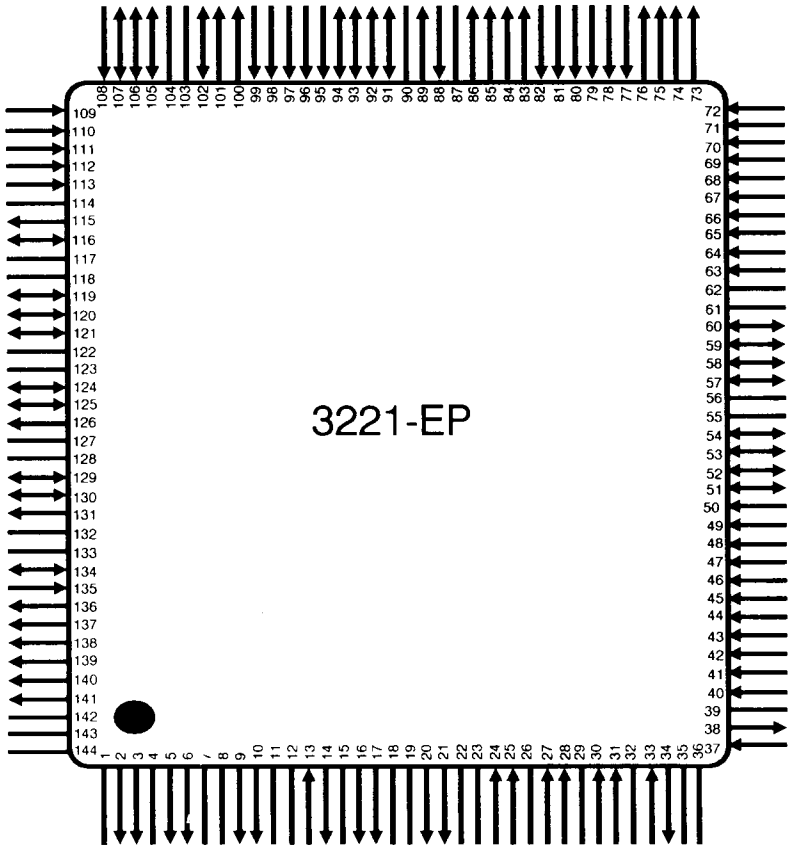
Typical Application



Features	3221-SP	3221-DP	3221-EP
Package	100 Pins	128 Pins	144 Pins
Three FDDS	Yes	Yes	Yes
Two Serial Ports	Yes	Yes	Yes
Parallel Port	1	2	2
Two IDE Drives	Yes	Yes	Yes

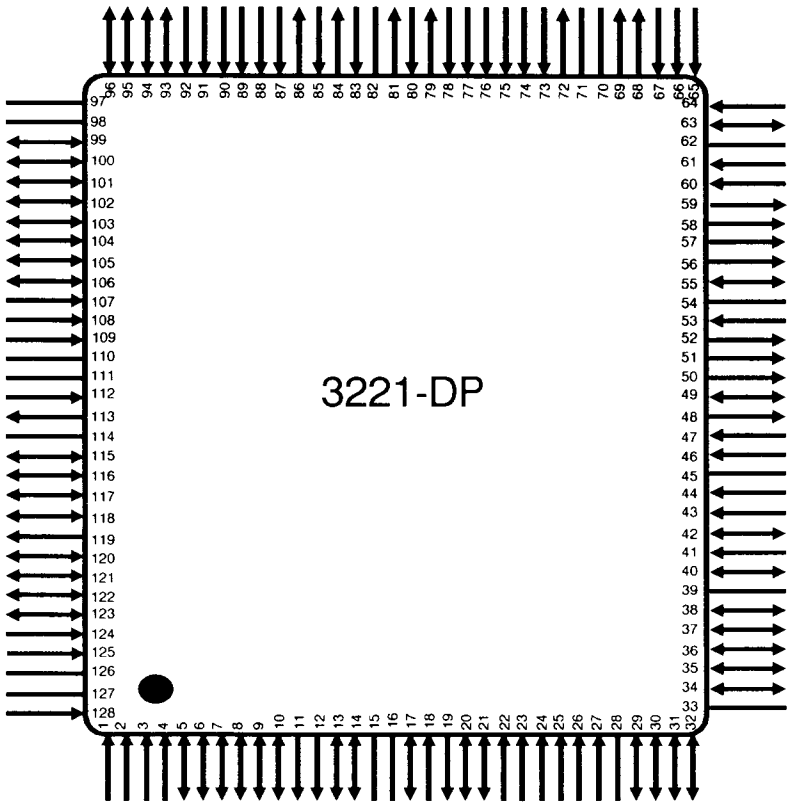
* Applies to 3221-EP and 3221-DP.
** Applies to 3221-EP only.

Pin Diagram (144-Pin Package)



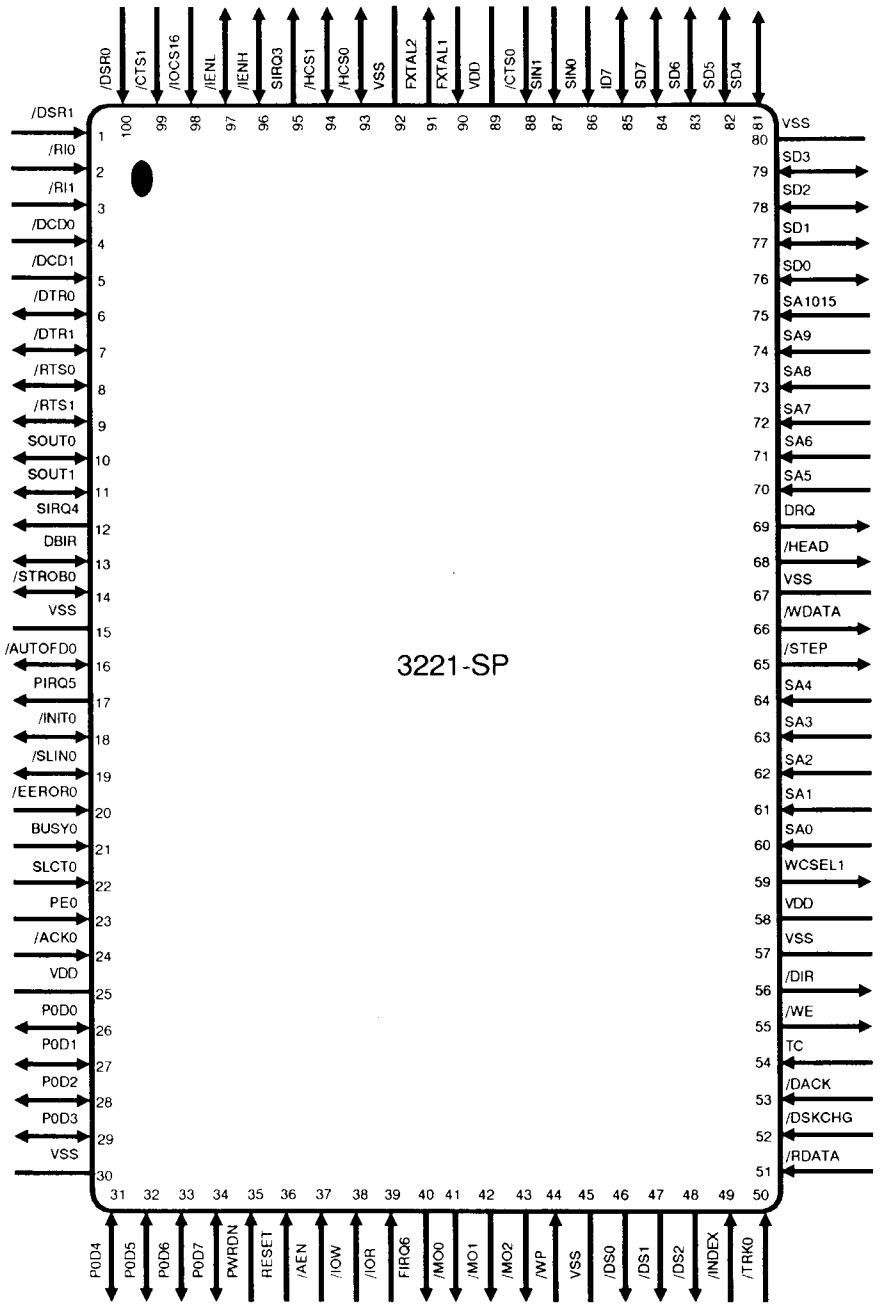
1 N.C.	49 SA9	65 /IOW	81 SIN1	97 PE0	113 /IOCS16, EISA7	129 P0D5
2 /MO0	50 /SA1015	66 /TRK0	82 SOUT1	98 SLCT0	114 VSS	130 P0D6
3 /MO1	51 SD0	67 /CTS0	83 /DTR1	99 /ACK0	115 /PDRD, EISA6	131/HCS1, EISA3
4 VSS	52 SD1	68 /DSR0	84 /RTS1	100 DBIR	116 P0D0	132 VSS
5 /DS0	53 SD2	69 /RI0	85 PIRQ5	101 /MODEM CS	117 VSS	133 VDD
6 /DS1	54 SD3	70 /DCD0	86 PIRQ7	102 /STROBE2, /RTCDS	118 VDD	134 P0D7
7 N.C	55 VSS	71 SIN0	87 VSS	103 VSS	119 P0D1	135 /TRISTATE
8 VSS	56 VDD	72 SOUT0	88 SXTAL1	104 VDD	120 P0D2	136 /PDLAT, /KBDCS
9 /MO2	57 SD4	73 /DTR0	89 SXTAL2	105 /AUTOFD1, /RTCWR	121 ID7, EISA2	137 /IENH, EISA4
10 /DS2	58 SD5	74 /RTS0	90 VDD	106 /INIT1, /GCS1, EISA0	122 VSS	138 /IENL, EISA5
11 N.C.	59 SD6	75 SIRQ3	91/STROBE0	107 /SLIN1, /GCS2, EISA1	123 VDD	139 PDOEO, RTCAS
12 VSS	60 SD7	76 SIRQ4	92 /AUTOFD0	108 /ERROR1, /A1215L	124 P0D3	140 FIRQ6
13 RESET	61 VSS	77 /CTS1	93/INIT0	109 BUSY1, 0/2EXG	125 P0D4	141 DRQ
14 /STEP	62 VDD	78 /DSR1	94 /SLIN0	110 SLCT1, EXTFDD	126/HCS0, EISAIDCS	142 VSS
15 N.C.	63 AEN	79 /RI1	95 /ERROR0	111 PE1, A11	127 VSS	143 N.C.
16 /WE	64 /IOR	80 /DCD1	96 BUSY0	112 /ACK1 ,A10	128 VDD	144 VDD
17 /WRDATA						
18 VSS						
19 N.C.						
20 /DIR						
21 /HEAD						
22 VSS						
23 N.C.						
24 TC						
25 /DACK						
26 N.C.						
27 /DSKCHG						
28 /RDDATA						
29 N.C.						
30 /WP						
31 /INDEX						
32 N.C.						
33 RWC						
34 MS						
35 N.C.						
36 VSS						
37 FXTAL1						
38 FXTAL2						
39 VDD						
40 SA0						
41 SA1						
42 SA2						
43 SA3						
44 SA4						
45 SA5						
46 SA6						
47 SA7						
48 SA8						

Pin Diagram (128-Pin Package)



1 /RI0	17 /AUTOFD0	33 VSS	49 /SLIN1*	65 /DSKCHG	81 /WDATA	97 VSS	113 FXTAL2
2 /RI1	18 /ERROR1*	34 /STROBE1*	50 /MO0	66 /DACK	82 VSS	98 VDD	114 VSS
3 /DCD0	19 PIRQ5	35 /AUTOFD1*	51 /MO1	67 TC	83 PE1*	99 P1D2*	115 P1D5
4 /DCD1	20 /INIT0	36 P0D4	52 /MO2	68 /WE	84 /HEAD	100 SD4	116 /HCS0*
5 /DTR0	21 /SLIN0	37 P0D5	53 /WP	69 /DIR	85 /ACK1*	101 SD5	117 /HCS1*
6 /DTR1	22 BUSY1*	38 P0D6	54 VSS	70 VSS	86 DRQ	102 SD6	118 P1D6
7 /RTS0	23 /EERROR0	39 VDD	55 P1D1*	71 VDD	87 SA5	103 P1D3	119 SIRQ3
8 /RTS1	24 BUSY0	40 P0D7	56 /DS0	72 RWCSEL1	88 SA6	104 SD7	120 /IENH*
9 SOUT0	25 SLCT0	41 PWRDN	57 /DS1	73 SA0	89 SA7	105 ID7*	121 /IENL*
10 SOUT1	26 PE0	42 /INIT1*	58 MS*	74 SA1	90 SA8	106 P1D4	122 P1D7
11 PIRQ7	27 /ACK0	43 RESET	59 /DS2	75 SA2	91 SA9	107 SIN0	123 /IOC16*
12 SIRQ4	28 VDD	44 /AEN	60 /INDEX	76 SA3	92 SA1015	108 SIN1	124 /CTS1
13 DBIR	29 P0D0	45 VSS	61 /TRK0	77 DISPAR2	93 SD0	109 /CTS0	125 /DSR0
14 /STROB0	30 P0D1	46 /IOW	62 VSS	78 SA4	94 SD1	110 VSS	126 VSS
15 VDD	31 P0D2	47 /IOR	63 P1D0*	79 /STEP	95 SD2	111 VDD	127 VDD
16 VSS	32 P0D3	48 FIRQ6	64 /RDATA	80 SLCT1*	96 SD3	112 FXTAL1	128 /DSR1

Pin Diagram (100-Pin Package)



Pin Descriptions

Symbol	Pin			I/O	Pin Description
	EP	DP	SP		
AT Bus					
SA0	40	73	60	I	Address bus.
SA1	41	74	61		
SA2	42	75	62		
SA3	43	76	63		
SA4	44	78	64		
SA5	45	87	70		
SA6	46	88	71		
SA7	47	89	72		
SA8	48	90	73		
SA9	49	91	74		
/SA1015	50	92	75	I	This input pin is active low signal when all I/O address bits 10-15 are low to ensure that I/O bus is fully decoded.
SD0	51	93	76	I/O	I/O Data bus. 16 ma.
SD1	52	94	77		
SD2	53	95	78		
SD3	54	96	79		
SD4	57	100	81		
SD5	58	101	82		
SD6	59	102	83		
SD7	60	104	84		
AEN	63	44	37	I	Address enable. Input from DMA controller. When this line is active, the DMA controller has control of the address bus.
RESET	13	43	36	I	Active high input that resets the controller to the idle state. Resets all the output lines to their disabled states. TTL Schmitt trigger.
/IOW	65	46	38	I	Command from the processor to transfer data from the SD bus to the 3221 chip.
/IOR	64	47	39	I	Command from the processor to transfer data from the chip to the SD bus.
DRQ	141	86	69	O	DMA request by FDC when DRQ=1. 16ma.

Pin Descriptions

Symbol	Pin			I/O	Pin Description
	EP	DP	SP		
/DACK	25	66	53	I	When set to 0, a DMA cycle is active and the controller performs a DMA transfer.
TC	24	67	54	I	When set to 1, terminates data transfer during Read/ Write/Scan commands in DMA or interrupt mode.
FIRQ6	140	48	40	O	Floppy controller interrupt request. 16ma
SIRQ3	75	119	95	O	Primary serial port interrupt request (programmable polarity). 16ma
SIRQ4	76	12	12	O	Secondary serial port interrupt request (programmable polarity). 16ma
PIRQ5	85	19	17	O	Primary parallel port interrupt request (programmable polarity). 16ma
PIRQ7	86	11	n/a	O	Secondary parallel port interrupt request (programmable polarity). 16ma
DBIR	100	13	13	O	Host data bus buffer direction. Low for internal access of serial ports, parallel ports, FDC and low byte of IDE. 4 ma.
Floppy Disk Controller					
FXTAL1	37	112	90	I	FDC XTAL oscillator input. 24 MHz.
FXTAL2	38	113	91	O	FDC XTAL oscillator output.
/MO0 /MO1 /MO2	2 3 9	50 51 52	41 42 43	O	When set to 0, the MOTOR ON enables the disk drive. This is an open drain output. 48ma
/DS0 /DS1 /DS2	5 6 10	56 57 59	46 47 48	O	When set to 0, the drive select enables the disk drive. This signal is an open drain output. 48ma
/WE	16	68	55	O	Write Enable. When set to 0, causes a write operation to the floppy disk drive. An open drain output. 48ma
/DIR	20	69	56	O	Direction of the head stepper motor. An open drain output. Logic 1 = outward motion. Logic 0 = inward motion. 48ma

Pin Descriptions

Symbol	Pin			I/O	Pin Description
	EP	DP	SP		
/HEAD	21	84	68	O	Head select. Open drain output. Determines which disk drive head is active. Logic 1 = Side 0. Logic 0 = Side 1. 48ma
/WRDATA	17	81	66	O	Write Data. Logic low open drain. Writes precompensated serial data to the selected FDD. An OD output. 48ma
/STEP	14	79	65	O	STEP output pulses. Active low open drain output. Produces a pulse at a programmable rate to move the head to another cylinder. 48ma
/INDEX	31	60	49	I	Active low Schmitt input from the disk drive. Senses the head positioning over the beginning of a track marked by an index hole. TTL Schmitt trigger.
/TRK0	66	61	50	I	Track 00. Active low schmitt input from the disk drive. Signals that the head is positioned over the outermost track. TTL Schmitt trigger.
/WP	30	53	44	I	Write Protected. Active low schmitt input from the disk drive indicates that the diskette is write protected. TTL Schmitt trigger.
/RDDATA	28	64	51	I	Read data input. Signals a read from the FDD to the microprocessor. TTL Schmitt trigger.
/DSKCHG	27	65	52	I	Diskette change. This signal is active low at power-on and when the diskette is removed. It remains active until a /STEP pulse is received with the diskette in place. TTL Schmitt trigger.
/RWC	33	72	59	O	Reduced write current. 48ma. 1: 500KB 0: 250, 300KB

Pin Descriptions

Symbol	Pin			I/O	Pin Description
	EP	DP	SP		
IDE HD Interface*0,1					
/HCS0*0,1	126	116	93	O	Chip selects for hard disk interface. In AT Mode /HCS0 is active for addresses 1F0h - 1F7h or 170h - 177h. /HCS1 is active for addresses 3F6h - 3F7h or 376h - 377h. 16ma. In XT Mode, /HCS0 is active for address 320h-323h.
/HCS1*0,1	131	117	94	O	
/IENH*0,1	137	120	96	O	IDE Bus Transceiver High Byte Enable. 4ma
/IENL*0,1	138	121	97	O	IDE Bus Transceiver Low Byte Enable. 4ma
/IOCS16*0,1	113	123	98	I	Indicating 16 Bit transfer in AT Mode. Using as DACK3 input in XT Mode.
ID7*0,1	121	105	85	I/O	IDE Data Bus Bit 7. 16ma
Serial Port					
SXTAL1	88	n/a	n/a	I	Serial port crystal/clock input, 1.84 MHz
SXTAL2	89	n/a	n/a	O	Serial port clock source output
/RTS0	74	7	8	O	Request to send. 4ma
/RTS1	84	8	9		
/CTS0	67	109	88	I	Clear to send
/CTS1	77	124	99		
/DTR0	73	5	6	O	Data Terminal Ready. 4ma
/DTR1	83	6	7		
/DSR0	68	125	100	I	Data Set Ready
/DSR1	78	128	1		
/RI0	69	1	2	I	Ring Indicator
/RI1	79	2	3		
/DCD0	70	3	4	I	Data Carrier Detected
/DCD1	80	4	5		
SIN0	71	107	86	I	Serial Data In
SIN1	81	108	87		
SOUT0	72	9	10	O	Serial data out. 4ma
SOUT1	82	10	11		

Pin Descriptions

Symbol	Pin			I/O	Pin Description
	EP	DP	SP		
Parallel Port A					
PD0	116	29	26	I/O	Parallel port A data bus. 16 ma
PD1	119	30	27		
PD2	120	31	28		
PD3	124	32	29		
PD4	125	36	31		
PD5	129	37	32		
PD6	130	38	33		
PD7	134	40	34		
/STROBE0	91	14	14	I/O	Parallel port A Strobe. 16ma
/AUTOFD0	92	17	16	I/O	Parallel port A Autofeed. 16ma
/INIT0	93	20	18	I/O	Parallel port A Initialize. 16ma
/SLIN0	94	21	19	I/O	Parallel port A Select. 16ma
/ERROR0	95	23	20	I	Parallel port A Error, TTL Schmitt trigger.
BUSY0	96	24	21	I	Parallel port A Busy, TTL Schmitt trigger.
SLCT0	98	25	22	I	Parallel port A Selected, TTL Schmitt trigger.
PE0	97	26	23	I	Parallel port A End of Paper, TTL Schmitt trigger.
/ACK0	99	27	24	I	Parallel port A Acknowledge signal from printer, TTL Schmitt trigger.
Parallel port B*[0]					
/STROBE1*[0]	102	34	n/a	I/O	Parallel port B Strobe. 16ma
/AUTOFD1*[0]	105	35	n/a	I/O	Parallel port B Autofeed. 16ma
/INIT1*[0]	106	42	n/a	I/O	Parallel port B Initialize. 16ma
/SLIN1*[0]	107	49	n/a	I/O	Parallel port B Select. 16ma
/ERROR1*[0]	108	18	n/a	I	Parallel port B Error.
BUSY1*[0]	109	22	n/a	I	Parallel port B Busy.
SLCT1*[0]	110	80	n/a	I	Parallel port B Selected.

Pin Descriptions

Symbol	Pin			I/O	Pin Description
	EP	DP	SP		
PE1*0	111	83	n/a	I	Parallel port B End of Paper.
/ACK1*0	112	85	n/a	I	Parallel port B Acknowledge Signal from printer.
PDLAT*0	136	n/a	n/a	O	Parallel port B, data output latch.
/PDOEO*0	139	n/a	n/a	O	Parallel port B data output enable.
/PDRD*0	115	n/a	n/a	O	Parallel port B data input enable.
P1D0*0	n/a	63	n/a	I/O	Parallel port B data bus. 16 ma
P1D1*0	n/a	55	n/a		
P1D2*0	n/a	99	n/a		
P1D3	n/a	103	n/a		
P1D4	n/a	106	n/a		
P1D5	n/a	115	n/a		
P1D6	n/a	118	n/a		
P1D7	n/a	122	n/a		
DISPAR2	n/a	77	n/a	I	Disable secondary parallel port
EISA page registers*2					
/A1215L*2	108	18	n/a	I	When /A1215L is active, addresses A12-A15 are logic 0.
SA11*2	111	83	n/a	I	Address input Bit 11.
SA10*2	112	85	n/a	I	Address input Bit 10.
/EISAIDCS*2	126	116	n/a	O	Active low when address = 0C80H-0C83H
EISA0*2	106	42	n/a	O	EISA page register, address = 0C00h
EISA1*2	107	49	n/a		
EISA2*2	121	105	n/a		
EISA3*2	131	117	n/a		
EISA4*2	137	120	n/a		
EISA5*2	138	121	n/a		
EISA6*2	115	99	n/a		
EISA7*2	113	123	n/a		

Pin Descriptions

Symbol	Pin			I/O	Pin Description
Miscellaneous					
	EP	**DP**	**SP**		
/TRISTATE	135	n/a	n/a	I	When /TRISTATE is active low, all the outputs are tristated to support board level in-circuit testing.
/PWRDOWN	n/a	41	35	I	When /PWRDOWN is active low, all the outputs are tristated to support board level in-circuit testing.
MS*[1,2]	34	58	n/a	O	Support for 3 1/2", 1.2MB drive.
/MODEM CS*[2]	101	99	n/a	O	Modem select. 4ma
RTCAS*[1]	139	99	n/a	O	Address strobe for 146818 Real Time Clock. Falling edge causes address to be latched in 146818.
/RTCDS*[1,2]	102	34	n/a	O	Data strobe for Real Time Clock. Identifies the cycle when the RTC and RAM drive the bus with read data.
/RTCWR*[1,2]	105	35	n/a	O	Read or write select for Real Time Clock.
/GCS1*[1]	106	42	n/a	O	General purpose chip select.
/GCS2*[1]	107	49	n/a	O	General purpose chip select.
/KBDCS*[1,2]	136	55	n/a	O	Keyboard chip select
EXTFDD*[1,2]	110	80	n/a	I	External FDD is powered on and connected to the system
0/2 EXG*[1,2]	109	22	n/a	I	External FDD's switch is exchanged by the operator to use the external FDD as the "A" drive

	144-Pin	**128-Pin**	**100-Pin**
VSS	4,8,12, 18,22,36, 55,61,87, 103,114, 117,122, 127,132,142	16,33,45, 54,62,70, 82,97,110, 114,126	15,30,45, 57,67,80, 92
VDD	39,56,62, 90,104, 118,123, 128,133,144	15,28,39 71,98,111, 127	25,58,89
N.C.	1,7,11, 15,19,23, 26,29,32, 35,143	n/a	n/a

Pin Numbers and Modes of Multifunction Pins

Pin Number		Mode 0 (Default)	Mode 1	Mode 2
EP	DP			
34	58		MS	MS
102	34	/STROBE1	/RTCDS	/RTCDS
105	35	/AUTOFD1	/RTCWR	/RTCWR
106	42	/INIT1	/GCS1	EISA0
107	49	/SLIN1	/GCS2	EISA1
108	18	/ERROR1		/A1215L
109	22	BUSY1	0/2EXG	0/2EXG
110	80	SLCT1	EXTFDD	EXTFDD
111	83	PE1		SA11
112	85	/ACK1	-	SA10
113	123	/IOCS16	/IOCS16	EISA7
115	63	P1D0		EISA6
121	105	ID7	ID7	EISA2
126	116	/HCS0	/HCS0	EISAIDCS2
131	117	/HCS1	/HCS1	EISA3
136	55	P1D1	KBDCS	KBDCS
137	120	/IENH	/IENH	EISA4
138	121	/IENL	/IENL	EISA5
139	99	P1D2	RTCAS	/MODEM, CS

Programmable Configuration Registers

Configuration registers in the 3221 are programmed with an indirect addressing scheme using I/O addresses F2 and F3. I/O address F2 contains the write-only configuration index register. F2 selects the correponding configuration register accessed at I/O address F3.

Configuration Register Index, BE (R/W)

Bit	Function
7	PIRQ 5 polarity. 1 = active high, default 0 = active low
6	PIRQ 7 polarity. 1 = active high, default 0 = active low
5	Primary Parallel Port Extended Mode 0 = Compatible mode, default 1 = Extended/Bidirectional mode.
4	Primary Parallel Port Disable 1 = Disable, 0 = Enable Power Up Default is set by pin 120 (3221-DP)/pin 96 (3221-SP)
3	Primary Parallel Port Power Down 1 = Power Down, default = 0
2**	Secondary Parallel Port Extended Mode 0 = Compatible mode, default 1 = Extended/Bidirectional mode
1**	Secondary Parallel Port Disable 1 = Disable, 0 = Enable Power Up Default is set by pin 77 (3221-DP)
0**	Secondary Parallel Port Power Down 1 = Power Down 0 = Enable, default

Note: Power Up not applicable to 3221-EP.

Configuration Register Index, BF (R/W)

Bit	Function
7-0	The 8 most significant address bits of the primary parallel port (A9-2) Default 9E (LPT2, at 278-27B)

Configuration Register Index, DA (R/W)**

Bit	Function
7-0	The 8 most significant address bits of the secondary parallel port (A9-2) Default DE (LPT1, at 378-37B).

Configuration Register Index, DB (R/W)

Bit	Function
7	SIRQ4 polarity. 1 = active high; default 0 = active low
6	SIRQ3 polarity. 1 = active high; default 0 = active low
5	SXTAL clock off. 1 = SCLK off, 0 = SCLK on, default
4	Primary serial port disable 1 = Disable, 0 = Enable Power Up default is set by pin 116 (3221-DP)/pin 93 (3221-SP)
3	Primary serial port power down 1 = Power down, 0 = Enable Power Up default is set by pin 116 (3221-DP)/pin 93 (3221-SP)
2	Reserved
1	Secondary serial port disable 1 = Disable, 0 = Enable Power Up default is set by pin 121 (3221-DP)/pin 97 (3221-SP)
0	Secondary serial port power down 1 = Power down, 0 = Enable Power Up default is set by pin 121 (3221-DP)/pin 97 (3221-SP)

Note: Power Up not applicable to 3221-EP.

Configuration Register DC (R/W)

Bit	Function
7-1	The MSB of the Primary Serial Port Address (bits A9-3). Default = 7F (COM1, at 3F8-3FF).
0	When this bit is set to 1, bit A2 of primary parallel port is decoded. Default is 0.

Configuration Register DD (R/W)

Bit	Function
7-1	The MSB of the Secondary Serial Port Address (bits A9-3). Default = 5F (COM2, at 2F8-2FF)
0**	When this bit is set to 1, bit A2 of secondary parallel port is decoded. Default is 0.

Note: Bit 0 is reserved in 3221-SP.

Configuration Register Index, DE (R/W)

Interrupt Request Source

Bit	Function		
7-6	SIRQ3 source		
	b7	b6	
	0	0	Disabled, tri-stated
	0	1	Disabled, tri-stated**
	1	0	Primary serial port
	1	1	Secondary serial port, default
5-4	SIRQ4 source		
	b5	b4	
	0	0	Disabled, tri-stated
	0	1	Disabled, tri-stated**
	1	0	Primary serial port, default
	1	1	Secondary serial port
3-2**	PIRQ7 source		
	b3	b2	
	0	0	Disabled, tri-stated, default
	0	1	Primary serial port
	1	0	Primary parallel port
	1	1	Secondary parallel port

Note: Bits 3-2 are reserved in 3221-SP.

1-0	PIRQ5 source		
	b1	b0	
	0	0	Disabled, tri-stated
	0	1	Secondary serial port
	1	0	Primary parallel port, default
	1	1	Secondary parallel port**

Configuration Register Index, DF (R/W)**

Bit	Function		
7-6	Reserved		
5	RTC interface disable 1 = /RTCCS disabled 0 = /RTCCS enabled, default		
4	Disable Modem Select 1 = Modem CS disabled, default 0 = Modem CS enabled		
3-2			
	b3	b2	
	1	1	Reserved
	1	0	Modem port address = 3E8-3EF (default)
	0	1	Modem port address: 2F8-2FF
	0	0	Modem port address: 3F8-3FF
1-0			
	b1	b0	
	1	1	Reserved
	1	0	Mode 2, EISA Mode
	0	1	Mode 1, AT BUS,
	0	0	Mode 0, Two parallel ports, default

Configuration Register Index, FA (R/W)**

Bit	Function
7	General purpose I/O register, Bit 7
6	General purpose I/O register, Bit 6
5	General purpose I/O register, Bit 5
4	General purpose I/O register, Bit 4
3	General purpose I/O register, Bit 3
2	General purpose I/O register, Bit 2
1	General purpose I/O register, Bit 1
0	General purpose I/O register, Bit 0

Configuration Register Index, FB (R/W)

Bit	Function
7	Reserved
6**	0/2 EXG (Read Only) In mode 1 and mode 2 operation, when the third floppy drive is installed, pin EXTFDD should be pulled high to enable the third floppy drive or be pulled low to disable the third floppy drive. 1 = Third floppy drive enabled 0 = Third floppy drive disabled
5**	EXTFDD (Read Only) In mode 1 and mode 2 operation, when the third floppy drive is installed and pin 0/2 EXG is pulled high, the third floppy drive becomes the bootable drive (drive 0). When pin 0/2 EXG is pulled low, the third floppy drive acts as drive 2. 1 = Third floppy as drive 0 (bootable) 0 = Third floppy as drive 2
4**	MS In mode 1 and mode 2, this bit is to control the output pin MS to support a special 3 1/2", 1.2M drive. When this bit is set to high (1), the MS pin sends a low signal. When this bit is set to low (0), the MS pin sends a high signal to support a 3 1/2", 1.2M drive.
3	FDC, Clock disable 0 = enable, default 1 = disable
2	Reserved
1	FDC disable 0 = enable, 1 = disable Power Up default set by pin 117 (3221-DP)/pin 94 (3221-SP)
0	FDC address 0 = Primary, default 1 = Secondary

Note: Bits 6-4 are reserved in 3221-SP.

Configuration Register Index, FE (R/W)

Bit	Function
7**	Disable general chip select 1 1 = disable, default 0 = enable
6**	Disable general chip select 2 1 = disable, default 0 = enable
5**	Enable SA2 decoding for general chip select 1 1 = enable 0 = disable, default
4**	Enable SA2 decoding for general chip select 2 1 = enable 0 = disable, default
3	Reserved
2	IDE XT selected 0 = IDE AT interface, default 1 = IDE XT interface
1	IDE disable, 1 = IDE disable 0 = IDE enable Power Up default set by pin 13 (3221-DP)/pin 13 (3221-SP)
0	Secondary IDE 1 = secondary 0 = primary, default

Note: Bits 6-4 are reserved in 3221-SP.

Configuration Register Index, BC (R/W)
General chip select 1**

Bit	Function
7-0	Address bits A9-A2

This register defines address for general chip select 1, /GCS1, default 00

Configuration Register Index, BD (R/W)
General chip select 2**

Bit	Function
7-0	Address bits A9-A2

This register defines address for general chip select 2, /GSC2, default 00

FDC Register Descriptions

There are six floppy disk controller registers in the 3221, three registers for the status of signals used in diskette operations, one for data register, and two controller registers. The I/O addresses of these registers are described in the tables below.

Input Register
(HEX 3F0) (R)

The Input Register is a general purpose input register.

Bit	Function
7	0
6	0
5	General purpose programmable bit 5
4	General purpose programmable bit 4
3	General purpose programmable bit 3
2	General purpose programmable bit 2
1	General purpose programmable bit 1
0	General purpose programmable bit 0

Digital Output Register
(HEX 3F2) (8-bits) (W)

The Digital Output Register controls drive motors, drive selection, and feature enable. All bits are cleared by the I/O reset line.

Bit	Function
7	Reserved
6	Motor Enable 2
5	Motor Enable 1
4	Motor Enable 0
3	DMA and Interrupt Enable
2	/Floppy Disk Controller reset
1,0	Drive Select 0 through 2 00 selects drive 0 01 selects drive 1 10 selects drive 2 11 Reserved

Address		Registers	
Primary	**Secondary**	**READ**	**WRITE**
3F0	370	Input register	
3F2	372		Digital output register
3F4	374	Main status register	
3F5	375	Data register	Data register
3F7	377	Digital input register	Diskette control register

Main Status Register
(HEX 3F4) (R)

The main status register controls data flow between the microprocessor and the controller.

Bit	Function
7	Request for Master 1 Data Register ready for transfer
6	Data Input/Output 1 Data transfer from Controller 0 Data transfer from the SD BUS
5	Execution Mode (Non-DMA mode) 1 Execution
4	Controller Busy 1 Controller busy
3	Drive 3 Busy 1 Diskette 3 in seek mode Drive 3 busy
2	Drive 2 Busy 1 Diskette 2 in seek mode Drive 2 Busy
1	Drive 1 Busy 1 Diskette 1 in the seek mode Drive 1 Busy
0	Drive 0 Busy 1 Diskette 0 in the seek mode Drive 0 Busy

Data Register
(HEX 3F5) (R/W)

The Data Register consists of four status registers in a stack. Only one register is presented to the data bus at a time. It stores data, commands and parameters, and provides diskette/drive status information. Data bytes are passed through the data register to program or obtain results after a command.

Status Register 0 (ST0)

Bit	Function
7-6	IC (Interrupt Code) 00 Normal termination of command 01 Abnormal termination of command 10 Invalid command issue 11 Abnormal termination because the ready signal from FDD changed state during command execution
5	SE (seek end) 1 seek end
4	EC (Equipment Check) 1 When a fault signal is received from the FDD, or the track 0 signal fails to occur after 77 step pulses 0 No error
3	NR (Not Ready) 1 Drive is not ready 0 Drive is ready
2	HD (Head address) 1 Head 1 select 0 Head 0 select
1-0	US1,US0. (Unit select) 00 Drive 0 select 01 Drive 1 select 10 Drive 2 select 11 Drive 3 select

Status Register 1 (ST1)

Bit	Function
7	EN (End of Cylinder) 1 When the FDC tries to access a sector beyond the final sector of a cylinder.
6	Not used. This bit is alv ays 0.
5	DE (Data Error) 1 When the FDC detects a CRC error in either the ID field or data field.
4	OR (Over Run) 1 IF the FDC is not serviced by the host system during data transfer within a certain time interval
3	Not used. This bit is always 0.
2	ND (No Data) 1 During execution of Read, Write or Verify Data if the specified sector cannot be found.
1	NW (Not Writable) 1 Set if the "write Protect" signal is detected from the diskette drive during the execution of Write Data.
0	Missing Address Mark 1 When the FDC cannot detect the data address mark or deleted data address mark

Status Register 2 (ST2)

Bit	Function
7	Not used. This bit is always 0
6	CM (Control Mark) 1 If deleted data is encountered during execution of the Read Data or Scan command.
5	DD (Data Error in Data Field) 1 If the FDC detects a CRC error in the data field.
4	WC (Wrong Cylinder) 1 Wrong Cylinder
3	SH (Scan Equal Hit) 1 During execution of the Scan command, if the condition "equal" is satisfied.
2	SN (Scan Not Satisfied) 1 During execution of the Scan command if FDC cannot find a sector.
1	BC (Bad Cylinder) 1 Bad Cylinder
0	MD (Missing Address Mark in Data Field) 1 When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark.

Status Register 3 (ST3)

Bit	Function
7	FT, Fault
6	WP, Write Protected
5	RY, Ready
4	T0, Track 0
3	TS, Two-Side
2	HD, Head Address
1	US1, Unit Select 1
0	US0, Unit Select 0

Digital Input Register
(HEX 3F7) (R)

The Digital Input Register is for diagnostic purposes.

Bit	Function
7	Diskette Change (DSKCHG)
6	Tri-State
5	Tri-State
4	Tri-State
3	Tri-State
2	Tri-State
1	Tri-State
0	Tri-State

Diskette Control Register
(HEX 3F7) (W)

The Diskette Control Register sets the precompensation.

Bit	Function		
7-2	Reserved		
1,0	Transfer Rates Select and Reduced Write Current Control		
	00	500 Kb/s	/RWC=1
	01	300 Kb/s	/RWC=0
	10	250 Kb/s	/RWC=0
	11	Reserved	

Commands

The diskette controller in 3221 is capable of performing fifteen commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: Command, Execution, and Result.

Command

The microprocessor issuses all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After completing the operation, status information and other housekeeping information are made available to the microprocessor.

Command Symbol Descriptions

A0 Address Line 0
A0 controls the selection of main status register (A0=0) or data register (A0=1).

C Cylinder Number
Current or selected cylinder (track), numbers 0 through 76.

D Data
Data pattern to be written into a sector.

D_7 -D_0 Data Bus
8 bit data bus, where D7 stands for the most significant bit, and D0 stands for the least significant bit.

DTL Data Length
The value of this byte is normally ignored by the controller. However, a byte must be written at this location.

EOT End of Track
The final sector number on a cylinder.

GPL Gap Length
The length of gap 3. During Read/ Write commands this value determines the number of bytes that VCO sync keeps low after two CRC bytes. During Format command it determines the size of gap 3.

H Head Address
Head number 0 or 1, as specified in the ID field.

HD Head
Selected head number 0 or 1. (H=HD in all commands)

HLT Head Load Time
The head load time in the selected FDD (2 to 254 ms in 2 ms increments.)

HUT Head Unload Time
Time after a Read or Write operation. (16 to 240 ms in 16 ms increments).

MF FM or MFM Mode
Must be 1 to select MFM mode.

MT Multitrack
If MT is high, a multitrack operation is performed. If MT=1 after finishing a read/write operation on side 0, FDC automatically starts searching for sector 1 on side 1.

N Number
The number of data bytes written in a sector.

NCN New Cylinder Number
New cylinder number reached as a result of the seek operation; desired position of head.

ND Non-DMA Mode

PCN Present Cylinder Number
Cylinder number at the completion of the Sense Interrupt Status command, current position of the head.

R Record
The sector number to be read or written.

R/W Read/Write
Either a Read or Write signal.

SC Sector
Number of sectors per cylinder.

SK Skip
Skip deleted data address mark.

SRT Stepping Rate
These bits indicate the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH=1ms, EH=2 ms, etc.).

ST0-ST3
Status 0-Status 3
One of the four registers that store status information after a command has been executed. This information is available during the result phase after command execution. These registers must not be confused with the main status register (selected by A0=0). ST0-ST3 are read only after a command has been executed and only if they contains information relevant to the command.

STP Scan Test
If STP=1 during a scan operation, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA). If STP=2, alternate sectors are read and compared.

US0-1 Unit Select
Selected drive number 0 or 1.

COMMAND FORMAT

The following commands can be issued to the controller. An "x" indicates a "don't care" condition.

READ DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	0	1	1	0
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

READ DELETED DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	1	1	0	0
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

READ A TRACK

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MF	SK	0	0	0	1	0
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

READ ID

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	0	1	0
Byte 1	x	x	x	x	x	HD	US1	US0

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

WRITE DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	0	1	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

WRITE DELETED DATA

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	1	0	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Data Length							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

FORMAT A TRACK

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	1	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Number of Data Bytes in Sector							
Byte 3	Sectors per Cylinder							
Byte 4	Gap Length							
Byte 5	Data							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

SCAN EQUAL

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	0	0	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

SCAN LOW OR EQUAL

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	1	0	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

SCAN HIGH OR EQUAL

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	1	1	0	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	Cylinder Number							
Byte 3	Head Address							
Byte 4	Sector Number							
Byte 5	Number of Data Bytes in Sector							
Byte 6	End of Track							
Byte 7	Gap Length							
Byte 8	Scan Test							

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Status Register 1							
Byte 2	Status Register 2							
Byte 3	Cylinder Number							
Byte 4	Head Address							
Byte 5	Sector Number							
Byte 6	Number of Data Bytes in Sector							

RECALIBRATE

Command Phase
(This command has no result phase.)

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	x	x	x	x	x	0	US1	US0

SENSE INTERRUPT STATUS

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0							
Byte 1	Present Cylinder Number							

SPECIFY

Command Phase
(This command has no result phase.)

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	SRT				HUT			
Byte 2	HLT							ND

SENSE DRIVE STATUS
Command phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	x	x	x	x	x	HD	US1	US0

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status 3 Register							

SEEK

Command Phase
(This command has no result phase.)

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	1
Byte 1	x	x	x	x	x	HD	US1	US0
Byte 2	New Cylinder Number for Seek							

INVALID

Result Phase

The following status byte is returned to the microprocessor when an invalid command is received.

	7	6	5	4	3	2	1	0
Byte 0	Status 0 Register							

Serial Port Interface

Each serial port interface has three types of internal registers: Control, Status, and Data registers.

Control registers

Bit Rate Select Register DLL
(Divisor Latch LSB)
Bit Rate Select Register DLM
(Divisor Latch MSB)
Line Control Register
Interrupt Enable Register
Interrupt Identification Register
Modem Control Register

Status registers

Line Status Registers
Modem Status Register

Data registers

Receiver Buffer Register
Transmitter Holding Register
Scratch Register

Table 1 summarizes the serial port registers.

Table 1 Serial Port Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Receiver Buffer Register (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
Transmitter Holding Register (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
Divisor Latch (LS)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (MS)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Interrupt Enable Register	0	0	0	0	Enable Modem Status Interrupt	Enable Receiver Line Status Interrupt	Enable Trans-mitter Holding Register Interrupt	Enable Received Data Avail-able Interrpt
Interrupt Identification Register	0	0	0	0	0	Interrupt ID Bit 1	Interrupt ID Bit 0	"0" IF Interrpt Pending
Line Control Register	Divisor Latch Address Bit	Set Break	Stick Parity	Even Parity Select	Parity Enable	Number of Stop Bits	Word Length Select Bit 1	Word Length Select Bit 0
Modem Control Register	0	0	0	Loop	Interrupt Enable	Not used	Request to Send	Data Terminal Ready
Line Status Register	0	Trans-mitter Empty	Trans-mitter Holding Register Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Data Ready
Modem Status Register . .	Data Carrier Detect	Ring Indicator	Data Ready Set	Clear to Send	Delta Receive Line Signal Detect	Trailing Edge Ring Indicator	Delta Data Set Ready	Delta Clear to Send
Scratch Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Address, Read, and Write inputs are used with the Divisor Latch Access Bit (DLAB) in the Line Control register bit 7 [LCR(7)] to select the register to be read or written. Refer to Table 2 for register select states.

Table 2 Serial Port Internal Register Selection

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver buffer register (read only)
0	0	0	0	Transmitter holding register (write only)
0	0	0	1	Interrupt enable register
x	0	1	0	Interrupt identification register (read only)
x	0	1	1	Line control register
x	1	0	0	Modem control register
x	1	0	1	Line status register
x	1	1	0	Modem status register
x	1	1	1	Scratch register
1	0	0	0	Divisor latch (LSB)
1	0	0	1	Divisor latch (MSB)

x = Don't care

Note that the serial port is accessed only when internal chip select signal /CSSE0(1) is low.

Line Control Register (LCR)

The Line Control Register controls the format of a data character. The contents of the LCR can be read precluding the need to store line characteristics in system memory. Table 3 contains the contents of the Line Control register.

Table 3 Line Control Register

Bit	Function	Logic 1	Logic 0
0	Word length select Bit 0		
1	Word length select Bit 1		
2	Stop bit select	1.5 or 2 stop bits	1 stop bit
3	Parity enable	Enabled	Disabled
4	Even parity select	Even parity	Odd parity
5	Stick parity	Enabled	Disabled
6	Set break	Enabled	Disabled
7	Divisor latch access bit		

Bit 0-1 The number of bits in each serial character is programmed according to the following states.

LCR(1)	LCR(0)	Word length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 2 Specifies the number of stop bits in each character transmitted. If Bit 2 = 0, one stop bit is generated or checked in the transmitted data. If Bit 2 = 1 when a 5-bit word is selected, 1.5 stop bits are generated. If Bit 2 = 1 when a 6-, 7- or 8-bit word is selected, two stop bits are generated. The receiver checks the first stop bit only regardless of the number of stop bits selected.

Bit 3 When high, generates and checks a parity bit between the last data word bit and stop bit of the serial data.

Bit 4 When parity is enabled (Bit 3 = 1), and Bit 4 = 0, odd parity is selected. When parity is enabled and Bit 4 = 1, even parity is selected.

Bit 5 When parity is enabled and Bit 5 = 1, a parity bit is transmitted and received in the opposite state from the state indicated by Bit 4. Parity can therefore be forced to a known state and the receiver can check the parity bit in a known state.

Bit 6 When set to 1, serial output is forced to the spacing (logic 0) state. The break is disabled when this bit is set to 0. Bit 6 acts only on serial output and has no effect on the transmitting logic. Bit 6 enables the CPU to alert a terminal in a computer system. If the following sequence is used, no erroneous or extraneous characters are transmitted because of the break.

1. Load an all zeros, pad character, in response to Line Status register Bit 5.

2. Set break in response to the next Line Status register Bit 5.

3. Wait for the transmitter to become idle (Line Status register Bit 6), and clear break when normal transmission must be restored.

Bit 7 Must be set high to access the Divisor latches DLL and DLM of the Baud rate generator during a read or write operation. This bit must be input low to access the Receiver buffer, the Transmitter holding, or the Interrupt enable registers.

Line Status Register (LSR)

The Line Status Register is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the serial port interface. Refer to Table 4 for bit definitions.

Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification register). This interrupt is enabled by setting the Interrupt Enable register Bit 2 to 1. Bits 1-4 are cleared when the Line Status register is read.

Bits 1-3 are three error flags that provide the status of an error condition detected in the receiver circuitry: Overrun error, Framing error, and Parity error. Error flags are set high by an error condition when stop bits are received.

Table 4 Line Status Register

Bit	Function	Logic 1	Logic 0
0	Data ready (DR)	Ready	Not ready
1	Overrun error (OE)	Error	No error
2	Parity error (PE)	Error	No error
3	Framing error (FE)	Error	No error
4	Break interrupt (BI)	Break	No break
5	Transmitter holding register empty (THRE)	Empty	Not empty
6	Transmitter empty (TEMT)	Empty	Not empty
7	Not used		

Bit 0 This bit is set high when an incoming character is received and transferred into the Receiver Buffer register. When the CPU reads the data in the Receiver Buffer register, Bit 0 is reset low.

Bit 1 Overrun error means that the Receiver Buffer register was not read by the CPU before the next character was transferred into the Receiver Buffer register, overwriting the previous character. This bit is reset when the CPU reads the contents of the Line Status register.

Bit 2 A parity error means that the last character received had a parity error based on the programmed and calculated parity of the received character (Line Control register Bit 4). This bit is set high when a parity error is detected, and reset low when the CPU reads the contents of the Line Status register.

Bit 3 A framing error means that the last character received had incorrect (low) stop bits (caused when the required stop bit is absent or by a stop bit too short to be detected). This bit is high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). This bit is reset low when the CPU reads the contents of the Line Status register.

Bit 4 This bit indicates that the last character received was a break character. A break character is defined as an invalid but complete data character, including parity and stop bits. This bit is set high when the received data input is held in the spacing (logic 0) state for a longer time than a full word transmission time (start bit + data bits + parity + stop bits). Bit 4 is reset when the CPU reads the contents of the Line Status register.

Bit 5 This bit indicates that the Transmitter Holding register is empty and can receive another character. If the interrupt is enabled (Interrupt Enable register Bit 1), this bit when active causes an interrupt. The interrupt is cleared when the Interrupt Identification register is read.

Bit 5 is set high when a character is transferred from the Transmitter Holding register into the Transmitter Shift register. This bit is reset low when the CPU loads the Transmitter Holding register. Bit 5 is NOT reset when the CPU reads the Line Status register.

Bit 6 This bit is set high when the Transmitter Holding register and the Transmitter Shift register are both empty. When a character is loaded into the Transmitter Holding register, this bit is set low and remains low until the character is transferred out of SOUT0(1) (Serial output pin). Bit 6 is NOT reset when the CPU reads the Line Status register.

Bit 7 This bit is always zero.

Modem Control Register (MCR)

The Modem Control Register controls the interface with the modem or data set. This register can be read or written. Table 5 contains Modem Control register bit definitions.

Table 5 Modem Control Register

Bit	Function
0	Data terminal ready (DTR)
1	Request to send (RTS)
2	Not used
3	Interrupt enable
4	Loopback
5	0
6	0
7	0

Bit 0 When set to 1, the Data terminal ready [/DTR0(1)] output is forced to a logic 0. When this bit is reset to a logic 0, /DTR0(1) output is forced to a logic 1.

Bit 1 When set to 1, the Request to send [/RTS0(1)] output is forced to a logic 0. When this bit is reset to a logic 0, /RTS0(1) output is forced to a logic 1.

Bit 3 When set high, Serial port interrupt (SIRQ3, SIRQ4) output is enabled.

Bit 4 This bit provides a local loopback feature to perform diagnostic testing of the channel. When set high, SOUT0(1) is set to the marking state (logic 1), and the receiver data input Serial Input [SIN0(1)] is disconnected. The output of the Transmitter Shift register is looped back into the Receiver Shift register input. The four modem control inputs are disconnected. Modem control outputs are connected to the four modem control inputs internally. Modem control output pins are forced to the high (inactive state).

In the diagnostic mode, data transmitted is received immediately so the processor can verify the transmit and receive data paths of the selected serial port.

Bits 5-7 Permanently set to logic 0.

Modem Status Register (MSR)

The Modem Status Register provides the CPU with the status of the modem input lines from the modem or peripheral devices. The CPU can read the serial port modem signal inputs by accessing the data bus interface of the 3221-DP. Four bits in this register indicate if the modem inputs have changed since the last read of the Modem status register. These bits are set high when a control input from the modem changes state. When the CPU reads the Modem Status register, these bits are reset low.

The /CTS0(1), /DSR0(1), /RI0(1) and /RLSD0(1) signals are the modem input lines for the channel. Bits 4 through 7 are status indications of these lines. If the modem status interrupt in the Interrupt Enable register Bit 3 is enabled, a change of state in a modem input signals is reflected by the modem status bits in the IIR register and an interrupt is generated. The Modem Status register is a priority 4 interrupt. Refer to Table 6 for bit definitions. Note that the state of the status bit is an inverted version of the actual input pin.

Table 6 Modem Status Register

Bit	Function
0	Delta clear to send
1	Delta data set ready
2	Trailing edge of ring indicator
3	Delta data carrier detect
4	Clear to send
5	Data set ready
6	Ring indicator
7	Data carrier detect

Bit 0 Indicates that /CTS0(1) input to the serial port interface has changed state since the last time it was read by the CPU.

Bit 1 Indicates that /DSR0(1) input to the serial port interface has changed state since the last time it was read by the CPU.

Bit 2 Indicates that /RI0(1) input to the serial port interface has changed state since the last time it was read by the CPU. Low to high transitions on Bit 6 do not activate this bit.

Bit 3 Indicates that /RLSD0(1) input to the serial port interface has changed state since the last time it was read by the CPU.

Bit 4 This bit is the complement of /CTS0(1) input from the modem. This input tells the serial port that the modem is ready to receive data from the transmitter output of the serial port. If the serial port interface is in loop mode (Modem Control register Bit 4 = 1), this bit is equivalent to Modem Control register Bit 1 (request to send).

Bit 5 This bit is the complement of the /DSR0(1) input from the modem to the serial port. This input tells the CPU that the modem is ready to provide received data to the serial port receiver circuitry. If the channel is in loop mode (Modem Control register Bit 4 = 1), this bit is equivalent to Modem Control register Bit 0 (data terminal ready).

Bit 6 This bit is the complement of the /RI0(1) pin. If the channel is in loop mode (Modem Control register Bit 4 = 1), this bit is not connected in the Modem Control register.

Bit 7 This bit is the complement of receiver line detect signal input and is equivalent to Modem control register Bit 3.

Modem status inputs reflect the modem input lines with any change of status. Reading the Modem Status register clears the delta modem status indications but does not affect the status bits. The status bits reflect the state of the input pins regardless of mask control signals. If bits 0-3 are true, and a state change occurs during a read operation, the state change is not reflected in the Modem Status register. If bits 0-3 are false, the state change is indicated after the read.

Setting status bits is inhibited for the Line Status register and Modem Status register during status read operations. If a status condition is generated during a CPU read, the status bit is not set until the trailing edge of the read.

If a status bit is set during a read operation, and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again.

Programmable Baud Rate Generator

The serial port interface in 3221 contains a programmable Baud Rate Generator that divides the clock from DC to 3.1 MHz. Any divisor from 1 to 2^{16-1} can be used. The output frequency of the baud generator is 16X the

data rate [divisor # = clock + (baud rate x 16)]. The divisor is stored in a 16-bit binary format by two 8-bit divisor latch registers. These divisor latch registers must be loaded during initialization. A 16-bit baud counter is immediately loaded after either of the divisor latches is loaded to prevent long counts on initial load.

The serial port receiver circuitry in the 3221 is programmable for 5, 6, 7 or 8 data bits per character. Word with less than eight bits are right justified, LSB = Data Bit 0, which is the first data bit received. Unused bits in a character less than eight bits are output low to the parallel output by the serial port.

Data received at the SIN0(1) (serial input) pin is shifted into the **Receiver Shift Register** by the clock (16X) provided at the XIN input. Based on the position of the start bit, this clock is synchronized to the incoming data. When a complete character is shifted into the Receiver Shift register, the assembled data bits are loaded in parallel into the **Receiver Buffer Register (RBR)**. The Data Ready flag in the Line Status register is set.

Transmitter Holding Register (THR) and Receiver Buffer Register

The Transmitter Holding Register and Receiver Buffer Register are data registers that hold from five to eight bits of data. If fewer than eight data bits are transmitted, bit 0 is always the first serial data bit received and transmitted. Data registers are buffered twice to allow read and write operations to be executed at the same time the UART is converting parallel to serial and serial to parallel.

The data received is buffered twice to permit continuous data reception without loss of data. As the Receiver Shift register is shifting a new character into the serial port, the Receiver Buffer register is holding a previously received character for the CPU. If data in the Receiver Buffer register is not read before complete reception of the next character, the data in the Receiver register goes low. The overrun condition is flagged by an Overrun error (Bit 1 of the Line Status register). Table 7 contains Receiver Buffer Register bit definitions.

Table 7 Receiver Buffer Register

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

The Transmitter Holding Register holds parallel data from the data bus until the Transmitter Shift register is empty and ready to accept a new character. The receiver word length and transmitter and number of stop bit are the same. If the character has less than eight bits, unused bits are ignored by the transmitter at the microprocessor data bus. Table 8 contains the bit definitions of the Transmitter Holding register.

Table 8 Transmitter Holding Register

Bit	Function
0	Data Bit 0 *
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

* Bit 0 is the first serial data bit transmitted.

Scratch Register (SR)

The Scratch Register is an 8-bit Read/Write register. This register does not affect either channel in the serial port. It is used by programmers to hold data temporarily. Table 9 contains bit definitions.

Table 9 Scratch Register

Bit	Function
0	Data Bit 0
1	Data Bit 1
2	Data Bit 2
3	Data Bit 3
4	Data Bit 4
5	Data Bit 5
6	Data Bit 6
7	Data Bit 7

Interrupt Identification Register (IIR)

The Interrupt Identification Register has the interrupt capability to interface to current microprocessors. The serial port interface prioritizes interrupts into four levels to minimize software overhead during data character transfer. The four levels of interrupt conditions include

Priority 1	Receiver Line Status
Priority 2	Received Data Ready
Priority 3	Transmitter Holding Register Empty
Priority 4	Modem Status

The Interrupt Identification register stores information that an interrupt is pending and the type of interrupt. When addressed during chip select time, this register indicates the highest priority interrupt pending. No other interrupts are acknowledged until the CPU services this interrupt. Table 10 contains Interrupt Identification register bit definitions. Table 11 contains interrupt identification, set and reset information.

Table 10 Interrupt Identification Register

Bit	Function
0	Indicates a pending interrupt
1-2	Identifies highest priority pending
3-7	0

Bit 0 Indicates if an interrupt is pending. When this bit is low, an interrupt is pending and the register contents can be used as a pointer to the appropriate interrupt service routine. When this bit is high, no interrupt is pending.

Bits 1-2 Identify the highest priority interrupt pending.

Bits 3-7 Must be set to 0.

Table 11 IIR Interrupt ID, Set and Reset

Interrupt Identification				Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
x	x	1		None	None	
1	1	0	1	Receiver line status	OE, PE FE, or BI	LSR Read
1	0	0	2	Received data available	Received data available	RBR Read
0	1	0	3	THRE	THRE	IIR Read if THRE is the interrupt source or THR write
0	0	0	4	Modem status	/CTS0(1), /DSR0(1). /RI0(1), /RLSD0(1)	MSR Read

x = not defined

Interrupt Enable Register (IER)

The Interrupt Enable Register is a write register that enables the four serial port interrupts independently. The interrupts activate the interrupt output. All interrupts are disabled by resetting Bits 0-3 of this register. Interrupts are enabled by setting the appropriate bits of this register high. When interrupts are disabled, the Interrupt Identification register and the active (high) SIRQ3(4) signal is inhibited in the 3221-DP while the INTSE0(1) signal in the 3221-EP and 3221-SP is inhibited. All other system functions operate normally, including the setting of the Line Status register and the Modem Status register. Table 12 contains Interrupt Enable register bit definitions.

Table 12 Interrupt Enable Register

Bit	Function
0	Received Data Available interrupt
1	Transmitter holding register empty interrupt
2	Receiver line status interrupt
3	Modem Status interrupt
4-7	Must be set to logic 0

Bit 0 Received Data Available interrupt.
1 = Enables
0 = Disables

Bit 1 Transmitter holding register empty interrupt.

1 = Enables
0 = Disables

Bit 2 Receiver line status interrupt.
1 = Enables
0 = Disables

Bit 3 Modem Status interrupt.
1 = Enables
0 = Disables

Bits 4-7 Must be set to logic 0.

Transmitting

The serial port interface transmitting function includes the Transmitter Holding register, Transmitter Shift register, and the associated control logic. Bits 5 and 6 in the Line Status Register indicate the status of the Transmitter Holding register and the Transmitter Shift register. To transmit a 5- to 8-bit word, the word is written to the Transmitter Holding register through SD0-SD7. The microprocessor performs a write operation only if it is transmitted.

Bit 5 of the Line Status register is high when the word is automatically transferred from the Transmitter Holding register to the Transmitter Shift register when the start bit is transmitted.

When the transmitter is idle, Bits 5 and 6 of the Line Status register are high. The first word written causes Bit 5 to be reset to zero. After the transfer, Bit 5 returns high. Bit 6 remains low while the data word is transmitted. If a second character is transmitted to the Transmitter Holding register, Bit 5 of the Line Status register is reset low. Because the data word cannot be transferred from the Transmitter Holding register to the Transmitter Shift register until its empty, Bit 5 of the Line Status register remains low until the word is completely transmitted. When the last word is transmitted out of the Transmitter Shift register, Bit 6 of the Line Status register is set high. Bit 5 of the Line Status register is set high one transfer time later.

Receiving

Serial asynchronous data is input into SIN0(1) (Serial Input pin). The idle state of the line providing the input into the SIN pin is high. Start bit detection circuitry continually searches for a high to low transition. When a transition is detected, a counter is reset. Count is the 16X clock to 7 1/2, which is the center of the start bit. If the SIN signal is still low at the mid-bit sample of the start bit, the start bit is considered valid. By verifying the start bit, the receiver is prevented from assembling a false data character caused by a low going noise spike on the Serial Input pin.

The Line Control register determines the number of data bits in a character, the number of stop bits, if parity is used, and the polarity of parity. The Line Status register provides status for the receiver to the Receiver Buffer register. The data received (indicated by Bit 0 of the Line Status register) is set high. The CPU reads the Receiver Buffer register through SD0-SD7. This read resets Bit 0 of the Line Status register. If a character is not read before a new character transfer from the Receiver Status register to the Receiver Buffer register, the overrun error status bit is set (Line Status register Bit 1). The parity check looks for even or odd parity on the parity bit which precedes the first stop bit. The parity error is set in Line Status register Bit 2 if an error is detected. If the stop bit is not high, a framing error is indicated by Line Status register Bit 3.

The center of the start bit is defined as clock count 7 1/2. If the data received by the Serial Input pin is a symmetrical square wave, the center of the data cells occurs within +/- 3.125% of the mid-point. This is a 46.875% error margin. The start bit can begin as much as one 16X clock cycle before it is detected.

Baud Rate Generator

The Baud Rate generator generates clocking for the UART function and provides standard

ANSI/CCITT bit rates. An external clock into CLK provides the oscillator driving the Baud Rate generator.

The Divisor Latch registers DLL and DLM, and external frequency determine the data rate. The bit rate is selected by programming the two divisor latches. When DLL is set to 1, and DLM is set to 0, the divisor divides by 1 (provides maximum baud rate for a given input frequency at the CLK input).

The Baud Rate generator can use three different frequencies, 1.8432 MHz, 2.4576 MHz, or 3.072 MHz, to provide standard baud rates. With these frequencies, standard bit rates from 50 to 38.5 kbps are available. Refer to Tables 13, 14, and 15 standard baud rates with these frequencies.

Table 13 Baud Rates for 1.8432 MHz Clock

Baud Rate	Divisor	Percent Error
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

Table 14 Baud Rates for 2.4576 MHz Clock

Baud Rate	Divisor	Percent Error
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

Table 15 Baud Rates for 3.072 MHz Clock

Baud Rate	Divisor	Percent Error
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Resetting

The /RESET input must be held low for 500 ns to reset the serial port circuits to an idle mode until initialization. A low state on the /RESET signal causes the following events.

1. Initializes the transmitter and receiver internal clock counters.

2. Clears the Line Status register except Bits 5 and 6 which are set. Also clears the Modem Control register. All discrete lines, memory elements and logic associated with these registers are also cleared or turned off. The Line Control register, Divisor latches, Receiver Buffer register and Transmitter Buffer register are not affected.

After the rest condition is removed, the serial port remains idle until programmed. A hardware reset sets Bits 5 and 6 of the Line Status register. When interrupts are enabled, Bit 5 activates the interrupt. Refer to Table 16 for summary of reset effects.

Table 16 Reset Summary

Register/Signal	Reset Control	Reset
Interrupt Enable reg	Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification reg	Reset	Bit 0 is high, Bits 1-2 low Bits 3-7 are permanently low
Line Control reg	Reset	All bits low
Modem Control reg	Reset	All bits low
Line Status reg	Reset	Bits 0-4 and 7 are low, Bits 5-6 high
Modem Status reg	Reset	Bits 0-3 low, Bits 4-7 input signal
Serial Output (SOUT)	Reset	High
Interrupt (Receiver line status)	Read LSR/Reset	Low
Interrupt (Receiver data available)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (Modem Status)	Read MSR/Reset	Low
/RTS	Reset	High
/DTR	Reset	High

Parallel Port Interface

The parallel port interface in the 3221 provides compatibility for a Centronics type printer. Configuration register BE Bit 5 = 1, sets the primary parallel port into extended bidirectional mode, Bit 2 = 1, sets the secondary parallel port into extended bidirectional mode. Table 17 lists the registers associated with the parallel port interface.

The microprocessor reads information on the parallel bus through Read Data register. The read and write functions of a register are controlled by the state of the read pin (/IOR) and write pin (/IOW).

The microprocessor reads the status of the printer in the five most significant bits of the Read Status register. Table 18 contains the bit definitions for this register.

Table 17 Parallel Port Interface Register Summary

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read Status	/BUSY	/ACK	PE	SLCT	/ERROR	1	1	1
Read Control	1	1	1	IRQENB	SLIN	/INIT	AUTOFD	STROBE
Write Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write Control	1	1	0	IRQENB	SLIN	/INIT	AUTOFD	STROBE

Table 18 Read Status Register

Bit	Function
0	1
1	1
2	1
3	Error
4	Printer select
5	Paper Empty
6	Acknowledge
7	Printer busy

The Read Control Register is for reading the state of the control lines. The Write Control Register sets the state of the control lines. Table 19 contains the bit definitions for the Write Control Register.

Table 19 Write Control Register

Bit	Function
0	Strobe to inform the printer of the presence of a valid byte on the parallel bus
1	Autofeed the paper
2	Initialize the printer
3	Select IN
4	Interrupt enable
5	Direction
6	Must be set to 1
7	Must be set to 1

The Microprocessor can write a byte to the parallel bus through the Write Data Register. When parallel ports are set into extended mode (Bit 5, 2 of Register BE = 1), Control Bit 5 will control the direction of the parallel ports. When set to 1, the parallel ports can receive data from external devices. When set to 0, the parallel ports are configured as the standard Centronics compatible parallel ports. Default is zero.

Decoder

The parallel port address decoder selects registers according to the states of the signals listed in Table 20.

Table 20 Address Decoder Register Selection

Control Signals					
/IOR	/IOW	/CSPA*	A1	A0	Register Selected
0	1	0	0	0	Read Data register
0	1	0	0	1	Read Status register
0	1	0	1	0	Read Control register
0	1	0	1	1	Invalid
1	0	0	0	0	Write Data register
1	0	0	0	1	Invalid
1	0	0	1	0	Write Control register
1	0	0	1	1	Invalid

* /CSPA is an internal signal to parallel port logic.

Interrupt Control Logic

The serial and parallel ports generate their own interrupts to the CPU. The INTPA (PIRQ5 or PIRQ7) signal from the parallel port controls the parallel port interrupt mechanism. The serial port generates the INTSE0(1) (SIRQ3 or SIRQ4) signal for interrupt service.

Rating Specifications

Absolute Maximum Ratings*

TA = 25° C

Parameter	Symbol	Min	Max	Units
Power supply voltage	VDD	-0.5	7.0	V
Input, Output voltage	Vin Vout	-0.5	VDD +0.5	V
DC Current Drain per Pin any input or output**	I		25	mA
DC Current Drain VDD and VSS Pins	I		100	mA
Storage Temperature	Tstg	-55	150	°C
Lead Temperature less than 10sec. solder	TI		250	°C
Operating Temperature Commercial	Toper	0	70	°C

* Exposing the device to stresses above those listed can cause permanent damage. The maximum rating is a stress rating only, and functional operation at the maximum is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

** Except 48 mA output pads which have a limit of 48mA.

Capacitance

TA = +25° C, VDD = 5 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input Capacitance	CI		10	pF	fc = 1 MHz unmeasured pins to ground
Output Capacitance	CO		10	pF	
I/O Capacitance	CIO		10	pF	

DC Specifications

TA = 0° C to +70° C, VDD = +5 V +/- 10%

EP SA0-9, SA1015, TC, /DACK, AEN, /IOR, /IOW, /CTS0-1, /DSR0-1, RI0-1, /DCD0-1, SIN0-1, SXTAL1,FXTAL1, (/ERROR1, /A1215L), (BUSY1, 0/2EXG), (SLCT1, EXTFDD), (PE1, A11), (ACK1, A10),TEST,/PWRDOWN, DISPAR2, TEST

DP SA0-9, SA1015, TC, /DACK, AEN, /IOR, /IOW, /CTS0-1, /DSR0-1, RI0-1, /DCD0-1, SIN0-1, FXTAL1, (/ERROR1, /A1215L), (BUSY1, 0/2EXG), (SLCT1, EXTFDD), (PE1, A11), (ACK1, A10),TEST,/PWRDOWN

SP SA0-9, SA1015, TC, /DACK, AEN, /IOR, /IOW, /CTS0-1, /DSR0-1, RI0-1, /DCD0-1, SIN0-1, FXTAL1

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VDD = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VDD = 5 +/- 0.5 V
Input low leakage current	IIL		-10.0	uA	VIN = 0.0V
Input high leakage current	IIH		10.0	uA	VIN = VDD

RESET, /DSKCHG, /RDDATA, /WP, /INDEX, /ERROR0, BUSY0, SLCT0, PE0, /ACK0

Parameter	Symbol	Min	Max	Unit	Test Condition
Threshold voltage low to high	VTL H	2.4	3.0	V	VDD = 5 +/- 0.5 V
Threshold voltage high to low	VTHL	1.2	1.8	V	VDD = 5 +/- 0.5 V
Hysteresis	VH	0.9	1.5	V	
Input low leakage current	IIL		-10	uA	VIN = 0.0V
Input high leakage current	IIH		10.0	uA	VIN = 5.5V

FXTAL2, SXTAL2*

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL=4.0mA
Output high voltage	VOH	2.4		V	IOH=-4.0mA

* This applies only to 3221-EP.

EP DBIR, /MODEMCS, (/PDRD, EISA6), (/PDLAT, /KBDCS), (/IENH, EISA4), (/IENL, EISA5), (PDOEO, RTCAS)

DP DBIR, EISA6, /KBDCS, (/IENH, EISA4), (/IENL, EISA5), RTCAS

SP DBIR, IENH, /IENL

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 4mA
Output high voltage	VOH	2.4		V	IOH = 4mA
Tristate Output Leakage Current	IOZ	-10.0	10	uA	0V<VOUT<VDD

EP/DP SIRQ3, SIRQ4, (/HCS0, EISAIDCS), FIRQ6, DRQ, PIRQ5, PIRQ7, TRK0, (HCS1, EISA3)

SP SIRQ3, SIRQ4, /HCS0, FIRQ6, DRQ, PIRQ5, TRK0, HCS1

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 16mA
Output high voltage	VOH	2.4		V	IOH = -16mA
Tristate Output Leakage Current	IOZ	-10.0	10	uA	0V<VOUT<VDD

/MO0-2, /DS0-2, /STEP, /WE, /WRDATA, /DIR, /HEAD, RWC, (MS**)

Parameter	Symbol	Min	Max	Unit	Test Condition
Output low voltage	VOL		0.4	V	IOL = 48mA
Output high leakage current	ILOH		10	mA	VOUT=VDD

EP/DP SOUT0-1, /DTR0-1, /RTS0-1, (/IOCS16, EISA7)

SP SOUT0-1, /DTR0-1, /RTS0-1, /IOCS16

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VDD = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VDD = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VDD
Output low voltage	VOL		0.4	V	IOL = 4.0mA
Output high voltage	VOH	2.4		V	IOH = -4.0mA
Tristate Output Leakage Current	IOZ	-10.0	10.0	uA	0V<VOUT<VDD

EP SD0-7, /STROBE0, /AUTOFD0, /INIT0, /SLIN0, (/STROBE1, /RTCDS), (/AUTOFD1, /RTCWR), (/INIT1, /GCS1, EISA0), (/SLIN1, /GCS2, EISA1), (ID7, EISA2), P0D0-7, (P1D0, EISA6), (P1D1, KBDCS), (P1D2, RTCAS, /MODEM CS), P1D3-7

DP SD0-7, /STROBE0, /AUTOFD0, /INIT0, /SLIN0, (/STROBE1, /RTCDS), (/AUTOFD1, /RTCWR), (/INIT1, /GCS1, EISA0), (/SLIN1, /GCS2, EISA1), (ID7, EISA2)

SP SD0-7, /STROBE, /AUTOFD, /INIT, /SUN, P0D0-7

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VDD = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VDD = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VDD
Output low voltage	VOL		0.4	V	IOL = 16mA
Output high voltage	VOH	2.4		V	IOH = -16.0mA
Tristate Output Leakage Current	IOZ	-10.0	10.0	uA	0V<VOUT<VDD

P0D0-7*

Parameter	Symbol	Min	Max	Unit	Test Condition
Input low voltage	VIL		0.8	V	VDD = 5 +/- 0.5 V
Input high voltage	VIH	2.0		V	VDD = 5 +/- 0.5 V
Input low current	IIL		-10.0	uA	VIN = 0.0V
Input high current	IIH		10.0	uA	VIN = VDD
Output low voltage	VOL		0.4	V	IOL = 24mA
Output high voltage	VOH	2.4		V	IOH = -24mA
Tristate Output Leakage Current	IOZ	-10.0	10.0	uA	0V<VOUT<VDD

AC Specifications

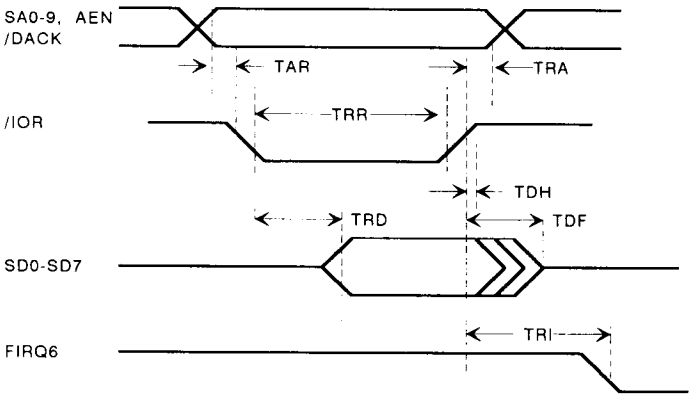
TA = 0°C to 70°C, VDD = +5V ± 10%

Parameter	Symbol	Min	Typ(2)	Max	Unit	Conditions
SA9-0, AEN, /DACK, setup time to /IOR falling edge	TAR	25			ns	
SA9-0, AEN, /DACK, hold time from /IOR rising edge	TRA	0			ns	
/IOR width	TRR	80			ns	
Data access time from /IOR falling edge	TRD			80	ns	CL = 100pf
Data hold from /IOR rising edge	TDH	10			ns	CL = 100pf
SD to float from /IOR rising edge	TDF	10		50	ns	CL = 100pf
FIRQ6 delay from /IOR rising edge	TRI			360/ 570/675(1)	ns	
SA9-0, AEN, /DACK, setup time to /IOW falling edge	TAW	25			ns	
SA9-0, AEN, /DACK, hold time from /IOW rising edge	TWA	0			ns	
/IOW width	TWW	60			ns	
Data setup time to /IOW rising edge	TDW	60			ns	
Data hold time from /IOW rising edge	TWD	0			ns	
FIRQ6 delay from /IOW rising edge	TWI			360/ 570/675(1)	ns	

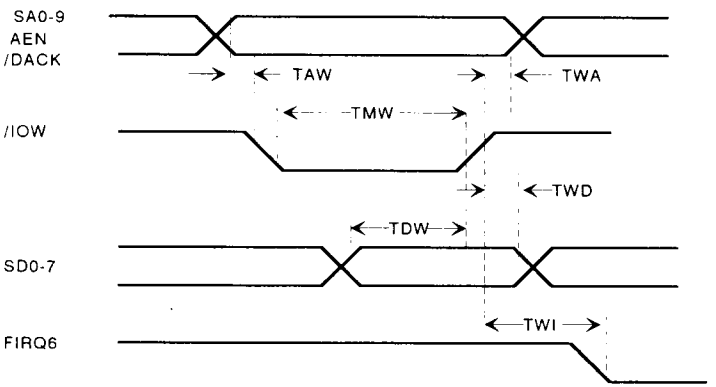
Parameter	Symbol	Min	Typ(2)	Max	Unit	Conditions
DRQ cycle time	TMCY	27			us	
DRQ delay time from /DACK falling edge	TAM			50	ns	
DRQ to /DACK delay	TMA	0			ns	
/DACK width	TAA	260/430/510(1)			ns	
/IOR delay from /DRQ	TMR	0			ns	
/IOW delay from /DRQ	TMW	0			ns	
/IOW or /IOR response time from DRQ	TMRW		12/20/24(1)		us	
TC Width	TTC	135/220/260(1)			ns	
RESET Width	TRST	1.8/3/3.5(1)			us	
/INDEX Width	TIDX	0.5/0.9/1.0(1)			us	
/DIR setup time to /STEP	TDST	1.0/1.6/2.0(1)			us	
/DIR hold time from /STEP	TSTD	24/40/48.0(1)			us	
/STEP pulse width	TSTP	6.8/11.5/13.8(1)	7/11.7/14(1)	7.2/11.9/14.2(1)	us	
/STEP cycle time	TSC	(3)	(3)	(3)	us	
/WRDATA pulse width	TWDD	100/185/225(1)	125/210/250	150/235/275(1)	ns	
Write Precompensation time		100/185/225(1)	125/210/250(1)	150/235/275(1)	ns	

(1) Refer to the data rate at 500/300/250 Kb/sec.
(2) Typical values for T = 25° C and nominal supply voltage.
(3) Programmable from 2ms through 32ms in 2ms increments.

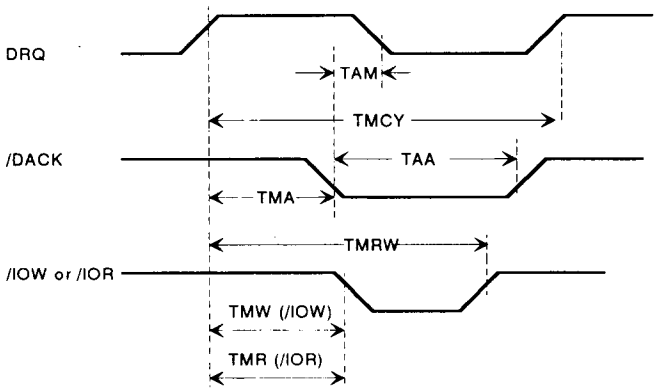
Processor Read Operation



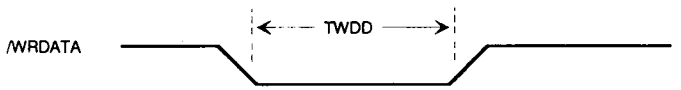
Processor Write Operation



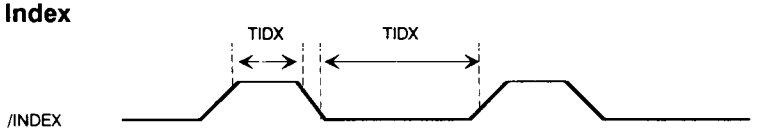
DMA Operation



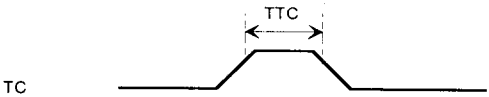
Write Data



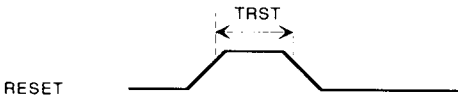
Index



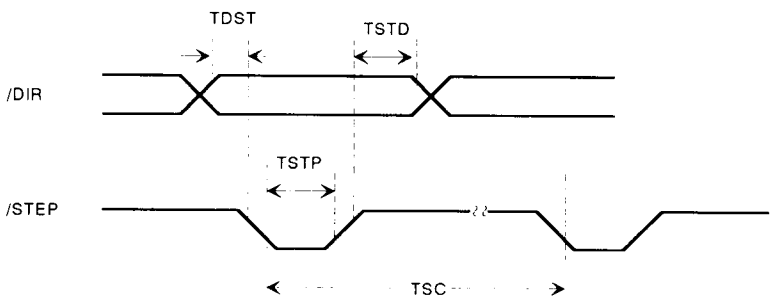
Terminal Count



Reset



Drive Seek Operation



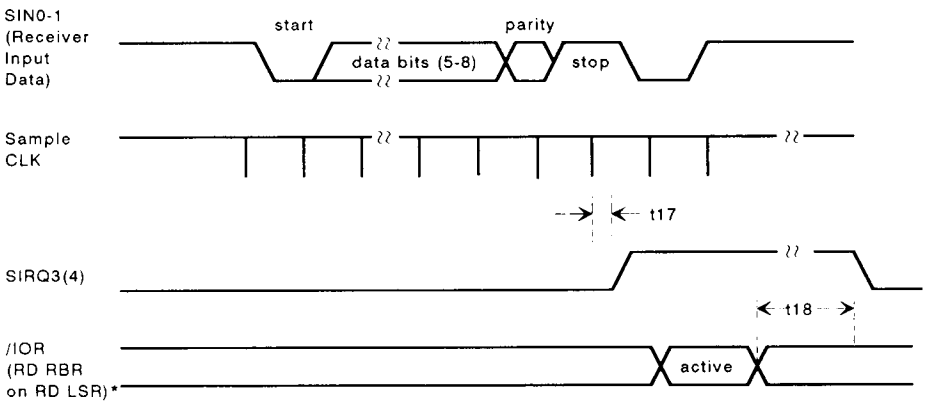
AC Specifications

Symbol	Description	Min	Max	Units
t1	Address hold time from /IOW	20		ns
t4	/IOW delay from address	60		ns
t5	/IOW strobe width	100		ns
t6	Write Cycle	360		ns
t7	Data setup time	40		ns
t8	Data hold time	40		ns
t9	Address hold time from /IOR	20		ns
t12	/IOR delay from address	60		ns
t13	/IOR strobe width	125		ns
t14	Read cycle	360		ns
t15	Delay from /IOR to data (@100 pF loading)		125	ns
t16	/IOR to floating data delay (@100 pF loading)	0	100	ns
t17	Delay from stop to set interrupt (receiver line status or received data available)		1	Receiver clock cycles
t18	Delay from /IOR (RD RBR OR RD LSR) to reset interrupt (100 pF load)		1	us
t19	Delay from initial interrupt reset to transmit start	24	40	Baud out cycles
t20	Delay from stop to interrupt (THRE)	8	8	Baud out cycles
t21	Delay from /IOW (WR THR) to reset interrupt (100 pF load)		175	ns
t22	Delay from initial write to interrupt	16	24	Baud out cycles
t23	Delay from /IOR (RD IIR) to reset interrupt (THRE) (100 pF load)		250	ns
t24	Delay from /IOW (WR MCR) to output (100 pF load)		200	ns

AC Specifications

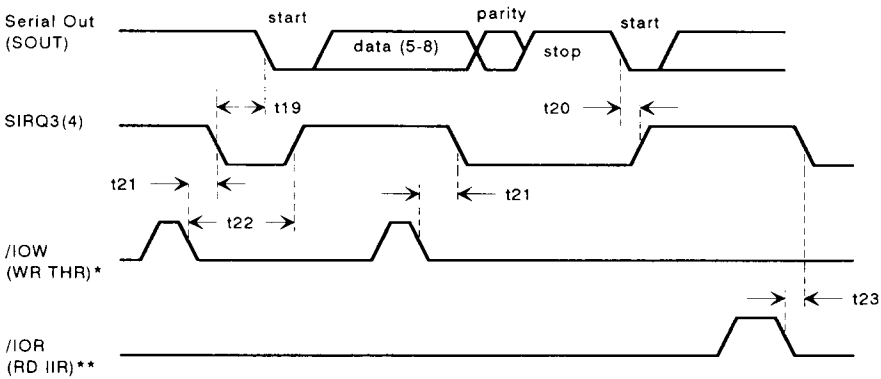
Symbol	Description	Min	Max	Units
t25	Delay to set interrupt from modem input (100 pF load)		250	ns
t63	Delay to reset interrupt from Modem input		250	ns
t26	Delay to reset interrupt from /IOR (RD MSR) (100 pF load)		250	ns
t27	Data time	1		us
t28	Strobe time	1	500	us

Receiver Timing



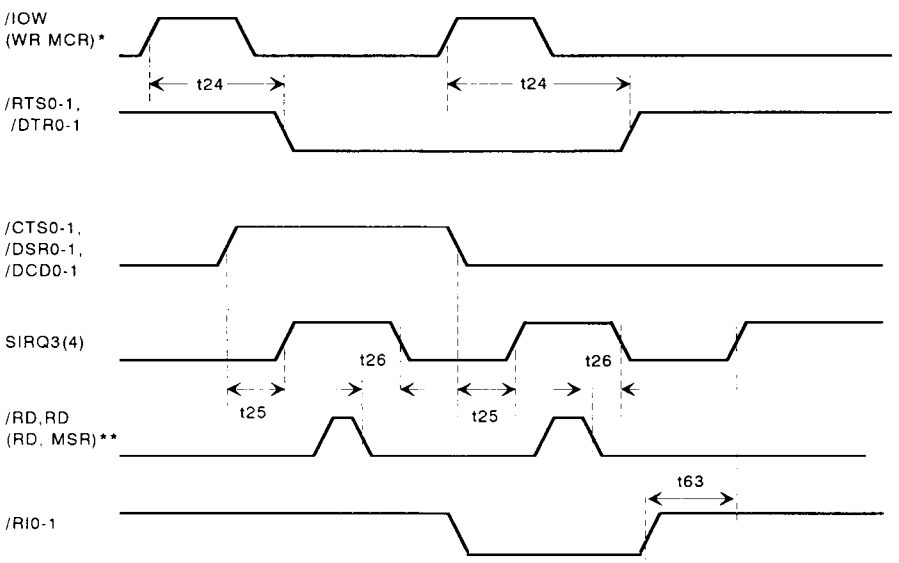
* See Read Cycle timing

Transmitter Timing



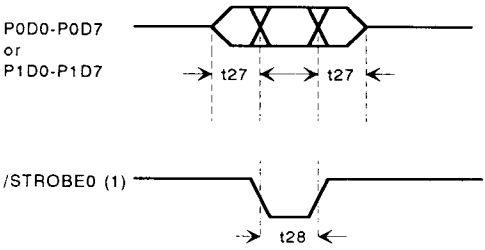
* See Write Cycle timing
** See Read Cycle timing

Modem Controls Timing



* See Write Cycle timing
** See Read Cycle timing, MSR = Modem status register

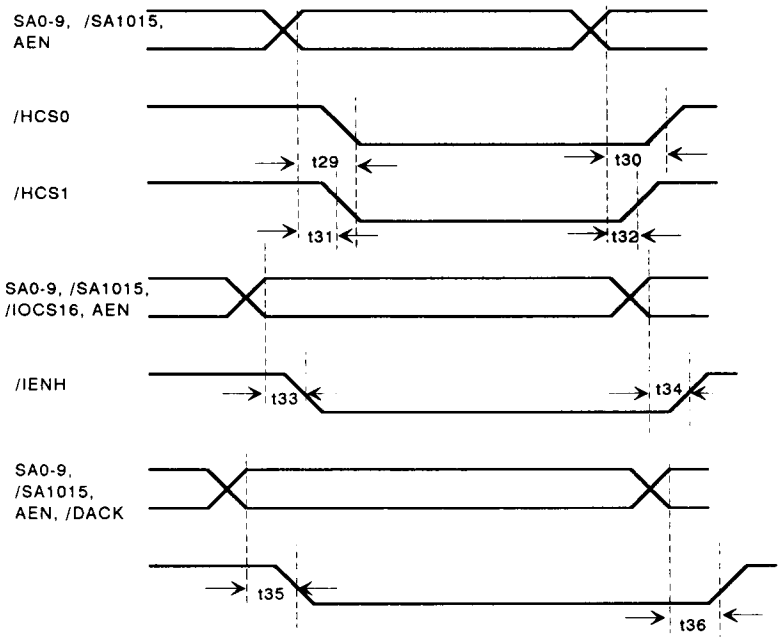
Parallel Port Timing



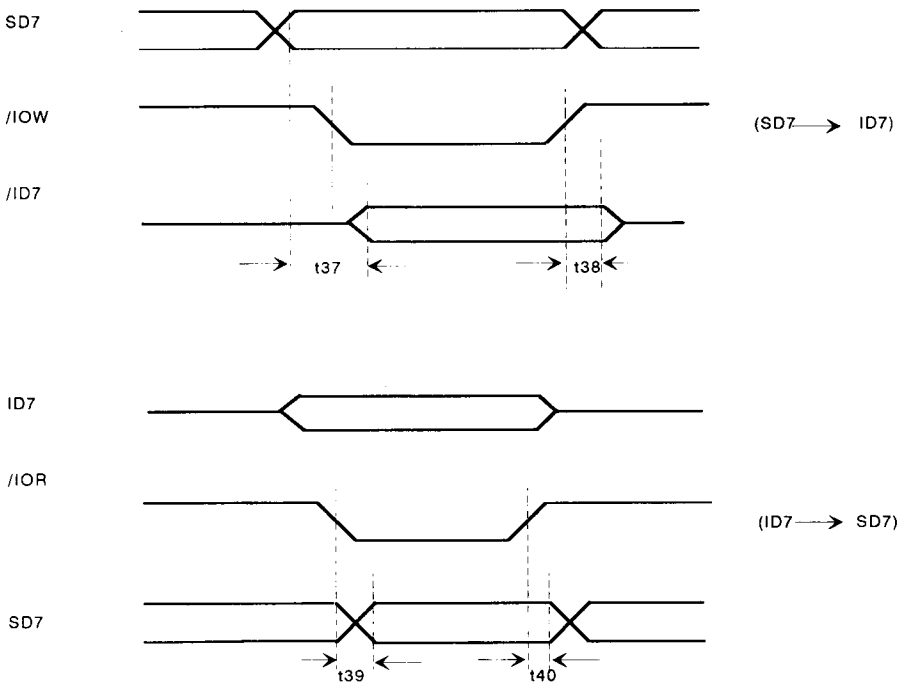
AC Specifications

Symbol	Description	Min	Max	Units
t29	/HCS0 delay from address bus	20	40	ns
t30	/HCS0 hold from address bus	15	30	ns
t31	/HCS1 delay from address bus	15	35	ns
t32	/HCS1 hold from address bus	15	25	ns
t33	/IENH and /IENL delay from AEN, IOCS16	20	45	ns
t34	/IENH and /IENL hold from AEN, IOCS16	15	30	ns
t35	/IENH and /IENL delay from address bus	20	45	ns
t36	/IENH and /IENL hold from address bus	20	40	ns
t37	Data Bus bit 7 to ID7 delay (write cycle)	15	25	ns
t38	Data Bus bit 7 to ID7 hold (write cycle)	5	7.5	ns
t39	ID7 to Data Bus bit 7 delay (read cycle)	15	30	ns
t40	ID7 to Data Bus bit 7 hold (read cycle)	7.5	12.5	ns

IDE Timing


SA0-9, /SA1015, AEN
/HCS0
/HCS1
t29
t30
t31
t32
SA0-9, /SA1015, /IOCS16, AEN
/IENH
t33
t34
SA0-9, /SA1015, AEN, /DACK
t35
t36

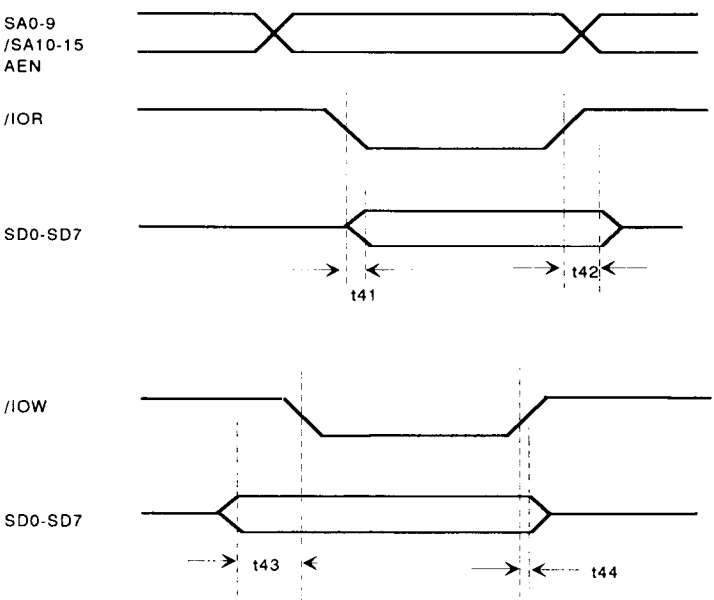
IDE Timing (continued)



AC Specifications

Symbol	Description	Min	Max	Units
t41	Data bus delay time from /IOR		35	ns
t42	Data bus hold time from /IOR	10		ns
t43	Data bus set up time from /IOW	10		ns
t44	Data bus hold time from /IOW		0	ns

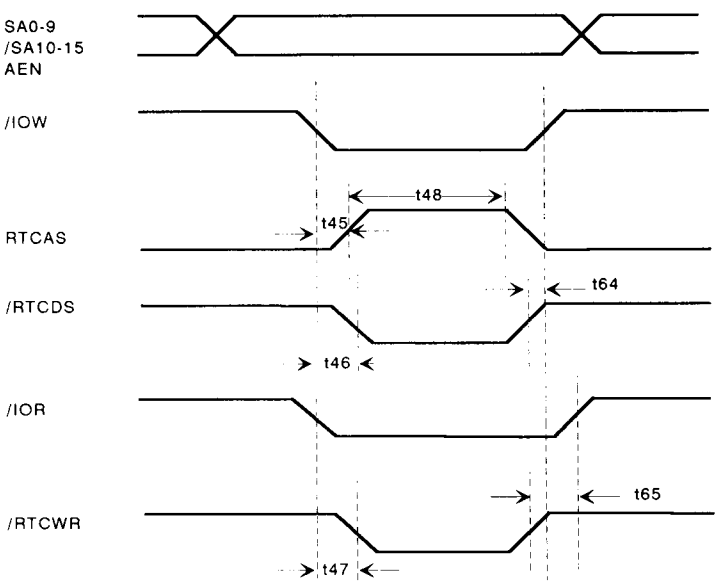
Configure Read/Write Timing



AC Specifications

Symbol	Description	Min	Max	Units
t45	RTCAS delay time from /IOW	12.5	27.5	ns
t46	/RTCDS delay time from /IOW	8	18	ns
t47	/RTCWR delay time from /IOR	8	17.5	ns
t48	RTCAS pulse duration	170	205	ns
t64	/RTCDS hold time	10		ns
t65	/RTCWR hold time	10		ns

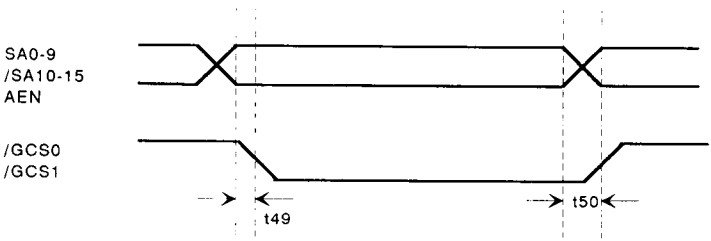
RTC Timing**



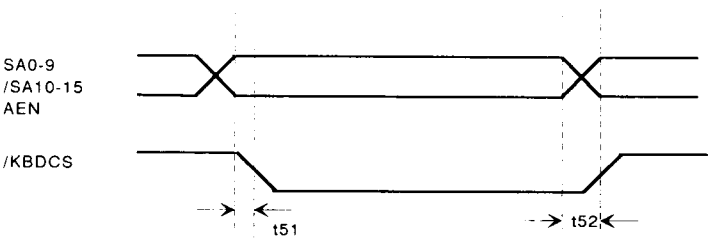
AC Specifications

Symbol	Description	Min	Max	Units
t49	/GCS0 and /GCS1 delay from address bus	12.5	27.5	ns
t50	/GCS0 and /GCS1 hold from address bus	10	17.5	ns
t51	/KBDCS delay from address bus	12.5	27.5	ns
t52	/KBDCS hold from address bus	12.5	25	ns

General Chip Select Timing**



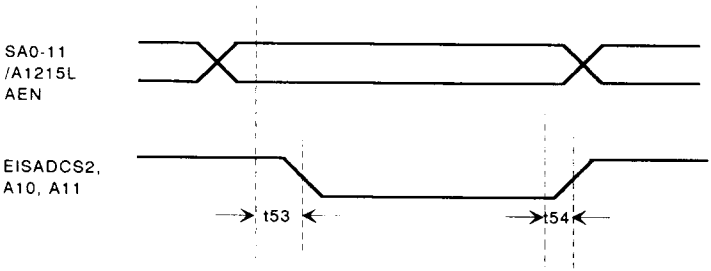
Keyboard Chip Select Timing**



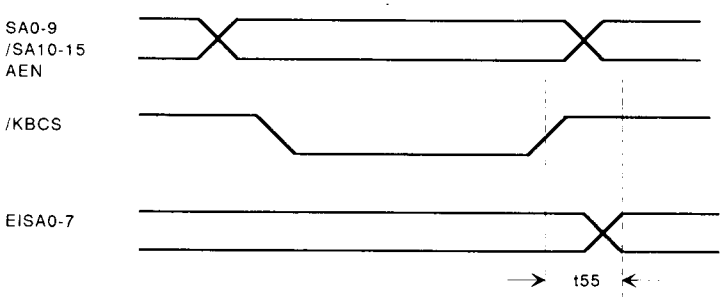
AC Specifications

Symbol	Description	Min	Max	Units
t53	/EISA IDCS delay from /IOR	12.5	30	ns
t54	/EISA IDCS hold from /IOR	10	25	ns
t55	EISA page register data hold time from address bus	10	22.5	ns
t56	/ModemCS delay from address bus	12.5	25	ns
t57	/ModemCS hold from address bus	8	17.5	ns

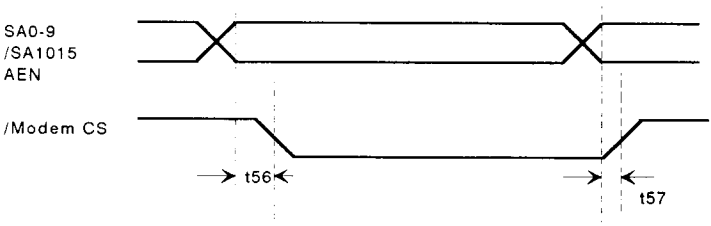
ESIA Chip Select Timing**



ESIA Page Register Output**



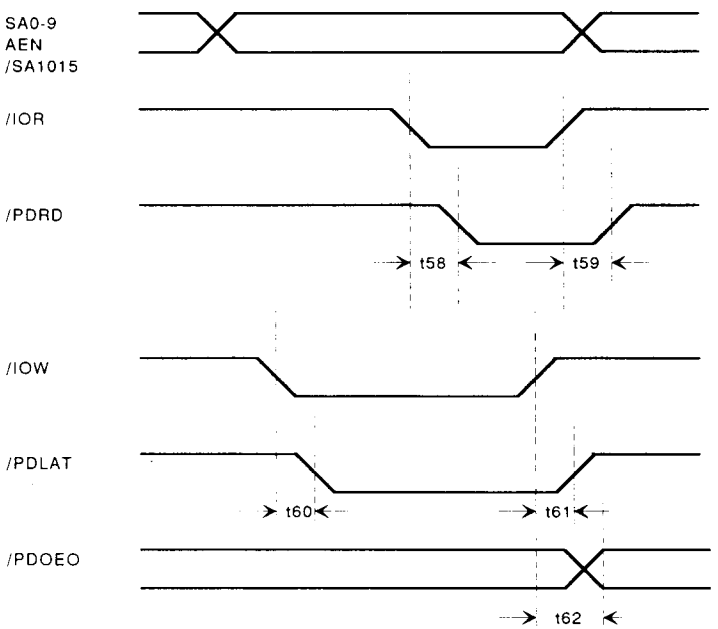
Modem Chip Select Timing**



AC Specifications

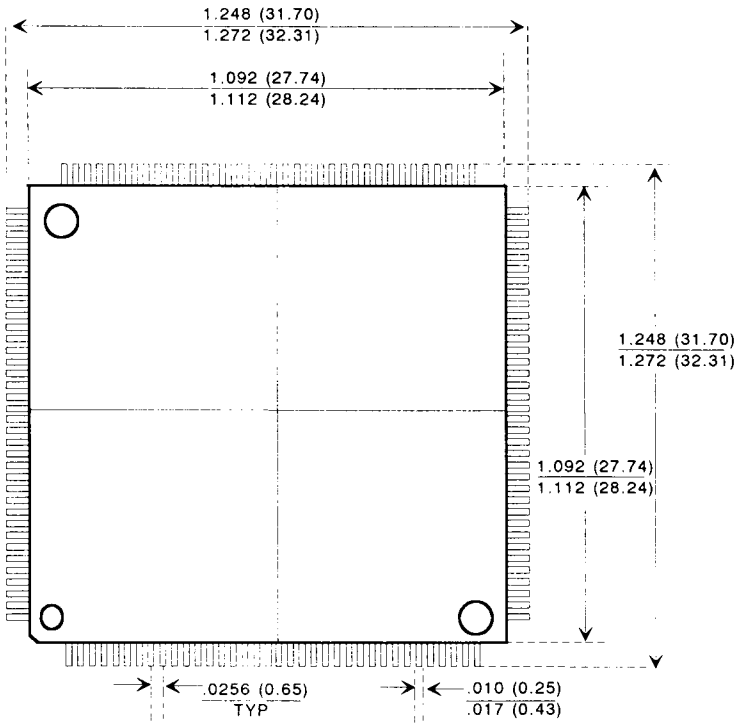
Symbol	Description	Min	Max	Units
t58	/PDRD delay from /IOR	15	22.5	ns
t59	/PDRD hold from /IOR	12.5	20	ns
t60	/PDLAT delay from /IOW	12.5	25	ns
t61	/PDLAT hold from /IOW	12	22	ns
t62	/PDOEO hold from /IOW	15	35	ns

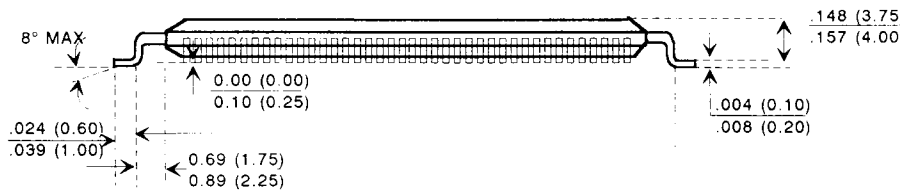
Second Parallel Port Timing**



Production Package Specification

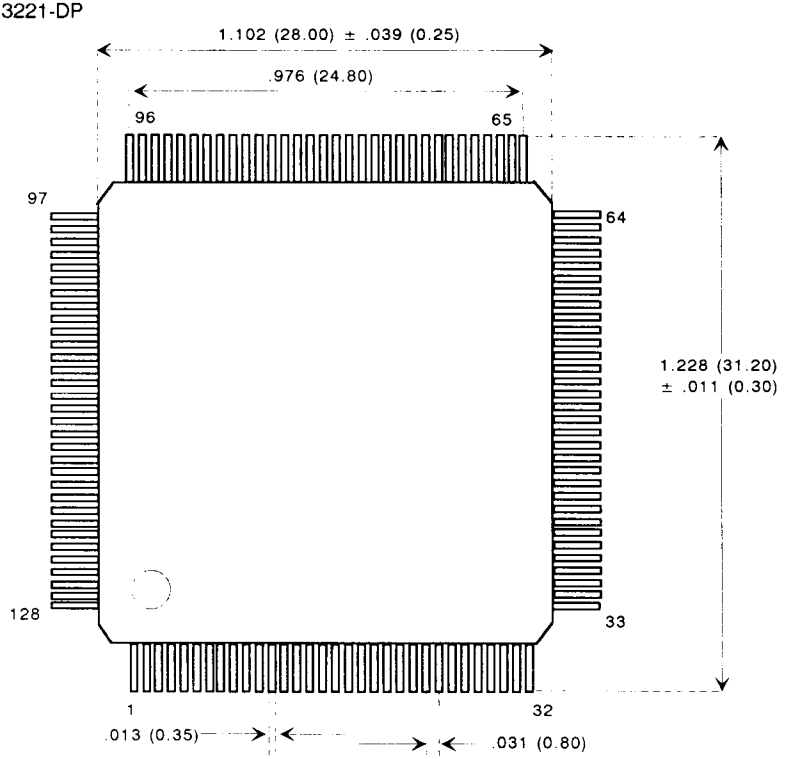
Package: 144-pin PQFP
Unit: inches (millimeters)
Chip: 3221-EP

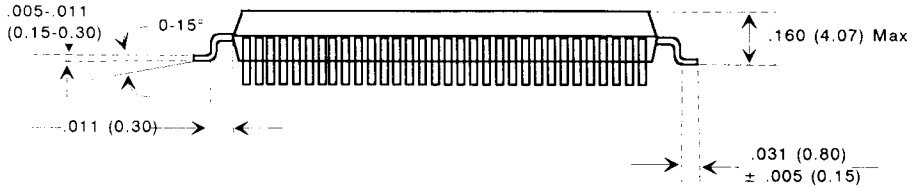




Production Package Specification

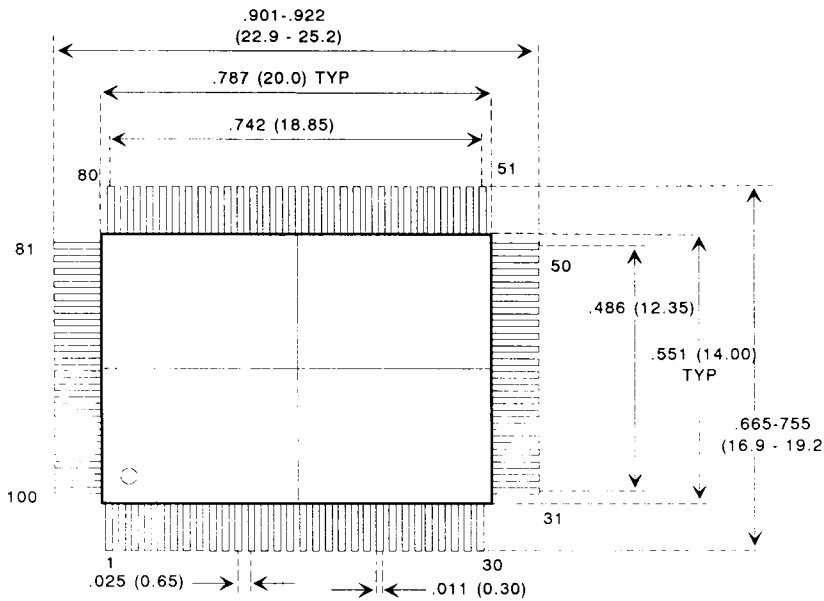
Package: 128-pin PQFP
Unit: inches (millimeters)
Chip: 3221-DP

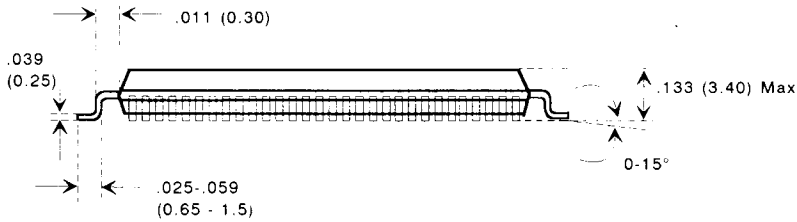




Production Package Specification

Package: 100-pin PQFP
Unit: inches (millimeters)
Chip: 3221- SP





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